TPS249x 正の高電圧電力制限、ホットスワップ・コントローラ

1 特長

- 電力制限と電流制限をプログラム可能で、完全な安全動作領域(SOA)保護を実現
- 広い動作電圧範囲: 9V～80V
- ラッチ動作(TPS2490)と自動再試行(TPS2491)
- ハイサイド駆動による低$R_{DS(on)}$の外付けNチャネルMOSFET
- プログラム可能なフォルト・タイマにより MOSFETを保護し、不都合なシャットダウンを排除
- ダウンストリームDC/DC連携のためのパワー・グッド・オープンドレイン出力
- イネーブルを使用して低電圧誤動作防止またはロジック制御をプログラム可能
- 小型で省スペースの10ピンVSSOPパッケージ
- カリキュレータ・ツールを利用可能(*TPS2490/91 デザインイン・カリキュレータ*、SLVC033)

2 アプリケーション

- サーバー・バックプレーン
- ストレージ・エリア・ネットワーク(SAN)
- 医療用システム
- プラグイン・モジュール
- 基地局

3 概要

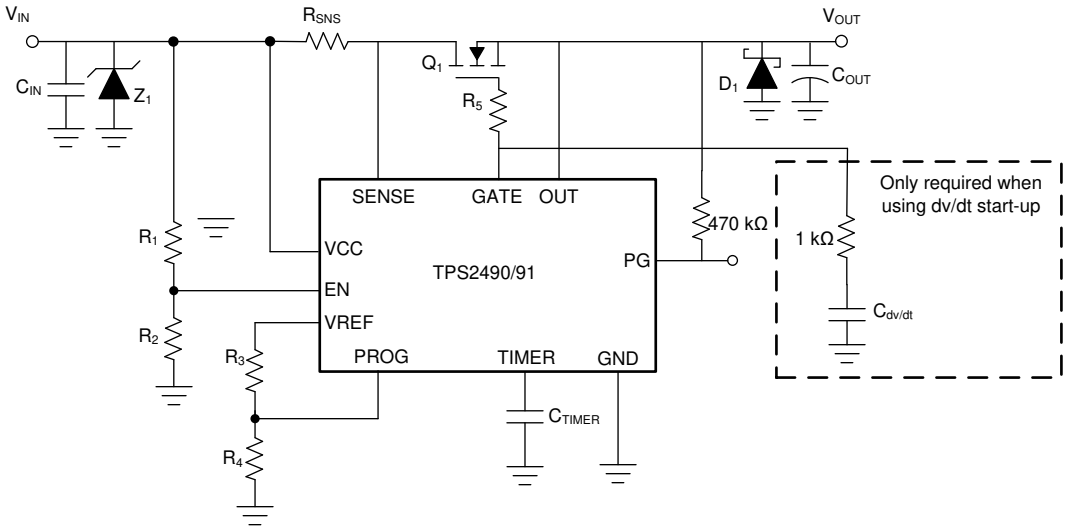
TPS249xは使いやすい、正の高電圧の10ピン・ホットスワップ電源マネージャ・デバイスで、外付けのNチャネルMOSFETスイッチを安全に駆動できます。電力制限および電流制限(どちらも変更可能で、互いに独立)により、外付けのMOSFETは最も過酷な動作状況においても、選択された安全動作領域(SOA)内で動作することが保証されます。アプリケーションとしては、突入電流制限、電子回路ブレーカ保護、負荷オンの制御、下流のDC/DCコンバータとのインターフェイス、電力フィード保護などがあります。これらのデバイスは小型で省スペースの10ピンVSSOPパッケージで利用でき、外付けデバイスの数を大幅に減らせるため、貴重な基板面積を削減できます。TPS249xには、アプリケーション・ノート、評価基板、および設計ツールが用意されています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TPS249x	VSSOP (10)	3.00mm×3.00mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

代表的なアプリケーション



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision E (February 2017) から Revision F に変更 **Page**

- Added Figure 12 ... 9

Revision D (July 2012) から Revision E に変更 **Page**

- 「*ESD定格*」表、「*熱に関する情報*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加 ... 1

Revision C (September 2011) から Revision D に変更 **Page**

- Added Operating voltage range to the RECOMMENDED OPERATING CONDITIONS table ... 5
- Changed Supply Current Disabled Test Conditions From: V_{EN} = Lo, V_{SENSE} = V_{VCC} = V_{OUT} = 0 To: V_{EN} = Lo, V_{SENSE} = V_{VCC} = V_{OUT} ... 6

Revision B (March 2010) から Revision C に変更 **Page**

- Changed Figure 15, From: I_{IN} = 5 A/div To: I_{IN} = 0.5 A/div ... 15

Revision A (March 2010) から Revision B に変更 **Page**

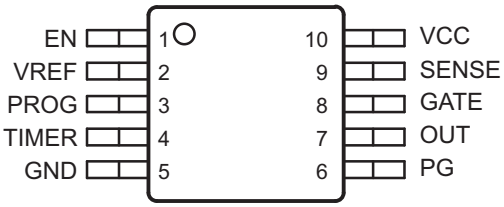
- 「特長」に「カリキュレータ・ツールを利用可能」(SLVC033)を 追加 ... 1
- Added the Gate Capacitor (dV/dt) Control section: Revised text and Equation 5 ... 17

2003年11月発行のものから更新 **Page**

- Deleted Lead temperature spec. from Abs Max Ratings table 5
- Changed V_{PROG} MIN voltage spec. from: 0 to: 0.4; added footnote (1) to the RECOMMENDED OPERATING CONDITIONS table 5
- Deleted footnote - Not tested in production from t_{F_TRIP} 7
- Added clarification sentence to the GATE pin description, regarding adding capacitance. 11
- Changed $V_{(VCC-OUT).}$ to $V_{(SENSE-OUT)}$ in the OUT pin description. 11
- Changed from: (0–4 V) to: (0.4 – 4 V) in the PROG pin description 12
- Changed from: 2.5 V to: 2.7 V in the PG pin description. 13
- Added text to the PG pin description. 13
- Changed from: $V_{(VCC–OUT)}$ to: $V_{(SENSE–OUT)}$ 14
- Added text to the Gate Capacitor (dV/dt) Control section description 17
- Added text to the High Gate Capacitance Applications section description 18
- Added The Input Bypass section description. 18

5 Pin Configuration and Functions

DGS Package
10-Pin VSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	EN	I	Device enable
2	VREF	O	Reference voltage output, used to set power threshold on PROG pin
3	PROG	I	Power-limit setting input
4	TIMER	I/O	Fault timing capacitor
5	GND	—	Ground
6	PG	O	Power good reporting output, open-drain
7	OUT	I	Output voltage feedback
8	GATE	O	Gate output
9	SENSE	I	Current-limit sense input
10	VCC	I	Supply input

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	VCC, SENSE, EN	–0.3	100	V
	OUT(2)	–1	100	V
	PROG	–0.3	6	V
Output voltage	GATE, PG	–0.3	100	V
	TIMER, VREF	–0.3	6	V
Sink current	PG		10	mA
	PROG		2	mA
Source current	VREF	0	2	mA
Maximum junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) OUT will withstand transients to –2 V for 1 ms or less.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{VCC}	Input voltage	9		80	V
V_{PROG}	Input voltage	0.4(1)		4	V
V_{OUT}	Operating voltage	0		80	V
I_{VREF}	Operating current range (sourcing), V_{REF}	0		1	mA
T_J	Operating junction temperature	–40		125	°C
T_A	Operating free-air temperature	–40		85	°C

(1) V_{PROG} may be set below this minimum with reduced accuracy.

6.4 Thermal Information

THERMAL METRIC(1)		TPS2490 TPS2491 DGS (VSSOP) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	164.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	85.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	84.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

unless otherwise noted, minimum and maximum limits apply across the recommended operating junction temperature and voltage range, V_{TIMER} = 0 V, and all outputs unloaded; typical specifications are at T_J = 25°C, V_{VCC} = 48 V, V_{TIMER} = 0 V, and all outputs unloaded; positive currents are into pins.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT (VCC)						
	Enabled	V_{EN} = Hi, V_{SENSE} = V_{OUT} = V_{VCC}		450	1000	µA
	Disabled	V_{EN} = Lo, V_{SENSE} = V_{VCC} = V_{OUT}		90	250	µA
CURRENT SENSE INPUT (SENSE)						
I_{SENSE}	Input bias current	V_{SENSE} = V_{VCC}, V_{OUT} = V_{VCC}		7.5	20	µA
REFERENCE VOLTAGE OUTPUT (VREF)						
V_{REF}	Reference voltage	0 < I_{VREF} < 1 mA	3.9	4	4.1	V
POWER LIMITING INPUT (PROG)						
I_{PROG}	Input bias current, device enabled, sourcing or sinking	0 < V_{PROG} < 4 V, V_{EN} = 48 V			5	µA
R_{PROG}	Pulldown resistance, device disabled	I_{PROG} = 200 µA, V_{EN} = 0 V		375	600	Ω
POWER LIMITING AND CURRENT LIMITING (SENSE)						
V_{CL}	Current sense threshold $V_{(VCC-SENSE)}$ with power limiting trip	V_{PROG} = 2.4 V, V_{OUT} = 0 V or V_{PROG} = 0.9 V, V_{OUT} = 30 V, V_{VCC} = 48 V	17	25	33	mV
V_{SENSE}	Current sense threshold $V_{(VCC-SENSE)}$ without power limiting trip	V_{PROG} = 4 V, V_{SENSE} = V_{OUT}	45	50	55	mV
TIMER OPERATION (TIMER)						
	Charge current (sourcing)	V_{TIMER} = 0 V	15	25	34	µA
		V_{TIMER} = 0 V, T_J = 25°C	20	25	30	µA
	Discharge current (sinking)	V_{TIMER} = 5 V	1.5	2.5	3.7	µA
		V_{TIMER} = 5 V, T_J = 25°C	2.1	2.5	3.1	µA
	TIMER upper threshold voltage		3.9	4	4.1	V
	TIMER lower reset threshold voltage	TPS2491 only	0.96	1	1.04	V
D_{RETRY}	Fault retry duty cycle	TPS2491 only	0.5%	0.75%	1%	
GATE DRIVE OUTPUT (GATE)						
I_{GATE}	GATE sourcing current	V_{SENSE} = V_{VCC}, $V_{(GATE-OUT)}$ = 7 V, V_{EN} = Hi	15	22	35	µA
	GATE sinking current	V_{EN} = Lo, V_{GATE} = V_{VCC}	1.8	2.4	2.8	mA
		V_{EN} = Hi, V_{GATE} = V_{VCC}, $V_{(VCC-SENSE)}$ ≥ 200 mV	75	125	250	mA
	GATE output voltage, $V_{(GATE-OUT)}$		12		16	V
POWER GOOD OUTPUT (PG)						
V_{PG_L}	Low voltage (sinking)	I_{PG} = 2 mA		0.1	0.25	V
		I_{PG} = 4 mA		0.25	0.5	V
V_{PGTL}	PG threshold voltage, V_{OUT} rising, PG goes open drain	V_{SENSE} = V_{VCC}, measure $V_{(VCC-OUT)}$	0.8	1.25	1.7	V
VPGTH	PG threshold voltage, V_{OUT} falling, PG goes low	V_{SENSE} = V_{VCC}, measure $V_{(VCC-OUT)}$	2.2	2.7	3.2	V
ΔV_{PGT}	PG threshold hysteresis voltage, $V_{(SENSE-OUT)}$	V_{SENSE} = V_{VCC}		1.4		V
	Leakage current, PG false, open drain				10	µA
OUTPUT VOLTAGE FEEDBACK INPUT (OUT)						
I_{OUT}	Bias current	V_{OUT} = V_{VCC}, V_{EN} = Hi, sinking		8	20	µA
		V_{OUT} = GND, V_{EN} = Lo, sourcing		18	40	µA

Electrical Characteristics (continued)

unless otherwise noted, minimum and maximum limits apply across the recommended operating junction temperature and voltage range, V_{TIMER} = 0 V, and all outputs unloaded; typical specifications are at T_J = 25°C, V_{VCC} = 48 V, V_{TIMER} = 0 V, and all outputs unloaded; positive currents are into pins.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ENABLE INPUT (EN)						
V_{EN_H}	Threshold, V_{EN} going high		1.32	1.35	1.38	V
V_{EN_L}	Threshold, V_{EN} going low		1.22	1.25	1.28	V
	V_{EN} hysteresis			100		mV
	Leakage current	V_{EN} = 48 V			1	µA
INPUT SUPPLY UVLO (VCC)						
	V_{VCC} turn on	Rising		8.4	8.8	V
	V_{VCC} turn off	Falling	7.5	8.3		V
	Hysteresis			75		mV

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER LIMITING AND CURRENT LIMITING (SENSE)						
t_{F_TRIP}	Large overload response time to GATE low	V_{PROG} = 4 V, V_{OUT} = V_{SENSE}, $V_{(VCC-SENSE)}$: 0 → 200 mV, $C_{(GATE-OUT)}$ = 2 nF, $V_{(GATE-OUT)}$ = 1 V			1.2	µs
GATE DRIVE OUTPUT (GATE)						
t_{D_ON}	Propagation delay: EN going true to GATE output high	V_{EN} = 0 → 2.5 V, 50% of V_{EN} to 50% of V_{GATE}, V_{OUT} = V_{VCC}, $R_{(GATE-OUT)}$= 1 MΩ		25	40	µs
t_{D_OFF}	Propagation delay: EN going false (0 V) to GATE output low	V_{EN} = 2.5 V → 0, 50% of V_{EN} to 50% of V_{GATE}, V_{OUT} = V_{VCC}, $R_{(GATE-OUT)}$= 1 MΩ, t_{FALL} < 0.1 µs		0.5	1	µs
	Propagation delay: TIMER expires to GATE output low	V_{TIMER}: 0 → 5 V, t_{RISE} < 0.1 µs, 50% of V_{TIMER} to 50% of V_{GATE}, V_{OUT} = V_{VCC}, $R_{(GATE-OUT)}$ = 1 MΩ,		0.8	1	µs
POWER GOOD OUTPUT (PG)						
t_{DPG}	PG deglitch delay, detection to output, rising and falling edges	V_{SENSE} = V_{VCC}	5	9	15	ms

6.7 Typical Characteristics

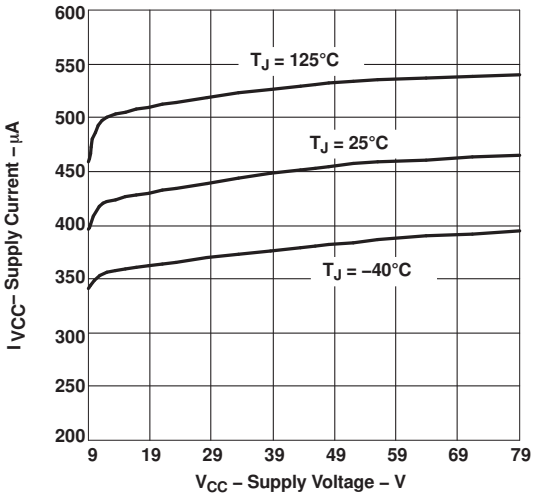


Figure 1. Supply Current vs Supply Voltage

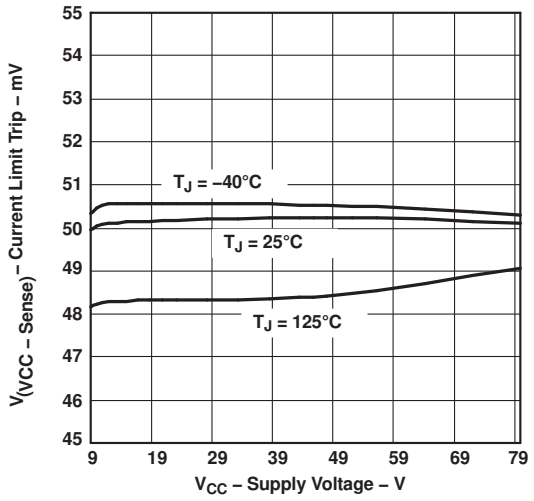


Figure 2. Current Limit Trip vs Supply Voltage

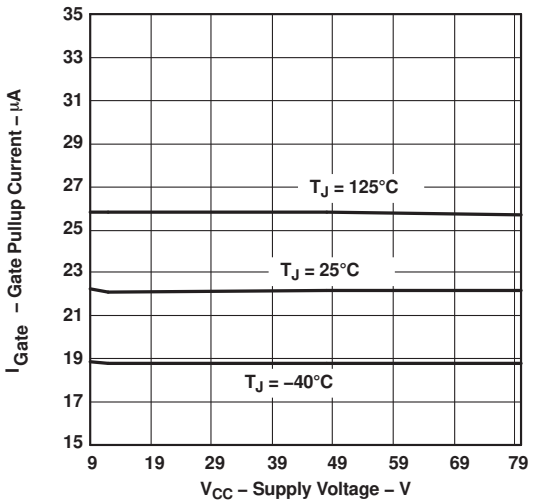


Figure 3. Gate Pullup Current vs Supply Voltage

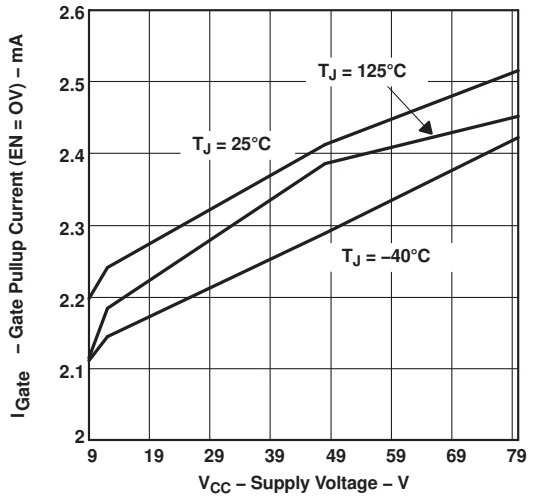


Figure 4. Gate Pulldown Current (EN = 0 V) vs Supply Voltage

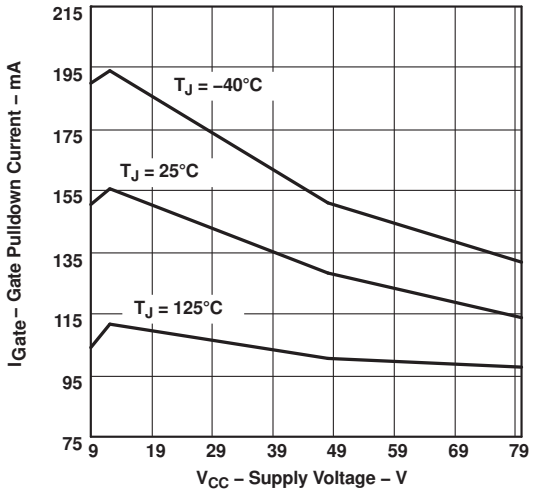


Figure 5. Gate Pulldown Current vs Supply Voltage (EN = 4 V, V(VCC – Sense) = 200 mV)

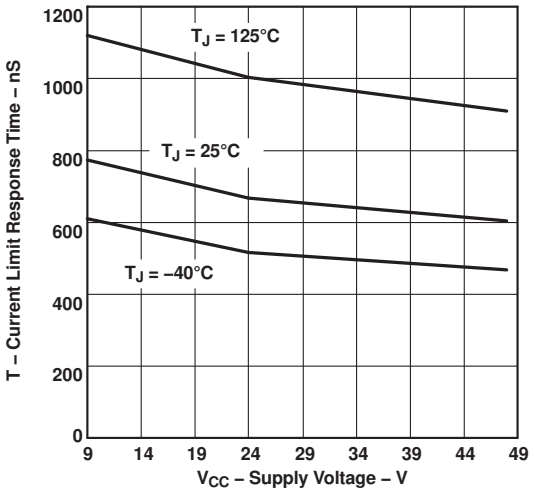


Figure 6. Current Limit Response Time vs Supply Voltage (EN = 4 V, V(VCC – Sense) = 200 mV)

Typical Characteristics (continued)

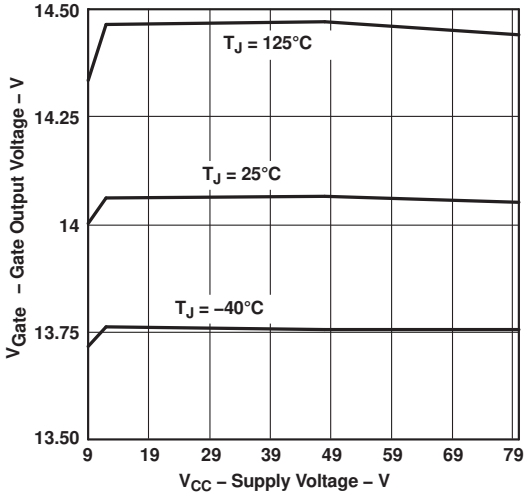


Figure 7. Gate Output Voltage vs Supply Voltage

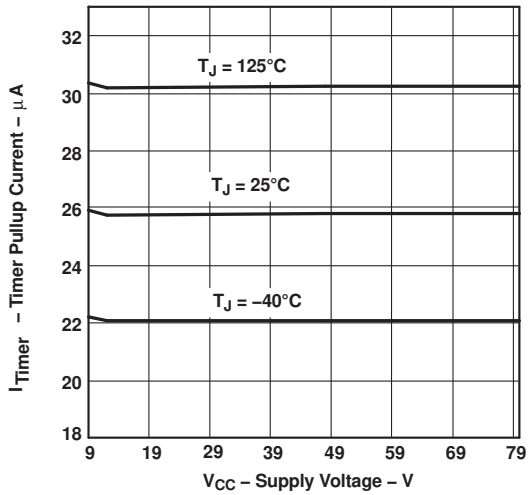


Figure 8. Timer Pullup Current vs Supply Voltage

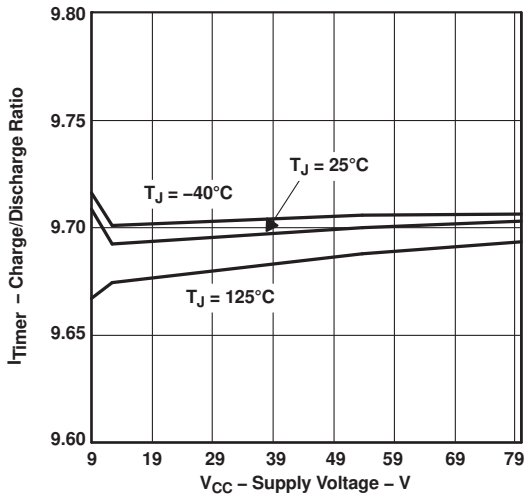


Figure 9. Timer Charge/Discharge Ratio vs Supply Voltage and Temperature

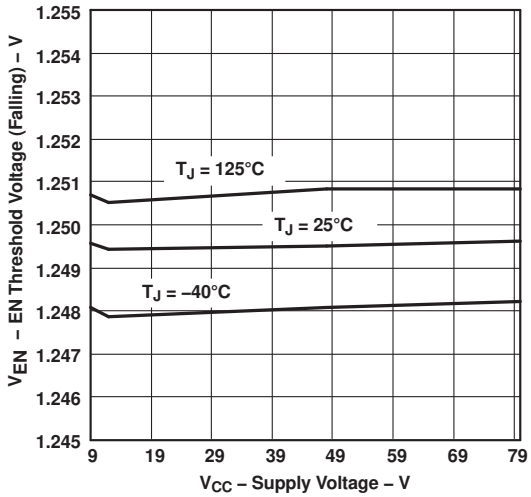


Figure 10. EN Threshold Voltage (Falling) vs Supply Voltage

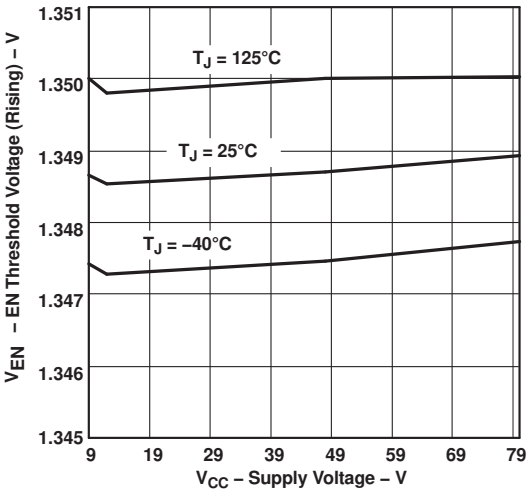


Figure 11. EN Threshold Voltage (Rising) vs Supply Voltage

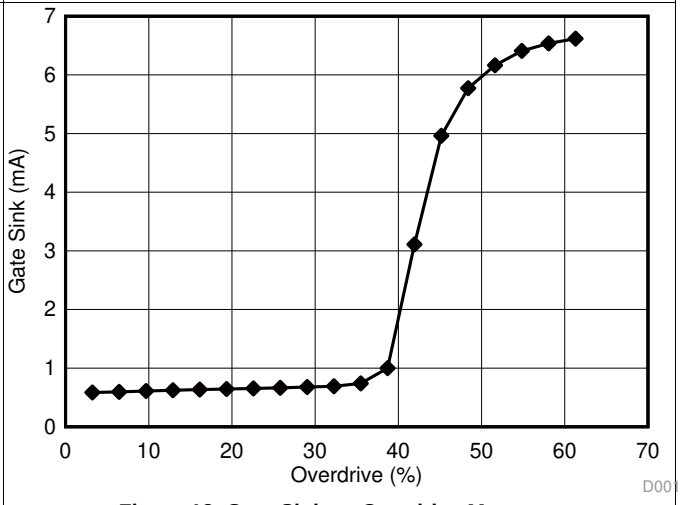


Figure 12. Gate Sink vs Overdrive Measurements

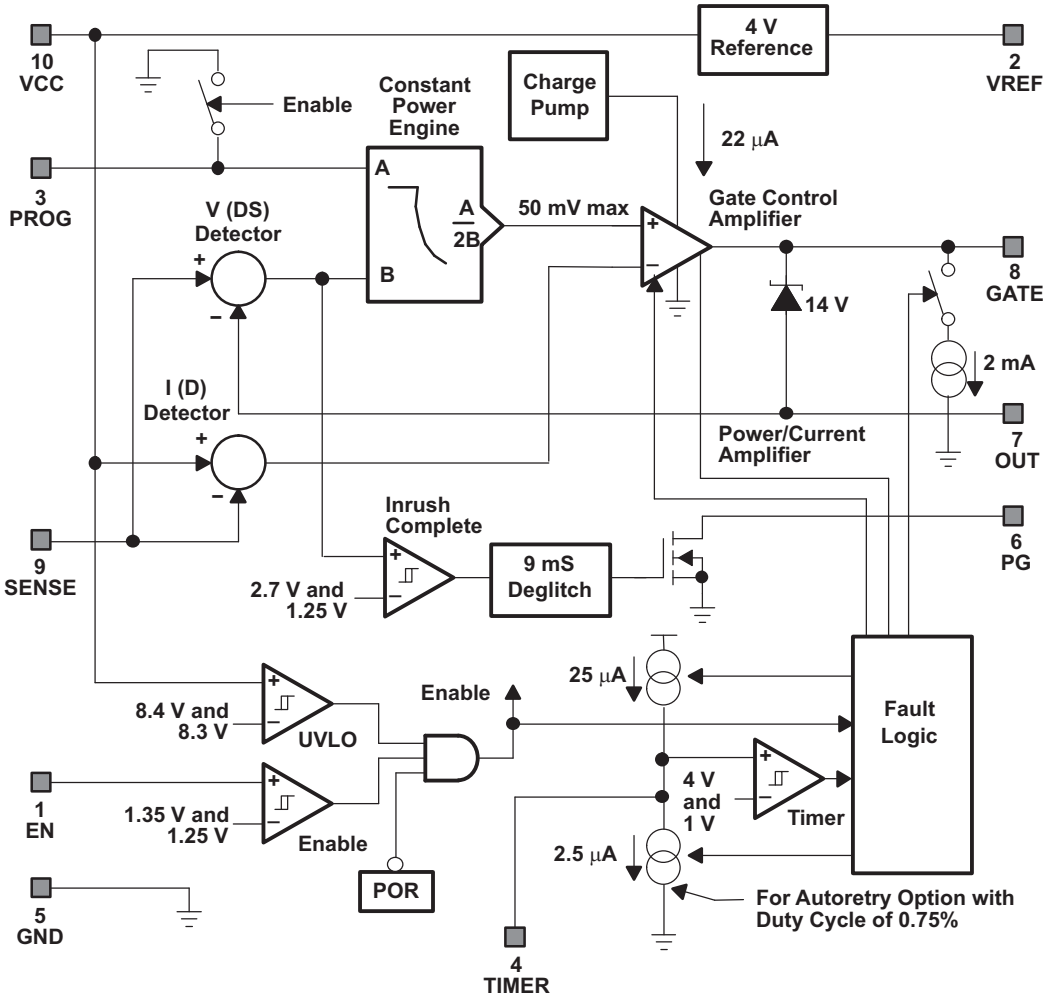
7 Detailed Description

7.1 Overview

The inline protection functionality of the TPS2490 is designed to control the inrush current to the load upon insertion of a circuit card into a live backplane or other hot power source, thereby limiting the voltage sag on the backplane's supply voltage and the dV/dt of the voltage applied to the load. Effects on other circuits in the system are minimized, preventing possible unintended resets. A controlled shutdown when the circuit card is removed can also be implemented using the TPS2490.

In addition to a programmable current limit, the TPS2490 monitors and limits the maximum power dissipation in the series pass device to maintain operating within the device Safe Operating Area (SOA). Either current limiting or power limiting for an extended period of time results in the shutdown of the series pass device. In this event, the TPS2490 will latch off while the TPS2491 will retry an infinite number of timer to recover after the fault is removed. Programmable EN circuit shuts down the TPS2490 when the system input voltage falls below the desired operating range.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 VCC

This pin is associated with three functions:

1. Biasing power to the integrated circuit
2. Input to power on reset (POR) and undervoltage lockout (UVLO) functions
3. Voltage sense at one terminal of R_S for Q1 current measurement

The voltage must exceed the POR (about 6 V for approximately 400 µs) and the internal UVLO (about 8 V) before normal operation (driving the GATE) may begin. Connections to VCC should be designed to minimize R_S voltage sensing errors and to maximize the effect of C1 and Z1; place C1 at R_S rather than at the IC pin to eliminate transient sensing errors. GATE, PROG, PG, and TIMER are held low when either UVLO or POR are active.

7.3.2 SENSE

Monitors the voltage at the drain of Q1, and the downstream side of R_S providing the constant power limit engine with feedback of both Q1 current (I_D) and voltage (V_{DS}). Voltage is determined by the difference between SENSE and OUT, while the current analog is the difference between VCC and SENSE. The constant power engine uses V_{DS} to compute the allowed I_D and is clamped to 50 mV, acting like a traditional current limit at low V_{DS}. The current limit is set by Equation 1:

$$I_{LIM} = \frac{50\ mV}{R_S} \tag{1}$$

Design the connections to SENSE to minimize R_S voltage sensing errors. Don't drive SENSE to a large voltage difference from VCC because it is internally clamped to VCC. The current limit function can be disabled by connecting SENSE to VCC.

7.3.3 GATE

Provides the high side (above VCC) gate drive for Q1. It is controlled by the internal gate drive amplifier, which provides a pull-up of 22 µA from an internal charge pump and a strong pulldown to ground of 75 mA (minimum). The pulldown current is a nonlinear function of the amplifier overdrive; it provides small drive for small overloads, but large overdrive for fast reaction to an output short. There is a separate pull-down of 2 mA to shut Q1 off when EN or UVLO cause this to happen. An internal clamp protects the gate of Q1 (to OUT) and generally eliminates the need for an external clamp in almost all cases for devices with 20-V $V_{GS(MAX)}$ ratings; an external Zener may be required to protect the gate of devices with $V_{GS(MAX)}$ < 16 V. A small series resistance (R5) of 10 Ω must be inserted in the gate lead if the C_{ISS} of Q1 > 200 pF, otherwise use 33 Ω for small MOSFETs.

A capacitor can be connected from GATE to ground to create a slower inrush with a constant current profile without affecting the amplifier stability. Add a series resistor of about 1 kΩ to the gate capacitor to maintain the gate clamping and current limit response time. Adding capacitance across Q1 gate to source requires some series damping resistance to avoid high-frequency oscillations.

7.3.4 OUT

This input pin is used by the constant power engine and the PG comparator to measure V_{DS} of Q1 as $V_{(SENSE-OUT)}$. Internal protection circuits leak a small current from this pin when it is low. If the load circuit can drive OUT below ground, connect a clamp (or freewheel) diode such as an S1B from OUT (cathode) to GND (anode).

7.3.5 EN

The GATE driver is enabled if the positive threshold is exceeded and the internal POR and UVLO thresholds have been satisfied. EN can be used as a logic control input, an analog input voltage monitor as illustrated by R1/R2 in the Figure 18 circuit, or it can be tied to VCC to always enable the TPS249x. The hysteresis associated with the internal comparator makes this a stable method of detecting a low input condition and shutting the downstream circuits off. A TPS2490 that has latched off can be reset by cycling EN below its negative threshold and back high.

Feature Description (continued)

7.3.6 VREF

Provides a 4-V reference voltage for use in conjunction with R3/R4 of the typical application circuit to set the voltage on the PROG pin. The reference voltage is available once the internal POR and UVLO thresholds have been met. It is not designed as a supply voltage for other circuitry, therefore ensure that no more than 1 mA is drawn. Bypass capacitance is not required, but if a special application requires one, less than 1000 pF can be placed on this pin.

7.3.7 PROG

The voltage applied to this pin (0.4 to 4 V) programs the power limit used by the constant power engine. Normally, a resistor divider R3/R4 is connected from VREF to PROG to set the power limit according to Equation 2:

$$V_{PROG} = \frac{P_{LIM}}{10 \times I_{LIM}} \quad (2)$$

where

- P_{LIM} is the desired power limit of Q1
- I_{LIM} is the current limit setpoint (see SENSE).

P_{LIM} is determined by the desired thermal stress on Q1:

$$P_{LIM} < \frac{T_{J(MAX)} - T_{S(MAX)}}{R_{\theta JC(MAX)}} \quad (3)$$

where

- $T_{J(MAX)}$ is the maximum desired transient junction temperature of Q1
- $T_{S(MAX)}$ is the maximum case temperature prior to a start or restart.

V_{PROG} is used in conjunction with V_{DS} to compute the (scaled) current, $I_{D\_ALLOWED}$, by the constant power engine. $I_{D\_ALLOWED}$ is compared by the gate amplifier to the actual I_D, and used to generate a gate drive. If $I_D < I_{D\_ALLOWED}$, the amplifier turns the gate of Q1 fully on because there is no overload condition; otherwise GATE is regulated to maintain the $I_D = I_{D\_ALLOWED}$ relationship.

A capacitor may be tied from PROG to ground to alter the natural constant power inrush current shape. If properly designed, the effect is to cause the leading step of current in Figure 13 to look like a ramp.

PROG is internally pulled to ground whenever EN, POR, or UVLO are not satisfied or the TPS2490 is latched off. This feature serves to discharge any capacitance connected to the pin. Do not apply voltages greater than 4 V to PROG. If the constant power limit is not used, PROG should be tied to VREF through a 47-kΩ resistor.

7.3.8 TIMER

An integrating capacitor, C_T, connected to the TIMER pin provides a timing function that controls the fault-time for both versions and the restart interval for the TPS2491. The timer charges at 25 µA whenever the TPS249x is in power limit or current limit and discharges at 2.5 µA otherwise. The charge-to-discharge current ratio is constant with temperature even though there is a positive temperature coefficient to both. If TIMER reaches 4 V, the TPS2490 pulls GATE to ground, latch off, and discharge C_T. The TPS2491 pulls GATE to ground and attempt a restart (reenable GATE) after a timing sequence consisting of discharging C_T down to 1 V followed by 15 more charge and discharge cycles. The TPS2490 can be reset by either cycling the EN pin or the UVLO (for example, power cycling). TIMER discharges when EN is low or UVLO or POR are active. The TIMER pin should be tied to ground if this feature is not used.

Feature Description (continued)

7.3.9 PG

This open-drain output is intended to interface to downstream DC/DC converters or monitoring circuits. PG goes open drain (high voltage with a pullup) after V_{DS} of Q1 has fallen to about 1.25 V and a 9-ms deglitch time period has elapsed. PG is false (low or low resistance to ground) whenever V_{DS} of Q1 has not been less than 1.25 V, V_{DS} of Q1 is above 2.7 V, or UVLO is active. Both V_{DS} rising and falling are deglitched while entering UVLO sets PG low immediately. PG can also be viewed as having an input and output voltage monitor function. The 9-ms deglitch circuit operates to filter short events that could cause PG to go inactive (low) such as a momentary overload or input voltage step. V_{PG} voltage can be greater than V_{VCC} because it's ESD protection is only with respect to ground.

7.3.10 GND

This pin is connected to system ground.

7.4 Device Functional Modes

The TPS249x devices provide all the features needed for a positive hot swap controller. These features include:

1. undervoltage lockout (UVLO)
2. adjustable (system-level) enable
3. turnon inrush limit
4. high-side gate drive for an external N-channel MOSFET
5. MOSFET protection (power limit and current limit)
6. adjustable overload timeout—also called an electronic circuit breaker
7. charge-complete indicator for downstream converter coordination
8. an optional automatic restart mode

The TPS249x devices feature superior power-limiting MOSFET protection that allows independent control of current limit (to set maximum full-load current), power limit (to control junction temperature rise), and overload time (to control case temperature rise).

The typical application circuit, and oscilloscope plots of Figure 13 through Figure 17 demonstrate many of the functions described *Device Functional Modes*.

7.4.1 Board Plug-In (Figure 13)

Only the bypass capacitor charge current and small bias currents are evident when a board is first plugged in. The TPS249x is held inactive, and GATE, PROG, TIMER, and PG are held low for less than 1 ms while internal voltages stabilize. A start-up cycle is ready to take place after the stabilization.

GATE, PROG, TIMER, and PG are released after stabilization in this example because both the internal UVLO threshold and the external EN (enable) thresholds have been exceeded. The part begins sourcing current from the GATE pin and Q1 begins to turn on while the voltage across it, $V_{(SENSE–OUT)}$, and current through it, $V_{(VCC–SENSE)}$, are monitored. Current initially rises to the value which satisfies the power limit engine ($P_{LIM} \div V_{VCC}$) since the output capacitor was discharged.

7.4.2 TIMER and PG Operation (Figure 13)

The TIMER pin charges C_T as long as limiting action continues, and discharges at a 1/10 charge rate when limiting stops. If the voltage on C_T reaches 4 V before the output is charged, Q1 is turned off and either a latch-off or restart cycle commences, depending on the part type. The open-drain PG output provides a deglitched end-of-charge indication which is based on the voltage across Q1. PG is useful for preventing a downstream DC/DC converter from starting while C_O is still charging. PG goes active (open drain) about 9 ms after C_O is charged. This delay allows Q1 to fully turn on and any transients in the power circuits to end before the converter starts up. The resistor pullup shown on pin PG in *代表的なアプリケーション* only demonstrates operation; the actual connection to the converter depends on the application. Timing can appear to terminate early in some designs if operation transitions out of the power limit mode into a gate charge limited mode at low V_{DS} values.

Device Functional Modes (continued)

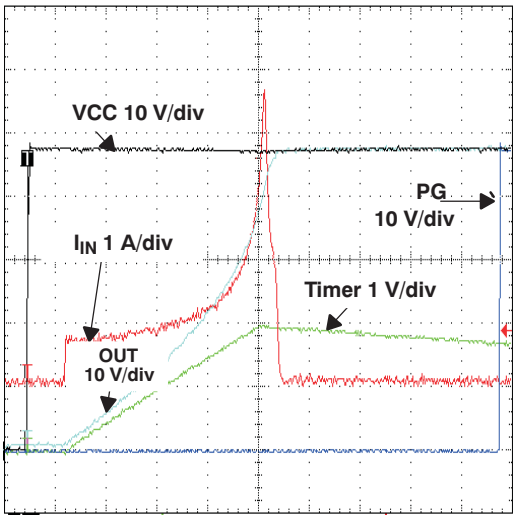


Figure 13. Basic Board Insertion

7.4.3 Action of the Constant Power Engine (Figure 14)

The calculated power dissipated in Q1, $V_{DS} \times I_D$, is computed under the same startup conditions as Figure 13 . The current of Q1, labeled I_{IN}, initially rises to the value that satisfies the constant power engine; in this case it is 34 W ÷ 48 V = 0.7 A. The 34 W value is programmed into the engine by setting the PROG voltage using Equation 2 given in the *PROG*. V_{DS} of Q1, which is calculated as $V_{(SENSE–OUT)}$, falls as C_O charges, thus allowing the Q1 drain current to increase. This is the result of the internal constant power engine adjusting the current limit reference to the GATE amplifier as C_O charges and V_{DS} falls. The calculated device power in Figure 14, labeled FET PWR, is seen to be flat-topped and constant within the limitations of circuit tolerance and acquisition noise. A fixed current limit is implemented by clamping the constant power engine's output to 50 mV when V_{DS} is low. This protection technique can be viewed as a specialized form of foldback limiting; the benefit over linear foldback is that it yields the maximum output current from a device over the full range of V_{DS} and still protects the device.

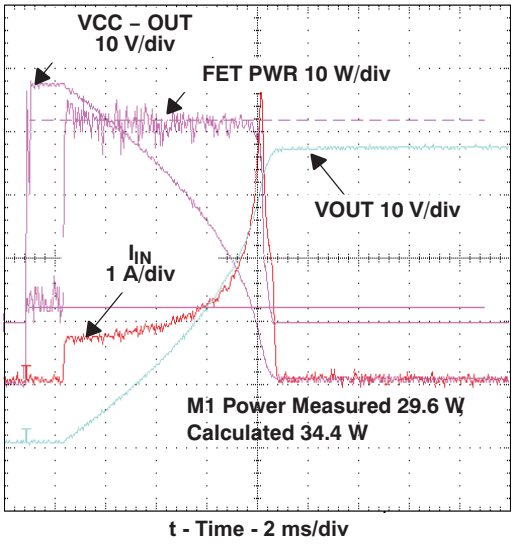


Figure 14. Computation of Q1 Stress During Startup

Device Functional Modes (continued)

7.4.4 Response to a Hard Output Short (Figure 15 and Figure 16)

Figure 15 shows the short circuit response over the full time-out period. The period begins when the output voltage falls and ends when Q1 is turned off. Q1 current is actively controlled by the constant power engine and gate amplifier circuit while the TIMER pin charges C_T to the 4-V threshold causing Q1 to be turned off. The TPS2490 latches off after the threshold is reached until either the input voltage drops below the UVLO threshold or EN cycles through the false (low) state. The TPS2491 goes through a timing sequence before attempting a restart.

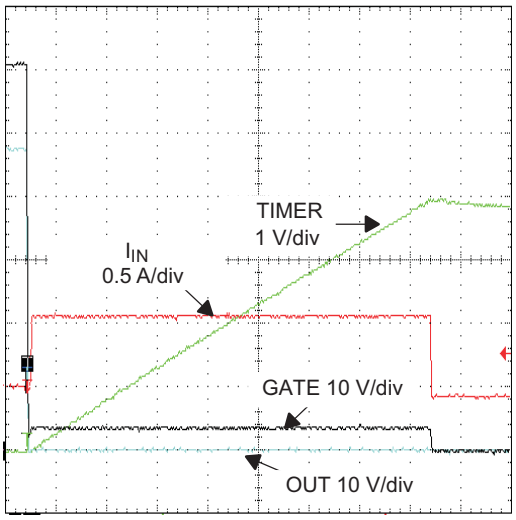


Figure 15. Current Limit Overview

The TPS249x responds rapidly to the short circuit as seen in Figure 16. The falling OUT voltage is the result of Q1 and C_O currents through the short's impedance at this time scale. The internal GATE clamp causes the GATE voltage to follow the output voltage down and subsequently limits the negative V_{GS} to 1 V to 2 V. The rapidly rising fault current overdrives the GATE amplifier causing it to overshoot and rapidly turn Q1 off by sinking current to ground. Q1 slowly turns back on as the GATE amplifier recovers; Q1 then settles to an equilibrium operating point determined by the power limiting circuit.

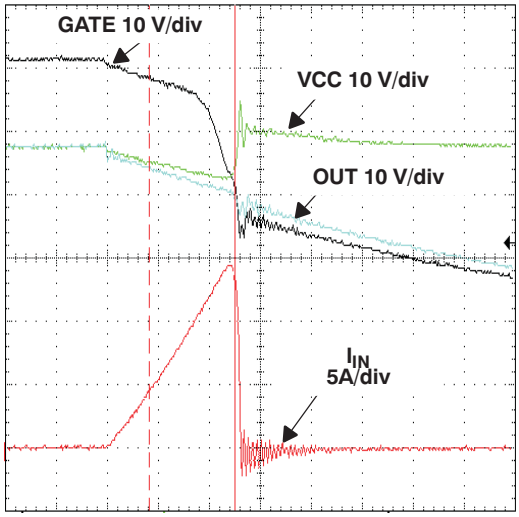


Figure 16. Current Limit Onset

Device Functional Modes (continued)

Minimal input voltage overshoot appears in Figure 16 because a local 100-µF bypass capacitor and very short input leads were used. The input voltage would overshoot as the input current abruptly drops in a typical application due to the stored energy in the input distribution's inductance. The exact waveforms seen in an application depend upon many factors including parasitics of the voltage distribution, circuit layout, and the short itself.

7.4.5 Automatic Restart (Figure 17)

The TPS2491 automatically initiates a restart after a fault has caused it to turn off Q1. Internal control circuits use C_T to count 16 cycles before re-enabling Q1. This sequence repeats if the fault persists. The TIMER has a 1:10 charge-to-discharge current ratio, and uses a 1-V lower threshold. The fault-retry duty cycle specification quantifies this behavior. This small duty cycle often reduces the average short-circuit power dissipation to levels associated with normal operation and eliminates special thermal considerations for surviving a prolonged output short.

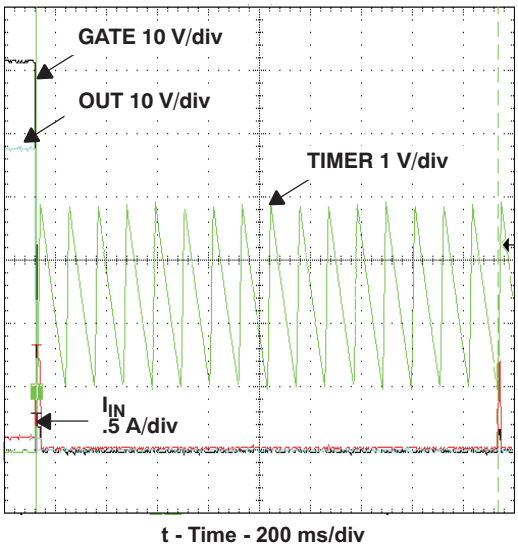


Figure 17. TPS2491 Restart Cycle Timing

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS2490 is a hot swap controller that provides inrush current limiting, electronic circuit breaker protection, controlled load turn-on, interfacing to down-stream dc-to-dc converters, and power feed protection. As a hot swap it is used to manage inrush current and protect in case of faults. When designing a hot swap three key scenarios should be considered:

- Start-up
- Output of a hot swap is shorted to ground when the hot swap is on. This is often referred to as a hot-short.
- Powering up a board when the output and ground are shorted. This is usually called a start-into-short.

All of these scenarios place a lot of stress on the hot swap MOSFET and thus special care is required when designing the hot swap circuit to keep the MOSFET within its SOA. Detailed design examples are provided in the following sections. Solving all of the equations by hand is cumbersome and can result in errors. Instead, TI recommends using the *TPS2490/91 Design-in Calculator* (SLVC033), which is provided on the product page.

8.1.1 Alternative Inrush Designs

8.1.1.1 Gate Capacitor (dV/dt) Control

The TPS249x can be used with applications that require constant turn-on currents. The current is controlled by a single capacitor from the GATE terminal to ground with a series resistor. Q1 appears to operate as a source follower (following the gate voltage) in this implementation. Choose a time to charge, Δt, based on the output capacitor, input voltage V_I, and desired charge current, I_{CHARGE}. Select I_{CHARGE} to be less than $P_{LIM} \div V_{VCC}$ if the power limit feature is kept. See *TPS2490/91 Design-in Calculator* (SLVC033) for a calculation tool.

$$\Delta t = \frac{C_O \times V_{VCC}}{I_{CHARGE}} \tag{4}$$

To select the gate capacitance:

$$C_G = \left(I_{GATE} \times \frac{\Delta t}{V_{VCC}} \right) - C_{RS} \tag{5}$$

where

- I_{GATE} is the nominal gate charge current.

This equation assumes that the MOSFET C_{GD} is the controlling element as the gate and output voltage rise. C_{GD} is non-linear with applied V_{DG}. An averaged estimate may be made using the MOSFET V_{GS} vs Q_G curve. Divide the charge accumulated during the plateau region by the plateau V_{GS} to get C_{RS}.

Because neither power nor current-limit faults are invoked during turnon, C_{TIMER} can be chosen for fast transient turnoff response using the Q1 SOA curve. Choose the single pulse time conservatively from the Q1 SOA curve using maximum operating voltage and maximum trip current. A series resistor of about 1 kΩ should be used in conjunction with C_G.

8.1.1.2 PROG Inrush Control

A capacitor can be connected from the PROG pin to ground to reduce the initial current step seen in Figure 13 based on the *代表的なアプリケーション* circuit. This method maintains a relatively fast turn-on time without the drawbacks of a gate-to-ground capacitor that include increased short circuit response time and less predictable gate clamping.

Application Information (continued)

8.1.2 Additional Design Considerations

8.1.2.1 Use of PG

Use the PG pin to control and coordinate a downstream dc/dc converter. A long time delay is needed to allow C_O to fully charge before the converter starts if this is not done. An undesirable latchup condition can be created between the TPS2490 output characteristic and the DC/DC converter input characteristic if the converter starts while C_O is still charging; the PG pin is one way to avoid this.

8.1.2.2 Faults and Backplane Voltage Droop

A hard short at the output of the TPS249x during normal operation could result in activation of the enable or UVLO circuit instead of the current limit if the input voltage droops sufficiently. The lower GATE drive in this condition will cause a prolonged, larger over-current spike. This can be eliminated by filtering EN, or distributing capacitance on the bus itself. Capacitance from adjacent plugged-in units may help with this as well.

8.1.2.3 Output Clamp Diode

Inductive loads on the output may drive the OUT pin below GND when the circuit is unplugged or during a current limit. The OUT pin ratings can be maintained with a diode, such as an D1, across TPS249x OUT to GND.

8.1.2.4 Gate Clamp Diode

The TPS249x has a relatively well-regulated gate voltage of 12 V to 16 V, even with low-supply voltages. A small clamp Zener from gate to source of Q1, such as a BZX84C7V5, is recommended if V_{GS} of Q1 is rated below this range.

8.1.2.5 High Gate Capacitance Applications

Gate voltage overstress and abnormally large fault current spikes can be caused by large gate capacitance. TI recommends an external gate clamp Zener diode to assist the internal Zener if the total gate capacitance of Q1 exceeds about 4000 pF. When gate capacitor dv/dt control is used, TI recommends a 1-kΩ resistor in series with C_G. If the series R-C combination is used for MOSFETs with C_{ISS} less than 3000 pF, then a Zener is not necessary.

8.1.2.6 Input Bypass

C_{IN} should be present for control of external noise at VCC and as a low-impedance source for high-speed circuits.

8.1.2.7 Output Short Circuit Measurements

Repeatable short-circuit testing results are difficult to obtain. The many details of source bypassing, input leads, circuit layout and component selection, output shorting method, relative location of the short, and instrumentation all contribute to obtaining different results. The actual short itself exhibits a certain degree of randomness as it microscopically bounces and arcs. Care in configuration and methods must be used to obtain realistic results. Do not expect to see waveforms exactly like those in the data sheet—every setup differs.

8.2 Typical Application

This section describes the design procedure for a 24-V, 10-A hot swap design.

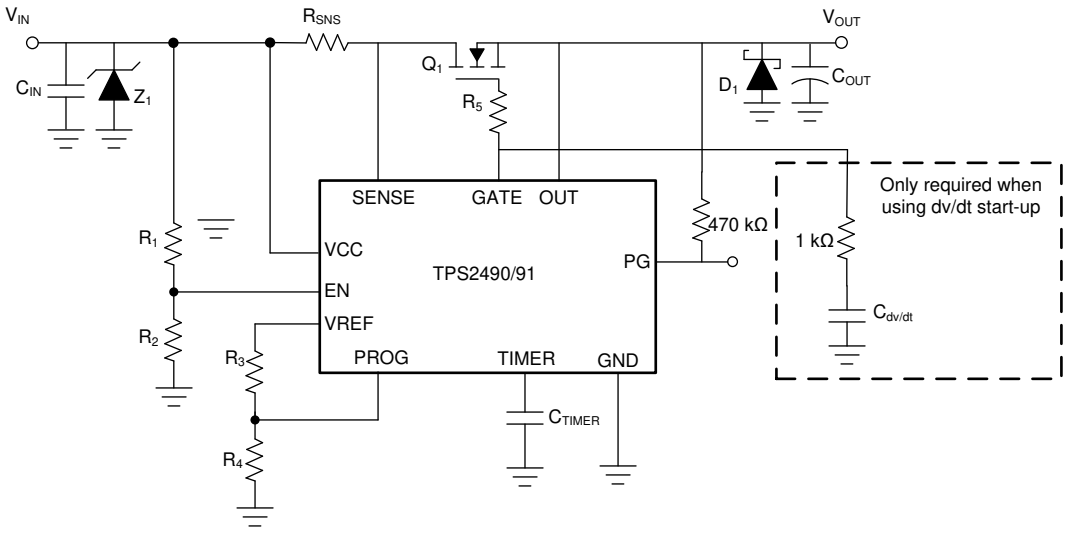


Figure 18. Typical Application Schematic, TPS2490

8.2.1 Design Requirements

Table 1 summarizes the design parameters that must be known before designing a hot swap circuit. When charging the output capacitor through the hot swap MOSFET, the FET's total energy dissipation equals the total energy stored in the output capacitor ($1/2CV^2$). Thus both the input voltage and Output capacitance will determine the stress experienced by the MOSFET. The maximum load current will drive the current limit and sense resistor selection. In addition, the maximum load current, maximum ambient temperature, and the thermal properties of the PCB ($R_{\theta CA}$) will drive the selection of the MOSFET R_{DSON} and the number of MOSFETs used. $R_{\theta CA}$ is a strong function of the layout and the amount of copper that is connected to the drain of the MOSFET. Note that the drain is not electrically connected to the ground plane and thus the ground plane cannot be used to help with heat dissipation. For this design example $R_{\theta CA}$ = 30°C/W is used, which is similar to the TPS2490 EVM. It's a good practice to measure the $R_{\theta CA}$ of a given design after the physical PCBs are available.

Finally, it is important to understand what test conditions the hot swap needs to pass. In general, a hot swap is designed to pass both a *Hot-Short* and a *Start into a Short*, which are described in the previous section. Also, TI recommends to keep the load OFF until the hot swap is fully powered up. Starting the load early causes unnecessary stress on the MOSFET and could lead to MOSFET failures or a failure to start-up.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	18 V - 30 V
Target UVLO Threshold	18 V
Maximum load current	10 A
Maximum Output Capacitance of the Hot swap	330 µF
Maximum Ambient Temperature	55°C
MOSFET $R_{\theta CA}$ (function of layout)	30°C/W
Pass *Hot-Short* on Output?	Yes
Pass a *Start into short*?	Yes
Is the load off until PG asserted?	Yes
Can a hot board be plugged back in?	Yes

8.2.2 Detailed Design Procedure

8.2.2.1 Select R_{SNS} and CL setting

The TPS2490 monitors the current in the external MOSFET (Q1) by measuring the voltage across the sense resistor (RS), connected from VIN to SENSE. When the voltage difference across the Vin and Sense pins (VCL) is greater than 50 mV(typical), the LM5069 will begin regulating the MOSFET gate. Size R_{SNS} for maximum or minimum V_{CL} for applications that require guaranteed shutoff or guaranteed conduction. In this design example, R_{SNS} is sized to exhibit minimum V_{CL} across R_{SNS} at maximum load current.

$$R_{SNS,CLC} = \frac{V_{CL}}{I_{LIM}} = \frac{45\ mV}{10\ A} = 4.5\ m\Omega \tag{6}$$

Typically sense resistors are only available in discrete values. If a precise current limit is desired, a sense resistor along with a resistor divider can be used as shown in Figure 19.

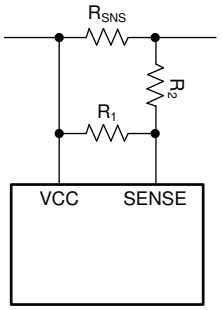


Figure 19. SENSE Resistor Divider

If using a resistor divider, then the next larger available sense resistor should be chosen (1 mΩ for example). The ratio of R1 and R2 can then be computed as follows:

$$\frac{R_3}{R_4} = \frac{R_{SNS,CLC}}{R_{SNS} - R_{SNS,CLC}} = \frac{4.5\ m\Omega}{5\ m\Omega - 4.5\ m\Omega} = 9 \tag{7}$$

Note that the SENSE pin typically pulls 7.5 µA of current, which creates an offset across R2. TI recommends to keep R2 below 10 Ω to reduce the offset that this introduces. In addition the 1% resistors add to the current monitoring error. Finally, if the resistor divider approach is used, the user should compute the effective sense resistance ($R_{SNS,EFF}$) using Equation 8 instead of R_{SNS} in all equations.

$$R_{SNS,EFF} = \frac{R_{SNS} \times R_3}{R_3 + R_4} \tag{8}$$

Note that for many applications, a precise current limit may not be required. In that case, it is simpler to pick the next smaller available sense resistor. For this application, a resistive divider was not used, and a 4 mΩ resistor was used for a 12.5 A (typical) current limit.

8.2.2.2 Selecting the Hot Swap FET(s)

It is critical to select the correct MOSFET for a hot swap design. The device must meet the following requirements:

- The V_{DS} rating should be sufficient to handle the maximum system voltage along with any ringing caused by transients. For most 12-V systems a 30-V FET is a good choice.
- The SOA of the FET should be sufficient to handle all usage cases: start-up, hot-short, start into short.
- R_{DSON} should be sufficiently low to maintain the junction and case temperature below the maximum rating of the FET. TI recommends to keep the steady state FET temperature below 125°C to allow margin to handle transients.
- Maximum continuous current rating should be above the maximum load current and the pulsed drain current

must be greater than the current threshold of the circuit breaker. Most MOSFETs that pass the first three requirements also pass these two.

- A V_{GS} rating of ±20 V is required, because the TPS2490 can pull up the gate as high as 16 V above source.

For this design the CSD19532KTT was selected for its low R_{DSON} and good SOA. After selecting the MOSFET, the maximum steady state case temperature can be computed as follows:

$$T_{C,MAX} = T_{A,MAX} + R_{\theta CA} \times I^2_{LOAD,MAX} \times R_{DSON}(T_J) \quad (9)$$

Note that the R_{DSON} is a strong function of junction temperature, which for most MOSFETs will be close to the case temperature. A few iterations of the above equations may be necessary to converge on the final R_{DSON} and $T_{C,MAX}$ value. According to the CSD17552Q5B datasheet, its R_{DSON} is approximately 1.4x at 78°C. The Equation 10 uses this R_{DSON} value to compute the $T_{C,MAX}$.

$$T_{C,MAX} = 55\ °C + 30\ °\frac{C}{W} \times (10\ A)^2 \times (1.4 \times 5.6\ m\Omega) = 78.5\ °C \quad (10)$$

This maximum steady state case temperature indicates that a second MOSFET is not needed to reduce and distribute power dissipation during normal operation.

For reference, when using parallel MOSFETs, the maximum steady state case temperature can be computed as follows:

$$T_{C,MAX} = T_{A,MAX} + R_{\theta CA} \times \left(\frac{I_{LOAD,MAX}}{\#\,of\,MOSFETs}\right)^2 \times R_{DSON}(T_J) \quad (11)$$

Iterate until the computed $T_{C,MAX}$ is using two parallel MOSFETs is less than to the junction temperature assumed for R_{DSON}. Then, no further iterations are necessary.

8.2.2.3 Select Power Limit

In general, a lower power limit setting is preferred to reduce the stress on the MOSFET. However, when the TPS2490 is set to a very low power limit setting, it has to regulate the FET current and hence the voltage across the sense resistor (V_{SNS}) to a very low value. V_{SNS} can be computed as shown in Equation 12:

$$V_{SNS} = \frac{P_{LIM} \times R_{SNS}}{V_{DS}} \quad (12)$$

To avoid significant degradation of the power limiting accuracy, a V_{SNS} of less than 5 mV is not recommended. Based on this requirement the minimum allowed power limit can be computed as follows:

$$P_{LIM,MIN} = \frac{V_{SNS,MIN} \times V_{IN,MAX}}{R_{SNS}} = \frac{5\ mV \times 30\ V}{4\ m\Omega} = 37.5\ W \quad (13)$$

Because the V_{PROG} pin, which programs the power limit of the device, has a minimum voltage of 0.4 V, the set PLIM must also result in the voltage at V_{PROG} being greater than 0.4 V. Based on this requirement the minimum allowed power limit can be computed as follows:

$$P_{LIM,MIN} = V_{PROG} * I_{LIM(MAX)} * 10 = 0.4 * 12.5 * 10 = 50\ W \quad (14)$$

Because the power limit has to satisfy both the V_{SNS} and V_{PROG}, the greater $P_{LIM,MIN}$ value is used as the basis for sizing the resistive divider. In this design example it is 50 W. The maximum ratio of the resistive divider can be computed as follows:

$$\frac{R_3}{R_4} = \frac{V_{REF}}{V_{PROG}} - 1 = \frac{V_{REF}}{\frac{P_{LIM,MIN}}{10 * I_{LIM}}} - 1 = \frac{4\ V}{\frac{50\ W}{10 * 12.5}} - 1 = 9 \quad (15)$$

In Equation 16 R3 is picked as 41.2 kΩ. R3 must be greater than 4 kΩ, but TI recommends that 10 kΩ or greater be used. The resistive divider ratio is used to calculate R4, and next largest available resistor is chosen.

$$R_4 = \frac{1}{\frac{R_3}{R_4}} * R_3 = \frac{1}{9} * 41.2\ k\Omega = 4.58\ k\Omega \tag{16}$$

We choose 4.64 kΩ for our final value of R4.

8.2.2.4 Set Fault Timer

The fault timer runs when the hot swap is in power limit or current limit, which is the case during start-up. Thus the timer has to be sized large enough to prevent a time-out during start-up. If the part starts directly into current limit (I_{LIM} x V_{DS} < P_{LIM}) the maximum start time can be computed with Equation 17:

$$t_{start,max} = \frac{C_{OUT} \times V_{IN,MAX}}{I_{LIM}} \tag{17}$$

For most designs (including this example) I_{LIM} x V_{DS} > P_{LIM} so the hot swap will start in power limit and transition into current limit. In that case the start time can be computed as follows:

$$t_{start} = \frac{C_{OUT}}{2} \times \left[\frac{V_{IN,MAX}^2}{P_{LIM,TYP}} + \frac{P_{LIM,TYP}}{I_{LIM}^2} \right] = \frac{330\ \mu F}{2} \times \left[\frac{(30\ V)^2}{50\ W} + \frac{50\ W}{(12.5\ A)^2} \right] = 2.92\ ms \tag{18}$$

The actual startup time is slightly longer, as the power limit is a function of V_{DS} and decreases as the output voltage increases. To ensure that the timer never times out during start-up, TI recommends to set the fault time (t_{flt}) to be 1.75 x t_{start} or 5.11ms. This accounts for the variation in power limit, timer current, and timer capacitance. Thus C_{TIMER} can be computed as follows:

$$C_{TIMER} = \frac{t_{flt} \times i_{timer}}{v_{timer}} = \frac{5.11\ ms \times 25\ \mu A}{4\ V} = 32\ nF \tag{19}$$

The next largest available C_{TIMER} is chosen as 33 nF. Once the C_{TIMER} is chosen the actual programmed fault time can be computed as follows:

$$t_{flt} = \frac{C_{TIMER} \times v_{timer}}{i_{timer}} = \frac{33\ nF \times 4\ V}{25\ \mu A} = 5.28\ ms \tag{20}$$

8.2.2.5 Check MOSFET SOA

Once the power limit and fault timer are chosen, it is critical to check that the FET stays within its SOA during all test conditions. During a *Hot-Short* the circuit breaker trips and the TPS2490 restarts into power limit until the timer runs out. In the worst case the MOSFET's V_{DS} will equal $V_{IN,MAX}$, I_{DS} will equal P_{LIM} / $V_{IN,MAX}$ and the stress event will last for t_{flt}. For this design example the MOSFET has 30 V, 1.83 A across it for 5.28 ms.

Based on the SOA of the CSD19532KTT, it can handle 30 V, 2.4 A for 10 ms and it can handle 30 V, 11A for 1ms. The SOA for 5.28 ms can be extrapolated by approximating SOA vs time as a power function as shown in Equation 21 through Equation 24:

$$I_{SOA}(t) = a \times t^m \tag{21}$$

$$m = \frac{\ln(I_{SOA}(t_1) / I_{SOA}(t_2))}{\ln(t_1 / t_2)} = \frac{\ln\left(\frac{12\ A}{2.4\ A}\right)}{\ln\left(\frac{1\ ms}{10\ ms}\right)} = -0.7 \tag{22}$$

$$a = \frac{I_{SOA}(t_1)}{t_1^m} = \frac{2.3\ A}{(10\ ms)^{-0.7}} = 2.4\ A \times (10\ ms)^{0.7} \quad (23)$$

$$I_{SOA}(6.24\ ms) = 2.4\ A \times (10\ ms)^{0.7} \times (5.28\ ms)^{-0.7} = 3.75\ A \quad (24)$$

Note that the SOA of a MOSFET is specified at a case temperature of 25°C, while the case temperature can be much hotter during a hot-short. The SOA should be de-rated based on $T_{C,MAX}$ using Equation 25 through Equation 26:

$$I_{SOA}(5.28\ ms, T_{C,MAX}) = I_{SOA}(5.28\ ms, 25\ °C) \times \frac{T_{J,ABSMAX} - T_{C,MAX}}{T_{J,ABSMAX} - 25\ °C} \quad (25)$$

$$= 3.75 \times \frac{175\ °C - 78.5\ °C}{175\ °C - 25\ °C} = 2.41\ A \quad (26)$$

Based on this calculation the MOSFET can handle 2.41 A, 30 V for 5.28 ms at elevated case temperature, but is required to handle 1.83 A during a hot-short. This means the MOSFET will not be at risk of getting damaged during a hot-short. In general, TI recommends for the MOSFET to be able to handle a minimum of 1.3x more power than what is required during a hot-short in order to provide margin to cover the variance of the power limit and fault time.

8.2.2.6 Set Under-Voltage Threshold

For this design example, the following values are targeted: V_{UVH} = 18 V, V_{UVL} = 17 V. First, pick R2 to be a common value such as 10 kΩ. R1 can be computed using the Equation 27:

$$R1 = \left(\frac{V_{UV}}{1.35\ V} - 1\right) * R2 = \left(\frac{18}{1.35\ V} - 1\right) * 10\ k\Omega = 123.3\ k\Omega \quad (27)$$

Nearest available 1% resistors should be chosen. Set R1 = 124 kΩ, R2 = 10 kΩ.

8.2.2.7 Choose R5, and C_{IN}

R5 is intended to suppress high-frequency oscillations; a resistor of 10 Ω will serve for most applications but if Q1 has a C_{ISS} below 200 pF, then use 33 Ω. Applications with larger MOSFETs and short wiring may not require R5. C_{IN} is a bypass capacitor to help with control of transient voltages, unit emissions, and local supply noise while in the disabled state. Where acceptable, TI recommends a value in the range of 0.001 µF to 0.1 µF.

8.2.2.8 Input and Output Protection

Proper operation of the TPS2490 hot swap circuit requires a voltage clamping element present on the supply side of the connector into which the hot swap circuit is plugged in. A TVS is ideal, as depicted in . The TVS is necessary to absorb the voltage transient generated whenever the hot swap circuit shuts off the load current. This effect is the most severe during a hot-short when a large current is suddenly interrupted when the FET shuts off. The TVS should be chosen to have minimal leakage current at $V_{IN,MAX}$ and to clamp the voltage during hot-short events. For many high power applications, SMBJ30A-13-F is a good choice.

8.2.2.9 Final Schematic and Component Values

shows the schematic used to implement the requirements described in the previous section. In addition, Table 2 provides the final component values that were used to meet the design requirements for a 24-V, 10-A hot swap design. The *Application Curves* are based on the component values in Table 2.

Table 2. Component Values

COMPONENT	VALUE
R_{SNS}	4 mΩ
R1	124 kΩ

Table 2. Component Values (continued)

COMPONENT	VALUE
R2	10 kΩ
R3	41.2 kΩ
R4	4.64 kΩ
Q1	CSD19532KTT
Z1	SMBJ30A-13-F
C_{TIMER}	33 nF

8.2.3 Application Curves

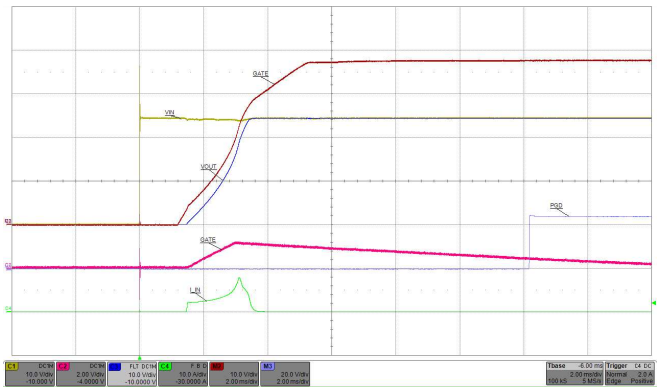


Figure 20. Start-Up

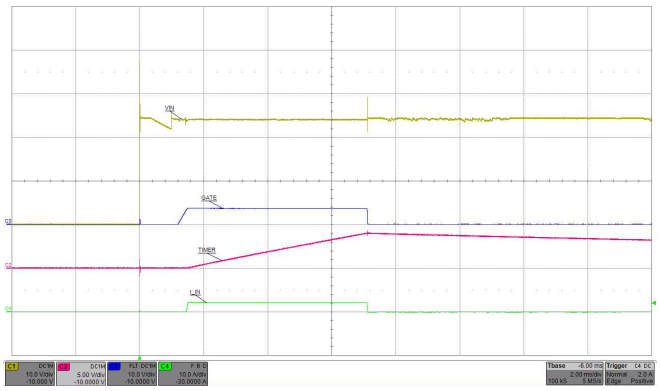


Figure 21. Start-Up into Short Circuit

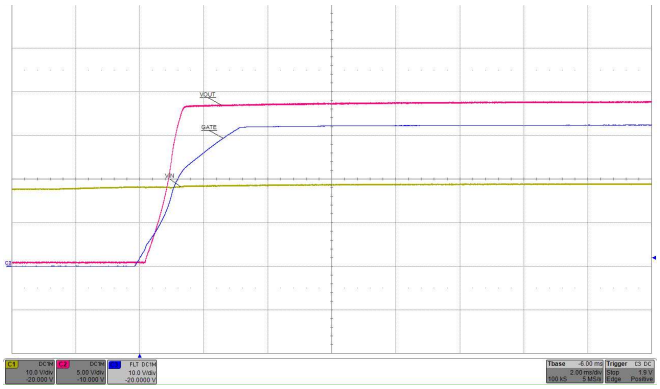


Figure 22. Under-Voltage

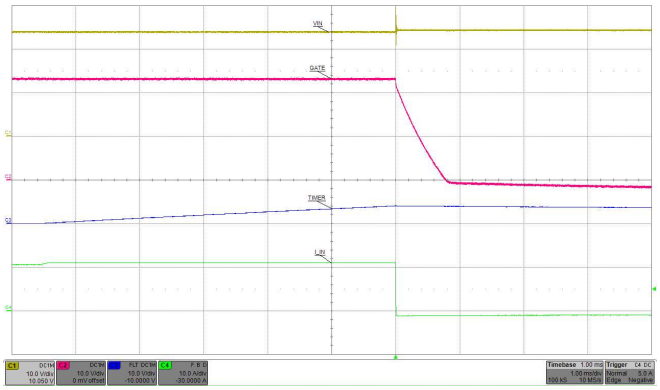


Figure 23. Gradual Over-Current

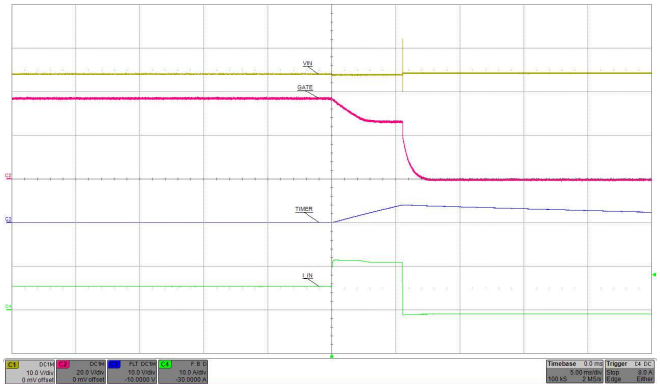


Figure 24. Loadstep

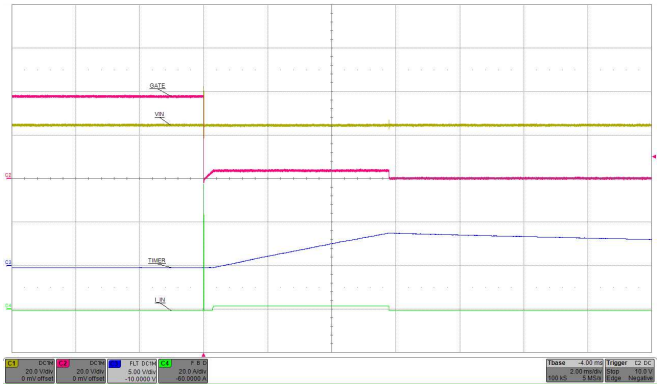


Figure 25. Hotshort on Output

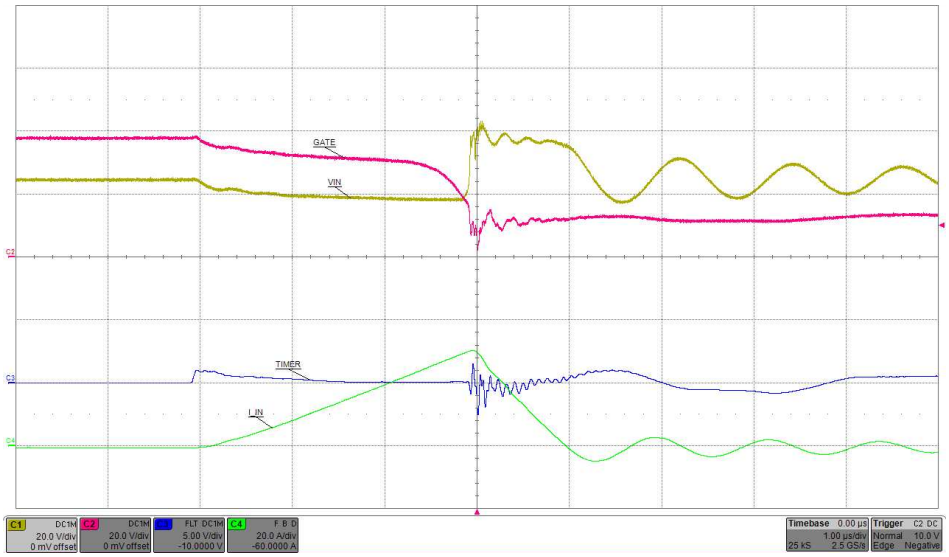


Figure 26. Hotshort (Zoomed-In)

9 Power Supply Recommendations

In general, the TPS2490 behavior is more reliable if it is supplied from a very regulated power supply. However, high-frequency transients on a backplane are not uncommon due to adjacent card insertions or faults. If this is expected in the end system, TI recommends placing a 1-µF ceramic capacitor to ground close to the drain of the hot swap MOSFET. This reduces the common mode voltage seen by VCC and SENSE. Additional filtering may be necessary to avoid nuisance trips.

10 Layout

10.1 Layout Guidelines

10.1.1 PC Board Guidelines

The following guidelines must be followed when designing the PC board for the TPS2490:

- Place the TPS2490 close to the board's input connector to minimize trace inductance from the connector to the FET.
- Note that special care must be taken when placing the bypass capacitor for the VCC pin. During hot shorts, there is a very large dV/dt on input voltage after the MOSFET turns off. If the bypass capacitor is placed right next to the pin and the trace from Rsns to the pin is long, an LC filter is formed. As a result, a large differential voltage can develop between VCC and SENSE. To avoid this, place the bypass capacitor close to Rsns instead of the VCC pin.
- The sense resistor (R_S) must be close to the TPS2490, and connected to it using Kelvin techniques.
- The high current path from the board's input to the load (via Q1), and the return path, must be parallel and close to each other to minimize loop inductance.
- The ground connection for the various components around the TPS2490 must be connected directly to each other and to the TPS2490's GND pin, and then connected to the system ground at one point. Do not connect the various component grounds to each other through the high current ground line.
- Provide adequate heat sinking for the series pass device (Q1) to help reduce stresses during turnon and turnoff.
- The board's edge connector can be designed to shut off the TPS2490 as the board is removed, before the supply voltage is disconnected from the TPS2490. A shorter edge connector pin can be used for the EN signal going to the TPS2490. In this case, when the board is inserted into the edge connector, the system voltage is applied to the TPS2490's VCC pin before the EN voltage is taken high.

10.1.2 System Considerations

A) Continued proper operation of the LM5069 hot swap circuit requires capacitance be present on the supply side of the connector into which the hot swap circuit is plugged in, as depicted in . The capacitor in the *Live Backplane* section is necessary to absorb the transient generated whenever the hot swap circuit shuts off the load current. If the capacitance is not present, inductance in the supply lines generate a voltage transient at shut-off which can exceed the absolute maximum rating of the TPS2490, resulting in its destruction.

B) If the load powered via the TPS2490 hot swap circuit has inductive characteristics, a diode is required across the TPS2490’s output. The diode provides a recirculating path for the load’s current when the TPS2490 shuts off that current. Adding the diode prevents possible damage to the TPS2490 as the OUT pin is taken below ground by the inductive load at shutoff. See Figure 27.

Layout Guidelines (continued)

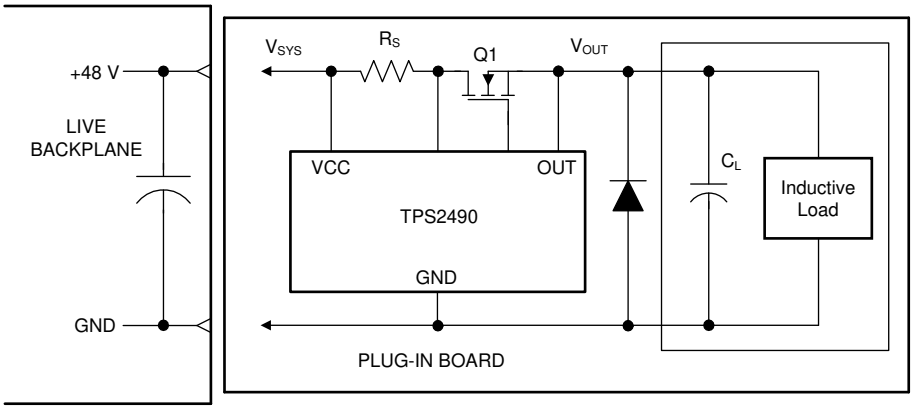


Figure 27. Output Diode Required for Inductive Loads

10.2 Layout Example

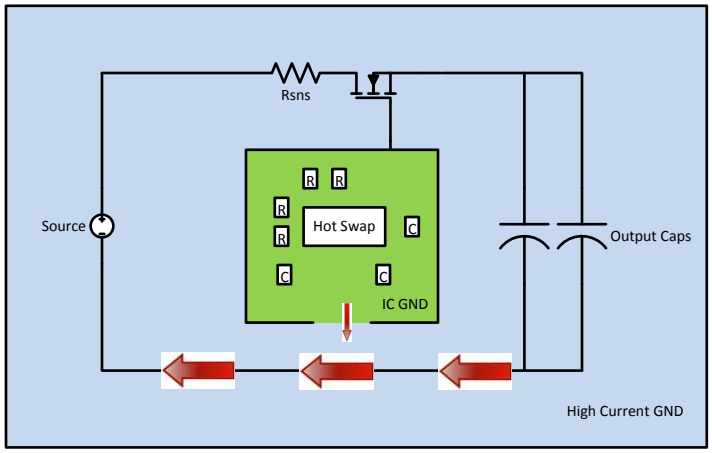


Figure 28. TPS249x Quiet IC Ground Layout

11 デバイスおよびドキュメントのサポート

11.1 開発サポート

TPS2490、TPS2491デザイン・カリキュレータ・ツールについては、*『TPS2490/91デザインイン・カリキュレータ』* (SLVC033)を参照してください。

11.2 ドキュメントのサポート

11.2.1 関連資料

関連資料については、以下を参照してください。

『堅牢なホットスワップ設計』、(SLVA673)

11.3 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 3. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
TPS2490	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TPS2491	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

11.4 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.5 コミュニティ・リソース

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.6 商標

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All other trademarks are the property of their respective owners.

11.7 静電気放電に関する注意事項

これらのデバイスは、限定的なESD（静電破壊）保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

11.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS2490DGS	Active	Production	VSSOP (DGS) | 10	80 | TUBE	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	BIY
TPS2490DGS.A	Active	Production	VSSOP (DGS) | 10	80 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BIY
TPS2490DGSG4	Active	Production	VSSOP (DGS) | 10	80 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BIY
TPS2490DGSR	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	BIY
TPS2490DGSR.A	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BIY
TPS2490DGSRG4	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BIY
TPS2491DGS	Active	Production	VSSOP (DGS) | 10	80 | TUBE	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	BIX
TPS2491DGS.A	Active	Production	VSSOP (DGS) | 10	80 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BIX
TPS2491DGSG4	Active	Production	VSSOP (DGS) | 10	80 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BIX
TPS2491DGSR	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	BIX
TPS2491DGSR.A	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BIX
TPS2491DGSRG4	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BIX

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

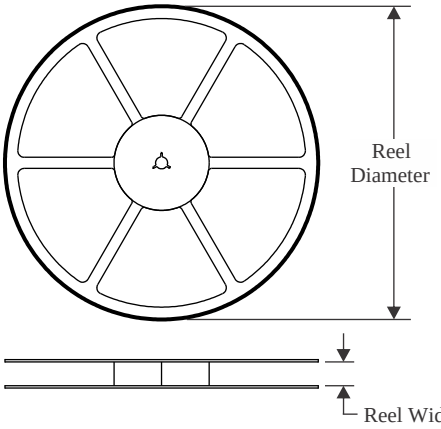
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

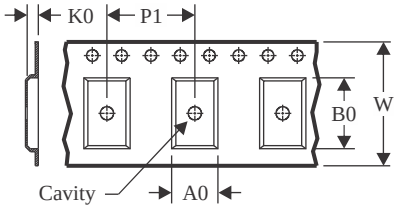
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

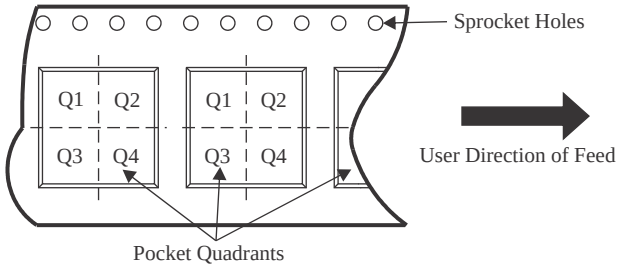


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

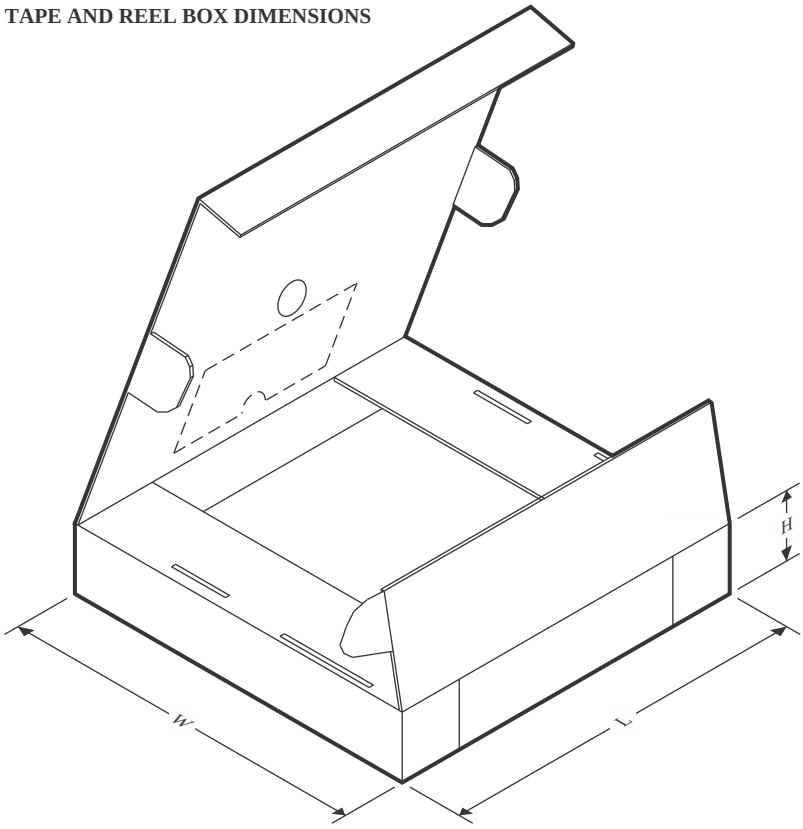
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2490DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS2491DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

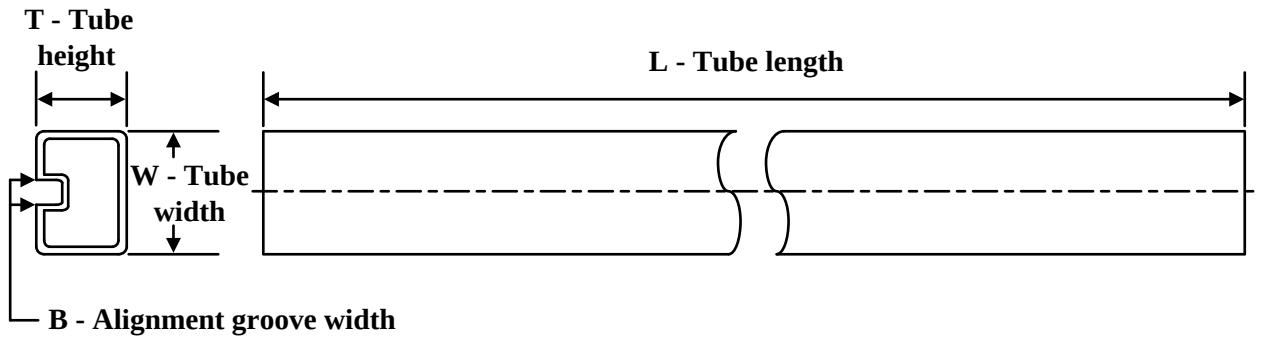
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2490DGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
TPS2491DGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0

TUBE



*All dimensions are nominal

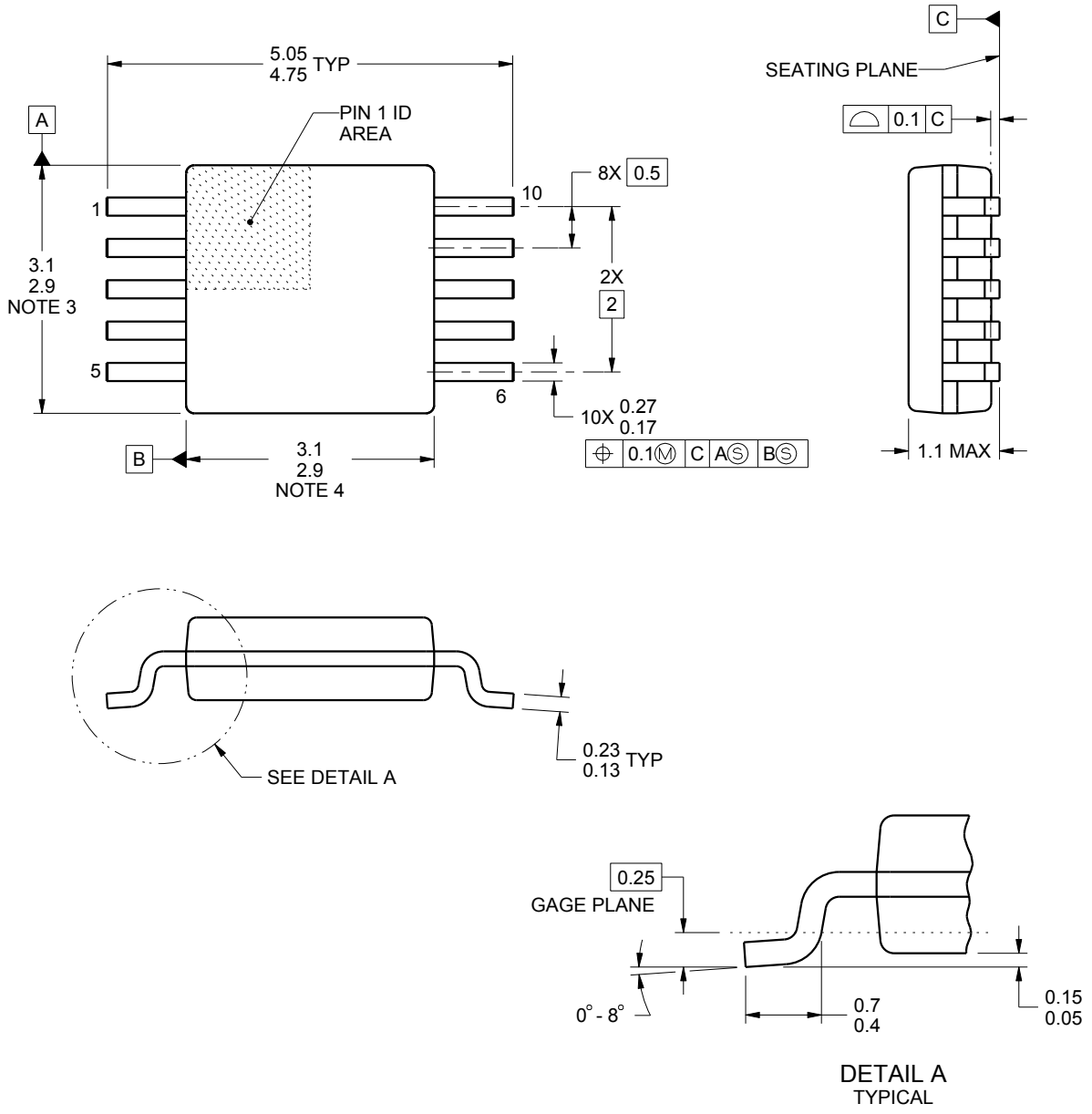
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS2490DGS	DGS	VSSOP	10	80	330	6.55	500	2.88
TPS2490DGS	DGS	VSSOP	10	80	322	6.55	1000	3.01
TPS2490DGS.A	DGS	VSSOP	10	80	330	6.55	500	2.88
TPS2490DGS.A	DGS	VSSOP	10	80	322	6.55	1000	3.01
TPS2490DGSG4	DGS	VSSOP	10	80	330	6.55	500	2.88
TPS2490DGSG4	DGS	VSSOP	10	80	322	6.55	1000	3.01
TPS2491DGS	DGS	VSSOP	10	80	322	6.55	1000	3.01
TPS2491DGS	DGS	VSSOP	10	80	330	6.55	500	2.88
TPS2491DGS.A	DGS	VSSOP	10	80	322	6.55	1000	3.01
TPS2491DGS.A	DGS	VSSOP	10	80	330	6.55	500	2.88
TPS2491DGSG4	DGS	VSSOP	10	80	322	6.55	1000	3.01
TPS2491DGSG4	DGS	VSSOP	10	80	330	6.55	500	2.88

PACKAGE OUTLINE

DGS0010A

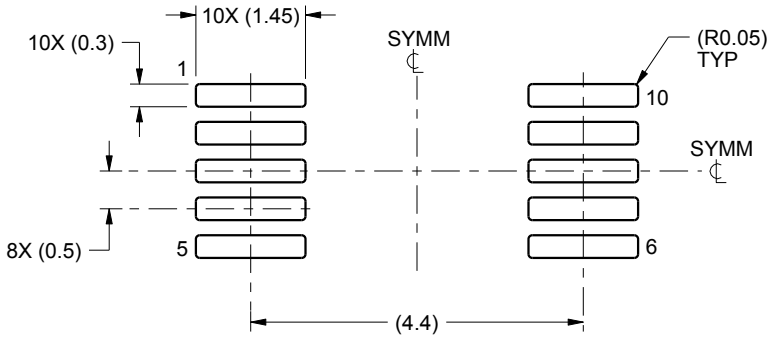
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

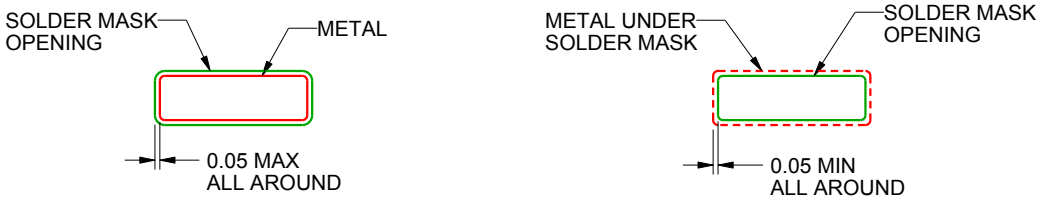


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

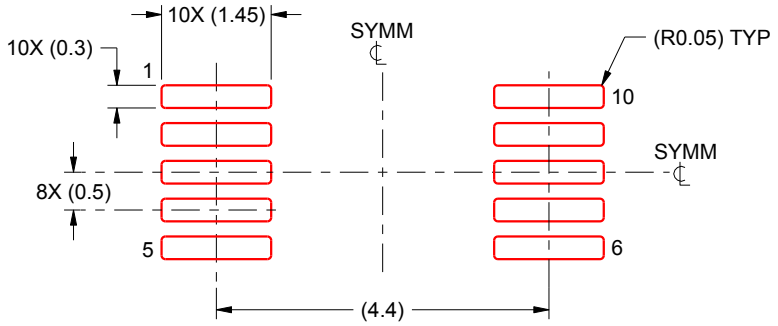


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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