参考資料

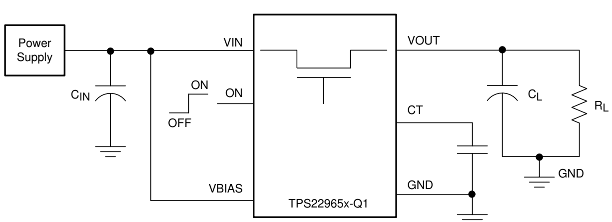
TPS22965x-Q1 車載対応、5.5V、4A、オン抵抗 16mΩ のロード・スイッチ

1 特長

- 車載アプリケーション認定済み
  - AEC-Q100 認定済み
  - デバイス温度グレード 2:40℃～+105℃ (TPS22965-Q1、TPS22965N-Q1)
  - デバイス温度グレード 1:40℃～+125℃ (TPS22965W-Q1、TPS22965NW-Q1)
  - デバイス HBM ESD 分類レベル 3A
  - デバイス CDM ESD 分類レベル C6
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- シングル・チャネル・ロード・スイッチを内蔵
- 入力電圧範囲:0.8V～5.5V
- 非常に低いオン抵抗 (R_{ON})
  - V_{IN} = 5V (V_{BIAS} = 5V) で R_{ON} = 16mΩ
  - V_{IN} = 3.6V (V_{BIAS} = 5V) で R_{ON} = 16mΩ
  - V_{IN} = 1.8V (V_{BIAS} = 5V) で R_{ON} = 16mΩ
- 連続スイッチ電流:最大 4A
- 低静止電流:50μA
- 制御入力しきい値が低いため、1.2、1.8、2.5、3.3V ロジックを使用可能
- 立ち上がり時間を設定可能
- クイック出力放電 (QOD) (TPS22965-Q1 および TPS22965W-Q1 のみ)
- サーマル・パッド付き WSON 8 ピン・パッケージ

2 アプリケーション

- 自動車用エレクトロニクス
- インフォテインメント
- ADAS (先進運転支援システム)



概略回路図

3 概要

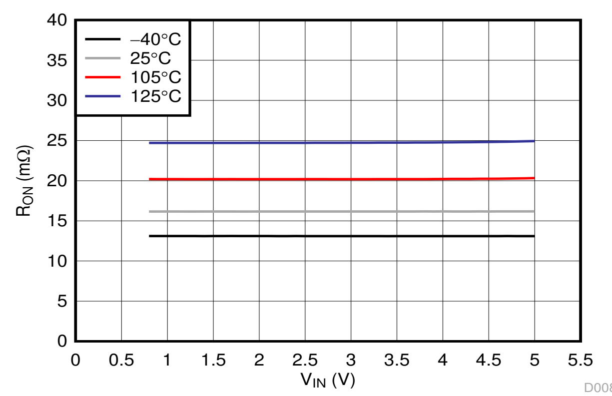
TPS22965x-Q1 は、ターンオンが制御された、小型で R_{ON} が非常に低いシングル・チャネル負荷スイッチです。このデバイスには N チャネル MOSFET が内蔵されており、0.8V～5.5V の入力電圧範囲で動作し、最大 4A の連続電流を供給できます。突入電流が小さくなるように、VOUT の立ち上がり時間を設定できます。TPS22965-Q1 および TPS22965W-Q1 デバイスには、スイッチがオフになった時に出力を迅速に放電できるように 225Ω のオンチップ負荷抵抗が内蔵されています。

TPS22965x-Q1 デバイスは、大きな消費電力に対応可能なサーマル・パッド付き、小型、省スペースの 2mm × 2mm、8 ピン WSON パッケージ (DSG0008A) で供給されます。TPS22965-Q1 および TPS22965N-Q1 デバイスは、-40℃～105℃ の自由気流温度範囲で動作が規定されています。さらに、TPS22965W-Q1 および TPS22965NW-Q1 デバイスは同じ WSON パッケージ (DSG0008B) でウェッタブル・フランクを採用しており、-40℃～+125℃ の自由気流温度範囲で動作が規定されています。

製品情報 (1)

部品番号	パッケージ	本体サイズ (公称)
TPS22965-Q1	DSG0008A WSON (8)	2.00mm × 2.00mm
TPS22965N-Q1		
TPS22965W-Q1	DSG0008B WSON (8)	
TPS22965NW-Q1		

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



R_{ON} と V_{IN} の関係 (V_{BIAS} = 5V、I_{OUT} = –200mA)

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (December 2019) to Revision E (July 2022) — **Page**

- 文書全体にわたって表、図、相互参照の採番方法を更新 ... 1
- ドキュメントのタイトルに「車載用」を追加 ... 1
- Updated the *ESD Ratings* table for automotive devices ... 4
- Added line item in the *Recommended Operating Conditions* table for VIL voltage at VBIAS = 2 V to 2.5 V ... 4
- Added line item in *Electrical Characteristics—V_{BIAS} = 2 V to 2.5 V* for QOD resistance at VBIAS = 2 V ... 7
- Expanded VBIAS minimum rating from 2.5 V to 2 V ... 7

Changes from Revision C (September 2016) to Revision D (December 2019) — **Page**

- *「特長」*セクションに機能安全対応のリンクを追加 ... 1

Changes from Revision B (December 2015) to Revision C (September 2016) — **Page**

- 「概要」セクションと「熱に関する情報」表にパッケージ指定子を追加。 ... 1

Changes from Revision A (June 2015) to Revision B (December 2015) — **Page**

- TPS22965W-Q1 デバイスのステータスを「アクティブ」に更新 ... 1
- Added 125°C temperature performance to typical AC timing parameters ... 12

Changes from Revision * (April 2014) to Revision A (June 2015) — **Page**

- 部品番号 TPS22965N-Q1 を追加 ... 1
- Updated Thermal Information table ... 5
- Updated typical AC timing parameters (tables, graphs and scope captures) ... 12

5 Device Comparison Table

DEVICE	R_{ON} AT 3.3 V (TYP)	QUICK OUTPUT DISCHARGE	PACKAGE WITH WETTABLE FLANKS	MAXIMUM OUTPUT CURRENT	TEMPERATURE RANGE
TPS22965-Q1	16 mΩ	Yes	No	4 A	–40°C to +105°C
TPS22965N-Q1	16 mΩ	No	No	4 A	–40°C to +105°C
TPS22965W-Q1	16 mΩ	Yes	Yes	4 A	–40°C to +125°C
TPS22965NW-Q1	16 mΩ	No	Yes	4 A	–40°C to +125°C

6 Pin Configuration and Functions

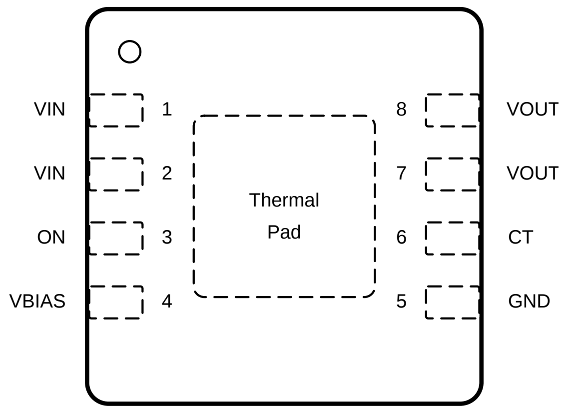


図 6-1. DSG Package 8-Pin WSON with Exposed Thermal Pad Top View

表 6-1. Pin Functions

PIN NO.	PIN NAME	I/O	DESCRIPTION
1, 2	VIN	I	Switch input. Input bypass capacitor recommended for minimizing V_{IN} dip. Must be connected to Pin 1 and Pin 2. See the *Application and Implementation* section for more information
3	ON	I	Active high switch control input. Do not leave floating
4	VBIAS	I	Bias voltage. Power supply to the device. Recommended voltage range for this pin is 2 V to 5.5 V. See the *Application and Implementation* section for more information
5	GND	—	Device ground
6	CT	O	Switch slew rate control. Can be left floating. See the *Application and Implementation* section for more information
7, 8	VOUT	O	Switch output
—	Thermal pad	—	Thermal pad (exposed center pad) to alleviate thermal stress. Tie to GND. See the *Layout* section for layout guidelines

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1] [2]

		MIN	MAX	UNIT [2]
V_{IN}	Input voltage	–0.3	6	V
V_{OUT}	Output voltage	–0.3	6	V
V_{BIAS}	Bias voltage	–0.3	6	V
V_{ON}	On voltage	–0.3	6	V
I_{MAX}	Maximum continuous switch current		4	A
I_{PLS}	Maximum pulsed switch current, pulse < 300 µs, 2% duty cycle		6	A
T_J	Maximum junction temperature		150	°C
T_{STG}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground pin.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100- 002 [1] HBM classification level 3A	±4000	V
		Charged device model (CDM), per AEC Q100- 011 CDM classification level C6	±1500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{IN}	Input voltage		0.8	V_{BIAS}	V
V_{BIAS}	Bias voltage		2	5.5	V
V_{ON}	ON voltage		0	5.5	V
V_{OUT}	Output voltage			V_{IN}	V
V_{IH}	High-level input voltage, ON	V_{BIAS} = 2.5 V to 5.5 V	1.2	5.5	V
V_{IL}	Low-level input voltage, ON	V_{BIAS} = 2.5 V to 5.5 V	0	0.5	V
		V_{BIAS} = 2 V to 2.5 V	0	0.45	V
C_{IN}	Input capacitor		1 [1]		µF
T_A	Operating free-air temperature [2]	TPS22965N-Q1, TPS22965-Q1	–40	105	°C
		TPS22965NW-Q1, TPS22965W-Q1	–40	125	

(1) See the *Application and Implementation* section.
(2) In applications where high power dissipation, poor package thermal resistance is present, the maximum ambient temperature can be derated. Maximum ambient temperature [$T_{A(max)}$] is dependent on the maximum operating junction temperature [$T_{J(max)}$], the maximum power dissipation of the device in the application [$P_{D(max)}$], and the junction-to-ambient thermal resistance of the part, package in the application ($R_{J\theta A}$), as given by the following equation: $T_{A(max)} = T_{J(max)} – (R_{\theta JA} \times P_{D(max)})$.

7.4 Thermal Information

THERMAL METRIC[(1)]		TPS22965-Q1, TPS22965N-Q1	TPS22965W-Q1, TPS22965NW-Q1	UNIT
		DSG0008A (WSON)	DSG0008B (WSON)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	72.3	67.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	96.1	95	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	42.1	37.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.3	2.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.5	37.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	13.2	8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics—V_{BIAS} = 5 V

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature: –40°C ≤ T_A ≤ +105°C (TPS22965N-Q1, TPS22965-Q1), –40°C ≤ T_A ≤ +125°C (TPS22965NW-Q1, TPS22965W-Q1). Typical values are for T_A = 25°C.

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
I_Q V_{BIAS}	V_{BIAS} quiescent current	I_{OUT} = 0 mA, V_{IN} = V_{ON} = V_{BIAS} = 5 V		–40°C to +105°C		50	75	µA
				–40°C to +125°C		50	75	
I_{SD} V_{BIAS}	V_{BIAS} shutdown current	V_{ON} = GND, V_{OUT} = 0 V		–40°C to +105°C			2	µA
				–40°C to +125°C			2	
I_{SD} V_{IN}	V_{IN} off-state supply current	V_{ON} = GND, V_{OUT} = 0 V	V_{IN} = 5 V	–40°C to +105°C		0.2	8	µA
				–40°C to +125°C			36	
			V_{IN} = 3.3 V	–40°C to +105°C		0.02	3	
				–40°C to +125°C			13	
			V_{IN} = 1.8 V	–40°C to +105°C		0.01	2	
				–40°C to +125°C			6	
			V_{IN} = 0.8 V	–40°C to +105°C		0.005	1	
				–40°C to +125°C			4	
I_{ON}	ON pin input leakage current	V_{ON} = 5.5 V		–40°C to +105°C			0.5	µA
				–40°C to +125°C			0.5	

7.5 Electrical Characteristics—V_{BIAS} = 5 V (continued)

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature: –40°C ≤ T_A ≤ +105°C (TPS22965N-Q1, TPS22965-Q1), –40°C ≤ T_A ≤ +125°C (TPS22965NW-Q1, TPS22965W-Q1). Typical values are for T_A = 25°C.

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
RESISTANCE CHARACTERISTICS								
R_{ON}	ON-state resistance	I_{OUT} = –200 mA, V_{BIAS} = 5 V	V_{IN} = 5 V	25°C		16	23	mΩ
				–40°C to +105°C 965N-Q1, 965-Q1			25	
				–40°C to +105°C 965NW-Q1, 965W-Q1			26	
				–40°C to +125°C			28	
			V_{IN} = 3.3 V	25°C		16	23	mΩ
				–40°C to +105°C 965N-Q1, 965-Q1			25	
				–40°C to +105°C 965NW-Q1, 965W-Q1			26	
				–40°C to +125°C			27	
			V_{IN} = 1.8 V	25°C		16	23	mΩ
				–40°C to +105°C 965N-Q1, 965-Q1			25	
				–40°C to +105°C 965NW-Q1, 965W-Q1			26	
				–40°C to +125°C			27	
			V_{IN} = 1.5 V	25°C		16	23	mΩ
				–40°C to +105°C 965N-Q1, 965-Q1			25	
				–40°C to +105°C 965NW-Q1, 965W-Q1			26	
				–40°C to +125°C			27	
			V_{IN} = 1.2 V	25°C		16	23	mΩ
				–40°C to +105°C 965N-Q1, 965-Q1			25	
				–40°C to +105°C 965NW-Q1, 965W-Q1			26	
				–40°C to +125°C			27	
			V_{IN} = 0.8 V	25°C		16	23	mΩ
				–40°C to +105°C 965N-Q1, 965-Q1			25	
				–40°C to +105°C 965NW-Q1, 965W-Q1			26	
				–40°C to +125°C			27	
R_{PD} [(1)]	Output pulldown resistance	V_{IN} = 5 V, V_{ON} = 0 V, I_{OUT} = 1 mA		–40°C to +105°C		225	300	Ω
				–40°C to +125°C		225	300	

(1) TPS22965-Q1 and TPS22965W-Q1 only.

7.6 Electrical Characteristics—V_{BIAS} = 2.5 V

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature: –40°C ≤ T_A ≤ +105°C (TPS22965N-Q1, TPS22965-Q1), –40°C ≤ T_A ≤ +125°C (TPS22965NW-Q1, TPS22965W-Q1). Typical values are for T_A = 25°C.

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
I_Q V_{BIAS}	V_{BIAS} quiescent current	I_{OUT} = 0 mA, V_{IN} = V_{ON} = V_{BIAS} = 2.5 V		–40°C to +105°C		20	30	µA
				–40°C to 125°C		20	30	
I_{SD} V_{BIAS}	V_{BIAS} shutdown current	V_{ON} = GND, V_{OUT} = 0 V		–40°C to +105°C			2	µA
				–40°C to 125°C			2	
I_{SD} V_{IN}	V_{IN} off-state supply current	V_{ON} = GND, V_{OUT} = 0 V	V_{IN} = 2.5 V	–40°C to +105°C		0.01	3	µA
				–40°C to 125°C			13	
			V_{IN} = 1.8 V	–40°C to +105°C		0.01	2	
				–40°C to 125°C			6	
			V_{IN} = 1.2 V	–40°C to +105°C		0.005	2	
				–40°C to 125°C			6	
			V_{IN} = 0.8 V	–40°C to +105°C		0.003	1	
				–40°C to 125°C			4	
I_{ON}	ON pin input leakage current	V_{ON} = 5.5 V		–40°C to +105°C			0.5	µA
				–40°C to +125°C			0.5	
RESISTANCE CHARACTERISTICS								

7.6 Electrical Characteristics—V_{BIAS} = 2.5 V (continued)

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature: –40°C ≤ T_A ≤ +105°C (TPS22965N-Q1, TPS22965-Q1), –40°C ≤ T_A ≤ +125°C (TPS22965NW-Q1, TPS22965W-Q1). Typical values are for T_A = 25°C.

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
R_{ON}	ON-state resistance	I_{OUT} = –200 mA, V_{BIAS} = 2.5 V	V_{IN} = 2.5 V	25°C		20	26	mΩ
				–40°C to +105°C 965N-Q1, 965-Q1			28	
				–40°C to 105°C 965NW-Q1, 965W-Q1			32	
				–40°C to +125°C			34	
			V_{IN} = 1.8 V	25°C		19	26	mΩ
				–40°C to +105°C 965N-Q1, 965-Q1			28	
				–40°C to +105°C 965NW-Q1, 965W-Q1			30	
				–40°C to +125°C			32	
			V_{IN} = 1.5 V	25°C		18	25	mΩ
				–40°C to +105°C 965N-Q1, 965-Q1			27	
				–40°C to +105°C 965NW-Q1/965W-Q1			29	
				–40°C to +125°C			31	
			V_{IN} = 1.2 V	25°C		18	25	mΩ
				–40°C to +105°C 965N-Q1, 965-Q1			27	
				–40°C to +105°C 965NW-Q1, 965W-Q1			28	
				–40°C to +125°C			30	
			V_{IN} = 0.8 V	25°C		17	25	mΩ
				–40°C to +105°C 965N-Q1, 965-Q1			27	
				–40°C to +105°C 965NW-Q1, 965W-Q1			28	
				–40°C to +125°C			30	
R_{PD} (1)	Output pulldown resistance	V_{BIAS} = V_{IN} = 2.5 V, V_{ON} = 0 V, I_{OUT} = 1 mA		–40°C to +105°C		275	325	Ω
				–40°C to +125°C			330	
		V_{BIAS} = V_{IN} = 2 V, V_{ON} = 0 V, I_{OUT} = 1 mA		–40°C to +125°C		310	470	Ω

(1) TPS22965-Q1 and TPS22965W-Q1 only.

7.7 Switching Characteristics

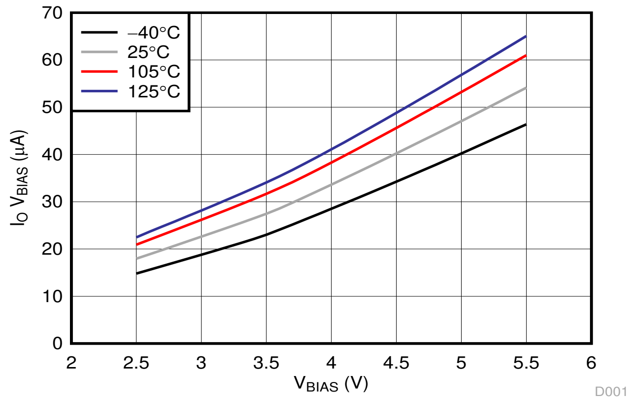
Over operating free-air temperature range (unless otherwise noted). These switching characteristics are only valid for the power-up sequence where VIN and VBIAS are already in steady state condition before the ON pin is asserted high.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN} = V_{ON} = V_{BIAS} = 5 V, T_A = 25°C (unless otherwise noted)						
t_{ON}	Turn-on time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		1600		µs
t_{OFF}	Turn-off time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		9		µs
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		1985		µs
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		3		µs
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		660		µs
V_{IN} = 0.8 V, V_{ON} = V_{BIAS} = 5 V, T_A = 25°C (unless otherwise noted)						
t_{ON}	Turn-on time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		730		µs
t_{OFF}	Turn-off time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		100		µs
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		380		µs
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		8		µs
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		560		µs
V_{IN} = 2.5 V, V_{ON} = 5 V, V_{BIAS} = 2.5 V, T_A = 25°C (unless otherwise noted)						
t_{ON}	Turn-on time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		2435		µs
t_{OFF}	Turn-off time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		9		µs
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		2515		µs
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		4		µs
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		1230		µs
V_{IN} = 0.8 V, V_{ON} = 5 V, V_{BIAS} = 2.5 V, T_A = 25°C (unless otherwise noted)						
t_{ON}	Turn-on time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		1565		µs
t_{OFF}	Turn-off time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		70		µs
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		930		µs
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		8		µs
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		1110		µs

7.8 Typical Characteristics

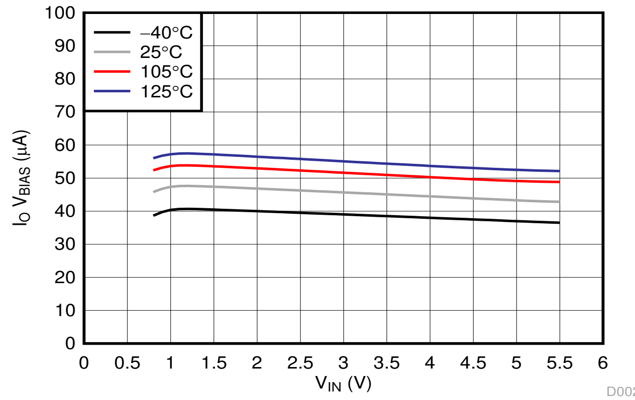
7.8.1 Typical DC Characteristics

T_A = 125°C data is only applicable to TPS22965NW-Q1 and TPS22965W-Q1.



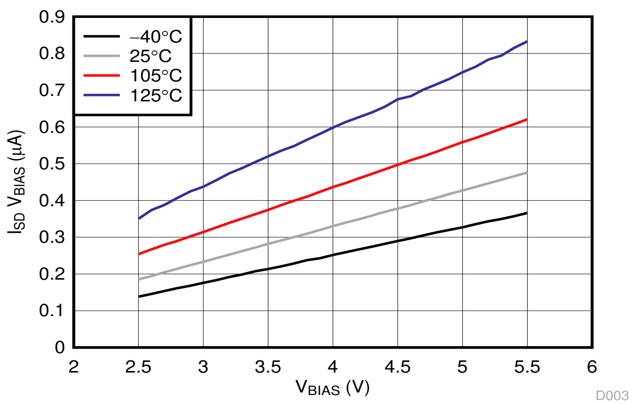
V_{IN} = 1.8 V　V_{ON} = 5 V　V_{OUT} = 0 V

図 7-1. V_{BIAS} Quiescent Current vs V_{BIAS}



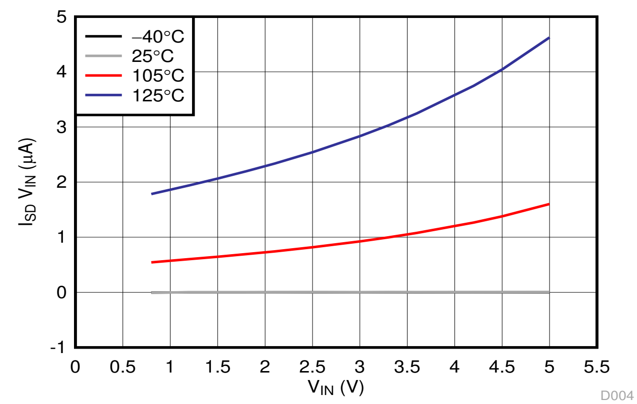
V_{BIAS} = 5 V　V_{ON} = 5 V　V_{OUT} = 0 V

図 7-2. I_Q V_{BIAS} vs V_{IN}



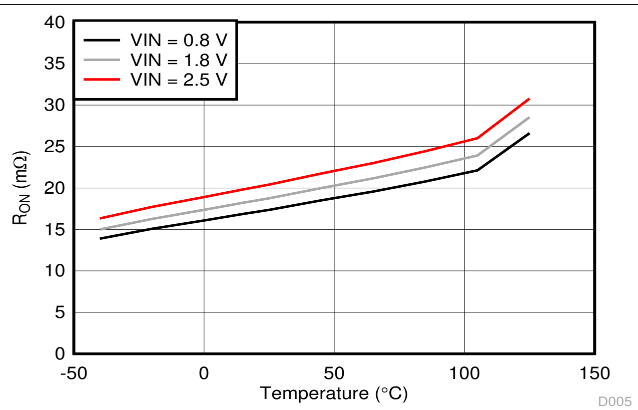
V_{IN} = 5 V　V_{ON} = 0 V　V_{OUT} = 0 V

図 7-3. I_{SD} V_{BIAS} vs V_{BIAS}



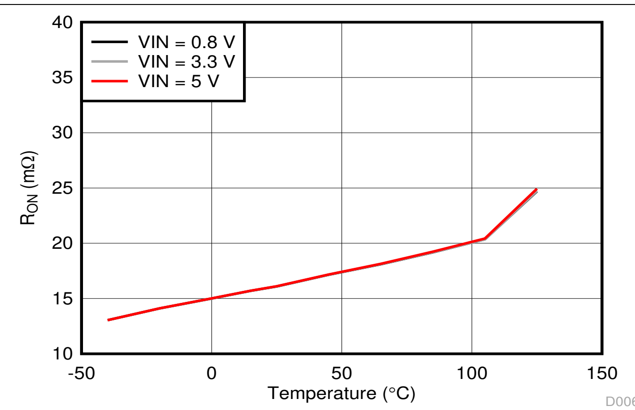
V_{BIAS} = 5 V　V_{ON} = 0 V　V_{OUT} = 0 V

図 7-4. I_{SD} V_{IN} vs V_{IN}



V_{BIAS} = 2.5 V　I_{OUT} = –200 mA　V_{ON} = 5.5 V

図 7-5. R_{ON} vs Ambient Temperature

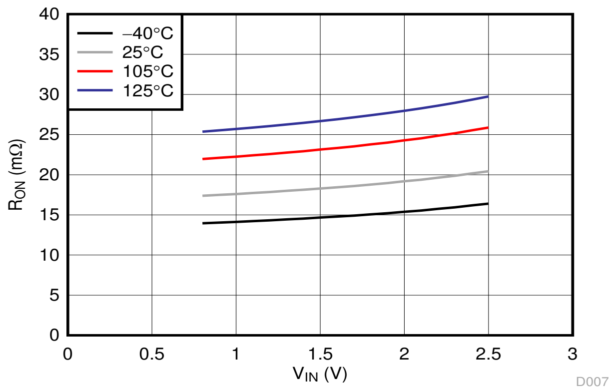


V_{BIAS} = 5 V　I_{OUT} = –200 mA　V_{ON} = 5.5 V

Note: All three R_{ON} curves have the same values; therefore, only one line is visible.

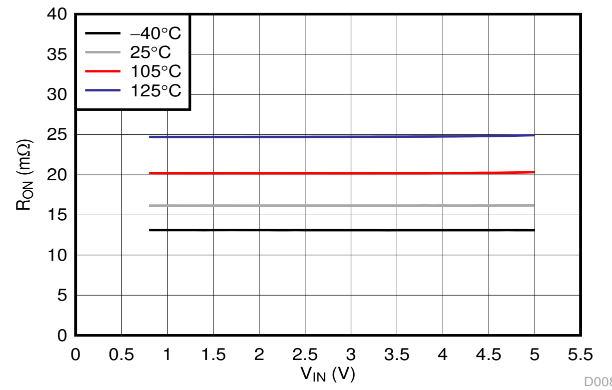
図 7-6. R_{ON} vs Ambient Temperature

7.8.1 Typical DC Characteristics (continued)



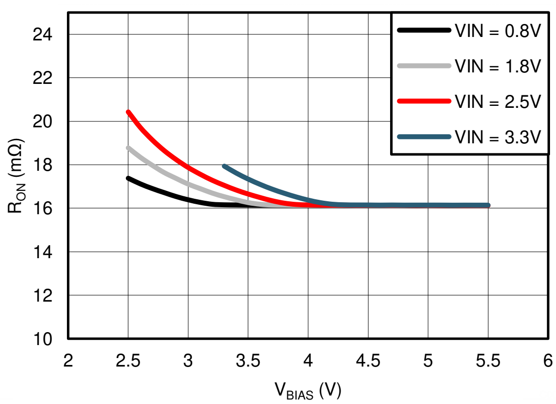
V_{BIAS} = 2.5 V I_{OUT} = –200 mA V_{ON} = 5.5 V

図 7-7. R_{ON} vs V_{IN}



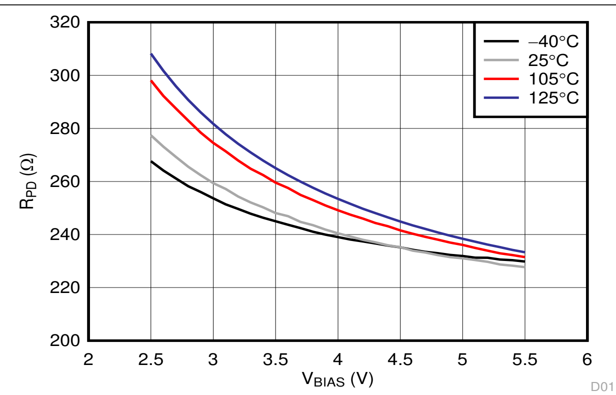
V_{BIAS} = 5 V I_{OUT} = –200 mA V_{ON} = 5.5 V

図 7-8. R_{ON} vs V_{IN}



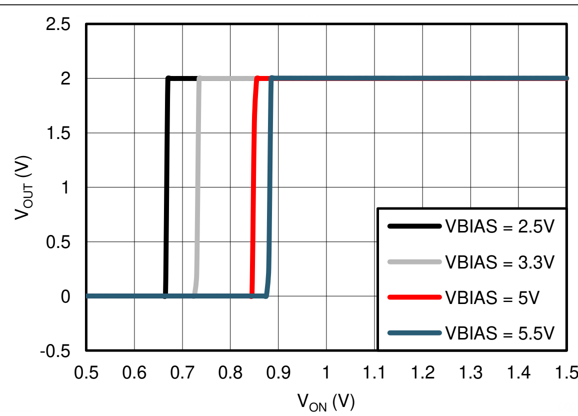
T_A = 25°C I_{OUT} = –200 mA V_{ON} = 5.5 V

図 7-9. R_{ON} vs V_{BIAS}



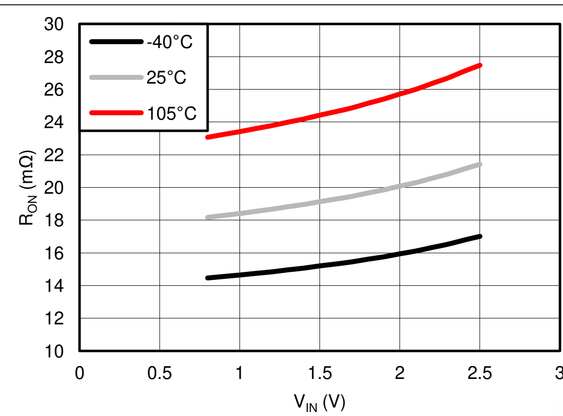
V_{IN} = 1.8 V V_{ON} = 0 V

図 7-10. R_{PD} vs V_{BIAS}



V_{IN} = 2 V T_A = 25°C

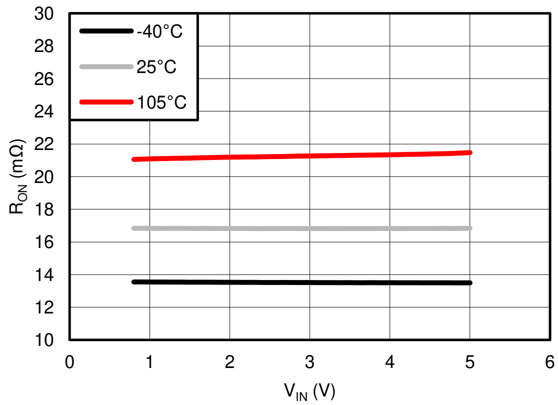
図 7-11. V_{OUT} vs V_{ON}



V_{BIAS} = 2.5 V I_{OUT} = –4 A V_{ON} = 5.5 V

図 7-12. R_{ON} vs V_{IN}

7.8.1 Typical DC Characteristics (continued)

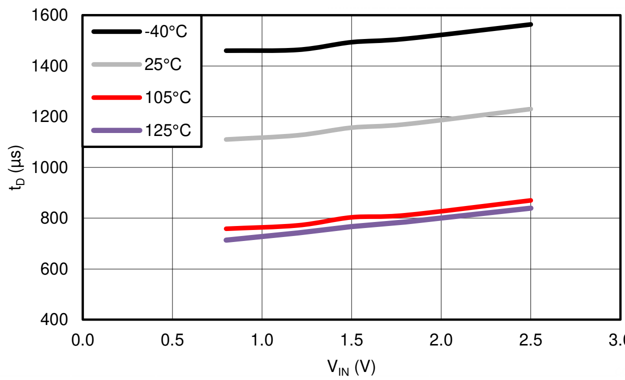


V_{BIAS} = 5 V I_{OUT} = –4 A V_{ON} = 5.5 V

図 7-13. R_{ON} vs V_{IN}

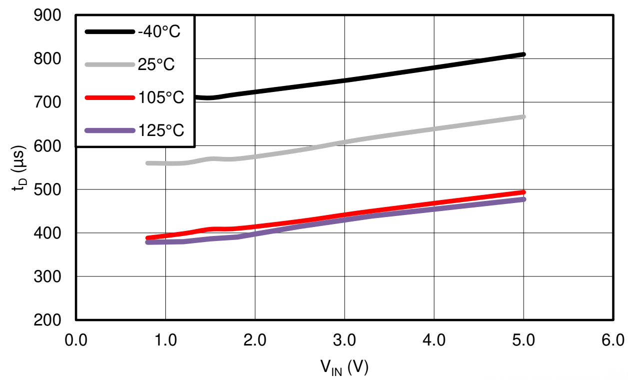
7.8.2 Typical Switching Characteristics

T_A = 25°C, C_T = 1000 pF, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω (unless otherwise specified). T_A = 125°C data is only applicable to TPS22965NW-Q1 and TPS22965W-Q1.



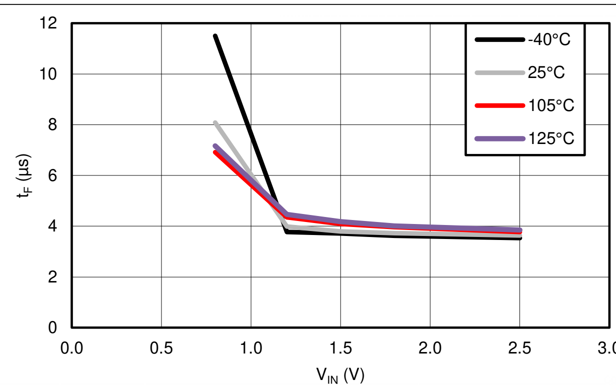
V_{BIAS} = 2.5 V CT = 1000 pF

図 7-14. t_D vs V_{IN}



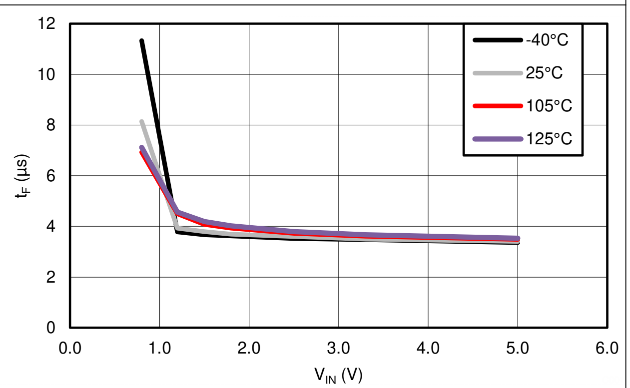
V_{BIAS} = 5 V CT = 1000 pF

図 7-15. t_D vs V_{IN}



V_{BIAS} = 2.5 V CT = 1000 pF

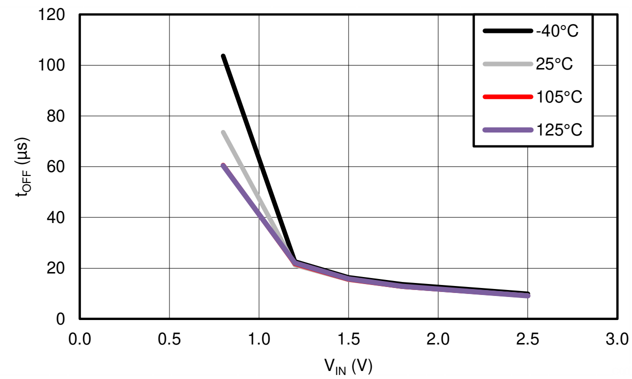
図 7-16. t_F vs V_{IN}



V_{BIAS} = 5 V CT = 1000 pF

図 7-17. t_F vs V_{IN}

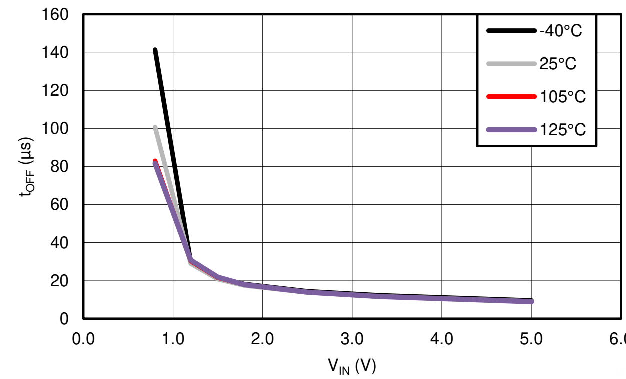
7.8.2 Typical Switching Characteristics (continued)



V_{BIAS} = 2.5 V CT = 1000 pF

Note: The 105°C and 125°C curves have similar values; therefore, only one line is visible.

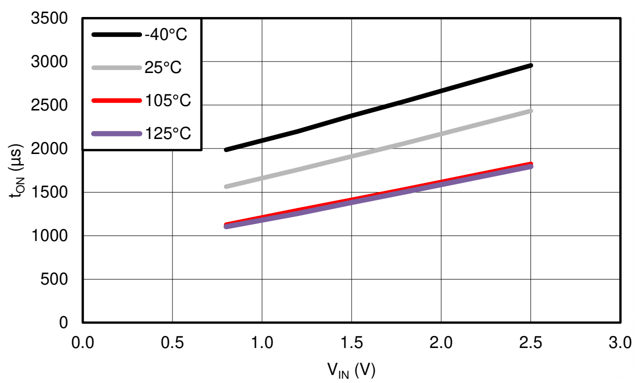
図 7-18. t_{OFF} vs V_{IN}



V_{BIAS} = 5 V CT = 1000 pF

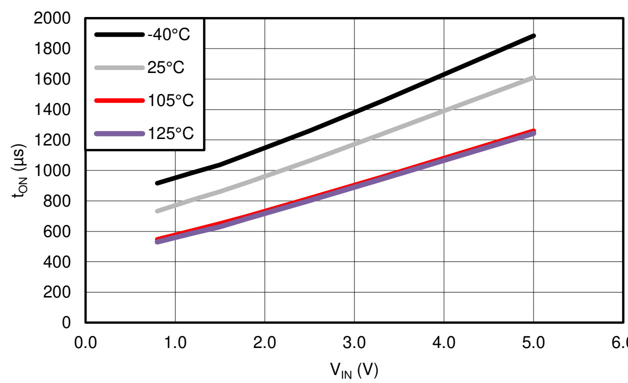
Note: The 105°C and 125°C curves have similar values; therefore, only one line is visible.

図 7-19. t_{OFF} vs V_{IN}



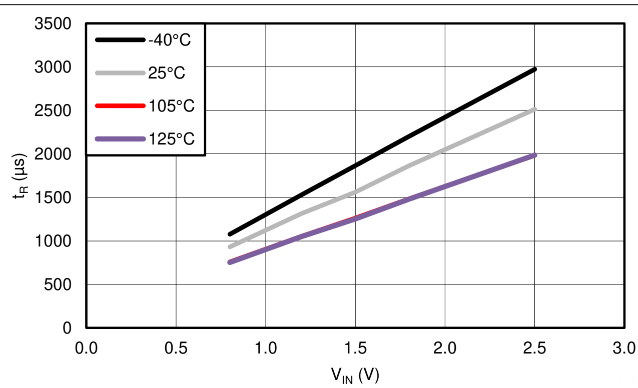
V_{BIAS} = 2.5 V CT = 1000 pF

図 7-20. t_{ON} vs V_{IN}



V_{BIAS} = 5 V CT = 1000 pF

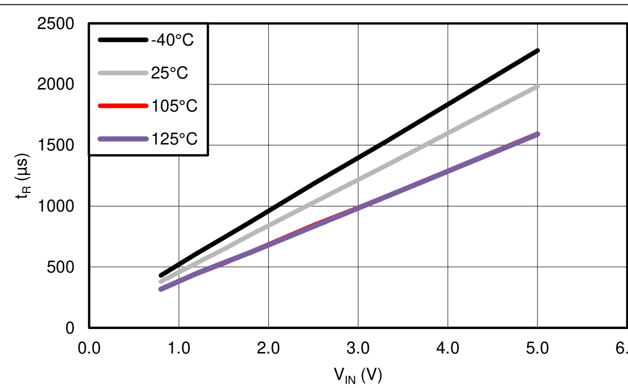
図 7-21. t_{ON} vs V_{IN}



V_{BIAS} = 2.5 V CT = 1000 pF

Note: The 105°C and 125°C curves have similar values; therefore, only one line is visible.

図 7-22. t_R vs V_{IN}

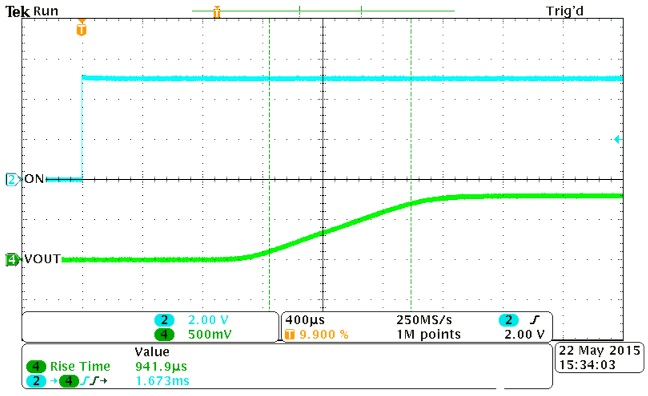


V_{BIAS} = 5 V CT = 1000 pF

Note: The 105°C and 125°C curves have similar values; therefore, only one line is visible.

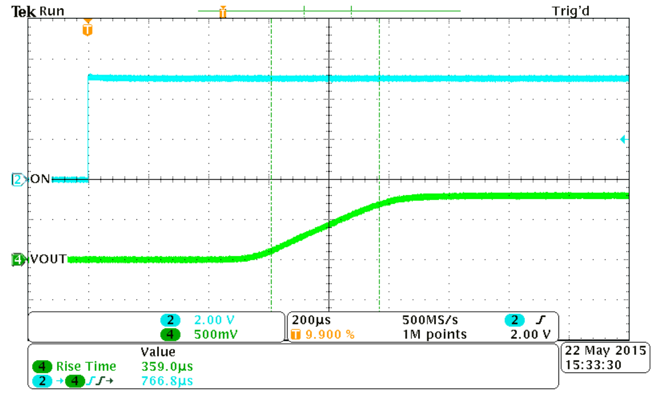
図 7-23. t_R vs V_{IN}

7.8.2 Typical Switching Characteristics (continued)



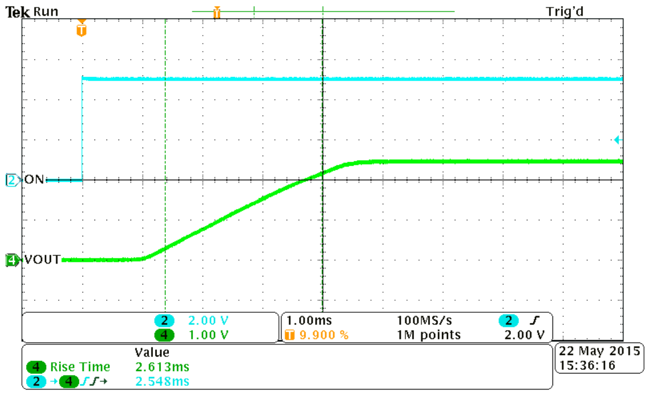
V_{IN} = 0.8 V V_{BIAS} = 2.5 V C_{IN} = 1 µF
C_L = 0.1 µF R_L = 10 Ω CT = 1000 pF

図 7-24. Turn-On Response Time



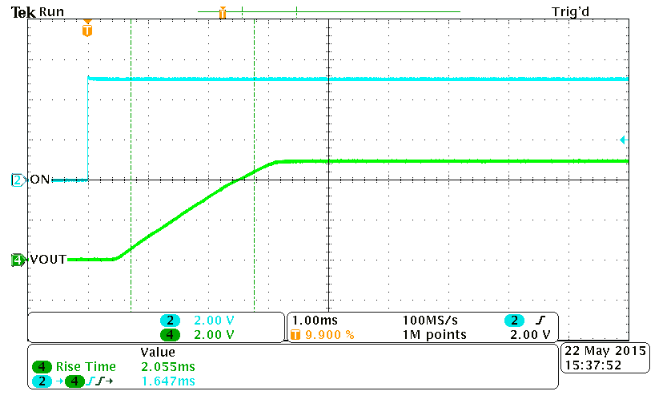
V_{IN} = 0.8 V V_{BIAS} = 5 V C_{IN} = 1 µF
C_L = 0.1 µF R_L = 10 Ω CT = 1000 pF

図 7-25. Turn-On Response Time



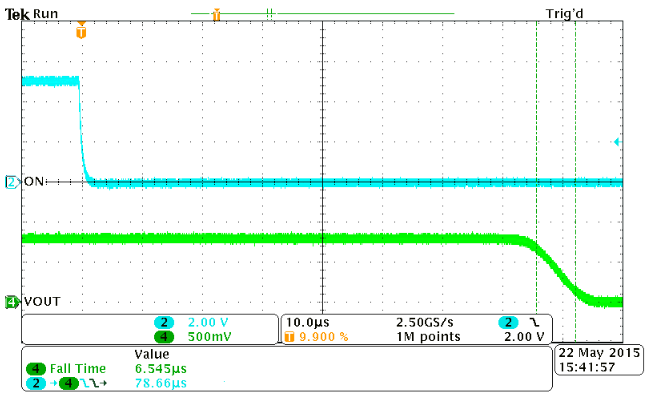
V_{IN} = 2.5 V V_{BIAS} = 2.5 V C_{IN} = 1 µF,
C_L = 0.1 µF R_L = 10 Ω CT = 1000 pF

図 7-26. Turn-On Response Time



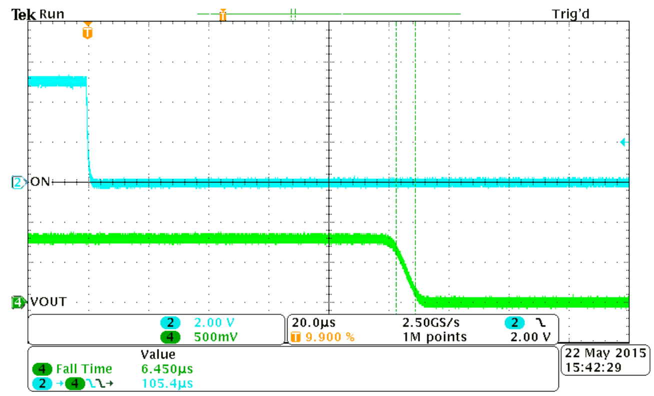
V_{IN} = 5 V V_{BIAS} = 5 V C_{IN} = 1 µF
C_L = 0.1 µF R_L = 10 Ω

図 7-27. Turn-On Response Time



V_{IN} = 0.8 V V_{BIAS} = 2.5 V C_{IN} = 1 µF
C_L = 0.1 µF R_L = 10 Ω

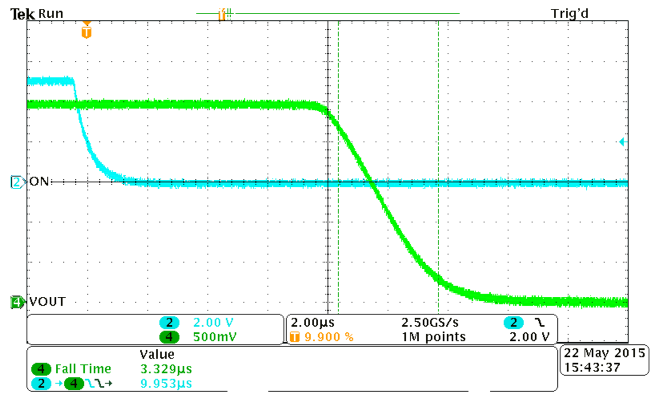
図 7-28. Turn-Off Response Time



V_{IN} = 0.8 V V_{BIAS} = 5 V C_{IN} = 1 µF
C_L = 0.1 µF R_L = 10 Ω

図 7-29. Turn-Off Response Time

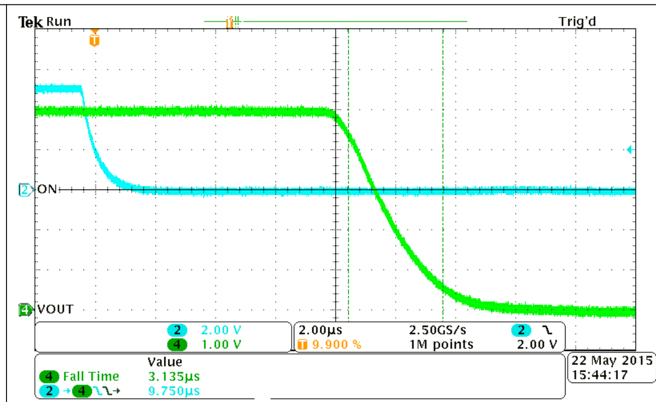
7.8.2 Typical Switching Characteristics (continued)



V_{IN} = 2.5 V V_{BIAS} = 2.5 V C_{IN} = 1 µF

C_L = 0.1 µF R_L = 10 Ω

図 7-30. Turn-Off Response Time

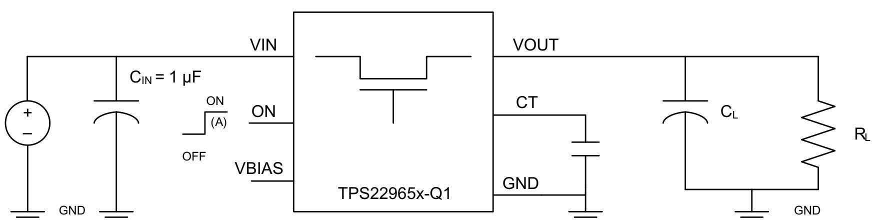


V_{IN} = 5 V V_{BIAS} = 5 V C_{IN} = 1 µF

C_L = 0.1 µF R_L = 10 Ω)

図 7-31. Turn-Off Response Time

8 Parameter Measurement Information



A. Rise and fall times of the control signal are 100 ns.

図 8-1. Test Circuit

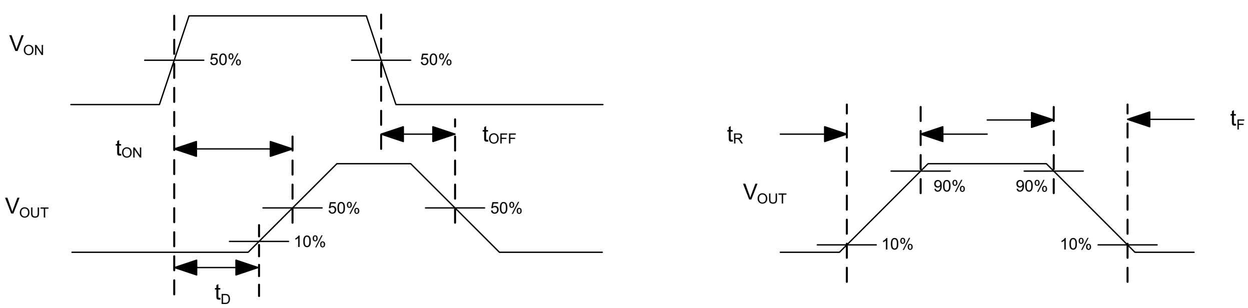


図 8-2. t_{ON} and t_{OFF} Waveforms

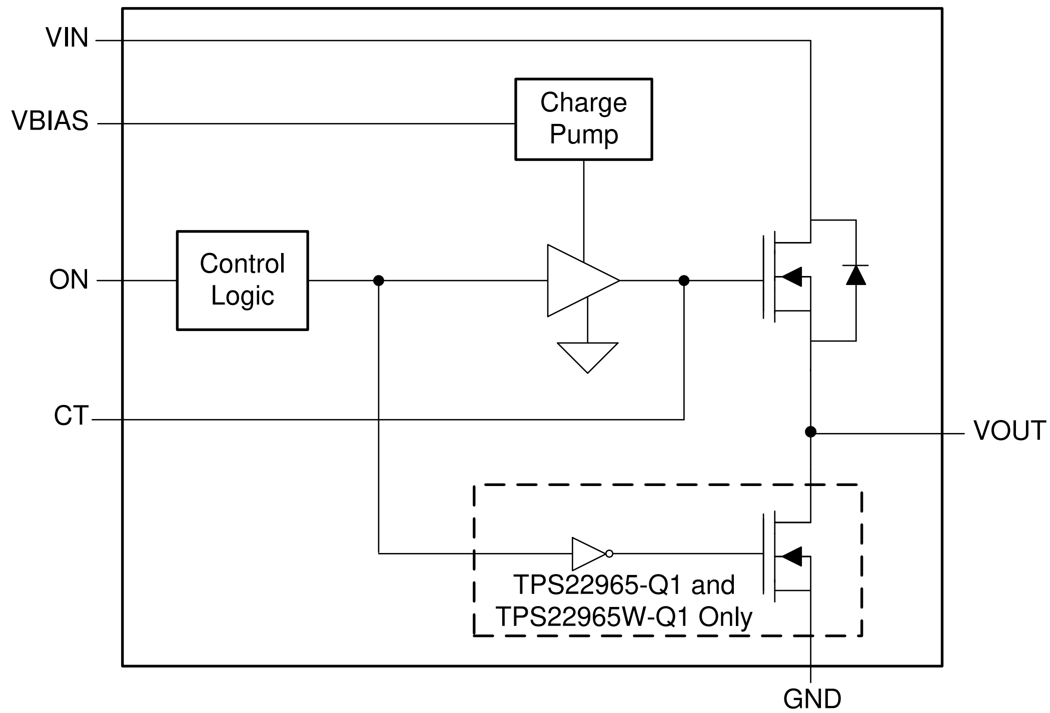
9 Detailed Description

9.1 Overview

The TPS22965x-Q1 is a single-channel, 4-A load switch in an 8-pin WSON package. To reduce the voltage drop in high current rails, the device implements an ultra-low resistance N-channel MOSFET. The device has a programmable slew rate for applications that require specific rise time.

The device has very low leakage current during OFF state. This low leakage prevents downstream circuits from pulling high standby current from the supply. Integrated control logic, driver, power supply, and output discharge FET eliminates the need for any external components, which reduces solution size and BOM count.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Adjustable Rise Time

A capacitor to GND on the CT pin sets the slew rate. The voltage on the CT pin can be as high as 12 V. Therefore, the minimum voltage rating for the CT cap must be 25 V for optimal performance. The below equations shows an approximate formula for the relationship between CT and slew rate when V_{BIAS} is set to 5 V. This equation accounts for 10% to 90% measurement on V_{OUT} and does *not* apply for CT = 0 pF. Use the below equation to determine rise times for when CT = 0 pF.

$$SR = 0.38 \times CT + 34 \quad (1)$$

where

- SR = slew rate (in µs/V).
- CT = the capacitance value on the CT pin (in pF).
- The units for the constant 34 are µs/V. The units for the constant 0.38 are µs/(V × pF).

Rise time can be calculated by multiplying the input voltage by the slew rate. 表 9-1 contains rise time values measured on a typical device. The rise times listed in 表 9-1 are only valid for the power-up sequence where V_{IN} and V_{BIAS} are already in steady state condition before the ON pin is asserted high.

表 9-1. Rise Time vs CT Capacitor

CT (pF)	RISE TIME (µs) 10% - 90%, C_L = 0.1 µF, C_{IN} = 1 µF, R_L = 10 Ω, V_{BIAS} = 5 V (1)						
	VIN = 5 V	VIN = 3.3 V	VIN = 1.8 V	VIN = 1.5 V	VIN = 1.2 V	VIN = 1.05 V	VIN = 0.8 V
0	180	136	94	84	74	70	60
220	547	378	232	202	173	157	129
470	962	654	386	333	282	252	206
1000	1983	1330	765	647	533	476	382
2200	4013	2693	1537	1310	1077	959	766
4700	8207	5490	3137	2693	2200	1970	1590
10000	17700	11767	6697	5683	4657	4151	3350

(1) Typical Values at 25°C with a 25-V X7R 10% Ceramic Capacitor on CT

9.3.2 Quick Output Discharge (TPS22965-Q1 and TPS22965W-Q1 Only)

The TPS22965-Q1 and TPS22965W-Q1 include a Quick Output Discharge (QOD) feature. When the switch is disabled, a discharge resistor is connected between VOUT and GND. This resistor has a typical value of 225 Ω and prevents the output from floating while the switch is disabled.

9.3.3 Low Power Consumption During OFF State

The I_{SD} V_{IN} supply current is 0.01-µA typical at 1.8 V VIN. Typically, the downstream loads must have a significantly higher off-state leakage current. The load switch allows system standby power consumption to be reduced.

9.4 Device Functional Modes

The below table lists the VOUT pin state as determined by the ON pin.

表 9-2. Functional Table

ON	TPS22965N-Q1 AND TPS22965NW-Q1	TPS22965-Q1 AND TPS22965W-Q1
L	Open	GND
H	VIN	VIN

10 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

10.1 Application Information

This section highlights some of the design considerations when implementing this device in various applications. A PSPICE model for this device is also available in the product page of this device on www.ti.com for further aid.

10.1.1 VIN to VOUT Voltage Drop

The VIN to VOUT voltage drop in the device is determined by the R_{ON} of the device and the load current. The R_{ON} of the device depends upon the V_{IN} and V_{BIAS} conditions of the device. Refer to the R_{ON} specification of the device in the *Electrical Characteristics—V_{BIAS} = 2 V to 2.5 V* table of this data sheet. After the R_{ON} of the device is determined based upon the V_{IN} and V_{BIAS} conditions, use the following equation to calculate the VIN to VOUT voltage drop.

$$\Delta V = I_{LOAD} \times R_{ON} \tag{2}$$

where

- ΔV = voltage drop from VIN to VOUT.
- I_{LOAD} = load current.
- R_{ON} = On-resistance of the device for a specific V_{IN} and V_{BIAS} combination.

An appropriate I_{LOAD} must be chosen such that the I_{MAX} specification of the device is not violated.

10.1.2 On and Off Control

The ON pin controls the state of the switch. ON is active high and has a low threshold, making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic thresholds. The ON pin can be used with any microcontroller with 1.2 V or higher GPIO voltage. This pin cannot be left floating and must be driven either high or low for proper functionality.

10.1.3 Input Capacitor (Optional)

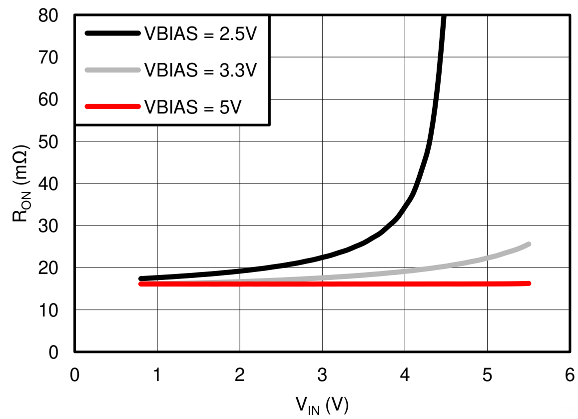
To limit the voltage drop on the input supply caused by transient inrush currents when the switch turns on into a discharged load capacitor or short circuit, a capacitor must be placed between VIN and GND. A 1-µF ceramic capacitor, C_{IN}, placed close to the pins, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high current applications. When switching heavy loads, TI recommends to have an input capacitor about 10 times higher than the output capacitor to avoid excessive voltage drop.

10.1.4 Output Capacitor (Optional)

Due to the integrated body diode in the NMOS switch, TI highly recommends a $C_{I\ N}$ greater than C_L. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This event can result in current flow through the body diode from V_{OUT} to V_{IN}. TI recommends a C_{IN} to C_L ratio of 10 to 1 for minimizing V_{IN} dip caused by inrush currents during startup; however, a 10 to 1 ratio for capacitance is not required for proper functionality of the device. A ratio smaller than 10 to 1 (such as 1 to 1) can cause slightly more V_{IN} dip upon turn-on due to inrush currents. This event can be mitigated by increasing the capacitance on the CT pin for a longer rise time (see the *Adjustable Rise Time* section).

10.1.5 V_{IN} and V_{BIAS} Voltage Range

For optimal R_{ON} performance, make sure $V_{IN} \le V_{BIAS}$. The device is still functional if $V_{IN} > V_{BIAS}$ but it exhibits R_{ON} greater than what is listed in the *Electrical Characteristics—V_{BIAS} = 2 V to 2.5 V* table. See the following figure for an example of a typical device. Notice the increasing R_{ON} as V_{IN} exceeds V_{BIAS} voltage. Be sure to never exceed the maximum voltage rating for V_{IN} and V_{BIAS}.



I_{OUT} = –200 mA T_A = 25°C

図 10-1. R_{ON} vs V_{IN} (V_{IN} > V_{BIAS})

10.2 Typical Application

This application demonstrates how the TPS22965x-Q1 can be used to power downstream modules.

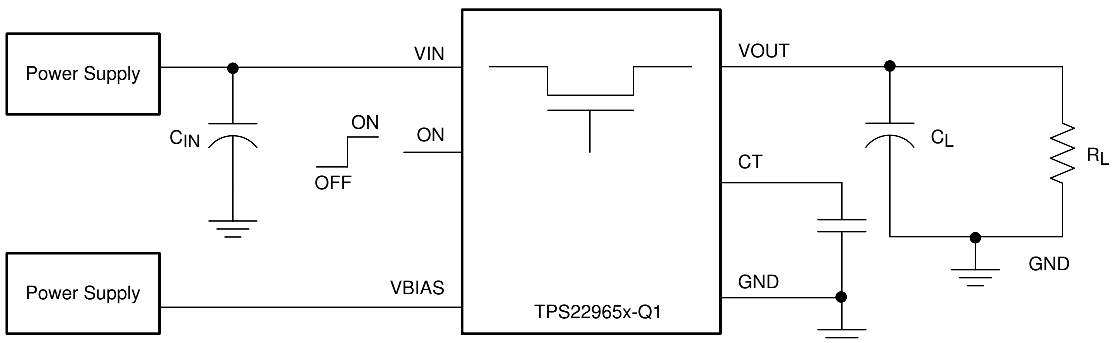


図 10-2. Schematic for Powering a Downstream Module

10.2.1 Design Requirements

Use the values listed in the following table as the design parameters.

表 10-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	3.3 V
V_{BIAS}	5 V
C_L	22 µF
Maximum acceptable inrush current	400 mA

10.2.2 Detailed Design Procedure

10.2.2.1 Inrush Current

When the switch is enabled, the output capacitors must be charged up from 0 V to the set value (3.3 V in this example). This charge arrives in the form of inrush current. Use the following equation to calculate inrush current.

$$\text{Inrush Current} = C \times dV/dt \tag{3}$$

where

- C = output capacitance
- dV = output voltage
- dt = rise time

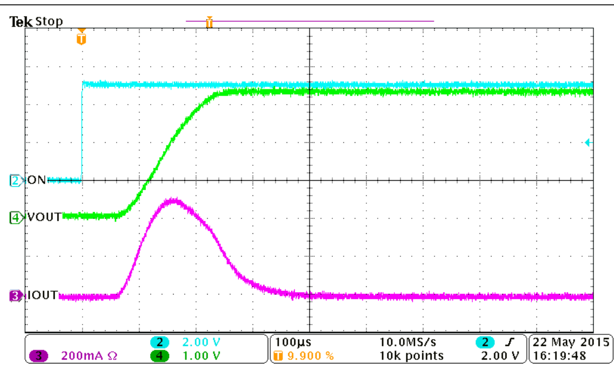
The TPS22965x-Q1 offers adjustable rise time for VOUT. This feature allows the user to control the inrush current during turn-on. The appropriate rise time can be calculated using the design requirements and the inrush current equation. See 式 4 and 式 5.

$$400\text{ mA} = 22\ \mu\text{F} \times 3.3\text{ V} / dt \tag{4}$$

$$dt = 181.5\ \mu\text{s} \tag{5}$$

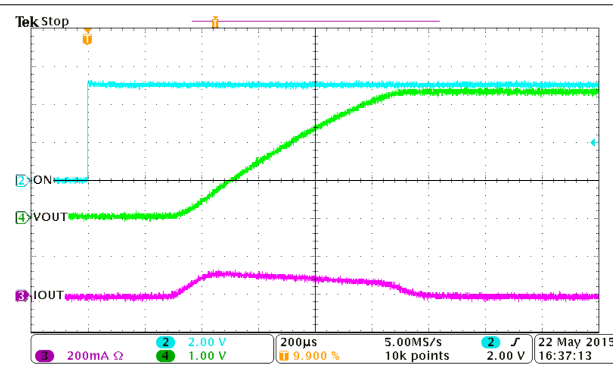
To ensure an inrush current of less than 400 mA, choose a CT value that yields a rise time of more than 181.5 µs. See the oscilloscope captures in the *Application Curves* section for an example of how the CT capacitor can be used to reduce inrush current.

10.2.3 Application Curves



V_{BIAS} = 5 V V_{IN} = 3.3 V C_L = 22 µF

図 10-3. Inrush Current with CT = 0 pF



V_{BIAS} = 5 V V_{IN} = 3.3 V C_L = 22 µF

図 10-4. Inrush Current with CT = 220 pF

11 Power Supply Recommendations

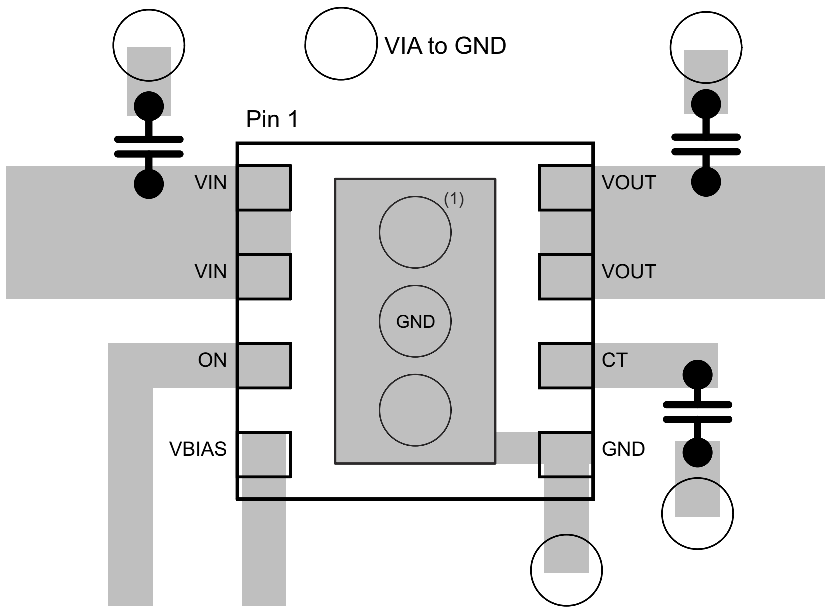
The device is designed to operate from a VBIAS range of 2 V to 5.5 V and a VIN range of 0.8 V to VBIAS.

12 Layout

12.1 Layout Guidelines

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances can have on normal operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance. The CT trace must be as short as possible to avoid parasitic capacitance.

12.2 Layout Example



A. Thermal relief vias. Thermal relief vias connected to the exposed thermal pad.

図 12-1. Layout Recommendation

12.3 Thermal Consideration

The maximum IC junction temperature must be restricted to 150°C under normal operating conditions. Use the below equation as a guideline to calculate the maximum allowable dissipation, $P_{D(max)}$, for a given output current and ambient temperature.

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{\theta_{JA}} \quad (6)$$

where

- $P_{D(max)}$ = maximum allowable power dissipation.
- $T_{J(max)}$ = maximum allowable junction temperature (150°C for the TPS22965x-Q1).
- T_A = ambient temperature of the device.
- Θ_{JA} = junction to air thermal impedance. See the *Thermal Information* table. This parameter is highly dependent upon board layout.

Refer to 図 12-1. Notice the thermal vias located under the exposed thermal pad of the device. The thermal vias allow for thermal diffusion away from the device.

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Load Switches: What Are They, Why Do You Need Them And How Do You Choose The Right One?* application note
- Texas Instruments, *Load Switch Thermal Considerations* application note
- Texas Instruments, *Managing Inrush Current* application note
- Texas Instruments, *TPS22965WDSGQ1EVM 5.7-V, 4-A, 16-mΩ On-Resistance Load Switch* user's guide

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 サポート・リソース

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13.4 Trademarks

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13.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS22965NQWDSGRQ1	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	11B
TPS22965NQWDSGRQ1.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	11B
TPS22965NQWDSGTQ1	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	11B
TPS22965NQWDSGTQ1.A	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	11B
TPS22965NTDSGRQ1	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ZDXI
TPS22965NTDSGRQ1.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZDXI
TPS22965QWDSGRQ1	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	11A
TPS22965QWDSGRQ1.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	11A
TPS22965QWDSGTQ1	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	11A
TPS22965QWDSGTQ1.A	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	11A
TPS22965TDSGRQ1	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ZYE
TPS22965TDSGRQ1.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZYE
TPS22965TDSGTQ1	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ZYE
TPS22965TDSGTQ1.A	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZYE

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TPS22965-Q1 :

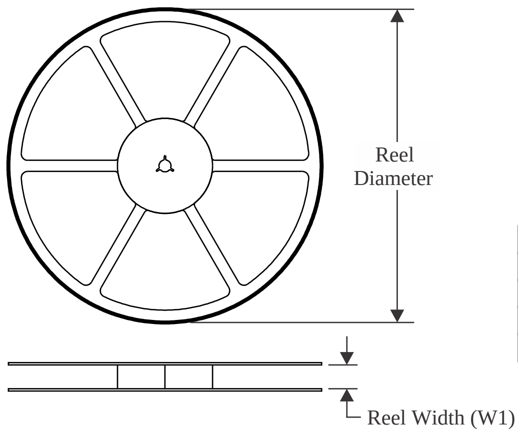
- Catalog : TPS22965

NOTE: Qualified Version Definitions:

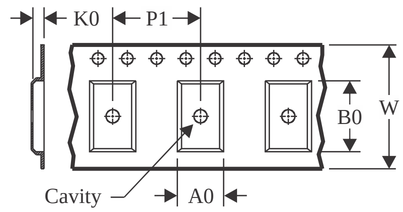
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

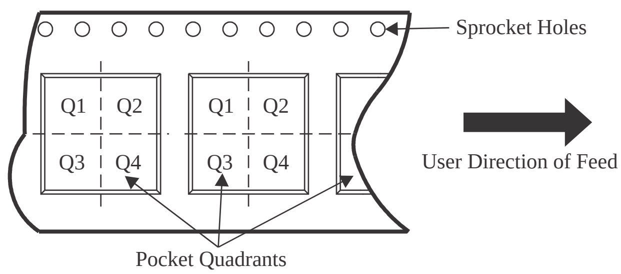


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

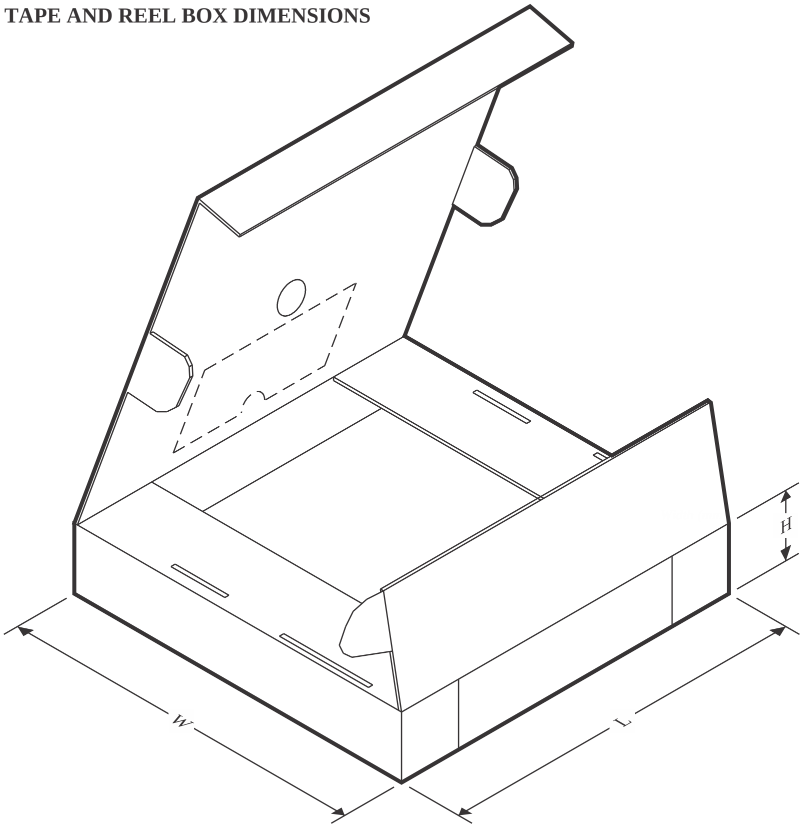
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22965NQWDSGRQ1	WSON	DSG	8	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS22965NQWDSGTQ1	WSON	DSG	8	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS22965NTDSGRQ1	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS22965QWDSGRQ1	WSON	DSG	8	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS22965QWDSGTQ1	WSON	DSG	8	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS22965TDSGRQ1	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS22965TDSGTQ1	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

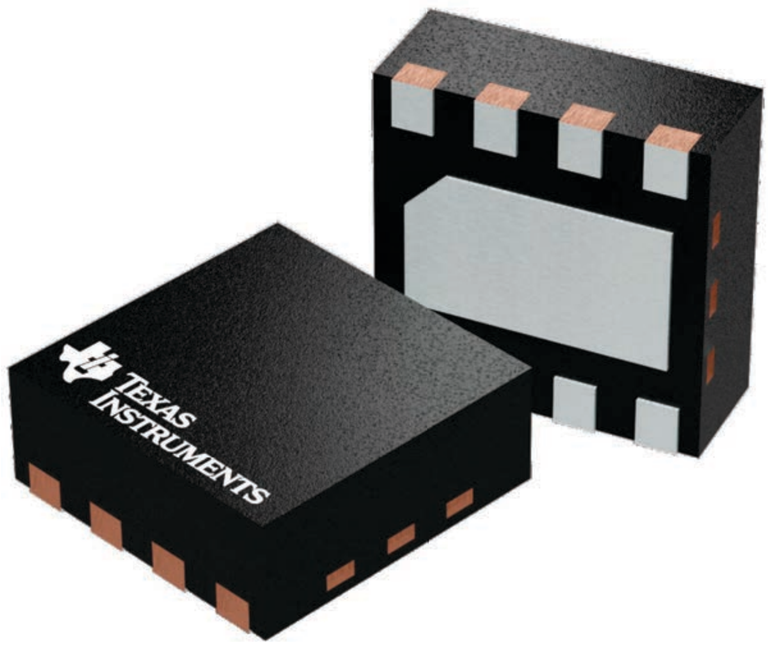
TAPE AND REEL BOX DIMENSIONS

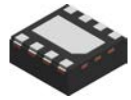


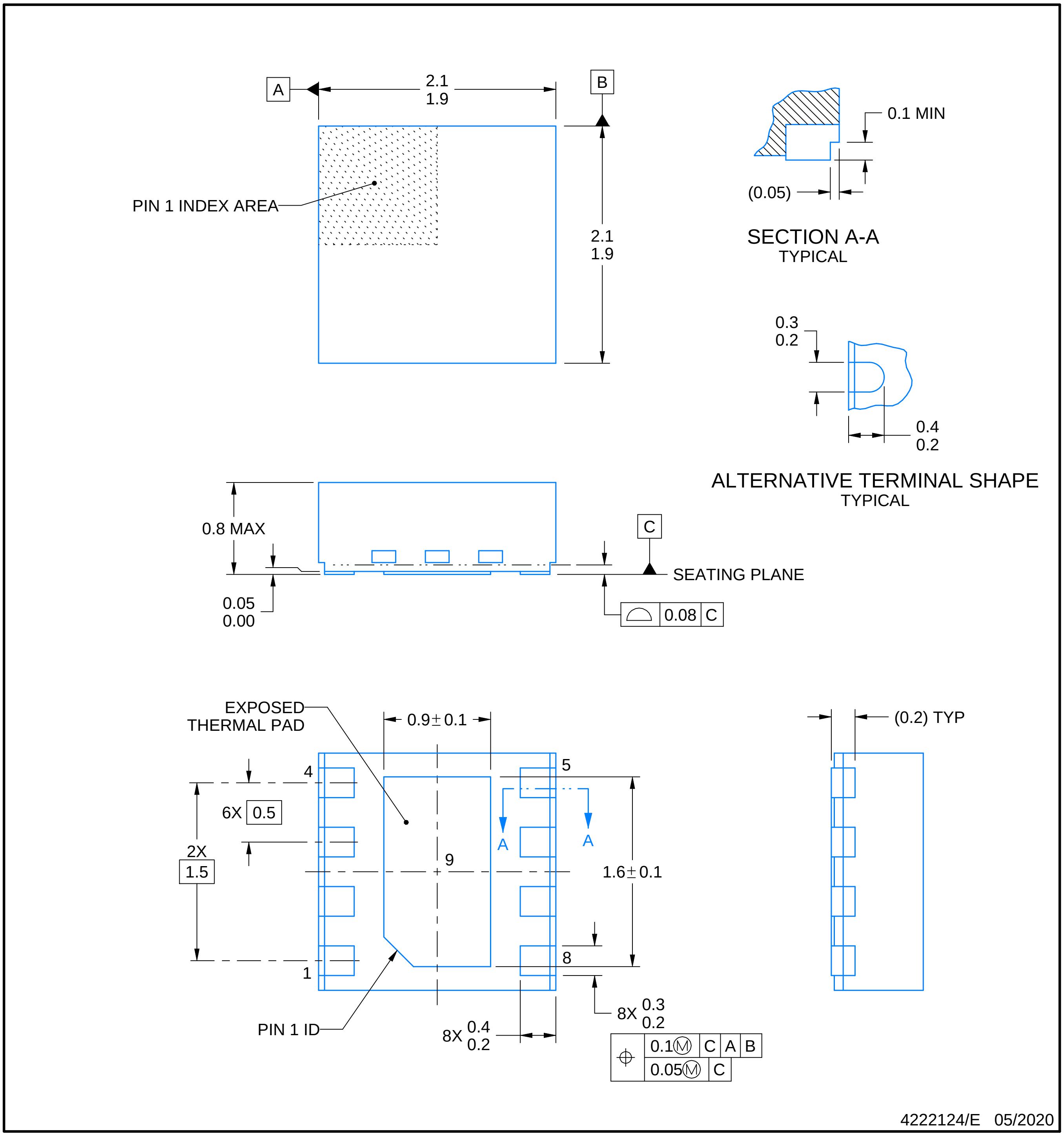
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22965NQWDSGRQ1	WSON	DSG	8	3000	213.0	191.0	35.0
TPS22965NQWDSGTQ1	WSON	DSG	8	250	213.0	191.0	35.0
TPS22965NTDSGRQ1	WSON	DSG	8	3000	210.0	185.0	35.0
TPS22965QWDSGRQ1	WSON	DSG	8	3000	213.0	191.0	35.0
TPS22965QWDSGTQ1	WSON	DSG	8	250	213.0	191.0	35.0
TPS22965TDSGRQ1	WSON	DSG	8	3000	210.0	185.0	35.0
TPS22965TDSGTQ1	WSON	DSG	8	250	210.0	185.0	35.0

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

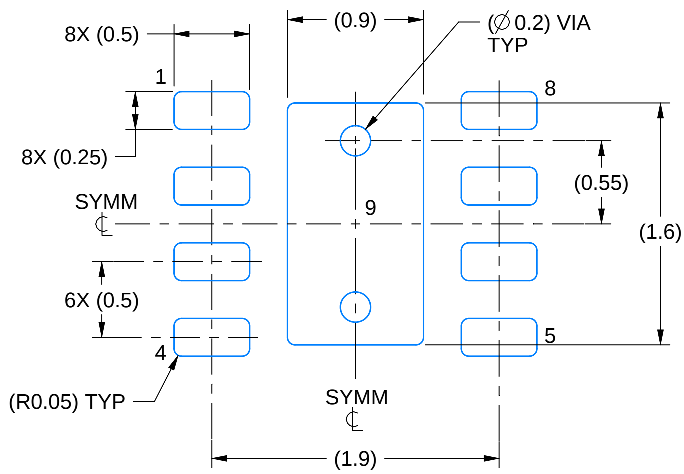




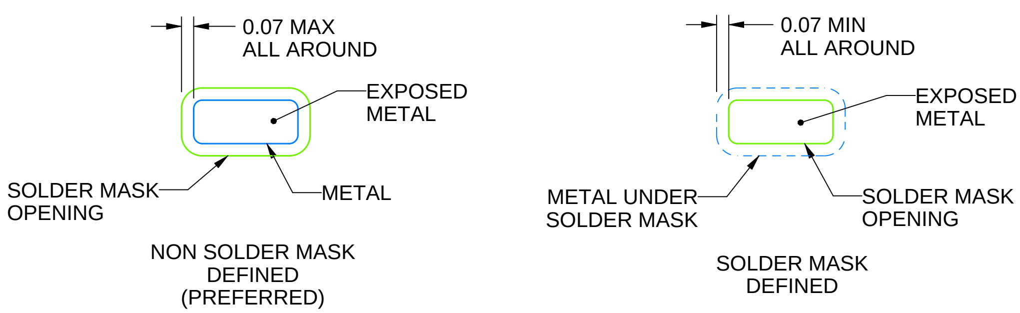


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

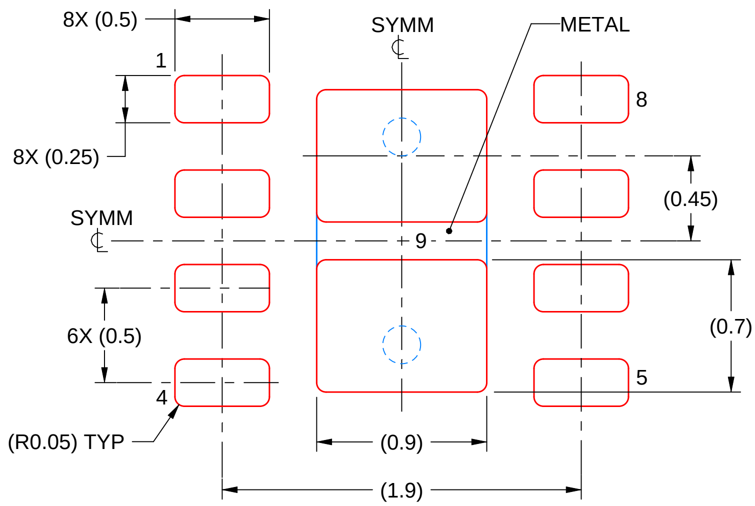


SOLDER MASK DETAILS

4222124/E 05/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4222124/E 05/2020

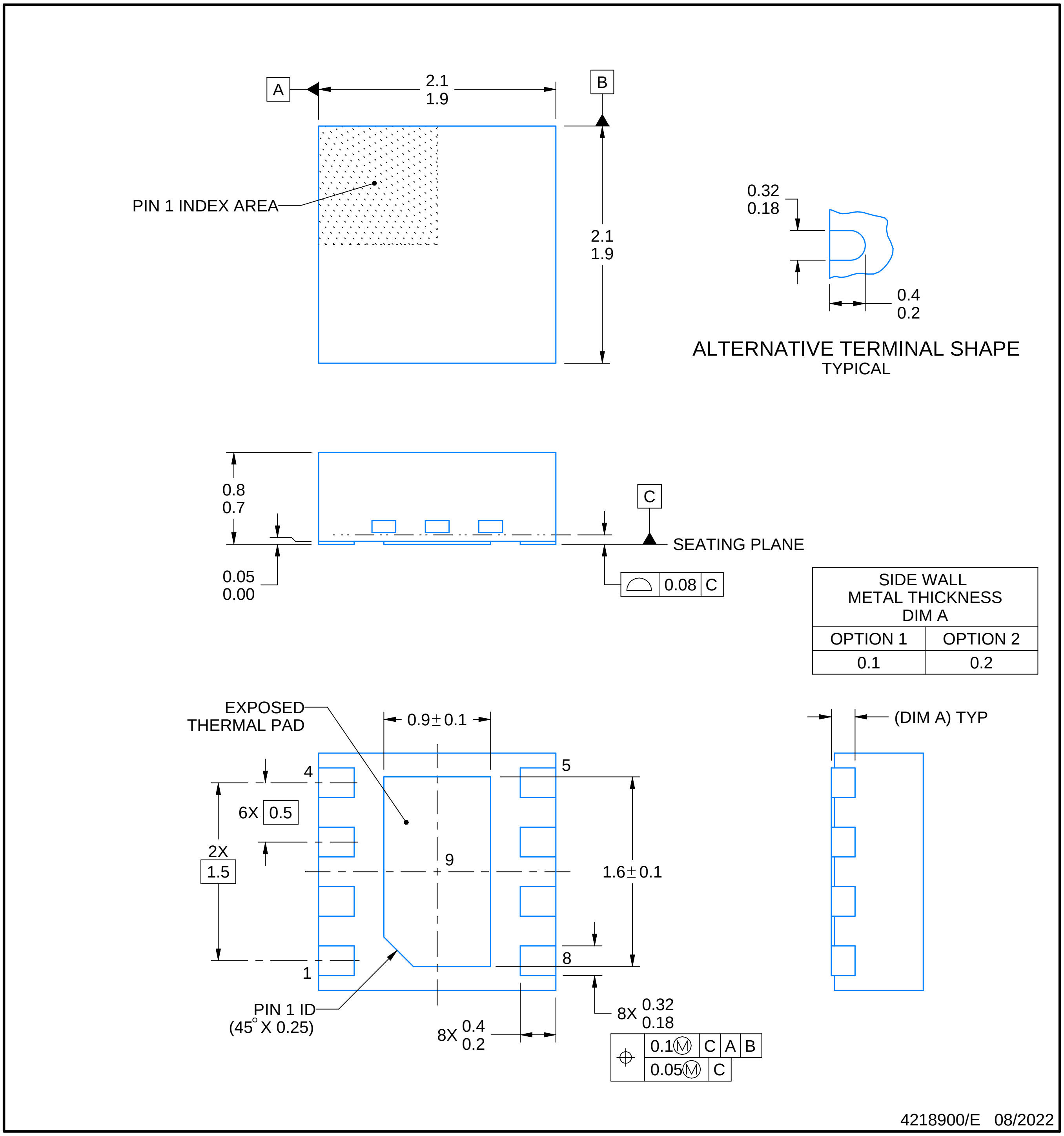
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

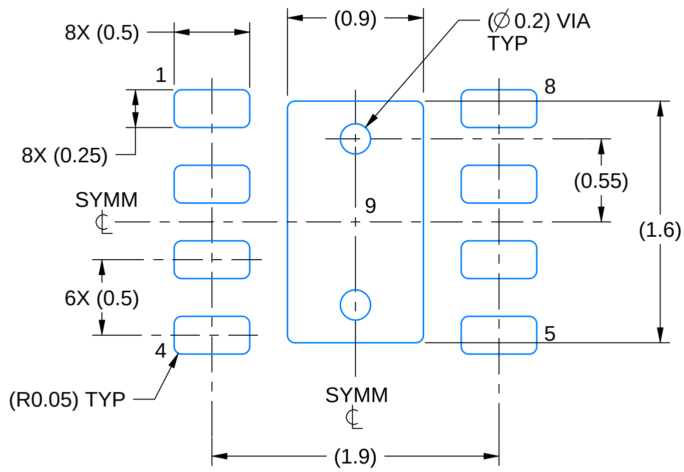
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

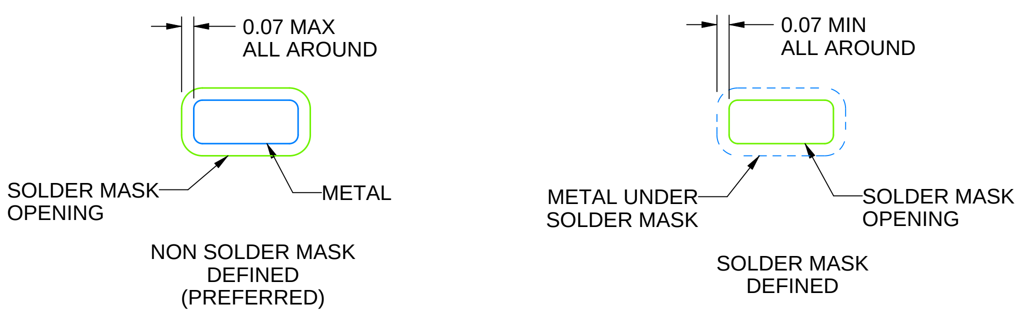


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

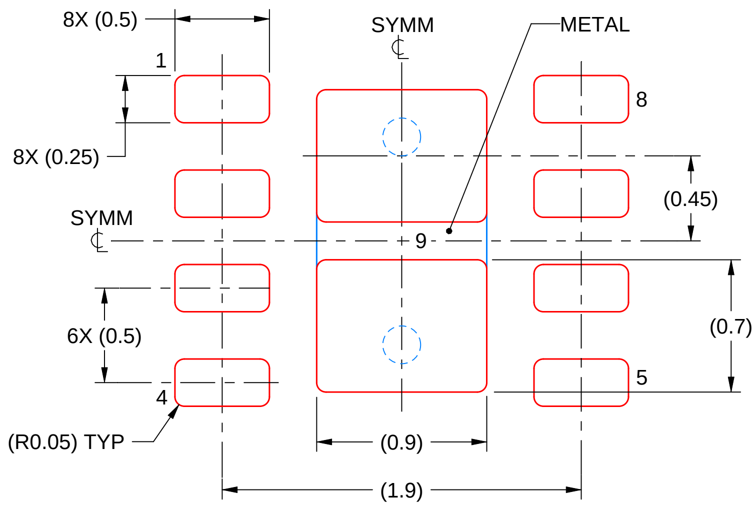


SOLDER MASK DETAILS

4218900/E 08/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/E 08/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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