TPS22916xx 1V～5.5V、2A、60mΩ、超低リーク負荷スイッチ

1 特長

- 動作入力電圧範囲 (V_{IN}):1V～5.5V
- 最大連続電流 (I_{MAX}):2A
- オン抵抗 (R_{ON}):
  - $5V_{IN}$ = 60mΩ (標準値)、100mΩ (最大 85℃)
  - $1.8V_{IN}$ = 100mΩ (標準値)、150mΩ (最大 85℃)
  - $1V_{IN}$ = 200mΩ (標準値)、325mΩ (最大 85℃)
- 超低消費電力:
  - オン状態 (I_Q):0.5μA (標準値)、1μA (最大値)
  - オフ状態 (I_{SD}):10nA (標準値)、100nA (最大値)
  - TPS22916BL/CL/CNL (I_{SD}):100nA (標準値)、300nA (最大値)
- ON ピンのスマート・プルダウン (R_{PD}):
  - ON ≥ V_{IH} (I_{ON}):10nA (最大値)
  - ON ≤ V_{IL} (R_{PD}):750kΩ (標準値)
- C バージョンでは低速なタイミングにより突入電流を制限
  - 5V ターンオン時間 (t_{ON}):1400μs (5mV/μs 時)
  - 1.8V ターンオン時間 (t_{ON}):3000μs (1mV/μs 時)
  - 1V ターンオン時間 (t_{ON}):6500μs (0.3mV/μs 時)
- B バージョンでは高速なタイミングによりウェイト時間を短縮
  - 5V ターンオン時間 (t_{ON}):115μs (57mV/μs 時)
  - 1.8V ターンオン時間 (t_{ON}):250μs (12mV/μs 時)
  - 1V ターンオン時間 (t_{ON}):510μs (3.3mV/μs 時)
- 常時オンの真の逆電流ブロック (RCB):
  - アクティブ化電流 (I_{RCB}):–500mA (標準値)
  - 逆リーク電流 ($I_{IN,RCB}$):–300nA (最大値)
- クイック出力放電 (QOD):150Ω (標準値)
  (N バージョンは QOD なし)
- アクティブ LOW のイネーブル・オプション (L バージョン)

2 アプリケーション

- ウェアラブル
- スマートフォン
- タブレット
- ポータブル・スピーカ

3 概要

TPS22916xx は小型のシングル・チャネル負荷スイッチで、リーク電流の低い P チャネル MOSFET を使用し、電力損失を最小限に抑えています。高度なゲート制御設計により、最低 1V の電圧で動作し、オン抵抗と電力損失の増大は最小限です。

各種のシステム負荷条件に対応するため、複数のタイミング・オプションが利用可能です。大きな容量性の負荷では、C バージョンの低速ターンオン・タイミングを使用して、突入電流を最小化できます。小さな容量性の負荷では、B バージョンの高速なタイミングにより、必要なウェイト時間を短縮できます。

スイッチのオン状態はデジタル入力により制御され、この入力は低電圧の制御信号と直接接続できます。アクティブ HIGH とアクティブ LOW (L) の両方のバージョンが利用可能です。電源が最初に印加されたときには、スマート・プルダウンを使用して、システムのシーケンシングが完了するまで、ON ピンがフローティング状態になることが防止されます。ON ピンが意図的に HIGH (≥ V_{IH}) に駆動された後、不必要な電力損失を避けるため、スマート・プルダウンは切断されます。

TPS22916xx は、小型で省スペースの 0.78mm × 0.78mm、0.4mm ピッチ、0.5mm 高さの 4 ピン・ウェハー・チップ・スケール (WCSP) パッケージ (YFP) で供給されます。このデバイスは、–40℃～+85℃の温度範囲での動作が規定されています。

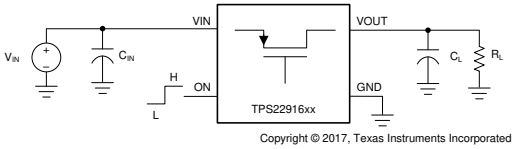
製品情報(1)

部品番号	パッケージ	本体サイズ (公称)
TPS22916xx	WCSP (4)	0.78mm × 0.78mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。

デバイス比較表

バージョン	タイミング	QOD	イネーブル (ON)
TPS22916B	高速	○	アクティブ HIGH
TPS22916BL	高速	○	アクティブ LOW
TPS22916C	低速	○	アクティブ HIGH
TPS22916CN	低速	×	アクティブ HIGH
TPS22916CL	低速	○	アクティブ LOW
TPS22916CNL	低速	×	アクティブ LOW



概略回路図

Table of Contents

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision E (September 2020) to Revision F (December 2021)	Page
• TPS22916CNL および TPS22916BL 注文可能部品をデータシートに追加	1

Changes from Revision D (October 2019) to Revision E (September 2020)	Page
• 文書全体にわたって表、図、相互参照の採番方法を更新	1

Changes from Revision C (October 2018) to Revision D (October 2019)	Page
• パッケージの寸法を 0.74mm × 0.74mm から 0.78mm × 0.78mm に変更	1

Changes from Revision B (December 2017) to Revision C (October 2018)	Page
• Changed Package Drawing Dimensions	21

Changes from Revision A (September 2017) to Revision B (December 2017)	Page
• レーザー・マーキングと表示されたピン配置図を変更	1

Changes from Revision * (July 2017) to Revision A (September 2017)	Page
• デバイスのドキュメントを「事前情報」から「量産データ」に変更	1

5 Pin Configuration and Functions

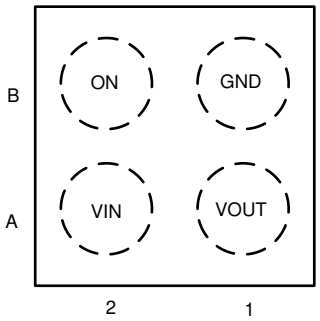


図 5-1. YFP Package 4-Pin WSON Laser Marking View

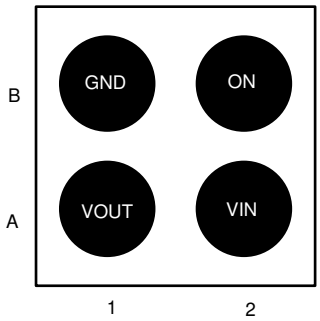


図 5-2. YFP Package 4-Pin WSON Bump View

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
A1	VOUT	Power	Switch output
A2	VIN	Power	Switch input
B1	GND	Ground	Device ground
B2	ON	Digital input	Device enable

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN}	Input voltage	–0.3	6	V
V_{OUT}	Output voltage	–0.3	6	V
V_{ON}	Enable voltage	–0.3	6	V
I_{MAX}	Maximum continuous switch current		2	A
I_{PLS}	Maximum pulsed switch current, pulse < 300-µs, 2% duty cycle		2.5	A
$T_{J,MAX}$	Maximum junction temperature		125	°C
T_{STG}	Storage temperature	–65	150	°C
T_{LEAD}	Maximum Lead temperature (10-s soldering time)		300	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±500 V may actually have higher performance.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input voltage	1	5.5	V
V_{OUT}	Output voltage	0	5.5	V
V_{IH}	High-level input voltage, ON	1	5.5	V
V_{IL}	Low-level input voltage, ON	0	0.35	V
T_A	Operating free-air temperature	–40	85	°C

6.4 Thermal Information

Thermal Parameters(1)		TPS22916xx YFP (WCSP) 4 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	193	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	2.3	°C/W
θ_{JB}	Junction-to-board thermal resistance	36	°C/W
ψ_{JT}	Junction-to-top characterization parameter	12	°C/W
ψ_{JB}	Junction-to-board characterization parameter	36	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Unless otherwise noted, the specification in the following table applies for all variants over the entire recommended power supply voltage range of 1 V to 5.5 V unless noted otherwise. Typical Values are at 25°C.

PARAMETER		TEST CONDITIONS		T_J	MIN	TYP	MAX	UNIT
INPUT SUPPLY (VIN)								
$I_{Q,VIN}$	V_{IN} Quiescent current	Enabled, V_{OUT} = Open		–40°C to +85°C		0.5	1.0	µA
$I_{SD,VIN}$	V_{IN} Shutdown current	Disabled, V_{OUT} = GND (TPS22916B/C/CN)		–40°C to +85°C		10	100	nA
		Disabled, V_{OUT} = GND (TPS22916BL/CL/CNL)		–40°C to +85°C		100	300	nA
ON-RESISTANCE (R_{ON})								
R_{ON}	ON-Resistance	I_{OUT} = 200 mA	V_{IN} = 5 V	25°C		60	80	mΩ
				–40°C to +85°C			100	
				–40°C to +105°C			120	
			V_{IN} = 3.6 V	25°C		70	90	
				–40°C to +85°C			120	
				–40°C to +105°C			140	
			V_{IN} = 1.8 V	25°C		100	125	
				–40°C to +85°C			150	
				–40°C to +105°C			175	
			V_{IN} = 1.2 V	25°C		150	200	
				–40°C to +85°C			250	
				–40°C to +105°C			300	
			V_{IN} = 1 V	25°C		200	275	
				–40°C to +85°C			325	
				–40°C to +105°C			375	
ENABLE PIN (ON)								
I_{ON}	ON Pin leakage	Enabled		–40°C to +85°C	–10		10	nA
R_{PD}	Smart Pull Down Resistance	Disabled		–40°C to +85°C		750		kΩ
REVERSE CURRENT BLOCKING (RCB)								
I_{RCB}	RCB Activation Current	Enabled, $V_{OUT} > V_{IN}$		–40°C to +85°C		-500		mA
t_{RCB}	RCB Activation time	Enabled, $V_{OUT} > V_{IN}$ + 200mV		–40°C to +85°C		10		µs
V_{RCB}	RCB Release Voltage	Enabled, $V_{OUT} > V_{IN}$		–40°C to +85°C		25		mV
$I_{IN,RCB}$	VIN Reverse Leakage Current	0 V ≤ V_{IN} + V_{RCB} ≤ V_{OUT} ≤ 5.5 V		–40°C to +85°C	–300			nA
QUICK OUTPUT DISCHARGE (QOD)								
QOD(1)	Output discharge resistance	Disabled (Not in TPS22916CN/CNL)		–40°C to +85°C		150		Ω

(1) For more information on which devices include quick output discharge, see the *Device Functional Modes* section.

6.6 Switching Characteristics

Unless otherwise noted, the typical characteristics in the following table applies over the entire recommended power supply voltage range of 1 V to 5.5 V at 25°C with a load of C_L = 0.1µF, R_L = 10Ω.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TPS22916B, TPS22916BL						
t_{ON}	Turn On Time	V_{IN} = 5 V		115		µs
		V_{IN} = 3.6 V		140		
		V_{IN} = 1.8 V		250		
		V_{IN} = 1.2 V		350		
		V_{IN} = 1 V		510		
t_{RISE}	Rise Time	V_{IN} = 5 V		70		µs
		V_{IN} = 3.6 V		80		
		V_{IN} = 1.8 V		130		
		V_{IN} = 1.2 V		190		
		V_{IN} = 1 V		240		
SR_{ON}	Slew Rate	V_{IN} = 5 V		57		mV/µs
		V_{IN} = 3.6 V		36		
		V_{IN} = 1.8 V		12		
		V_{IN} = 1.2 V		5.1		
		V_{IN} = 1 V		3.3		
t_{OFF}	Turn Off Time	V_{IN} = 5 V		5		µs
		V_{IN} = 3.6 V		5		
		V_{IN} = 1.8 V		10		
		V_{IN} = 1.2 V		15		
		V_{IN} = 1 V		25		
t_{FALL}	Fall Time	C_L = 0.1 µF, R_L = 10 Ω(1)		2.3		µs
		C_L = 1µF, R_L = Open(1)		315		

6.6 Switching Characteristics (continued)

Unless otherwise noted, the typical characteristics in the following table applies over the entire recommended power supply voltage range of 1 V to 5.5 V at 25°C with a load of C_L = 0.1µF, R_L = 10Ω.

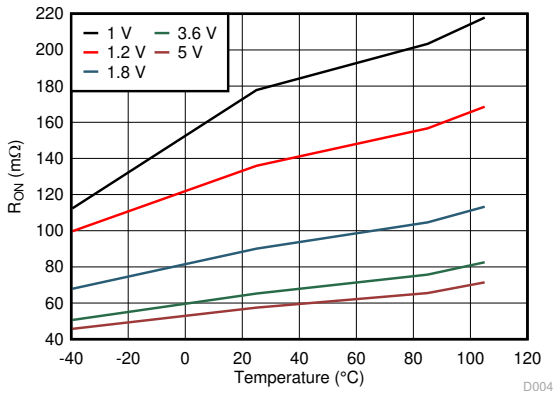
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TPS22916C, TPS22916CN, TPS22916CL, TPS22916CNL						
t_{ON}	Turn On Time	V_{IN} = 5 V		1400		µs
		V_{IN} = 3.6 V		1700		
		V_{IN} = 1.8 V		3000		
		V_{IN} = 1.2 V		5000		
		V_{IN} = 1 V		6500		
t_{RISE}	Rise Time	V_{IN} = 5 V		800		µs
		V_{IN} = 3.6 V		900		
		V_{IN} = 1.8 V		1400		
		V_{IN} = 1.2 V		2300		
		V_{IN} = 1 V		3000		
SR_{ON}	Slew Rate	V_{IN} = 5 V		5		mV/µs
		V_{IN} = 3.6 V		3.2		
		V_{IN} = 1.8 V		1		
		V_{IN} = 1.2 V		0.4		
		V_{IN} = 1 V		0.3		
t_{OFF}	Turn Off Time	V_{IN} = 5 V		5		µs
		V_{IN} = 3.6 V		5		
		V_{IN} = 1.8 V		10		
		V_{IN} = 1.2 V		15		
		V_{IN} = 1 V		25		
t_{FALL}	Fall Time(2)	C_L = 0.1 µF, R_L = 10 Ω(1)		2.3		µs
		CL = 10µF, RL = Open(1)		3150		

(1) See the *Fall Time (t_{FALL}) and Quick Output Discharge (QOD)* section for information on how R_L and C_L affect Fall Time.
(2) Devices without Quick Output Discharge (QOD) may not discharge completely.

6.7 Typical Characteristics

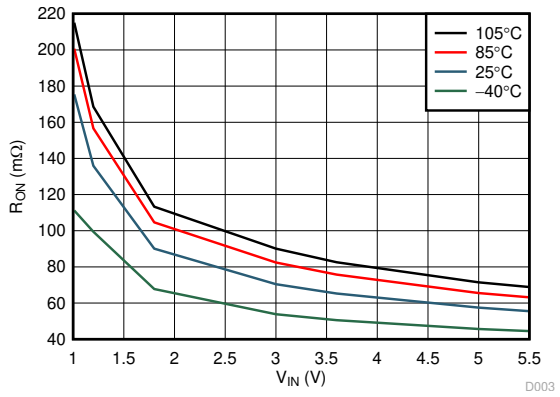
6.7.1 Typical Electrical Characteristics

The typical characteristics curves in this section apply to all devices unless otherwise noted.



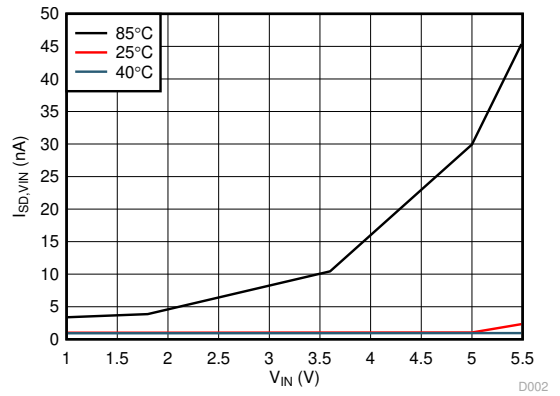
Enabled

図 6-1. ON-Resistance vs Temperature



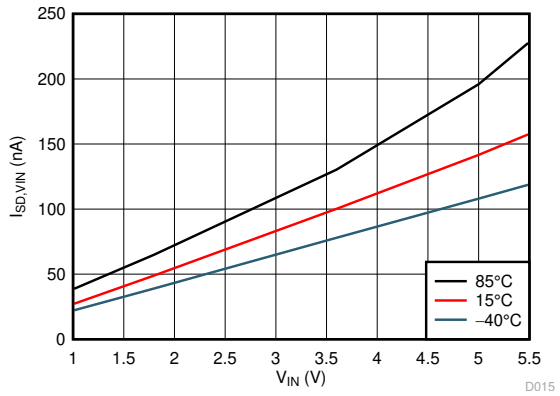
Enabled

図 6-2. ON-Resistance vs Input voltage



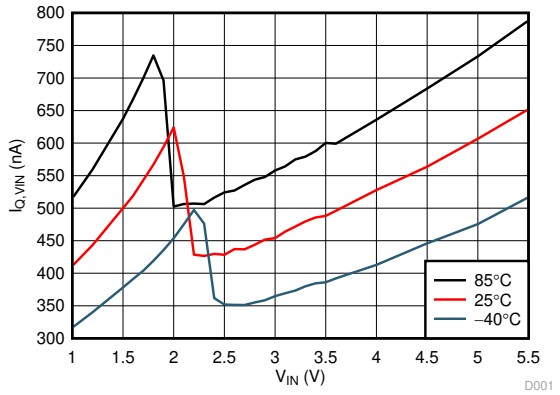
TPS22916C, TPS22916CN, TPS22916B $V_{ON} \le V_{IL}$

図 6-3. Shutdown Current



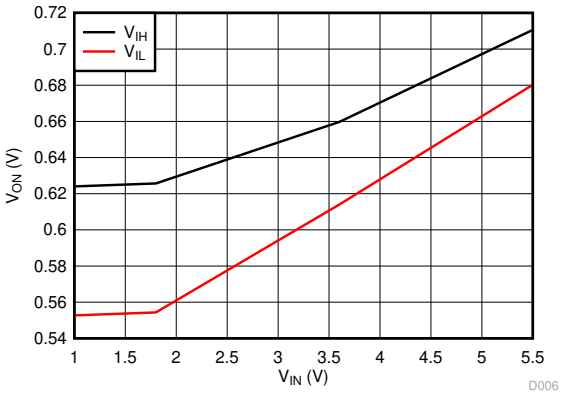
TPS22916CL, TPS22916BL, TPS22916CNL $V_{ON} \ge V_{IH}$

図 6-4. Shutdown Current (Active Low)



Enabled

図 6-5. Quiescent Current

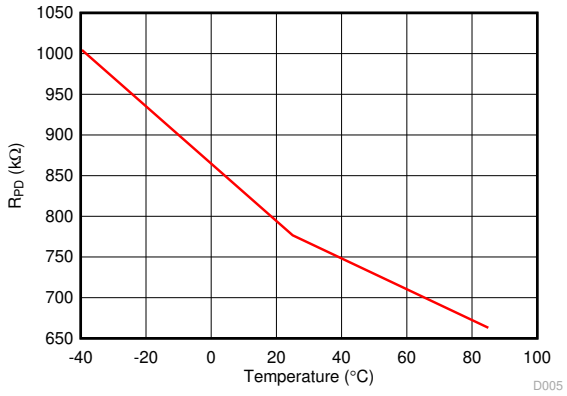


–40°C to +85°C

図 6-6. ON Pin Threshold

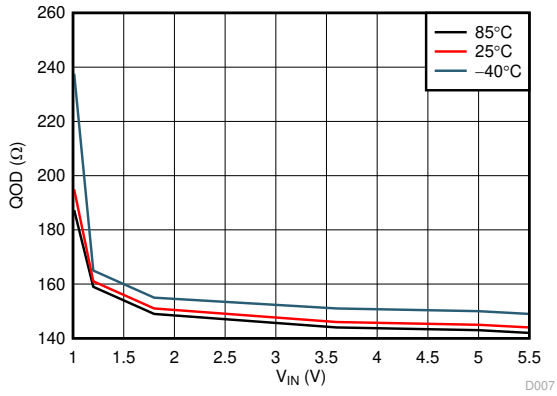
6.7.1 Typical Electrical Characteristics (continued)

The typical characteristics curves in this section apply to all devices unless otherwise noted.



$V_{ON} \leq V_{IL}$

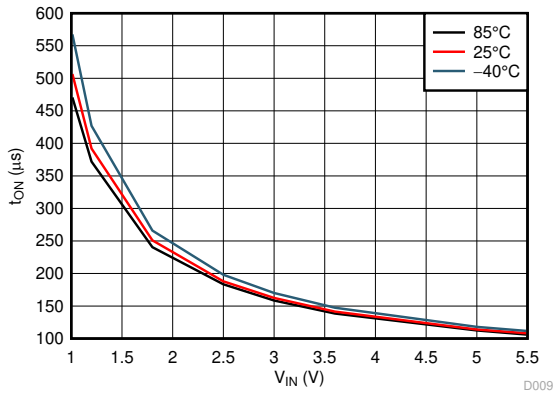
図 6-7. ON Pin Smart Pulldown



TPS22916C, TPS22916CL, TPS22916B, TPS22916BL

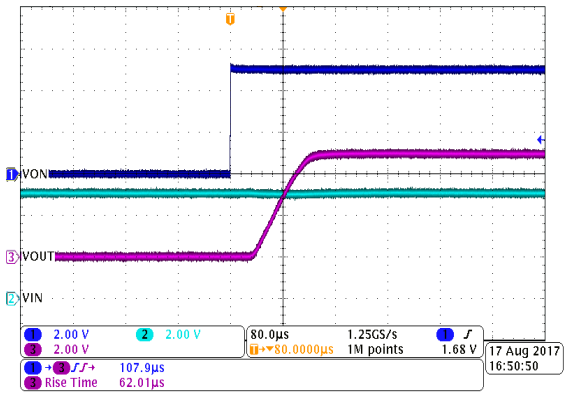
図 6-8. Quick Output Discharge

6.7.2 Typical Switching Characteristics



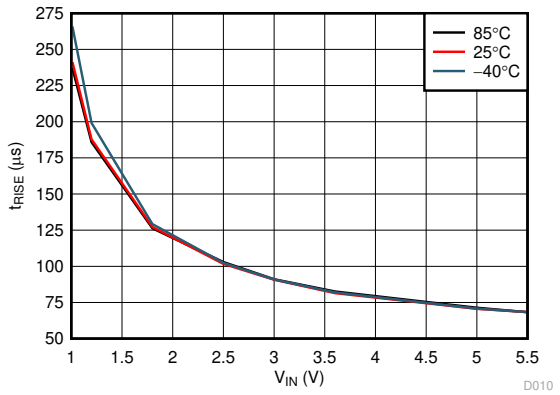
C_L = 0.1 µF R_L = 10 Ω

図 6-9. Fast Turn-On Time



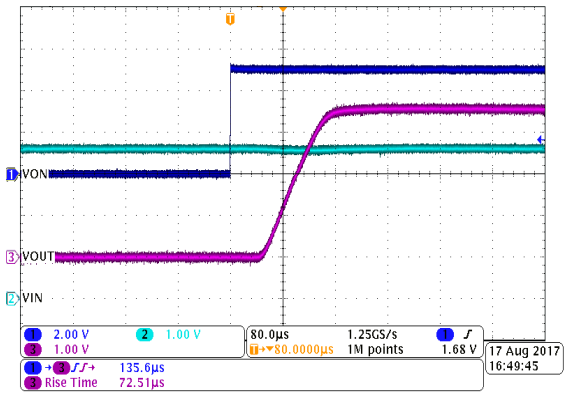
TPS22916B V_{IN} = 5 V C_L = 0.1 µF R_L = 10 Ω

図 6-10. Fast Turn-On at 5 V



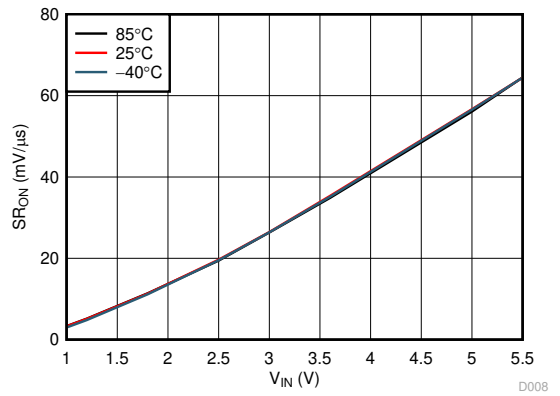
C_L = 0.1 µF R_L = 10 Ω

図 6-11. Fast Rise Time



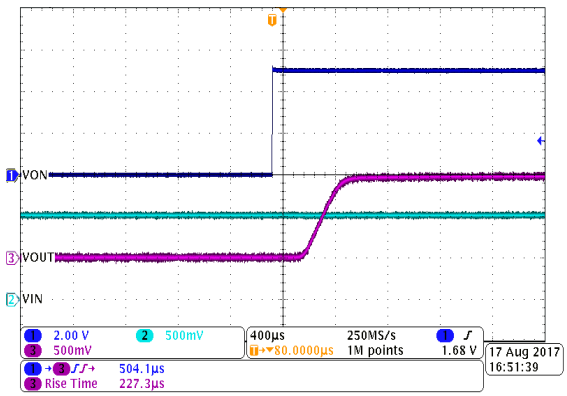
TPS22916B V_{IN} = 3.6 V C_L = 0.1 µF R_L = 10 Ω

図 6-12. Fast Turn-On at 3.6 V



C_L = 0.1 µF R_L = 10 Ω

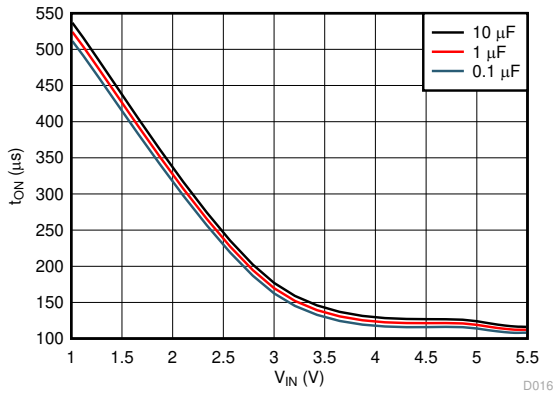
図 6-13. Fast Slew Rate



TPS22916B V_{IN} = 1 V C_L = 0.1 µF R_L = 10 Ω

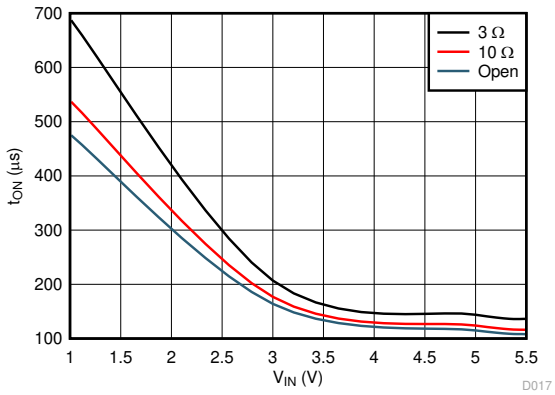
図 6-14. Fast Turn-On at 1 V

6.7.2 Typical Switching Characteristics (continued)



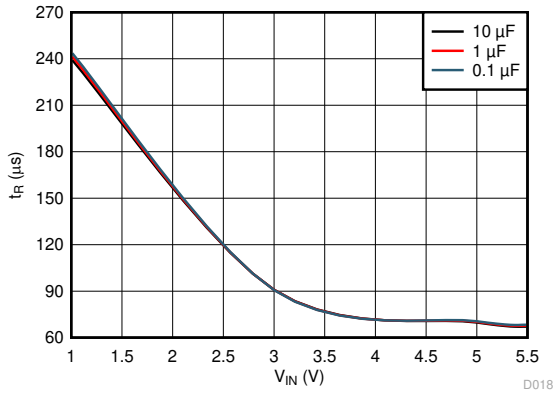
R_L = 10 Ω TPS22916B

図 6-15. Fast Turn-On vs Load Capacitance



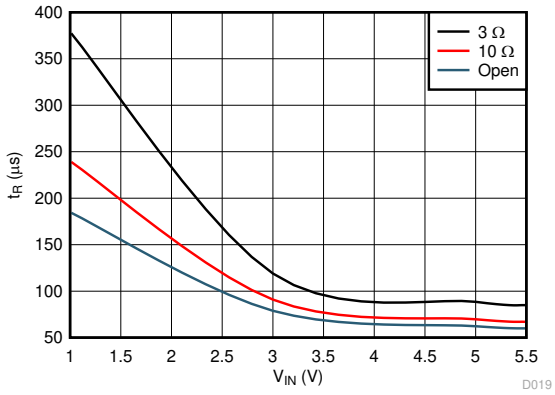
C_L = 10 µF TPS22916B

図 6-16. Fast Turn-On vs Load Resistance



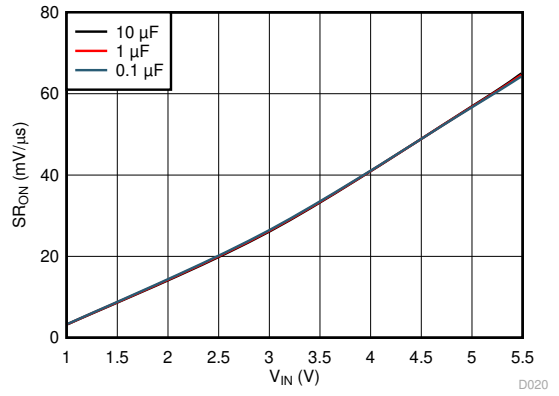
R_L = 10 Ω TPS22916B

図 6-17. Fast Rise Time vs Load Capacitance



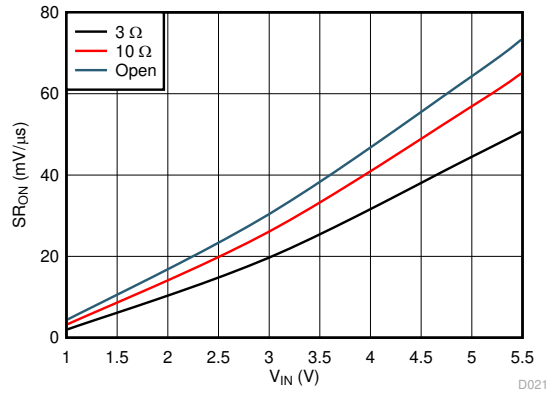
C_L = 10 µF TPS22916B

図 6-18. Fast Rise Time vs Load Capacitance



R_L = 10 Ω TPS22916B

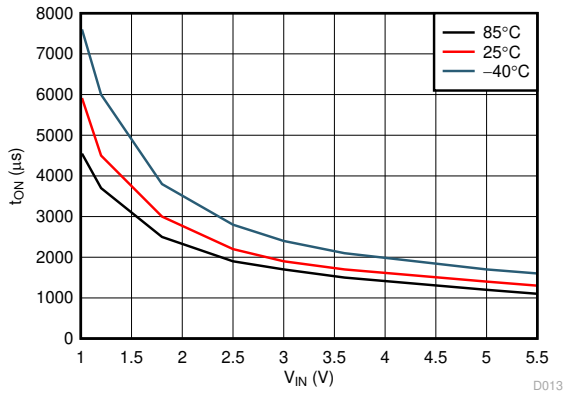
図 6-19. Fast Slew Rate vs Load Capacitance



C_L = 10 µF TPS22916B

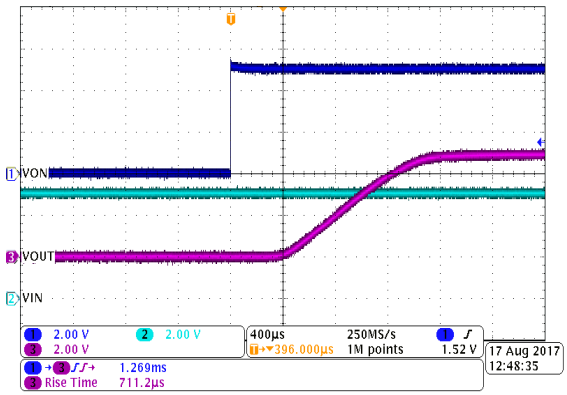
図 6-20. Fast Slew Rate vs Load Resistance

6.7.2 Typical Switching Characteristics (continued)



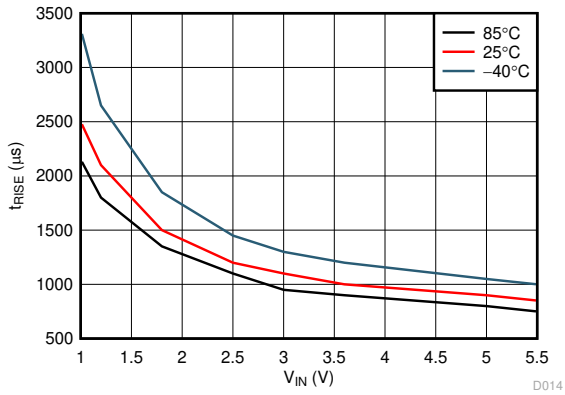
C_L = 0.1 µF R_L = 10 Ω

図 6-21. Slow Turn-On Time



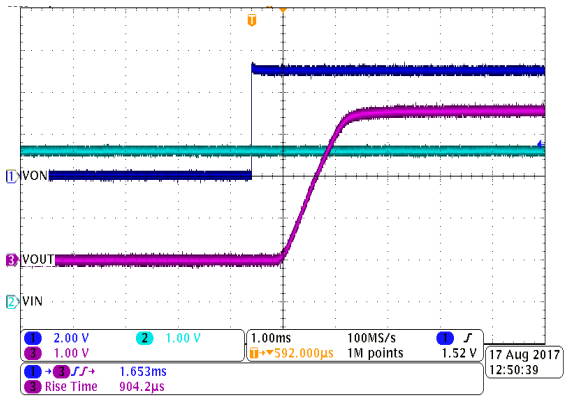
TPS22916C V_{IN} = 5 V C_L = 0.1 µF R_L = 10 Ω

図 6-22. Slow Turn-On at 5 V



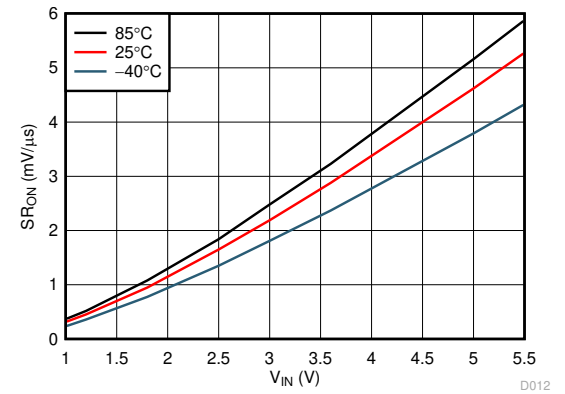
C_L = 0.1 µF R_L = 10 Ω

図 6-23. Slow Rise Time



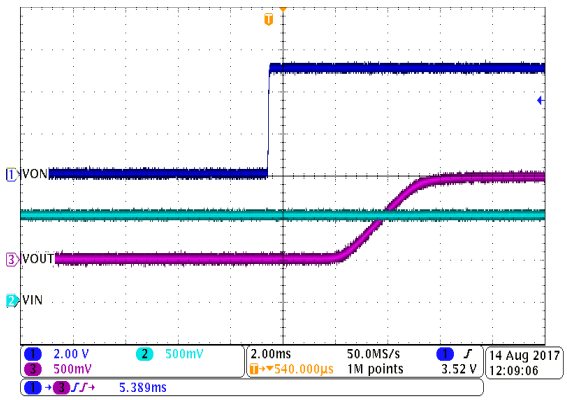
TPS22916C V_{IN} = 3.6 V C_L = 0.1 µF R_L = 10 Ω

図 6-24. Slow Turn-On at 3.6 V



C_L = 0.1 µF R_L = 10 Ω

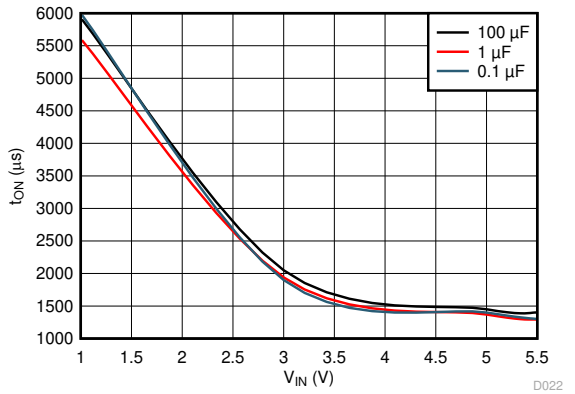
図 6-25. Slow Slew Rate



TPS22916C V_{IN} = 1 V C_L = 0.1 µF R_L = 10 Ω

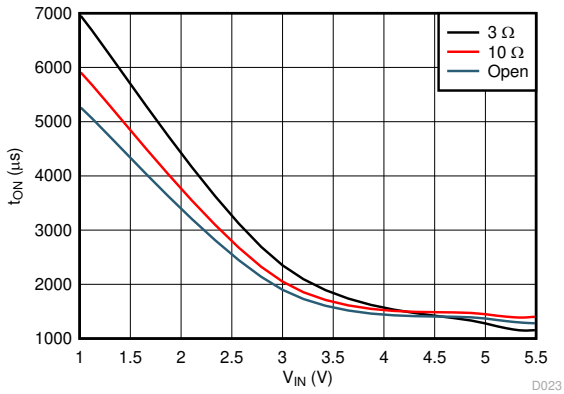
図 6-26. Slow Turn-On at 1 V

6.7.2 Typical Switching Characteristics (continued)



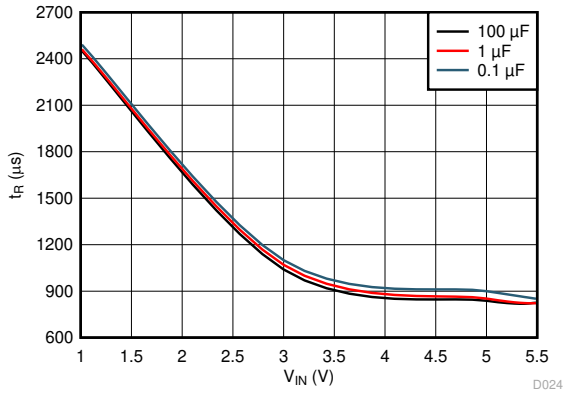
R_L = 10 Ω TPS22916C TPS22916CN TPS22916CL

図 6-27. Slow Turn-On vs Load Capacitance



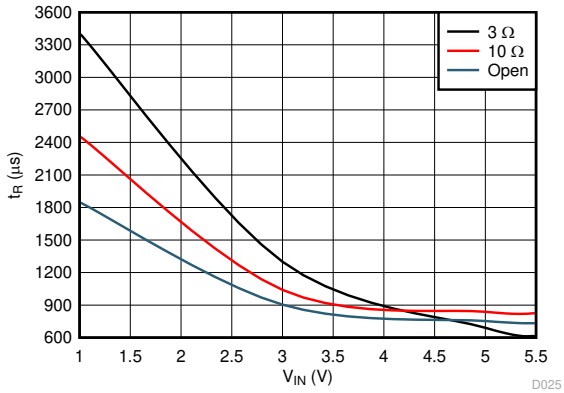
C_L = 100 µF TPS22916C TPS22916CN TPS22916CL

図 6-28. Slow Turn-On vs Load Resistance



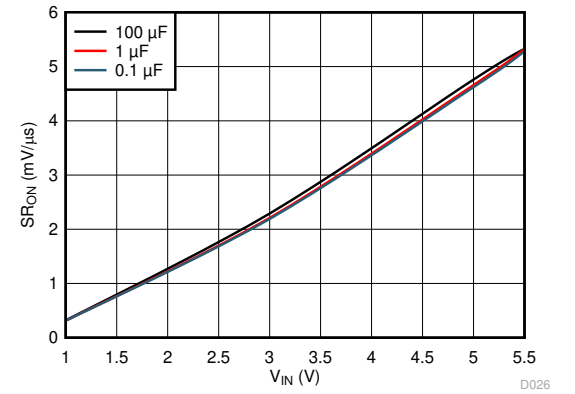
R_L = 10 Ω TPS22916C TPS22916CN TPS22916CL

図 6-29. Slow Rise Time vs Load Capacitance



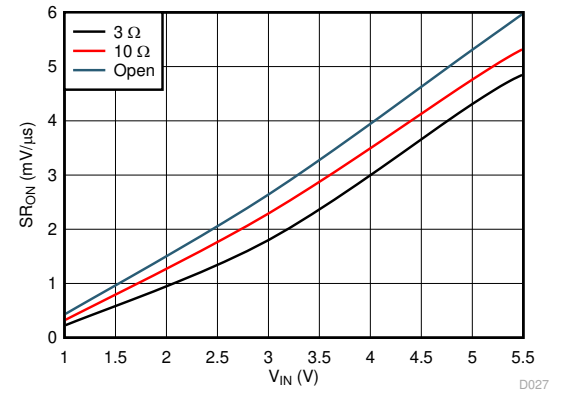
C_L = 100 µF TPS22916C TPS22916CN TPS22916CL

図 6-30. Slow Rise Time vs Load Resistance



R_L = 10 Ω TPS22916C TPS22916CN TPS22916CL

図 6-31. Slow Slew Rate vs Load Capacitance



C_L = 100 µF TPS22916C TPS22916CN TPS22916CL

図 6-32. Slow Slew Rate vs Load Resistance

6.7.2 Typical Switching Characteristics (continued)

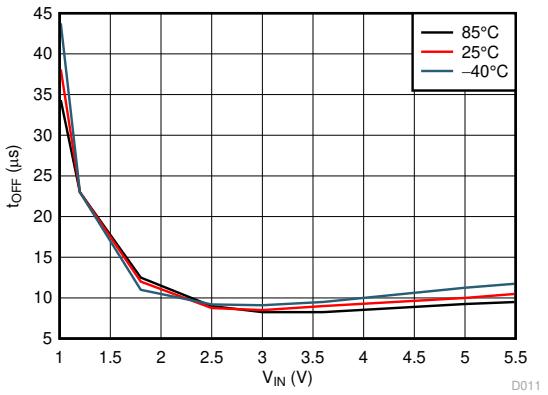
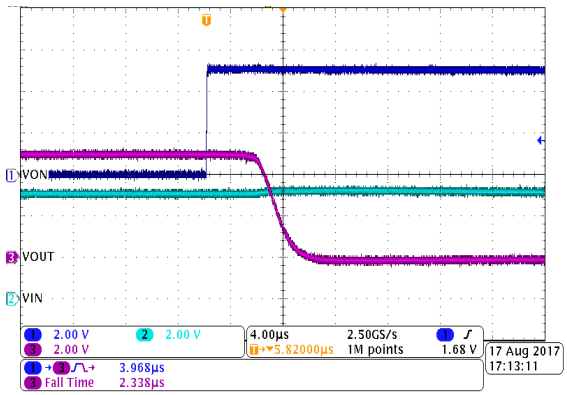
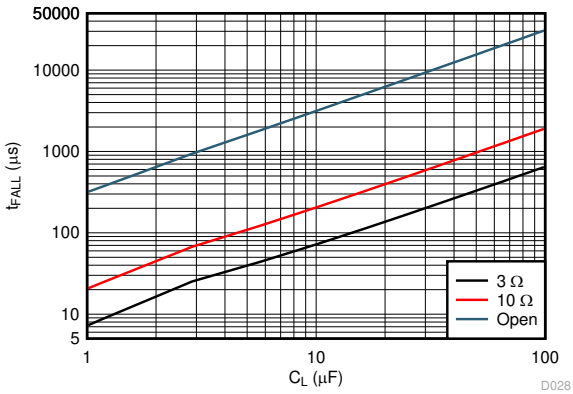


図 6-33. Turn-Off Time



TPS22916CL V_{IN} = 5 V C_L = 0.1 µF R_L = 10 Ω

図 6-34. Turn-Off at 5 V (Active Low)



V_{IN} = 1 V to 5.5 V TPS22916C TPS22916CL TPS22916B

図 6-35. Fall Time

7 Parameter Measurement Information

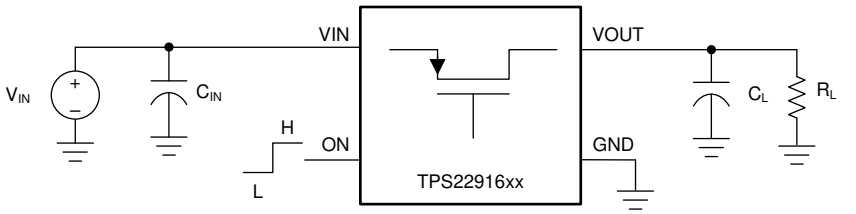


図 7-1. TPS22916 Test Circuit

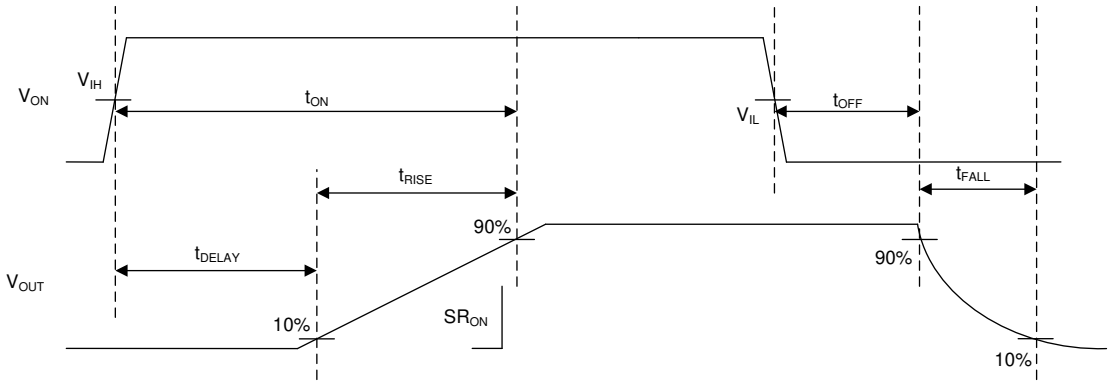


図 7-2. TPS22916 Timing Waveform

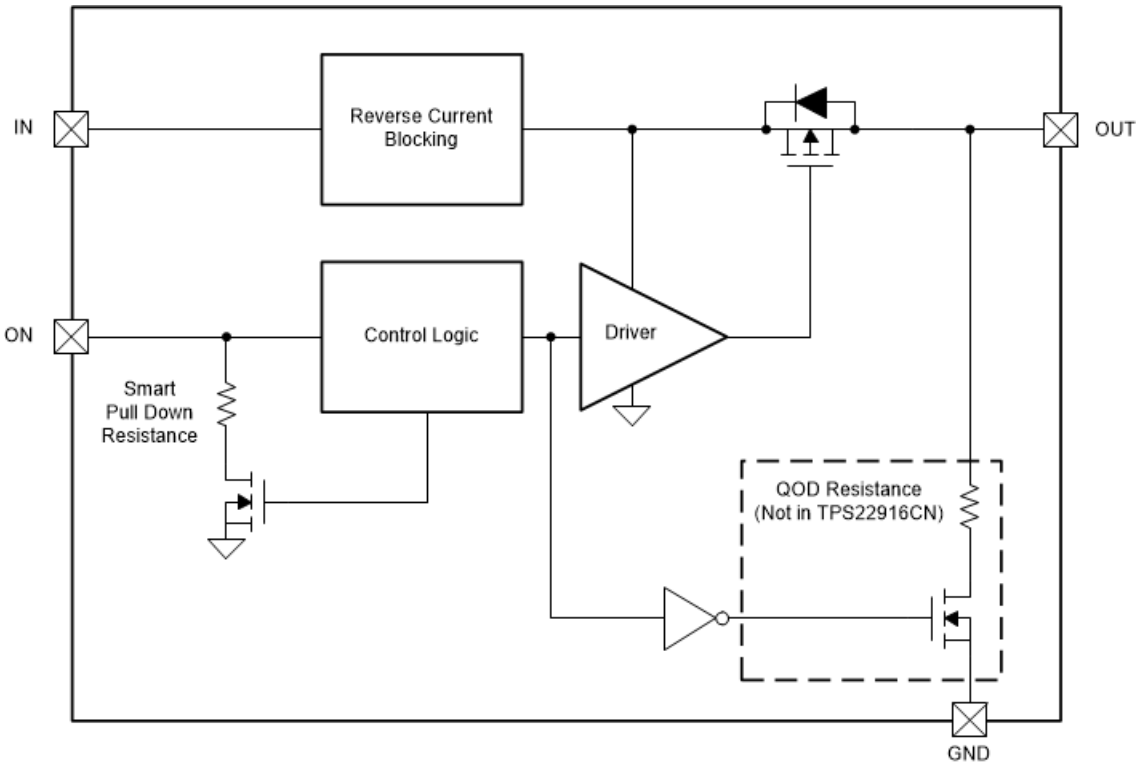
8 Detailed Description

8.1 Overview

This family of devices are single channel, 2-A load switches in ultra-small, space saving 4-pin WCSP package. These devices implement a low resistance P-channel MOSFET with a controlled rise time for applications that must limit inrush current.

These devices are designed to have very low leakage current during OFF state. This design prevents downstream circuits from pulling high standby current from the supply. Integrated control logic, driver, power supply, and output discharge FET eliminates the need for additional external components, which reduces solution size and BOM count.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 On and Off Control

The ON pin controls the state of the switch. The ON pin is compatible with standard GPIO logic threshold. the pin can be used with any microcontroller with 1.2-V, 1.8-V, 2.5-V, 3.3-V, or 5.5-V GPIO.

8.3.2 Fall Time (t_{FALL}) and Quick Output Discharge (QOD)

The TPS22916B, TPS22916BL, TPS22916C, and TPS22916CL include a Quick Output Discharge feature. When the switch is disabled, a discharge resistor is connected between VOUT and GND. This resistor has a typical value of QOD and prevents the output from floating while the switch is disabled.

As load capacitance and load resistance increase: t_{FALL} increases. The larger the load resistance or load capacitance is, the longer it takes to discharge the capacitor, resulting in a longer fall time.

The output fall time is determined by how quickly the load capacitance is discharged and can be found using 式 1 .

$$t_{FALL} = – (R_{DIS}) \times C_L \times \ln (V_{10\%} / V_{90\%}) \quad (1)$$

Where

- $V_{10\%}$ is 10% of the initial output voltage
- $V_{90\%}$ is 90% of the initial output voltage
- R_{DIS} is the result of the QOD resistance in parallel with the Load Resistance R_L
- C_L is the load capacitance

With the Quick Output Discharge feature, the QOD resistance is in parallel with R_L. This provides a lower total load resistance as seen from the load capacitance which discharges the capacitance faster resulting in a smaller t_{FALL}.

8.3.3 Full-Time Reverse Current Blocking

In a scenario where the device is enabled and V_{OUT} is greater than V_{IN} there is potential for reverse current to flow through the pass FET or the body diode. When the reverse current threshold (I_{RCB}) is exceeded, the switch is disabled within t_{RCB}. The switch remains off and block reverse current as long as the reverse voltage condition exists. After V_{OUT} has dropped below the V_{RCB} release threshold the TPS22916xx turns back on with slew rate control.

8.4 Device Functional Modes

表 8-1 describes the state for each variant as determined by the ON pin.

表 8-1. Device Function Table

ON	TPS22916B	TPS22916BL	TPS22916C	TPS22916CN	TPS22916CL	TPS22916CNL
≤ V_{IL}	Disabled	Enabled	Disabled	Disabled	Enabled	Enabled
≥ V_{IH}	Enabled	Disabled	Enabled	Enabled	Disabled	Disabled

表 8-2 shows when QOD is active for each variant.

表 8-2. QOD Function Table

Device	TPS22916B	TPS22916BL	TPS22916C	TPS22916CN	TPS22916CL	TPS22916CNL
Enabled	No	No	No	No	No	No
Disabled	Yes	Yes	Yes	No	Yes	No

表 8-3 shows when the ON pin smart pulldown is active.

表 8-3. Smart-ON Pulldown

V_{ON}	Pulldown
≤ V_{IL}	Connected
≥ V_{IH}	Disconnected

9 Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

This section highlights some of the design considerations when implementing this device in various applications. A PSPICE model for this device is also available in the product page of this device.

9.2 Typical Application

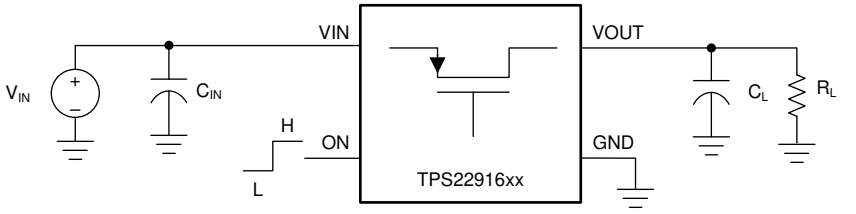


図 9-1. Typical Application

9.2.1 Design Requirements

For this design example, below, use the input parameters shown in 表 9-1.

表 9-1. Design Parameters

Design Parameter	Example Value
Input voltage (V_{IN})	3.6 V
Load capacitance (C_L)	47 µF
Maximum inrush current (I_{RUSH})	300 mA

9.2.2 Detailed Design Procedure

9.2.2.1 Maximum Inrush Current

When the switch is enabled, the output capacitors must be charged up from 0 V to VIN voltage. This charge arrives in the form of inrush current. Inrush current can be calculated using the following equation:

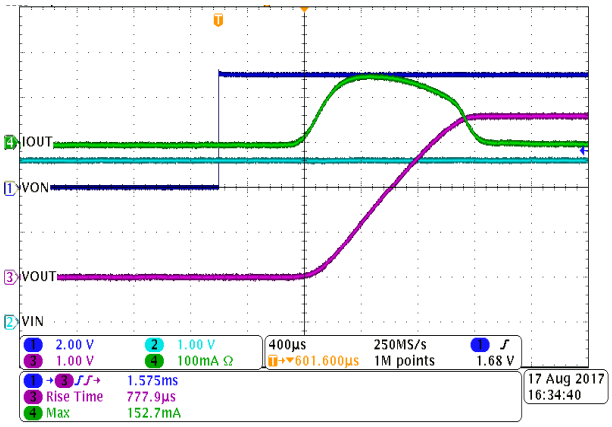
$$I_{RUSH} = C_L \times SR_{ON} \quad (2)$$

$$I_{RUSH} = 47\ \mu F \times 3.2\ mV/\mu s \quad (3)$$

$$I_{RUSH} = 150\ mA \quad (4)$$

The TPS22916x offers multiple rise time options to control the inrush current during turn-on. The appropriate device can be selected based upon the maximum acceptable slew rate which can be calculated using the design requirements and the inrush current equation. In this case, the TPS22916C provides a slew rate slow enough to limit the inrush current to the desired amount.

9.2.3 Application Curve



V_{IN} = 3.6 V C_L = 47 µF R_L = Open
TPS22916C T_A = 25°C

図 9-2. Inrush Current

10 Power Supply Recommendations

The device is designed to operate with a VIN range of 1 V to 5.5 V. The VIN power supply must be well regulated and placed as close to the device terminal as possible. The power supply must be able to withstand all transient load current steps. In most situations, using an input capacitance (C_{IN}) of 1 µF is sufficient to prevent the supply voltage from dipping when the switch is turned on. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance can be required on the input.

11 Layout

11.1 Layout Guidelines

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances can have on normal operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects.

11.2 Layout Example

式 3 shows an example for these devices. Notice the connection to system ground between the V_{OUT} Bypass Capacitor ground and the GND pin of the load switch,. This connection creates a ground barrier which helps to reduce the ground noise seen by the device.

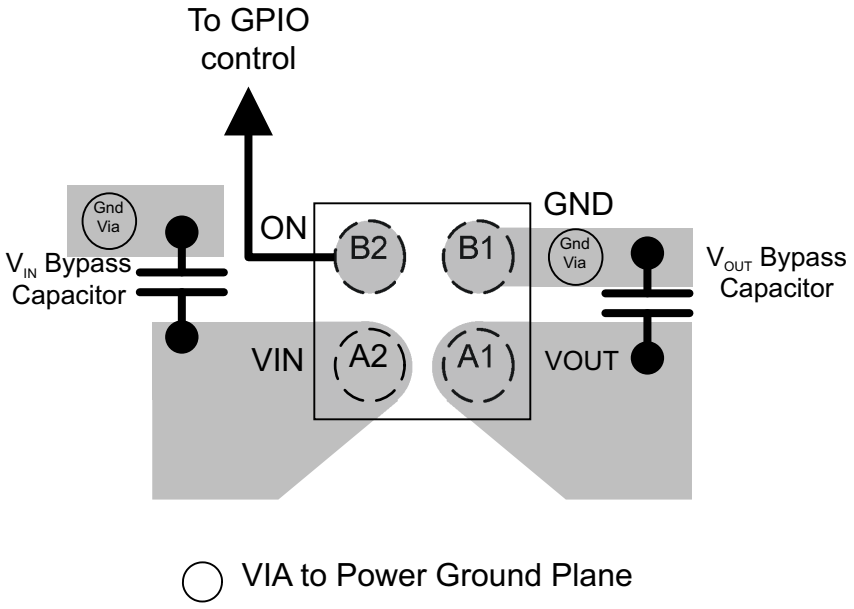


図 11-1. TPS22916xx Layout

11.3 Thermal Considerations

The maximum IC junction temperature must be restricted to 125°C under normal operating conditions. To calculate the maximum allowable dissipation, $P_{D(max)}$ for a given output current and ambient temperature, use 式 5 as a guideline:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{R_{\theta JA}} \quad (5)$$

Where,

$P_{D(max)}$ = maximum allowable power dissipation

$T_{J(max)}$ = maximum allowable junction temperature

T_A = ambient temperature for the device

θ_{JA} = junction to air thermal impedance. See the *Thermal Information* section.

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

Texas Instruments, *TPS22916 Load Switch Evaluation Module* User's Guide

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

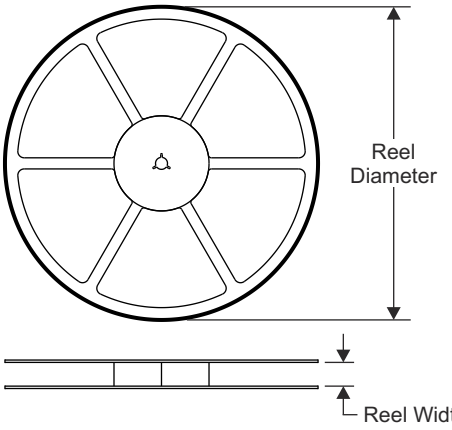
TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

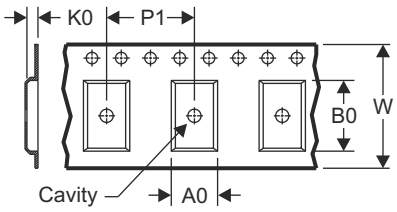
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

13.1 Tape and Reel Information

REEL DIMENSIONS

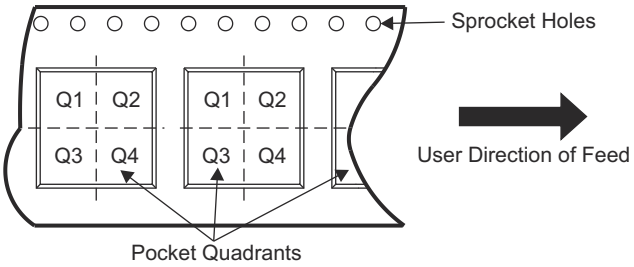


TAPE DIMENSIONS



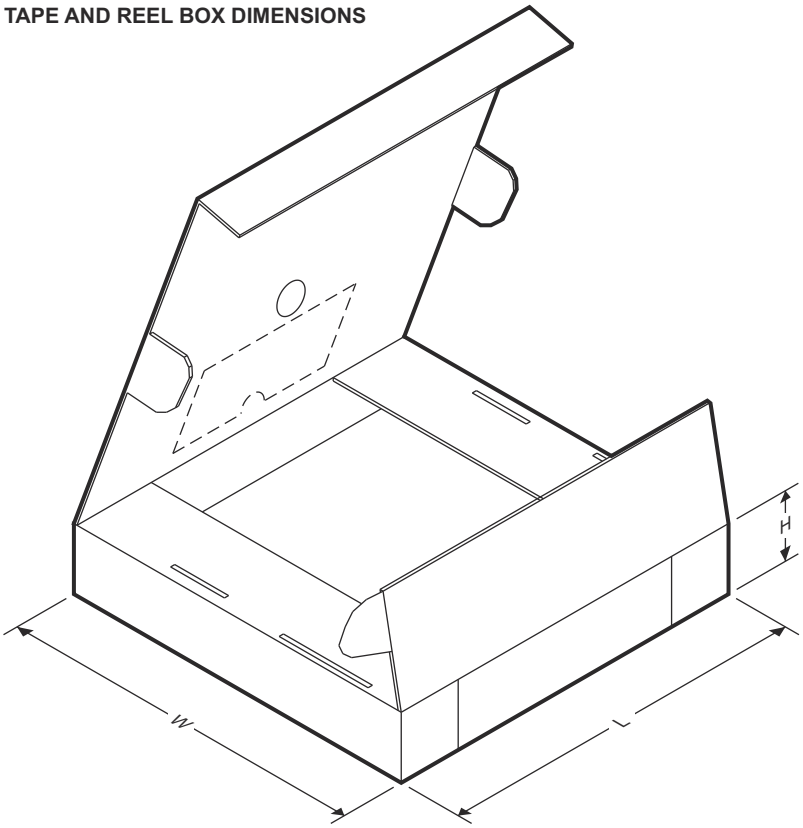
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22916BYFPR	DSBGA	YFP	4	3000	180.0	8.4	0.86	0.86	0.59	4.0	8.0	Q1
TPS22916BYFPT	DSBGA	YFP	4	250	180.0	8.4	0.86	0.86	0.59	4.0	8.0	Q1
TPS22916CLYFPR	DSBGA	YFP	4	3000	180.0	8.4	0.86	0.86	0.59	4.0	8.0	Q1
TPS22916CLYFPT	DSBGA	YFP	4	250	180.0	8.4	0.86	0.86	0.59	4.0	8.0	Q1
TPS22916CNYFPR	DSBGA	YFP	4	3000	180.0	8.4	0.86	0.86	0.59	4.0	8.0	Q1
TPS22916CNYFPT	DSBGA	YFP	4	250	180.0	8.4	0.86	0.86	0.59	4.0	8.0	Q1
TPS22916CYFPR	DSBGA	YFP	4	3000	180.0	8.4	0.86	0.86	0.59	4.0	8.0	Q1
TPS22916CYFPT	DSBGA	YFP	4	250	180.0	8.4	0.86	0.86	0.59	4.0	8.0	Q1
TPS22916CNLYFPR	DSBGA	YFP	4	3000	180.0	8.4	0.86	0.86	0.59	4.0	8.0	Q1
TPS22916BLYFPR	DSBGA	YFP	4	3000	180.0	8.4	0.86	0.86	0.59	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



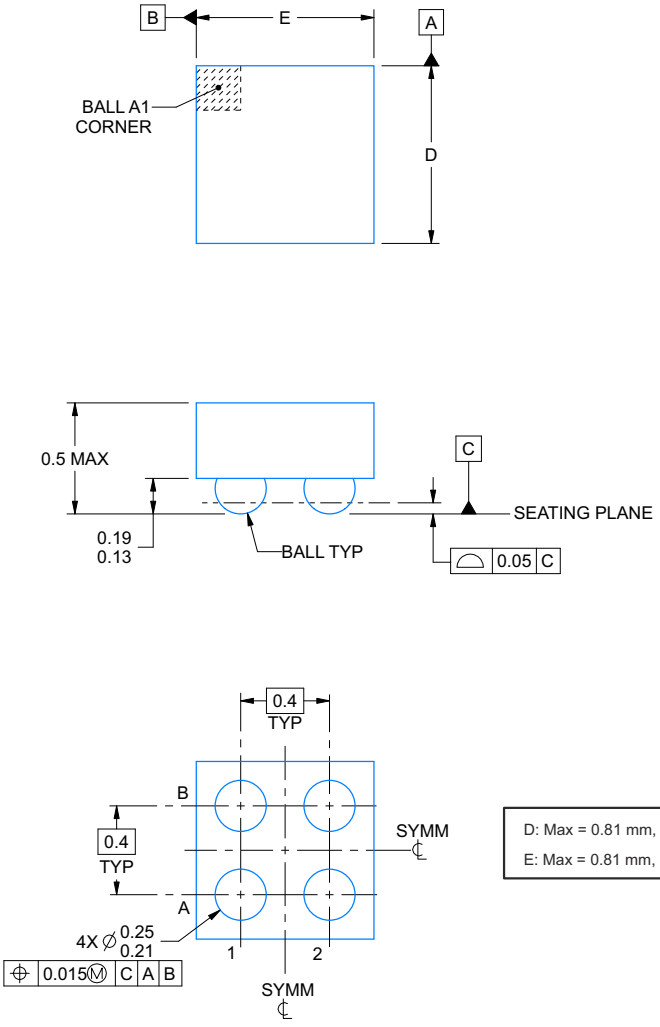
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22916BYFPR	DSBGA	YFP	4	3000	182.0	182.0	20.0
TPS22916BYFPT	DSBGA	YFP	4	250	182.0	182.0	20.0
TPS22916CLYFPR	DSBGA	YFP	4	3000	182.0	182.0	20.0
TPS22916CLYFPT	DSBGA	YFP	4	250	182.0	182.0	20.0
TPS22916CNYFPR	DSBGA	YFP	4	3000	182.0	182.0	20.0
TPS22916CNYFPT	DSBGA	YFP	4	250	182.0	182.0	20.0
TPS22916CYFPR	DSBGA	YFP	4	3000	182.0	182.0	20.0
TPS22916CYFPT	DSBGA	YFP	4	250	182.0	182.0	20.0
TPS22916CNLYFPR	DSBGA	YFP	4	3000	182.0	182.0	20.0
TPS22916BLYFPR	DSBGA	YFP	4	3000	182.0	182.0	20.0

PACKAGE OUTLINE

YFP0004

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

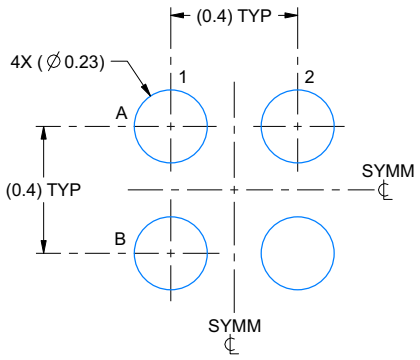
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

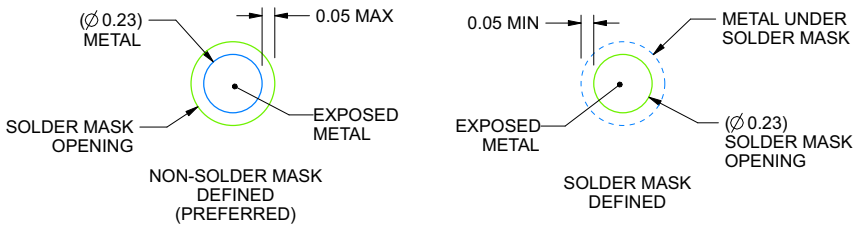
YFP0004

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:50X



SOLDER MASK DETAILS
NOT TO SCALE

4223507/A 01/2017

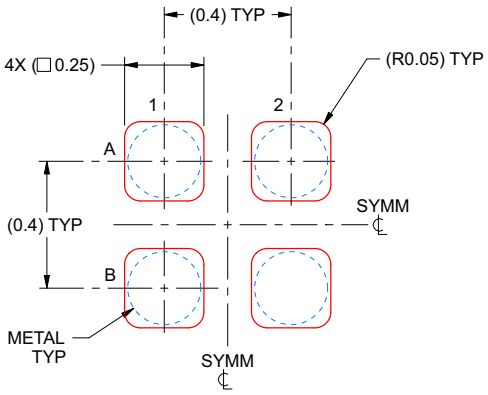
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YFP0004 — **DSBGA - 0.5 mm max height**

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

4223507/A 01/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS22916BLYFPR	Active	Production	DSBGA (YFP) | 4	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	Q
TPS22916BLYFPR.A	Active	Production	DSBGA (YFP) | 4	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	Q
TPS22916BYFPR	Active	Production	DSBGA (YFP) | 4	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(BA, R)
TPS22916BYFPR.A	Active	Production	DSBGA (YFP) | 4	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(BA, R)
TPS22916BYFPT	Active	Production	DSBGA (YFP) | 4	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(BA, R)
TPS22916BYFPT.A	Active	Production	DSBGA (YFP) | 4	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(BA, R)
TPS22916CLYFPR	Active	Production	DSBGA (YFP) | 4	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	B9
TPS22916CLYFPR.A	Active	Production	DSBGA (YFP) | 4	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	B9
TPS22916CLYFPT	Active	Production	DSBGA (YFP) | 4	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	B9
TPS22916CLYFPT.A	Active	Production	DSBGA (YFP) | 4	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	B9
TPS22916CNLYFPR	Active	Production	DSBGA (YFP) | 4	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	S
TPS22916CNLYFPR.A	Active	Production	DSBGA (YFP) | 4	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	S
TPS22916CNYFPR	Active	Production	DSBGA (YFP) | 4	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	B8
TPS22916CNYFPR.A	Active	Production	DSBGA (YFP) | 4	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	B8
TPS22916CNYFPT	Active	Production	DSBGA (YFP) | 4	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	B8
TPS22916CNYFPT.A	Active	Production	DSBGA (YFP) | 4	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	B8
TPS22916CYFPR	Active	Production	DSBGA (YFP) | 4	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	B7
TPS22916CYFPR.A	Active	Production	DSBGA (YFP) | 4	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	B7
TPS22916CYFPT	Active	Production	DSBGA (YFP) | 4	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	B7
TPS22916CYFPT.A	Active	Production	DSBGA (YFP) | 4	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	B7

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件 、 TI の総合的な品質ガイドライン 、 ti.com または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。 TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

最終更新日：2025 年 10 月