TPS2117 マニュアル / 優先切り替え機能搭載、1.6V～5.5V、4A、低静止電流 (IQ) パワー・マルチプレクサ

1 特長

- 入力電圧範囲:1.6V～5.5V
- 最大連続電流:4A
- オン抵抗:20mΩ (標準値)
- VIN2 のスタンバイ電流:50nA (標準値)
- 静止電流:1.32µA (標準値)
- 切り換えモード:
  - 優先モード
  - マニュアル・モード
  - ダイオード・モード
- 制御された出力スルーレート:
  - 1.3ms (標準値、3.3V 時)
- VOUT > VINx のときの逆電流ブロック
- サーマル・シャットダウン

2 アプリケーション

- バックアップ・バッテリ・システム
- e メーター
- モーター駆動
- ビル・オートメーション

3 概要

TPS2117 は、1.6V～5.5V の電圧定格と 4A の最大電流定格を持つパワー・マルチプレクサ・デバイスです。本デバイスは、N チャネル MOSFET を使用して電源を切り換えると同時に、電圧が最初に印加された際にもスルーレートを制御します。

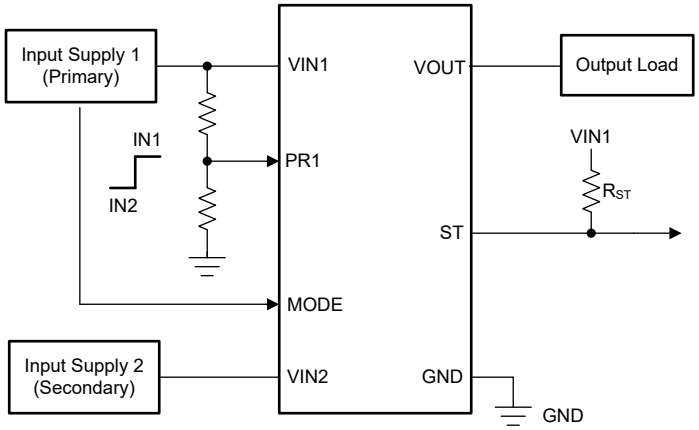
TPS2117 の小さい静止電流 (1.32µA、標準値) とスタンバイ電流 (50nA、標準値) は、バッテリがいずれかの入力に接続されているシステムに理想的です。これらの小さい電流は、使用時のバッテリ寿命を延ばします。

TPS2117 は、アプリケーションに応じて 2 通りの切り換え挙動を行うように構成できます。自動優先モードでは、VIN1 に接続された電源が優先され、VIN1 が低下すると第 2 の電源 (VIN2) に切り替わります。マニュアル・モードを使うと、GPIO をトグルするか信号をイネーブルして、チャネルを切り換えることができます。

パッケージ情報

部品番号	パッケージ (1)	パッケージ・サイズ (2)
TPS2117	DRL (SOT、8)	2.10mm × 1.60mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ・サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



基本的なアプリケーション

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (March 2023) to Revision A (August 2023)	Page
• ステータスを「事前情報」から「量産データ」に変更	1

5 Pin Configuration and Functions

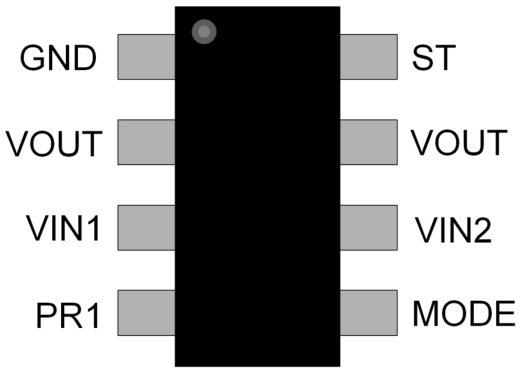


図 5-1. DRL Package, 8-Pin SOT (Top View)

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	1	—	Device ground.
VOUT	2, 7	O	Output power.
VIN1	3	I	Channel 1 input power.
PR1	4	I	Selects between VIN1 and VIN2. When PR1 is high VIN1 is selected, and when PR1 is low VIN2 is selected.
MODE	5	I	Device is put into Priority mode when MODE is tied to VIN1 and manual mode when MODE is pulled up to an external voltage.
VIN2	6	I	Channel 2 input power.
ST	8	O	Open drain status pin. Pulled low when VIN1 is not being used.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN1}, V_{IN2}	Input voltage	–0.3	6	V
V_{OUT}	Output voltage	–0.3	6	V
V_{ST}, V_{PR1}, V_{MODE}	Control pin voltage	–0.3	6	V
C_{MAX}	Maximum output capacitance, V_{INX} = 5.5V		1.5	mF
	Maximum output capacitance, V_{INX} = 6V		220	µF
I_{MAX}	Maximum current		4	A
$I_{MAX,PLS}$	Maximum pulsed current Max duration 1ms, Duty cycle of 2%		6.4	A
T_J	Junction temperature		Internally Limited	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN1}, V_{IN2}	Input voltage	1.6		5.5	V
V_{OUT}	Output voltage	0		5.5	V
V_{ST}, V_{MODE}, V_{PR1}	Control pin voltage	0		5.5	V
T_A	Ambient temperature	–40		105	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS2117 DRL (SOT) 8-PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	111.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	36.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	18.1	°C/W

6.4 Thermal Information (continued)

THERMAL METRIC[1]		TPS2117 DRL (SOT) 8-PINS	UNIT
Ψ_{JT}	Junction-to-top characterization parameter	1.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	17.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

over operating free-air temperature range and operating voltage range of 1.6 V to 5.5 V (unless otherwise noted). Typical specifications are at an input voltage of 3.3 V and ambient temperature of 25°C.

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
POWER CONSUMPTION							
$I_{STBY, VIN1}$	VIN1 standby current	VIN2 powers VOUT VIN1 > VIN2 + 0.1 V	25°C		1.1		µA
			–40°C to 85°C			1.9	
			–40°C to 105°C			2	
		VIN2 powers VOUT VIN2 > VIN1 + 0.2 V	25°C		0.22		
			–40°C to 85°C			0.31	
			–40°C to 105°C			0.32	
$I_{STBY, VIN2}$	VIN2 standby current	VIN1 powers VOUT VIN2 > VIN1 + 0.2 V	25°C		1.2		µA
			–40°C to 85°C			2	
			–40°C to 105°C			2.1	
		VIN1 powers VOUT VIN1 > VIN2 + 0.1 V	25°C		0.05		
			–40°C to 85°C			0.06	
			–40°C to 105°C			0.08	
$I_{Q, VIN1}$	VIN1 quiescent current	VIN1 powers VOUT VIN1 > VIN2 + 0.1 V	25°C		1.32		µA
			–40°C to 85°C			3.6	
			–40°C to 105°C			4.4	
		VIN1 powers VOUT VIN2 > VIN1 + 0.2 V	25°C		0.3		
			–40°C to 85°C			0.46	
			–40°C to 105°C			0.50	
$I_{Q, VIN2}$	VIN2 quiescent current	VIN2 powers VOUT VIN2 > VIN1 + 0.2 V	25°C		1.35		µA
			–40°C to 85°C			3.7	
			–40°C to 105°C			4.5	
		VIN2 powers VOUT VIN1 > VIN2 + 0.1 V	25°C		0.1		
			–40°C to 85°C			0.22	
			–40°C to 105°C			0.27	
$I_{SD,VIN1}$	VIN1 shutdown current	MODE = 0 V, PR1 = 5 V VIN1 > VIN2 VOUT = 0 V	25°C		0.1		µA
			–40°C to 85°C			1.9	
			–40°C to 105°C			5.3	
		MODE = 0 V, PR1 = 5 V VIN1 < VIN2 VOUT = 0 V	25°C		0.05		
			–40°C to 85°C			1.6	
			–40°C to 105°C			4.5	

6.5 Electrical Characteristics (continued)

over operating free-air temperature range and operating voltage range of 1.6 V to 5.5 V (unless otherwise noted). Typical specifications are at an input voltage of 3.3 V and ambient temperature of 25°C.

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
$I_{SD,VIN2}$	VIN2 shutdown current	MODE = 0 V, PR1 = 5 V VIN2 > VIN1 VOUT = 0 V	25°C		0.05		µA
			–40°C to 85°C			1.8	
			–40°C to 105°C			4.5	
		MODE = 0 V, PR1 = 5 V VIN2 < VIN1 VOUT = 0 V	25°C		0.05		
			–40°C to 85°C			1.4	
			–40°C to 105°C			3.8	
I_{REV}	Reverse leakage current out of VINx	V_{OUT} = 5.5 V V_{INx} = 0 V, V_{INy} = open	25°C		0.04		µA
			85°C		0.2		
			105°C		0.5		
	Reverse leakage current into VOUT	V_{OUT} = 5.5 V V_{INx} = 0 V, V_{INy} = open	25°C		0.1		
			85°C		0.3		
			105°C		1		
I_{PR1}	PR1 pin leakage		–40°C to 105°C			0.05	µA
I_{MODE}	MODE pin leakage		–40°C to 105°C			0.05	µA
I_{ST}	ST pin leakage		–40°C to 105°C			0.03	µA
PERFORMANCE							
R_{ON}	On-resistance	VINx = 5 V I_{OUT} = 200 mA	25°C		18.5	25	mΩ
			–40°C to 85°C			31	
			–40°C to 105°C			33	
		VINx = 3.3 V I_{OUT} = 200 mA	25°C		20	26	
			–40°C to 85°C			31	
			–40°C to 105°C			33	
		VINx = 1.8 V I_{OUT} = 200 mA	25°C		20.5	27	
			–40°C to 85°C			34	
			–40°C to 105°C			38	
		VINx = 1.6 V I_{OUT} = 200 mA	25°C		21	28	
			–40°C to 85°C			37	
			–40°C to 105°C			40	
$V_{OL,ST}$	Status pin V_{OL}	I_{ST} = 1 mA	–40°C to 105°C			0.1	V
t_{ST}	Status pin response time	ST pin pulled high to low R_{ST} = 10 kΩ	–40°C to 105°C		5		µs
V_{REF}	PR1 reference voltage		–40°C to 105°C	0.92	1	1.08	V
$V_{IH,MODE}$	MODE logic high level		–40°C to 105°C	1		5.5	V
$V_{IL,MODE}$	MODE logic low level		–40°C to 105°C	0		0.35	V
PROTECTION							
V_{HYST}	VIN1/VIN2 comparator hysteresis	Diode Mode	–40°C to 105°C		60		mV
t_{RCB}	Reverse current blocking response time	VOUT > selected VIN + 1 V	–40°C to 105°C		2		µs
$V_{RCB,R}$	Reverse current blocking rising threshold (V_{OUT} – V_{IN})		–40°C to 105°C		42	70	mV
$V_{RCB,F}$	Reverse current blocking falling threshold (V_{OUT} – V_{IN})		–40°C to 105°C		17	40	mV

6.5 Electrical Characteristics (continued)

over operating free-air temperature range and operating voltage range of 1.6 V to 5.5 V (unless otherwise noted). Typical specifications are at an input voltage of 3.3 V and ambient temperature of 25°C.

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
I_{RCB}	Reverse current blocking activation current		–40°C to 105°C		1.4	4	A
TSD	Thermal shutdown	VIN1 = VIN2			170		°C
TSD_{HYS}	Thermal shutdown hysteresis	VIN1 = VIN2			20		°C

6.6 Switching Characteristics

Typical switching characteristics are defined at an ambient temperature of 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SWITCHOVER						
t_{SW}	Switchover time, VINx = 5 V	R_L = 10 Ω, C_L = 10 µF		16		µs
t_{SW}	Switchover time, VINx = 3.3 V	R_L = 10 Ω, C_L = 10 µF		15		µs
t_{SW}	Switchover time, VINx = 1.8 V	R_L = 10 Ω, C_L = 10 µF		12		µs
t_D	Delay time, VINx = 5 V	R_L = 100 Ω, C_L = 10 µF		1		ms
t_D	Delay time, VINx = 3.3 V	R_L = 100 Ω, C_L = 10 µF		1.2		ms
t_D	Delay time, VINx = 1.8 V	R_L = 100 Ω, C_L = 10 µF		1.4		ms
t_{SS}	Soft-start time, VINx = 5 V	R_L = 100 Ω, C_L = 10 µF		1.7		ms
t_{SS}	Soft-start time, VINx = 3.3 V	R_L = 100 Ω, C_L = 10 µF		1.3		ms
t_{SS}	Soft-start time, VINx = 1.8 V	R_L = 100 Ω, C_L = 10 µF		0.9		ms

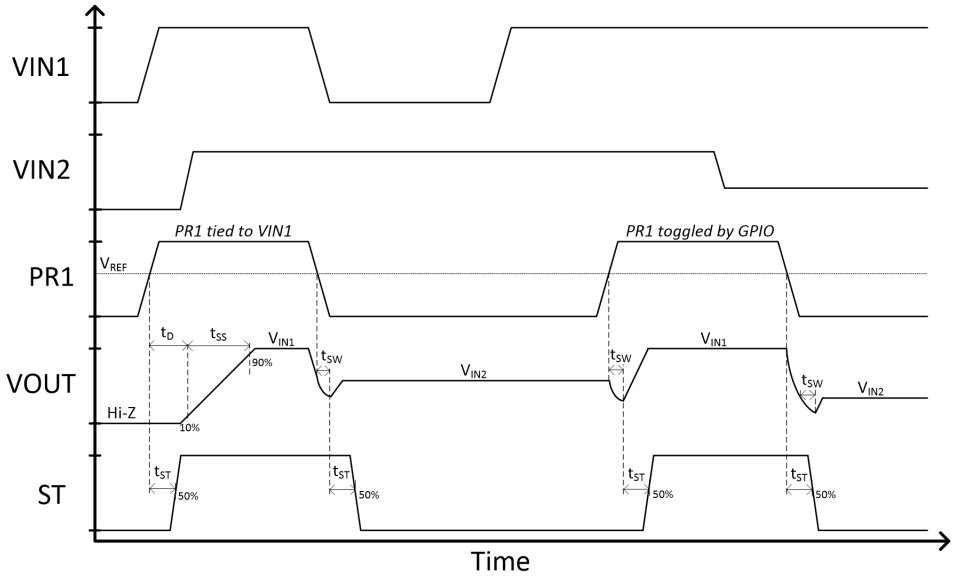
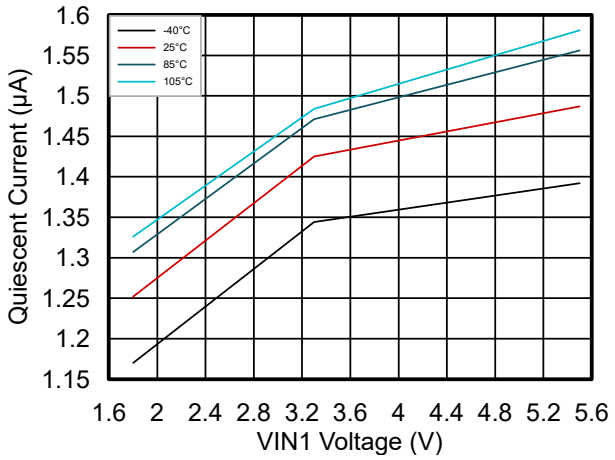


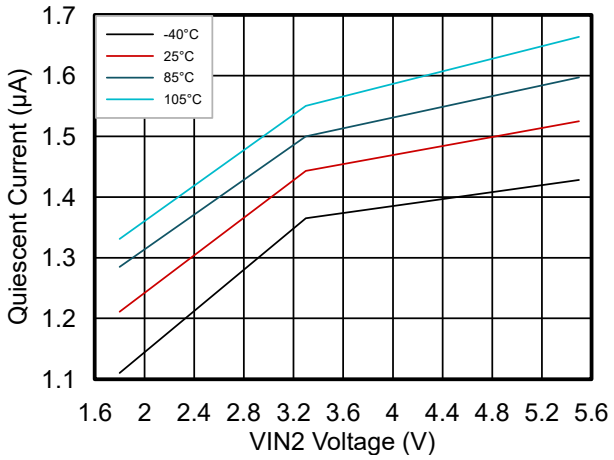
図 6-1. TPS2117 Timing Diagram

6.8 Typical Characteristics



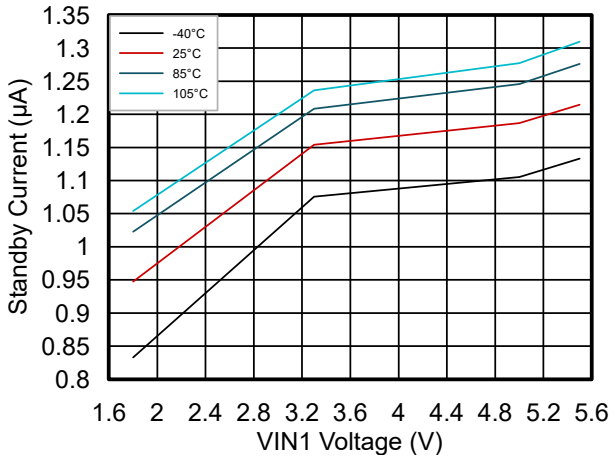
VIN2 = 1.6 V VOUT = Open

図 6-2. VIN1 Quiescent Current vs Input Voltage



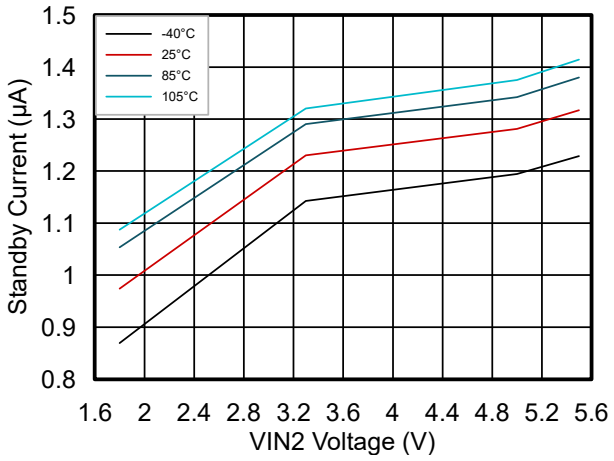
VIN1 = 1.6 V VOUT = Open

図 6-3. VIN2 Quiescent Current vs Input Voltage



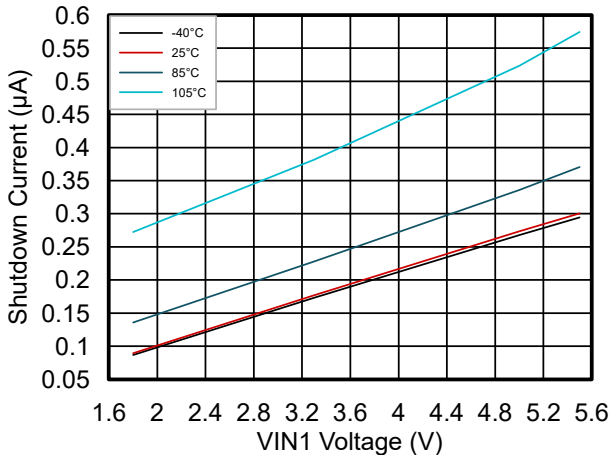
VIN2 = 1.6 V VOUT = Open

図 6-4. VIN1 Standby Current vs Input Voltage



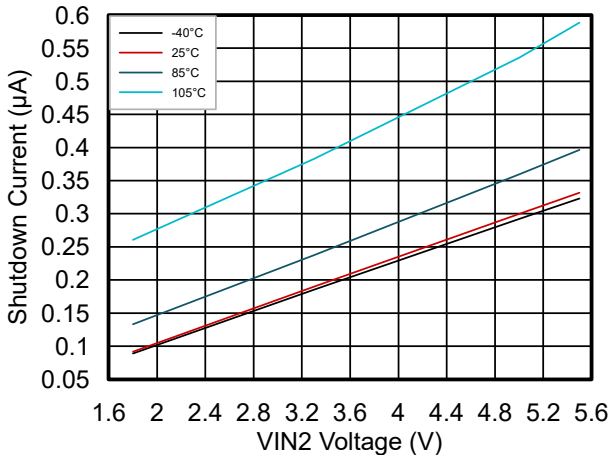
VIN1 = 1.6 V VOUT = Open

図 6-5. VIN2 Standby Current vs Input Voltage



VIN2 = 1.6 V VOUT = Open

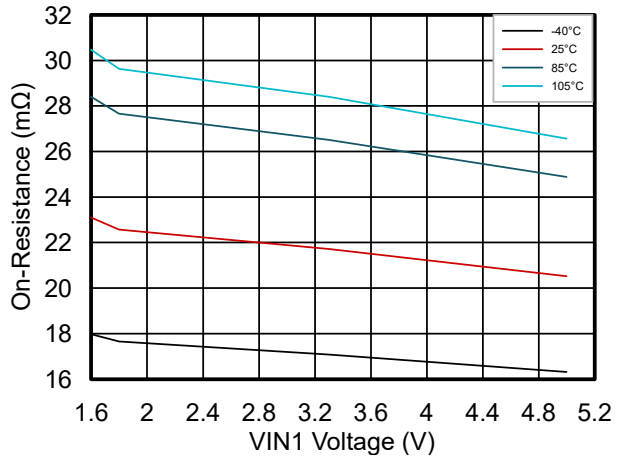
図 6-6. VIN1 Shutdown Current vs Input Voltage



VIN1 = 1.6 V VOUT = 0 V

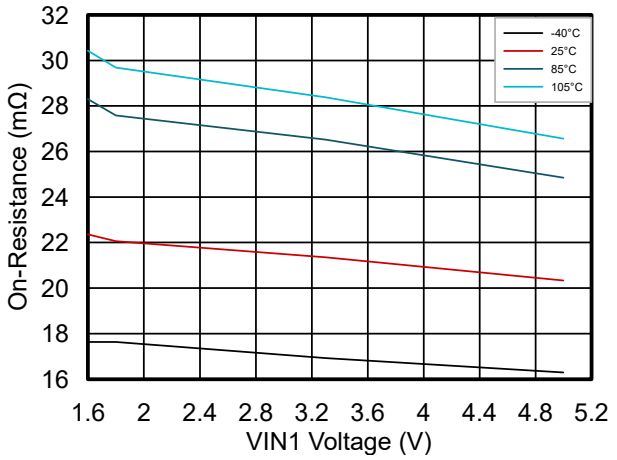
図 6-7. VIN2 Shutdown Current vs Input Voltage

6.8 Typical Characteristics (continued)



I_{OUT} = 200 mA

図 6-8. Channel 1 On-Resistance vs Input Voltage



I_{OUT} = 200 mA

図 6-9. Channel 2 On-Resistance vs Input Voltage

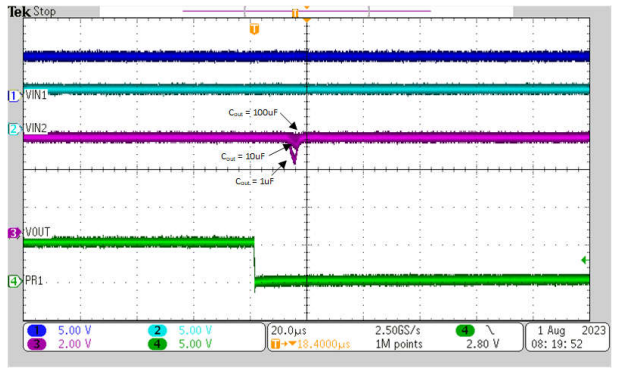


図 6-10. Output Voltage Drop vs Output Capacitance (MODE = V_{IN1} = V_{IN2} = 5 V, R_L = 10 Ω)

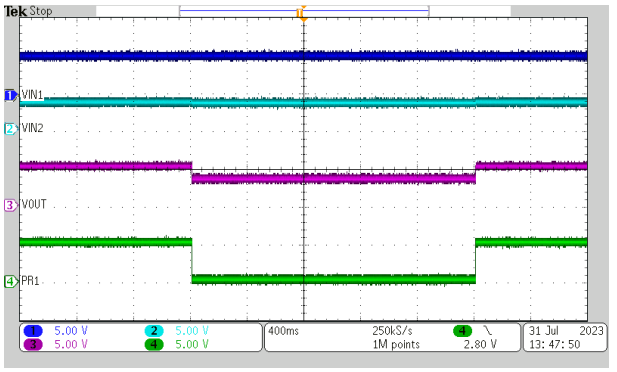


図 6-11. Manual Mode Switchover Behavior (MODE = V_{IN1} = 5 V, V_{IN2} = 3.3 V, R_L = 10 Ω, CL = 10 µF)

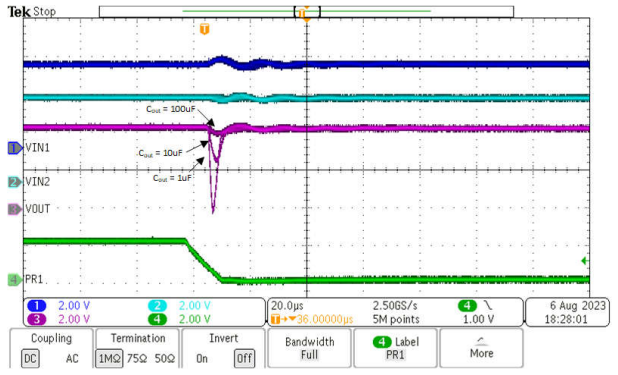


図 6-12. Output Voltage Drop vs Output Capacitance (MODE = V_{IN1} = V_{IN2} = 4 V, R_L = 1 Ω)

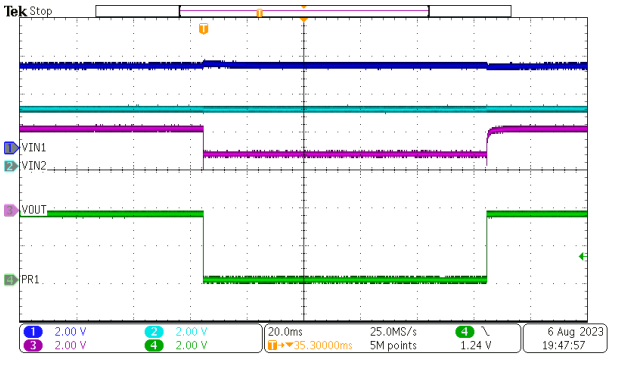


図 6-13. Manual Mode Switchover Behavior (MODE = V_{IN1} = 4 V, V_{IN2} = 3.3 V, R_L = 1 Ω, CL = 10 µF)

7 Detailed Description

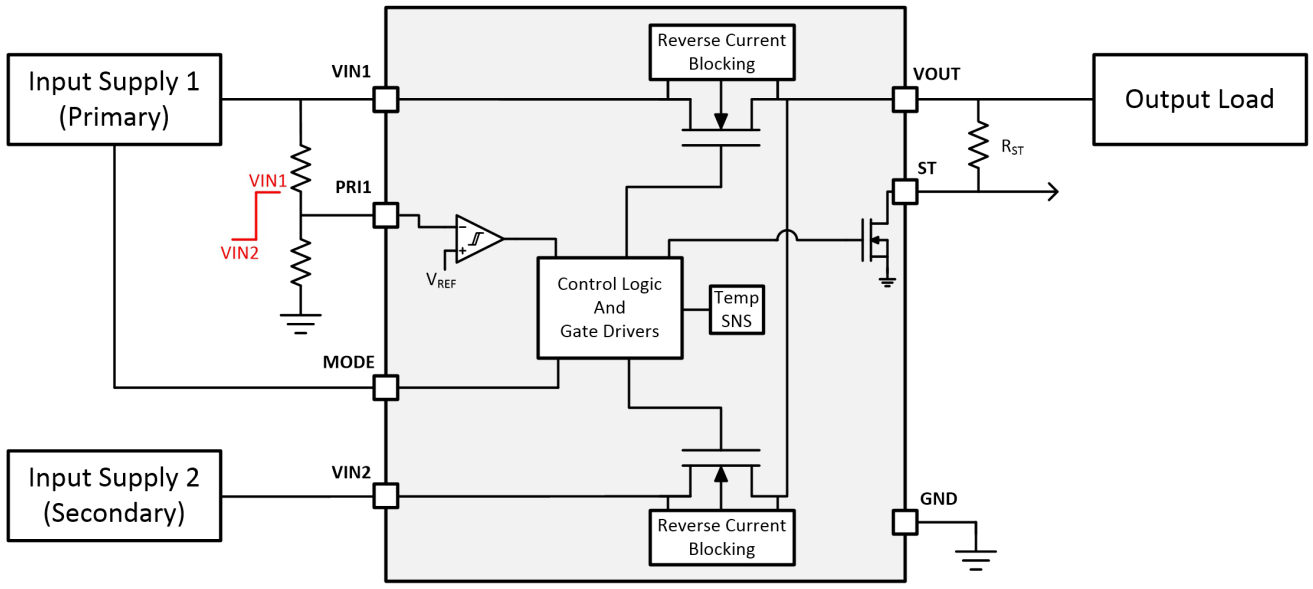
7.1 Overview

The TPS2117 is a power mux device with a voltage rating of 1.6 V to 5.5 V and a maximum current rating of 4 A. The device uses N-channel MOSFETs to switch between supplies while providing a controlled slew rate when voltage is first applied.

The TPS2117 can be configured for two different switchover behaviors depending on the application. Automatic priority mode prioritizes the supply connected to VIN1 and switches over to the secondary supply (VIN2) when VIN1 drops. Manual mode allows the user to toggle a GPIO or enable signal to switch between channels.

Due to its low quiescent of 1.32 µA (typical) and standby current of 50 nA (typical), the TPS2117 is ideal for systems where a battery is connected to one of the inputs. These low currents extend the life and operation of the battery when in use.

7.2 Functional Block Diagram



7.3 Device Functional Modes

TPS2117 can be used in many operating modes depending on the application requirements. The device will always be powered from the highest voltage rail that is connected to the VINx pins. The below sections detail the two different configuraiton options for the device.

7.3.1 Priority and Manual Mode

When MODE is tied high, PR1 determines the channel selected. To configure VIN1 as the priority supply, connect MODE to VIN1 and set the proper threshold through a resistor divider from VIN1 to PR1. To configure manual selection, pull up MODE to an external supply and follow the truth table (表 7-1). When PR1 is pulled above V_{REF}, the voltage on VIN1 is used to power the output, and when it is pulled below V_{REF}, VIN2 is used to power the output. The expected behavior for the device is shown in 図 7-1.

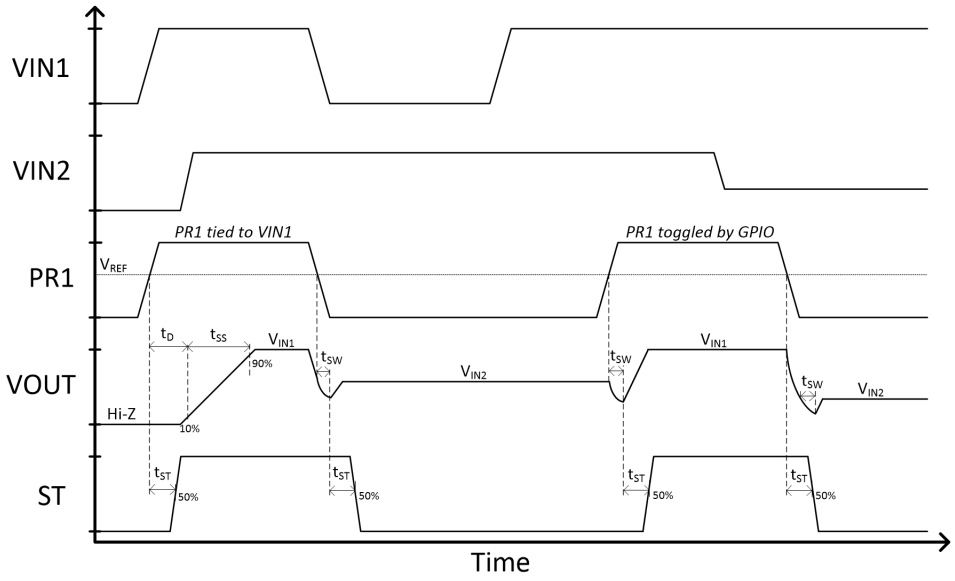


図 7-1. Priority and Manual Mode Switching

When PR1 is toggled, the device implements a break-before-make switchover which shuts off both channels before turning on the new channel to power the output. This means that for time t_{SW}, the output is unpowered and will dip depending on the load current and output capacitance. If the output voltage is greater than the input supply being switched to, then the device will not turn on the new channel until the output has discharged down to V_{IN} + V_{RCB} to prevent reverse current flow.

When MODE is pulled low and PR1 is pulled high, the device enters shutdown. Both channels are turned off and the output is high impedance. When the PR1 pin is pulled low, the higher voltage supply between VIN1 and VIN2 is passed to the output.

7.3.1.1 Priority Switching

In the case where VIN1 takes priority over VIN2, a resistor divider can be used to set the switchover voltage threshold. When VIN1 is first applied, PR1 is brought high and VOUT is powered by that input. As VIN1 begins to drop, the voltage on PR1 is lowered until it crosses the V_{REF} threshold. At this point, the device switches over to VIN2.

7.3.1.2 Manual Switching

For applications where a GPIO pin is used to select which input passes to the output, the GPIO pin can be directly connected to the PR1 pin when MODE is tied high (≥ 1 V). When the GPIO is pulled high, VIN1 is used. When the GPIO pin is pulled low, VIN2 is used.

Manual mode can also disable both channels by pulling the MODE pin low and keeping PR1 high. In this state, the output of the device is high impedance and the leakage on each input is the shutdown current, $I_{SD,VINx}$.

7.3.2 Diode Mode

When the MODE pin is pulled below 0.35 V, the device enters a diode mode of operation. When both inputs are applied to the device, the highest voltage is used to power the output. The PR1 pin is used as an active low device enable, turning off the device when it is pulled high. When the device is turned back on, soft start is used to power the output. The expected behavior for the device is shown in 図 7-2. It is not recommended to use diode operation for two inputs of the same voltage, that is when the device is to multiplex and to connect one input channel to the output. In the event that the input voltage sources are prone to droop in voltage when loaded, it is also recommended to use input capacitance to stabilize the rails. This can especially aid in providing stable input rails during switchover in diode mode.

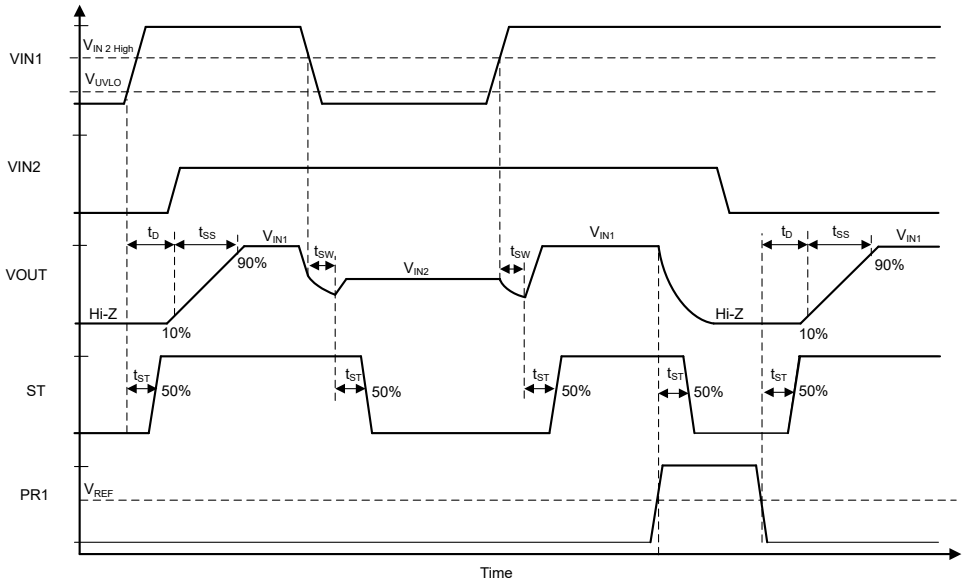


図 7-2. Diode Mode Switching

7.4 Feature Description

The following sections detail the features of the TPS2117.

7.4.1 Truth Table

表 7-1 shows the expected behavior of the TPS2117. Manual mode and priority mode require MODE pin to be connected to source that is within the specification for $V_{IH,MODE}$. This can be either one of the VINx sources or an external bias. For manual mode switching, PR1 is to be controlled via an external source to select between the channels. For priority mode, PR1 voltage is set via a resistor divider from VINx sources. For diode mode, voltage on the MODE pin must be within the specification for $V_{IL,MODE}$.

表 7-1. TPS2117 Truth Table

MODE	VIN1	VIN2	PR1	ST	VOUT
VIN1 or external bias ≥ 1 V (Priority/manual mode)	≥ 1.6 V	X(1)	≥ V_{REF}	High	VIN1
	≥ 1.6 V	≥ 1.6 V	< V_{REF}	Low	VIN2
	< 1.6 V	< 1.6 V	X(1)	Low	Hi-Z
	< 1.6 V	X(1)	≥ V_{REF}	Low	Hi-Z
VIN2 or external bias ≥ 1 V (Priority/manual mode)	X(1)	≥ 1.6 V	< V_{REF}	Low	VIN2
	≥ 1.6 V	≥ 1.6 V	≥ V_{REF}	High	VIN1
	< 1.6 V	< 1.6 V	X(1)	Low	Hi-Z
	X(1)	< 1.6 V	< V_{REF}	Low	Hi-Z
External bias ≤ 0.35 V (Diode mode)	X(1)	X(1)	≥ V_{REF}	Low	Hi-Z
	> V_{IN2} and ≥ 1.6 V	X(1)	< V_{REF}	High	VIN1
	X(1)	> V_{IN1} and ≥ 1.6 V	< V_{REF}	Low	VIN2

(1) X = do not care

7.4.2 Soft Start

When an input voltage is applied to the TPS2117 and the output voltage is lower than 1 V, the output will be brought up with soft start to minimize the inrush current due to output capacitance. However, when the device switches from one power supply to another (switchover) and VOUT > 1 V, soft start is not used to minimize the output voltage drop. For linear soft start behavior, it is recommended to have an output capacitance of at least 0.1 µF.

7.4.3 Status Indication

The ST pin is an open drain output that should be pulled up to an external voltage for proper operation. When the TPS2117 is powering the output using VIN1, the ST pin will be pulled high by the external voltage source. Even if the device is blocking reverse current from VOUT to VIN1, selection of VIN1 will keep the ST pin pulled high. When the TPS2117 is powering the output using VIN2 or both channels are disabled, the ST pin will be pulled low. During thermal shutdown, the ST pin will be pulled low regardless of the channel being used.

7.4.4 Reverse Current Blocking

The TPS2117 initiates reverse current blocking (RCB) when the VOUT voltage is externally biased and exceeds the input voltage supply being used. Once the output voltage is higher than the input voltage by 42 mV ($V_{RCB,R}$), the device will shutoff. During this state, the leakage into VOUT and out of VIN is defined by I_{REV}. Once the voltage difference between the output and input lowers to 17 mV ($V_{RCB,F}$), the channel will turn back on.

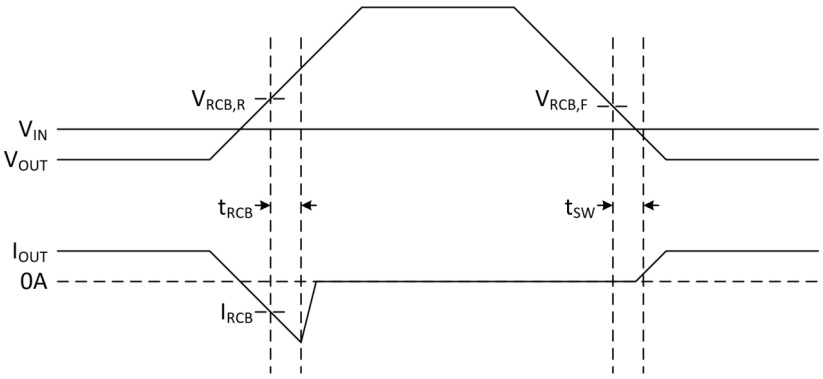


図 7-3. Reverse Current Blocking Behavior

If RCB is expected to occur, it is recommended to clamp the output or use a high output capacitance (about 100 µF). This will prevent voltage spikes from damaging the device due to output inductance. Reverse current is not

a concern during normal switchover from one channel to another. This is because the device implements a break-before-make switching methodology that prevents cross conduction and will not complete switchover until the output voltage is less than the chosen input voltage.

7.5 VINx Collapse Rate

The TPS2117 uses the highest voltage supply to power the device. When one supply drops below the other, the device changes the supply used to power the device. If the supply powering the device drops at a rate faster than 1 V/10 µs, the other supply must be at 2.5 V or higher to prevent the device from resetting. If the other supply is lower than 2.5 V, then the device may not be able to switch to the supply quickly enough, and the device will reset and turn on with soft start timing if VOUT < 1 V.

7.6 Fast Switchover Behavior

The TPS2117 transitions between a primary and secondary supply with a fast switchover time of t_{SW}. After the secondary input is connected to the output, like t_{SW}, the device heavily drives the channel of the secondary supply to ramp up the output voltage as fast as possible. This is performed to keep the driven load in a stable operating condition and to minimize the voltage dip. The duration of this channel boost is typically 11 µs. In the case of a heavy load, the output voltage may not reach the final value after 11 µs and in this case the device reverts back to the soft start output ramp rate. This behavior reduces the amount of time a large pulse of current can flow through the enabled channel and into the load.

7.7 Output Voltage Drop

The output voltage drop during switchover from one supply to another is based on the load capacitance and load resistance. The stronger the resistive load, the faster the output will discharge. The higher the capacitance on the output, the less the voltage will drop during switchover.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

This section highlights some of the design considerations when implementing this device in various applications.

8.2 Typical Application

This typical application demonstrates how the TPS2117 device can be used to control inrush current for high output capacitances.

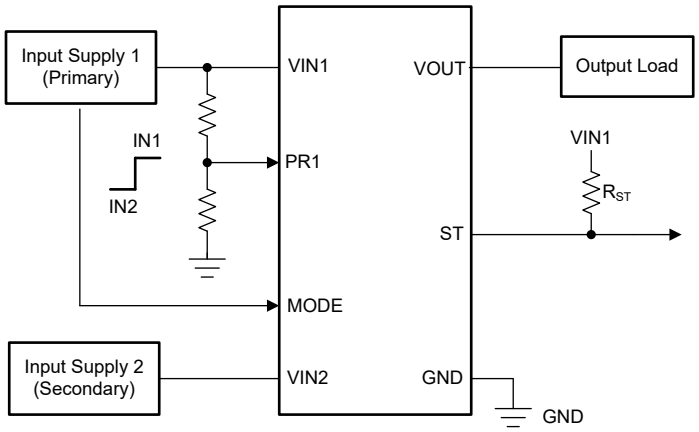


図 8-1. TPS2117 Typical Application Diagram

8.2.1 Design Requirements

For this example, the values below are used as the design parameters.

表 8-1. Design Parameters

PARAMETER	VALUE
VIN1 input voltage	5 V
Mode	Priority
Output capacitance	100 µF
Maximum inrush current	500 mA

8.2.2 Detailed Design Procedure

To determine how much inrush current is caused by the output capacitor, use 式 1.

$$I_{INRUSH} = C_{OUT} \times V_{OUT} / t_{SS} \quad (1)$$

where

- I_{INRUSH} = amount of inrush current caused by C_{OUT}
- C_{OUT} = capacitance on V_{OUT}
- t_{SS} = output voltage soft start time
- V_{OUT} = final value of the output voltage

With a final output voltage of 5 V, the expected rise time is 1.7 ms. Using the inrush current equation, the inrush current caused by a 100-µF capacitance would be 294 mA, well below the 500-mA target.

8.2.3 Application Curves

図 8-2 shows 5 V being applied to VIN1. The output comes up with slew rate control and limits the inrush current to below 500 mA.

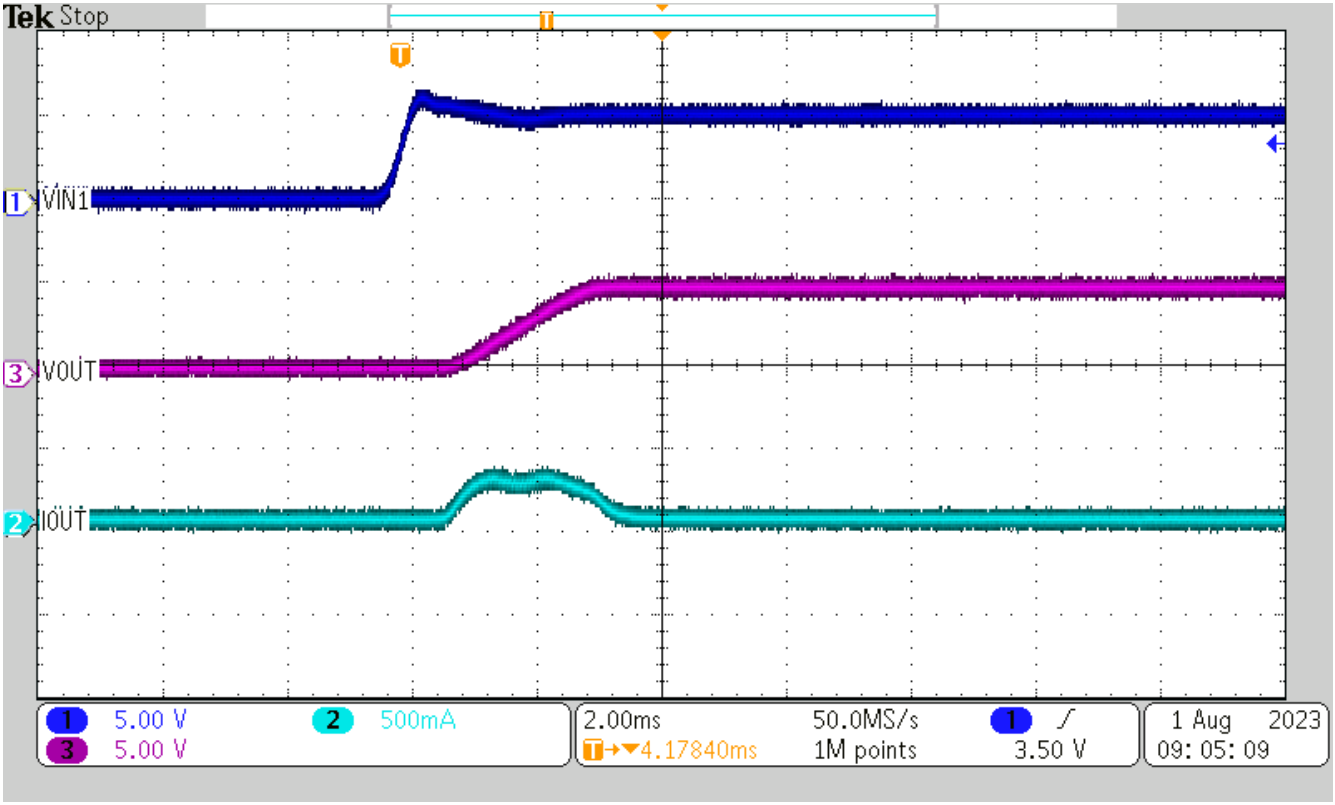


図 8-2. TPS2117 Inrush Current Control

8.3 Power Supply Recommendations

The device is designed to operate with a VIN range of 1.6 V to 5.5 V. The VIN power supplies must be well regulated and placed as close to the device terminals as possible. The power supplies must be able to withstand all transient load current steps. In most situations, using an input capacitance (C_{IN}) of 1 µF is sufficient to prevent the supply voltage from dipping when the switch is turned on. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance may be required on the input.

8.4 Layout

8.4.1 Layout Guidelines

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for VIN1, VIN2, VOUT, and GND helps minimize the parasitic electrical effects.

8.4.2 Layout Example

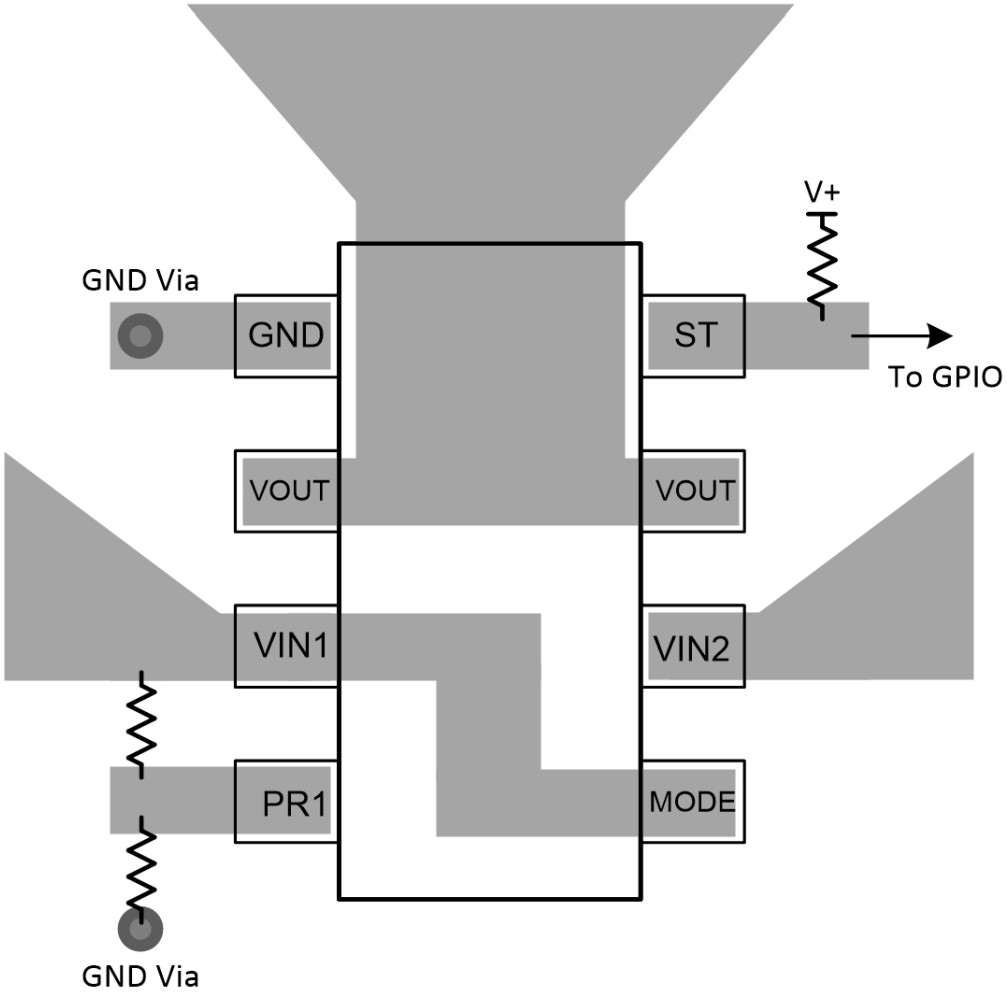


図 8-3. TPS2117 Layout Example

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- Basics of Power MUX
- 11 Ways to Protect Your Power Path

9.2 ドキュメントの更新通知を受け取る方法

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9.4 静電気放電に関する注意事項

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9.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS2117DRLR	Active	Production	SOT-5X3 (DRL) | 8	4000 | LARGE T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 125	2117
TPS2117DRLR.A	Active	Production	SOT-5X3 (DRL) | 8	4000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 105	2117
TPS2117DRLR.B	Active	Production	SOT-5X3 (DRL) | 8	4000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 105	2117

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

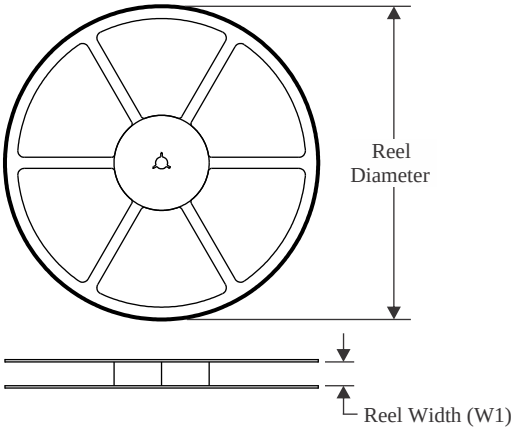
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

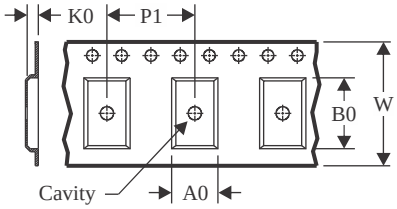
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

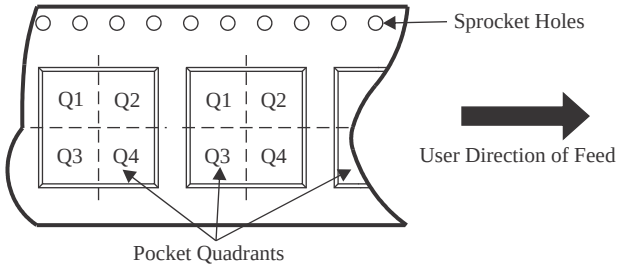


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

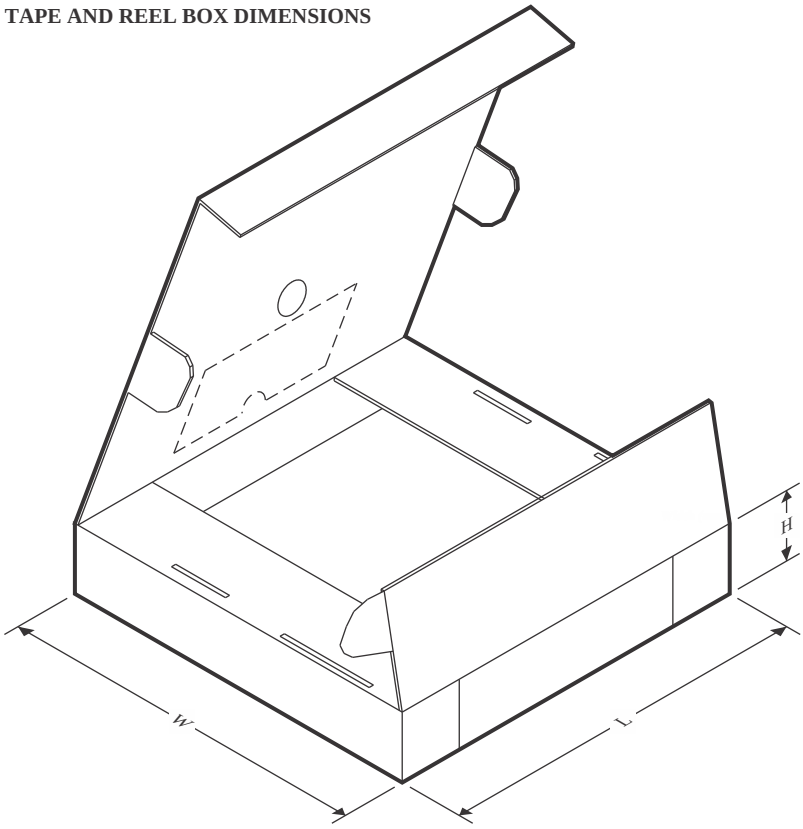
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2117DRLR	SOT-5X3	DRL	8	4000	180.0	8.4	2.75	1.9	0.8	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

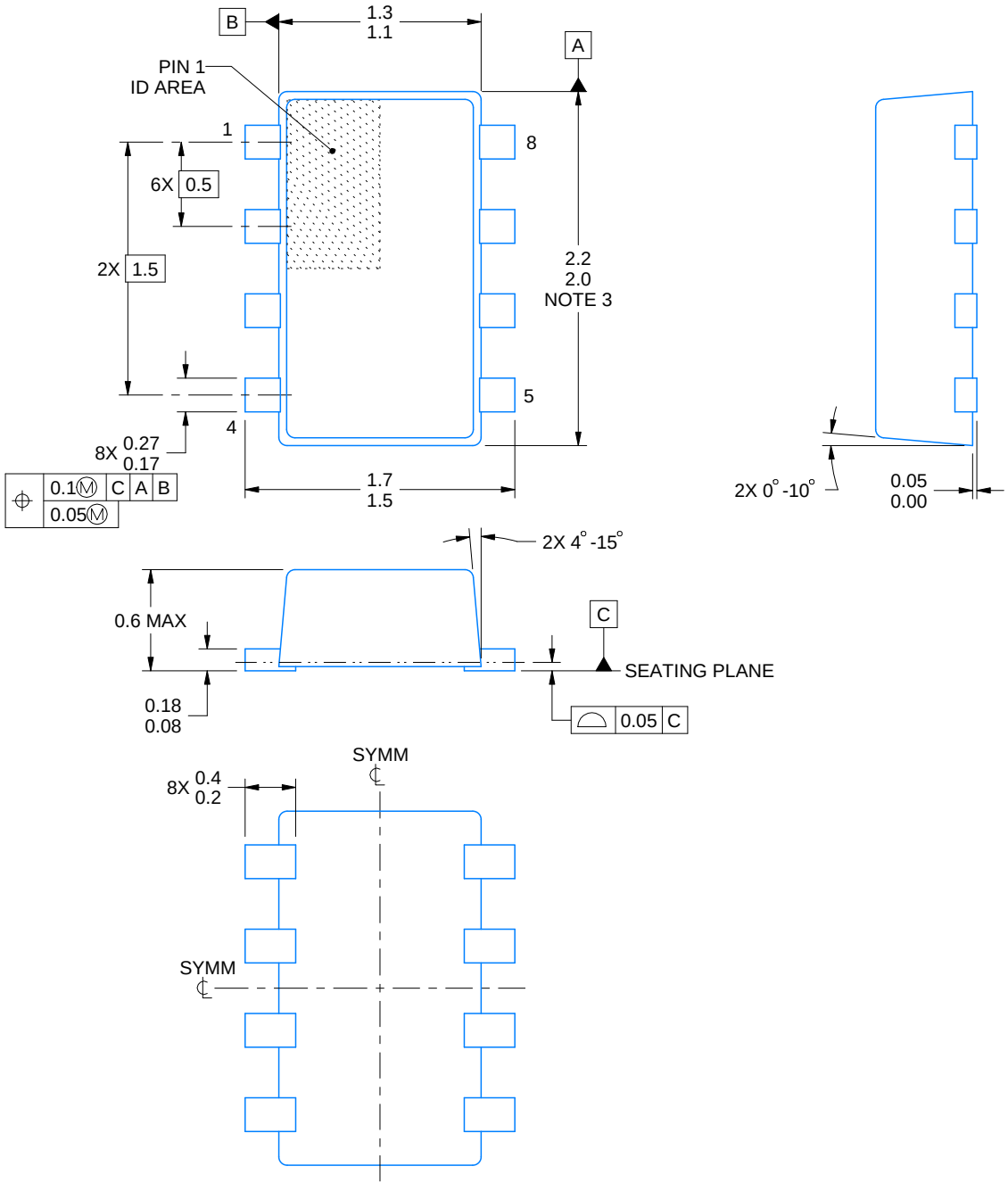
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2117DRLR	SOT-5X3	DRL	8	4000	210.0	185.0	35.0

PACKAGE OUTLINE

DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



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NOTES:

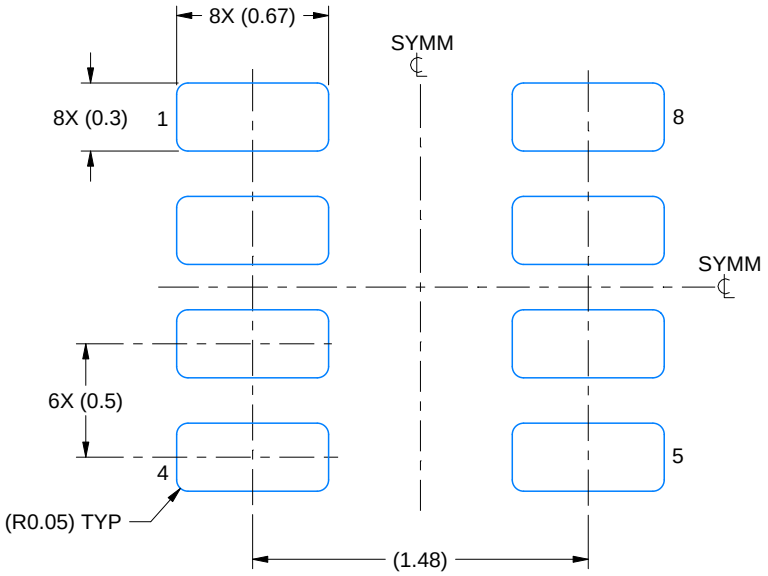
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC Registration MO-293, Variation UDAD

EXAMPLE BOARD LAYOUT

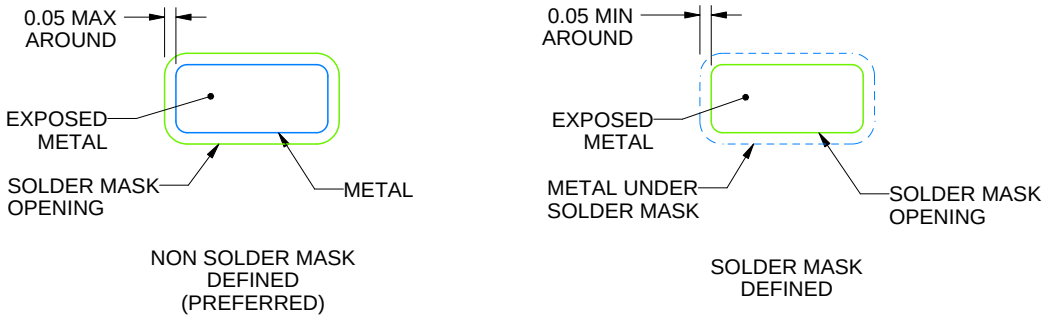
DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



SOLDERMASK DETAILS

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NOTES: (continued)

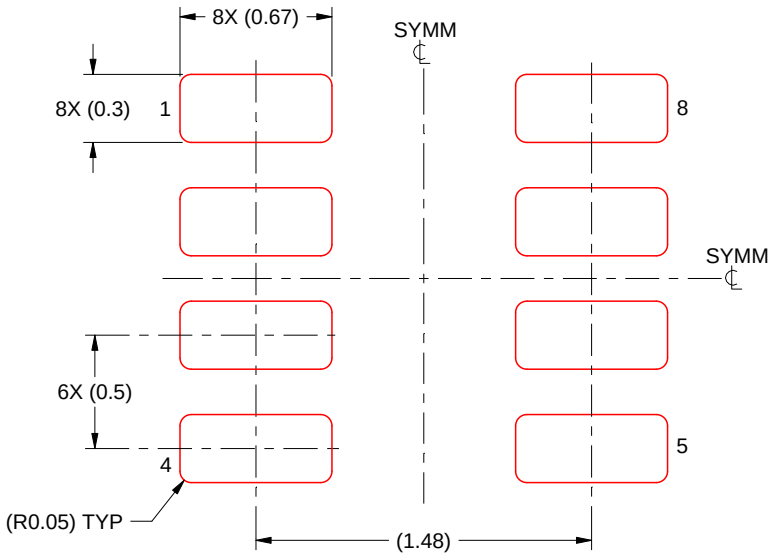
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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