TEXAS INSTRUMENTS
TPS2041B-Q1, TPS2042B-Q1, TPS2051B-Q1
JAJSJN2D – NOVEMBER 2007 – REVISED OCTOBER 2020

# TPS20xxB-Q1 電流制限パワー・ディストリビューション・スイッチ

## 1 特長

- 車載アプリケーション認定済み
- 下記内容で AEC-Q100 認定済み:
  - デバイス温度グレード 1:-40℃～125℃ の動作時周囲温度範囲
  - デバイス HBM ESD 分類レベル 2
  - デバイス CDM ESD 分類レベル C6
  - デバイス MM ESD 分類レベル M0
- 105mΩ のハイサイド MOSFET
- 500mA の連続電流
- 過熱および短絡保護
- 正確な電流制限:0.75A (最小値)、1.25A (最大値)
- 動作範囲:2.7V～5.5V
- 0.6ms の標準立ち上がり時間
- 低電圧誤動作防止
- デグリッチ・フォルト・レポート ($\overline{OC}$)
- 電源投入時の $\overline{OC}$ グリッチなし
- スタンバイ時の最大電源電流:1μA (シングル、デュアル) または 2μA (トリプル、クワッド)
- 双方向スイッチ
- UL はファイル番号 E169910 で認識されています

## 2 アプリケーション

- 大きな容量性負荷
- 短絡保護

## 3 概要

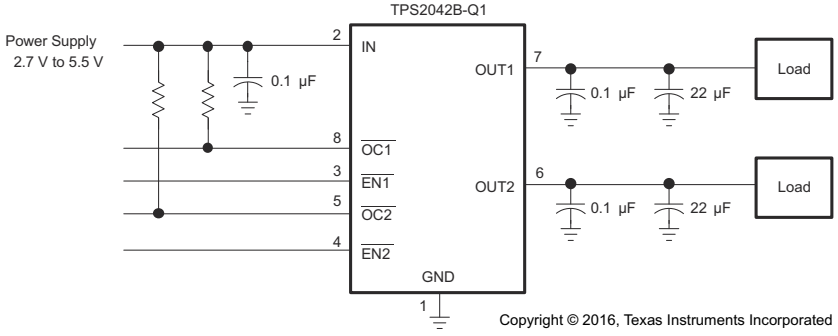
TPS20xxB-Q1 パワー・ディストリビューション・スイッチは、大きな容量性負荷があり、短絡が発生しやすいアプリケーションを対象としています。これらのデバイスは、複数のパワー・スイッチを 1 つのパッケージに搭載する必要があるパワー・ディストリビューション・システム向けに、105mΩ の N チャネル MOSFET パワー・スイッチを内蔵しています。各スイッチは、ロジック・イネーブル入力によって制御されます。ゲート・ドライブは、内部チャージ・ポンプによって供給され、スイッチング中の電流サージを最小限に抑えるために、パワー・スイッチの立ち上がり時間と立ち下がり時間を制御するように設計されています。チャージ・ポンプには外付け部品が不要で、最低 2.7V の電源で動作できます。

出力負荷が電流制限スレッショルドを超えた場合、または短絡が存在する場合、デバイスは定電流モードに切り替えて過電流 ($\overline{OCx}$) ロジック出力を Low にすることで、出力電流を安全なレベルに制限します。連続的に大きな過負荷と短絡が発生すると、スイッチの消費電力が増加し、接合部温度が上昇すると、熱保護回路によってスイッチがシャットオフされ、損傷を防止します。デバイスの温度が十分に低下すると、自動的にサーマル・シャットダウンからの回復が行われます。内部回路により、有効な入力電圧が印加されるまでスイッチがオフに維持されます。このパワー・ディストリビューション・スイッチは、電流制限を 1A (標準値) に設定するように設計されています。

**製品情報**(1)

| 部品番号 | パッケージ | 本体サイズ (公称) |
|---|---|---|
| TPS2041B-Q1 | SOT-23 (5) | 2.80mm × 2.90mm |
| TPS2042B-Q1、TPS2051B-Q1 | SOIC (8) | 4.90mm × 6.00mm |

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。




**代表的なアプリケーション回路図**

# Table of Contents



## 4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| Changes from Revision C (September 2016) to Revision D (October 2020) | Page |
|---|---|
| • 文書全体にわたって表、図、相互参照の採番方法を更新 | 1 |
| • 「特長」一覧の「70mΩ ハイサイド MOSFET」を「105mΩ ハイサイド MOSFET」に変更 | 1 |
| • 「概要」セクションの「70mΩ ハイサイド MOSFET」を「105mΩ ハイサイド MOSFET」に変更 | 1 |
| • Updated $r_{DS(ON)}$ TYP and MAX values in the *Electrical Characteristics* table | 5 |
| • Updated 図 6-9 | 7 |
| • Changed "70-mΩ High-Side MOSFET" to "105-mΩ High-Side MOSFET" in the *Overview* section | 10 |

| Changes from Revision B (October 2011) to Revision C (September 2016) | Page |
|---|---|
| • 「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加。 | 1 |
| • 「注文情報」表を削除 (データシートの末尾にある POA を参照) | 1 |
| • 汎用スイッチ・カタログの画像を削除 | 1 |
| • AEC-Q100 認定の箇条書きを追加 | 1 |
| • Added *Thermal Information* table | 5 |
| • Deleted *Dissipation Ratings* section | 7 |
| • Combined Functional Block Diagrams for TPS2041B-Q1 and TPS2051B-Q1 as they are the same | 10 |

| Changes from Revision A (June 2010) to Revision B (October 2011) | Page |
|---|---|
| • 注文部品番号を TPS2041QDBVRQ1 から TPS2041BQDBVRQ1 に変更 | 1 |

| Changes from Revision * (November 2007) to Revision A (June 2010) | Page |
|---|---|
| • TPS2041B-Q1 のデバイス情報を追加 | 1 |

## 5 Pin Configuration and Functions

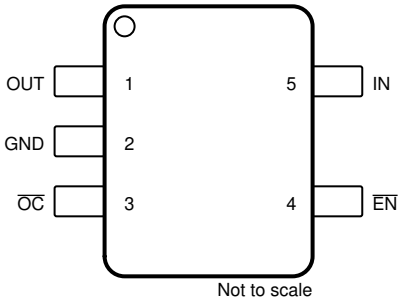



図 5-1. TPS2041B-Q1 DBV Package 5-Pin SOT-23 Top View

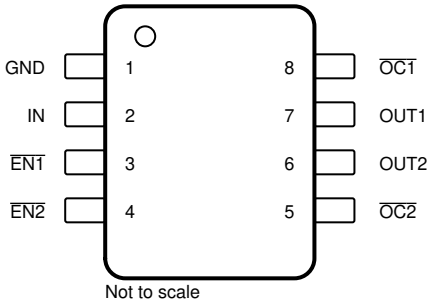



図 5-2. TPS2042B-Q1 D Package 8-Pin SOIC Top View

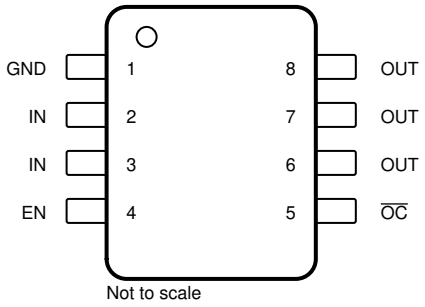



図 5-3. TPS2051B-Q1 D Package 8-Pin SOIC Top View

表 5-1. Pin Functions: TPS2041B-Q1

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| EN | 4 | I | Enable input, logic low turns on power switch |
| GND | 2 | GND | Ground |
| IN | 5 | PWR | Supply input voltage |
| OC | 3 | O | Overcurrent, open-drain output, active low |
| OUT | 1 | O | Power-switch output |

表 5-2. Pin Functions: TPS2042B-Q1

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| EN1 | 3 | I | Enable input, logic low turns on power switch IN-OUT1 |
| EN2 | 4 | I | Enable input, logic low turns on power switch IN-OUT2 |
| GND | 1 | GND | Ground |
| IN | 2 | PWR | Supply input voltage |
| OC1 | 8 | O | Overcurrent, open-drain output, active low, IN-OUT1 |
| OC2 | 5 | O | Overcurrent, open-drain output, active low, IN-OUT2 |

**表 5-2. Pin Functions: TPS2042B-Q1 (continued)**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| OUT1 | 7 | O | Power-switch output, IN-OUT1 |
| OUT2 | 6 | O | Power-switch output, IN-OUT2 |

**表 5-3. Pin Functions: TPS2051B-Q1**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| EN | 4 | I | Enable input, logic high turns on power switch |
| GND | 1 | GND | Ground |
| IN | 2, 3 | PWR | Supply input voltage |
| $\overline{OC}$ | 5 | O | Overcurrent open-drain output, active low |
| OUT | 6, 7, 8 | O | Power-switch output |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Input voltage(2) | IN | –0.3 | 6 | V |
| Output voltage(2) | OUT, OUTx | –0.3 | 6 | V |
| Input voltage | $\overline{ENx}$, EN | –0.3 | 6 | V |
| Voltage, $V_{I(\overline{OC})}$, $V_{I(\overline{OCx})}$ | $\overline{OC}$, $\overline{OCx}$ | –0.3 | 6 | V |
| Continuous output current | | Internally limited | | |
| Continuous total power dissipation | | See *ESD Ratings* | | |
| Operating virtual-junction temperature, $T_J$ | | –40 | 125 | °C |
| Storage temperature, $T_{stg}$ | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| TPS2041B-Q1 in DBV Package and TPS2042B-Q1 in D package | | | | |
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002(1) | ±2500 | V |
| | | Charged-device model (CDM), per AEC Q100-011 | ±1500 | |
| | | Machine model (MM), per AEC Q100-003 | ±50 | |
| TPS2051B-Q1 in D package | | | | |
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002(1) | ±2000 | V |
| | | Charged-device model (CDM), per AEC Q100-011 | ±1500 | |
| | | Machine model (MM), per AEC Q100-003 | ±50 | |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 6.3 Recommended Operating Conditions

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{I(IN)}$ | Input voltage (IN) | 2.7 | 5.5 | V |
| $V_{I(\overline{ENx})}$, $V_{I(EN)}$ | Input voltage ( $\overline{ENx}$, EN) | 0 | 5.5 | V |
| $I_{O(OUT)}$, $I_{O(OUTx)}$ | Continuous output current (OUT, OUTx) | 0 | 500 | mA |
| $T_J$ | Operating virtual-junction temperature | –40 | 125 | °C |

## 6.4 Thermal Information

| THERMAL METRIC[1] | | TPS2041B-Q1 DBV (SOT-23) 5 PINS | TPS2042B-Q1 D (SOIC) 8 PINS | TPS2051B-Q1 D (SOIC) 8 PINS | UNIT |
|---|---|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 224.1 | 117.2 | 124.5 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 131.2 | 63.3 | 72.7 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 55.4 | 57.5 | 64.9 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 19.2 | 15.3 | 24.7 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 54.3 | 37 | 64.4 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Electrical Characteristics

over recommended operating junction temperature range, $V_{I(IN)}$ = 5.5 V, $I_O$ = 0.5 A, $V_{I(\overline{ENx})}$ = 0 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS[1] | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| **POWER SWITCH** | | | | | | | | |
| $r_{DS(ON)}$ | Static drain-source on-state resistance, 5-V or 3.3-V operation | $V_{I(IN)}$ = 5 V or 3.3 V, $I_O$ = 0.5 A | –40°C ≤ $T_J$ ≤ 125°C | | | 105 | 160 | mΩ |
| | Static drain-source on-state resistance, 2.7-V operation[2] | $V_{I(IN)}$ = 2.7 V, $I_O$ = 0.5 A | –40°C ≤ $T_J$ ≤ 125°C | | | 110 | 175 | |
| $t_r$ | Rise time, output[2] | $V_{I(IN)}$ = 5.5 V | $C_L$ = 1 µF, $R_L$ = 10 Ω | $T_J$ = 25°C | | 0.6 | 1.5 | ms |
| | | $V_{I(IN)}$ = 2.7 V | | | | 0.4 | 1 | |
| $t_f$ | Fall time, output[2] | $V_{I(IN)}$ = 5.5 V | $C_L$ = 1 µF, $R_L$ = 10 Ω | $T_J$ = 25°C | 0.05 | | 0.5 | ms |
| | | $V_{I(IN)}$ = 2.7 V | | | 0.05 | | 0.5 | |
| **ENABLE INPUT ( $\overline{EN}$, $\overline{ENx}$)** | | | | | | | | |
| $V_{IH}$ | High-level input voltage | 2.7 V ≤ $V_{I(IN)}$ ≤ 5.5 V | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | 2.7 V ≤ $V_{I(IN)}$ ≤ 5.5 V | | | | | 0.8 | |
| $I_I$ | Input current | $V_{I(\overline{ENx})}$ = 0 V or 5.5 V | | | –0.5 | | 0.5 | µA |
| $t_{on}$ | Turnon time[2] | $C_L$ = 100 µF, $R_L$ = 10 Ω | | | | | 3 | ms |
| $t_{off}$ | Turnoff time[2] | $C_L$ = 100 µF, $R_L$ = 10 Ω | | | | | 10 | |
| **CURRENT LIMIT** | | | | | | | | |
| $I_{OS}$ | Short-circuit output current | $V_{I(IN)}$ = 5 V, OUT connected to GND, device enabled into short-circuit | | $T_J$ = 25°C | 0.65 | 1 | 1.25 | A |
| | | | | –40°C ≤ $T_J$ ≤ 125°C | 0.6 | 1 | 1.3 | |
| **SUPPLY CURRENT (TPS2041B-Q1, TPS2051B-Q1)** | | | | | | | | |
| | Supply current, low-level output | No load on OUT, $V_{I(\overline{EN})}$ = 5.5 V or $V_{I(EN)}$ = 0 V | | $T_J$ = 25°C | | 0.5 | 1 | µA |
| | | | | –40°C ≤ $T_J$ ≤ 125°C | | 0.5 | 5 | |
| | Supply current, high-level output | No load on OUT, $V_{I(\overline{EN})}$ = 0 V or $V_{I(EN)}$ = 5.5 V | | $T_J$ = 25°C | | 43 | 60 | µA |
| | | | | –40°C ≤ $T_J$ ≤ 125°C | | 43 | 70 | |
| | Leakage current | OUT connected to ground, $V_{I(\overline{EN})}$ = 5.5 V or $V_{I(EN)}$ = 0 V | | –40°C ≤ $T_J$ ≤ 125°C | | 1 | | µA |
| | Reverse leakage current | $V_{I(OUTx)}$ = 5.5 V, IN = ground[2] | | $T_J$ = 25°C | | 0 | | µA |

## 6.5 Electrical Characteristics (continued)

over recommended operating junction temperature range, $V_{I(IN)}$ = 5.5 V, $I_O$ = 0.5 A, $V_{I(\overline{ENx})}$ = 0 V (unless otherwise noted)

| PARAMETER | TEST CONDITIONS[1] | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY CURRENT (TPS2042B-Q1)** | | | | | | |
| Supply current, low-level output | No load on OUT, $V_{I(\overline{ENx})}$ = 5.5 V | $T_J$ = 25°C | | 0.5 | 1 | µA |
| | | –40°C ≤ $T_J$ ≤ 125°C | | 0.5 | 5 | |
| Supply current, high-level output | No load on OUT, $V_{I(\overline{ENx})}$ = 0 V | $T_J$ = 25°C | | 50 | 70 | µA |
| | | –40°C ≤ $T_J$ ≤ 125°C | | 50 | 90 | |
| Leakage current | OUT connected to ground, $V_{I(\overline{ENx})}$ = 5.5 V | –40°C ≤ $T_J$ ≤ 125°C | | 1 | | µA |
| Reverse leakage current | $V_{I(OUTx)}$ = 5.5 V, IN = ground[2] | $T_J$ = 25°C | | 0.2 | | µA |
| **UNDERVOLTAGE LOCKOUT** | | | | | | |
| Low-level input voltage, IN, INx | | | 2 | | 2.5 | V |
| Hysteresis, IN, INx | | $T_J$ = 25°C | | 75 | | mV |
| **OVERCURRENT ( $\overline{OC}$, $\overline{OCx}$)** | | | | | | |
| Output low voltage, $V_{OL(\overline{OCx})}$ | $I_{O(\overline{OCx})}$ = 5 mA | | | | 0.4 | V |
| OFF-state current[2] | $V_{O(\overline{OCx})}$ = 5 V or 3.3 V | | | | 1 | µA |
| $\overline{OC}$ deglitch[2] | $\overline{OCx}$ assertion or deassertion | | 4 | 8 | 15 | ms |
| **THERMAL SHUTDOWN**[3] | | | | | | |
| Thermal shutdown threshold[2] | | | 135 | | | °C |
| Recovery from thermal shutdown[2] | | | 125 | | | °C |
| Hysteresis[2] | | | | 10 | | °C |

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be accounted for separately.
(2) Specified by design.
(3) The thermal shutdown only reacts under overcurrent conditions.

## 6.6 Typical Characteristics

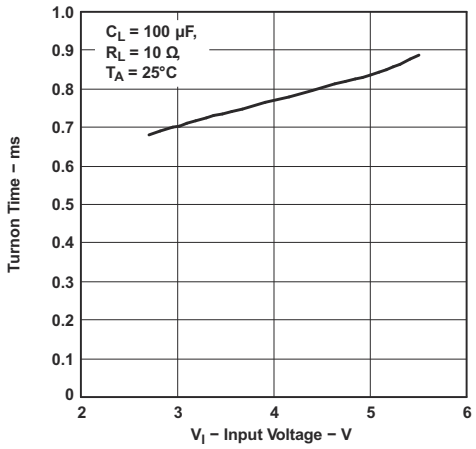



図 6-1. Turnon Time vs Input voltage

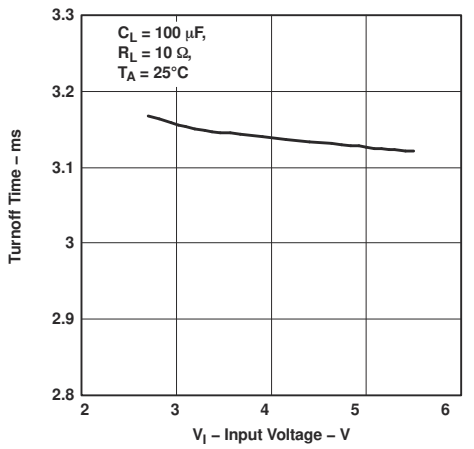



図 6-2. Turnoff Time vs Input Voltage

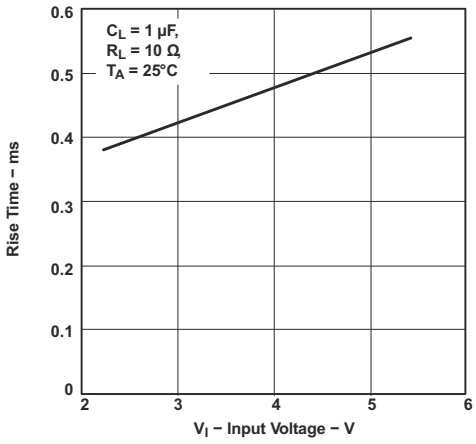



図 6-3. Rise Time vs Input Voltage

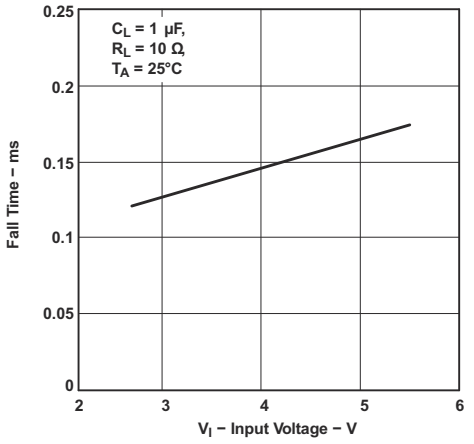



図 6-4. Fall Time vs Input Voltage

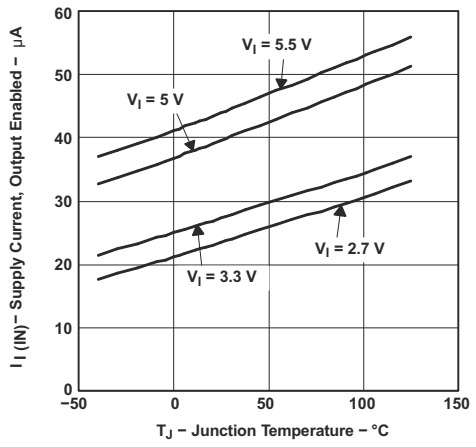



図 6-5. TPS2041B-Q1 and TPS2051B-Q1 Supply Current, Output Enabled vs Junction Temperature

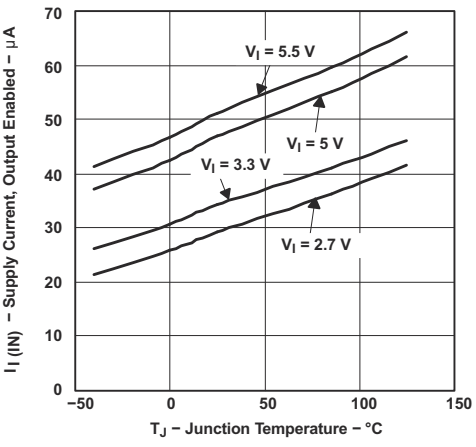



図 6-6. TPS2042B-Q1 Supply Current, Output Enabled vs Junction Temperature

## 6.6 Typical Characteristics (continued)

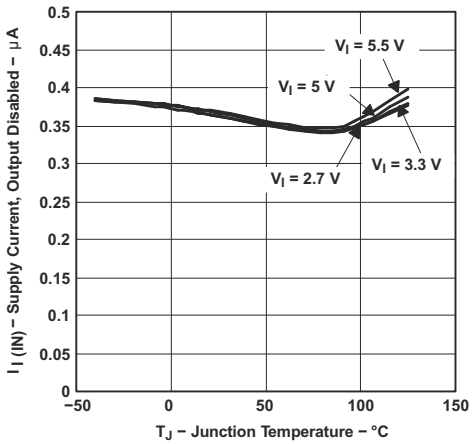



図 6-7. TPS2041B-Q1 and TPS2051B-Q1 Supply Current, Output Disabled vs Junction Temperature

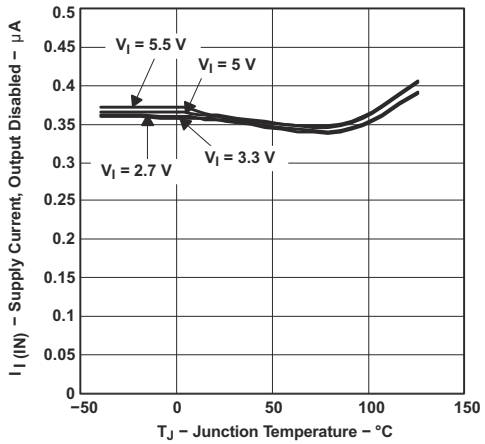



図 6-8. TPS2042B-Q1 Supply Current, Output Disabled vs Junction Temperature

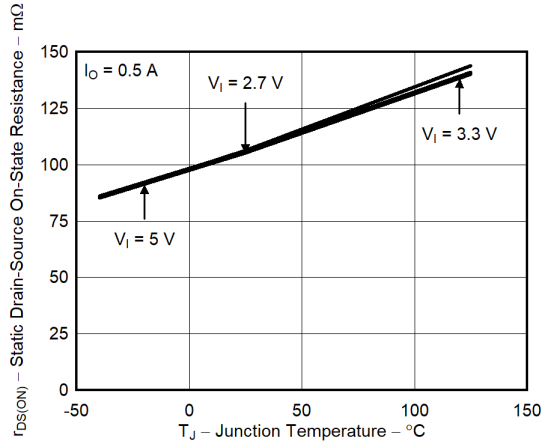



図 6-9. Static Drain-Source ON-state Resistance vs Junction Temperature

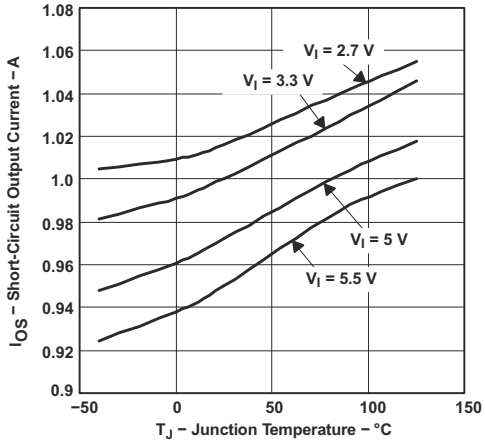



図 6-10. Short-Circuit Output Current vs Junction Temperature

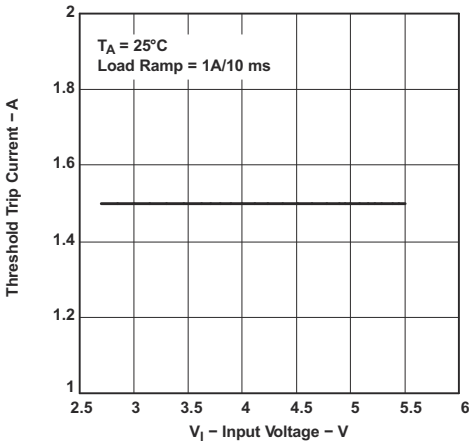



図 6-11. Threshold Trip Current vs Input Voltage

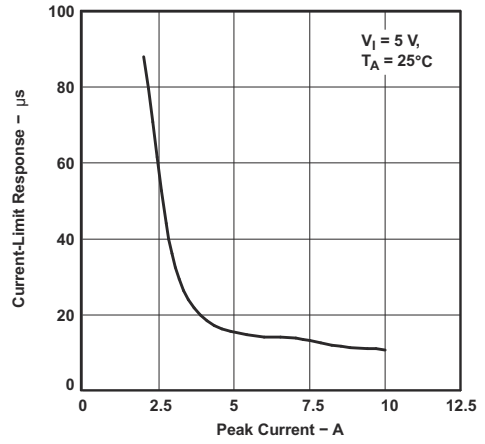



図 6-12. Current-Limit Response vs Peak Current

## 6.6 Typical Characteristics (continued)

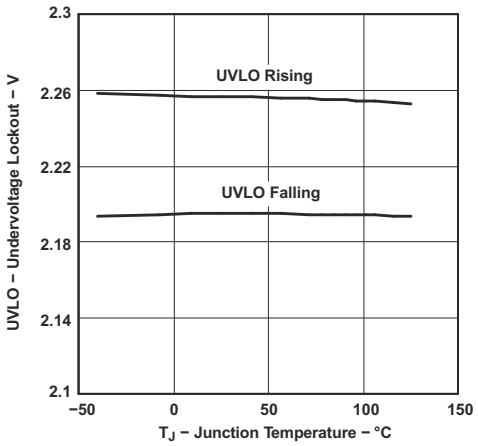



図 6-13. Undervoltage Lockout vs Junction Temperature

## 7 Parameter Measurement Information

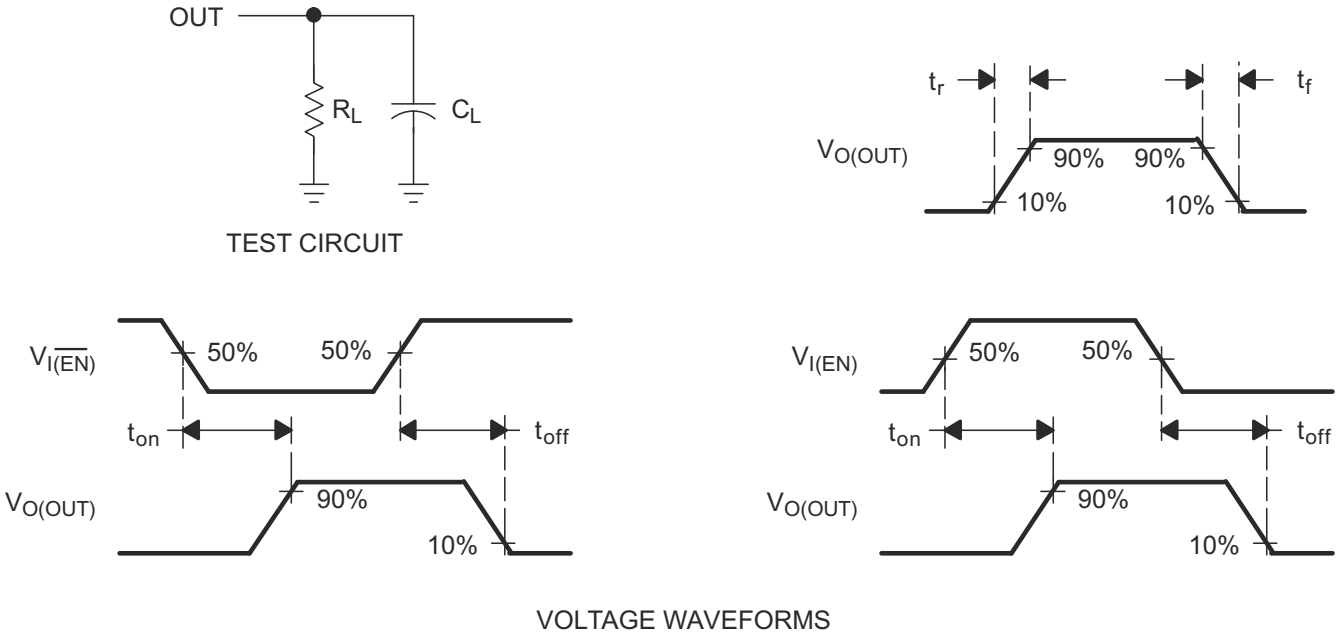


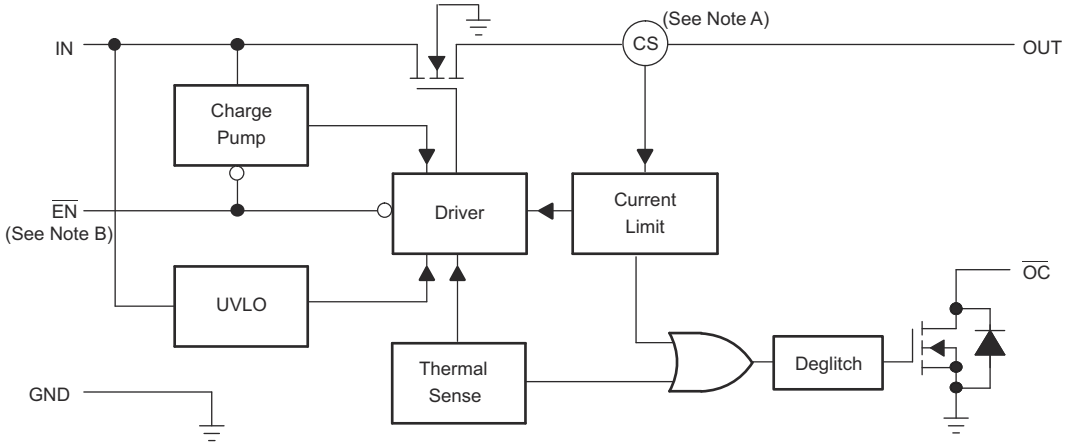

図 7-1. Test Circuit and Voltage Waveforms

# 8 Detailed Description

## 8.1 Overview

The TPS20xxB-Q1 devices are current-limited, power-distribution switches providing 0.5-A continuous-load current. These devices incorporate 105-mΩ N-channel MOSFET power switches for power-distribution systems that require multiple power switches in a single package. A gate driver is provided by an internal charge pump designed to minimize current surges during switching. The charge pump requires no external components and allows operation supplies as low as 2.7 V.

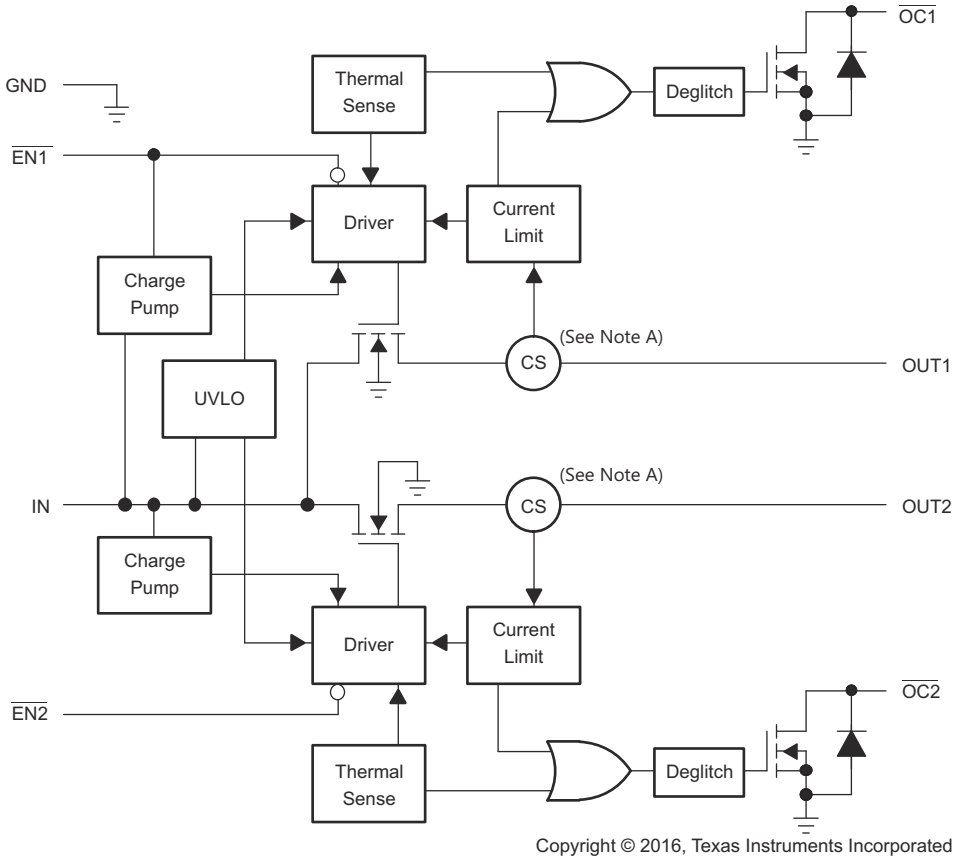
## 8.2 Functional Block Diagrams




A. CS = Current sense

B. EN = Active low ( $\overline{EN}$) for TPS2041B-Q1; Active high (EN) for TPS2051B-Q1

**図 8-1. Functional Block Diagram (TPS2041B-Q1 and TPS2051B-Q1)**




A. CS = Current sense

**図 8-2. Functional Block Diagram (TPS2042B-Q1)**

## 8.3 Feature Description

### 8.3.1 Power Switch

The power switch is an N-channel MOSFET with a low ON-state resistance. Configured as a high-side switch, the power switch prevents current flow from OUT to IN and IN to OUT when disabled. The power switch supplies a minimum current of 500 mA.

### 8.3.2 Charge Pump

An internal charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7 V and requires little supply current.

### 8.3.3 Driver

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage.

### 8.3.4 Enable ( $\overline{\text{ENx}}$)

The logic enable pin disables the power switch and the bias for the charge pump, driver, and other circuitry to reduce the supply current. The supply current is reduced to less than 1 µA or 2 µA when a logic high is present on $\overline{\text{EN}}$. A logic zero input on $\overline{\text{EN}}$ restores bias to the drive and control circuits and turns the switch on. The enable input is compatible with both TTL and CMOS logic levels.

### 8.3.5 Enable (EN)

The logic enable disables the power switch and the bias for the charge pump, driver, and other circuitry to reduce the supply current. The supply current is reduced to less than 1 µA or 2 µA when a logic low is present on EN. A logic high input on EN restores bias to the drive and control circuits and turns the switch on. The enable input is compatible with both TTL and CMOS logic levels.

### 8.3.6 Overcurrent ( $\overline{\text{OCx}}$)

The $\overline{\text{OCx}}$ open-drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output remains asserted until the overcurrent or overtemperature condition is removed. A 10-ms deglitch circuit prevents the $\overline{\text{OCx}}$ signal from oscillation or false triggering. If an overtemperature shutdown occurs, the $\overline{\text{OCx}}$ is asserted instantaneously.

### 8.3.7 Current Sense

A sense FET monitors the current supplied to the load. The sense FET measures current more efficiently than conventional resistance methods. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver in turn reduces the gate voltage and drives the power FET into its saturation region, which switches the output into a constant-current mode and holds the current constant while varying the voltage on the load.

### 8.3.8 Thermal Sense

Thermal protection prevents damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The TPS204xB-Q1 and TPS205xB-Q1 implement a thermal sensing to monitor the operating junction temperature of the power distribution switch. In an overcurrent or short-circuit condition, the junction temperature rises due to excessive power dissipation. Once the die temperature rises to approximately 140°C due to overcurrent conditions, the internal thermal sense circuitry turns the power switch off, thus preventing the power switch from damage. Hysteresis is built into the thermal sense circuit, and after the device has cooled approximately 10°C, the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed. The $\overline{\text{OCx}}$ open-drain output is asserted (active low) when an overtemperature shutdown or overcurrent occurs.

### 8.3.9 Undervoltage Lockout (UVLO)

A voltage sense circuit monitors the input voltage. When the input voltage is below approximately 2 V, a control signal turns off the power switch.

## 8.4 Device Functional Modes

表 8-1 lists OUT pin state as determined by the $\overline{\text{EN}}$ pin.

**表 8-1. OUT Pin State**

| EN | TPS2041B-Q1 | TPS2042B-Q1 | TPS2051B-Q1 |
|---|---|---|---|
| Low | IN | Open | Open |
| High | Open | IN | IN |

# 9 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

## 9.1 Application Information

### 9.1.1 Universal Serial Bus (USB) Applications

The universal serial bus (USB) interface is a 12-Mbps, or 1.5-Mbps, multiplexed serial bus designed for low-to-medium bandwidth PC peripherals (for example, keyboards, printers, scanners, and mice). The four-wire USB interface is conceived for dynamic attach-detach (hot plug-unplug) of peripherals. Two lines are provided for differential data, and two lines are provided for 5-V power distribution.

USB data is a 3.3-V level signal, but power is distributed at 5 V to allow for voltage drops in cases where power is distributed through more than one hub across long cables. Each function must provide its own regulated 3.3 V from the 5-V input or its own internal power supply.

The USB specification defines the following five classes of devices, each differentiated by power-consumption requirements:

- Hosts and self-powered hubs (SPHs)
- Bus-powered hubs (BPHs)
- Low-power bus-powered functions
- High-power bus-powered functions
- Self-powered functions

Self-powered and bus-powered hubs distribute data and power to downstream functions. The TPS204xB-Q1 and TPS205xB-Q1 can provide power-distribution solutions to many of these classes of devices.

## 9.2 Typical Applications

### 9.2.1 TPS2042B-Q1 Typical Application

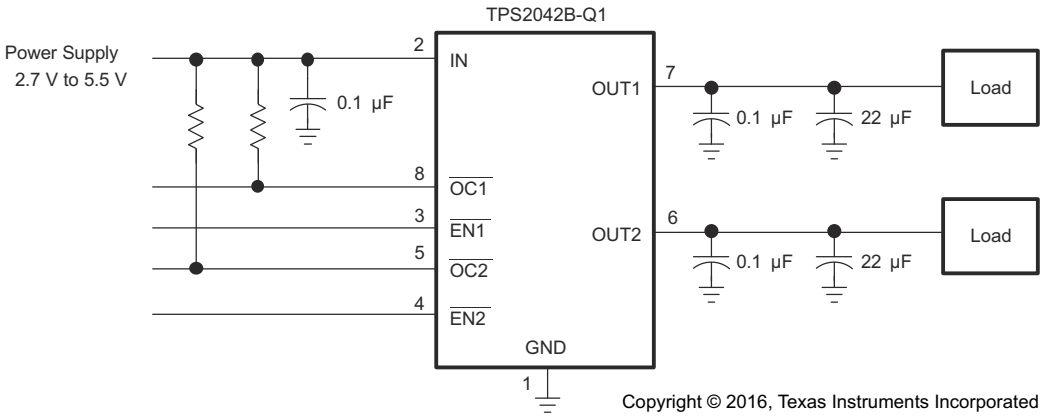



**図 9-1. Typical Application Schematic Using the TPS2042B-Q1**

#### 9.2.1.1 Design Requirements

For this design example, use the parameters listed in 表 9-1 as the input parameters.

**表 9-1. Design Parameters**

| PARAMETER | VALUE |
|---|---|
| Input voltage | 5 V |
| Output1 voltage | 5 V |
| Output2 voltage | 5 V |
| Output1 current | 0.5 A |
| Output2 current | 0.5 A |

#### 9.2.1.2 Detailed Design Procedure

##### 9.2.1.2.1 Overcurrent

A sense FET is employed to check for overcurrent conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before $V_{I(IN)}$ has been applied (see 図 9-7 through 図 9-10). The TPS20xxB-Q1 senses the short and immediately switches into a constant-current output.

In the second condition, a short or an overload occurs while the device is enabled. At the instant the overload occurs, high currents may flow for a short period of time before the current-limit circuit can react. After the current-limit circuit has tripped (reached the overcurrent trip threshold), the device switches into constant-current mode.

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached or until the thermal limit of the device is exceeded (see 図 6-7 through 図 6-8). The TPS20xxB-Q1 is capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its constant-current mode.

##### 9.2.1.2.2 $\overline{OC}$ Response

The $\overline{OCx}$ open-drain output is asserted (active low) when an overcurrent or overtemperature shutdown condition is encountered after a 10-ms deglitch timeout. The output remains asserted until the overcurrent or overtemperature condition is removed. Connecting a heavy capacitive load to an enabled device can cause a momentary overcurrent condition; however, no false reporting on $\overline{OCx}$ occurs due to the 10-ms deglitch circuit. The TPS20xxB-Q1 is designed to eliminate false overcurrent reporting. The internal overcurrent deglitch eliminates the need for external components to remove unwanted pulses. $\overline{OCx}$ is not deglitched when the switch is turned off due to an overtemperature shutdown.

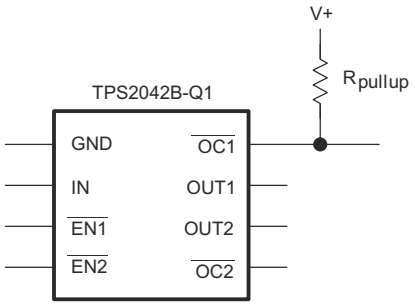





**図 9-2. Typical Circuit for the $\overline{OC}$ Pin (TPS2042B-Q1)**

### 9.2.1.3 Application Curves

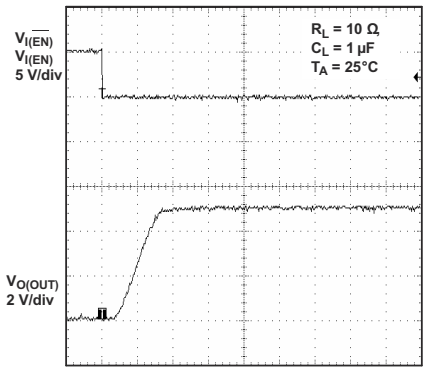



図 9-3. Turnon Delay and Rise Time With 1-µF Load

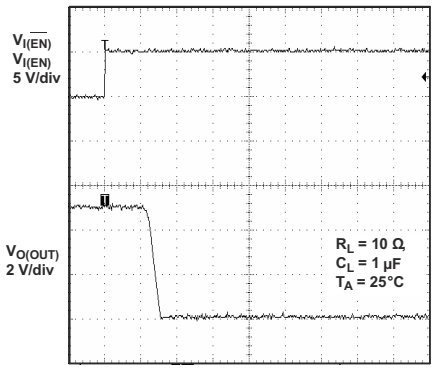



図 9-4. Turnoff Delay and Fall Time With 1-µF Load

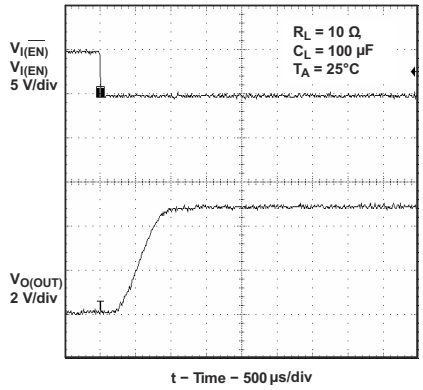



図 9-5. Turnon Delay and Rise Time With 100-µF Load

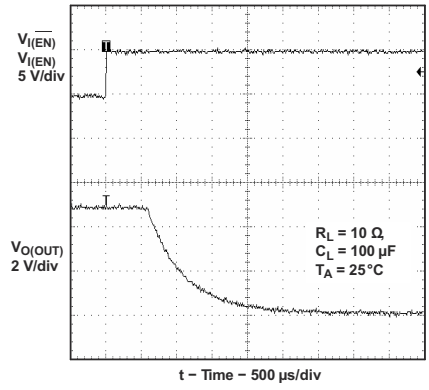



図 9-6. Turnoff Delay and Fall Time With 100-µF Load

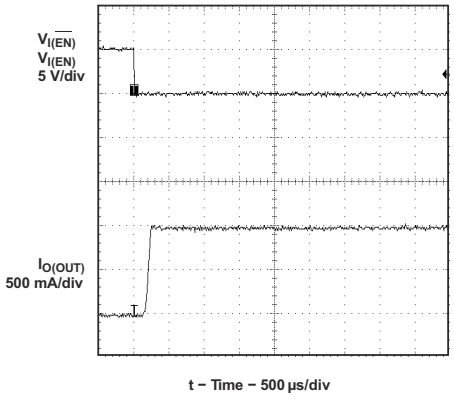



図 9-7. Short-Circuit Current, Device Enabled Into Short

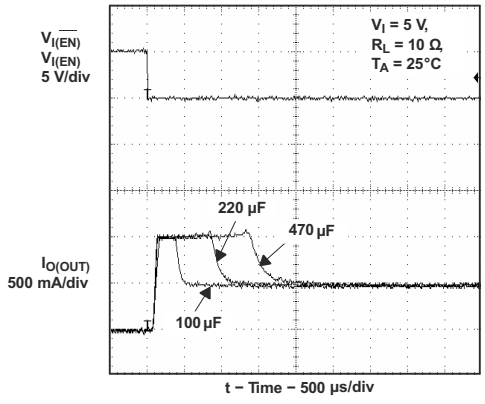



図 9-8. Inrush Current With Different Load Capacitance

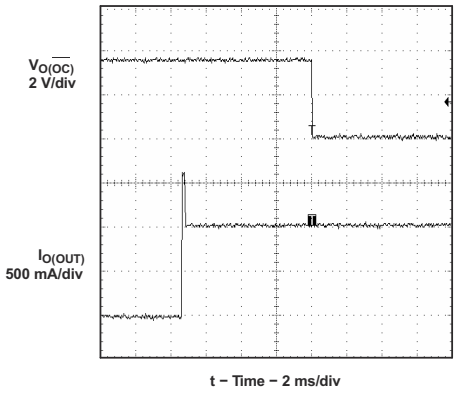



図 9-9. 3-Ω Load Connected to Enabled Device

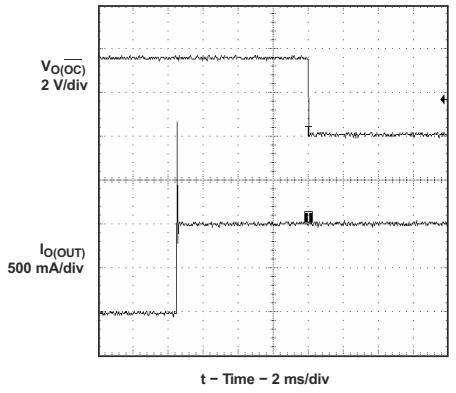



図 9-10. 2-Ω Load Connected to Enabled Device

### 9.2.2 Hosts and Self-Powered Hubs and Bus-Powered Hubs

Hosts and self-powered hubs have a local power supply that powers the embedded functions and the downstream ports (see 図 9-11). This power supply must provide from 5.25 V to 4.75 V to the board side of the downstream connection under full-load and no-load conditions. Hosts and SPHs are required to have current-limit protection and must report overcurrent conditions to the USB controller. Typical SPHs are desktop PCs, monitors, printers, and stand-alone hubs.

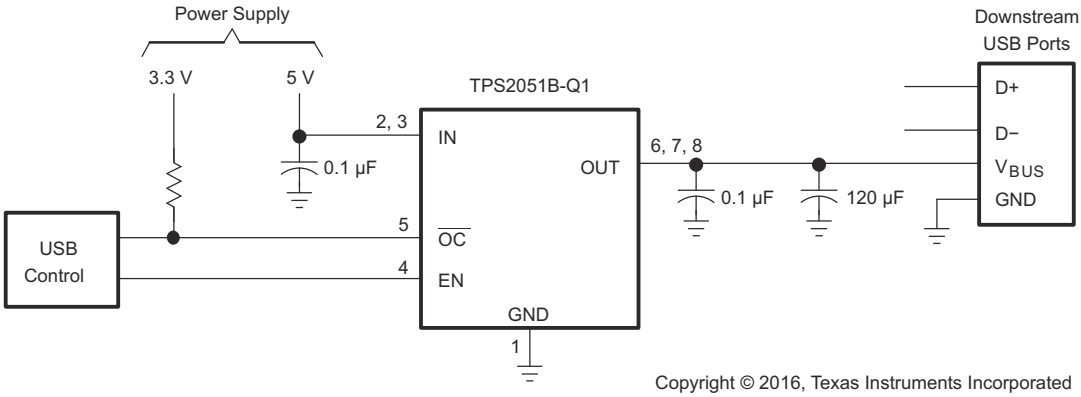



図 9-11. Typical One-Port USB Host or Self-Powered Hub

#### *9.2.2.1 Design Requirements*

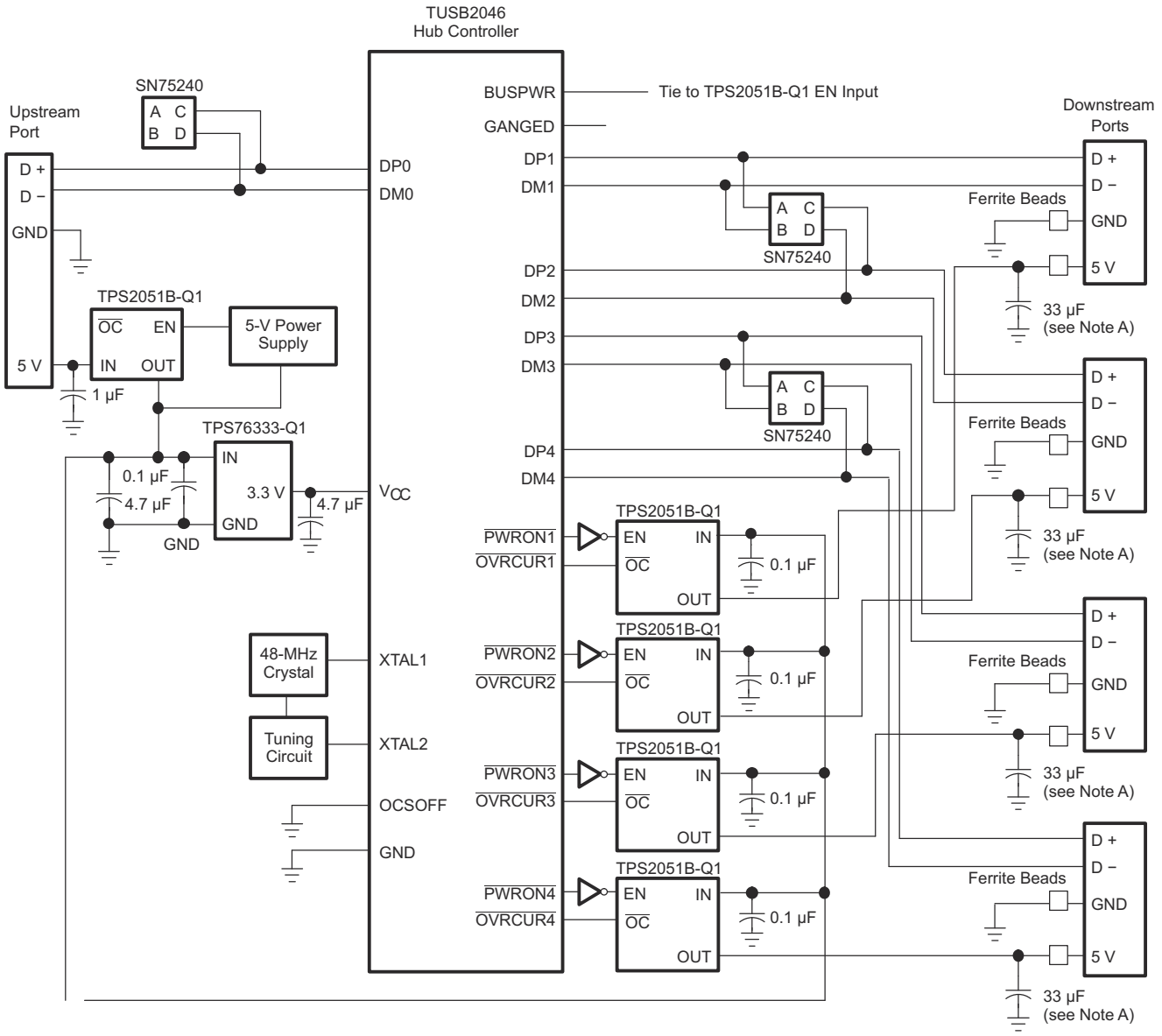
##### 9.2.2.1.1 USB Power-Distribution Requirements

USB can be implemented in several ways, and, regardless of the type of USB device being developed, several power-distribution features must be implemented.

- Hosts and self-powered hubs must:
  - Current-limit downstream ports
  - Report overcurrent conditions on USB $V_{BUS}$
- Bus-powered hubs must:
  - Enable and disable power to downstream ports
  - Power up at < 100 mA
  - Limit inrush current (< 44 Ω and 10 µF)
- Functions must:
  - Limit inrush currents
  - Power up at < 100 mA

The feature set of the TPS204xB-Q1 and TPS205xB-Q1 allows them to meet each of these requirements. The integrated current-limiting and overcurrent reporting is required by hosts and self-powered hubs. The logic-level

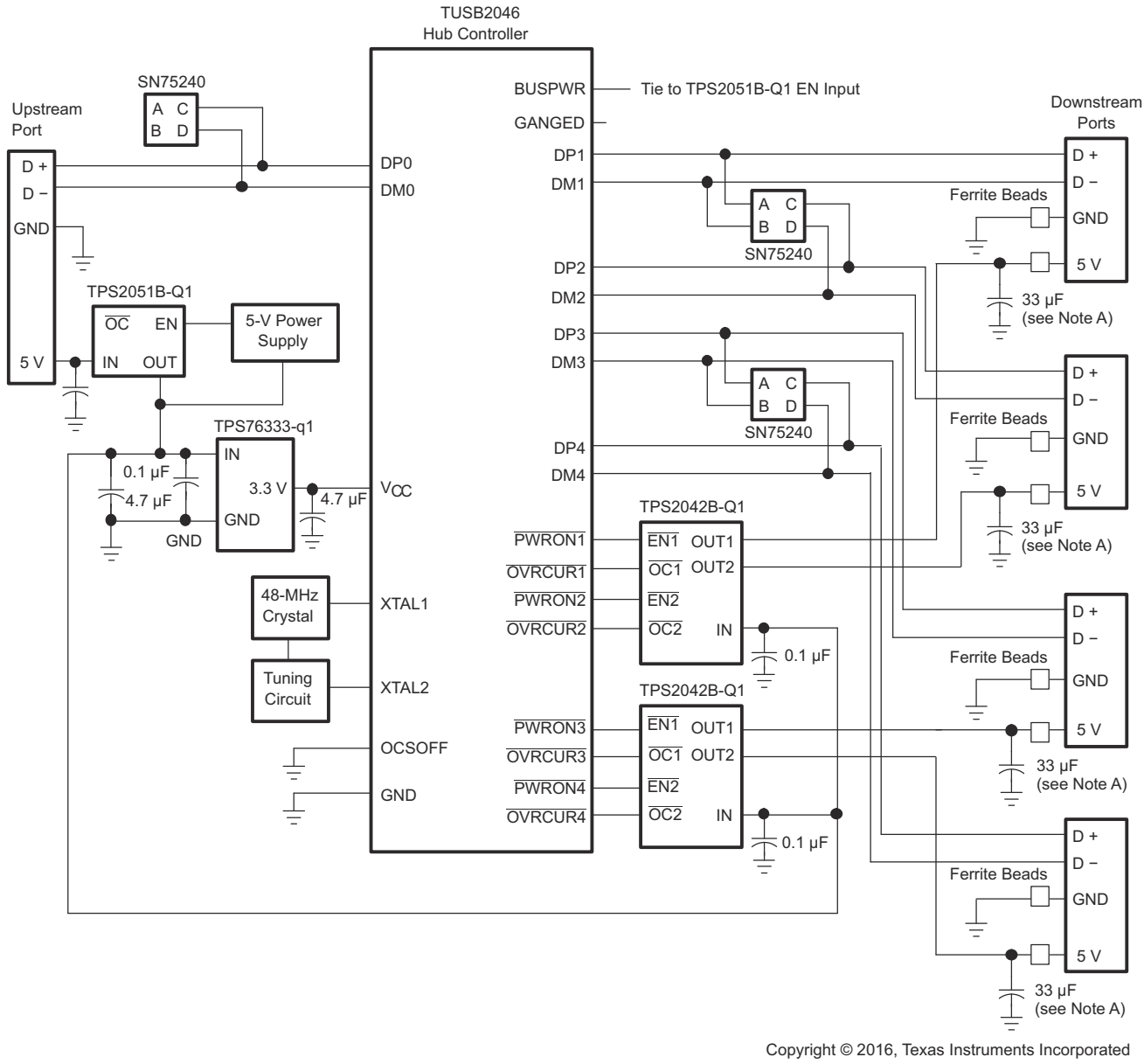
enable and controlled rise times meet the need of both input and output ports on bus-powered hubs, as well as the input ports for bus-powered functions (see 図 9-12 and 図 9-13).






A. USB rev 1.1 requires 120 µF per hub.

**図 9-12. Hybrid Self-Powered or Bus-Powered Hub Implementation (TPS2051B-Q1)**






A. USB rev 1.1 requires 120 µF per hub.

**図 9-13. Hybrid Self-Powered or Bus-Powered Hub Implementation (TPS2042B-Q1)**

### *9.2.2.2 Detailed Design Procedure*

Bus-powered hubs obtain all power from upstream ports and often contain an embedded function. The hubs are required to power up with less than one unit load. The BPH usually has one embedded function, and power is always available to the controller of the hub. If the embedded function and hub require more than 100 mA on power up, the power to the embedded function may need to be kept off until enumeration is completed. This can be accomplished by removing power or by shutting off the clock to the embedded function. Power switching the embedded function is not necessary if the aggregate power draw for the function and controller is less than one unit load. The total current drawn by the bus-powered device is the sum of the current to the controller, the embedded function, and the downstream ports, and it is limited to 500 mA from an upstream port.

#### 9.2.2.2.1 Low-Power Bus-Powered and High-Power Bus-Powered Functions

Both low-power and high-power bus-powered functions obtain all power from upstream ports; low-power functions always draw less than 100 mA; high-power functions must draw less than 100 mA at power up and can draw up to 500 mA after enumeration. If the load of the function is more than the parallel combination of 44 Ω and 10 µF at power up, the device must implement inrush current limiting (see 図 9-14).

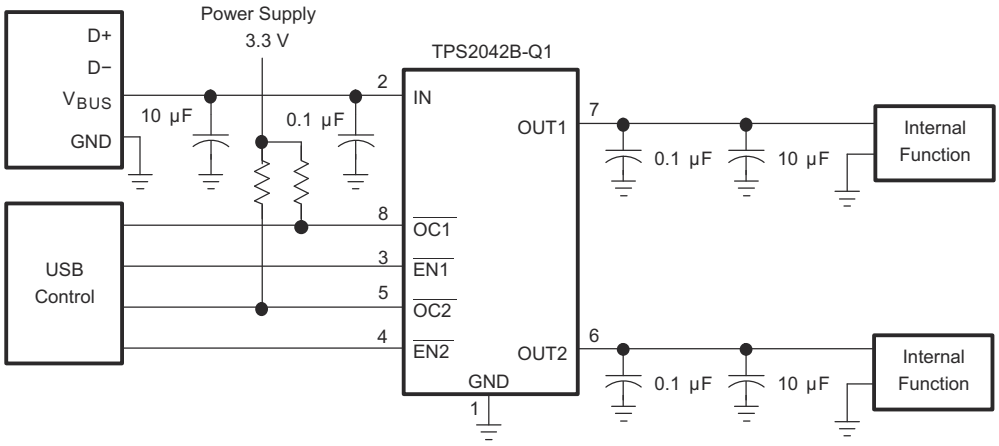





**図 9-14. High-Power Bus-Powered Function (TPS2042B-Q1)**

### 9.2.3 Generic Hot-Plug Applications

In many applications, it may be necessary to remove modules or PC boards while the main unit is still operating. These are considered hot-plug applications. Such implementations require the control of current surges seen by the main power supply and the card being inserted. The most effective way to control these surges is to limit and slowly ramp the current and voltage being applied to the card, similar to the way in which a power supply normally turns on. Due to the controlled rise and fall times of the TPS204xB-Q1 and TPS205xB-Q1, these devices can be used to provide a softer start-up to devices being hot-plugged into a powered system. The UVLO feature of the TPS204xB-Q1 and TPS205xB-Q1 also ensures that the switch is off after the card has been removed, and that the switch is off during the next insertion. The UVLO feature ensures a soft start with a controlled rise time for every insertion of the card or module.

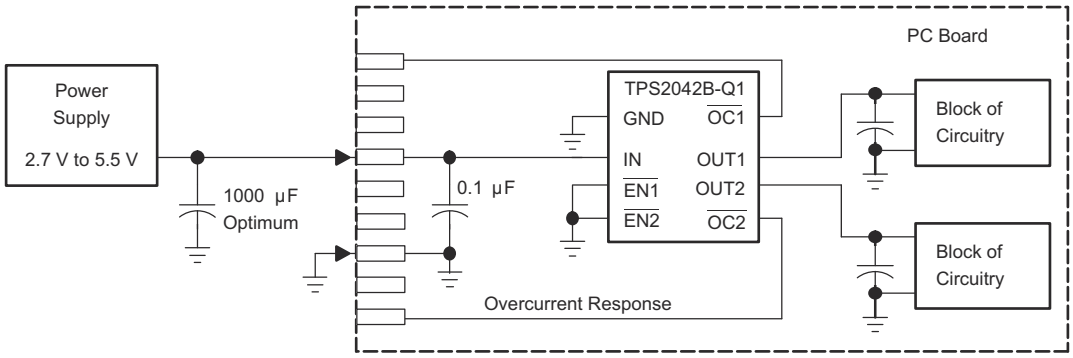





**図 9-15. Example Hot-Plug Implementation (TPS2042B-Q1)**

By placing the TPS204xB-Q1 or TPS205xB-Q1 between the $V_{CC}$ input and the rest of the circuitry, the input power reaches these devices first after insertion. The typical rise time of the switch is approximately 1 ms, providing a slow voltage ramp at the output of the device. This implementation controls system surge currents and provides a hot-plugging mechanism for any device.

#### 9.2.3.1 Design Requirements

For this design example, use the parameters listed in 表 9-2 as the input parameters.

**表 9-2. Design Parameters**

| PARAMETER | VALUE |
|---|---|
| Input voltage | 5 V |
| Output1 voltage | 5 V |
| Output2 voltage | 5 V |
| Output1 current | 0.5 A |
| Output2 current | 0.5 A |

#### 9.2.3.2 Detailed Design Procedure

To begin the design process a few parameters must be decided upon. The designer must know the following:

- Normal input operation voltage
- Current limit

Input and output capacitance improves the performance of the device; the actual capacitance must be optimized for the particular application. For all applications, TI recommends a 0.1 µF or greater ceramic bypass capacitor between IN and GND, as close to the device as possible for local noise decoupling. This precaution reduces ringing on the input due to power-supply transients. Additional input capacitance may be required on the input to reduce voltage undershoot from exceeding the UVLO of other load share one power rail with TPS2042B-Q1 device or overshoot from exceeding the absolute-maximum voltage of the device during heavy transient conditions. This is especially important during bench testing when long, inductive cables are used to connect the evaluation board to the bench power supply. Output capacitance is not required, but TI recommends placing a high-value electrolytic capacitor on the output pin when large transient currents are expected on the output to reduce the undershoot, which is caused by the inductance of the output power bus just after a short has occurred and the TPS2042B-Q1 device has abruptly reduced OUT current. Energy stored in the inductance drives the OUT voltage down and potentially negative as it discharges.

## 10 Power Supply Recommendations

TI recommends a 0.01-µF to 0.1-µF ceramic bypass capacitor close to the device between IN and GND. TI recommends placing a high-value electrolytic capacitor on the output pins when the output load is heavy. This precaution reduces power-supply transients that may cause ringing on the input. Additionally, bypassing the output with a 0.01-µF to 0.1-µF ceramic capacitor improves the immunity of the device to short-circuit transients. See 図 9-1.

# 11 Layout

## 11.1 Layout Guidelines

- Place the 100-nF bypass capacitor near the IN and GND pins and make the connections using a low-inductance trace.
- TI recommends placing a high-value electrolytic capacitor and a 100-nF bypass capacitor on the output pin when large transient currents are expected on the output.

## 11.2 Layout Example

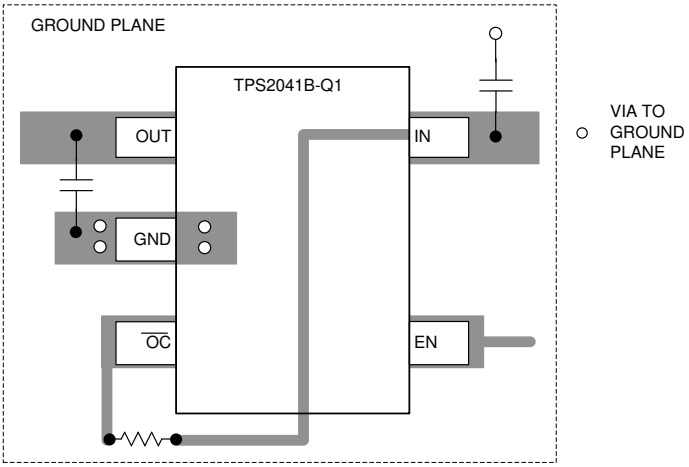



**図 11-1. Layout Recommendation**

## 11.3 Thermal Considerations

The low on-resistance on the N-channel MOSFET allows the small surface-mount packages to pass large currents. The thermal resistances of these packages are high compared to those of power packages; it is good design practice to check power dissipation and junction temperature. Begin by determining the $r_{DS(ON)}$ of the N-channel MOSFET relative to the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(ON)}$ from 図 6-9. Using this value, the power dissipation per switch can be calculated by 式 1:

$$P_D = r_{DS(ON)} \times I^2 \quad (1)$$

Multiply this number by the number of switches being used. This step renders the total power dissipation from the N-channel MOSFETs.

Finally, calculate the junction temperature with 式 2:

$$T_J = P_D \times R_{\theta JA} + T_A \quad (2)$$

where

- $T_A$ = Ambient temperature °C
- $R_{\theta JA}$ = Thermal resistance
- $P_D$ = Total power dissipation based on number of switches being used.

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation, using the calculated value as the new estimate. Two or three iterations are generally sufficient to get a reasonable answer.

# 12 Device and Documentation Support

## 12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**表 12-1. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| TPS2041B-Q1 | Click here | Click here | Click here | Click here | Click here |
| TPS2042B-Q1 | Click here | Click here | Click here | Click here | Click here |
| TPS2051B-Q1 | Click here | Click here | Click here | Click here | Click here |

## 12.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。*「更新の通知を受け取る」をクリック*して登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

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## 12.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい ESD 対策をとらないと、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

## 12.6 用語集

TI 用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS2041BQDBVRQ1 | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PLIQ |
| TPS2041BQDBVRQ1.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PLIQ |
| TPS2041BQDBVRQ1.B | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PLIQ |
| TPS2042BQDRQ1 | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2042B |
| TPS2042BQDRQ1.A | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2042B |
| TPS2051BQDRQ1 | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2051BQ |
| TPS2051BQDRQ1.A | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2051BQ |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**OTHER QUALIFIED VERSIONS OF TPS2041B-Q1, TPS2042B-Q1, TPS2051B-Q1 :**

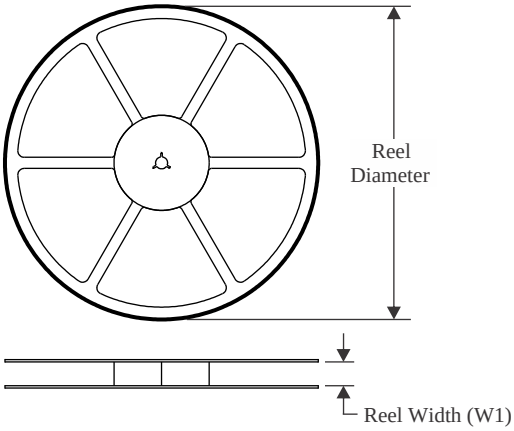
- Catalog : TPS2041B, TPS2042B, TPS2051B
- Enhanced Product : TPS2041B-EP

NOTE: Qualified Version Definitions:

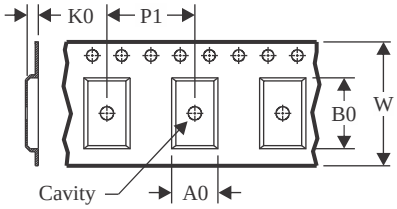
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

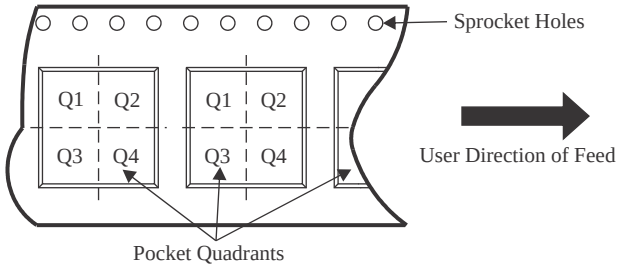



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

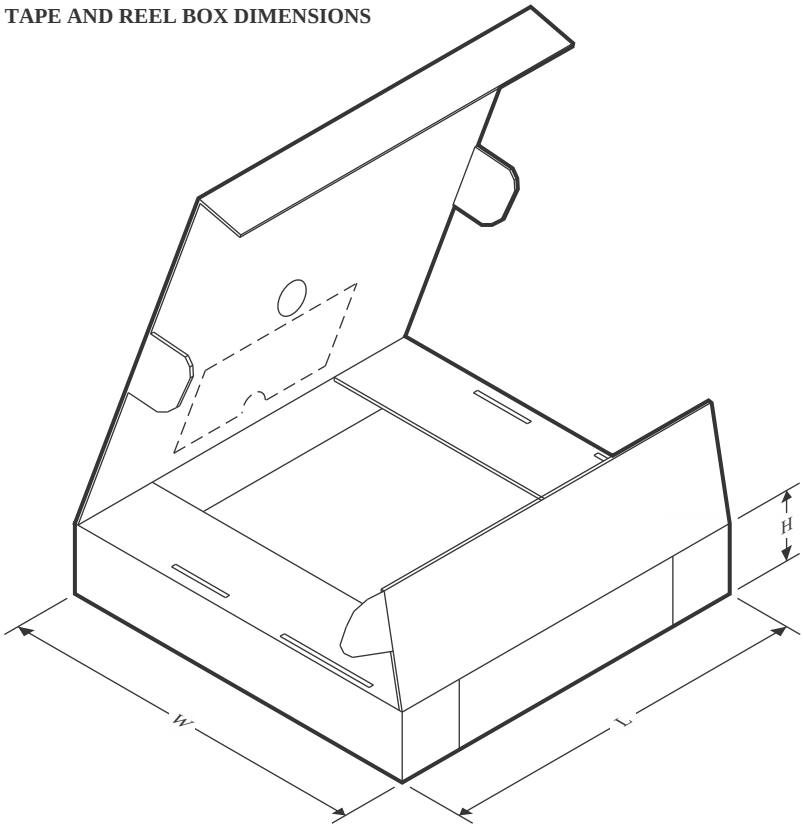
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS2041BQDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS2042BQDRQ1 | SOIC | D | 8 | 2500 | 330.0 | 12.5 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TPS2051BQDRQ1 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

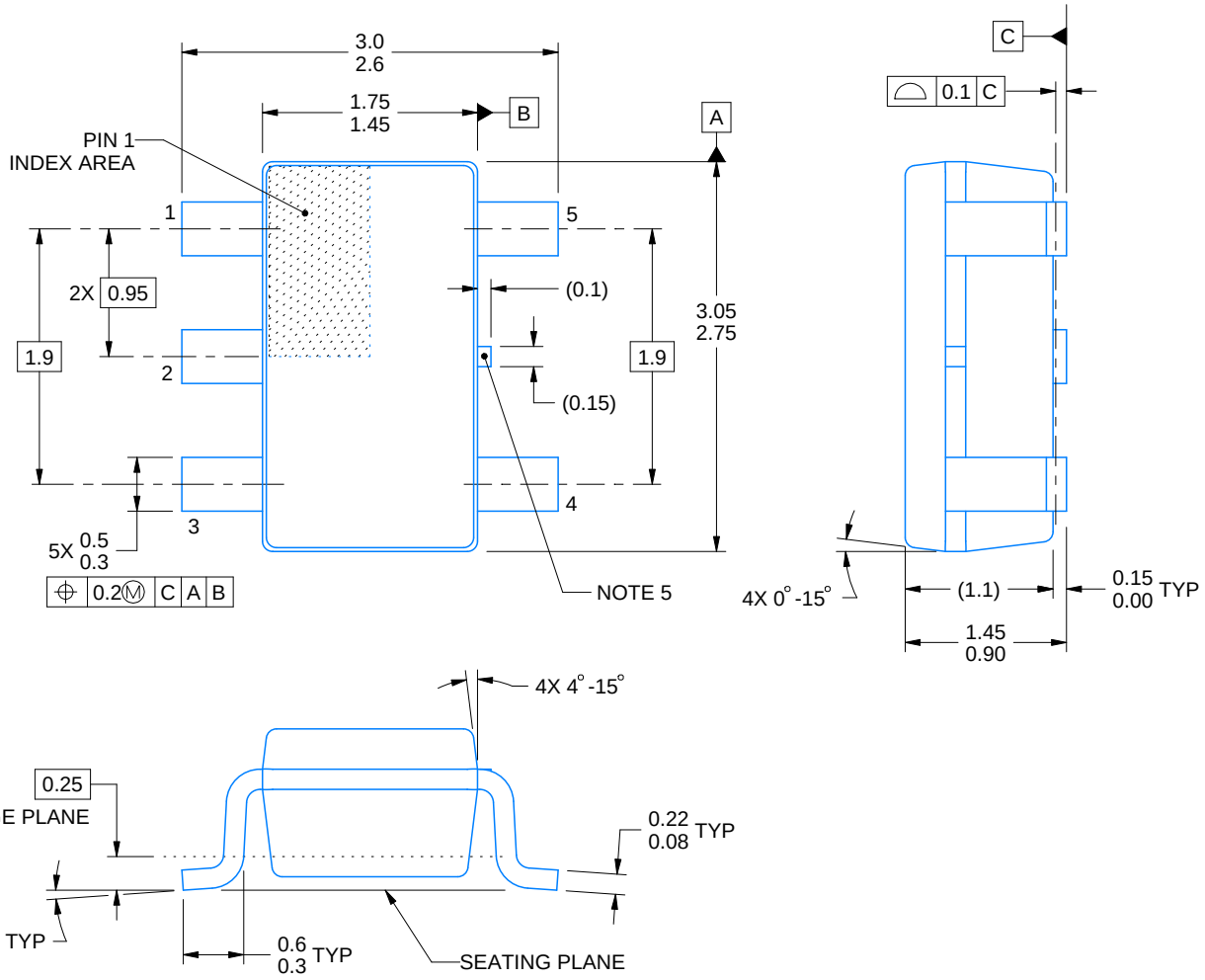
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS2041BQDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 200.0 | 183.0 | 25.0 |
| TPS2042BQDRQ1 | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TPS2051BQDRQ1 | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |

# PACKAGE OUTLINE

## DBV0005A

## SOT-23 - 1.45 mm max height

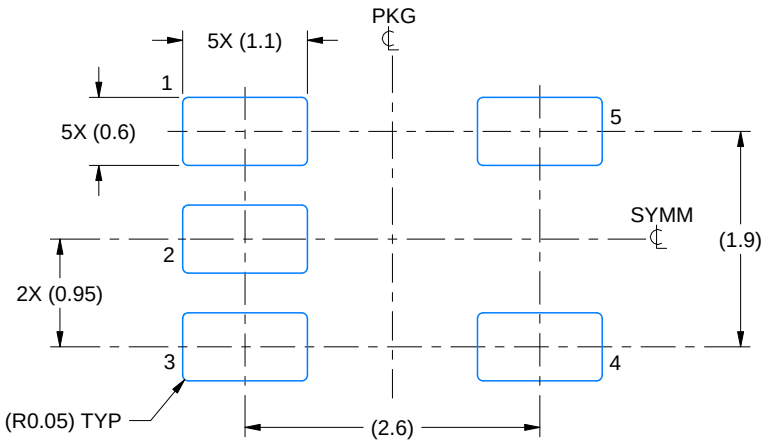
SMALL OUTLINE TRANSISTOR



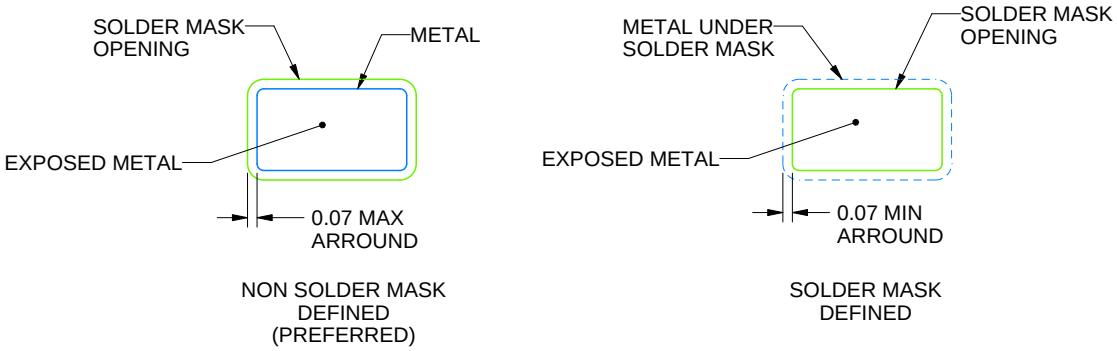

4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

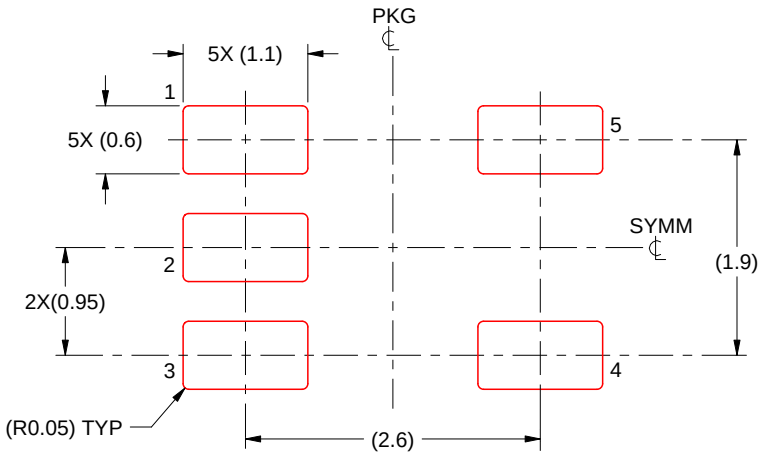



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

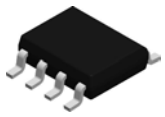



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

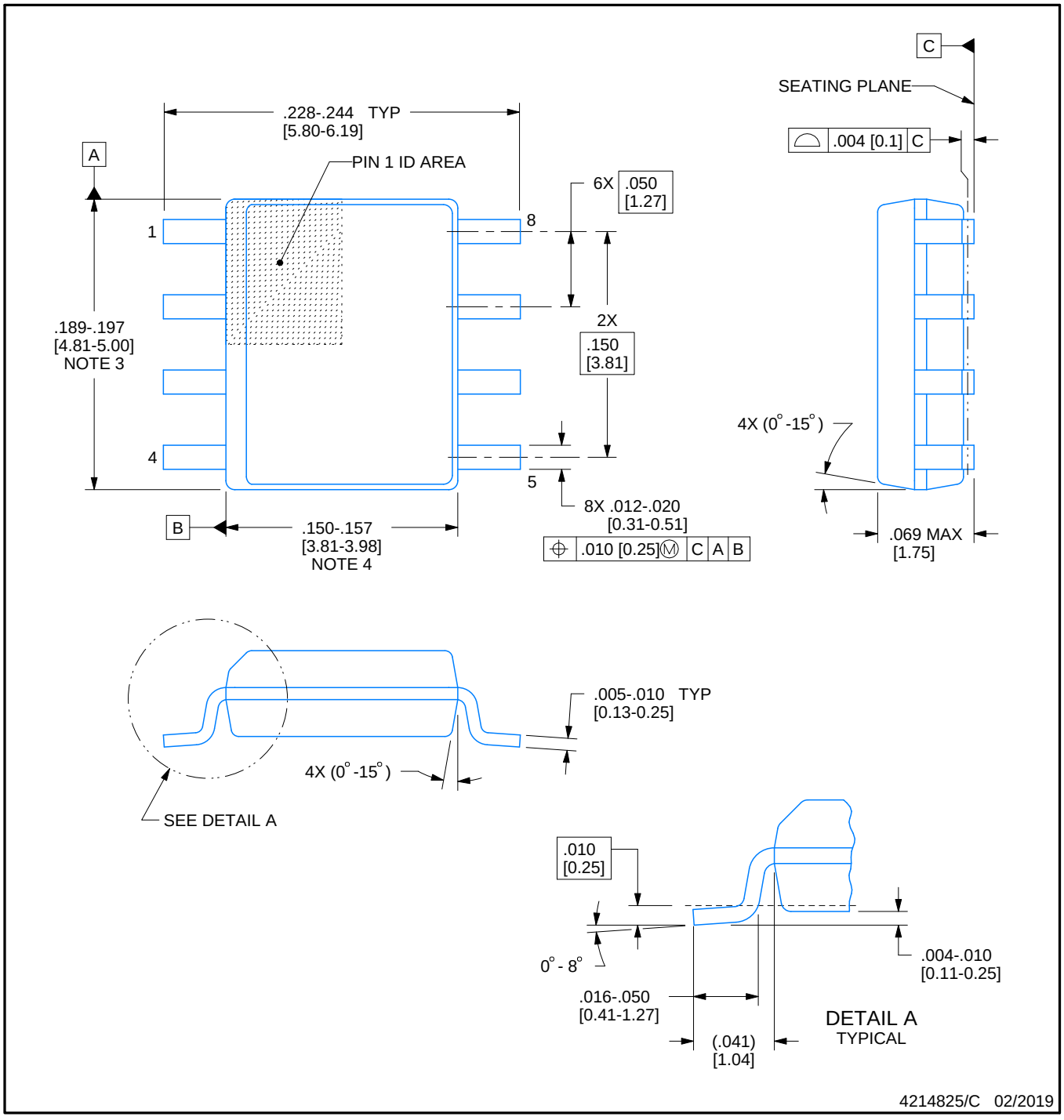


# PACKAGE OUTLINE

## D0008A

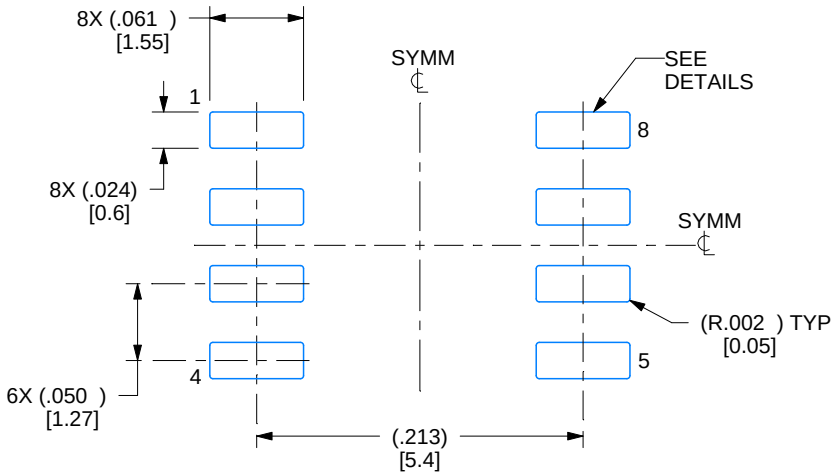
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

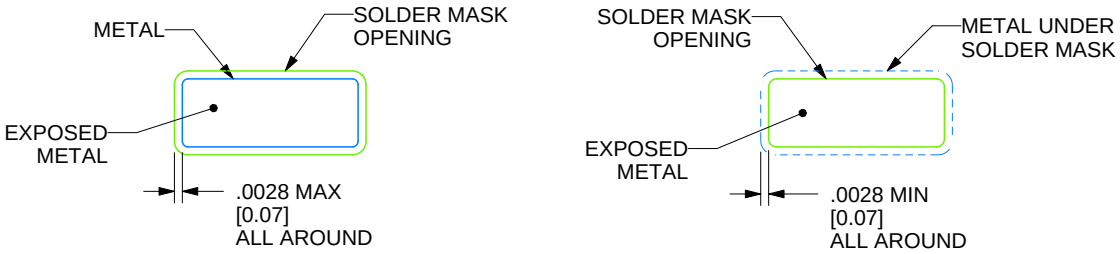



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

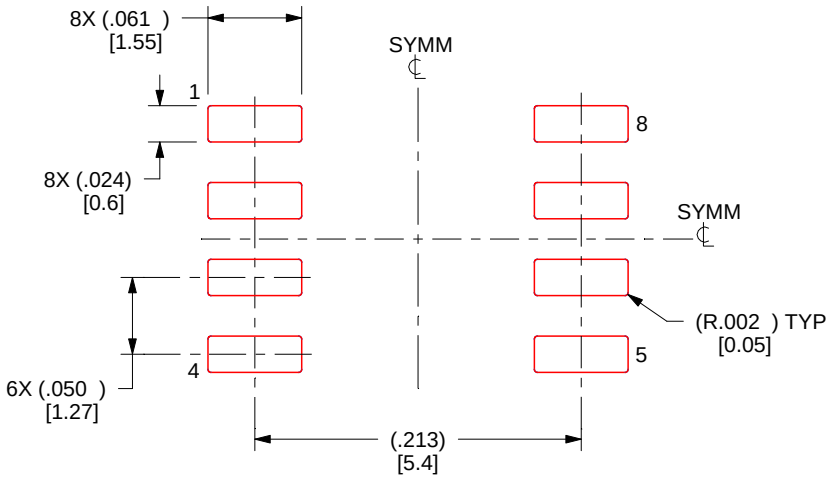
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0008A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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