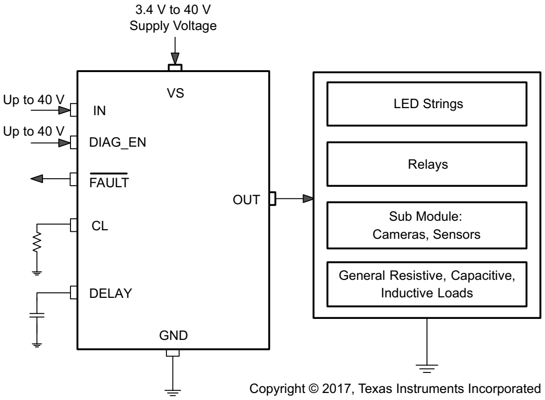
参考資料

TPS1H000-Q1 車載 40V、1Ω、シングル チャネル スマート ハイサイド スイッチ

1 特長

- 車載アプリケーション認定済み
- 以下の結果で AEC-Q100 認定済み：
  - デバイス温度グレード 1：動作時周囲温度範囲 -40℃～125℃
  - デバイス HBM ESD 分類レベル H2
  - デバイス CDM ESD 分類レベル C4B
- シングル チャネル 1000mΩ スマート ハイサイド スイッチ
- 広い動作電圧範囲：3.4V～40V
- 小さいスタンバイ電流：<500nA
- 外付け抵抗で電流制限を調整可能
  - 150mA 以上のとき±15%
  - 300mA 以上のとき±10%
- 電流制限後の動作を設定可能
  - ホールド モード
  - ラッチオフ モード、遅延時間を設定可能
  - 自動再試行モード
- MCU なしのスタンドアロン動作をサポート
- 保護機能：
  - GND への短絡および過負荷
  - サーマル シャットダウンおよびサーマル スイング
  - 誘導性負荷の負電圧クランプ
  - GND 消失およびバッテリ消失
- 診断機能：
  - 過負荷および GND への短絡の検出
  - オンまたはオフ状態での開放負荷およびバッテリへの短絡の検出
  - サーマル シャットダウンおよびサーマル スイング



代表的なブロック図

2 アプリケーション

- シングル チャネル LED ドライバ
- シングル チャネル ハイサイド リレー ドライバ
- 車体 / 照明
- 先進運転支援システム (ADAS) センサ
- 一般的な抵抗性、誘導性、容量性負荷

3 概要

TPS1H000-Q1 デバイスは、完全に保護されたシングル チャネル ハイサイド パワー スイッチで、1000mΩ の NMOS パワー FET を内蔵しています。

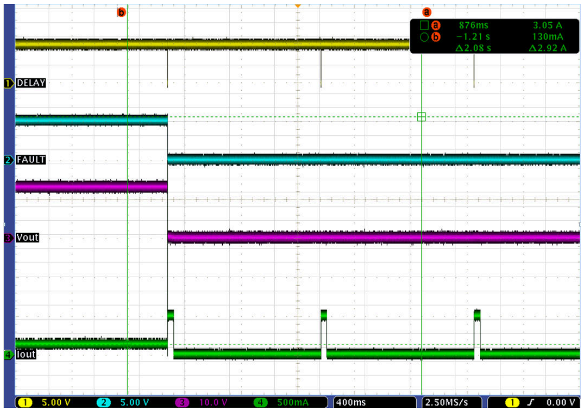
電流制限を調整可能なため、突入電流や過負荷電流を制限し、システムの信頼性を向上できます。電流制限の精度が高いので、過負荷保護が強化され、前段の電源設計が簡単になります。電流制限以外の特徴も可変であるため、機能、コスト、熱放散について柔軟な設計が可能です。

このデバイスは完全な診断機能をサポートし、状態をデジタル出力します。開放負荷検出は、オンとオフの両方の状態で利用可能です。このデバイスは、MCU ありでも、なしでも動作できます。スタンドアロン モードにより、絶縁システムでもデバイスを使用できます。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
TPS1H000-Q1	DGN (HVSSOP、8)	3.00mm × 4.90mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値で、該当する場合はピンも含まれます。



自動再試行モードでの電流制限保護

English Data Sheet: SLVSDO6

Table of Contents

4 Pin Configuration and Functions

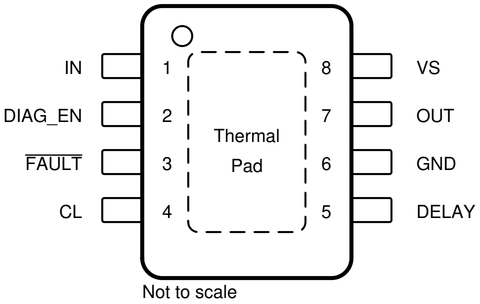


図 4-1. DGN PowerPAD™ Package, 8-Pin HVSSOP With Exposed Thermal Pad (Top View)

表 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CL	4	O	Adjustable current limit. Connect to device GND if external current limit is not used.
DELAY	5	I/O	Function configuration when in current limit; internal pullup.
DIAG_EN	2	I	Enable the diagnostic function.
FAULT	3	O	Open-drain diagnostic status output. Leave floating if not used.
GND	6	—	Ground pin.
IN	1	I	Input control for output activation; internal pulldown.
OUT	7	O	Output, source of the high-side switch, connected to the load.
VS	8	I	Power supply, drain for the high-side switch.
Thermal pad	—	—	Thermal pad. Connect to device GND or leave floating.

5 Specifications

5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
Supply voltage VS pin	t < 400 ms	—	42	V
Reverse polarity voltage (3)	t < 1 minute	–36	—	V
Current on GND	t < 2 minutes	–100	250	mA
Voltage on IN and DIAG_EN pins		–0.3	42	V
Current on IN and DIAG_EN pins		–10	—	mA
Voltage on DELAY pin		–0.3	7	V
Current on DELAY pin		–60	—	mA
Voltage on $\overline{\text{FAULT}}$ pin		–0.3	7	V
Current on $\overline{\text{FAULT}}$ pin		–30	10	mA
Voltage on CL pin		–0.3	7	V
Current on CL pin		—	6	mA
Voltage on OUT pin		—	42	V
Inductive load switch-off energy dissipation single pulse(4)		—	40	mJ
Operating junction temperature		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to ground.
(3) Reverse polarity condition: V_{IN} = 0 V, reverse current < $I_{R(2)}$, GND pin 1-kΩ resistor in parallel with diode.
(4) Test condition: V_{VS} = 13.5 V, L = 300 mH, T_J = 150°C. FR4 2s2p board, 2 × 70-µm Cu, 2 × 35-µm Cu. 600 mm^2 thermal pad copper area.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	All pins except VS, OUT, and GND	±2000	V
			Pins VS, OUT, and GND	±3000	
		Charged-device model (CDM), per AEC Q100-011		±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Operating voltage	4		40	V
	Voltage on IN and DIAG_EN pins	0		40	V
	Voltage on $\overline{\text{FAULT}}$ pin	0		5	V
$I_{o,nom}$	Nominal dc load current	0		1	A
T_J	Operating junction temperature	–40		150	°C

5.4 Thermal Information

THERMAL METRIC[1]		TPS1H000-Q1 DGN (HVSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	21.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	21.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.1	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.

5.5 Electrical Characteristics

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATING VOLTAGE						
$V_{VS(nom)}$	Nominal operating voltage		4		40	V
$V_{VS(uvr)}$	Undervoltage restart	V_{VS} rising	3.5	3.7	4	V
$V_{VS(uvf)}$	Undervoltage shutdown	V_{VS} falling	3	3.2	3.4	V
$V_{(uv,hys)}$	Undervoltage shutdown, hysteresis			0.5		V
OPERATING CURRENT						
$I_{(op)}$	Nominal operating current	V_{VS} = 13.5 V, V_{IN} = 5 V, V_{DIAG_EN} = 0 V, I_{OUT} = 0.1 A, I_{CL} = 0.5 A.			5	mA
$I_{(off)}$	Standby current	V_{VS} = 13.5 V, V_{IN} = V_{DIAG_EN} = V_{CL} = V_{OUT} = 0 V, T_J = 25 °C			0.5	µA
		V_{VS} = 13.5 V, V_{IN} = V_{DIAG_EN} = V_{CL} = V_{OUT} = 0 V, T_J = 125 °C			3	
$I_{(off,diag)}$	Standby current with diagnostics enabled	V_{VS} = 13.5 V, V_{IN} = 0 V, V_{DIAG_EN} = 5 V			3	mA
$t_{(off,deg)}$	Standby-mode deglitch time[1]	IN from high to low, if deglitch time≥ $t_{(off,deg)}$, the device enters into standby mode.		12.5		ms
$I_{lkg(out)}$	Output leakage current in off-state	V_{VS} = 13.5 V, V_{IN} = V_{DIAG_EN} = V_{OUT} = 0 V			3	µA
POWER STAGE						
$r_{DS(on)}$	On-state resistance	V_{VS} ≥ 3.5 V, T_J = 25°C		1000		mΩ
		V_{VS} ≥ 3.5 V, T_J = 150°C			2000	
$I_{CL(int)}$	Internal current limit	CL pin connected to GND	1		1.8	A
$I_{CL(TSD)}$	Current-limit value percentage during thermal shutdown			60%		
$V_{DS(clamp)}$	Drain−to−source voltage internally clamped		45		65	V
OUTPUT DIODE CHARACTERISTICS						
V_F	Drain−to−source diode voltage	IN = 0, I_{OUT} = −0.15 A	0.3	0.7	1	V
$I_{R(1)}$	Continuous reverse current from source to drain during a short-to-battery condition[1]	t < 60 s, V_{IN}= 0 V, T_J = 25°C.			1	A
$I_{R(2)}$	Continuous reverse current from source to drain during a reverse-polarity condition[1]	t < 60 s, V_{IN}= 0 V, T_J = 25°C. GND pin 1-kΩ resistor in parallel with diode.			1	A

5.5 Electrical Characteristics (続き)

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC INPUT (IN, DIAG_EN)						
V_{IH}	Logic high-level voltage		2			V
V_{IL}	Logic low-level voltage				0.8	V
$R_{pd,in}$	Logic-pin pulldown resistor	IN. V_{IN} = 5 V	150		400	kΩ
		DIAG_EN. $V_{VS} = V_{DIAG\_EN}$ = 5 V	350		850	
DIAGNOSTICS						
$I_{lkg(loss,GND)}$	Loss of ground output leakage current				100	µA
$t_{d(ol,on)}$	Open-load deglitch time in on-state	V_{IN} = 5 V, V_{DIAG_EN} = 5 V, when $I_{OUT} < I_{(ol,on)}$, duration longer than $t_{d(ol,on)}$, open load is detected.	200	300	450	µs
$I_{(ol,on)}$	Open-load detection threshold in on-state	V_{IN} = 5 V, V_{DIAG_EN} = 5 V, when $I_{OUT} < I_{(ol,on)}$, duration longer than $t_{d(ol,on)}$, open load is detected.	1	5	8	mA
$V_{(ol,off)}$	Open-load detection threshold in off-state	V_{IN} = 0 V, V_{DIAG_EN} = 5 V, when $V_{VS} – V_{OUT} < V_{(ol,off)}$, duration longer than $t_{d(ol,off)}$, open load is detected.	1.4		2.6	V
$t_{d(ol,off)}$	Open-load deglitch time in off-state	V_{IN} = 0 V, V_{DIAG_EN} = 5 V, when $V_{VS} – V_{OUT} < V_{(ol,off)}$, duration longer than $t_{d(ol,off)}$, open load is detected.	200	300	450	µs
$I_{(ol,off)}$	Off-state output sink current	V_{IN} = 0 V, V_{DIAG_EN} = 5 V, $V_{VS} = V_{OUT}$ = 13.5 V	–70			µA
$V_{\overline{FAULT}}$	$\overline{\text{FAULT}}$ low output voltage	$I_{\overline{FAULT}}$ = 2 mA			0.2	V
$t_{\overline{FAULT}}$	$\overline{\text{FAULT}}$ signal holding time(1)			8.5		ms
$T_{(SD)}$	Thermal shutdown threshold(1)			175		°C
$T_{(SD,rst)}$	Thermal shutdown status reset(1)			155		°C
$T_{(sw)}$	Thermal swing shutdown threshold(1)			60		°C
$T_{(hys)}$	Hysterisis for resetting the thermal shutdown and swing(1)			10		°C
CURRENT LIMIT AND DELAY CONFIGURATION						
$K_{(CL)}$	Current-limit current ratio(1)			600		
$V_{CL(th)}$	Current-limit internal threshold voltage(1)			0.8		V
$dK_{(CL)}/K_{(CL)}$	External current limit accuracy(2) $(I_{OUT} – I_{CL} × K_{(CL)}) × 100 / (I_{CL} × K_{(CL)})$	I_{limit} ≥ 0.05 A, $V_{VS} – V_{OUT}$ ≥ 2.5V	–20%		20%	
		I_{limit} ≥ 0.15 A , $V_{VS} – V_{OUT}$ ≥ 2.5V	–15%		15%	
		I_{limit} ≥ 0.3 A, I_{limit} < 1 A, $V_{VS} – V_{OUT}$ ≥ 2.5V	–10%		10%	
$I_{dl(chg)}$	Delay pin charging current in latch-off mode(1)			4.5		µA
$V_{dl(th)}$	Pulling up threshold in auto-retry mode		2.7			V
$V_{dl(ref)}$	Internal reference voltage in latch-off mode			1.45		V
t_{dl1}	Internal fixed delay time(1)		300	400	500	µs
t_{dl2}	Adjustable delay time by external capacitor on DELAY pin(1)	Connect with 3.3 uF capacitor as the maximum value.			1000	ms

5.5 Electrical Characteristics (続き)

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{CL(deg)}$	Deglitch time when current limit (1)	IN low to high, V_{DIAG_EN} = 5 V, the deglitch time from IN rising edge to FAULT reporting out.	300		500	µs
		IN keeps high, V_{DIAG_EN} = 5 V, the deglitch time from CL start-point to FAULT reporting out.	80		180	
$t_{hic(on)}$	On-time when in auto-retry mode(1)		35	40	45	ms
$t_{hic(off)}$	Off-time when in auto-retry mode(1)		0.8	1	1.2	s

(1) Value specified by design, not subject to production test
(2) External current limit accuracy is only applicable to overload conditions greater than 1.5 x the current limit setting

5.6 Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{d(on)}$	Turnon delay time, IN rising edge to 10% of V_{OUT}	V_{VS} = 13.5 V, V_{DIAG_EN} = 5 V, I_{OUT} = 0.1 A	20	50	90	µs
$t_{d(off)}$	Turnoff delay time, IN falling edge to 90% of V_{OUT}	V_{VS} = 13.5 V, V_{DIAG_EN} = 5 V, I_{OUT} = 0.1 A	20	50	90	µs
$dV/dt_{(on)}$	Slew rate on, V_{OUT} from 10% to 90%	V_{VS} = 13.5 V, V_{DIAG_EN} = 5 V, I_{OUT} = 0.1 A	0.1		0.6	V/µs
$dV/dt_{(off)}$	Slew rate off, $V_{OUT}$from 90% to 10%	V_{VS} = 13.5 V, V_{DIAG_EN} = 5 V, I_{OUT} = 0.1 A	0.3		0.9	V/µs

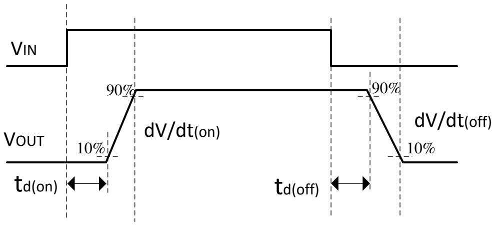


図 5-1. Output Delay Characteristics

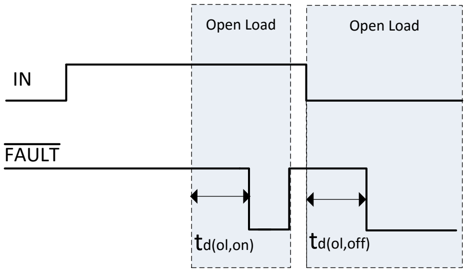


図 5-2. Open-Load Blanking-Time Characteristic

5.7 Typical Characteristics

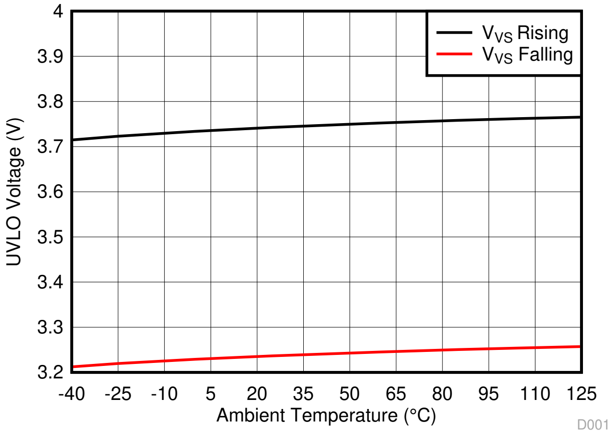


図 5-3. UVLO Voltage Threshold

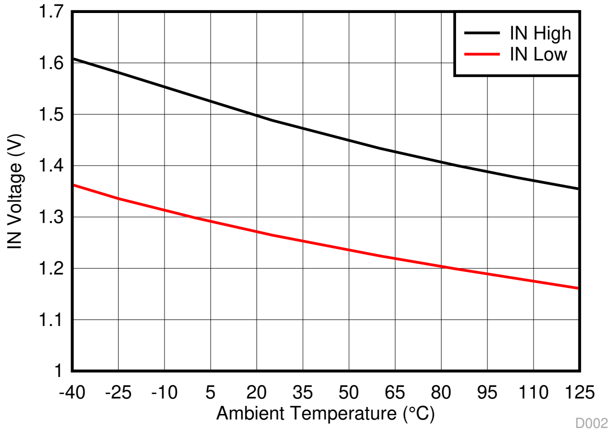


図 5-4. IN Voltage Threshold

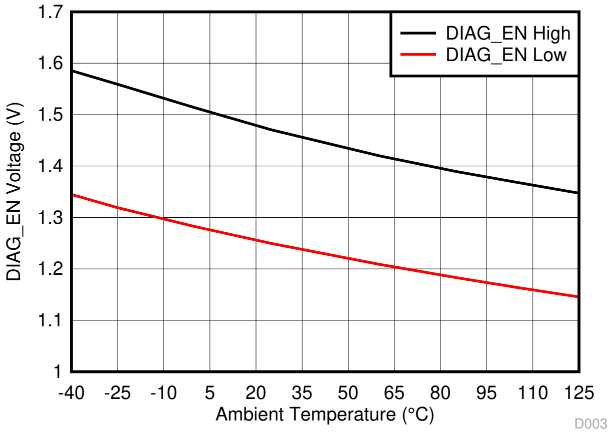


図 5-5. DIAG_EN Voltage Threshold

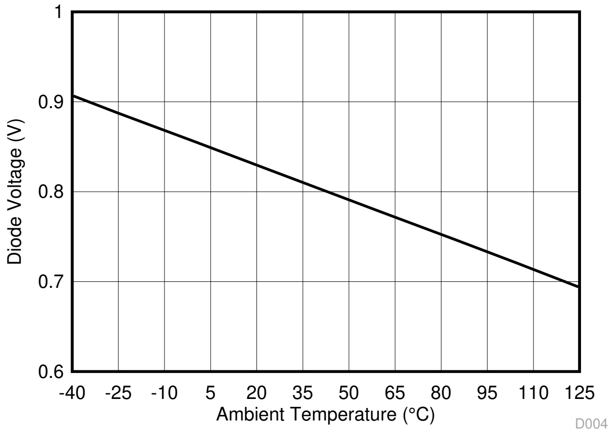


図 5-6. Body-Diode Forward Voltage

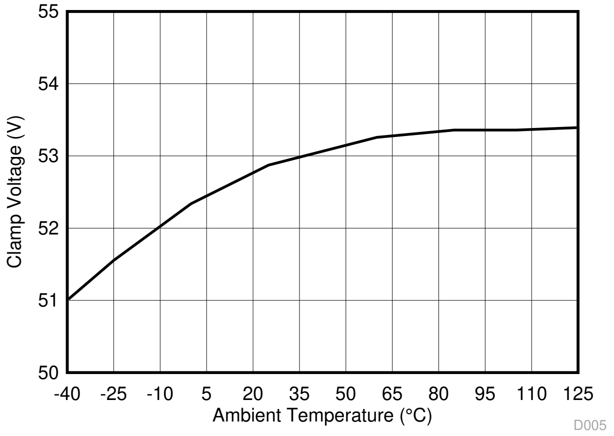


図 5-7. Drain-to-Source Clamp Voltage

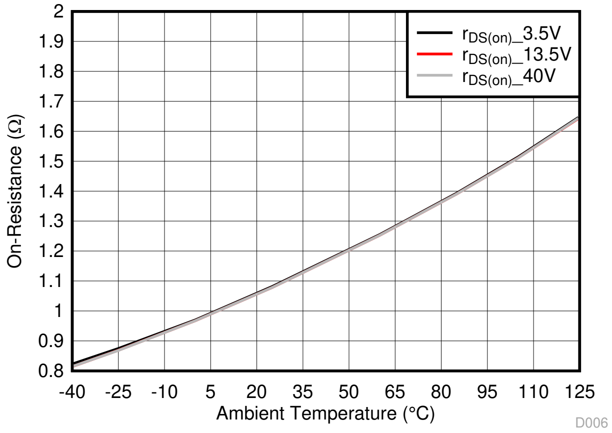
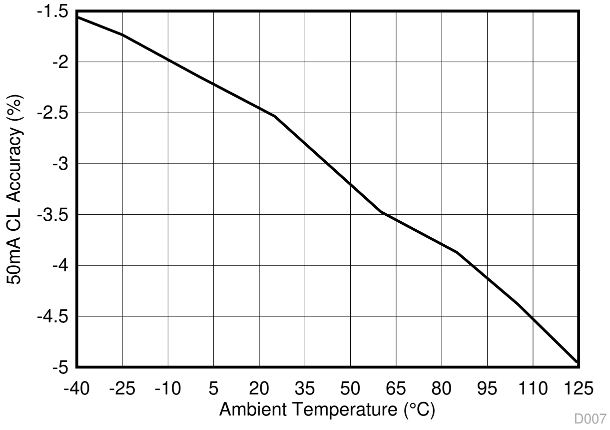


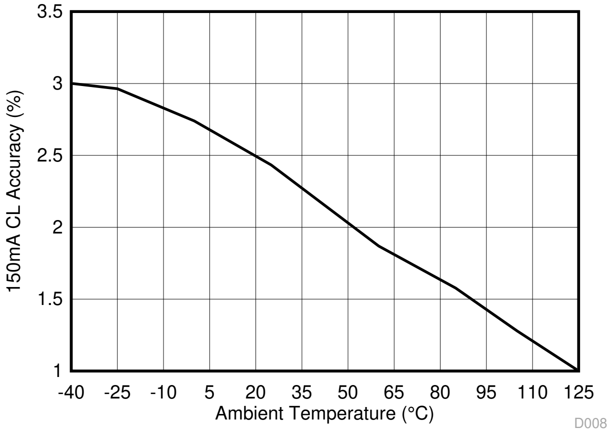
図 5-8. FET On-Resistance

5.7 Typical Characteristics (continued)



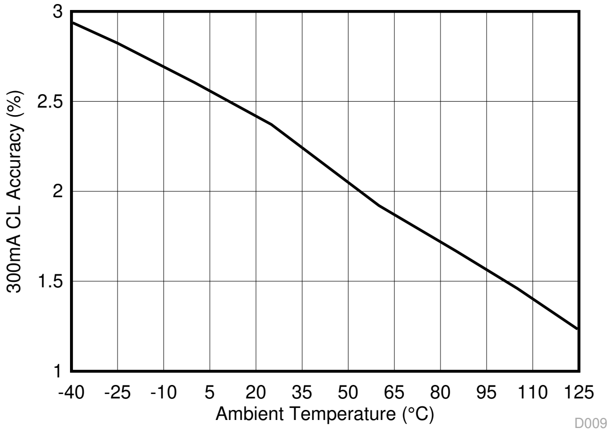
I_{OUT} = 50 mA

図 5-9. Current-Limit Accuracy at 50 mA



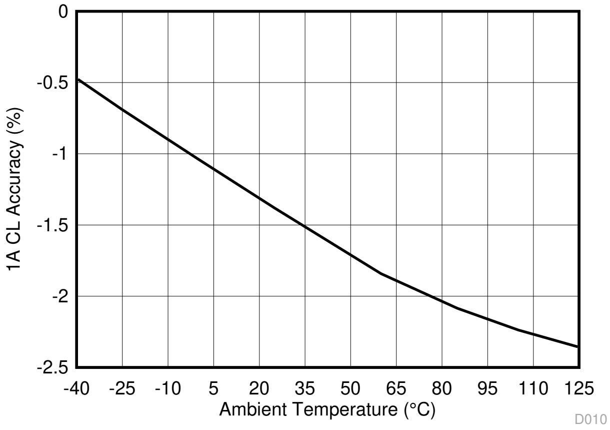
I_{OUT} = 150 mA

図 5-10. Current-Limit Accuracy at 150 mA



I_{OUT} = 300 mA

図 5-11. Current-Limit Accuracy at 300 mA



I_{OUT} = 1 A

図 5-12. Current-Limit Accuracy at 1 A

6 Detailed Description

6.1 Overview

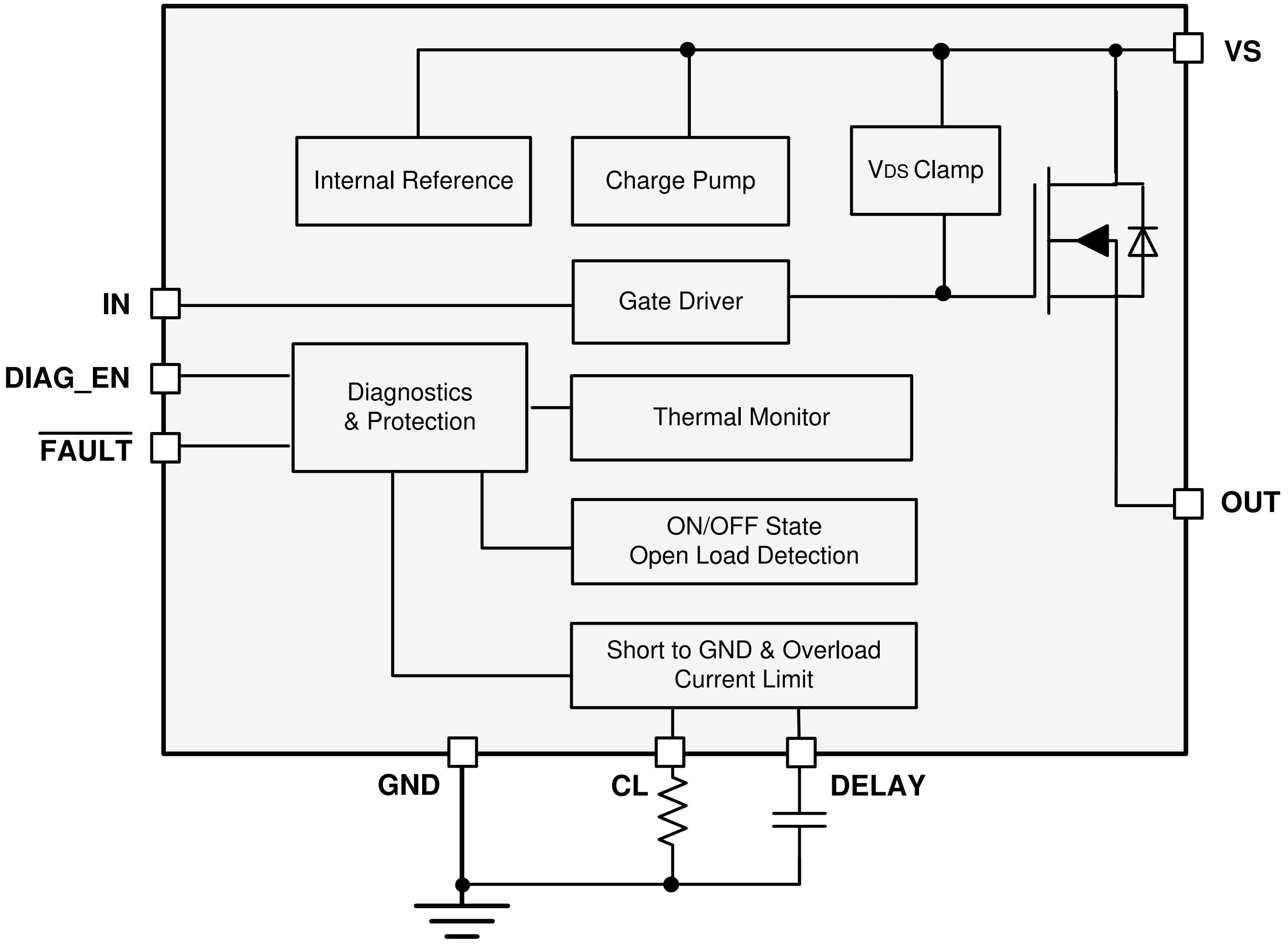
The TPS1H000-Q1 device is a smart high-side switch, with an internal charge pump and single-channel integrated NMOS power FET. The adjustable current-limit function greatly improves the reliability of the whole system. Full diagnostic features enable intelligent control of the load.

The external high-accuracy current limit allows setting the current-limit value for the application. When overcurrent occurs, the device improves system reliability by clamping the inrush current effectively. The TPS1H000-Q1 device can also save system cost by reducing the size of PCB traces and connectors, and the capacity of the preceding power stage. The TPS1H000-Q1 device allows three modes when a current limit occurs. Through the configuration on the DELAY pin, users can set the output to any of three modes: hold the current consistently, latch off immediately, or retry automatically. The configurable behaviors during current limit provide design flexibility that considers functionality, cost, and thermal dissipation.

The TPS1H000-Q1 device supports full diagnostics with the digital status output. High-accuracy and low-threshold open-load detection enables real-time on-state monitoring. The TPS1H000-Q1 device also supports operation without an MCU, the standalone mode, which allows the system to implement the full functionality locally.

The TPS1H000-Q1 device is a smart high-side switch for a wide variety of resistive, inductive, and capacitive loads, including LEDs, relays, and sub-modules.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Current Limit

A high-accuracy current limit allows high reliability of the design. It protects the load and the power supply from overstressing during short-circuit-to-GND or power-up conditions. The current limit can also save system cost by reducing the size of PCB traces and connectors, and the capacity of the preceding power stage.

When a current-limit threshold is reached, a closed loop activates immediately. The output current is clamped at the set value, and a fault is reported out. The device heats up due to the high power dissipation on the power FET.

The device has two current-limit thresholds.

- Internal current limit – The internal current limit is fixed at $I_{CL(int)}$. Tie the CL pin directly to the device GND for large-transient-current applications.
- External adjustable current limit – An external resistor is used to set the current-limit threshold. Use 式 1 to calculate $R_{(CL)}$. $V_{CL(th)}$ is the internal band-gap voltage. $K_{(CL)}$ is the ratio of the output current and the current-limit set value. $K_{(CL)}$ is constant across temperature and supply voltage. The external adjustable current limit allows the flexibility to set the current-limit value by application.

$$R_{CL} = \frac{V_{CL(th)} \times K_{(CL)}}{I_{OUT}} \tag{1}$$

Note that if using a GND network which causes a level shift between the device GND and board GND, the CL pin must be connected to the device GND.

For better protection from a hard short-to-GND condition (when the IN pin is enabled, a short to GND occurs suddenly), the device implements a fast-trip protection to turn off the output before the current-limit closed loop is set up. The fast-trip response time is less than 1 µs, typically. With this fast response, the device can achieve better inrush current-suppression performance.

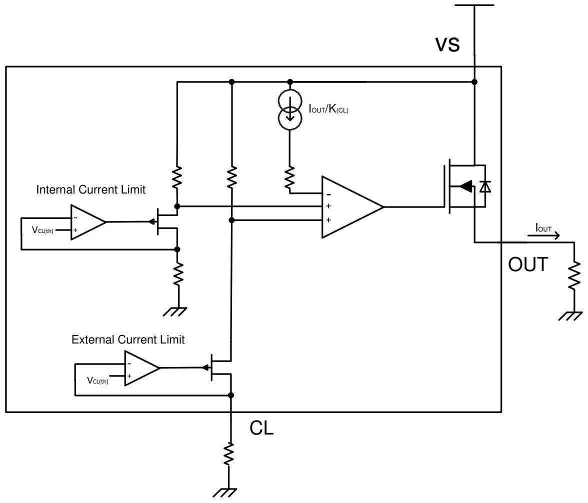


図 6-1. Current Limit

6.3.2 DELAY Pin Configuration

When a current limit occurs, the TPS1H000-Q1 device supports three different behaviors of the output.

表 6-1. Current Limit Configurations

MODE	DELAY CONFIGURATION	OUTPUT CURRENT BEHAVIOR	$\overline{\text{FAULT}}$ RECOVERY
Holding	Connect to GND directly	When hitting a current limit, the output current holds at the setting current. The device enters into thermal shutdown mode when $T_J > T_{(SD)}$.	$\overline{\text{FAULT}}$ clears when IN turns low for a duration longer than $t_{\overline{FAULT}}$ OR when the current limit is removed when IN is high.
Latch-off	Connect to GND through a capacitor	When hitting a current limit, the output current holds at the setting current, but latches off after a preset DELAY time (t_{dl1}+ t_{dl2}). t_{dl1} is the default delay time; t_{dl2} is a capacitor-configurable delay time. The output stays latched off regardless of whether the current limit is removed. The output recovers only when IN is toggling.	$\overline{\text{FAULT}}$ clears when IN turns low for a duration longer than $t_{\overline{FAULT}}$.
Auto-retry	External pullup	When hitting a current limit, the output current holds at the setting current, but periodically comes on for $t_{hic(on)}$ and turns off for $t_{hic(off)}$.	$\overline{\text{FAULT}}$ clears when IN turns low for a duration longer than $t_{\overline{FAULT}}$ OR when the current limit is removed for $t_{hic(on)}$

6.3.2.1 Holding Mode

Holding mode is active when the DELAY pin connects to GND directly. When hitting a current limit, the output current holds at the setting current. The device enters into thermal shutdown mode when $T_J > T_{(SD)}$.

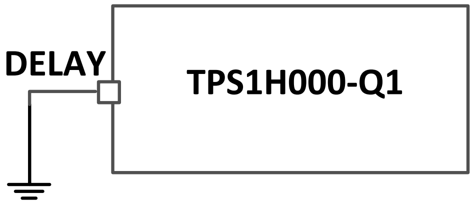


図 6-2. Holding Mode Connection

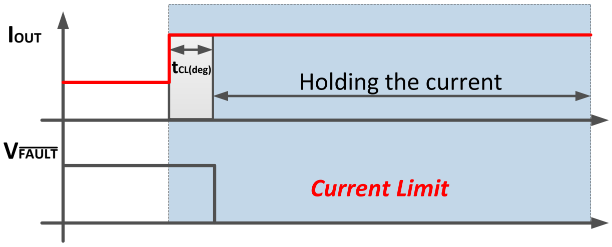


図 6-3. Holding Mode Example

6.3.2.2 Latch-Off Mode

Latch-off mode is active when the DELAY pin connects to GND through a capacitor. When hitting a current limit, the output current holds at the setting current, but latches off after a preset DELAY time (t_{dl1}+ t_{dl2}). t_{dl1} is the default delay time, t_{dl2} is a configurable delay time set by a capacitor. The output stays latched off regardless of whether the current limit is removed. The output recovers only when IN is toggling.

t_{dl2} can be calculated by 式 2. The $I_{dl(chg)}$is the device charging current in latch-off mode, $V_{dl(ref)}$ is the internal reference voltage in latch off mode, t_{dl2} is the user-setting delay time, and C_{DELAY} is the capacitor connected on the DELAY pin.

$$C_{DELAY} = \frac{I_{dl(chg)} \times t_{dl2}}{V_{dl(ref)}} \quad (2)$$

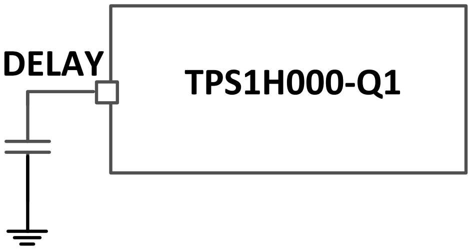


図 6-4. Latch-Off-Mode Connection

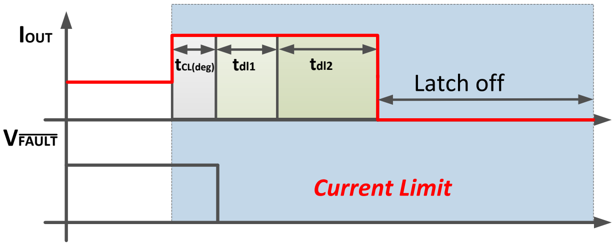


図 6-5. Latch-Off-Mode Example

6.3.2.3 Auto-Retry Mode

Auto-retry mode is active when the DELAY pin is externally pulled up. The pullup voltage must be higher than $V_{dl(th)}$. When hitting the current limit, the output current holds at the setting current, but periodically comes on for $t_{hic(on)}$ and turns off for $t_{hic(off)}$.

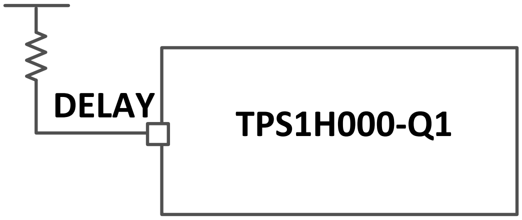


図 6-6. Auto-Retry-Mode Connection

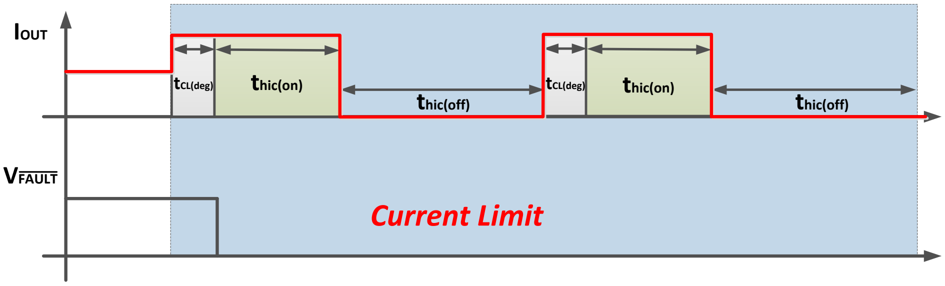


図 6-7. Auto-Retry-Mode Example

6.3.3 Standalone Operation

In a typical application, the TPS1H000-Q1 device is controlled by a microcontroller. The device also supports standalone operation. IN and DIAG_EN have a 40-V maximum dc rating, and can be connected to the VS pin directly. In auto-retry mode, the DELAY pin can also be connected to the VS pin through a 100-kΩ resistor.

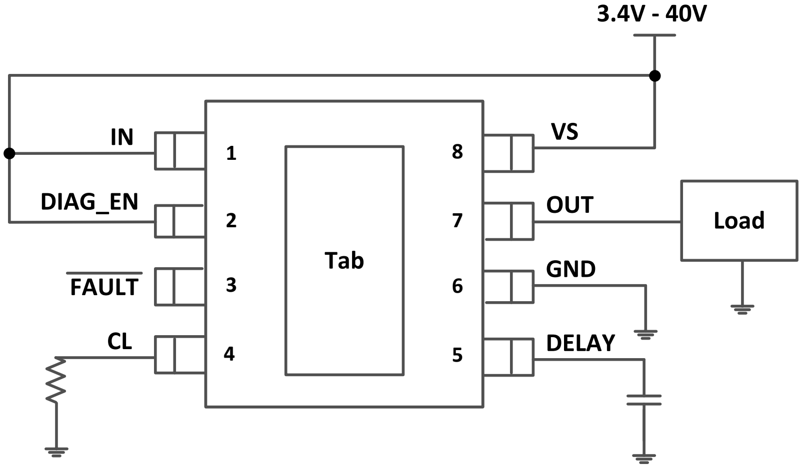


図 6-8. Standalone Operation in Latch-Off Mode

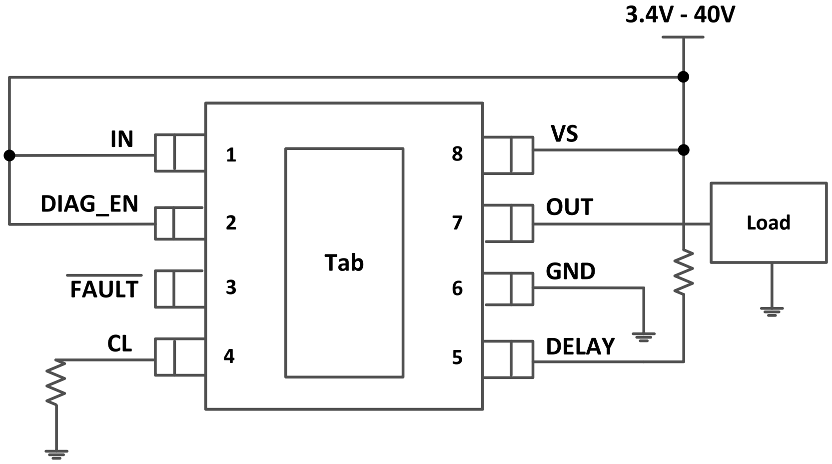


図 6-9. Standalone Operation in Auto-Retry Mode

6.3.4 Fault Truth Table

The DIAG_EN pin enables or disables the diagnostic functions. If multiple devices are used, but the ADC resource is limited in the microcontroller, the microcontroller can use GPIOs to set DIAG_EN high to enable the diagnostics of one device while disabling the diagnostics of the other devices by setting DIAG_EN low. In addition, the device can keep the power consumption to a minimum by setting DIAG_EN and IN low.

表 6-2 applies when the DIAG_EN pin is enabled. 表 6-3 applies when the DIAG_EN pin is disabled.

表 6-2. Fault Truth Table

CONDITION	IN	OUT	CRITERION	$\overline{\text{FAULT}}$	FAULT RECOVERY
Normal	L	L	—	H	—
	H	H	—	H	
Overload or short to GND	H	L	Current limit triggered.	L	See 表 6-1.
Open load or short to battery	H	H	$I_{OUT} < I_{(ol,on)}$	L	$\overline{\text{FAULT}}$ clears when IN turns low for a duration longer than $t_{\overline{\text{FAULT}}}$. OR $\overline{\text{FAULT}}$ clears when the open load is removed.
	L[1]	H	$V_{VS} – V_{OUT} < V_{(ol,off)}$	L	$\overline{\text{FAULT}}$ clears when IN is toggling OR $\overline{\text{FAULT}}$ clears when the open load is removed.
Thermal shutdown	H	—	Thermal shutdown triggered	L	$\overline{\text{FAULT}}$ clears when IN turns low for a duration longer than $t_{\overline{\text{FAULT}}}$. OR $\overline{\text{FAULT}}$ clears when thermal shutdown quits.
Thermal swing	H	—	Thermal swing triggered	L	$\overline{\text{FAULT}}$ clears when IN turns low for a duration longer than $t_{\overline{\text{FAULT}}}$. OR $\overline{\text{FAULT}}$ clears when thermal swing quits.

(1) An external pullup is required for open-load detection.

表 6-3. DIAG_EN Disabled Condition

DIAG_EN	IN	PROTECTIONS AND DIAGNOSTICS
LOW	ON	Diagnostics disabled, full protections
	OFF	Diagnostics disabled, no protection

6.3.5 Full Diagnostics

6.3.5.1 Short-to-GND and Overload Detection

When the output is on, a short to GND or an overload condition causes overcurrent. If the overcurrent triggers either the internal or external current-limit threshold, a fault condition is reported out as $\overline{\text{FAULT}}$ pin = low.

6.3.5.2 Open-Load Detection

6.3.5.2.1 Output On

When the output is on, if the current flowing through the output $I_{OUT} < I_{(ol,on)}$, the device recognizes an open-load fault. For open-load detection in output on, no external circuitry is required.

6.3.5.2.2 Output Off

When the output is off, if a load is connected, the output is pulled down to GND. But if an open load occurs, the output voltage is close to the supply voltage ($V_{VS} – V_{OUT} < V_{(ol,off)}$), and the device recognizes an open-load fault.

There is always a leakage current $I_{(ol,off)}$ present on the output due to the internal logic control path or external humidity, corrosion, and so forth. So an external pullup resistor is recommended to offset the leakage current when an open load is detected. The recommended pullup resistance is 15 kΩ.

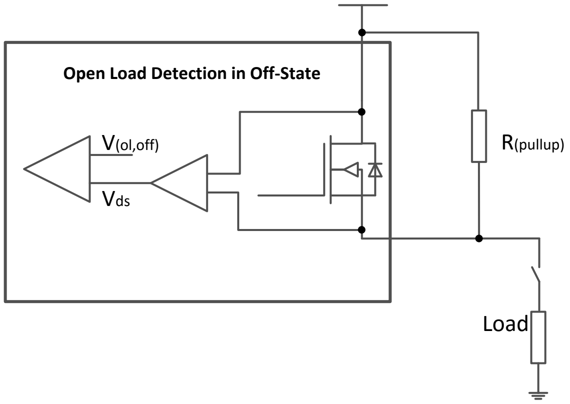


図 6-10. Open-Load Detection in Output Off

6.3.5.3 Short-to-Battery Detection

Short-to-battery has the same detection mechanism and behavior as open-load detection, in both the on-state and off-state.

6.3.5.4 Thermal Fault Detection

To protect the device in severe power stressing cases, the device implements two types of thermal fault detection, absolute temperature protection (thermal shutdown) and dynamic temperature protection (thermal swing).

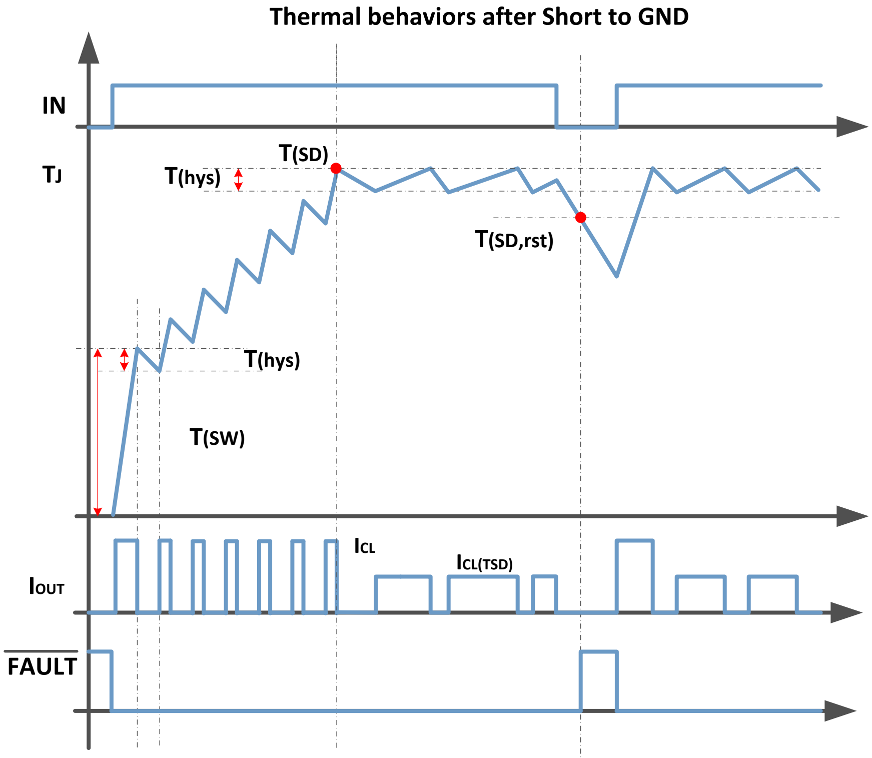


図 6-11. Thermal Behavior Diagram

6.3.5.4.1 Thermal Shutdown

Thermal shutdown is active when the absolute temperature $T_J > T_{(SD)}$. When thermal shutdown occurs, the output turns off.

6.3.5.4.2 Thermal Swing

Thermal swing activates when the power FET temperature is increasing sharply, that is, when $\Delta T = T_{(FET)} - T_{(Logic)} > T_{(sw)}$, then the output turns off. The output automatically recovers and the fault signal clears when $\Delta T = T_{(FET)} - T_{(Logic)} < T_{(sw)} - T_{(hys)}$. The thermal swing function improves the device reliability when subjected to repetitive fast thermal variation.

6.3.5.4.3 Fault Report Holding

When using PWM dimming, $\overline{\text{FAULT}}$ is easily cleared by the PWM falling edge. Even if the fault condition remains all the time, $\overline{\text{FAULT}}$ is discontinuous. To avoid this unexpected fault report behavior, the device implements fault-report holding time. 図 6-12 shows a typical issue when PWM dimming, the $\overline{\text{FAULT}}$ is cleared unexpectedly even when the short-to-GND still exists. The TPS1H000-Q1 device with fault-report holding function allows the right behavior as shown in 図 6-13.

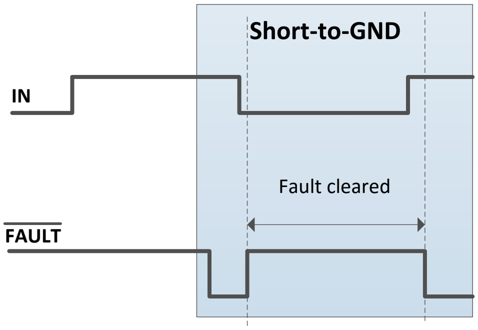


図 6-12. Without Fault-Report Holding

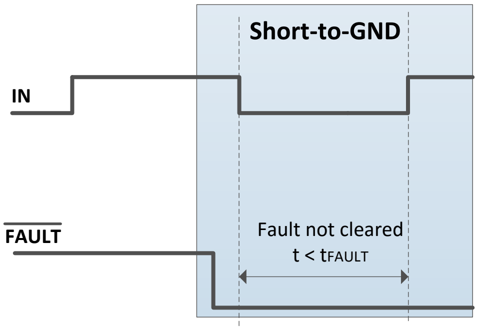


図 6-13. With Fault-Report Holding

6.3.6 Full Protections

6.3.6.1 UVLO Protection

The device monitors the supply voltage, V_{VS}, to prevent unpredicted behaviors when V_{VS} is too low. When V_{VS} falls down to $V_{VS(uvf)}$, the device shuts down. When V_{VS} rises up to $V_{VS(uvr)}$, the device turns on.

6.3.6.2 Inductive Load Switching Off Clamp

When switching an inductive load off, the inductive reactance tends to pull the output voltage negative. Excessive negative voltage could cause the power FET to break down. To protect the power FET, an internal clamp between drain and source is implemented, namely $V_{DS(clamp)}$.

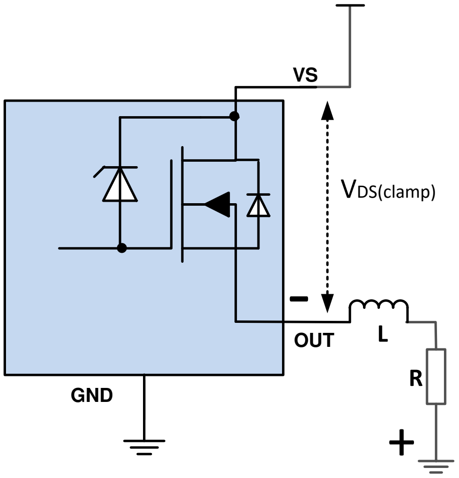


図 6-14. Drain-to-Source Clamping Structure

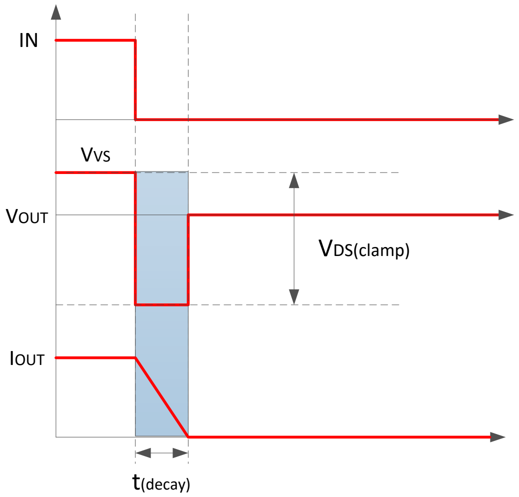


図 6-15. Inductive-Load Switching-Off Diagram

6.3.6.3 Loss-of-GND Protection

When loss of GND occurs, the output is shut down regardless of whether the IN pin is high or low. The device can protect against two ground-loss conditions, loss of device GND and loss of module GND.

6.3.6.4 Loss-of-Power-Supply Protection

When loss of supply occurs, the output is shut down regardless of whether the IN pin is high or low. For a resistive or a capacitive load, loss of supply has no risk. But for a charged inductive load, the current is driven from all the logic control pins to maintain the inductance current. To protect the system in this condition, TI recommends protection with an external free-wheeling diode.

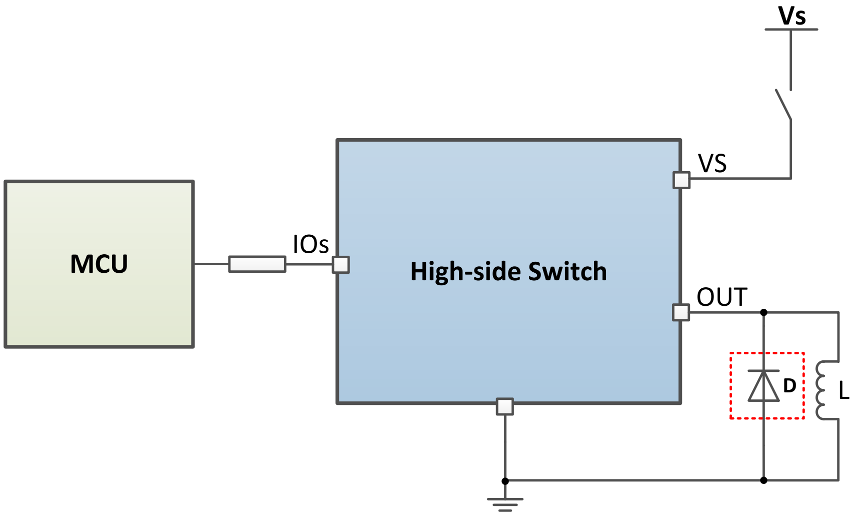


図 6-16. Protection for Loss of Power Supply

6.3.6.5 Reverse-Current Protection

Reverse current occurs in two conditions: short to supply and reverse polarity.

- When a short to the supply occurs, there is only reverse current through the body diode. $I_{R(1)}$ specifies the limit of the reverse current.
- In a reverse-polarity condition, there are reverse currents through the body diode and the device GND pin. $I_{R(2)}$ specifies the limit of the reverse current.

To protect the device, TI recommends two types of external circuitry.

- Adding a blocking diode (method 1). Both the device and load are protected when in reverse polarity.
- Adding a GND network (method 2). The reverse current through the device GND is blocked. The reverse current through the FET is limited by the load itself. TI recommends a resistor in parallel with the diode as a GND network. The recommended configuration is a 1-kΩ resistor in parallel with a >100-mA diode. The reverse current protection diode in the GND network forward voltage should be less than 0.6 V in any circumstances. In addition a minimum resistance of 4.7 K is recommended on the I/O pins.

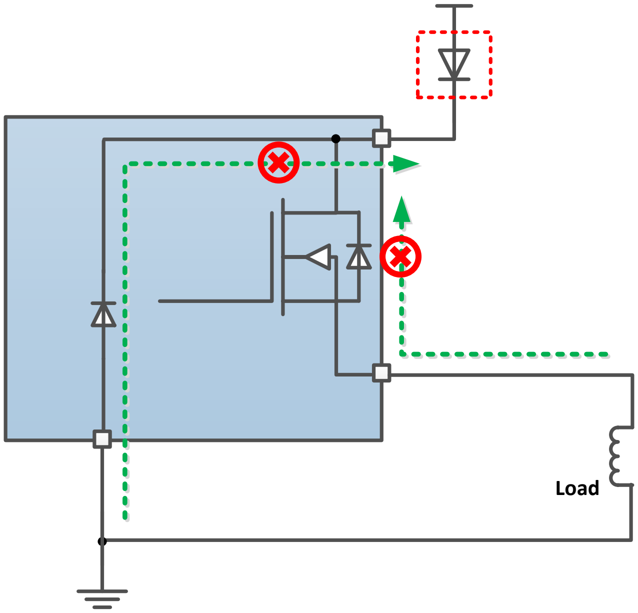


図 6-17. Reverse-Current External Protection, Method 1

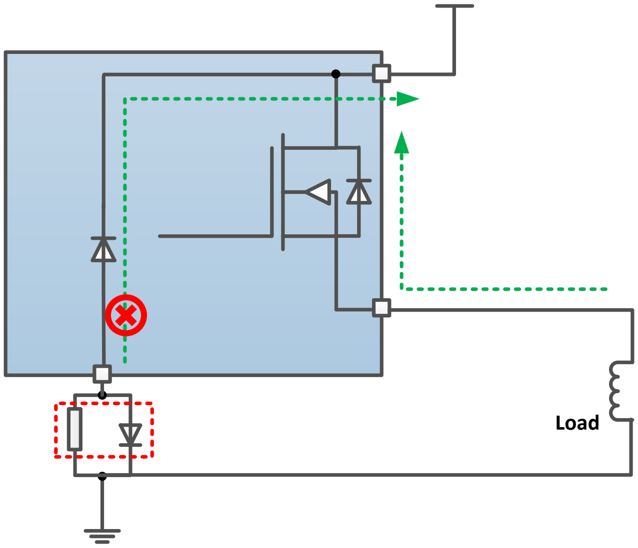


図 6-18. Reverse-Current External Protection, Method 2

6.3.6.6 MCU I/O Protection

TI recommends series resistors to protect the microcontroller, for example, 4.7-kΩ when using a 3.3-V microcontroller and 10-kΩ for a 5-V microcontroller.

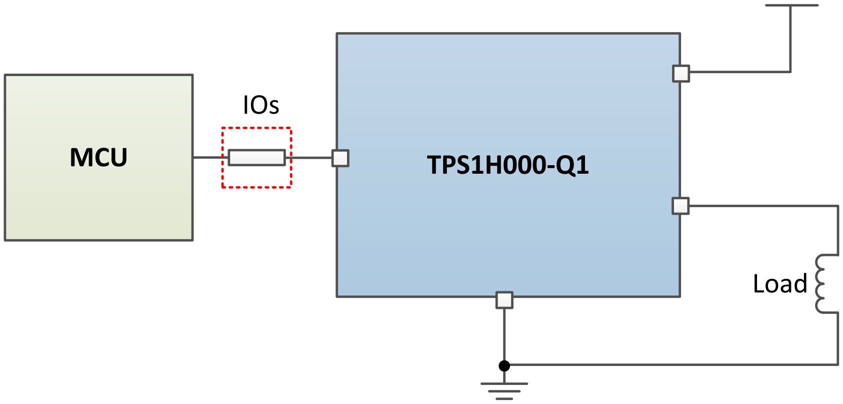


図 6-19. MCU I/O External Protection

6.4 Device Functional Modes

6.4.1 Working Modes

The device has three working modes, the normal mode, the standby mode, and the standby mode with diagnostics, as shown in 図 6-20.

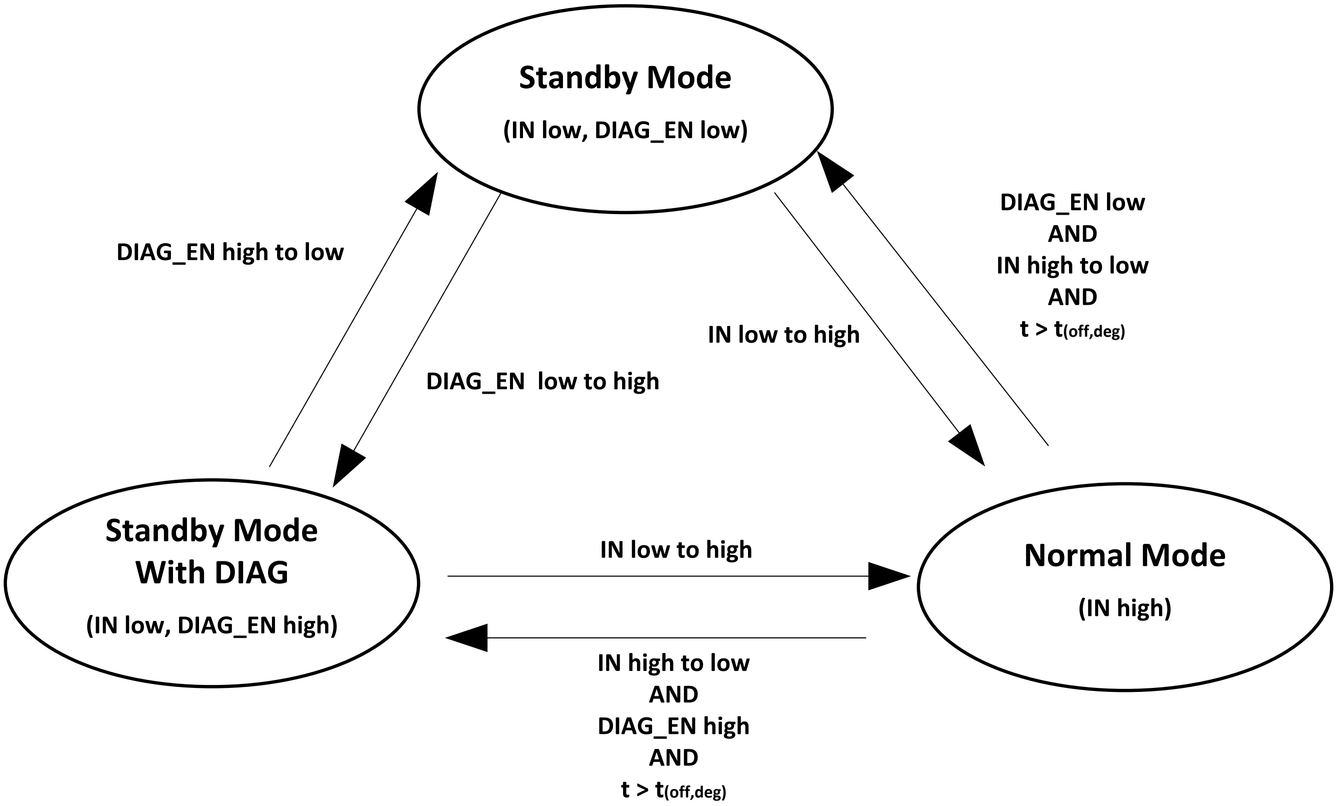


図 6-20. Working Modes

6.4.1.1 Normal Mode

When IN is high, the device enters normal mode.

6.4.1.2 Standby Mode

When IN is low and DIAG_EN is low, the device enters standby mode with ultralow power consumption.

6.4.1.3 Standby Mode With Diagnostics

When IN is low and DIAG_EN is high, the device enters standby mode with diagnostics. The device still supports open-load and short-to-battery detection even when IN is low.

7 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TPS1H000-Q1 device is a smart high-side switch, with an internal charge pump and single-channel integrated NMOS power FET. The adjustable current-limit function greatly improves the reliability of the whole system. Full diagnostic features enable intelligent control of the load. The TPS1H000-Q1 device can be used for a wide variety of resistive, inductive, and capacitive loads, including LEDs, relays, and sub-modules.

7.2 Typical Application

図 7-1 shows an example of how to design the external circuitry parameters.

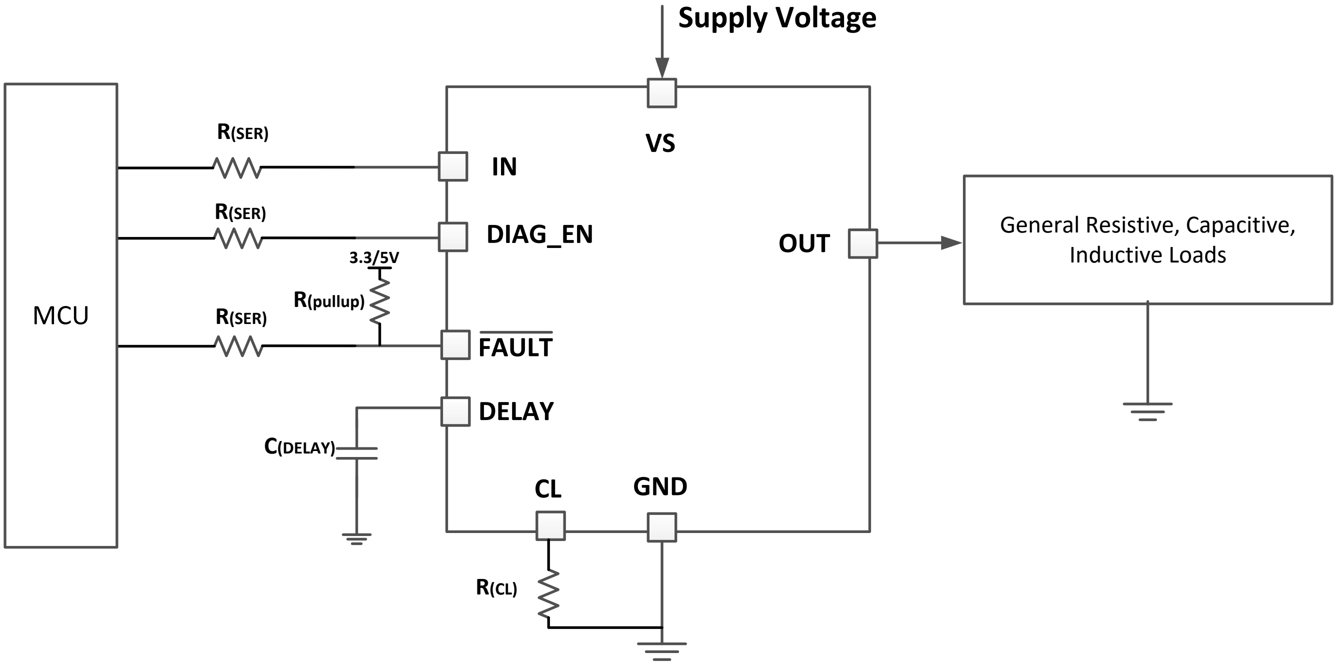


図 7-1. Typical Application Circuitry

7.2.1 Design Requirements

- V_{VS} range from 6 V to 18 V
- Nominal current of 100 mA
- Expected current limit value of 500 mA
- Thermal sensitive system, when current limit occurs, the output latches off after 0.2 s. The 0.2 s is to ensure the safe start-up for a capacitive load, clamping the inrush current but without latch-off during start-up.
- Full diagnostics with 5-V MCU, including on-state open-load detection, short-to-GND or overcurrent detection, and thermal shutdown detection

7.2.2 Detailed Design Procedure

To set the adjustable current limit value at 500 mA, calculate $R_{(CL)}$ as follows:

$$R_{(CL)} = \frac{V_{CL(th)} \times K_{(CL)}}{I_{OUT}} = \frac{0.8 \times 600}{0.5} = 960\ \Omega \tag{3}$$

To set the adjustable latch-off delay at 0.2 s, calculate $C_{(DELAY)}$ as follows:

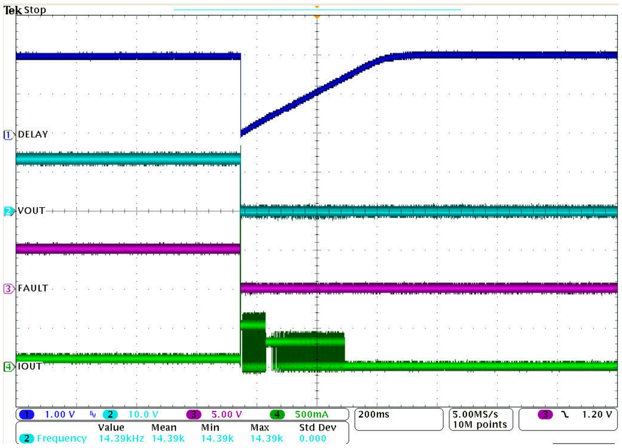
$$t_{dl} = t_{CL(deg)} + t_{dl1} + t_{dl2} = 0.2 \approx t_{dl2}$$

$$C_{DELAY} = \frac{I_{dl(chg)} \times t_{dl2}}{V_{dl(ref)}} = \frac{4.5 \times 0.2}{1.45} \times 10^{-6} = 0.62\ \mu F \tag{4}$$

TI recommends $R_{(SER)}$ = 10 kΩ for a 5-V MCU, and $R_{(pullup)}$ = 10 kΩ as the pullup resistor.

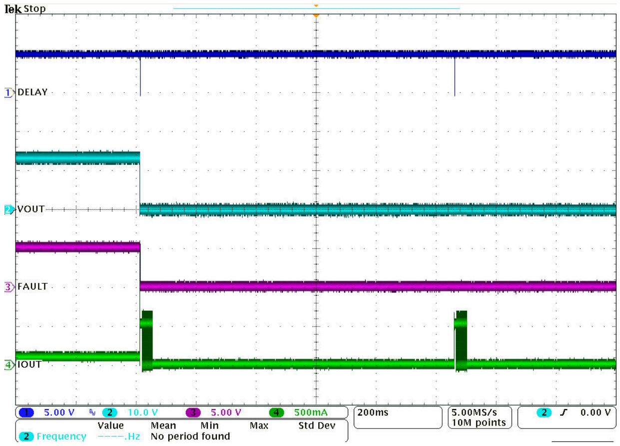
7.2.3 Application Curves

The following curves are test examples of hard short conditions. The load is 0.1 A and the current limit value is 0.5 A. 図 7-2 shows a waveform of the latch-off mode. 図 7-3 shows a waveform of the auto-retry mode.



Load = 0.1 A Current limit = 0.5 A

図 7-2. Hard-Short Condition in Latch-Off Mode



Load = 0.1 A Current limit = 0.5 A

図 7-3. Hard-Short Condition in Auto-Retry Mode

7.3 Power Supply Recommendations

The device can be used for both 12-V and 24-V applications. The normal power supply connection is a 12-V or 24-V system.

7.4 Layout

7.4.1 Layout Guidelines

To prevent thermal shutdown, T_J must be less than 175°C. If the output current is very high, the power dissipation may be large. However, the PCB layout is very important. Good PCB design can optimize heat transfer, which is absolutely essential for the long-term reliability of the device.

- Maximize the copper coverage on the PCB to increase the thermal conductivity of the board. The major heat-flow path from the package to the ambient is through the copper on the PCB. Maximum copper is extremely important when there are not any heat sinks attached to the PCB on the other side of the board opposite the package.
- Add as many thermal vias as possible directly under the package thermal pad to optimize the thermal conductivity of the board.
- All thermal vias should either be plated shut or plugged and capped on both sides of the board to prevent solder voids. To ensure reliability and performance, the solder coverage should be at least 85%.

7.4.2 Layout Example

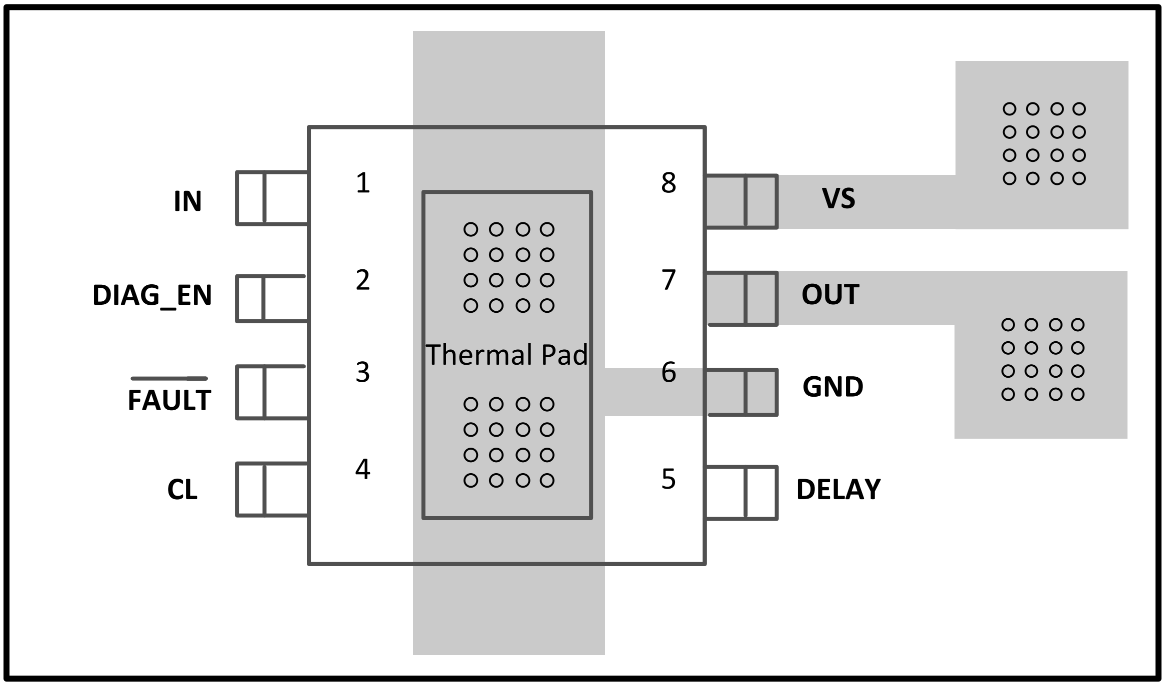


図 7-4. Layout Example

8 Device and Documentation Support

8.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.2 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

8.3 Trademarks

PowerPAD™ and テキサス・インスツルメンツ E2E™ are trademarks of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

8.4 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.5 用語集

テキサス・インスツルメンツ用語集	この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (June 2019) to Revision D (December 2024) **Page**

- ドキュメント全体にわたって表、図、相互参照の採番方法を更新 1
- Updated maximum ratings of VS pin and IN/DIAG_EN pins to 42V in the Absolute Maximum Ratings table 4

Changes from Revision B (March 2018) to Revision C (June 2019) **Page**

- Changed IN is high and DIAG_EN is high to IN is low and DIAG_EN is low in the *Standby Mode* section 21

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS1H000AQDGNRQ1	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	17SX
TPS1H000AQDGNRQ1.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	17SX

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

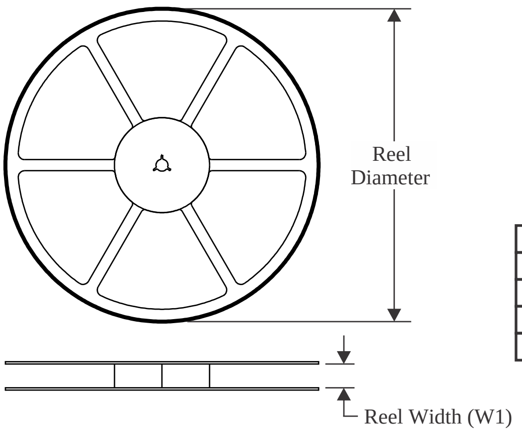
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

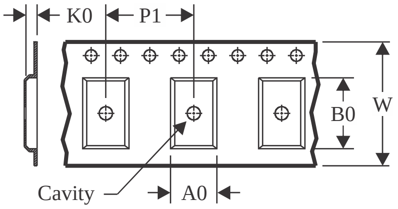
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

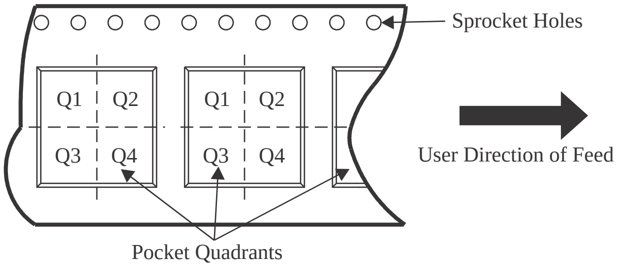


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

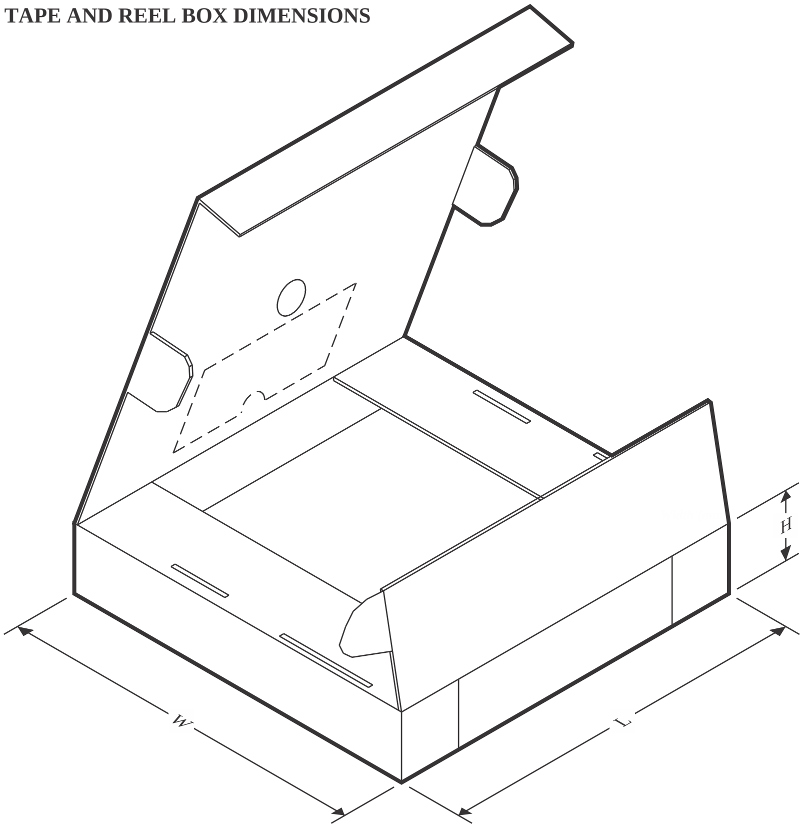
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS1H000AQDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

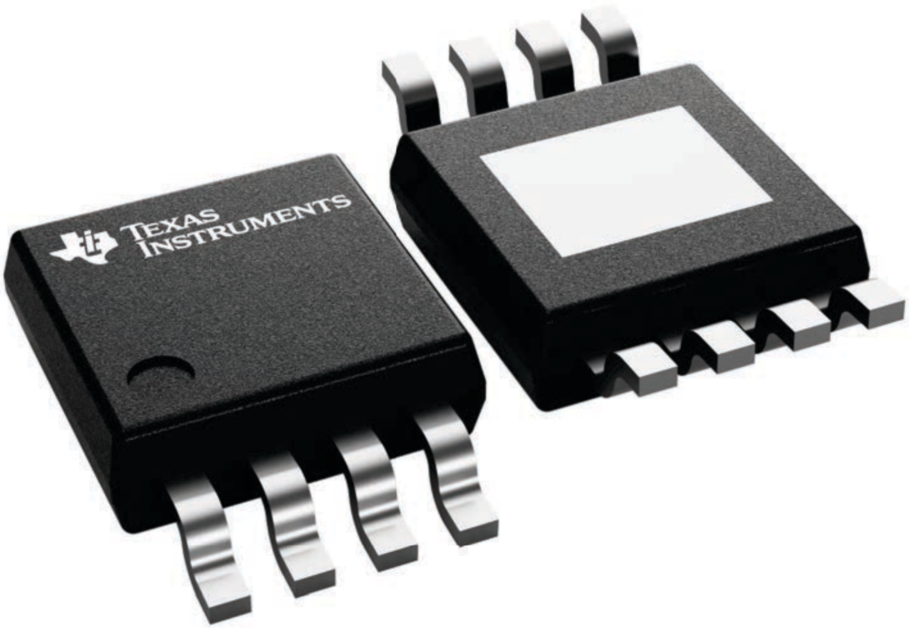
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS1H000AQDGNRQ1	HVSSOP	DGN	8	2500	366.0	364.0	50.0

GENERIC PACKAGE VIEW

DGN 8 **PowerPAD^{TM} HVSSOP - 1.1 mm max height**

3 x 3, 0.65 mm pitch SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



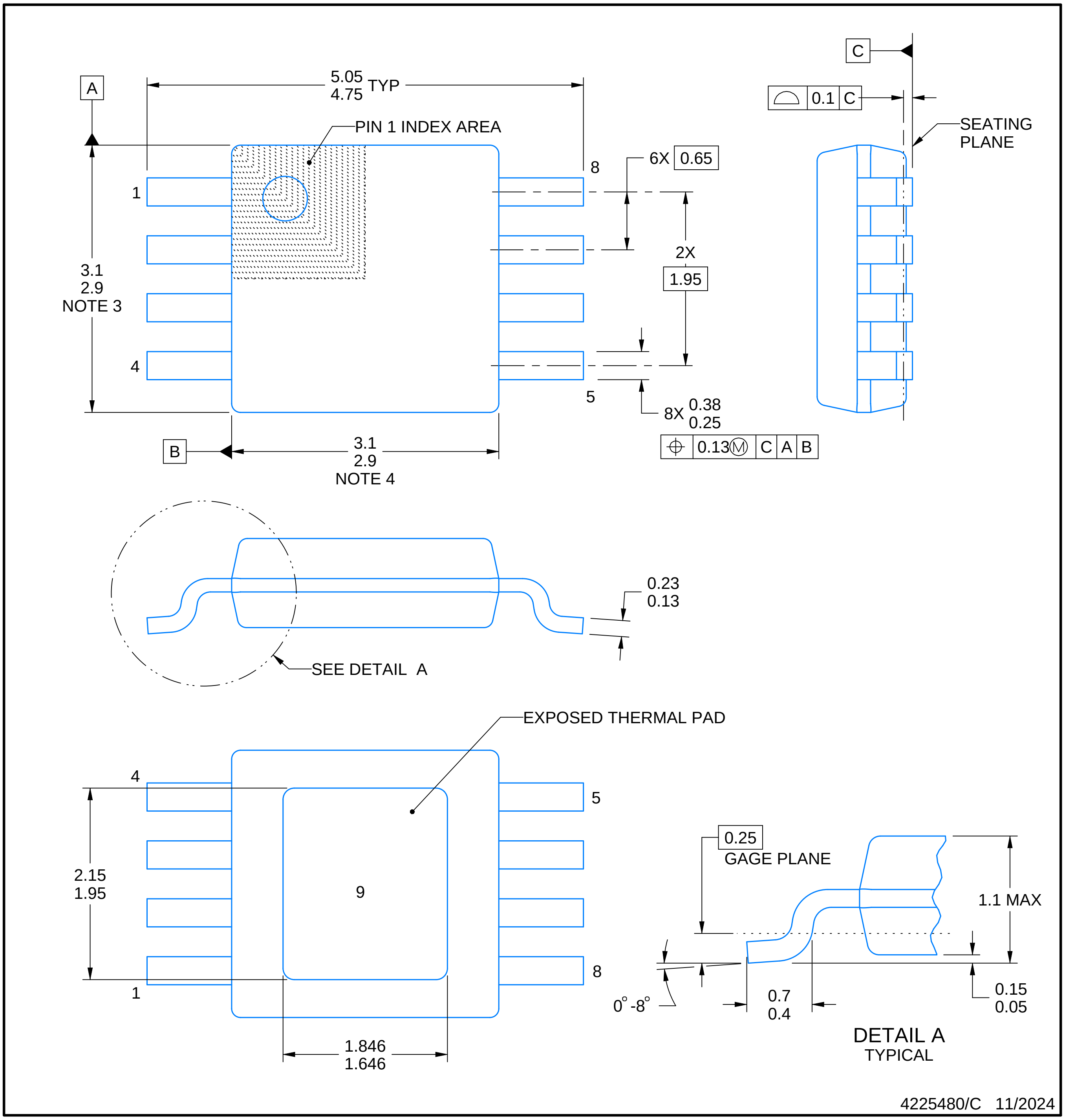
4225482/B

PACKAGE OUTLINE

DGN0008G

PowerPAD™ HVSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

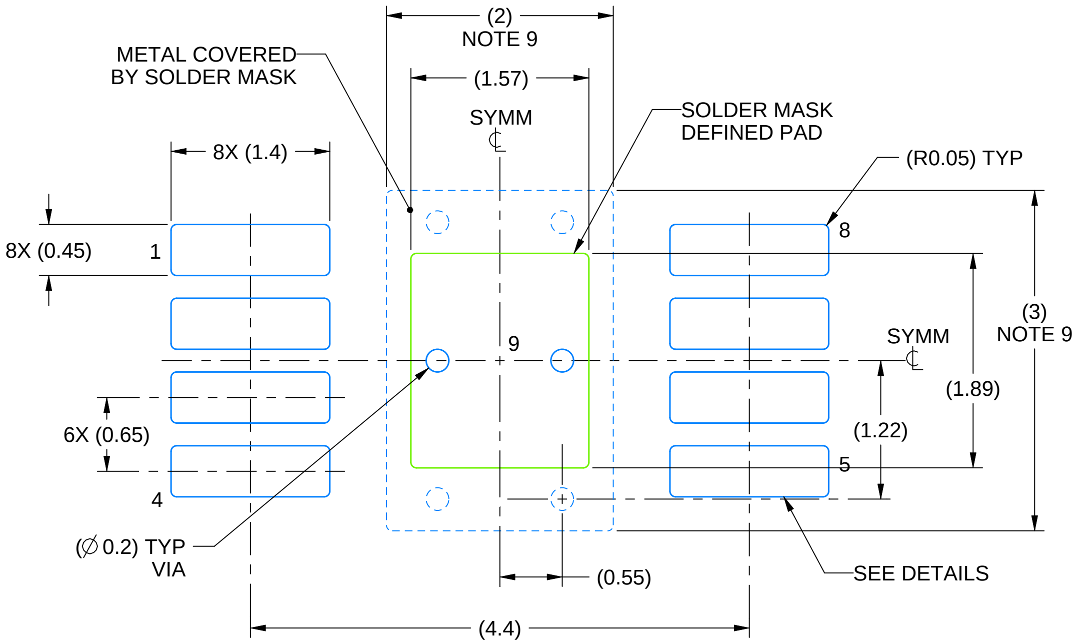


4225480/C 11/2024

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

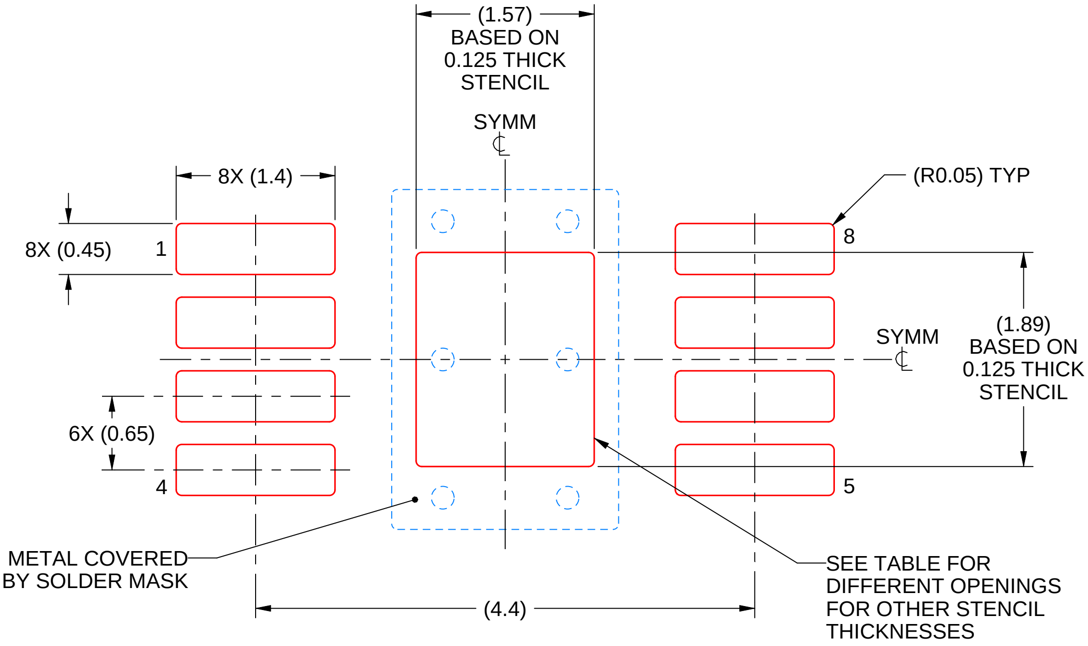
NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265