TPS1211-Q1 45V 車載用スマート ハイサイド ドライバ、保護および診断機能付き

1 特長

- 下記結果で AEC-Q100 認定済み
  - デバイス温度グレード 1:
    動作時周囲温度範囲 -40℃～+125℃
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 3.5V～40V の入力範囲 (絶対最大定格 45V)
- 最小 -30V までの出力逆極性保護
- 100µA の電流能力を持つ内蔵 12V チャージ ポンプ
- 低シャットダウン電流 (EN/UVLO = Low):0.9µA
- 強力なプルアップ (3.7A) およびプルダウン (4A) ゲートドライバ
- 外付けバックツーバック N チャネル MOSFET を駆動
- 容量性負荷を駆動するためのプリチャージ スイッチ ドライバを内蔵したバリアント (TPS12111-Q1)
- 可変応答時間 (TMR) とフォルト フラグ出力 ($\overline{FLT\_I}$) を備えた 2 レベルの可変過電流保護機能 (IWRN、ISCP)
- 高速な短絡保護:1.2µs (TPS12111-Q1、TPS12112-Q1)、4µs (TPS12110-Q1)
- 高精度アナログ電流モニタ出力 (IMON):±2% (30mV 時) (V_{SNS})
- 調整可能な低電圧誤動作防止 (UVLO) および過電圧保護 (OV)< ±2%
- フォルト フラグ出力 ($\overline{FLT\_T}$) を備えたリモート過熱検出 (DIODE) および保護
- TPS4811-Q1 とピン互換

2 アプリケーション

- パワー ディストリビューション ボックス
- ボディ コントロール モジュール
- DC/DC コンバータ
- バッテリ管理システム (BMS)

3 概要

TPS1211-Q1 ファミリは、保護および診断機能を備えた 45V のスマート ハイサイド ドライバです。本デバイスは、動作電圧範囲が 3.5V ～ 40V と広く、12V のシステム設計に理想的です。

本デバイスは、大電流システム設計において並列 FET を使って電力をスイッチングできる、強力な 3.7A ピーク ソース (PU) と 4A ピーク シンク (PD) ゲート ドライバを備えています。ゲート ドライバの制御入力として INP を使います。

本デバイスは、エネルギー管理システムを可能にする、高精度の電流検出 (30mV で±2%) 出力 (IMON) を備えています。本デバイスは、スレッショルドと応答時間を精密に調整できる $\overline{FLT\_I}$ 出力を備えた 2 レベルの過電流保護機能を備えています。自動リトライおよびラッチオフ フォルト動作は設定可能です。本デバイスは、$\overline{FLT\_T}$ 出力を備えたリモート過熱保護機能を備えています。

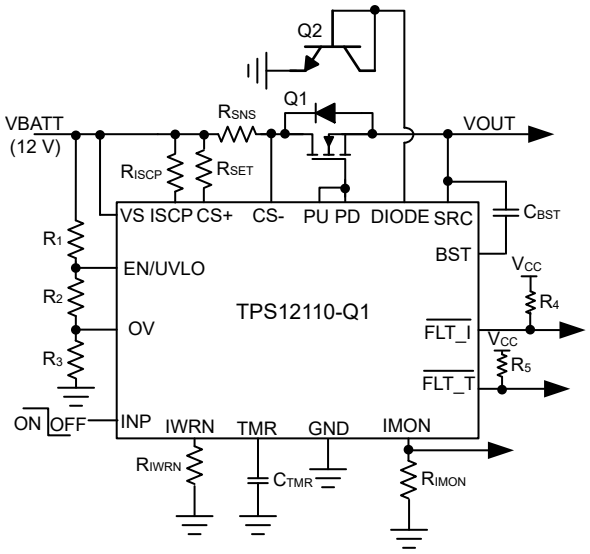
TPS12111-Q1 は、制御入力 (INP_G) を備えたプリチャージ ドライバ (G) を内蔵しています。この機能は、大きな容量性負荷を駆動する必要がある設計を可能にします。シャットダウン モード (EN/UVLO < 0.3V) では、コントローラは 0.9µA (標準値) の合計シャットダウン電流を消費します。

TPS1211-Q1 は、隣接する高電圧ピンと低電圧ピンの間のピンを取り除くことで 0.8mm の間隔を確保した 19 ピン VSSOP パッケージで供給されます。

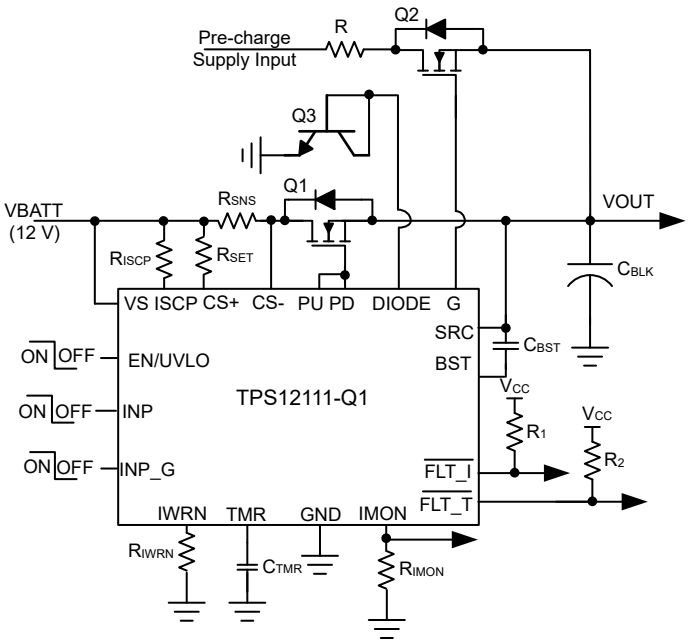
パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
TPS12110-Q1、TPS12111-Q1、TPS12112-Q1	DGX (VSSOP、19)	5.10mm × 3.00mm

(1) 供給されているすべてのパッケージについては、セクション 12 を参照してください。
(2) パッケージサイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



ヒーター負荷用スマート ハイサイド ドライバ



DC/DC コンバータ用サーキット ブレーカ

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4 Device Comparison Table

	TPS12110-Q1	TPS12111-Q1	TPS12112-Q1
Overvoltage protection	Yes	No	Yes
Precharge driver	No	Yes	No
Short-circuit protection response time	4 µs	1.2 µs	1.2 µs
Overtemperature fault response	Auto-retry with fixed 512-ms timer	Latch-off	Auto-retry with fixed 512-ms timer
IMON Output	Disabled when PD goes low	Disabled when PD goes low	Disabled when EN/UVLO is low below $V_{(ENF)}$ or $V_{(VS)} < V_{(VS\_PORF)}$

5 Pin Configuration and Functions

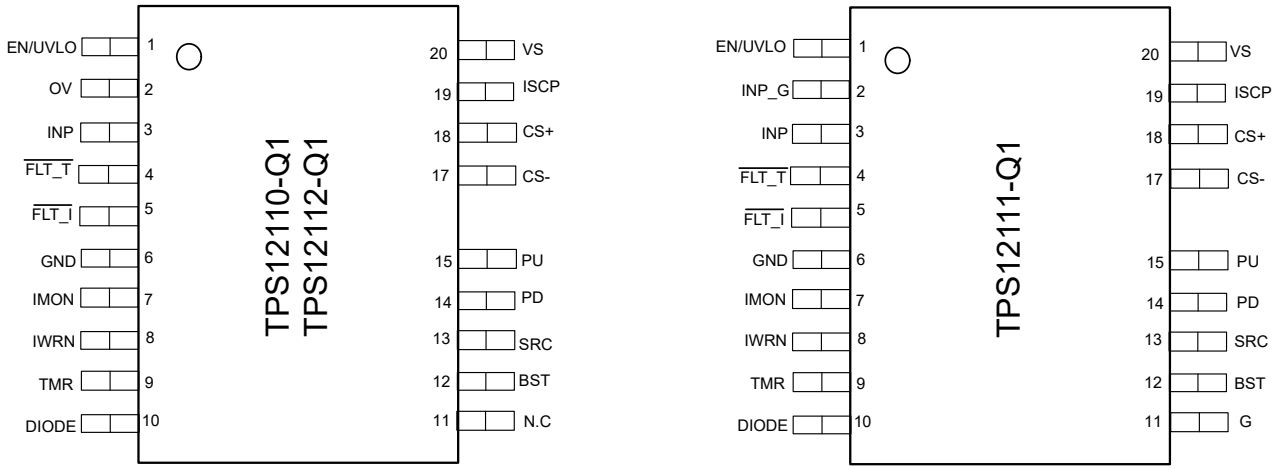

図 5-1. DGX Package, 19-Pin VSSOP (Top View)

表 5-1. Pin Functions

PIN				TYPE	DESCRIPTION
NAME	TPS12110-Q1	TPS12111-Q1	TPS12112-Q1		
	DGX-19 (VSSOP)				
EN/UVLO	1	1	1	I	EN/UVLO input. A voltage on this pin above 1.21 V enables normal operation. Forcing this pin below 0.3 V shuts down the TPS1211x-Q1, reducing quiescent current to approximately 0.9 µA (typical). Optionally connect to the input supply through a resistive divider to set the undervoltage lockout. When EN/UVLO is left floating an internal pulldown of 60 nA pulls EN/UVLO low and keeps the device in OFF state.
OV	2	—	2	I	Adjustable overvoltage threshold input. Connect a resistor ladder from input supply, OV to GND. When the voltage at OVP exceeds the over voltage cutoff threshold then the PD is pulled down to SRC turning OFF the external FET. When the voltage at OV goes below OV falling threshold then PU gets pulled up to BST, turning ON the external FET. OV must be connected to GND when not used. When OV is left floating an internal pulldown of 60 nA pulls OV low and keeps PU pulled up to BST.

表 5-1. Pin Functions (続き)

PIN				TYPE	DESCRIPTION
NAME	TPS12110-Q1	TPS12111-Q1	TPS12112-Q1		
	DGX-19 (VSSOP)				
INP_G	—	2	—	I	Input signal. CMOS compatible input reference to GND that sets the state of G pin. INP_G has an internal pulldown to GND to keep G pulled to SRC when INP_G is left floating.
INP	3	3	3	I	Input signal. CMOS compatible input reference to GND that sets the state of PD and PU pins. INP has an internal pulldown to GND to keep PD pulled to SRC when INP is left floating.
$\overline{\text{FLT\_T}}$	4	4	4	O	Open drain fault output. This pin asserts low when overtemperature fault is detected.
$\overline{\text{FLT\_I}}$	5	5	5	O	Open drain fault output. This pin asserts low after the voltage on the TMR pin has reached the fault threshold of 1.1V. this pin indicates the pass transistor is about to turn off due to an overcurrent condition. The $\overline{\text{FLT\_I}}$ pin does not go to a high-impedance state until the overcurrent condition and the auto-retry time expire.
GND	6	6	6	G	Connect GND to system ground.
IMON	7	7	7	O	Analog current monitor output. This pin sources a scaled down ratio of current through the external current sense resistor R_{SNS}. A resistor from this pin to GND converts current proportional to voltage. If unused, connect it to GND.
IWRN	8	8	8	I	Overcurrent detection setting. A resistor across IWRN to GND sets the over current comparator threshold. Connect IWRN to GND if over current protection feature is not desired.
TMR	9	9	9	I	Fault timer input. A capacitor across TMR pin to GND sets the times for fault warning, fault turn-off ($\overline{\text{FLT\_I}}$) and retry periods. Leave it open for fastest setting. Connect TMR to GND to disable overcurrent protection.
DIODE	10	10	10	I	Diode connection for temperature sensing. Connect it to base and collector of an MMBT3904 NPN BJT. Connect DIODE to GND, if remote over temperature sensing and protection feature is not desired.
G	—	11	—	O	GATE of external Precharge FET. Connect to the GATE of the external FET.
N.C	11	—	11	—	No connect.
BST	12	12	12	O	High-side bootstrapped supply. An external capacitor with a minimum value of > $Q_{g(tot)}$ of the external FET must be connected between this pin and SRC.
SRC	13	13	13	O	Source connection of the external FET.
PD	14	14	14	O	High current gate driver pulldown. This pin pulls down to SRC. For the fastest turn-off, tie this pin directly to the gate of the external high side MOSFET.
PU	15	15	15	O	High current gate driver pullup. This pin pulls up to BST. Connect this pin to PD for maximum gate drive transition speed. A resistor can be connected between this pin and the gate of the external MOSFET to control the inrush current during turn-on.
CS-	17	17	17	I	Current sense negative input.
CS+	18	18	18	I	Current sense positive input. Connect a 50 - 100-Ω resistor across CS+ to the external current sense resistor.
ISCP	19	19	19	I	Short-circuit detection threshold setting. Connect ISCP to CS– if short-circuit protection is not desired.

表 5-1. Pin Functions (続き)

PIN				TYPE	DESCRIPTION
NAME	TPS12110-Q1	TPS12111-Q1	TPS12112-Q1		
	DGX-19 (VSSOP)				
VS	20	20	20	Power	Supply pin of the controller.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input Pins	VS, CS+, CS–, ISCP to GND	–1	45	V
	VS, CS+, CS– to SRC	–60	45	
	SRC to GND	–30	45	
	PU, PD, G, BST to SRC	–0.3	16	
	TMR, IWRN, DIODE to GND	–0.3	5.5	
	OV, EN/UVLO, INP, INP_G, $\overline{FLT\_I}$, $\overline{FLT\_T}$ to GND	–1	20	
	CS+ to CS–	–0.3	0.3	
	$I_{(\overline{FLT\_I})}$, $I_{(\overline{FLT\_T})}$		10	mA
	$I_{(CS+)}$ to $I_{(CS–)}$, 1msec	–100	100	
Output Pins	PU, PD, G, BST to GND	–30	60	V
	IMON to GND	–1	7.5	
Operating junction temperature, T_j (2)		–40	150	°C
Storage temperature, T_{stg}		–40	150	

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (EN/UVLO, DIODE, G, VS)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
Input Pins	VS, CS+, CS– to GND	0		40	V
	EN/UVLO, OV to GND	0		15	
Output Pins	$\overline{FLT\_I}$, $\overline{FLT\_T}$ to GND	0		15	
	IMON to GND	0		5	
External Capacitor	VS to GND	22			nF
	BST to SRC	0.1			µF
Tj	Operating Junction temperature(2)	–40		150	°C

(1) Recommended Operating Conditions are conditions under which the device is intended to be functional. For specifications and test conditions, see Electrical Characteristics.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.4 Thermal Information

THERMAL METRIC(1)		TPS1211x-Q1	UNIT
		DGX	
		19 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	87	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	43.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

T_J = –40°C to +125°C; typical values at T_J = 25°C, $V_{(VS)}$ = $V_{(CS+)}$ = $V_{(CS–)}$ = 12 V, $V_{(BST – SRC)}$ = 12 V, $V_{(SRC)}$ = 0 V, V_{SNS} = Voltage across R_{SNS}

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
$V_{(VS)}$	Operating input voltage		3.5		40	V
$V_{(VS\_PORR)}$	VS POR threshold, rising		2.75	3	3.2	V
$V_{(VS\_PORF)}$	VS POR threshold, falling		2.65	2.9	3.1	V
$I_{(Q)}$	Total System Quiescent current, $I_{(GND)}$	$V_{(EN/UVLO)}$ = 2 V		613	700	µA
$I_{(SHDN)}$	SHDN current, $I_{(GND)}$	$V_{(EN/UVLO)}$ = 0 V, $V_{(SRC)}$ = 0 V		0.9	5.36	µA
		$V_{(EN/UVLO)}$ = 0 V, $V_{(SRC)}$ = 0 V, –40°C < T_j < 85°C		0.9	2.65	µA
ENABLE AND UNDERVOLTAGE LOCKOUT (EN/UVLO) INPUT						
$V_{(UVLOR)}$	UVLO threshold voltage, rising		1.16	1.18	1.2	V
$V_{(UVLOF)}$	UVLO threshold voltage, falling		1.1	1.11	1.13	V
$V_{(ENR)}$	Enable threshold voltage for low IQ shutdown, rising				1	V
$V_{(ENF)}$	Enable threshold voltage for low IQ shutdown, falling		0.3			V
$I_{(EN/UVLO)}$	Enable input leakage current	$V_{(EN/UVLO)}$ = 12 V		61	320	nA
OVER VOLTAGE PROTECTION (OV) INPUT - TPS12110-Q1 and TPS12112-Q1 Only						
$V_{(OVR)}$	Overvoltage threshold input, rising	TPS12110-Q1 and TPS12112-Q1 Only	1.16	1.18	1.2	V
$V_{(OVF)}$	Overvoltage threshold input, falling		1.1	1.11	1.13	V
$I_{(OV)}$	OV Input leakage current	0 V < $V_{(OV)}$ < 5 V		60	300	nA
CHARGE PUMP (BST–SRC)						
$I_{(BST)}$	Charge Pump Supply current	$V_{(BST – SRC)}$ = 10 V	80	100	126	µA
$V_{(BST – SRC)}$	Charge Pump Turn ON voltage		11	11.7	12.3	V
	Charge Pump Turn OFF voltage		11.6	12.3	13	V
$V_{(BST\_UVLOR)}$	$V_{(BST – SRC)}$ UVLO voltage threshold, rising		7	7.6	8.1	V
$V_{(BST\_UVLOF)}$	$V_{(BST – SRC)}$ UVLO voltage threshold, falling		6	6.5	6.9	V
$V_{(BST – SRC)}$	Charge Pump Voltage at $V_{(VS)}$ = 3.5 V		8.6			V
GATE DRIVER OUTPUTS (PU, PD, G)						
$R_{(PD)}$	Pull-Down Resistance			0.69	1.34	Ω

6.5 Electrical Characteristics (続き)

T_J = –40°C to +125°C; typical values at T_J = 25°C, $V_{(VS)}$ = $V_{(CS+)}$ = $V_{(CS–)}$ = 12 V, $V_{(BST – SRC)}$ = 12 V, $V_{(SRC)}$ = 0 V, V_{SNS} = Voltage across R_{SNS}

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(PU)}$	Peak Source Current			3.75		A
$I_{(PD)}$	Peak Sink Current			4		A
$I_{(G)}$	Gate charge (sourcing) current, on state	TPS12111-Q1 Only	72	100	140	µA
	Gate discharge (sinking) current, off state		92	131	190	mA
CURRENT SENSE AND OVER CURRENT PROTECTION (CS+, CS–, IMON, ISCP, IWRN)						
$V_{(OS\_SET)}$	Input referred offset (V_{SNS} to $V_{(IMON)}$ scaling)	R_{SET} = 100 Ω, R_{IMON} = 5 kΩ, 10 kΩ (corresponds to V_{SNS} = 6 mV to 30 mV) Gain of 45 and 90 respectively.	–200		200	µV
$V_{(GE\_SET)}$	Gain error (V_{SNS} to $V_{(IMON)}$ scaling)		–1.27		1.27	%
$V_{(IMON\_Acc)}$	IMON accuracy	V_{SNS} = 30 mV, R_{SET} = 100 Ω, R_{IMON} = 10 kΩ	–2		2	%
		V_{SNS} = 6 mV, R_{SET} = 100 Ω, R_{IMON} = 5 kΩ	–5		5	%
$V_{(SNS\_WRN)}$	Overcurrent protection (OCP) voltage threshold	R_{SET} = 100 Ω, R_{IWRN} = 39.7 kΩ	29.2	30.6	31.5	mV
		R_{SET} = 100 Ω, R_{IWRN} = 120 kΩ	8	10	12	mV
$I_{(ISCP)}$	SCP Input Bias current		13.7	15.6	17.6	µA
$V_{(SNS\_SCP)}$	Short-circuit protection (SCP) voltage threshold	R_{ISCP} = 2.1 kΩ	35	40	45	mV
		R_{ISCP} = 750 Ω		19		mV
DELAY TIMER (TMR)						
$I_{(TMR\_SRC\_CB)}$	TMR source current		73	82	91	µA
$I_{(TMR\_SRC\_FLT)}$	TMR source current		2.1	2.5	3.3	µA
$I_{(TMR\_SNK)}$	TMR sink current		2.1	2.5	3	µA
$V_{(TMR\_OC)}$	TMR voltage threshold for over current shutdown		1.112	1.2	1.3	V
$V_{(TMR\_FLT)}$	TMR voltage threshold for $\overline{FLT\_T}$ assertion		1.03	1.1	1.2	V
$V_{(TMR\_LOW)}$	Voltage at TMR pin for AR counter falling threshold		0.15	0.2	0.22	V
INPUT CONTROLS (INP, INP_G), FAULT FLAGS ($\overline{FLT\_I}$, $\overline{FLT\_T}$)						
$R_{(\overline{FLT\_I})}$	$\overline{FLT\_I}$ Pull-down resistance		54	70	90	Ω
$R_{(\overline{FLT\_T})}$	$\overline{FLT\_T}$ Pull-down resistance			70		Ω
$I_{(\overline{FLT\_T})}$	$\overline{FLT}$ Input leakage current				400	nA
$V_{(INP\_H)}$				1.6	2	V
$V_{(INP\_L)}$			0.8	1.2		V
$V_{(INP\_Hys)}$				400		mV
$V_{(INP\_G\_H)}$		TPS12111-Q1 Only		1.6	2	V
$V_{(INP\_G\_L)}$			0.8	1.2		V
$V_{(INP\_G\_Hys)}$				400		mV
TEMPERATURE SENSING AND PROTECTION (DIODE)						
$I_{(DIODE)}$	External diode current source	High level		160		µA
		Low level		10		µA
	Diode current ratio		15.4	16	16.6	A/A
$T_{(DIODE\_TSD\_rising)}$	DIODE sense TSD rising threshold	With MMBT3904 BJT for sensing	140	150	160	°C

6.6 Switching Characteristics

T_J = –40°C to +125°C; typical values at T_J = 25°C, $V_{(VS)}$ = $V_{(CS+)}$ = $V_{(CS–)}$ = 12 V, $V_{(BST – SRC)}$ = 12 V, $V_{(SRC)}$ = 0 V, V_{SNS} = Voltage across R_{SNS}

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PU(INP\_H)}$	INP Turn ON propogation Delay	INP ↑ to PU ↑, C_L = 47 nF		1	2	µs
$t_{PD(INP\_L)}$	INP Turn OFF propogation Delay	INP ↓ to PD ↓, C_L = 47 nF			1	µs
$t_{G(INP\_G\_H)}$	INP_G Turn ON propogation Delay	INP_G ↑ to G ↑, C_L = 1 nF		21		µs
$t_{G(INP\_G\_L)}$	INP_G Turn OFF propogation Delay	INP_G ↓ to G ↓, C_L = 1 nF		0.55	0.8	µs
$t_{PD(EN\_OFF)}$	EN Turn OFF Propogation Delay	EN ↓ to PD ↓, C_L = 47 nF		3.2	5	µs
$t_{PD(UVLO\_OFF)}$	UVLO Turn OFF Propogation Delay	UVLO ↓ to PD ↓, C_L = 47 nF		3.5	6	µs
$t_{PD(VS\_OFF)}$	PD Turn OFF delay during input supply (VS) interruption	VS ↓ $V_{(VS\_PORF)}$ to PD ↓, C_L = 47 nF, INP = EN/UVLO = 2 V		54		µs
$t_{PU(VS\_ON)}$	PU Turn ON delay during input supply (VS) recovery	VS ↑ $V_{(VS\_PORR)}$ to PU ↑, C_L = 47 nF, INP = EN/UVLO = 2 V, $V_{(BST–SRC)}$ > $V_{(BST\_UVLOR)}$		328	465	µs
$t_{PD(OV\_OFF)}$	OV Turn Off progopation Delay	OV ↑ to PD ↓, C_L = 47 nF		2.6	4	µs
t_{SC}	Short-circuit protection propogation Delay	(V_{CS+} – $V_{CS–}$) ↑ $V_{(SNS\_SCP)}$ to PD ↓, C_L = 47 nF, TPS12111-Q1 and TPS12112-Q1 Only		1.16	1.6	µs
	Short-circuit protection propogation Delay	(V_{CS+} – $V_{CS–}$) ↑ $V_{(SNS\_SCP)}$ to PD ↓, C_L = 47 nF, TPS12110–Q1 Only		4	5	µs
t_{OC}	Over current protection delay	(V_{CS+} – $V_{CS–}$) ↑ $V_{(SNS\_WRN)}$ to PD ↓, C_L = 47 nF, C_{TMR} = 0 nF		25	30	µs
	Over current protection delay	(V_{CS+} – $V_{CS–}$) ↑ $V_{(SNS\_WRN)}$ to PD ↓, C_L = 47 nF, C_{TMR} = 22 nF		370		µs
$t_{(\overline{FLT}\_I\_ASSERT)}$	$\overline{FLT}$_I assertion delay	C_{TMR} = 22 nF		340		µs
$t_{(\overline{FLT}\_I\_DEASSERT)}$	$\overline{FLT}$_I de-assertion delay			260		µs
$t_{(\overline{FLT}\_T)AR}$	TSD Auto-retry	TPS12110-Q1 and TPS12112-Q1 Only		512		msec

6.7 Typical Characteristics

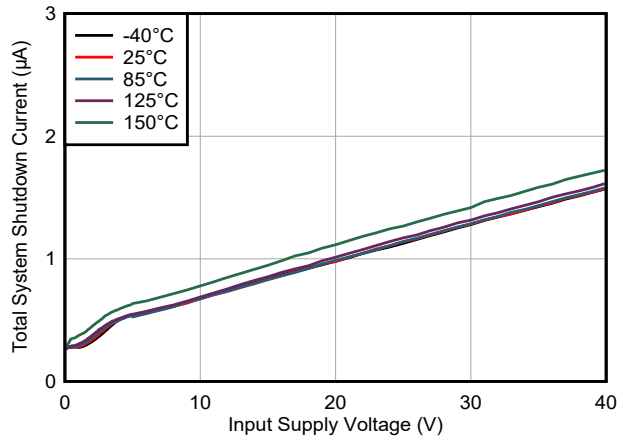

図 6-1. Shutdown Supply Current vs Supply Voltage

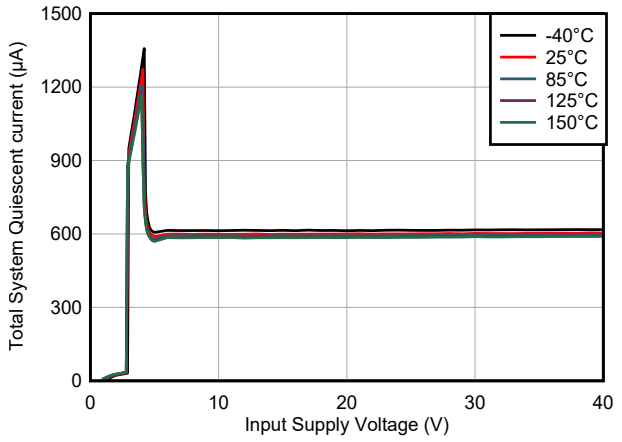

図 6-2. Operating Quiescent Current vs Supply Voltage

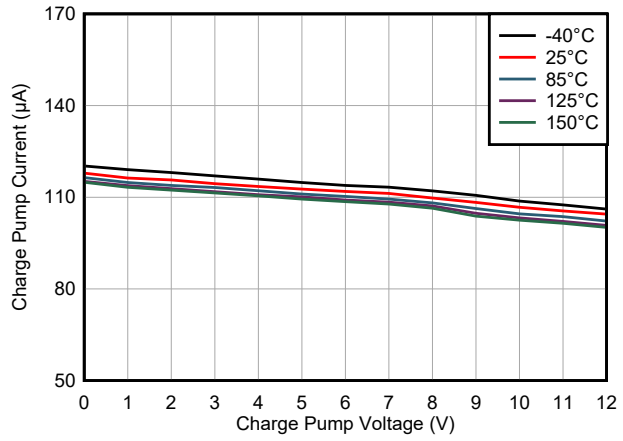

図 6-3. Charge Pump Current vs Charge Pump Voltage

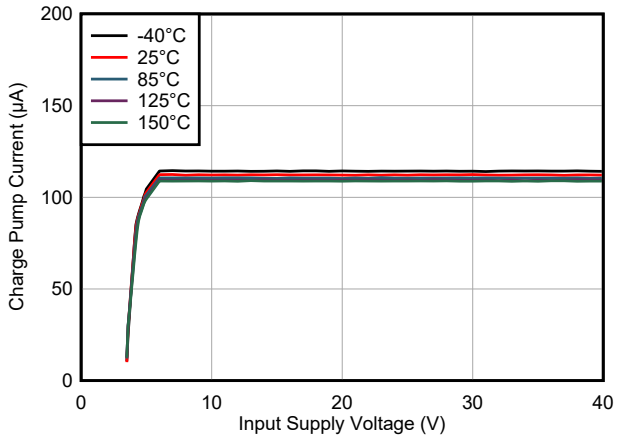

図 6-4. Charge Pump Current vs Input Supply Voltage

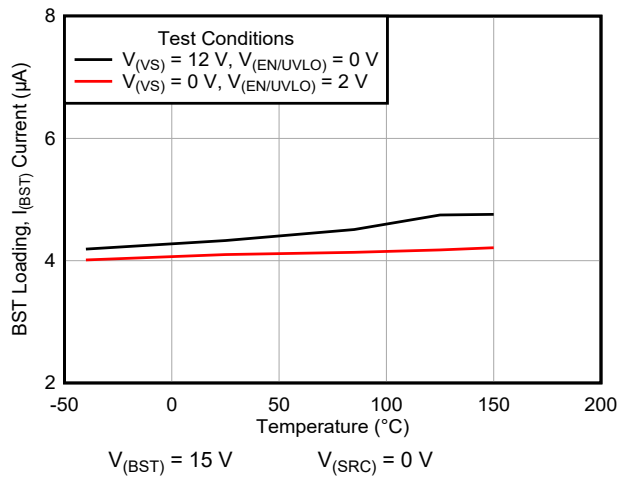

図 6-5. BST Loading Current ($I_{(BST)}$) vs Temperature

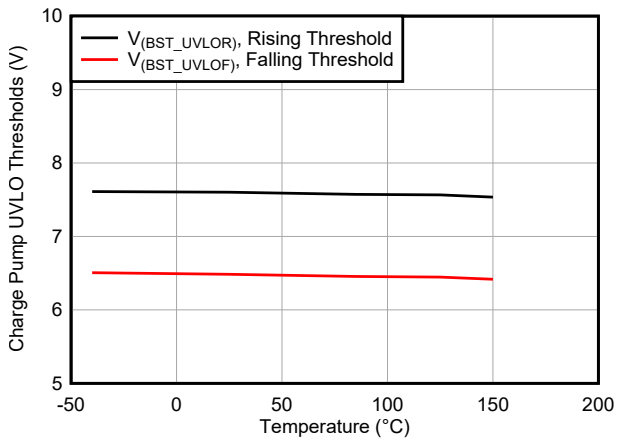

図 6-6. Charge Pump UVLO Thresholds vs Temperature

6.7 Typical Characteristics (continued)

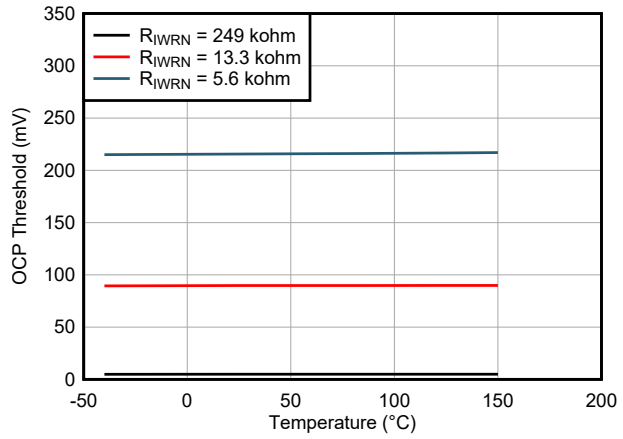

図 6-7. Overcurrent Threshold ($V_{(SNS\_WRN)}$) vs Temperature

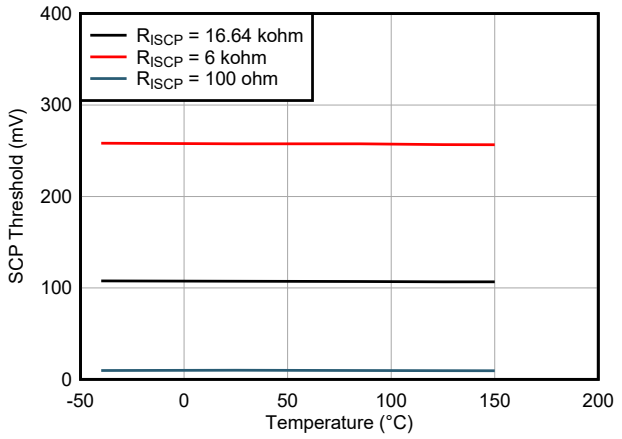

図 6-8. Short-Circuit Threshold ($V_{(SNS\_SCP)}$) vs Temperature

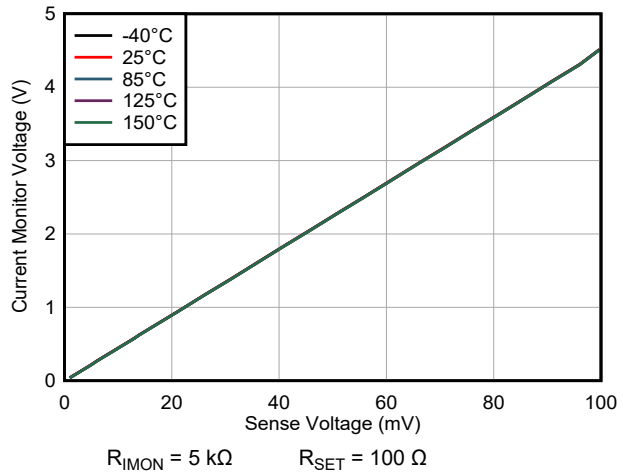

図 6-9. Current Monitor Voltage ($V_{(IMON)}$) vs Sense Voltage (V_{SNS})

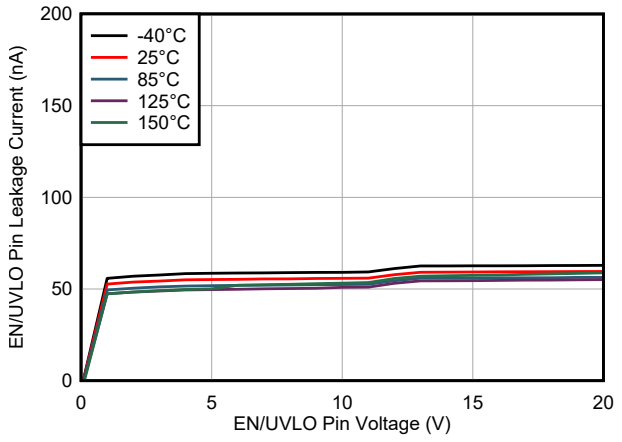

図 6-10. EN/UVLO Pin Voltage vs Leakage Current

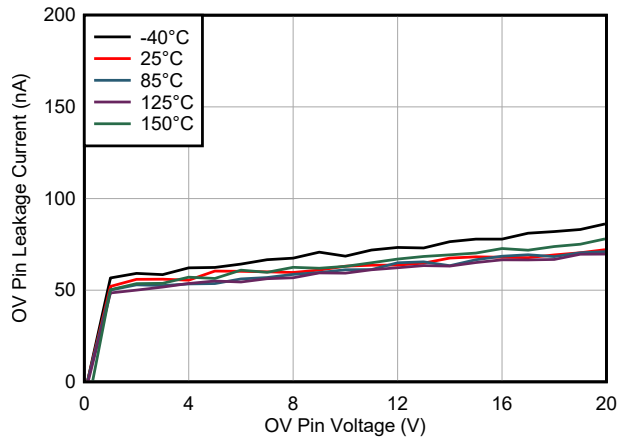

図 6-11. OV Pin Voltage vs Leakage Current

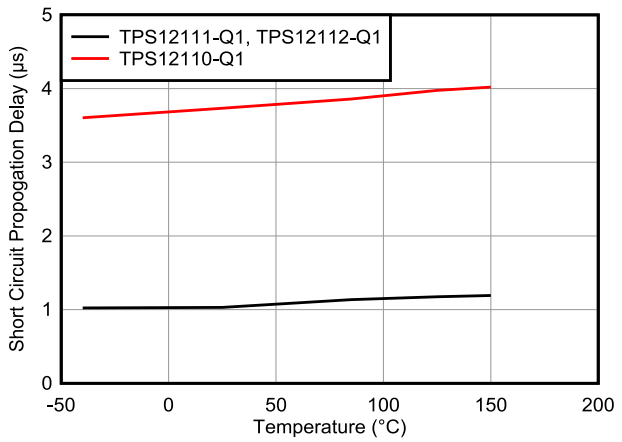

図 6-12. Short Circuit Protection Response Time (t_{SC}) vs Temperature

6.7 Typical Characteristics (continued)

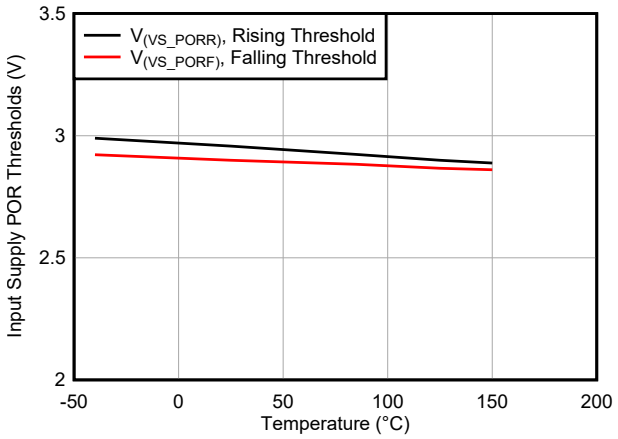

図 6-13. Input Supply POR Thresholds vs Temperature

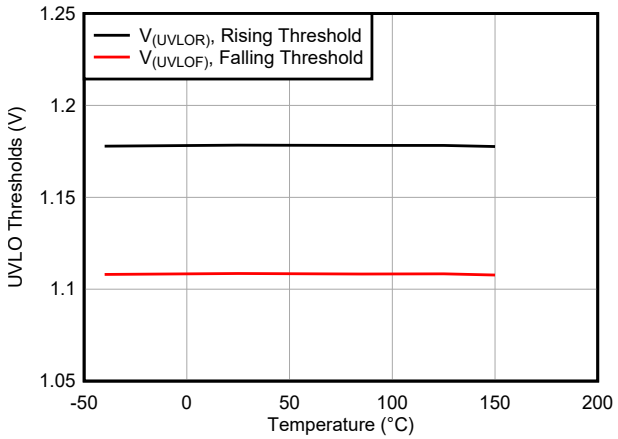

図 6-14. Input Supply UVLO Thresholds vs Temperature

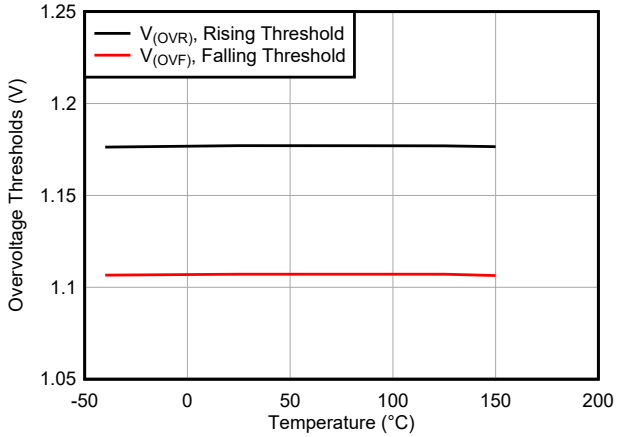

図 6-15. Overvoltage Thresholds vs Temperature

7 Parameter Measurement Information

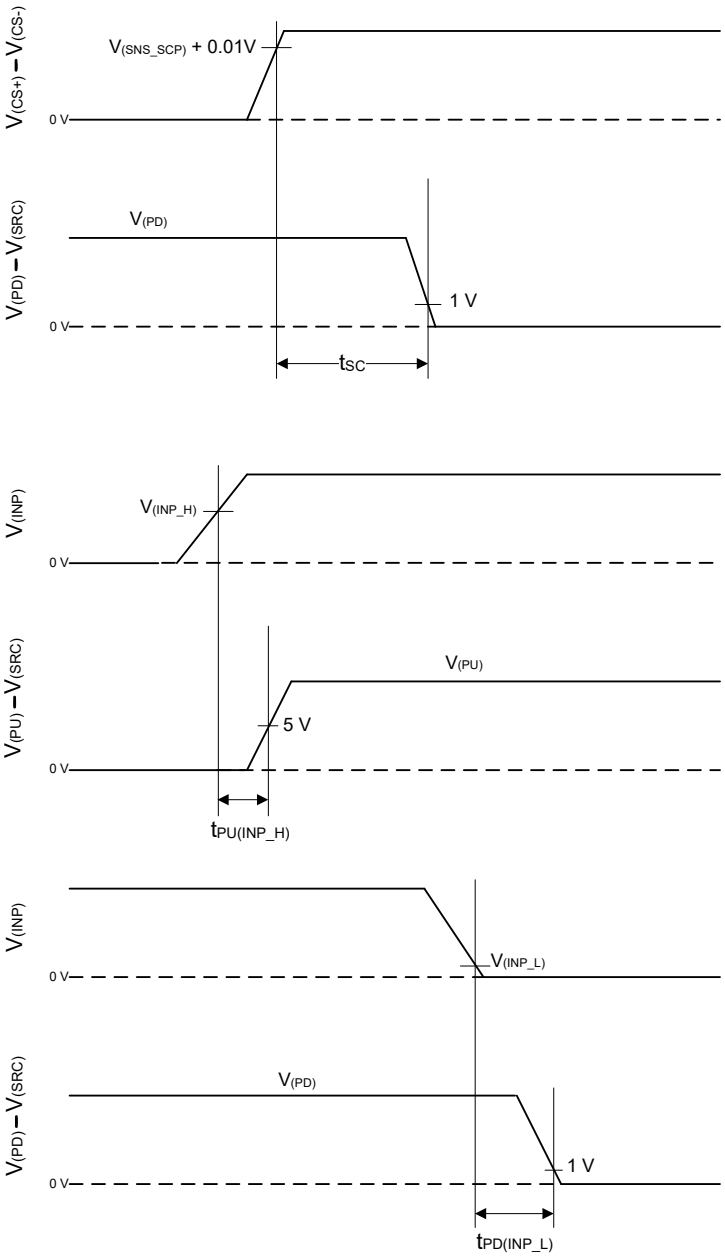

図 7-1. Timing Waveforms

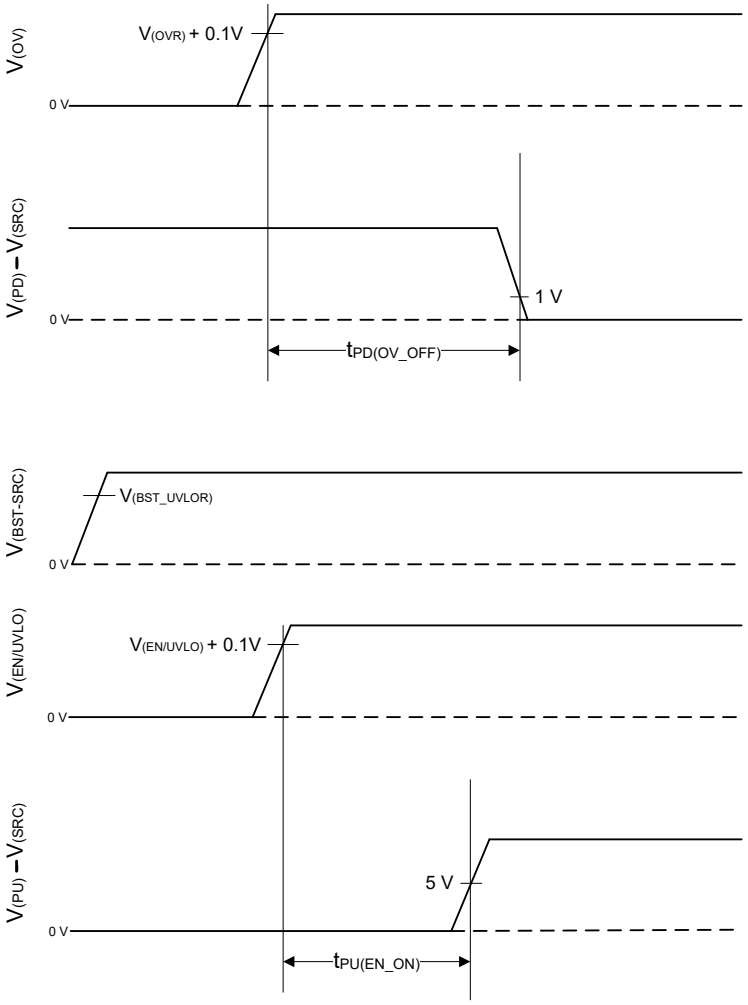

図 7-2. Timing Waveforms

8 Detailed Description

8.1 Overview

The TPS1211-Q1 family is a 45-V smart high-side drivers with protection and diagnostics. With wide operating voltage range of 3.5 V – 40 V, the device is suitable for 12-V system designs.

The device has a strong 3.7-A peak source (PU) and 4-A peak sink (PD) gate driver that enables power switching using parallel FETs in high current system designs. Use INP as the gate driver control input. MOSFET slew rate control (ON and OFF) is possible by placing external R-C components.

The device has accurate current sensing (±2 % at 30 mV) output (IMON) enabling system designs for energy management. The device has integrated two-level, overcurrent protection with $\overline{\text{FLT\_I}}$ output with complete adjustability of thresholds and response time. Auto-retry and latch-off fault behavior can be configured.

The device features remote overtemperature protection with $\overline{\text{FLT\_T}}$ output enabling robust system protection.

TPS12110-Q1 and TPS12112-Q1 have an accurate overvoltage protection (< ±2 %), providing robust load protection.

The TPS12111-Q1 integrates a precharge driver (G) with control input (INP_G). This feature enables system designs that must drive large capacitive loads by precharging first and then turning ON the main power FETs.

TPS1211-Q1 has an accurate undervoltage protection (< ±2 %) using the EN/UVLO pin. Pull EN/UVLO low (< 0.3 V) to turn OFF the device and enter into shutdown mode. In shutdown mode, the controller draws a total shutdown current of 0.9 µA (typical) at 12-V supply input.

8.2 Functional Block Diagram

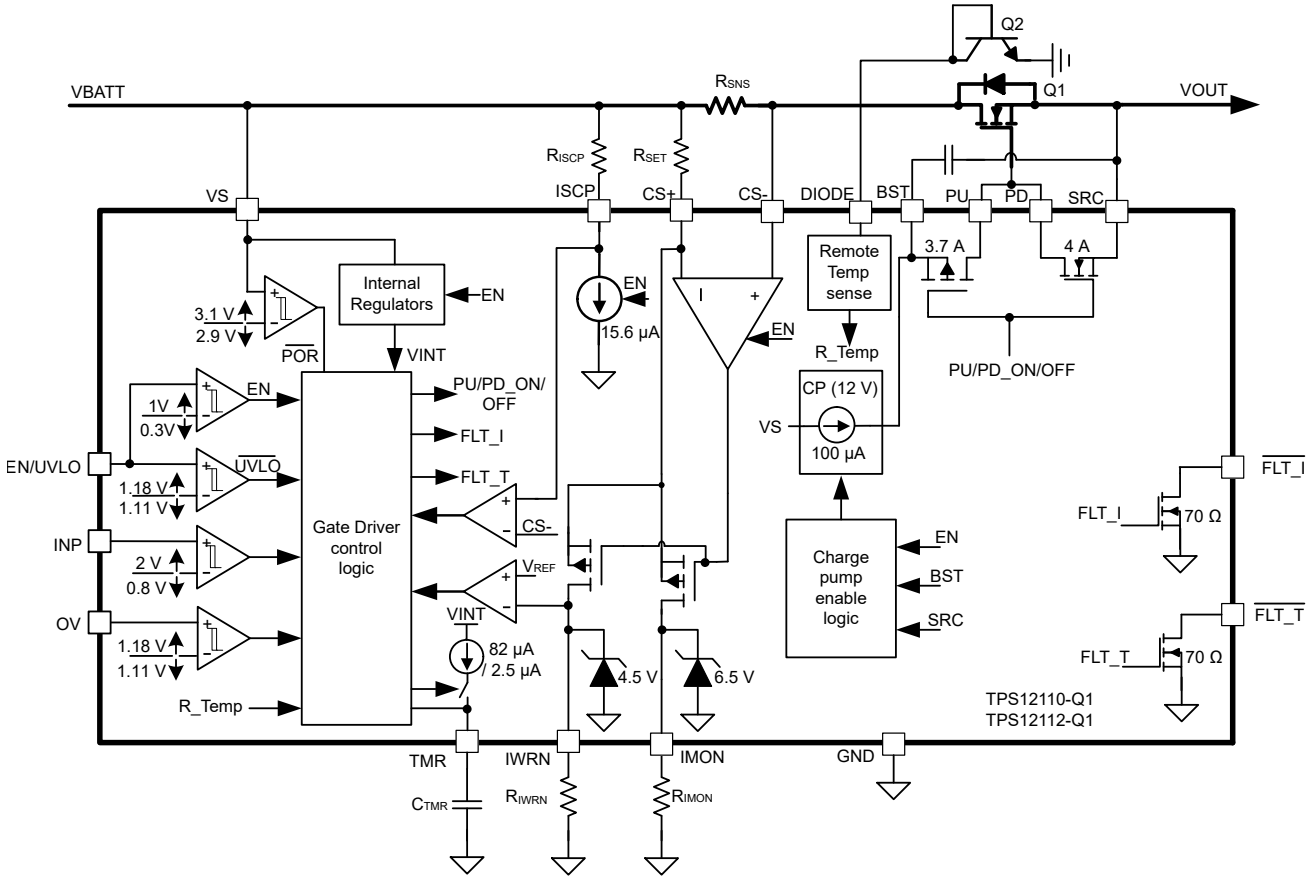

図 8-1. TPS12110-Q1 and TPS12112-Q1 Functional Block Diagram

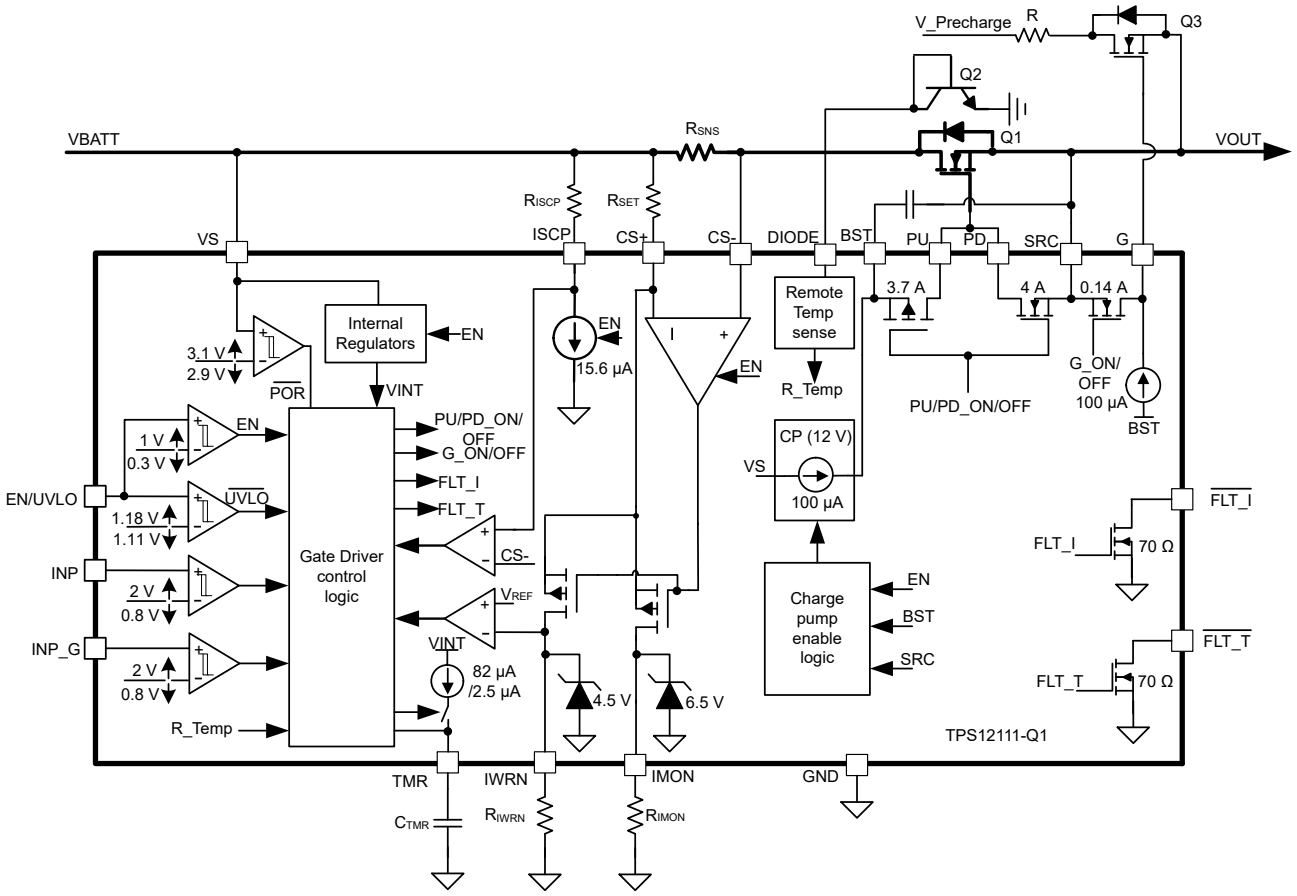

図 8-2. TPS12111-Q1 Functional Block Diagram

8.3 Feature Description

8.3.1 Charge Pump and Gate Driver Output (VS, PU, PD, BST, SRC)

図 8-3 shows a simplified diagram of the charge pump and gate driver circuit implementation. The device houses a strong 3.7-A peak source and 4-A peak sink gate drivers. The strong gate drivers enable paralleling of FETs in high power system designs ensuring minimum transition time in saturation region. A 12-V, 100-µA charge pump is derived from VS terminal and charges the external boot-strap capacitor, C_{BST} that is placed across the gate driver (BST and SRC).

In switching applications, if the charge pump supply demand is higher than 100 µA, then supply BST externally using a low leakage diode and V_{AUX} supply as shown in the 図 8-3.

VS is the supply pin to the controller. With VS applied and EN/UVLO pulled high, the charge pump turns ON and charges the C_{BST} capacitor. After the voltage across C_{BST} crosses $V_{(BST\_UVLOR)}$, the GATE driver section is activated. The device has a 1-V (typical) UVLO hysteresis to ensure chattering less performance during initial GATE turn ON. Choose C_{BST} based on the external FET QG and allowed dip during FET turn-ON. The charge pump remains enabled until the BST to SRC voltage reaches 12.3 V, typically, at which point the charge pump is disabled decreasing the current draw on the VS pin. The charge pump remains disabled until the BST to SRC voltage discharges to 11.7 V typically at which point the charge pump is enabled. The voltage between BST and SRC continue to charge and discharge between 12.3 V and 11.7 V as shown in the 図 8-3.

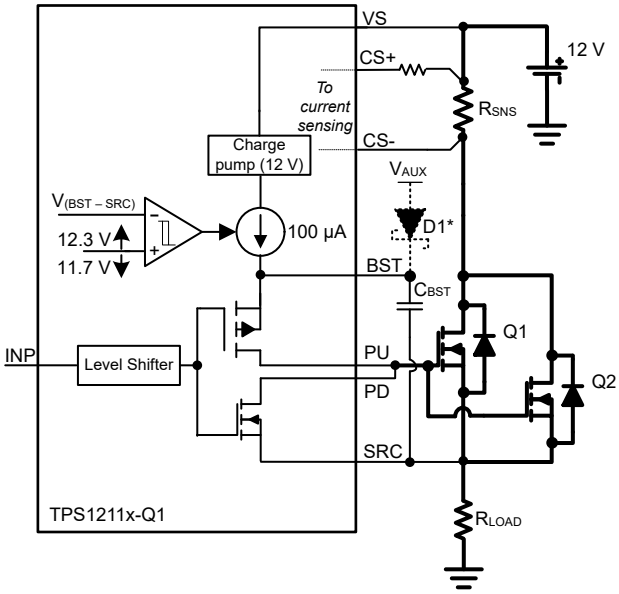

図 8-3. Gate Driver

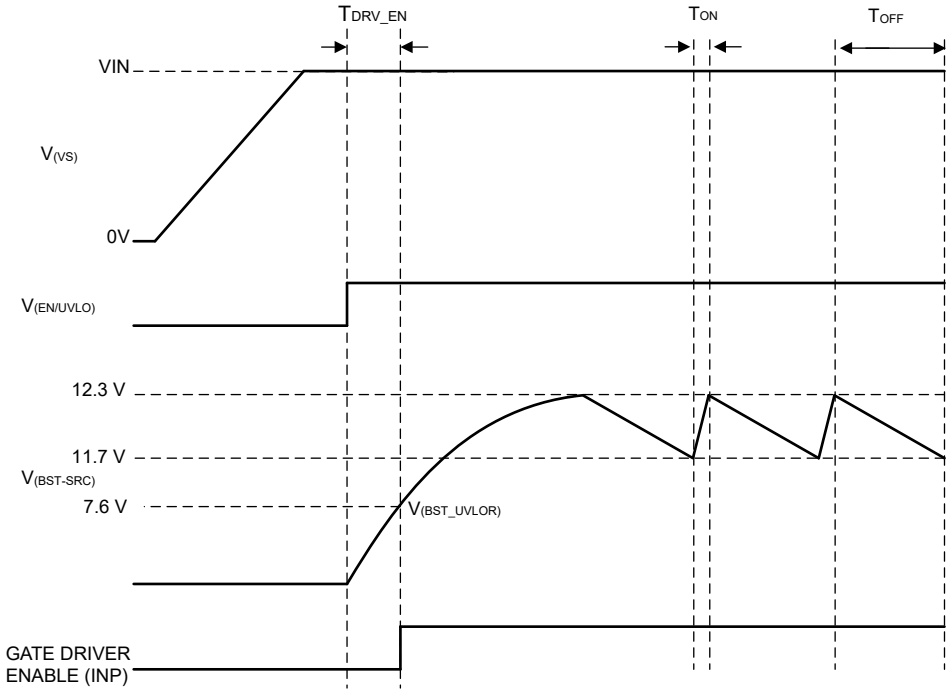

図 8-4. Charge Pump Operation

Use the following equation to calculate the initial gate driver enable delay.

$$T_{DRV\_EN} = \frac{C_{BST} \times V_{(BST\_UVLOR)}}{100\ \mu A} \quad (1)$$

Where,

C_{BST} is the charge pump capacitance connected across BST and SRC pins.

$V_{(BST\_UVLOR)}$ = 7.6 V (typical).

If T_{DRV_EN} must be reduced, then pre-bias the BST terminal externally using an external V_{AUX} supply through a low leakage diode D_1 as shown in 図 8-3. With this connection, T_{DRV_EN} reduces to 350 µs. TPS1211x-Q1 application circuit with external sypply to BST is shown in 図 8-5.

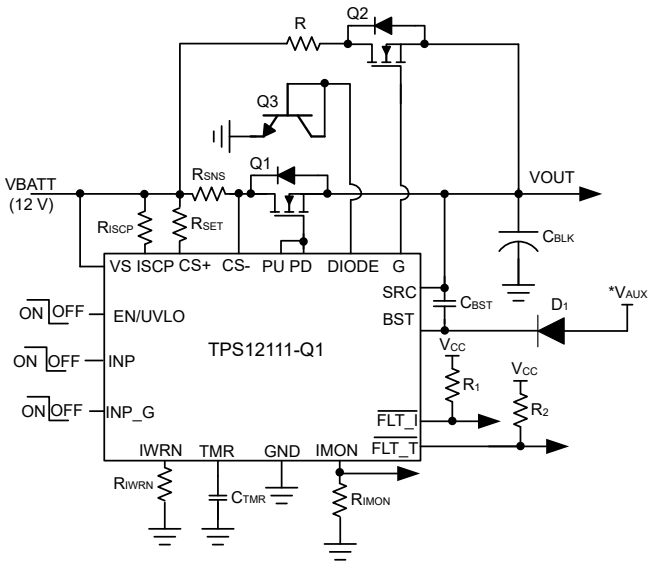

図 8-5. TPS12111-Q1 Application Circuit with external supply to BST

注

V_{AUX} can be supplied by external supply ranging between 8.1 V and 15 V.

8.3.2 Capacitive Load Driving

Certain end equipments like automotive power distribution unit power different loads including other ECUs. These ECUs can have large input capacitances. If power to the ECUs is switched on in uncontrolled way, large inrush currents can occur potentially damaging the power FETs.

To limit the inrush current during capacitive load switching, the following system design techniques can be used with TPS1211x-Q1 devices.

8.3.2.1 FET Gate Slew Rate Control

For limiting inrush current during turn-ON of the FET with capacitive loads, use R_1, R_2, C_1 as shown in 図 8-6. The R_1 and C_1 components slow down the voltage ramp rate at the gate of the FET. The FET source follows the gate voltage resulting in a controlled voltage ramp across the output capacitors.

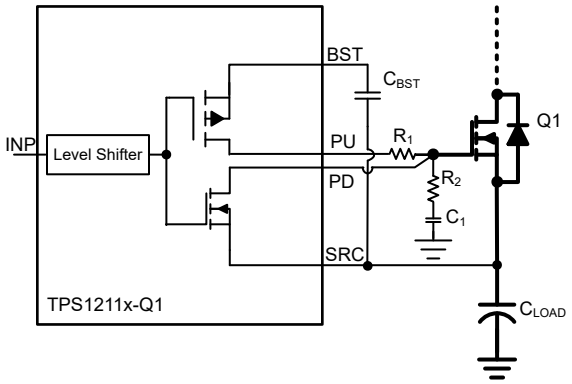

図 8-6. Inrush Current Limiting with FET Gate Slew Rate Control

Use the 式 2 to calculate the inrush current during turn-ON of the FET.

$$I_{INRUSH} = C_{LOAD} \times \frac{V_{BATT}}{T_{charge}} \quad (2)$$

$$I_{INRUSH} = \frac{0.63 \times V_{(BST-SRC)} \times C_{LOAD}}{R_1 \times C_1} \quad (3)$$

Where,

C_{LOAD} is the load capacitance, VBATT is the input voltage and T_{charge} is the charge time, $V_{(BST-SRC)}$ is the charge pump voltage (12 V),

Use a damping resistor R_2 (~ 10 Ω) in series with C_1. 式 3 can be used to compute required C_1 value for a target inrush current. A 100-kΩ resistor for R_1 can be a good starting point for calculations.

Connecting PD pin of TPS1211x-Q1 directly to the gate of the external FET ensures fast turn-OFF without any impact of R_1 and C_1 components.

C_1 results in an additional loading on C_{BST} to charge during turn-ON. Use 式 4 to calculate the required C_{BST} value.

$$C_{BST} > Q_{g(total)} + 10 \times C_1 \quad (4)$$

Where, $Q_{g(total)}$ is the total gate charge of the FET.

8.3.2.2 Using Precharge FET - (with TPS12111-Q1 Only)

In high-current applications where several FETs are connected in parallel, the gate slew rate control for the main FETs is not recommended due to unequal distribution of inrush currents among the FETs. This action makes FET selection complex and results in over sizing of the FETs.

The TPS12111-Q1 integrates precharge gate driver (G) with a dedicated control input (INP_G). This feature can be used to drive a separate FET that can be used to precharge the capacitive load. 図 8-7 shows the precharge FET implementation for capacitive load charging using TPS12111-Q1. An external capacitor C_g reduces the gate turn-ON slew rate and controls the inrush current.

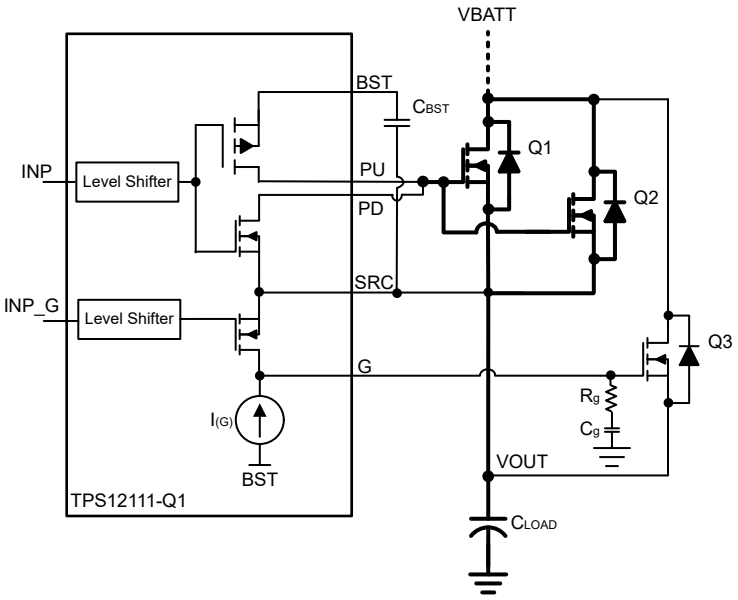

図 8-7. Capacitor Charging Using Gate Slew Rate Control of Precharge FET

During power up with EN/UVLO high and C_{BST} voltage above $V_{(BST\_UVLOR)}$ threshold, INP and INP_G controls are active. For the precharge functionality, drive INP low to keep the main FETs OFF and drive INP_G high. G output gets pulled up to BST with $I_{(G)}$. Use 式 5 to calculate the required C_g value.

$$C_g = \frac{C_{LOAD} \times I_{(G)}}{I_{INRUSH}} \quad (5)$$

Where,

$I_{(G)}$ is 100 µA (typical),

Use 式 2 to calculate the I_{INRUSH}.

A series resistor R_g must be used in conjunction with C_g to limit the discharge current from C_g during turn-off . The recommended value for Rg is between 220 Ω to 470 Ω. After the output capacitor is charged, turn OFF the precharge FET by driving INP_G low. G gets pulled low to SRC with an internal 135-mA pulldown switch. The main FETs can be turned ON by driving INP high.

図 8-8 shows other system design approaches to charge large output capacitors in high current applications. The designs involve an additional power resistor in series in series with precharge FET. The back-to-back FET topology shown is typically used in bi-directional power control applications like battery management systems.

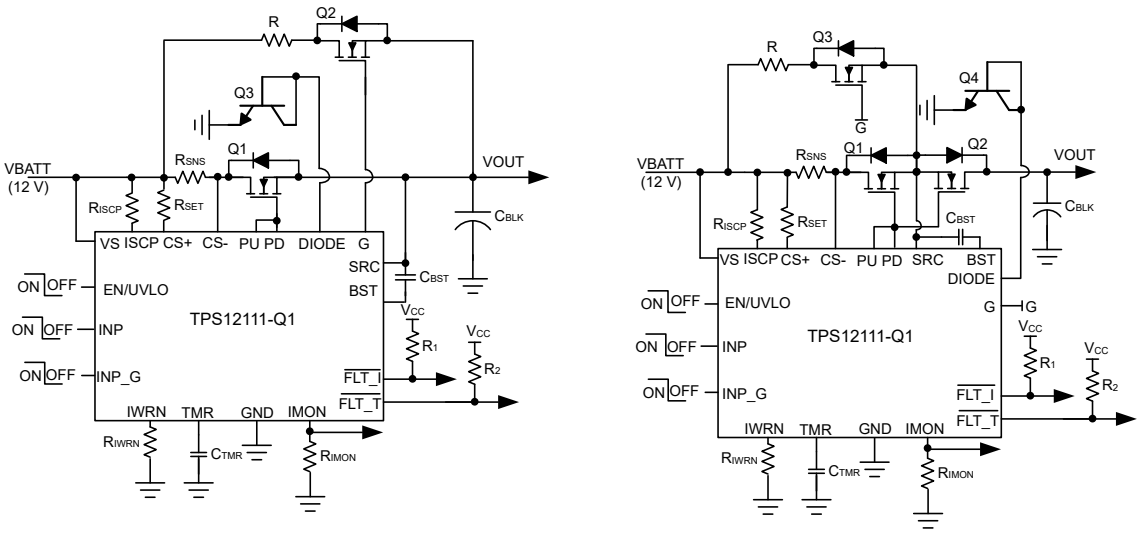

図 8-8. TPS12111-Q1 application Circuits for Capacitive Load Driving Using Precharge FET and a Series Power Resistor

8.3.3 Overcurrent and Short-Circuit Protection

TPS1211x-Q1 has two-level current protection.

- Adjustable overcurrent protection (I_{OC}) threshold and response time (t_{OC}),
- Adjustable short-circuit threshold (I_{SC}) with internally fixed fast response (t_{SC}).

図 8-9 shows the I-T characteristics.

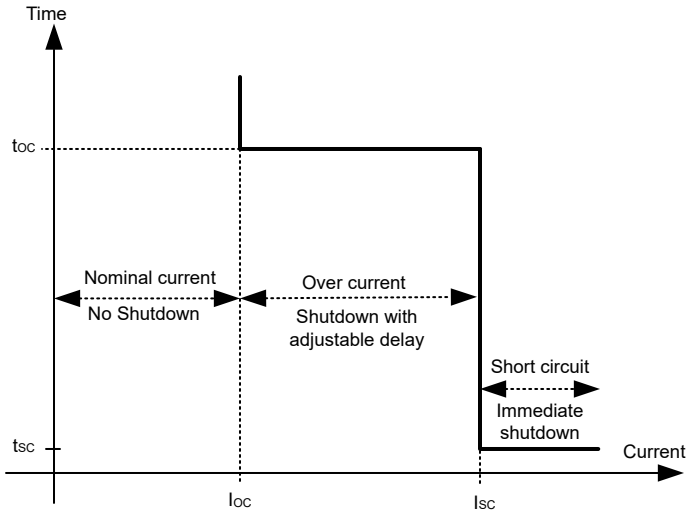

図 8-9. Overcurrent and Short-Circuit Protection Characteristics

The device senses the voltage across the external current sense resistor through CS+ and CS−. Set the overcurrent protection threshold using an external resistor R_{IWRN} across IWRN and GND. Use 式 6 to calculate the required R_{IWRN} value.

$$R_{IWRN}\ (\Omega) = \frac{11.9 \times R_{SET}}{R_{SNS} \times I_{OC}} \quad (6)$$

Where, R_{SET} is the resistor connected across CS+ and VS, R_{SNS} is the current sense resistor and I_{OC} is the overcurrent level.

注

For short-circuit protection feature only, connect IWRN pin to GND and select R_{ISCP} resistor as per セクション 8.3.3.3.

For overcurrent protection feature only, connect ISCP pin to CS– pin directly and select R_{IWRN} resistor as per 式 6.

In case of overcurrent or short-circuit event, TPS12111-Q1 controller turns off main FET by pulling PD low but state of pre-charge FET drive (G) is not changed.

8.3.3.1 *Overcurrent Protection with Auto-Retry*

The C_{TMR} programs the over current protection delay (t_{OC}) and auto-retry time (t_{RETRY}). Once the voltage across CS+ and CS– exceeds the set point, the C_{TMR} starts charging with 82-µA pullup current. After the C_{TMR} charges up to $V_{(TMR\_FLT)}$, $\overline{FLT\_I}$ asserts low providing warning on impending FET turn OFF. After C_{TMR} charges to $V_{(TMR\_OC)}$, PD pulls low to SRC turning OFF the FET. Post this event, the auto-retry behavior starts. The C_{TMR} capacitor starts discharging with 2.5-uA pulldown current. After the voltage reaches $V_{(TMR\_LOW)}$ level, the capacitor starts charging with 2.5-uA pullup. After 32 charging, discharging cycles of C_{TMR} the FET turns ON back and $\overline{FLT\_I}$ de-asserts after de-assertion delay of 260 µs.

Use 式 7 to calculate the C_{TMR} capacitor to be connected between TMR and GND.

$$C_{TMR} = \frac{I_{TMR} \times t_{OC}}{1.2} \quad (7)$$

Where, I_{TMR} is internal pull-up current of 82-µA, t_{OC} is desired overcurrent response time.

Use 式 8 to calculate the T_{FLT} duration.

$$T_{FLT} = \frac{1.1 \times C_{TMR}}{82\ \mu} \quad (8)$$

Where, T_{FLT} is the $\overline{FLT\_I}$ assertion delay.

The auto-retry time can be computed as, $t_{RETRY} = 22.7 \times 10^6 \times C_{TMR}$.

If the overcurrent pulse duration is below t_{OC}, then the FET remains ON and C_{TMR} gets discharged using internal pulldown switch.

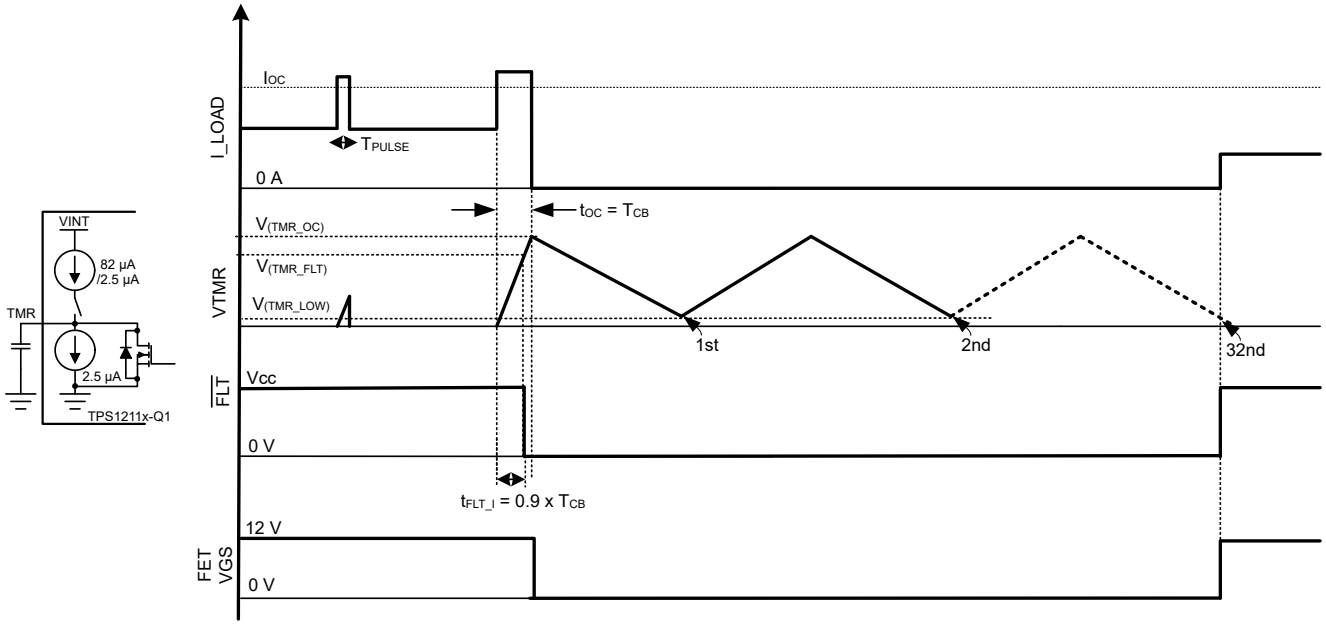

図 8-10. *Overcurrent Protection with Auto-Retry*

8.3.3.2 *Overcurrent Protection with Latch-Off*

Connect an approximately 100-kΩ resistor across C_{TMR} as shown in the following figure. With this resistor, during the charging cycle, the voltage across C_{TMR} gets clamped to a level below $V_{(TMR\_OC)}$ resulting in a latch-off behavior.

Use 式 9 to calculate C_{TMR} capacitor to be connected between TMR and GND for R_{TMR} = 100-kΩ.

$$C_{TMR} = \frac{t_{OC}}{R_{TMR} \times \ln\left(\frac{1}{1 - \frac{1.2}{R_{TMR} \times I_{TMR}}}\right)} \quad (9)$$

Where, I_{TMR} is internal pull-up current of 82-µA, t_{OC} is desired overcurrent response time.

Toggle INP or EN/UVLO (below ENF) or power cycle VS below $V_{(VS\_PORF)}$ to reset the latch. At low edge, the timer counter is reset and C_{TMR} is discharged. PU pulls up to BST when INP is pulled high.

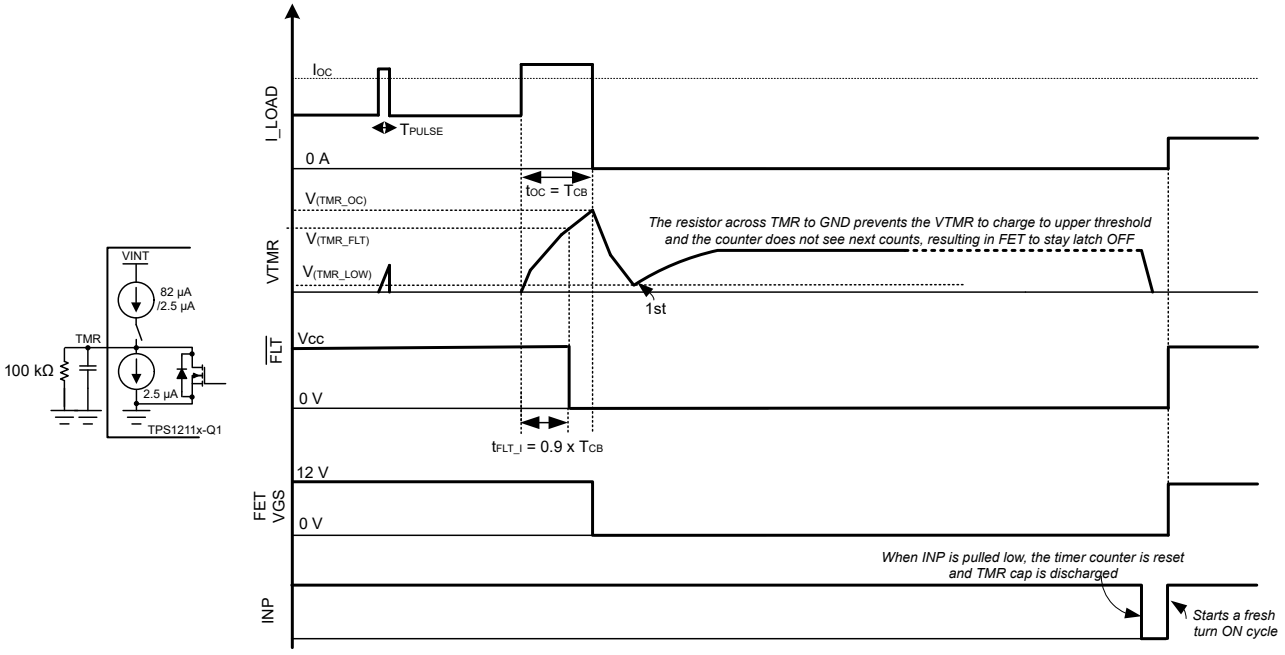

図 8-11. *Overcurrent Protection with Latch-Off*

8.3.3.3 Short-Circuit Protection

Connect a resistor, R_{ISCP}, as shown in 図 8-12.

Use 式 10 to calculate the required R_{ISCP} value.

$$R_{ISCP}\left(\Omega\right) = \frac{I_{SC} \times R_{SNS}}{15.6\ \mu} - 600 \tag{10}$$

Where, R_{SNS} is the current sense resistor, and I_{SC} is the desired short-circuit protection level. After the current exceeds the I_{SC} threshold then, PD pulls low to SRC within 1.2 µs in TPS12111-Q1, TPS12112-Q1 and 4 µs in TPS12110-Q1, protecting the FET. $\overline{FLT\_I}$ asserts low at the same time. Subsequent to this event, the charge and discharge cycles of C_{TMR} starts similar to the behavior post FET OFF event in the over current protection scheme.

Latch-off can also achieved in the similar way as explained in the overcurrent protection scheme.

> **注**
>
> Connect IWRN pin to GND if only short-circuit protection is required. R_{ISCP} resistor can be selected as per セクション 8.3.3.3.

8.3.4 Analog Current Monitor Output (IMON)

TPS1211x-Q1 features an accurate analog load current monitor output (IMON) with adjustable gain. The current source at IMON terminal is configured to be proportional to the current flowing through the R_{SNS} current sense resistor. This current can be converted to a voltage using a resistor R_{IMON} from IMON terminal to GND terminal. This voltage, computed using 式 11 can be used as a means of monitoring current flow through the system.

Use 式 11 to calculate the $V_{(IMON)}$.

$$V_{(IMON)} = \left(V_{SNS} + V_{(OS\_SET)}\right) \times \text{Gain} \tag{11}$$

Where V_{SNS} = I_LOAD × R_{SNS} and $V_{(OS\_SET)}$ is the input referred offset (± 200 µV) of the current sense amplifier (V_{SNS} to $V_{(IMON)}$ scaling). Use the following equation to calculate gain.

$$\text{Gain} = \frac{0.9 \times R_{IMON}}{R_{SET}} \tag{12}$$

Where 0.9 is the current mirror factor between the current sense amplifier and the IMON pass FET.

The maximum voltage range for monitoring the current ($V_{(IMONmax)}$) is limited to minimum([$V_{(VS)}$ – 0.5V], 5.5V) to ensure linear output. This puts limitation on maximum value of R_{IMON} resistor. The IMON pin has an internal clamp of 6.5 V (typical).

Accuracy of the current mirror factor is < ± 1%. Use the following equation to calculate the overall accuracy of $V_{(IMON)}$.

$$\%\, V_{(IMON)} = \frac{V_{(OS\_SET)}}{V_{SNS}} \times 100 \tag{13}$$

図 8-12 shows external connections and simplified block diagram of current sensing and overcurrent protection implementation.

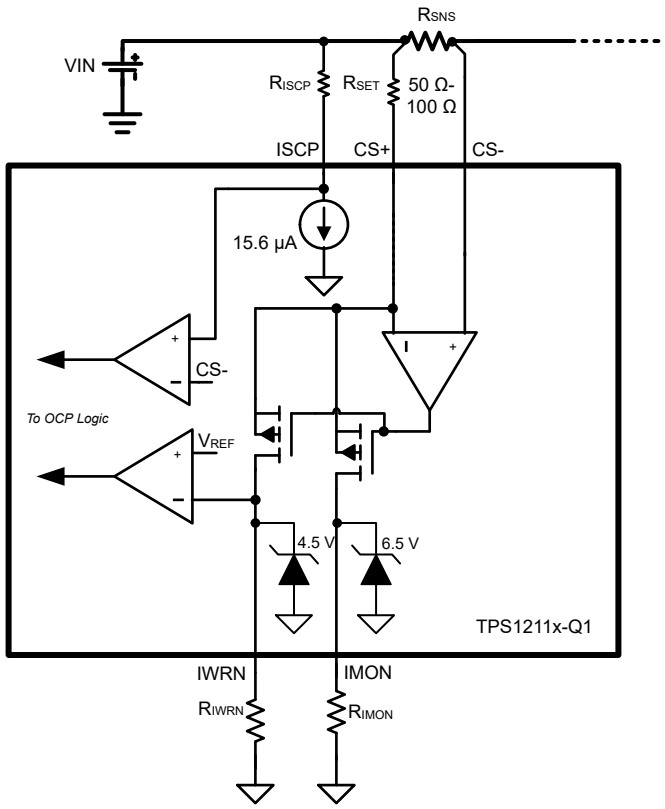

図 8-12. Current Sensing and Overcurrent Protection

In TPS12110-Q1 and TPS12111-Q1, IMON amplifer output is turned OFF when PD is pulled low to SRC (due to INP pulled low or fault event) whereas IMON output remains enabled in TPS12112-Q1 even if PD is pulled low to SRC. In TPS12112-Q1, IMON output gets disabled only when the device is disabled by pulling EN/UVLO low below $V_{(ENF)}$ or $V_{(VS)}$ below $V_{(VS\_PORF)}$.

TPS12112-Q1 can be used in applications where grouped IMON output is desired as shown in 図 8-13:

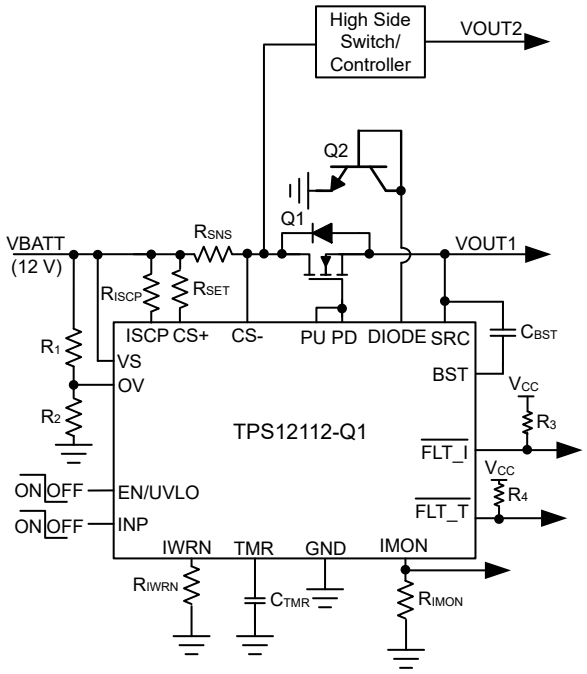

図 8-13. TPS12112-Q1 Application Circuit with Grouped IMON Output

8.3.5 Overvoltage (OV) and Undervoltage Protection (UVLO)

TPS1211x-Q1 has an accurate undervoltage protection (< ±2 %) using EN/UVLO pin.

TPS12110-Q1 and TPS12112-Q1 have an accurate overvoltage protection (< ±2 %), providing robust load protection. Connect a resistor ladder as shown in 図 8-14 for undervoltage and overvoltage protection threshold programming.

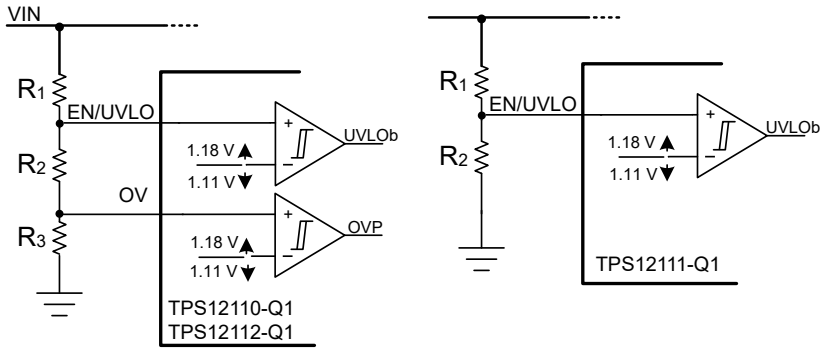

図 8-14. Programming Overvoltage and Undervoltage Protection Threshold

8.3.6 Remote Temperature Sensing and Protection (DIODE)

The device features an integrated remote temperature sensing, protection and dedicated fault output. In TPS1211x-Q1, remote temperature measurement is done by using transistor in diode configuration. Connect the

DIODE pin of TPS1211x-Q1 to the collector and base of a MMBT3904 BJT. The temperature is calculated internally based on difference of measured diode voltages at two test currents.

In TPS12110-Q1 and TPS12112-Q1, after the sensed temperature reaches approximately 150ºC, the device pulls PD low to SRC, turning off the external FET and also asserts $\overline{\text{FLT\_T}}$ low. After the temperature reduces to 130ºC, an internally fixed auto-retry cycle of 512 ms commences. $\overline{\text{FLT\_T}}$ de-asserts and the external FET turns ON after the retry duration of 512 ms is lapsed.

In TPS12111-Q1, after the sensed temperature crosses 150°C, PD and G get pulled low to SRC. After the TSD hysteresis, PU and G stays latched OFF. The latch gets reset by toggling EN/UVLO below $V_{(ENF)}$ or by power cycling VS below $V_{(VS\_PORF)}$.

図 8-15 shows simplified block diagram of TPS1211x-Q1 DIODE based remote temperature sensing.

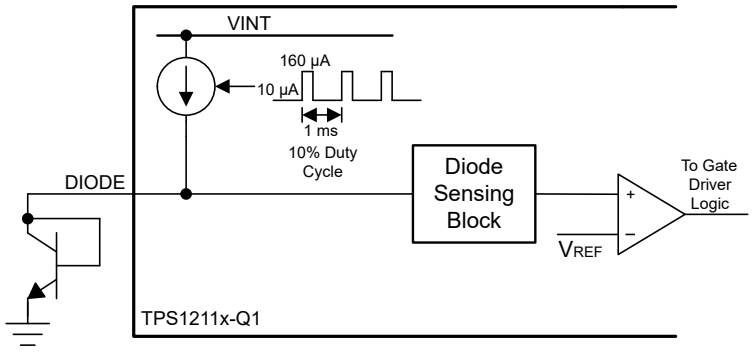

図 8-15. DIODE based Remote Temperature Sensing Block Diagram

8.3.7 Output Reverse Polarity Protection

The TPS1211x-Q1 withstands output reverse voltages down to -30 V. With INP low, PD is pulled low to SRC and keeps the external FET OFF even with output (SRC) voltage at negative levels preventing high current flow and protecting the main FET. Refer to 図 8-16 and 図 8-17 for test waveforms.

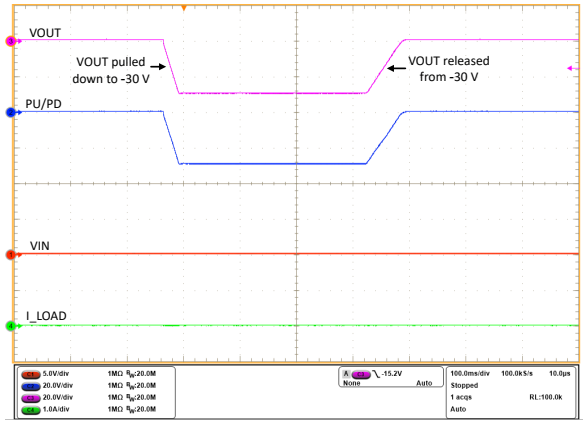

図 8-16. Output Short to -30 V Response with VIN = 0 V and INP = LOW

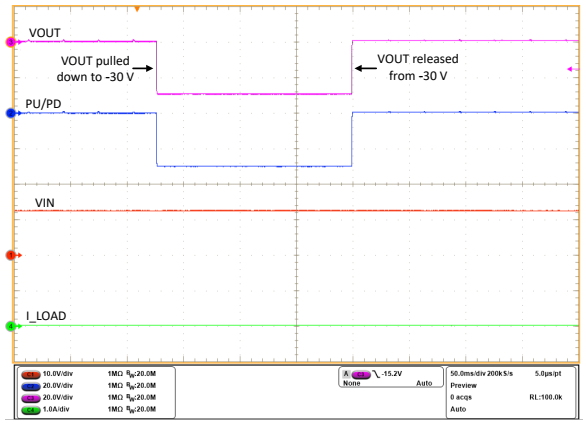

図 8-17. Output Short to -30 V Response with VIN = 12 V and INP = LOW

8.3.8 TPS1211x-Q1 as a Simple Gate Driver

図 8-18 shows application schematics of TPS1211x-Q1 as a simple gate driver in load disconnect switch as well as back-to-back FETs driving topologies. The protection features like two-level overcurrent protection, overvoltage protection, and overtemperature protection are disabled.

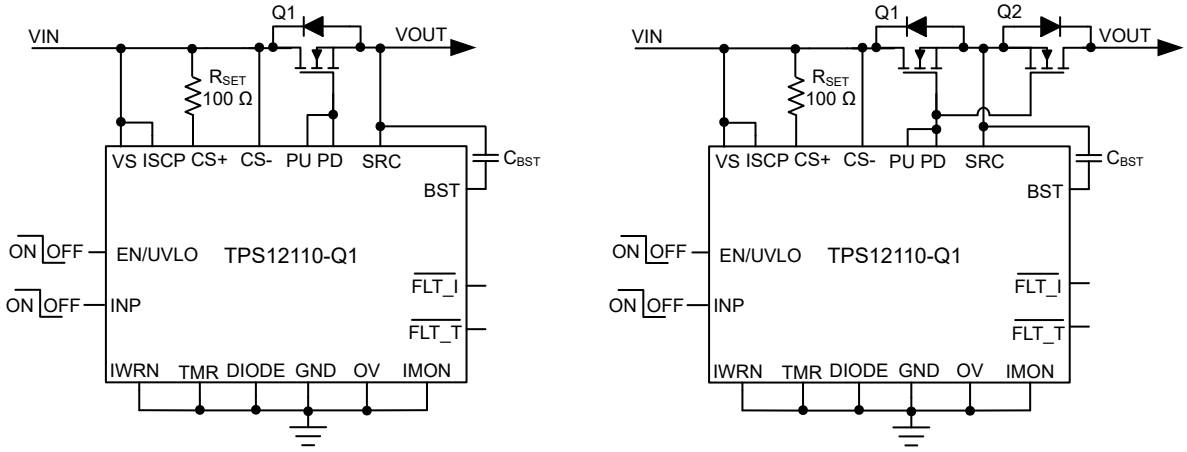

図 8-18. Connection Diagram of TPS12110-Q1 for Simple Gate Driver Design

8.4 Device Functional Modes

The TPS1211-Q1 has two modes of operation. Active mode and low IQ shutdown mode. If the EN/UVLO pin voltage is greater than the rising threshold, then the device is in active mode. In active state the internal charge pump is enabled, gate drivers and all the protection and diagnostic features are enabled.

If the EN/UVLO voltage is pulled < $V_{(ENF)}$, the device enters into low IQ shutdown mode. In this mode, the charge pump, gate drivers and all the protection features are disabled. The external FETs turn OFF. The TPS1211-Q1 consumes low IQ of 0.9 µA (typical) in this mode.

9 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

The TPS1211x-Q1 family is a 45-V smart high-side driver with protection and diagnostics. The TPS1211x-Q1 device controls external N-channel MOSFETs and its drive architecture is suitable to drive back-to-back N-Channel MOSFETs. The strong gate 3.7-A peak source and 4-A peak sink capabilities enable switching parallel MOSFETs in high current applications such as circuit breaker in powertrain (DC/DC converter), driving loads in power distribution unit, electric power steering, driving PTC heater loads, and so forth. The TPS1211x-Q1 device provides two-level, adjustable, overcurrent protection with adjustable circuit breaker timer, fast short-circuit protection, accurate analog current monitor output, and remote overtemperature protection.

The variant TPS12111-Q1 features a separate precharge driver (G) with independent control input (INP_G). This feature enables system designs that must precharge the large output capacitance before turning ON the main power path.

The following design procedure can be used to select the supporting component values based on the application requirement. Additionally, a spreadsheet design tool TPS1211-Q1 Design Calculator is available in the web product folder.

9.2 Typical Application: Driving Zonal Controller Loads on 12-V Line in Power Distribution Unit

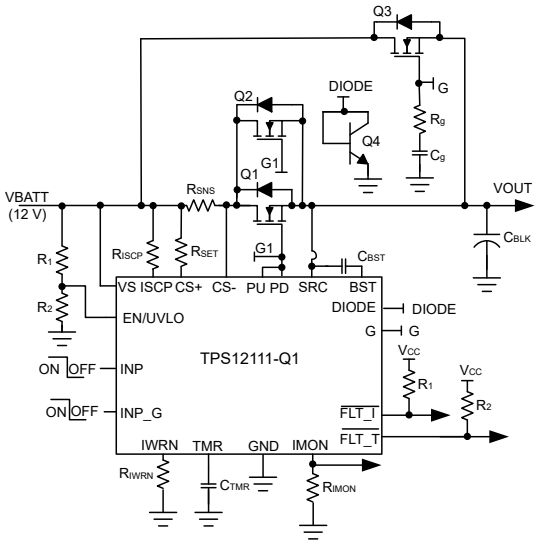

図 9-1. Typical Application Schematic: Driving Zonal Controller Loads with Precharging the Output Capacitance

9.2.1 Design Requirements

表 9-1 shows the design parameters for this application example.

表 9-1. Design Parameters

PARAMETER	VALUE
Typical input voltage, V_{IN}	12 V
Undervoltage lockout set point, VIN_{UVLO}	6.5 V
Maximum load current, I_{OUT}	25 A
Overcurrent protection threshold, I_{OC}	30 A
Short-circuit protection threshold, I_{SC}	35 A
Fault timer period (t_{OC})	1 ms
Fault response	Auto-retry
Load capacitance, C_{OUT}	1 mF
Charging time, T_{start}	10 ms

9.2.2 Detailed Design Procedure

Selection of Current Sense Resistor, R_{SNS}

The recommended range of the overcurrent protection threshold voltage, $V_{(SNS\_WRN)}$, extends from 10 mV to 200 mV. Values near the low threshold of 10 mV can be affected by the system noise. Values near the upper threshold of 200 mV can cause high power dissipation in the current sense resistor. To minimize both the concerns, 25 mV is selected as the overcurrent protection threshold voltage. Use the following equation to calculate the current sense resistor, R_{SNS}.

$$R_{SNS} = \frac{V_{(SNS\text{-}WRN)}}{I_{OC}} = \frac{25\ mV}{30\ A} = 833\ \mu\Omega \quad (14)$$

The next smaller available sense resistor 800 µΩ, 1% is chosen.

To improve signal to noise ratio or for better overcurrent protection accuracy, higher overcurrent protection threshold voltage, $V_{(SNS\_WRN)}$ can be selected.

Selection of Scaling Resistor, R_{SET}

R_{SET} is the resistor connected between VS and CS+ pins. This resistor scales the overcurrent protection threshold voltage and coordinates with R_{IWRN} and R_{IMON} to determine the overcurrent protection threshold and current monitoring output. The recommended range of R_{SET} is 50 Ω – 100 Ω.

R_{SET} is selected as 100 Ω, 1% for this design example.

Programming the Overcurrent Protection Threshold – R_{IWRN} Selection

The R_{IWRN} sets the overcurrent protection threshold, whose value can be calculated using 式 15.

$$R_{IWRN}\ (\Omega) = \frac{11.9 \times R_{SET}}{R_{SNS} \times I_{OC}} \quad (15)$$

To set 30 A as overcurrent protection threshold, R_{IWRN} value is calculated to be 49.5 kΩ.

Choose the closest available standard value: 49.9 kΩ, 1%

.

Programming the Short-Circuit Protection Threshold – R_{ISCP} Selection

The R_{ISCP} sets the short-circuit protection threshold. Use the following equation to calculate the value.

$$R_{ISCP}\left(\Omega\right) = \frac{I_{SC} \times R_{SNS}}{15.6\,\mu} - 600 \quad (16)$$

To set 35 A as short-circuit protection threshold, R_{ISCP} value is calculated to be 1.19 kΩ.

Choose the closest available standard value: 1.2 kΩ, 1%.

In case where large di/dt is involved, the system and layout parasitic inductances can generate large differential signal voltages between ISCP and CS– pins. This action can trigger false short-circuit protection and nuisance trips in the system. To overcome such scenario, TI recommends to add filter capacitor of 1 nF across ISCP and CS– pins close to the device. Because nuisance trips are dependent on the system and layout parasitics, TI recommends to test the design in a real system and tweaked as necessary.

Programming the Fault timer Period – C_{TMR} Selection

For the design example under discussion, overcurrent transients are allowed for 1-ms duration. This blanking interval, t_{OC} can be set by selecting appropriate capacitor C_{TMR} from TMR pin to ground. Use the following equation to calculate the value of C_{TMR} to set 1 ms for t_{OC}.

$$C_{TMR} = \frac{82\,\mu \times t_{OC}}{1.2} = 68.33\ \text{nF} \quad (17)$$

Choose closest available standard value: 68 nF, 10%.

Selection of MOSFETs, Q_1 and Q_2

For selecting the MOSFET Q_1, important electrical parameters are the maximum continuous drain current I_D, the maximum drain-to-source voltage $V_{DS(MAX)}$, the maximum drain-to-source voltage $V_{GS(MAX)}$, and the drain-to-source ON-resistance R_{DSON}.

The maximum continuous drain current, I_D, rating must exceed the maximum continuous load current.

The maximum drain-to-source voltage, $V_{DS(MAX)}$, must be high enough to withstand the highest voltage seen in the application. Considering 35 V as the maximum application voltage, MOSFETs with V_{DS} voltage rating of 40 V is suitable for this application.

The maximum V_{GS} TPS1211-Q1 can drive is 13 V, so a MOSFET with 15-V minimum V_{GS} rating must be selected.

To reduce the MOSFET conduction losses, lowest possible $R_{DS(ON)}$ is preferred.

Based on the design requirements, BUK7S0R5-40HJ is selected and its ratings are:

- 40-V $V_{DS(MAX)}$ and 20-V $V_{GS(MAX)}$
- $R_{DS(ON)}$ is 0.47-mΩ typical at 10-V V_{GS}
- MOSFET $Q_{g(total)}$ is 190 nC

Selection of Bootstrap Capacitor, C_{BST}

The internal charge pump charges the external bootstrap capacitor (connected between BST and SRC pins) with approximately 100 µA. Use the following equation to calculate the minimum required value of the bootstrap capacitor for driving two parallel BUK7S0R5-40HJ MOSFETs.

$$C_{BST} = \frac{Q_{g(total)}}{1\ V} = 380\ nF \quad (18)$$

Choose closest available standard value: 470 nF, 10 %.

Setting the Undervoltage Lockout

The undervoltage lockout (UVLO) can be adjusted using an external voltage divider network of R_1 and R_2 connected between VS, EN/UVLO and GND pins of the device. The values required for setting the undervoltage and overvoltage are calculated by solving 式 19.

$$V_{(UVLOR)} = \frac{R_2}{(R_1 + R_2)} \times VIN_{UVLO} \quad (19)$$

For minimizing the input current drawn from the power supply, TI recommends to use higher values of resistance for R_1 and R_2. However, leakage currents due to external active components connected to the resistor string can add error to these calculations. So, the resistor string current, $I(R_{12})$ must be chosen to be 20 times greater than the leakage current of UVLO pin.

From the device electrical specifications, $V_{(UVLOR)}$ = 1.18 V. From the design requirements, VIN_{UVLO} is 6.5 V. To solve the equation, first choose the value of R_1 = 470 kΩ and use 式 19 to solve for R_2 = 104.24 kΩ. Choose the closest standard 1% resistor values: R_1 = 470 kΩ, and R_2 = 105 kΩ.

Selection of Precharge Path Components, C_g and R_g

For charging the large capacitors on output, the output slew rate can be controlled by using a capacitor on the gate (G) of the precharge FET Q_3. The target inrush current to charge 1 mF of output capacitance to 12-V in 10 ms can be estimated by 式 20. The required gate capacitance Cg to limit the inrush current to 1.2 A can be calculated by using , where $I_{(G)}$ = 100 µA (typical) is the gate charging current of pin 'G'. By solving , we get C_g as 83.33 nF.

Choose the closest available standard value: 82 nF, 10%.

$$I_{INRUSH} = C_{OUT} \times \frac{V_{IN}}{T_{start}} = 1.2\ A \quad (20)$$

$$C_g = \frac{C_{OUT} \times I_{(G)}}{I_{INRUSH}} \quad (21)$$

A series resistor R_g must be used in conjunction with C_g to limit the discharge current from C_g during turn-off and to stabilize the gate 'G' during slew rate control. The recommended value for R_g is between 220 Ω to 470 Ω.

Choosing the Current Monitoring Resistor, R_{IMON}

Voltage at IMON pin $V_{(IMON)}$ is proportional to the output load current. This can be connected to an ADC of the downstream system for monitoring the operating condition and health of the system. The R_{IMON} must be selected based on the maximum load current and the input voltage range of the ADC used. R_{IMON} is set using 式 22.

$$V_{(IMON)} = \left(V_{SNS} + V_{(OS\_SET)}\right) \times \frac{0.9 \times R_{IMON}}{R_{SET}} \quad (22)$$

Where $V_{SNS} = I_{OC} \times R_{SNS}$ and $V_{(OS\_SET)}$ is the input referred offset (± 200 µV) of the current sense amplifier.

The maximum voltage range for monitoring the current ($V_{(IMONmax)}$) is limited to minimum([$V_{(VS)}$ – 0.5V], 5.5V) to ensure linear output. This puts a limitation on the maximum value of R_{IMON} resistor. The IMON pin has an internal clamp of 6.5 V (typical).

For I_{OC} = 30 A and considering the operating range of ADC to be 0 V to 3.3 V (for example, $V_{(IMON)}$ = 3.3 V), R_{IMON} can be calculated as

$$R_{IMON} = \frac{V_{(IMON)} \times R_{SET}}{\left(V_{SNS} + V_{(OS\_SET)}\right) \times 0.9} = 16.52\ k\Omega \quad (23)$$

Selecting R_{IMON} value less than shown in 式 23 ensures that ADC limits are not exceeded for maximum value of load current. Choose the closest available standard value: 16.5 kΩ, 1%.

9.2.3 Application Curves

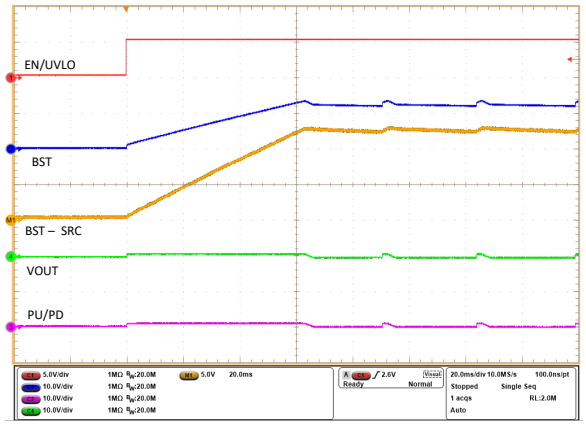

図 9-2. Start-Up Profile of Bootstrap Voltage for INP = GND and C_{BST} = 470 nF

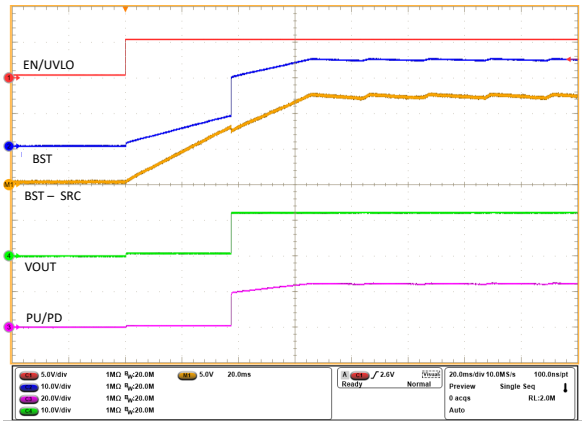

図 9-3. Start-Up Profile of Bootstrap Voltage for INP = HIGH and C_{BST} = 470 nF

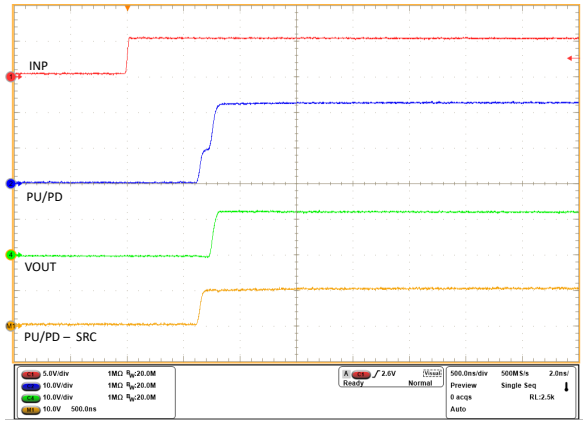

図 9-4. Turn-ON Response of TPS12111-Q1 for INP -> LOW to HIGH and C_{BST} = 470 nF

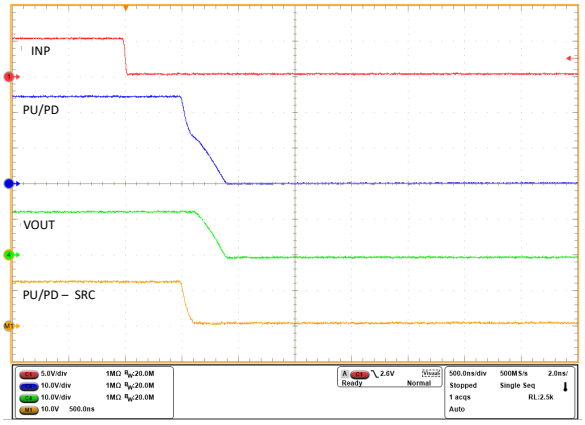

図 9-5. Turn-OFF Response of TPS12111-Q1 for INP -> HIGH to LOW and C_{BST} = 470 nF

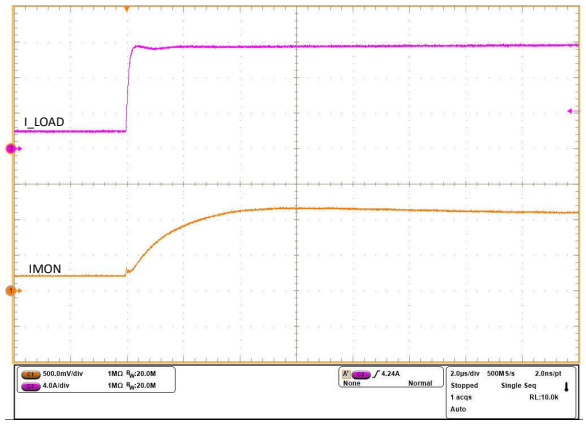

図 9-6. IMON Response During 12-A Load Step

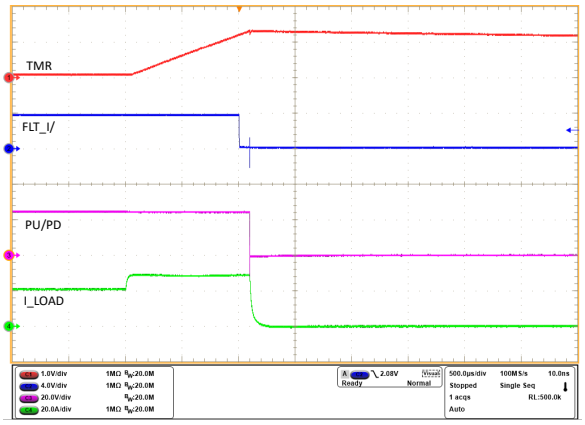

図 9-7. Overcurrent Response of TPS12111-Q1 for a Load Step from 20 A to 32 A with 30-A Overcurrent Protection Setting

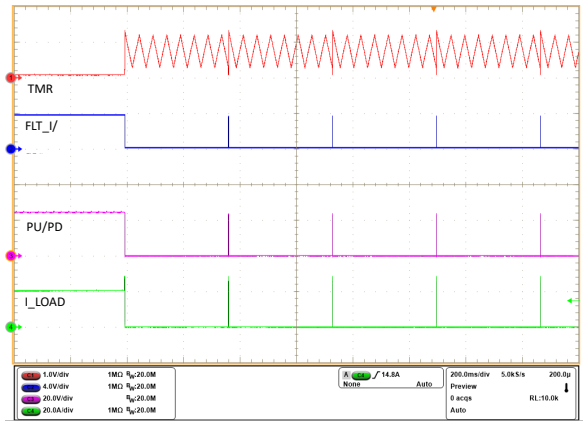

図 9-8. Auto-Retry Response of TPS12111-Q1 for an Overcurrent Fault

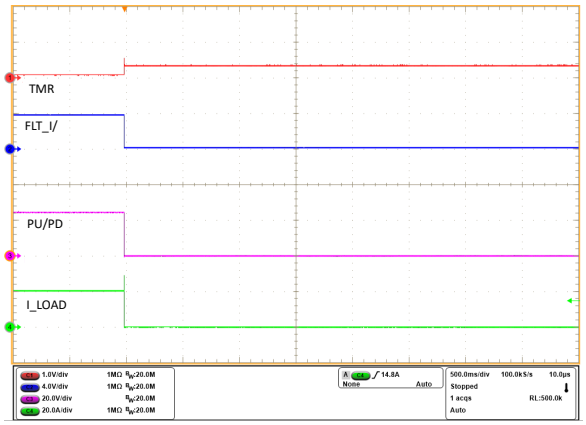

図 9-9. Latch-Off Response of TPS12111-Q1 for an Overcurrent Fault

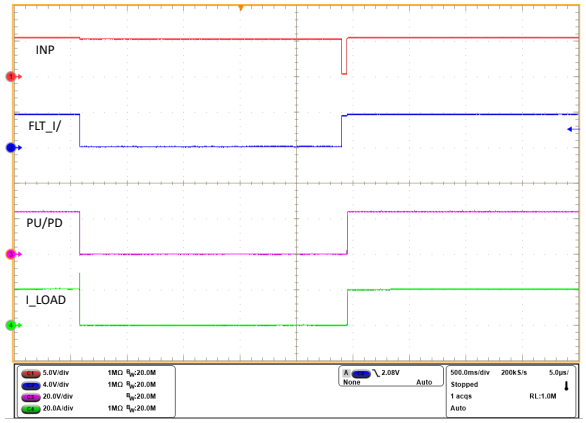

図 9-10. Response During Coming out of Overload Fault with INP Reset

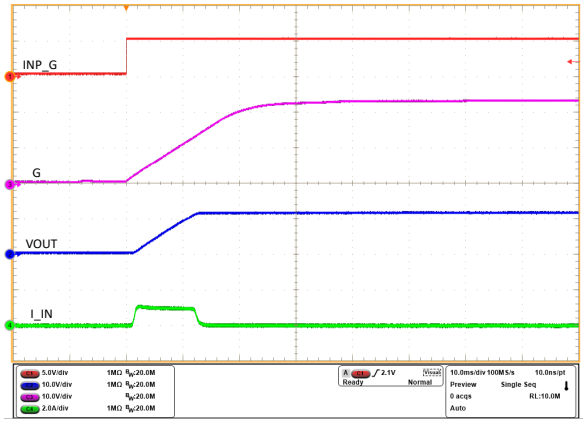

図 9-11. Precharge Profile of the Output Capacitance (VIN = 12 V, C_{OUT} = 1 mF, No Load)

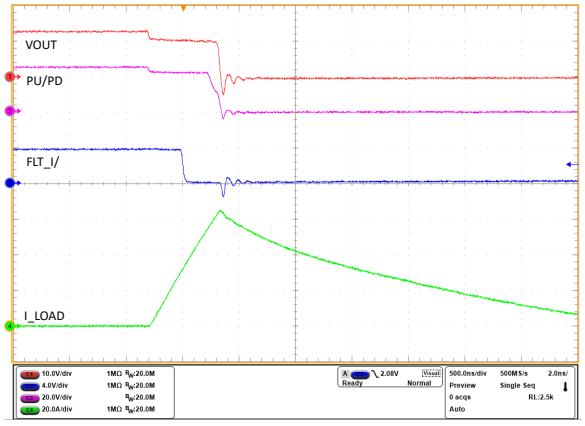

図 9-12. Output Hot-Short Response of the TPS12111-Q1 Device

9.3 Typical Application: Reverse Polarity Protection with TPS12110-Q1

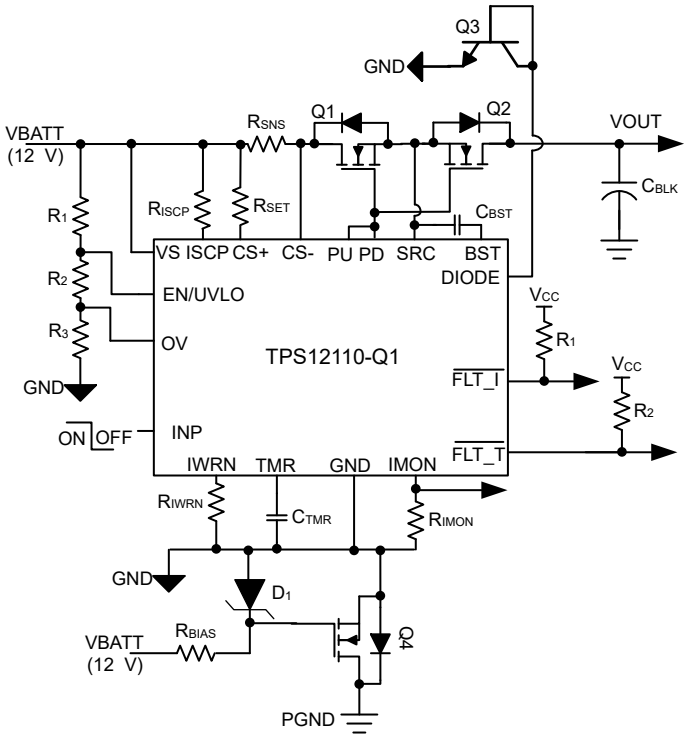

図 9-13. Typical Application Schematic: TPS12110-Q1 High-Side Driver with Input Reverse Polarity Protection

For applications such as powering electronic power steering (EPS) system, the input must be protected from any possible reverse polarity scenarios. The TPS12110-Q1 configured as shown in 図 9-13 meets the system requirements. The back-to-back FET (Q_1 and Q_2) configuration blocks reverse current flow and provides protection for the load against static input reverse polarity event. The N-MOSFET (Q_4) in the ground path protects the TPS12110-Q1 controller, and Zener diode D_1 is added for V_{GS} protection of Q_4.

9.3.1 Design Requirements

表 9-2 shows the design parameters for this application example.

表 9-2. Design Parameters

PARAMETER	VALUE
Typical input voltage, V_{IN}	12 V
Undervoltage lockout set point, VIN_{UVLO}	6.5 V
OV set point, VIN_{OVP}	36 V
Maximum load current, I_{OUT}	20 A
Overcurrent protection threshold, I_{OC}	24 A
Short-circuit protection threshold, I_{SC}	30 A
Fault timer period (t_{OC})	1 ms
Fault response	Auto-retry

表 9-2. Design Parameters (続き)

PARAMETER	VALUE
Input reverse polarity protection	Yes

9.3.2 External Component Selection

By following similar design procedure as outlined in *Detailed Design Procedure*, the external component values are calculated as below:

- R_{SNS} = 1 mΩ.
- R_{SET} = 100 Ω.
- R_{IWRN} = 49.9 kΩ to set 24 A as overcurrent protection threshold.
- R_{ISCP} = 1.468 kΩ to set 30 A as short-circuit protection threshold.
- C_{TMR} = 68 nF to set 1-ms over current protection time.
- R_1 , R_2 and R_3 are selected as 390 kΩ, 71.5 kΩ and 15.8 kΩ respectively to set VIN undervoltage lockout threshold at 6.5 V and overvoltage cutoff threshold at 36 V.
- R_{IMON} = 15 kΩ to limit maximum $V_{(IMON)}$ voltage to 3.3 V at full-load current of 24 A.
- To reduce conduction losses, BUK7S0R5-40HJ MOSFET is selected. Two FETs are used in back-to-back configuration for reverse current blocking.
  - 40-V $V_{DS(MAX)}$ and 20-V $V_{GS(MAX)}$.
  - $R_{DS(ON)}$ is 0.47-mΩ typical at 10-V V_{GS}.
  - Q_g of each MOSFET is 190 nC.
- C_{BST} = (2 × Q_g) / 1 V = 380 nF; Choose the closest available standard value: 470 nF, 10 %.
- Q_4 selection: Any signal N-MOSFET with 40-V V_{DS} support is sufficient. DMN601WKQ-7 is selected for the current design and a 12-V Zener diode SZMM3Z12VST1G is used for V_{GS} protection.

9.3.3 Application Curves

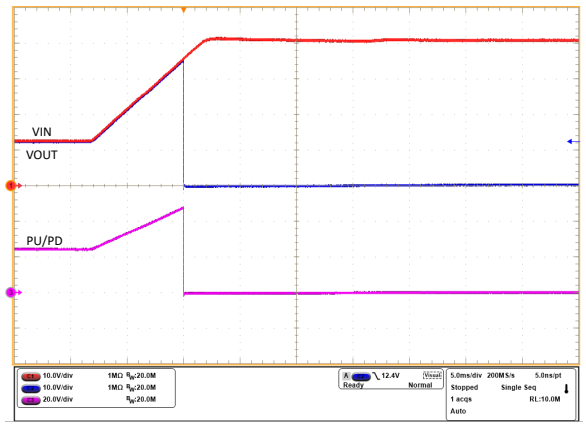

図 9-14. Overvoltage Cutoff Response of TPS12110-Q1 at 36-V Level

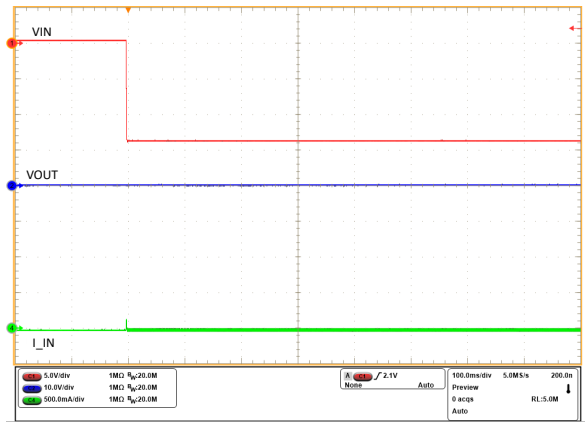

図 9-15. Input Reverse Polarity Protection with TPS12110-Q1

9.4 Power Supply Recommendations

When the external MOSFETs turn OFF during the conditions such as INP control, overvoltage cutoff, overcurrent protection causing an interruption of the current flow, the input parasitic line inductance generates a positive voltage spike on the input and output parasitic inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) depends on the value of inductance in series to the input or output of the device. These transients can exceed the *Absolute Maximum Ratings* of the device if steps are not taken to address the issue. Typical methods for addressing transients include:

- Use of a TVS diode and input capacitor filter combination across input to and GND to absorb the energy and dampen the positive transients.
- Use of a diode or a TVS diode across the output and GND to absorb negative spikes.

The TPS1211-Q1 gets powered from the VS pin. Voltage at this pin must be maintained above $V_{(VS\_PORR)}$ level to ensure proper operation. If the input power supply source is noisy with transients, then TI recommends to place a R_{VS} - C_{VS} filter between the input supply line and VS pin to filter out the supply noise. TI recommends R_{VS} value around 100 Ω.

In case where large di/dt is involved, the system and layout parasitic inductances can generate large differential signal voltages between ISCP and CS- pins. This action can trigger false short-circuit protection and nuisance trips in the system. To overcome such scenario, TI recommends to add filter capacitor of 1 nF (C_{SCP}) across ISCP and CS- pins close to the device. Because nuisance trips are dependent on the system and layout parasitics, TI recommends to test the design in a real system and tweaked as necessary.

The following figure shows the circuit implementation with optional protection components.

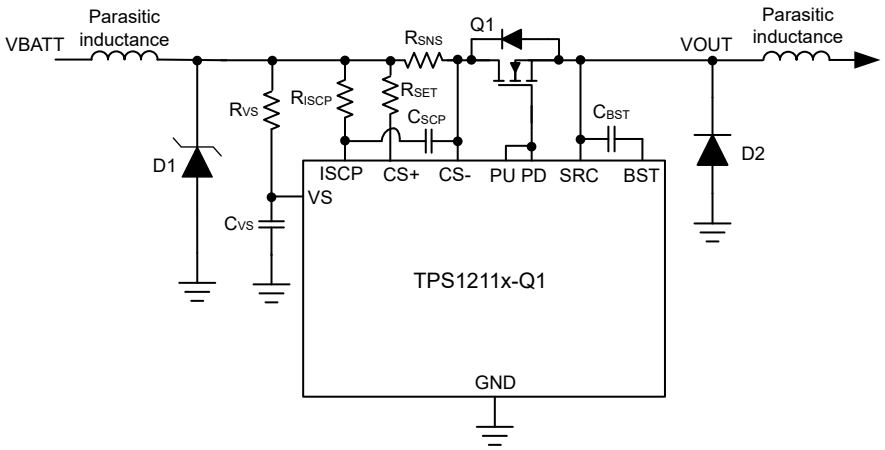

図 9-16. Circuit Implementation with Optional Protection Components for TPS1211-Q1

9.5 Layout

9.5.1 Layout Guidelines

- The sense resistor (R_{SNS}) must be placed close to the TPS1211x-Q1 and then connect R_{SNS} using the Kelvin techniques. Refer to *Choosing the Right Sense Resistor Layout* for more information on the Kelvin techniques.
- For all the applications, TI recommends a 0.1 µF or higher value ceramic decoupling capacitor between VS terminal and GND. Consider adding RC network at the supply pin (VS) of the controller to improve decoupling against the power line disturbances.
- The high-current path from the board input to the load, and the return path, must be parallel and close to each other to minimize loop inductance.
- The external MOSFETs must be placed close to the controller such that the GATE of the MOSFETs are close to PU/PD pins to form short GATE loop. Consider adding a place holder for a resistor in series with the Gate of each external MOSFET to damp high frequency oscillations if need arises.
- Place a TVS diode at the input to clamp the voltage transients during hot-plug and fast turn-off events.
- The external boot-strap capacitor must be placed close to BST and SRC pins to form very short loop.
- The ground connections for the various components around the TPS1211x-Q1 must be connected directly to each other, and to the TPS1211x-Q1 GND, and then connected to the system ground at one point. Do not connect the various component grounds to each other through the high current ground line.
- The DIODE pin sources current to measure the temperature. TI recommends BJT MMBT3904 to use as a remote temperature sense element. Take care in the PCB layout to keep the parasitic resistance between the DIODE pin and the MMBT3904 low so as not to degrade the measurement. In addition, TI recommends to

make a Kelvin connection from the emitter of the MMBT3904 to the GND of the part to ensure an accurate measurement. Additionally, a small 1000 pF bypass capacitor must be placed in parallel with the MMBT3904 to reduce the effects of noise.

9.5.2 Layout Example

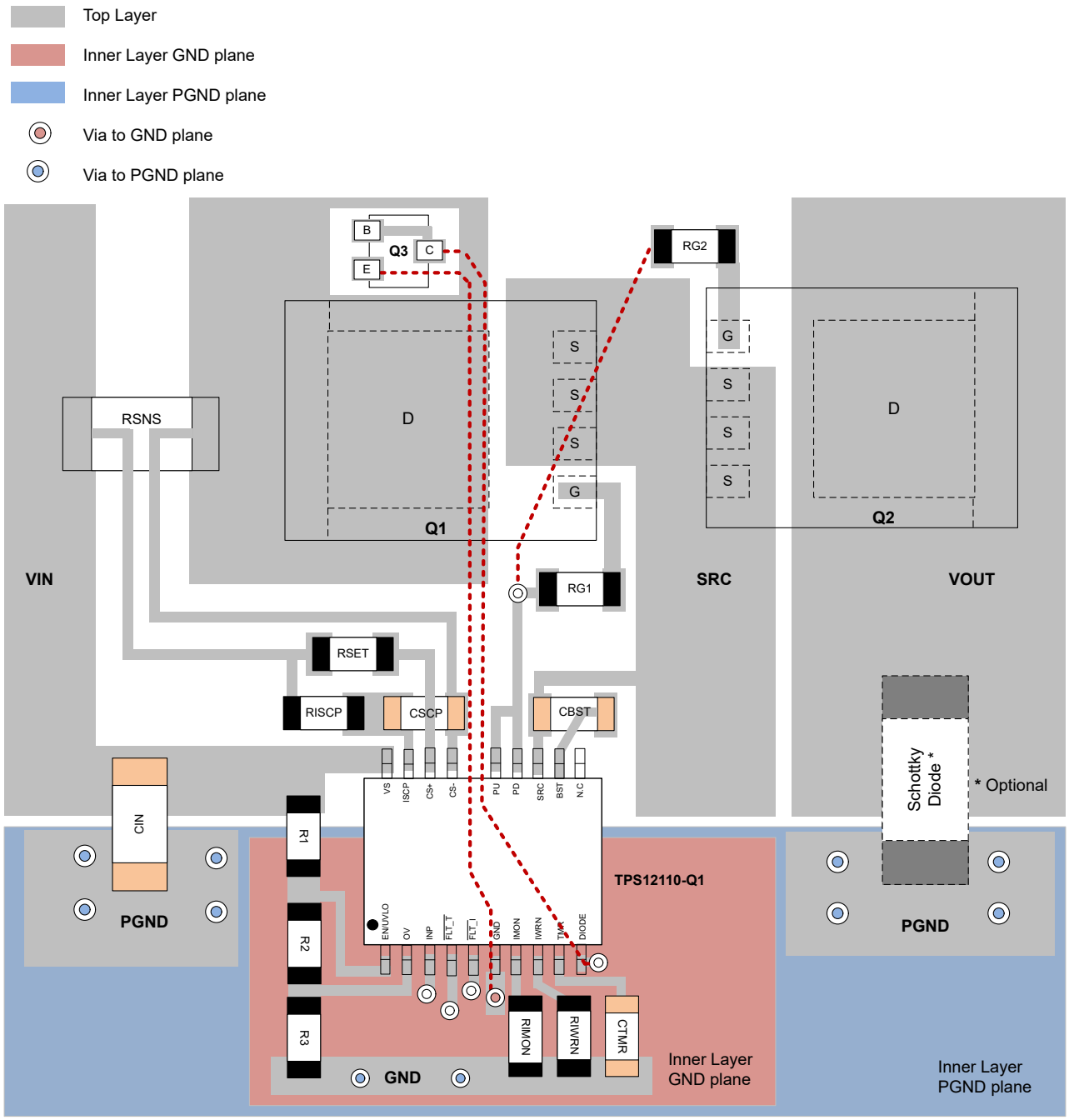

図 9-17. Typical PCB Layout Example for TPS12110-Q1 With B2B MOSFETs

10 Device and Documentation Support

10.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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10.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (April 2024) to Revision E (April 2025)	Page
• Updated trace connected to ISCP pin for "Typical PCB Layout Example for TPS12110-Q1 With B2B MOSFETs" figure in the *Layout Example* section	41

Changes from Revision C (October 2023) to Revision D (April 2024)	Page
• Updated the DIODE sense TSD rising threshold, $T_{(DIODE\_TSD\_rising)}$, specification in the *Electrical Characteristics* section	7

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS12110AQDGXRQ1	Active	Production	VSSOP (DGX) | 19	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2ZAS
TPS12110AQDGXRQ1.A	Active	Production	VSSOP (DGX) | 19	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2ZAS
TPS12111LQDGXRQ1	Active	Production	VSSOP (DGX) | 19	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2Z9S
TPS12111LQDGXRQ1.A	Active	Production	VSSOP (DGX) | 19	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2Z9S
TPS12112AQDGXRQ1	Active	Production	VSSOP (DGX) | 19	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	3CLS
TPS12112AQDGXRQ1.A	Active	Production	VSSOP (DGX) | 19	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	3CLS

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

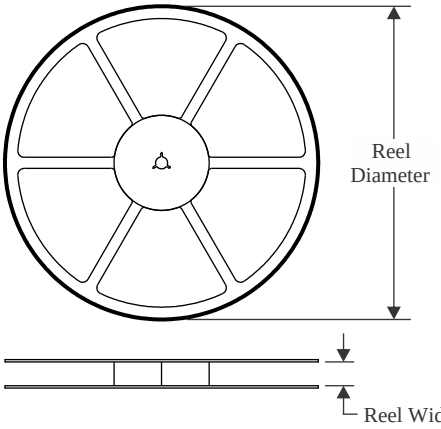
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

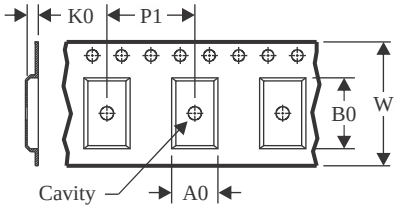
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

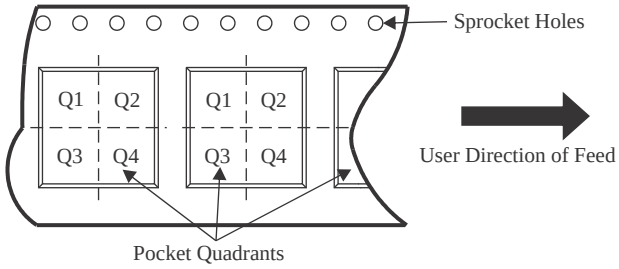


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

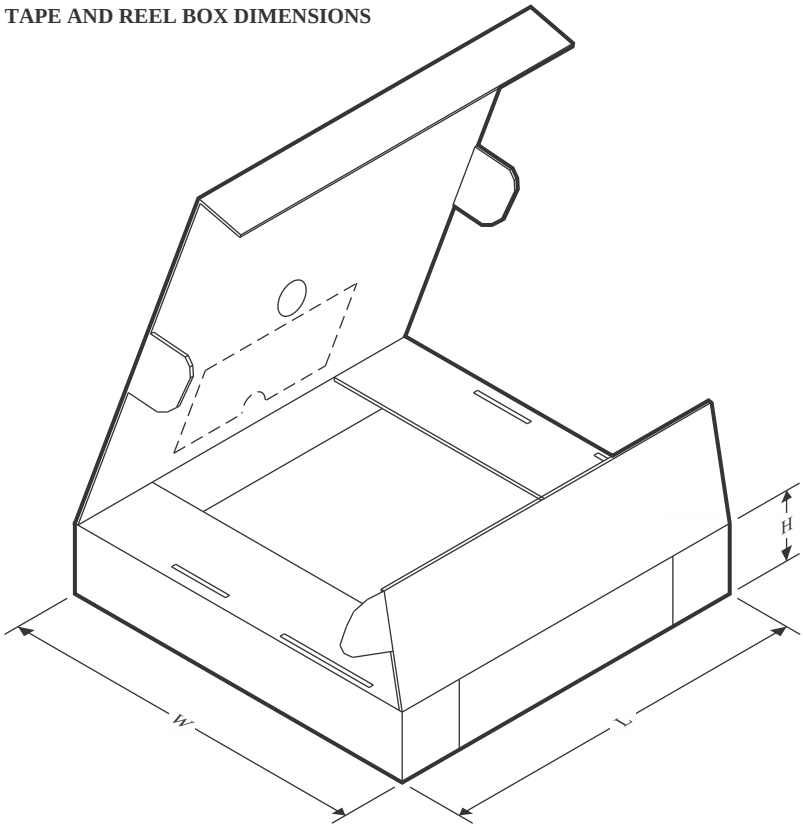
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS12110AQDGXRQ1	VSSOP	DGX	19	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1
TPS12111LQDGXRQ1	VSSOP	DGX	19	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1
TPS12112AQDGXRQ1	VSSOP	DGX	19	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

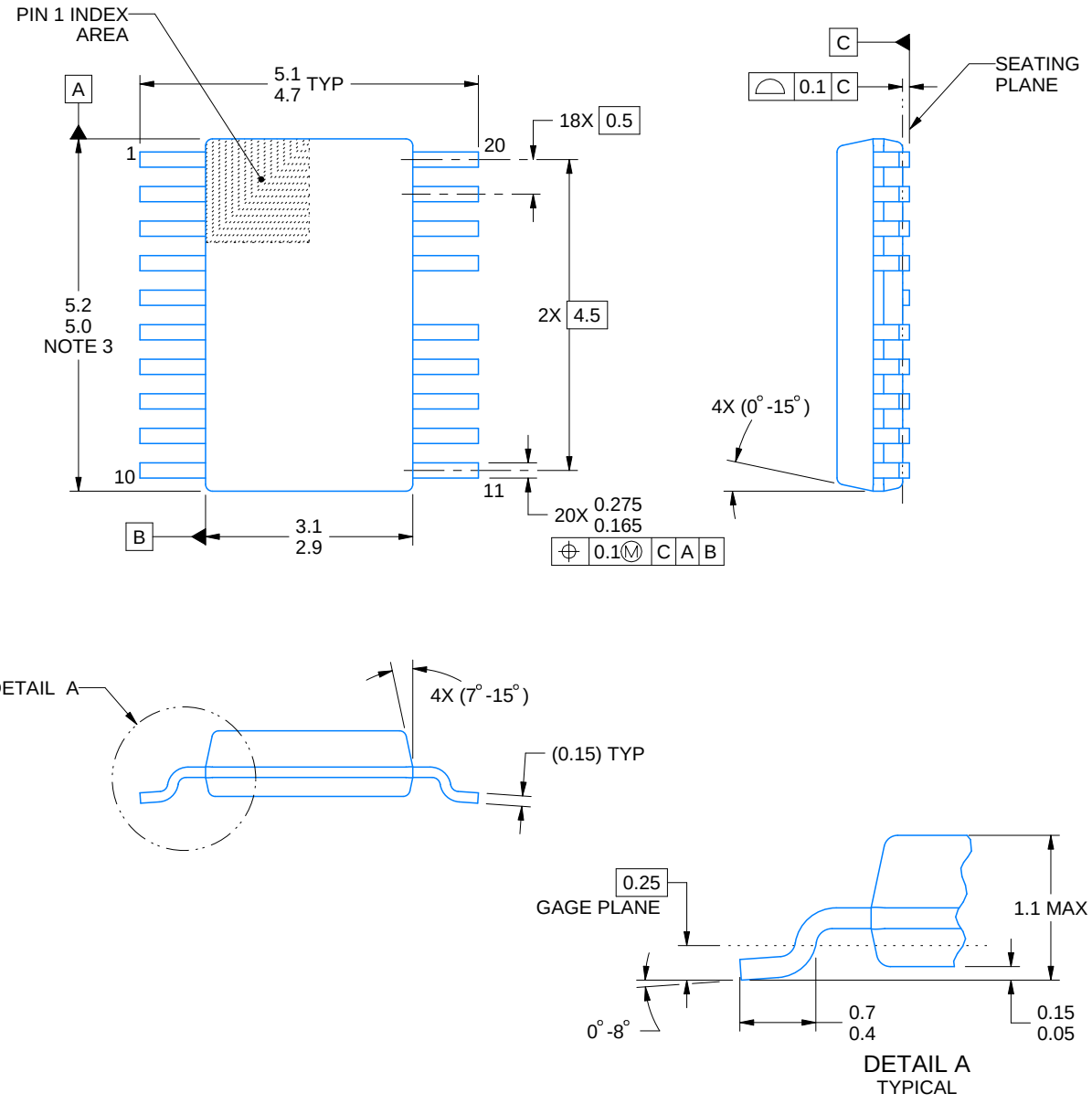
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS12110AQDGXRQ1	VSSOP	DGX	19	5000	353.0	353.0	32.0
TPS12111LQDGXRQ1	VSSOP	DGX	19	5000	353.0	353.0	32.0
TPS12112AQDGXRQ1	VSSOP	DGX	19	5000	353.0	353.0	32.0

PACKAGE OUTLINE

DGX0019A

VSSOP - 1.1 mm max height

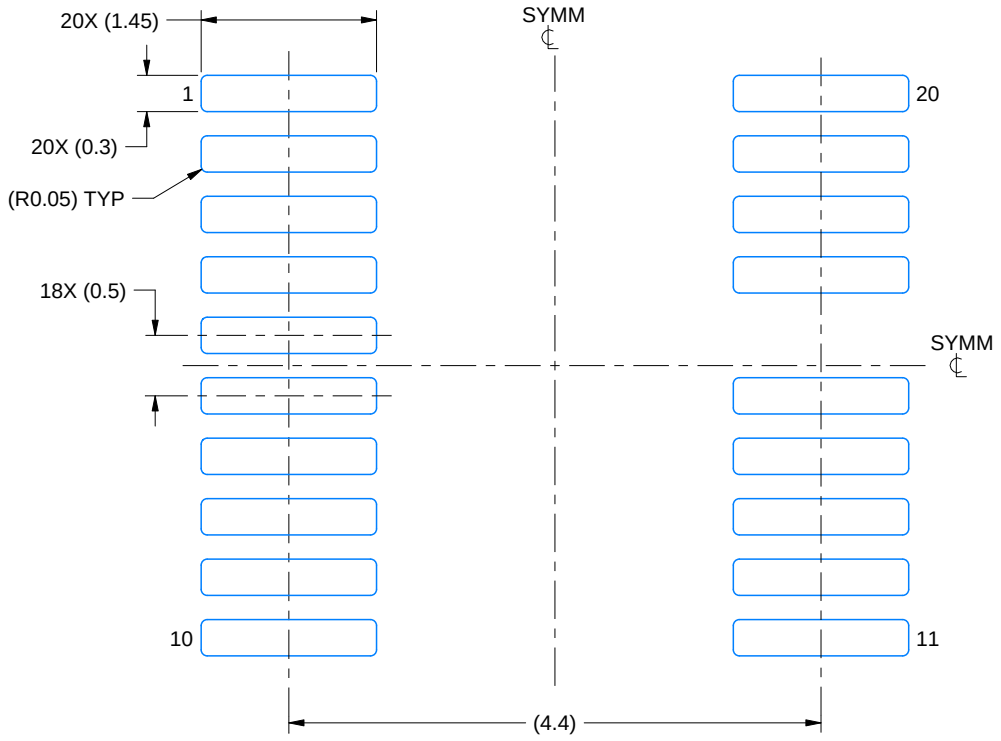
SMALL OUTLINE PACKAGE



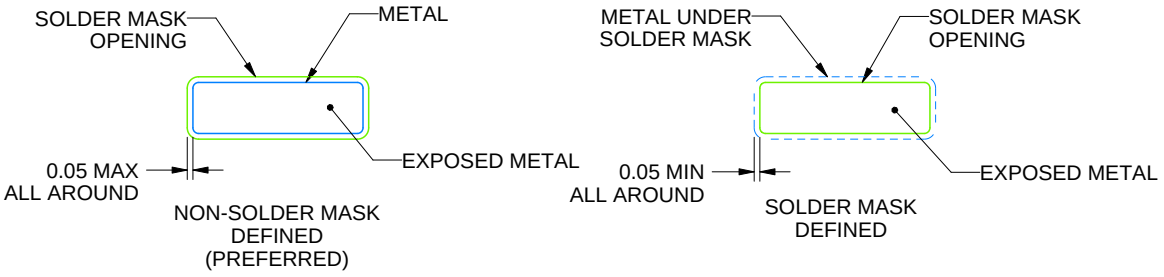
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of July 2021.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
SCALE: 16X

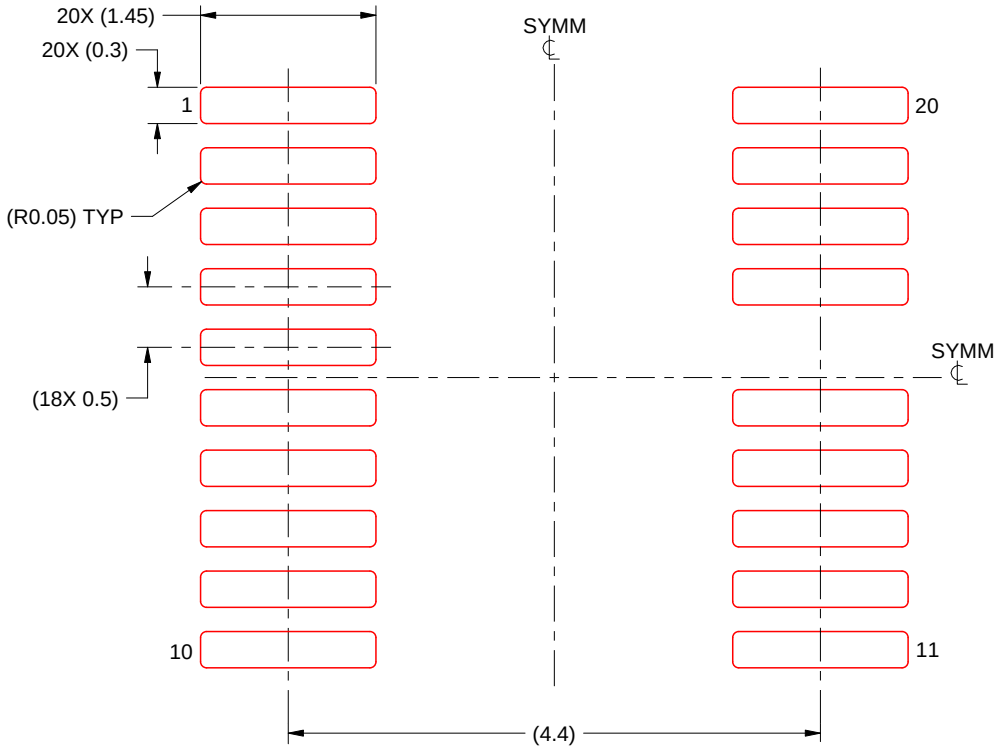


SOLDER MASK DETAILS

4226944/A 07/2021

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 16X

4226944/A 07/2021

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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