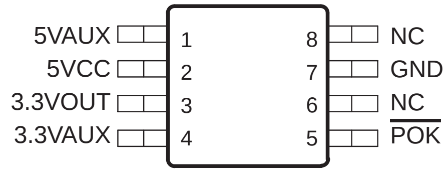
- **Automatic Input Voltage Source Selection**
- **Glitch-Free Regulated Output**
- **5-V Input Voltage Source Detector With Hysteresis**
- **400-mA Load Current Capability With 5-V or 3.3-V Input Source**
- **Power OK Feature Based on Voltage Supervisor of 3.3VOUT**
- **Low $r_{DS(on)}$ Auxiliary Switch**
- **Thermally Enhanced PowerPAD™ Packaging Concept for Efficient Heat Management**

DGN PACKAGE
(TOP VIEW)



NC – No connect

description

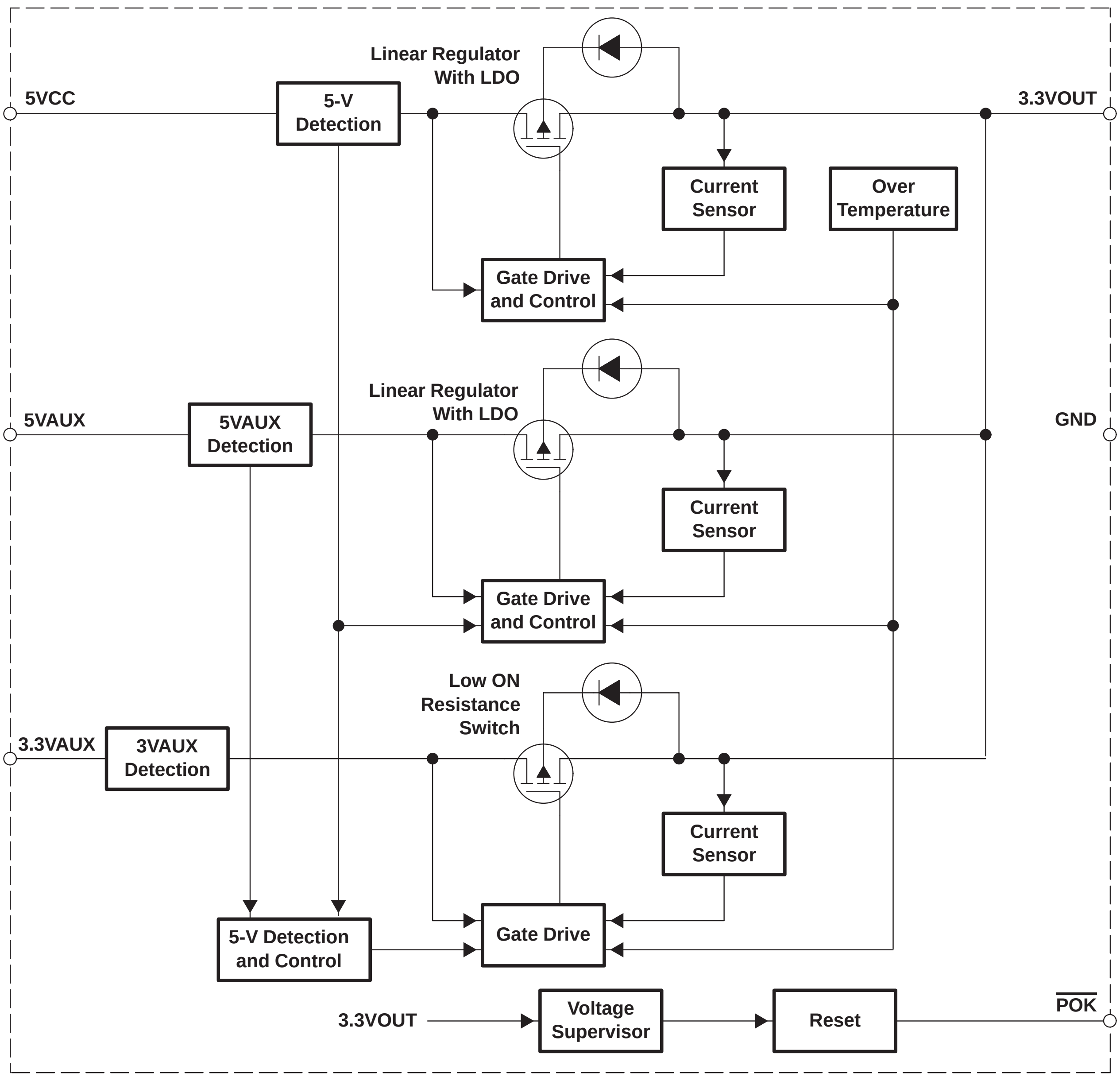
The TPPM0302 is a low-dropout regulator with auxiliary power management that provides a constant 3.3-V supply at the output capable of driving a 400-mA load.

The TPPM0302 provides a regulated power output for systems that have multiple input sources and require a constant voltage source with a low-dropout voltage. This is a single output, multiple input, intelligent power source selection device with a low-dropout regulator for either 5VCC or 5VAUX inputs, and a low-resistance bypass switch for the 3.3VAUX input.

Transitions may occur from one input supply to another without generating a glitch, outside of the specification range, on the 3.3-V output. The device has an incorporated reverse blocking scheme to prevent excess leakage from the input terminals in the event that the output voltage is greater than the input voltage. The output voltage is continually monitored for constant output, and any deviation from the internal set limit (≈2.8 V) is reported by a low signal on the $\overline{\text{POK}}$ output.

The input voltage is prioritized in the following order: 5VCC, 5VAUX, and 3.3VAUX.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
3.3VAUX	4	I	3.3-V auxiliary input
3.3VOUT	3	O	3.3-V output with a typical capacitance load of 4.7 µF
5VAUX	1	I	5-V auxiliary input
5VCC	2	I	5-V main input
GND	7	I	Ground
NC	6, 8	I	No internal connection
$\overline{\text{POK}}$	5	O	Power OK

Table 1. Input Selection

INPUT VOLTAGE STATUS (V)			INPUT SELECTED	OUTPUT (V)	OUTPUT (I)
5VCC	5VAUX	3.3VAUX	5VCC/5VAUX/3.3VAUX	3.3VOUT	I_L (mA)
0	0	0	None	0	0
0	0	3.3	3.3VAUX	3.3	375
0	5	0	5VAUX	3.3	400
0	5	3.3	5VAUX	3.3	400
5	0	0	5VCC	3.3	400
5	0	3.3	5VCC	3.3	400
5	5	0	5VCC	3.3	400
5	5	3.3	5VCC	3.3	400

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, 5-V main input, $V_{(5VCC)}$ (see Notes 1 and 2) . . . . 7 V
Auxiliary voltage, 5-V input, $V_{(5VAUX)}$ (see Notes 1 and 2) . . . . 7 V
Auxiliary voltage, 3.3-V input, $V_{(3.3VAUX)}$ (see Notes 1 and 2) . . . . 5 V
3.3-V output current limit, $I_{(LIMIT)}$ . . . . 1.5 A
Continuous power dissipation, P_D (see Note 3) . . . . 1.36 W
Electrostatic discharge susceptibility, human body model, $V_{(HBMESD)}$ . . . . 2 kV
Operating ambient temperature range, T_A . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . –55°C to 150°C
Operating junction temperature range, T_J . . . . –5°C to 120°C
Lead temperature (soldering, 10 second), $T_{(LEAD)}$ . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. Absolute negative voltage on these terminal should not be below –0.5 V.
3. Refer to the Thermal Information Section.

recommended operating conditions

	MIN	TYP	MAX	UNIT
5-V main input, $V_{(5VCC)}$	4.5		5.5	V
5-V auxiliary input, $V_{(5VAUX)}$	4.5		5.5	V
3.3-V auxiliary input, $V_{(3.3VAUX)}$	3		3.6	V
Load capacitance, C_L	4.23	4.7	5.17	µF
Load current, I_L	0		400	mA
Ambient temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range, T_A = 0°C to 70°C, C_L = 4.7 μF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(5VCC)}$/ $V_{(5VAUX)}$	5-V inputs		4.5	5	5.5	V
$I_{(Q)}$	Quiescent supply current	From 5VCC or 5VAUX terminals, I_L = 0 mA to 400 mA		2.5	5	mA
		From 3.3VAUX terminal, I_L = 0 A		250	500	μA
I_L	Output load current		0.4			A
$I_{(LIMIT)}$	Output current limit	3.3VOUT = 0 V		1	1.5	A
$T_{(TSD)}$†	Thermal shutdown	3.3VOUT output shorted to 0 V	150		180	°C
T_{hys}†	Thermal hysteresis			15		
$V_{(3.3VOUT)}$	3.3-V output	I_L = 400 mA	3.135	3.3	3.465	V
C_L	Load capacitance	Minimal ESR to insure stability of regulated output		4.7		μF
$I_{lkg(REV)}$	Reverse leakage output current	Tested for input that is grounded. 3.3VAUX, 5VAUX, or 5VCC = GND, 3.3VOUT = 3.3 V			50	μA

† Design targets only. Not tested in production.

5-V detect

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(TO\_LO)}$	Threshold voltage, low	5VAUX or 5VCC↓	3.85	4.05	4.25	V
$V_{(TO\_HI)}$	Threshold voltage, high	5VAUX or 5VCC↑	4.1	4.3	4.5	V

auxiliary switch

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{(SWITCH)}$	Auxiliary switch resistance	5VAUX = 5VCC = 0 V, 3.3VAUX = 3.3 V, I_L = 150 mA			0.4	Ω
$\Delta V_{O(\Delta VI)}$	Line regulation voltage	5VAUX or 5VCC = 4.5 V to 5.5 V		2		mV
$\Delta V_{O(\Delta IO)}$	Load regulation voltage	20 mA < I_L < 400 mA		40		mV
$V_I - V_O$	Dropout voltage	I_L < 400 mA			1	V

Power OK ($\overline{\text{POK}}$)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(TO\_POK)}$	POK threshold voltage	3.3VOUT = 0 → 3.3 V and starts $\overline{\text{POK}}$ delay timer	2.67	2.8	2.93	V
V_{OL}	Output low voltage				0.4	
I_{OH}	Output high current				200	μA
V_{OH}	Output high voltage	5K pullup to 3.3VOUT		3.3		V

timing characteristics, T_A = 0°C to 70°C, C_L = 4.7 μF (unless otherwise noted)†

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_d	Power OK delay	5VCC or 5VAUX or 3.3VAUX > V_{TO} and $\overline{\text{POK}}$ ↑		5	10	ms

† Design targets only. Not tested in production.

thermal characteristics‡

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal impedance, junction-to-case		4.7		°C/W
$R_{\theta JA}$	Thermal impedance, junction-to-ambient		59		°C/W

‡ Based on Texas Instrument recommended board for PowerPAD package.

PARAMETER MEASUREMENT INFORMATION

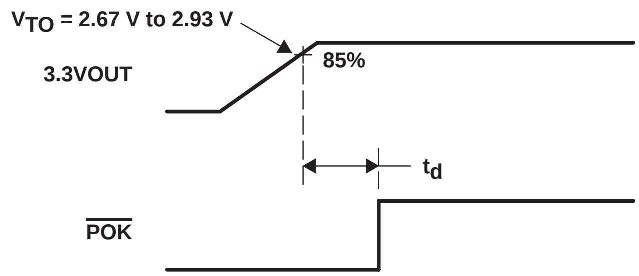


Figure 1. Power OK Timing Diagram

TYPICAL CHARACTERISTICS

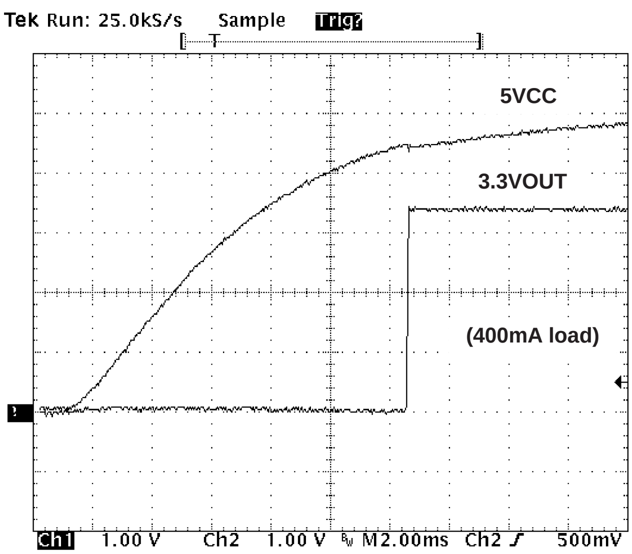


Figure 2. 5VCC Cold Start

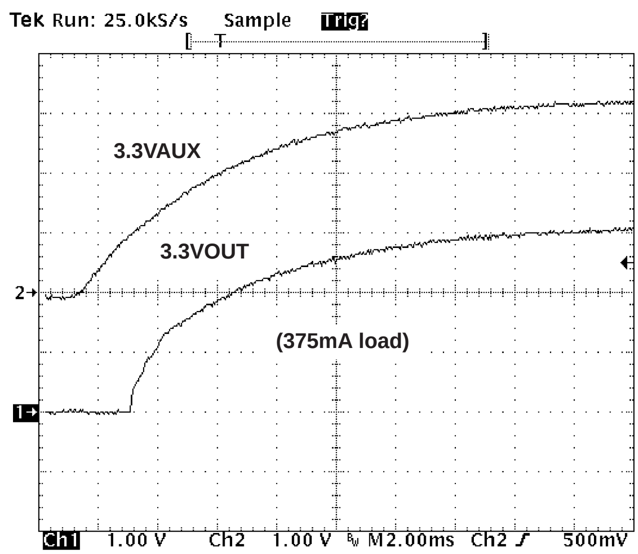


Figure 3. 3.3VAUX Cold Start

TYPICAL CHARACTERISTICS

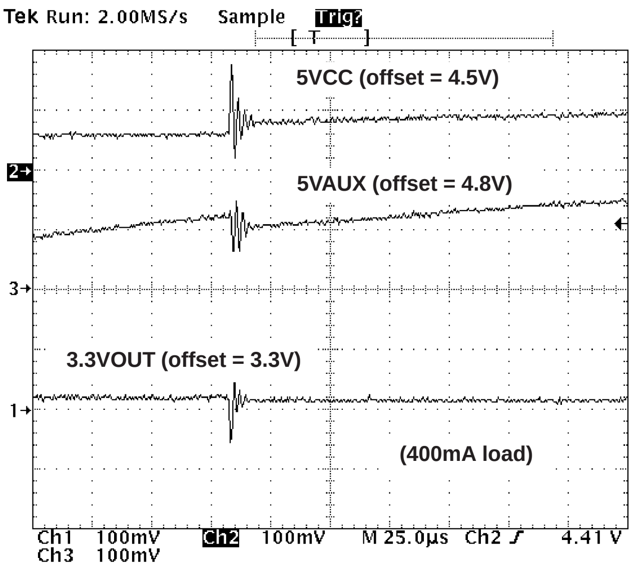


Figure 4. 5VCC Power Up (5VAUX = 5 V)

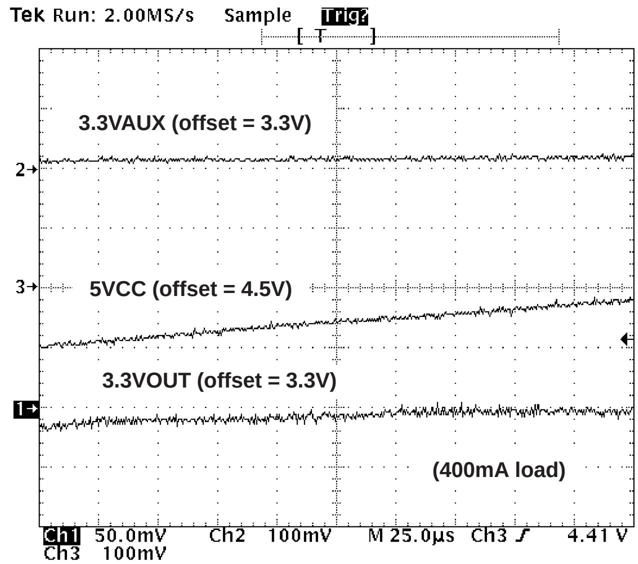


Figure 5. 5VCC Power Up (3.3VAUX = 3.3 V)

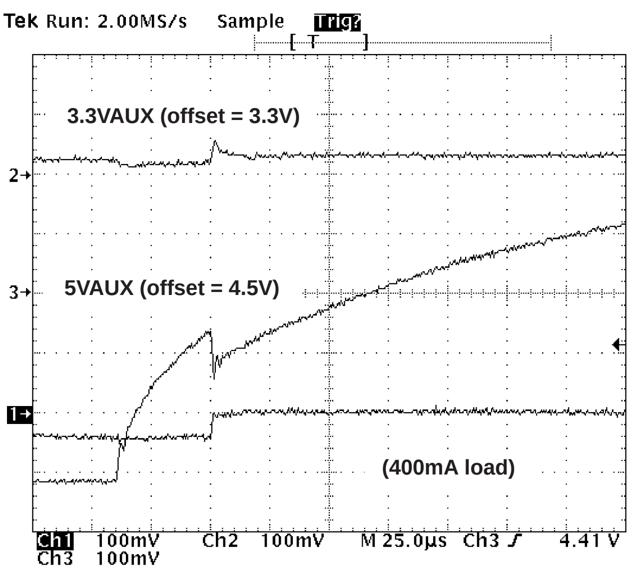


Figure 6. 5VAUX Power Up (3.3VAUX = 3.3 V)

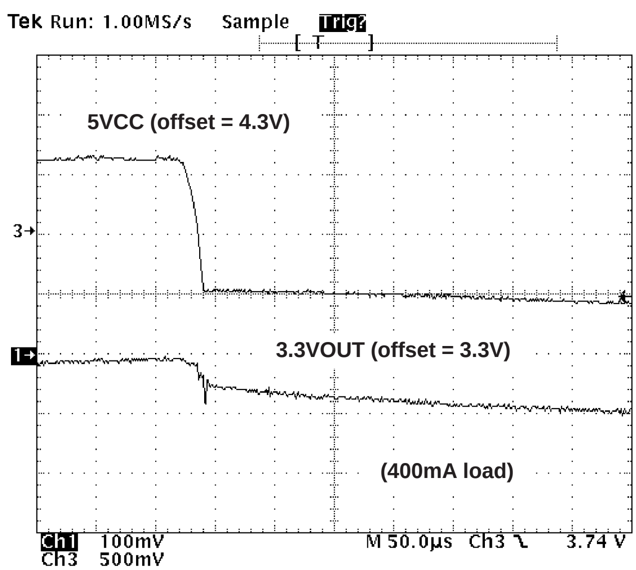


Figure 7. 5VCC Power Down (3.3VAUX = 3.3 V)

TYPICAL CHARACTERISTICS

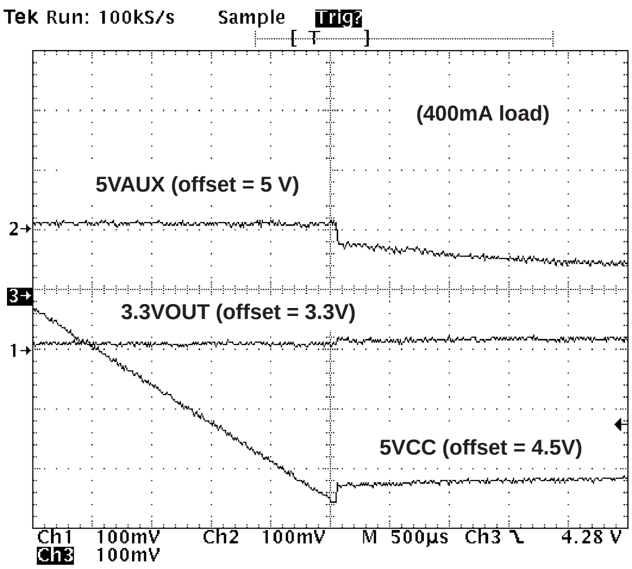


Figure 8. 5VCC Power Down (5VAUX = 5 V)

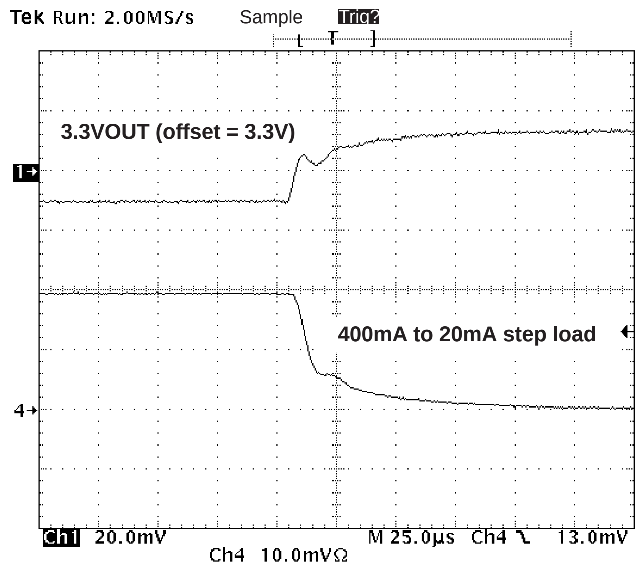


Figure 9. 5VCC Load Transient Responses Falling

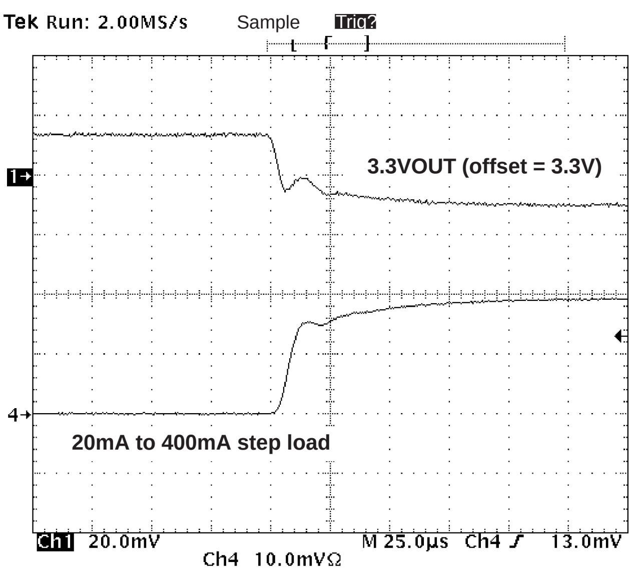


Figure 10. 5VCC Load Transient Response Rising

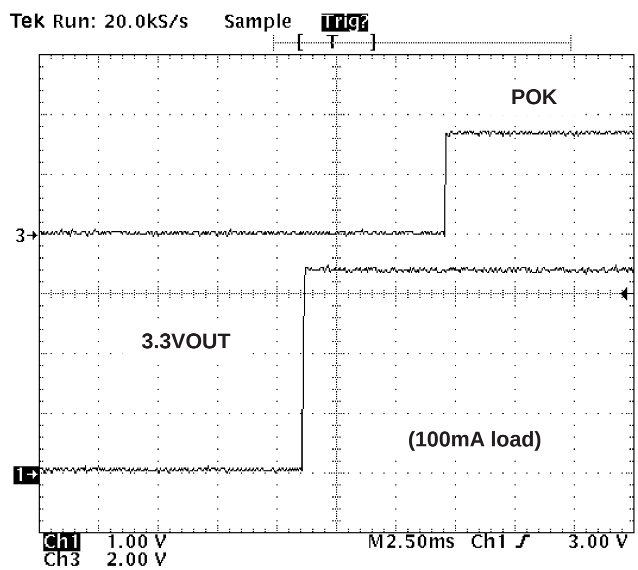


Figure 11. 5VCC Cold Start, $\overline{\text{POK}}$ Released

THERMAL INFORMATION

To ensure reliable operation of the device, the junction temperature of the output device must be within the safe operating area (SOA). This is achieved by having a means to dissipate the heat generated from the junction of the output structure. There are two components that contribute to thermal resistance. They consist of two paths in series. The first is the junction to case thermal resistance, $R_{\theta JC}$; the second is the case to ambient thermal resistance, $R_{\theta CA}$. The overall junction to ambient thermal resistance, $R_{\theta JA}$, is determined by:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

The ability to efficiently dissipate the heat from the junction is a function of the package style and board layout incorporated in the application. The operating junction temperature is determined by the operating ambient temperature, T_A, and the junction power dissipation, P_J.

The junction temperature, T_J, is equal to the following thermal equation:

$$T_J = T_A + P_J\,(R_{\theta JC}) + P_J\,(R_{\theta CA})$$

$$T_J = T_A + P_J\,(R_{\theta JA})$$

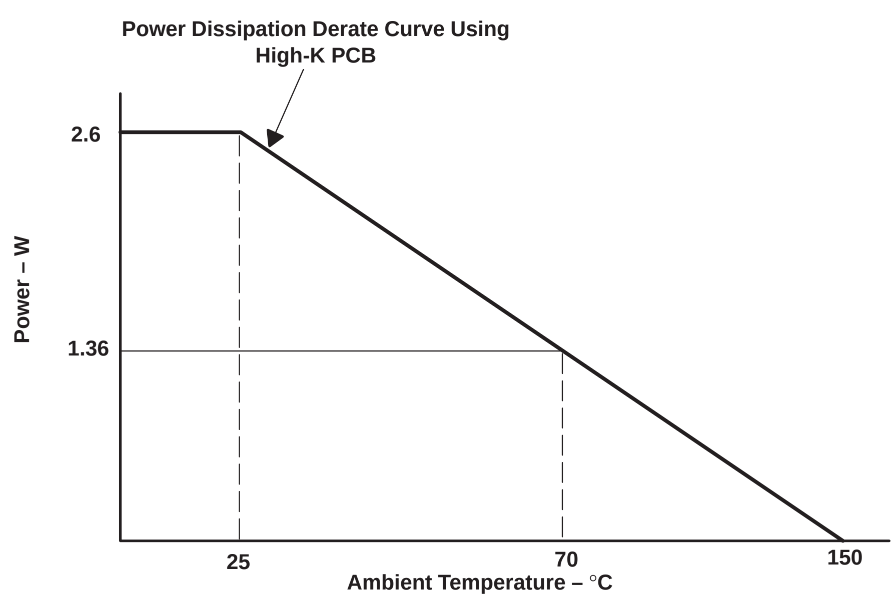
This particular application uses the 8-pin DGN PowerPAD package with a standard lead frame with dedicated ground terminal. Using a multilayer printed-circuit board (PCB), the power pad is mounted as recommended in the TI packaging application. The power pad is electrically connected to the ground plane of the circuit board through the dedicated ground pin and the die mount power pad. This will provide a means for heat spreading through the copper plane associated within the PCB (GND Layer). This concept could provide a thermal resistance from junction to ambient, $R_{\theta JA}$, of 59°C/W if implemented correctly.

Hence, maximum power dissipation allowable for an operating ambient temperature of 70°C, and a maximum junction temperature of 150°C is determined as:

$$P_J = (T_J – T_A) / R_{\theta JA}$$

$$P_J = (150 – 70) /59 = 1.36\ W$$

Using a multilayer board and utilizing the ground plane for heat spreading.



NOTE: This curve is to be used for guideline purposes only. For a particular application, a more specific thermal characterization is required.

Figure 12. Power Dissipation Derating Curve

APPLICATION INFORMATION

packaging

To maximize the efficiency of this package for application on a single layer or multilayer PCB, certain guidelines must be followed.

The following information is to be used as a guideline only. For further information, refer to the PowerPAD concept implementation document.

multilayer PCB

Guidelines for mounting the PowerPAD IC on a multilayer PCB with a ground plane.

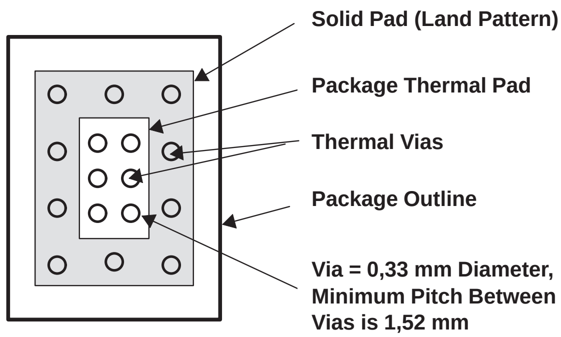


Figure 13. Package and Land Configuration for a Multilayer PCB

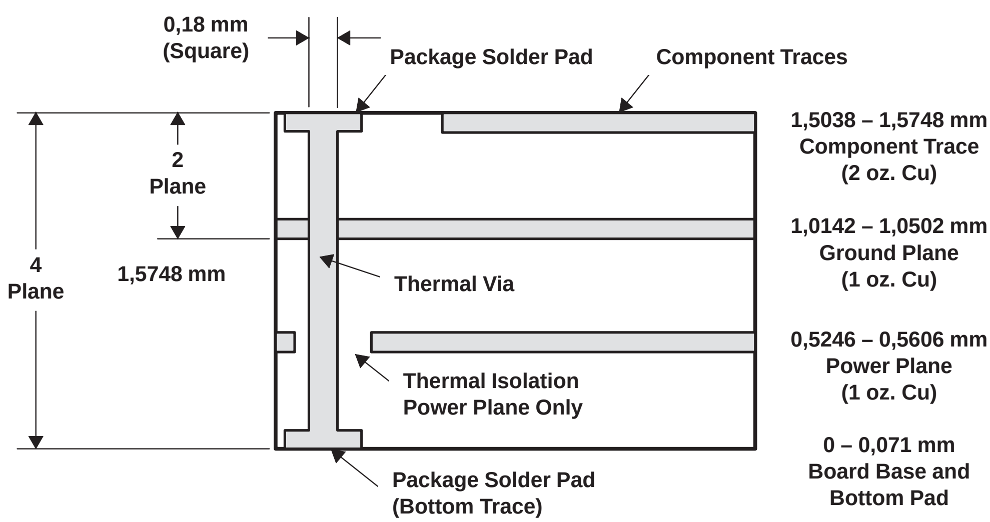


Figure 14. Multilayer Board (Side View)

APPLICATION INFORMATION

In a multilayer board application, the thermal vias are the primary method of heat transfer from the package thermal pad to the internal ground plane. The efficiency of this method depends on several factors (die area, number of thermal vias, thickness of copper) Consult the *PowerPAD Thermally Enhanced Package Technical Brief.*

single-layer PCB

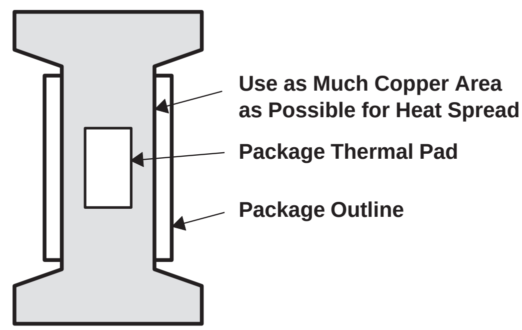


Figure 15. Land Configuration for Single-layer PCB

Layout recommendations for a single-layer PCB utilize as much copper area as possible for power management.

In a single layer board application, the thermal pad is attached to a heat spreader (copper area) by using low thermal impedance attachment method (solder paste or thermal conductive epoxy).

In both of the methods mentioned above, it is advisable to use as many copper traces as possible to dissipate the heat.

IMPORTANT

If the attachment method is NOT implemented correctly, the functionality of the product is not efficient. Power dissipation capability will be adversely affected if the device is incorrectly mounted onto the circuit board.

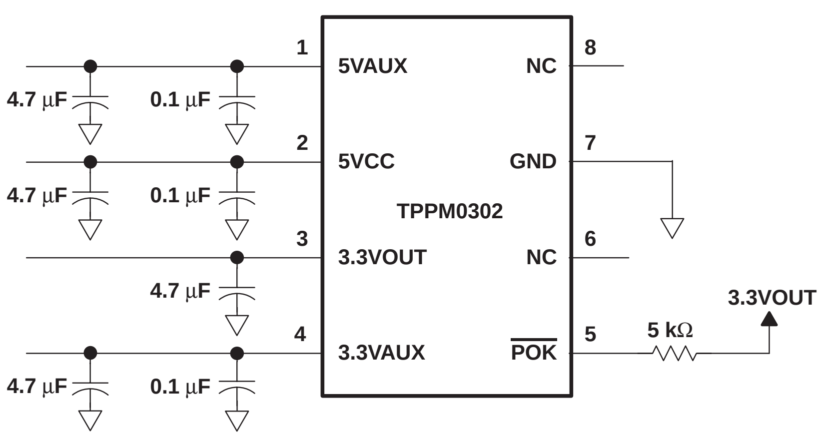


Figure 16. Typical Application Schematic

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPPM0302DGN	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	APF
TPPM0302DGN.A	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	APF

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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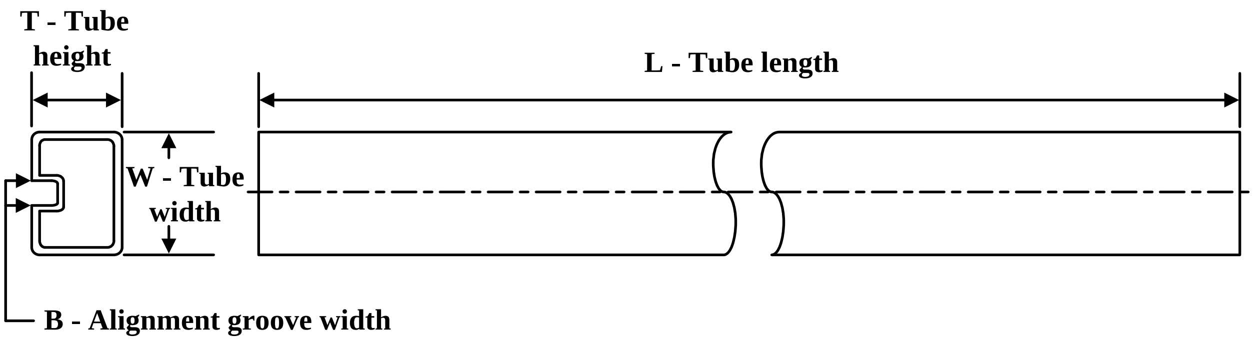
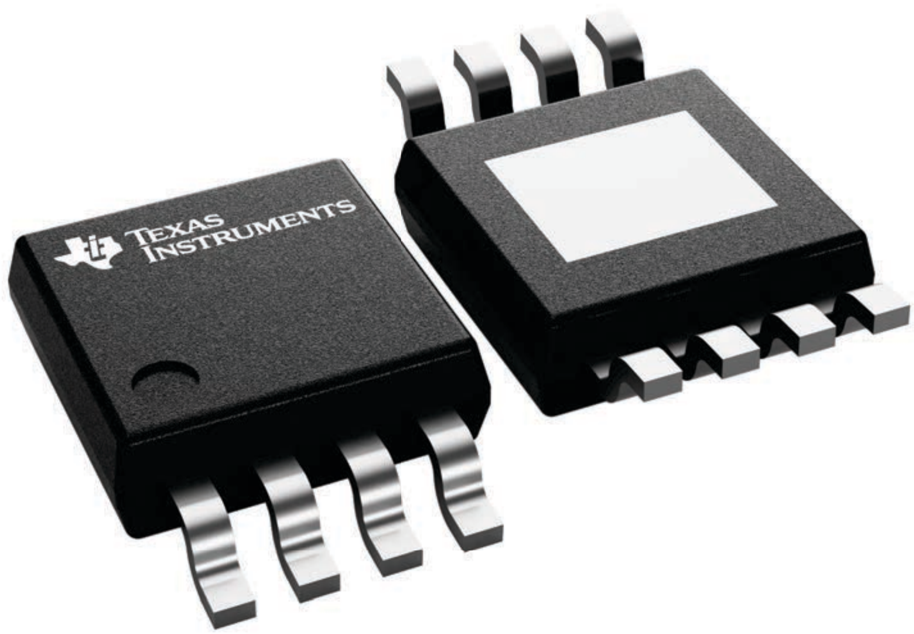
TUBE

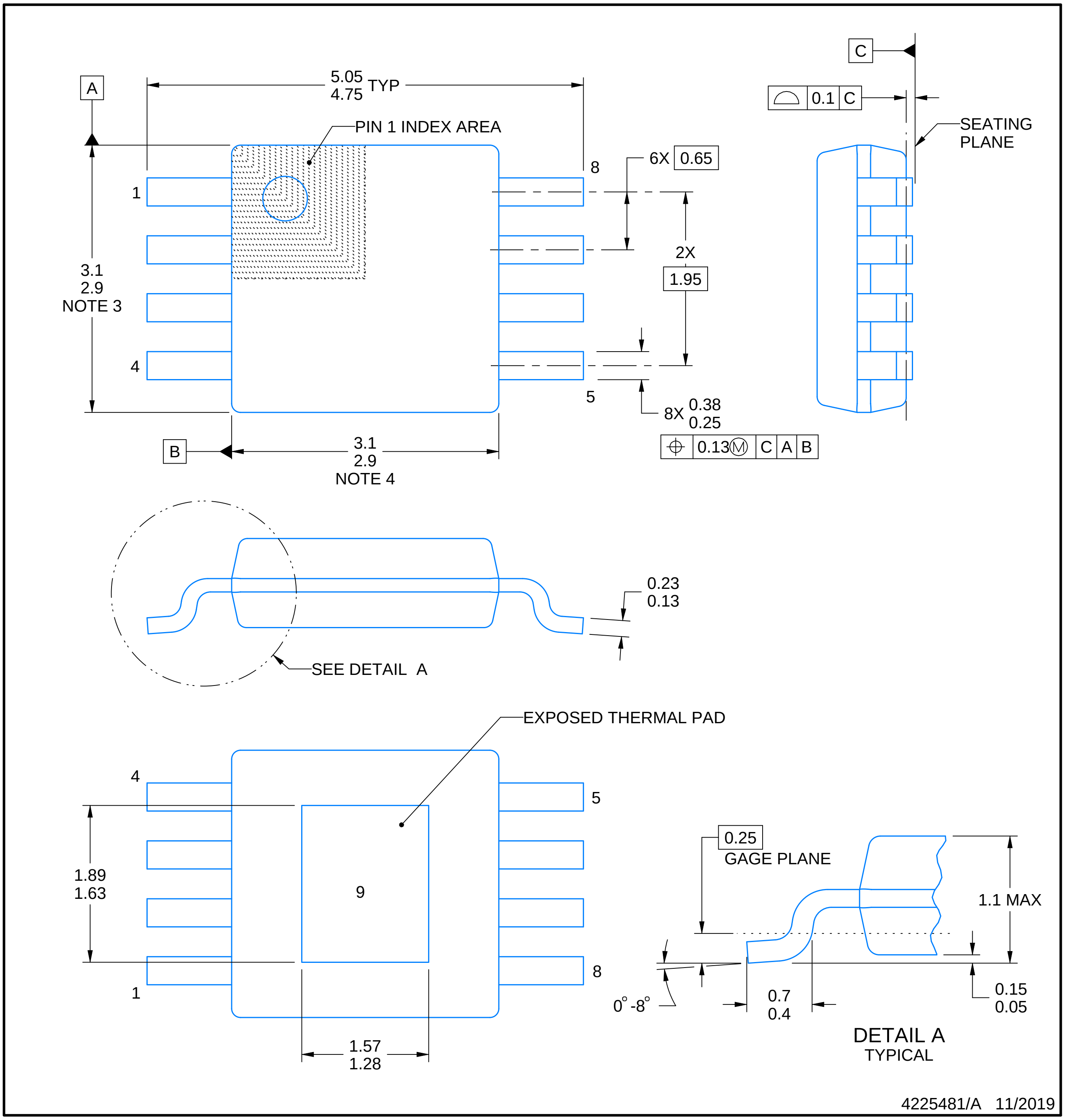


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPPM0302DGN	DGN	HVSSOP	8	80	331.47	6.55	3000	2.88
TPPM0302DGN.A	DGN	HVSSOP	8	80	331.47	6.55	3000	2.88

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



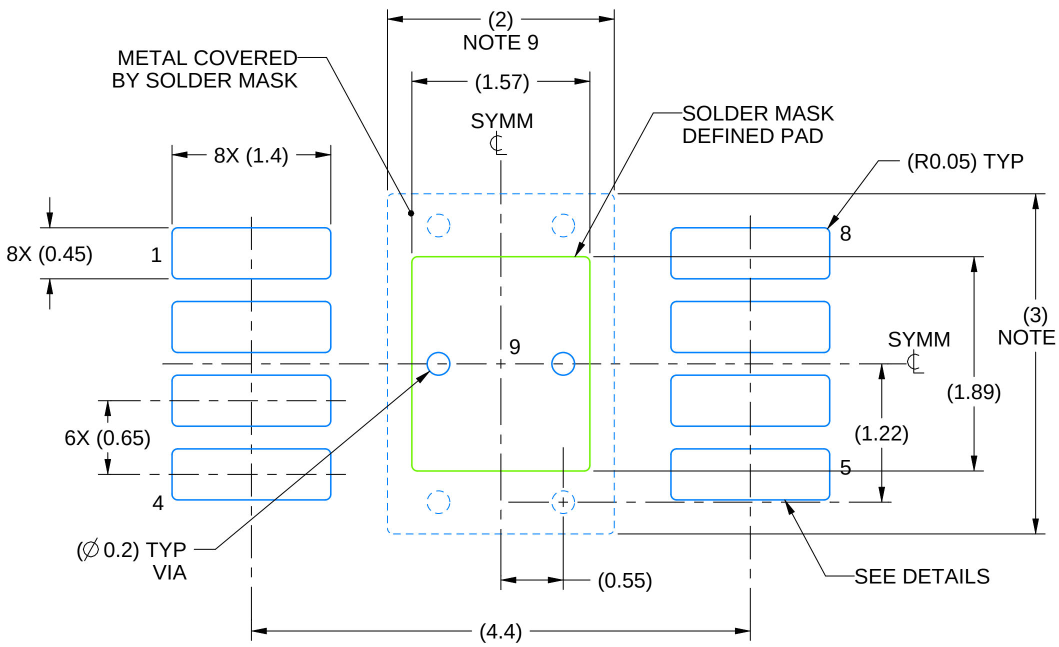


4225481/A 11/2019

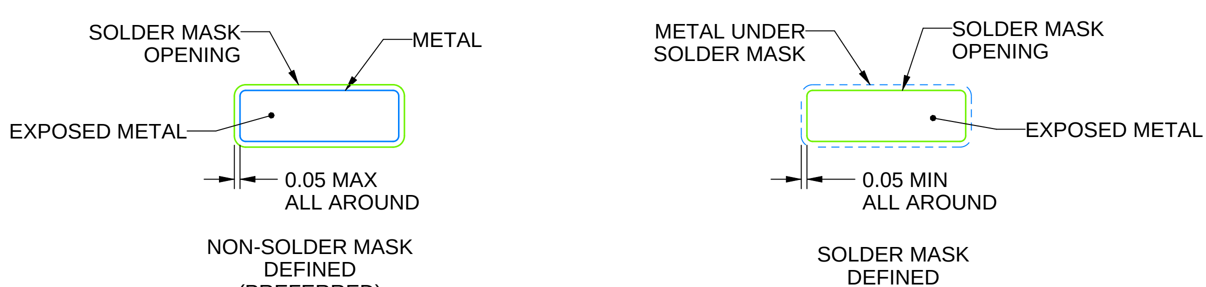
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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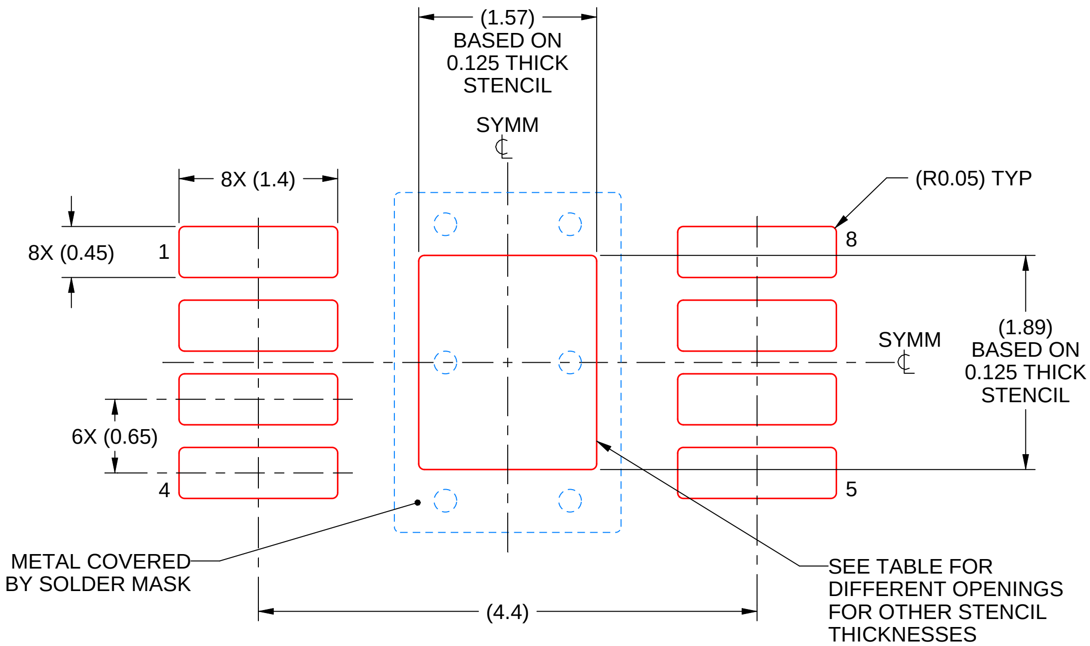
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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