TPD4S014 USB Charger Port Protection Including ESD Protection for All Lines and Overvoltage Protection on V_{BUS}

1 Features

- Input Voltage Protection at V_{BUS} up to 28 V
- Low Ron nFET Switch
- Supports > 2 A Charging Current
- ESD Performance D+/D–/ID/V_{BUS} Pins:
  - ±15-kV Contact Discharge (IEC 61000-4-2)
  - ±15-kV Air Gap Discharge (IEC 61000-4-2)
- Overvoltage and Undervoltage Lockout Features
- Low Capacitance TVS ESD Clamp for USB2.0 High Speed Data Rate
- Internal 17 ms Startup Delay
- Integrated Input Enable and Status Output Signal
- Thermal Shutdown Feature
- Space Saving SON Package (2 mm × 2 mm)

2 Applications

- Cell Phones
- eBook
- Portable Media Players
- Digital Camera

3 Description

The TPD4S014 is a single-chip solution for USB charger port protection. This device offers low capacitance transient voltage suppressor (TVS) electrostatic discharge (ESD) clamps for the D+, D–, and standard capacitance for the ID pin. On the V_{BUS} pin, this device provides overvoltage protection (OVP) up to 28 V DC. The overvoltage lockout feature ensures that if there is a fault condition at the V_{BUS} line, the TPD4S014 is able to isolate the V_{BUS} line to protect the internal circuitry from damage. There is a 17-ms turn-on delay after V_{BUS} rises above the undervoltage lockout (UVLO) threshold in order to let the voltage stabilize before turning the nFET on. This function acts as a de-glitch and prevents unnecessary switching if there is any ringing on the line during connection.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPD4S014	WSON (10)	2.00 mm x 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Block Diagram

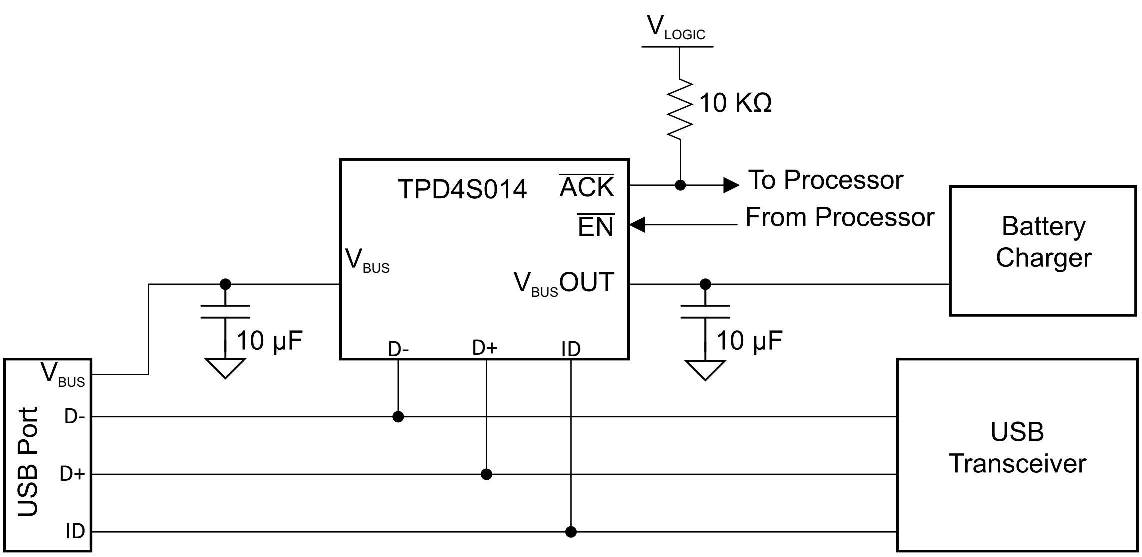


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (September 2015) to Revision G — **Page**

- Added a frequency test condition to capacitance in the *Electrical Characteristics* table. ... 6

Changes from Revision E (June 2014) to Revision F — **Page**

- Corrected V_{DROP} on nFET under load ... 10

Changes from Revision D (April 2014) to Revision E — **Page**

- Updated Recommended Operating Conditions table. ... 5
- Changed terminal name to I_{LEAK} from I_L ... 6
- Updated Electrical Characteristics OVP Circuits table. ... 7
- Changed t_{ON} MAX value from 18 ms to 22ms ... 7
- Changed t_{OFF} 8 µs value from MAX to TYP. ... 7
- Changed $t_{d(OVP)}$ 11 µs value from MAX to TYP. ... 7
- Changed t_{REC} MAX value from 9 ms to 10.5 ms. ... 7
- Updated Application and Implementation section. ... 13

Changes from Revision C (December 2011) to Revision D — **Page**

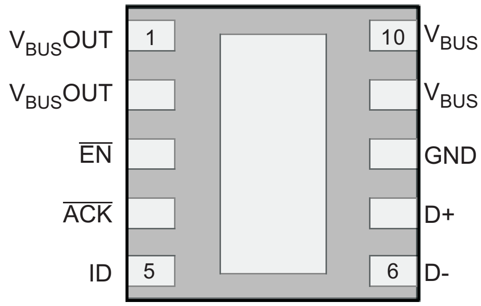
- Added ESD Ratings table. ... 5
- Added Recommended Operating Conditions table. ... 5
- Added Thermal Information table. ... 6
- Updated Electrical Characteristics OVP Circuits table. ... 7

Changes from Revision B (October 2011) to Revision C	Page
• Made changes to the datasheet to tighten the parameters, VOP+ changed from 5.55 V to 5.9 V.	1
• Updated Description.	1

Changes from Revision A (June 2011) to Revision B	Page
• Changed name of V_{CC} to V_{BUS}OUT throughout the entire document.	10
• Deleted row from Device Operation table.	12
• Added Eye Diagrams to Typical Characteristics section.	14

5 Pin Configuration and Functions

DSQ Package
10-Pin WSON
Top Side/See-Through View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
$V_{BUS}OUT$	1, 2	Power Output	Connect to PCB internal PCB plane
$\overline{EN}$	3	IO	Enable Active-Low Input. Drive EN low to enable the switch. Drive $\overline{EN}$ high to disable the switch.
$\overline{ACK}$	4	I	Open-Drain Adapter-Voltage Indicator Output. $\overline{ACK}$ is driven low after the VIN voltage is stable between UVLO and OVLO for 17 ms (typ). Connect a pullup resistor from $\overline{ACK}$ to the logic I/O voltage of the host system.
ID	5	IO	ESD-protected line
D–	6	IO	ESD-protected line
D+	7	IO	ESD-protected line
GND	8	Ground	Ground
V_{BUS}	9, 10	USB Input Power	Connector Side of V_{BUS}
Central PAD	Central PAD	Heat Sink	Electrically disconnected. Use as heat sink. Connect to GND plane via large PCB PAD

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
Maximum junction temperature	–40	150	°C
Max Voltage on V_{BUS}	–0.5	30	V
Continuous current through nFET		2.6	A
Continuous current through $\overline{ACK}$	–50	50	mA
Max Current through D+, D–, ID, V_{BUS} ESD clamps		50	mA
Max voltage on $\overline{EN}$, $\overline{ACK}$, D+, D-, ID, V_{BUS}OUT		6	V
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)		±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		±1000	
		IEC 61000-4-2 Contact Discharge	D+, D–, ID, V_{BUS} pins	±1500	
		IEC 61000-4-2 Air-gap Discharge	D+, D–, ID, V_{BUS} pins	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±1000 V may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
T_A	Operating free-air temperature		–40		85	°C
V_I	Input voltage	V_{BUSOUT}	–0.1		5.5	V
		V_{BUS}	–0.1		5.5	
		$\overline{EN}$	–0.1		5.5	
		$\overline{ACK}$	–0.1		5.5	
		D+, D-, ID,	–0.1		5.5	
I_{VBUS}	V_{BUS} continuous current(1)	V_{BUS}OUT			2.0	A
C_{VBUS}	Capacitance on V_{BUS}	V_{BUS} Pin		10		µF
C_{VBUS}OUT	Capacitance on V_{BUS}OUT	V_{BUS}OUT Pin		10		µF
$R_{\overline{ACK}}$	Pullup resistor on $\overline{ACK}$	$\overline{ACK}$ Pin		10		kΩ

(1) IV_{BUS} Max value is dependent on ambient temperature. See *Thermal Shutdown* section.

6.4 Thermal Information

THERMAL METRIC(1)		TPD4S014 DSQ (WSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	70.3	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	46.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	33.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	33.5	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	16.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics, $\overline{EN}$, $\overline{ACK}$, D+, D–, ID Pins

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage $\overline{EN}$	Load current = 50 µA	1			V
V_{IL}	Low-level input voltage $\overline{EN}$	Load current = 50 µA			0.5	V
I_{LEAK}	Input Leakage Current $\overline{EN}$, D+, D–, ID	V_{IO} = 3.3 V			1	µA
V_{OL}	Low-level output voltage $\overline{ACK}$	I_{OL} = 2 mA			0.1	V
V_D	Diode forward Voltage D+, D–, ID pins; lower clamp diode	I_O = 8 mA			0.95	V
ΔC_{IO}	Differential Capacitance between the D+, D– lines			0.03		pF
C_{IO}	Capacitance to GND for the D+, D– lines	f = 1 MHz		1.6		pF
$C_{IO\text{-}ID}$	Capacitance to GND for the ID line			19		pF
V_R	Reverse stand-off voltage of D+, D- and ID pins			5		V
V_{BR}	Breakdown voltage D+, D–, ID pins	I_{BR} = 1 mA	6			V
$V_{BR\ VBUS}$	Breakdown voltage on V_{BUS}	I_{BR} = 1 mA	28			V
R_{DYN}	Dynamic on resistance D+, D–, ID clamps	I_I = 1 A		1		Ω

6.6 Electrical Characteristics OVP Circuits

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT UNDERVOLTAGE LOCKOUT							
V_{UVLO+}	Under-voltage lock-out, input power detected threshold rising		V_{BUS} increasing from 0 V to 5 V, No load on OUT pin	2.65	2.8	3	V
$V_{UVLO–}$	Under-voltage lock-out, input power detected threshold falling		V_{BUS} decreasing from 5 V to 0 V, No load on OUT pin	2.25	2.44	2.7	V
$V_{HYS\text{-}UVLO}$	Hysteresis on UVLO		Δ of V_{UVLO+} and $V_{UVLO–}$	150	360	550	mV
INPUT TO OUTPUT CHARACTERISTICS							
$R_{DS\_VBUSSWITCH}$	V_{BUS} switch resistance		V_{BUS} = 5 V, I_{OUT} = 500 mA		151	200	mΩ
t_{ON}	Turn-ON time		V_{BUS} increasing from 2.8 V to 4.75 V, $\overline{EN}$ = 0 V, R_L = 36 Ω, C_L = 10 uF	16	17.4	22	ms
t_{OFF}	Turn-OFF time		V_{BUS} decreasing from 2.44 V to 0.5 V, $\overline{EN}$ = 0V, R_L = 36 Ω, C_L = 10 uF		8		µs
INPUT OVERVOLTAGE PROTECTION (OVP)							
V_{OVP+}	Input over –voltage protection threshold rising	V_{BUS}	V_{BUS} increasing from 5 V to 7 V, No Load	5.9	6.15	6.45	V
V_{OVP-}	Input over –voltage protection threshold falling	V_{BUS}	V_{BUS} decreasing from 7 V to 5 V, No Load	5.75	5.98	6.24	V
$V_{HYS\text{-}OVP}$	Hysteresis on OVP	V_{BUS}	Δ of V_{OVP+} and $V_{OVP–}$	25	100	275	mV
$t_{d(OVP)}$	Over voltage delay	V_{BUS}	R_L = 36 Ω, C_L = 10 µF; V_{BUS} increasing from 5 V to 7 V		11		µs
t_{REC}	Recovery time from input over voltage condition	V_{BUS}	R_L = 36 Ω, C_L = 10 µF; V_{BUS} decreasing from 7 V to 5 V		8	10.5	ms

6.7 Supply Current Consumption

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VBUS}	V_{BUS} Operating Current Consumption	No load on V_{BUS_OUT} pin, V_{BUS} = 5 V, $\overline{EN}$ = 0 V		147.6	160	µA
I_{VBUS_OFF}	V_{BUS} Operating Current Consumption	No load on V_{BUS_OUT} pin, V_{BUS} = 5 V, $\overline{EN}$ = 5 V		111.8	120	µA

6.8 Thermal Shutdown Feature

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{SHDN}	Thermal Shutdown			144		°C
$T_{SHDN\text{-}HYS}$	Thermal-Shutdown Hysteresis			23		°C

6.9 Typical Characteristics

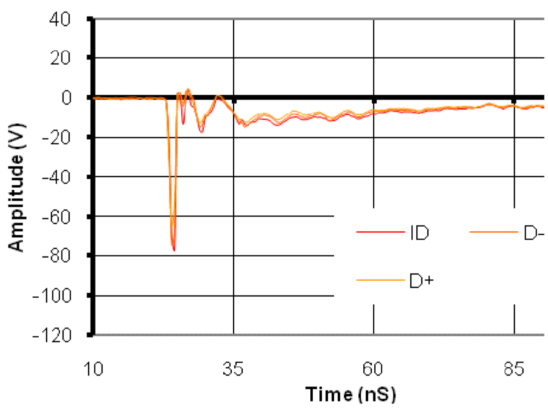


Figure 1. IEC61000-4-2 -8-kV Contact Waveform

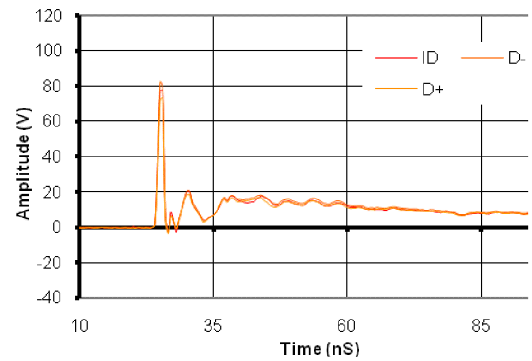


Figure 2. IEC61000-4-2 +8-kV Contact Waveform

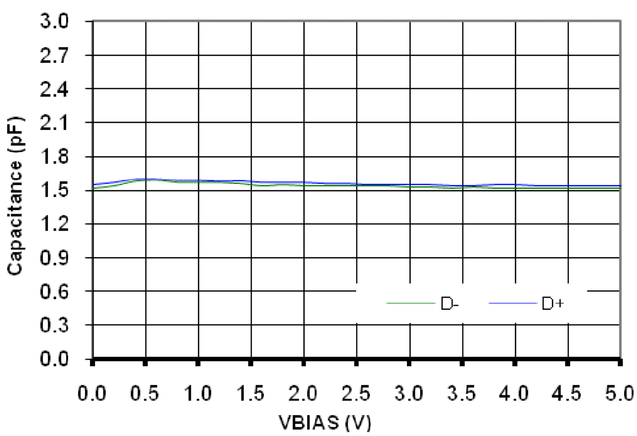


Figure 3. Capacitance Variation With Voltage

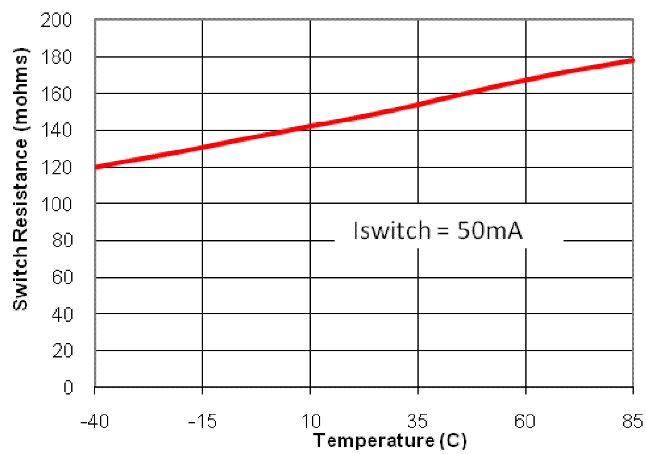


Figure 4. Variation of On Resistance with Ambient Temperature

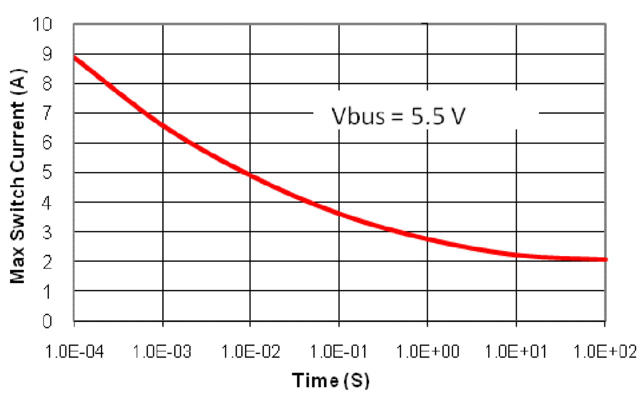


Figure 5. Max Pulse Current Through Switch vs Pulse Duration

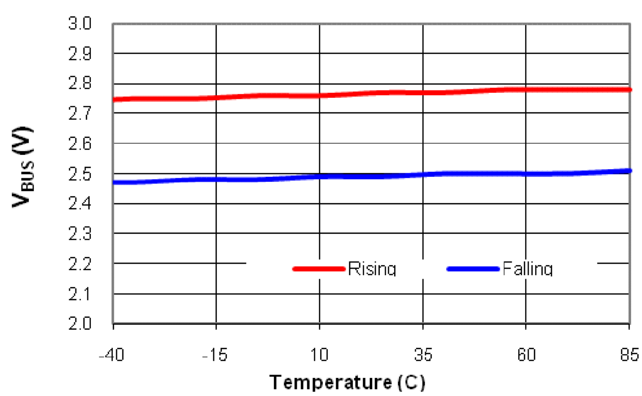


Figure 6. UVLO Threshold Variation With Temperature

Typical Characteristics (continued)

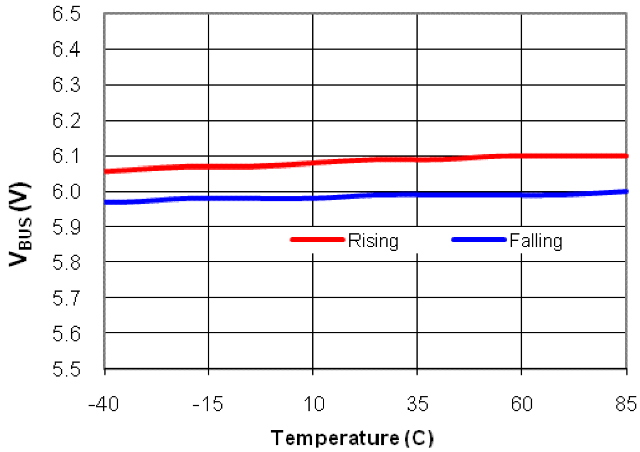


Figure 7. OVP Threshold Variation With Temperature

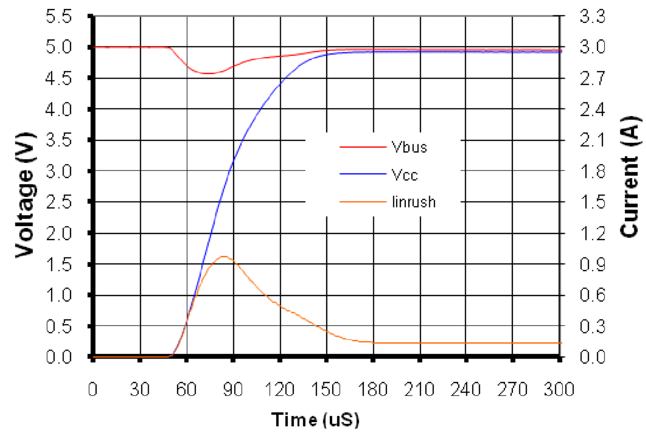


Figure 8. Start Up Inrush Current Characteristics

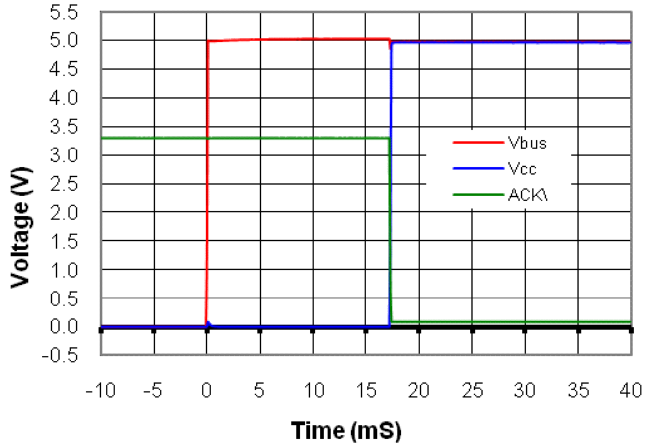


Figure 9. Device Turn on Characteristics

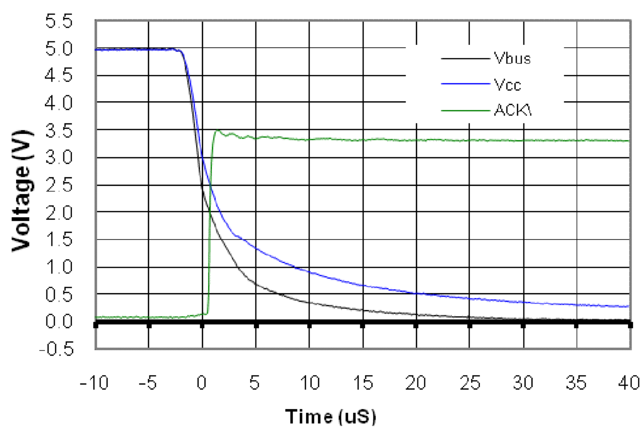


Figure 10. Device Turn OFF Characteristics (Undervoltage)

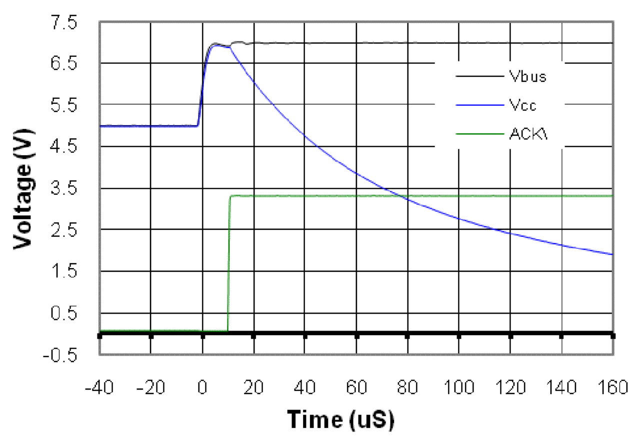


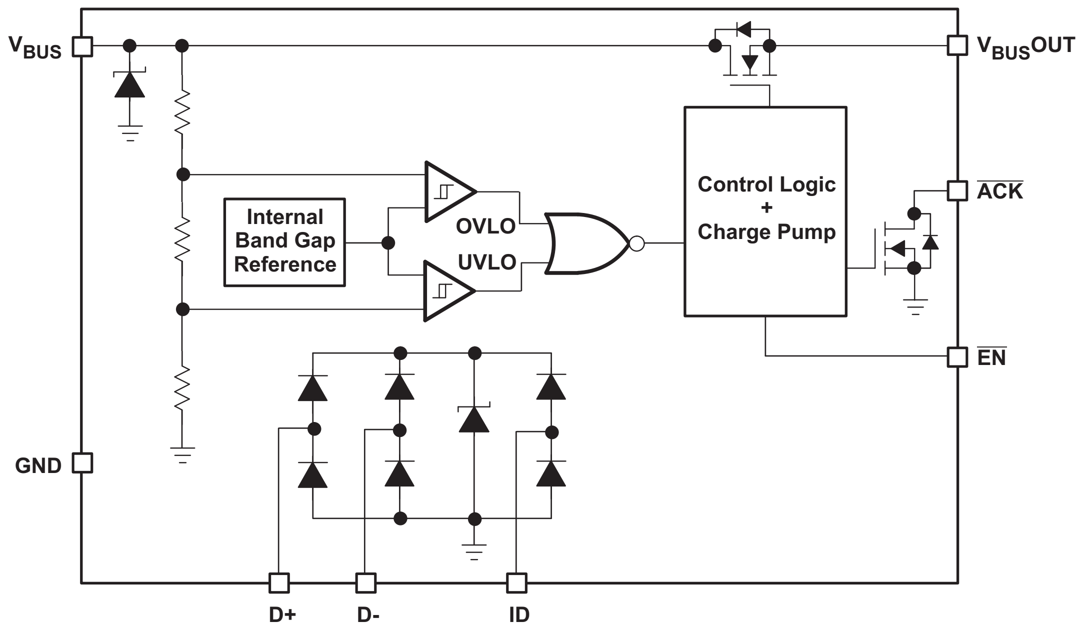
Figure 11. Device Turn OFF Characteristics (Overvoltage)

7 Detailed Description

7.1 Overview

The TPD4S014 provides a single-chip protection solution for USB charger interfaces. The V_{BUS} line is tolerant up to 28 V DC. A Low RON nFET switch is used to disconnect the downstream circuits in case of a fault condition. At power-up, when the voltage on V_{BUS} is rising, the switch will close 17 ms after the input crosses the under voltage threshold, thereby making power available to the downstream circuits. The TPD4S014 also has an $\overline{ACK}$ output, which de-asserts to alert the system a fault has occurred. The TPD4S014 offers 4 channel ESD clamps for D+, D-, ID, and V_{BUS} pins that provide IEC61000-4-2 level 4 ESD protection. This eliminates the need for external TVS clamp circuits in the application.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input Voltage Protection at V_{BUS} up to 28 V DC

When the input voltage rises above V_{OVP}, or drops below the V_{UVLO}, the internal V_{BUS} switch is turned off, removing power to the application. The $\overline{ACK}$ signal is de-asserted when a fault condition is detected. If the fault was an over voltage event, the V_{BUS} nFET switch turns on 8 ms (t_{REC}) after the input voltage returns below V_{OVP} – V_{HYS_OVP} and remains above V_{UVLO}. If the fault was an under voltage event, the switch turns on 17 ms after the voltage returns above V_{UVLO+} (similar to start up). When the switch turns on, the $\overline{ACK}$ is asserted once again.

7.3.2 Low RON nFET Switch

The nFET switch has a total on resistance (R_{ON}) of 151 mΩ. This equates to a voltage drop of 302 mV when charging at the maximum 2.0 A current level. Such low RON helps provide maximum potential to the system as provided by an external charger.

7.3.3 ESD Performance D+/D–/ID/V_{BUS} Pins

The D+, D–, ID, and V_{BUS} pins can withstand ESD events up to ±15-kV contact and air-gap. An ESD clamp diverts the current to ground.

Feature Description (continued)

7.3.4 Overvoltage and Undervoltage Lockout Features

The over voltage and under voltage lockout feature ensures that if there is a fault condition at the V_{BUS} line, the TPD4S014 is able to isolate the V_{BUS} line and protect the internal circuitry from damage. Due to the body diode of the nFET switch, if there is a short to ground on V_{BUS} the system is expected to limit the current to V_{BUS}OUT.

7.3.5 Capacitance TVS ESD Clamp for USB2.0 Hi-Speed Data Rate

The D+/D– ESD protection pins have low capacitance so there is no significant impact to the signal integrity of the USB 2.0 Hi-Speed data rate.

7.3.6 Start-up Delay

Upon startup, TPD4S014 has a built in startup delay. An internal oscillator controls a charge pump to control the turn-on delay (t_{ON}) of the internal nFET switch. The internal oscillator controls the timers that enable the turn-on of the charge pump and sets the state of the open-drain $\overline{ACK}$ output. If $V_{BUS} < V_{UVLO}$ or if $V_{BUS} > V_{OVLO}$, the internal oscillator remains off, thus disabling the charge pump. At any time, if V_{BUS} drops below V_{UVLO} or rises above V_{OVLO}, $\overline{ACK}$ is released and the nFET switch is disabled.

7.3.7 OVP Glitch Immunity

A 17 ms deglitch time has been introduced into the turn on sequence to ensure that the input supply has stabilized before turning the nFET switch ON. Noise on the V_{BUS} line could turn ON the nFET switch when the fault condition is still active. To avoid this, OVP glitch immunity allows noise on the V_{BUS} line to be rejected. Such a glitch protection circuitry is also introduced in the turn off sequence in order to prevent the switch from turning off for voltage transients. The glitch protection circuitry integrates the glitch over time, allowing the OVP circuitry to trigger faster for larger voltage excursions above the OVP threshold and slower for shorter excursions.

7.3.8 Integrated Input Enable and Status Output Signal

External control of the nFET switch is provided by an active low $\overline{EN}$ pin. An $\overline{ACK}$ pin provides output logic to acknowledge V_{BUS} is between UVLO and OVP by asserting low.

7.3.9 Thermal Shutdown

When the device is ON, current flowing through the device will cause the device to heat up. Overheating can lead to permanent damage to the device. To prevent this, an over temperature protection has been designed into the device. Whenever the junction temperature exceeds 145ºC, the switch will turn off, thereby limiting the temperature. The $\overline{ACK}$ signal will be asserted for an over temperature event. Once the device cools down to below 120ºC the $\overline{ACK}$ signal will be de-asserted, and the switch will turn on if the EN is active and the V_{BUS} voltage is within the UVLO and OVP thresholds. While the over temperature protection in the device will not kick-in unless the die temperature reaches 145ºC, it is generally recommended that care is taken to keep the junction temperature below 125 ºC. Operation of the device above 125 ºC for extended periods of time can affect the long-term reliability of the part.

The junction temperature of the device can be calculated using below formula:

$$T_j = T_a + P_D \theta_{JA}$$

where

- T_J = Junction temperature
- T_a = Ambient temperature
- θ_{JA} = Thermal resistance
- P_D = Power dissipated in device (1)

$$P_D = I^2 R_{on}$$

where

- I = Current through device
- R_{ON} = Max on resistance of device (2)

Feature Description (continued)

Example

At 2-A continuous current power dissipation is given by:

$$P_D = 2^2 \times 0.2 = 0.8W$$

If the ambient temperature is about 60°C the junction temperature will be:

$$T_j = 60 + (0.8 \times 70.3) = 116.24$$

This implies that, at an ambient temperature of 60ºC, TPD4S014 can pass a continuous 2 A without sustaining damage. Conversely, the above calculation can also be used to calculate the total continuous current the TPD4S014 can handle at any given temperature.

7.4 Device Functional Modes

Table 1 is the function table for TPD4S014.

Table 1. Function Table

OTP	UVLO	OVLO	$\overline{EN}$	SW	$\overline{ACK}$
X	H	X	X	OFF	H
X	X	H	X	OFF	H
L	L	L	H	OFF	L
L	L	L	L	ON	L
H	X	X	X	OFF	H

OTP = Over temperature protection circuit active
UVLO = Under voltage lock-out circuit active
OVLO = Over voltage lock-out circuit active
SW = Load switch
CP = Charge pump
X = Don’t Care
H = True
L = False

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPD4S014 is a single-chip solution for USB charger port protection. This device offers low capacitance TVS type ESD clamps for the D+, D–, and standard capacitance for the ID pin. On the V_{BUS} pin, this device can handle over voltage protection up to 28 V. The over voltage lockout feature ensures that if there is a fault condition at the V_{BUS} line TPD4S014 is able to isolate the V_{BUS} line and protect the internal circuitry from damage. In order to let the voltage stabilize before closing the switch there is a 17 ms turn on delay after V_{BUS} crosses the UVLO threshold. This function acts as a de-glitch which prevents unnecessary switching if there is any ringing on the line during connection. Due to the body diode of the nFET switch, if there is a short to ground on V_{BUS} the system is expected to limit the current to V_{BUS}OUT.

8.2 Typical Applications

8.2.1 For Non-OTG USB Systems

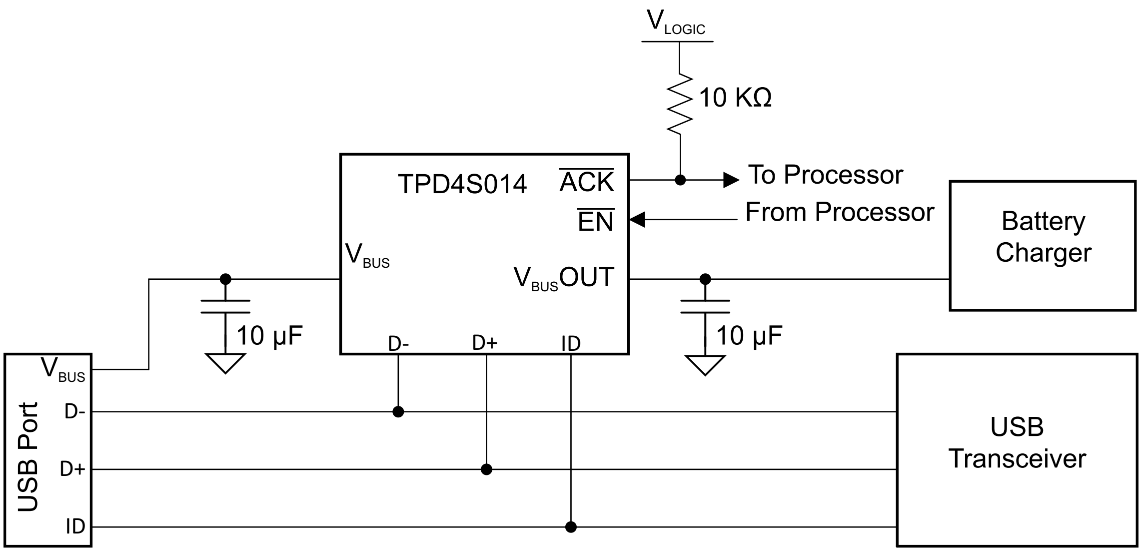


Figure 12. Non-OTG Schematic

8.2.1.1 Design Requirements

Table 2 shows the design parameters.

Table 2. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
Signal range on V_{BUS}	3.3 V – 5.9 V
Signal range on V_{BUS}OUT	3.9 V – 5.9 V
Signal range on D+/D– and ID	0 V – 5 V
Drive $\overline{EN}$ low (enabled)	0 V – 0.5 V
Drive $\overline{EN}$ high (disabled)	1 V – 6 V

8.2.1.2 Detailed Design Procedure

To begin the design process, some parameters must be decided upon. The designer needs to know the following:

- V_{BUS} voltage range
- Processor logic levels V_{OH}, V_{OL} for $\overline{EN}$ and V_{IH}, V_{IL} for $\overline{ACK}$ pins

8.2.1.3 Application Curves

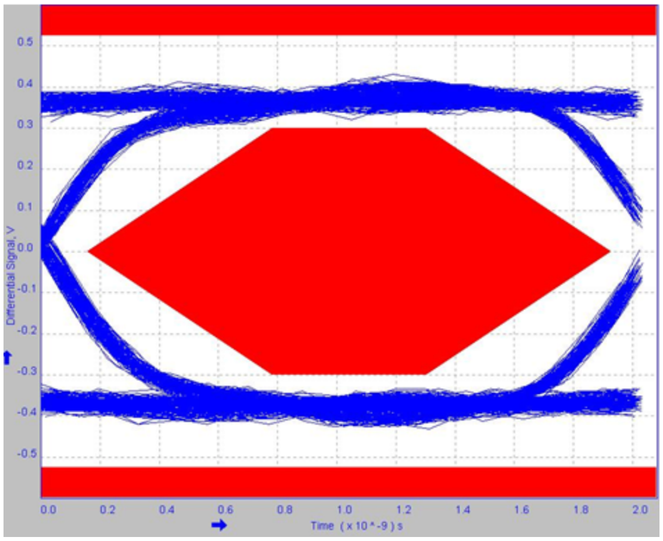


Figure 13. Eye Diagram With No EVM and No IC, Full USB2.0 Speed at 480 Mbps

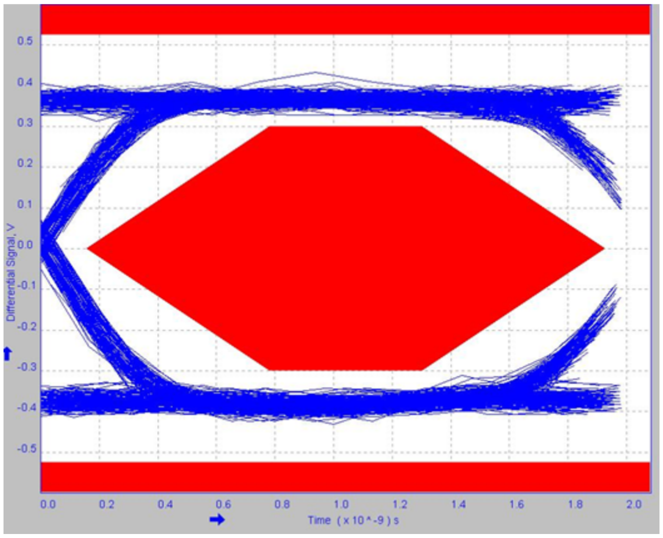


Figure 14. Eye Diagram With EVM, No IC, Full USB2.0 Speed at 480 Mbps

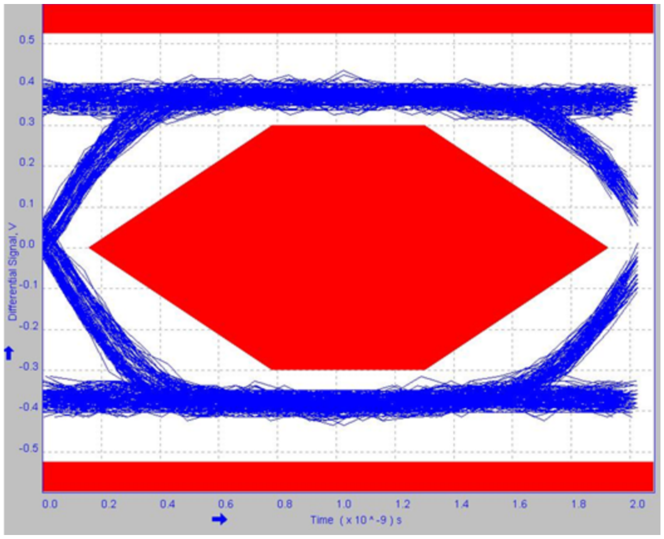


Figure 15. Eye Diagram With EVM and IC, Full USB2.0 Speed at 480 Mbps

8.2.2 For OTG USB Systems

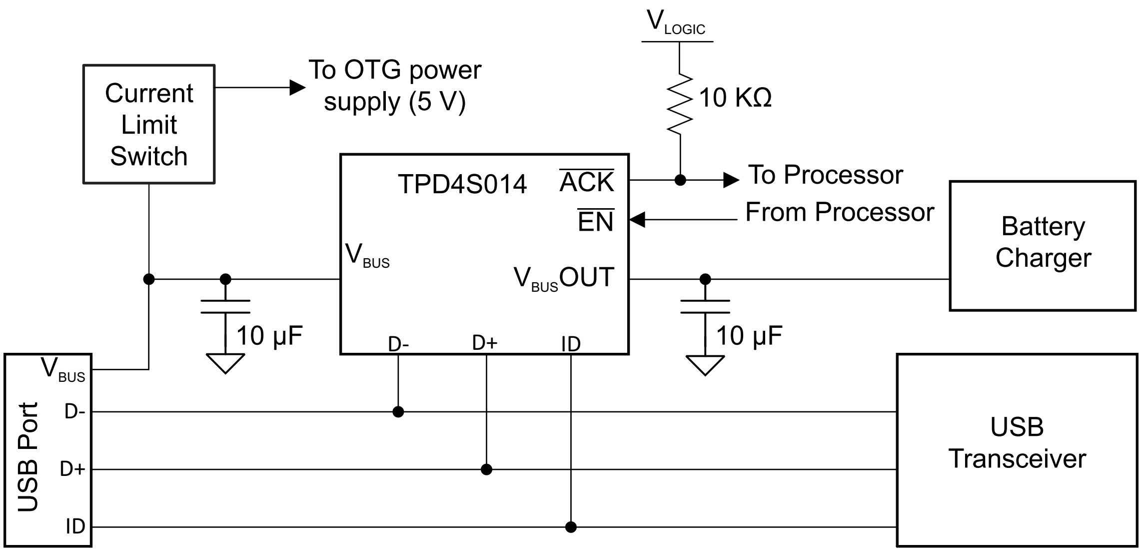


Figure 16. OTG Schematic

8.2.2.1 Design Requirements

Table 3 shows the design parameters.

Table 3. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
Signal range on V_{BUS}	3.3 V – 5.9 V
Signal range on V_{BUS}OUT	3.9 V – 5.9 V
Signal range on D+/D– and ID	0 V – 5 V
Drive $\overline{EN}$ low (enabled)	0 V – 0.5 V
Drive $\overline{EN}$ high (disabled)	1 V – 6 V

8.2.2.2 Detailed Design Procedure

To begin the design process, some parameters must be decided upon. The designer needs to know the following:

- V_{BUS} voltage range
- Processor logic levels V_{OH}, V_{OL} for $\overline{EN}$ and V_{IH}, V_{IL} for $\overline{ACK}$ pins
- OTG power supply output voltage range

8.2.2.3 Application Curves

Refer to *Application Curves* in the previous section.

9 Power Supply Recommendations

TPD4S014 Is designed to receive power from a USB 3.0 (or lower) V_{BUS} source. It can operate normally (nFET ON) between 3.0 V and 5.9 V. Thus, the power supply (with a ripple of V_{RIPPLE}) requirement for TPD4S014 to be able to switch the nFET ON is between 3.0 V + V_{RIPPLE} and 5.9 V – V_{RIPPLE}.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
  - Keep traces between the connector and TPD4S014 on the same layer as TPD4S014.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

When designing layout for TPD4S014, note that V_{BUS}OUT and V_{BUS} pins allow for extra wide traces for good power delivery. In the example shown, these pins are routed with 25 mil (0.64 mm) wide traces. Place the V_{BUS}OUT and V_{BUS} capacitors as close to the device pins as possible. Pull $\overline{ACK}$ up to the Processor logic level high with a resistor. Use external and internal ground planes and stitch them together with VIAs as close to the GND pins of TPD4S014 as possible. This allows for a low impedance path to ground so that the device can properly dissipate any ESD events.

10.2 Layout Example

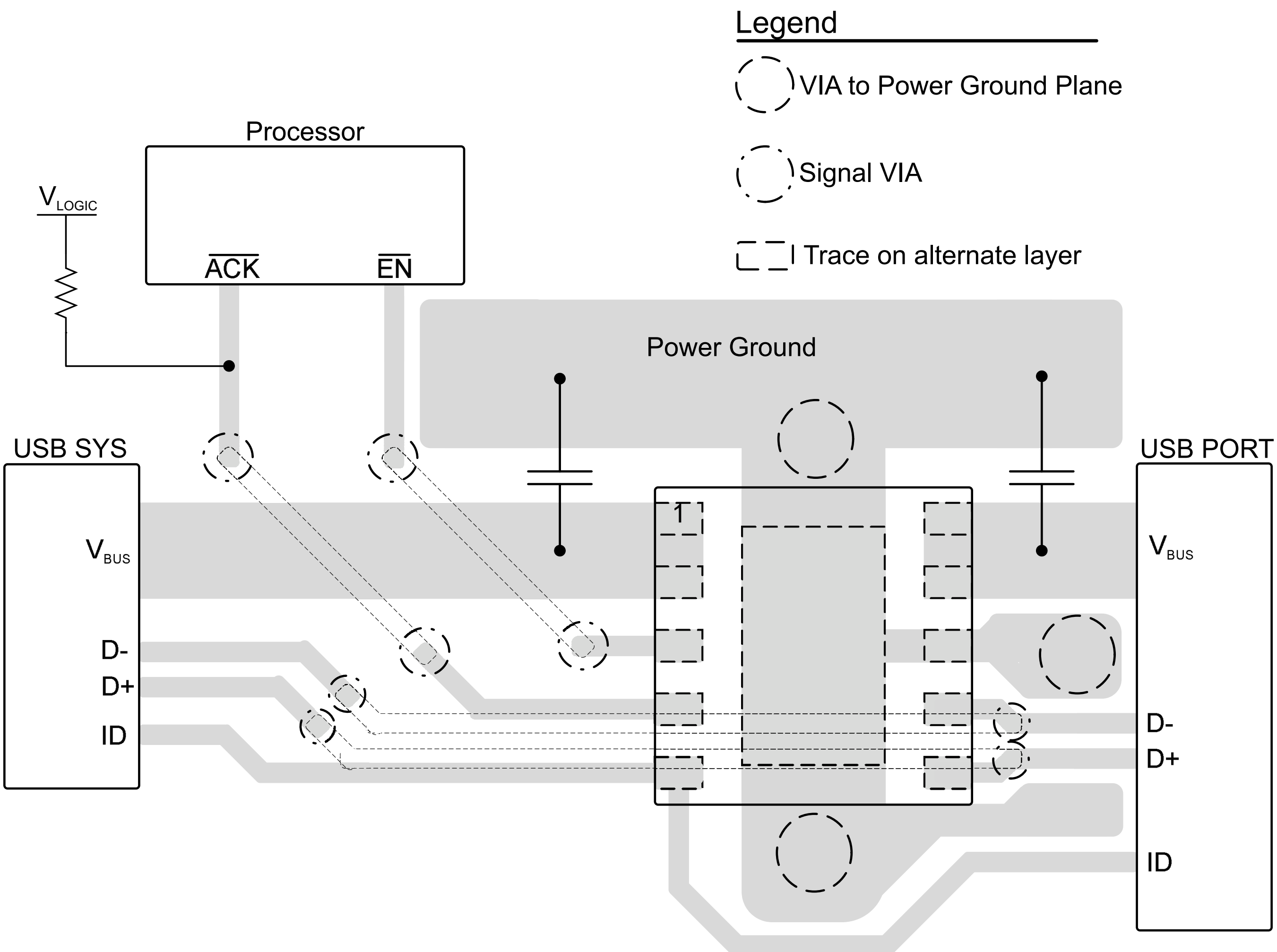


Figure 17. Layout Recommendation

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPD4S014DSQR	Active	Production	WSON (DSQ) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZTE
TPD4S014DSQR.A	Active	Production	WSON (DSQ) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZTE

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

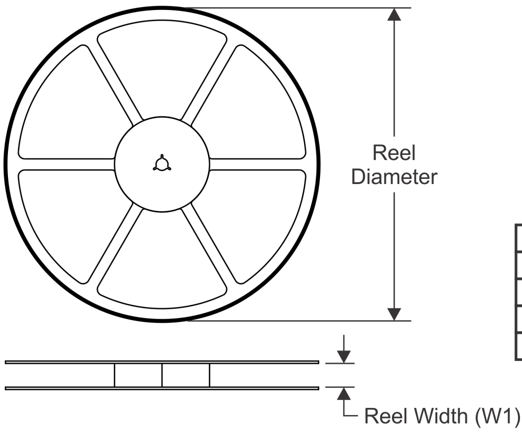
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

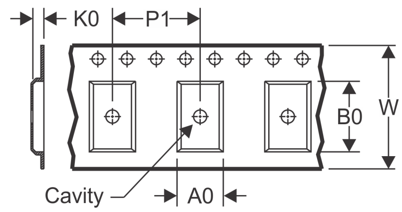
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

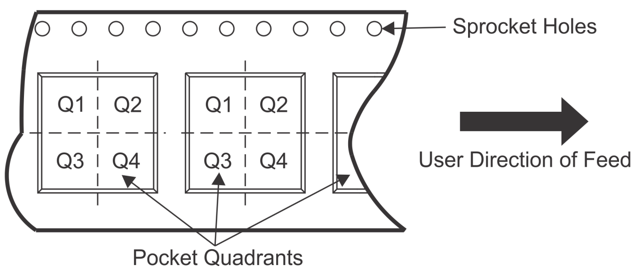


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

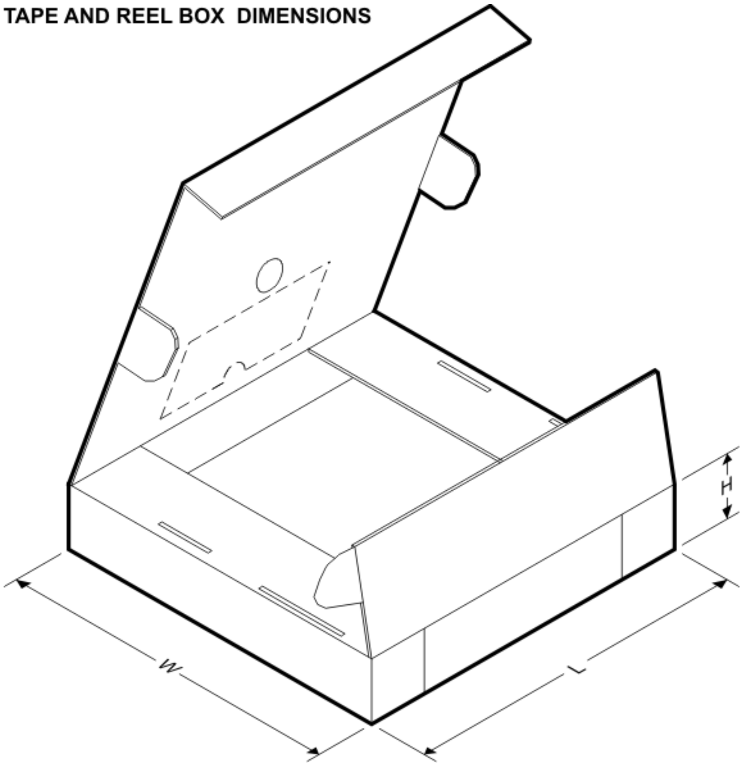
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

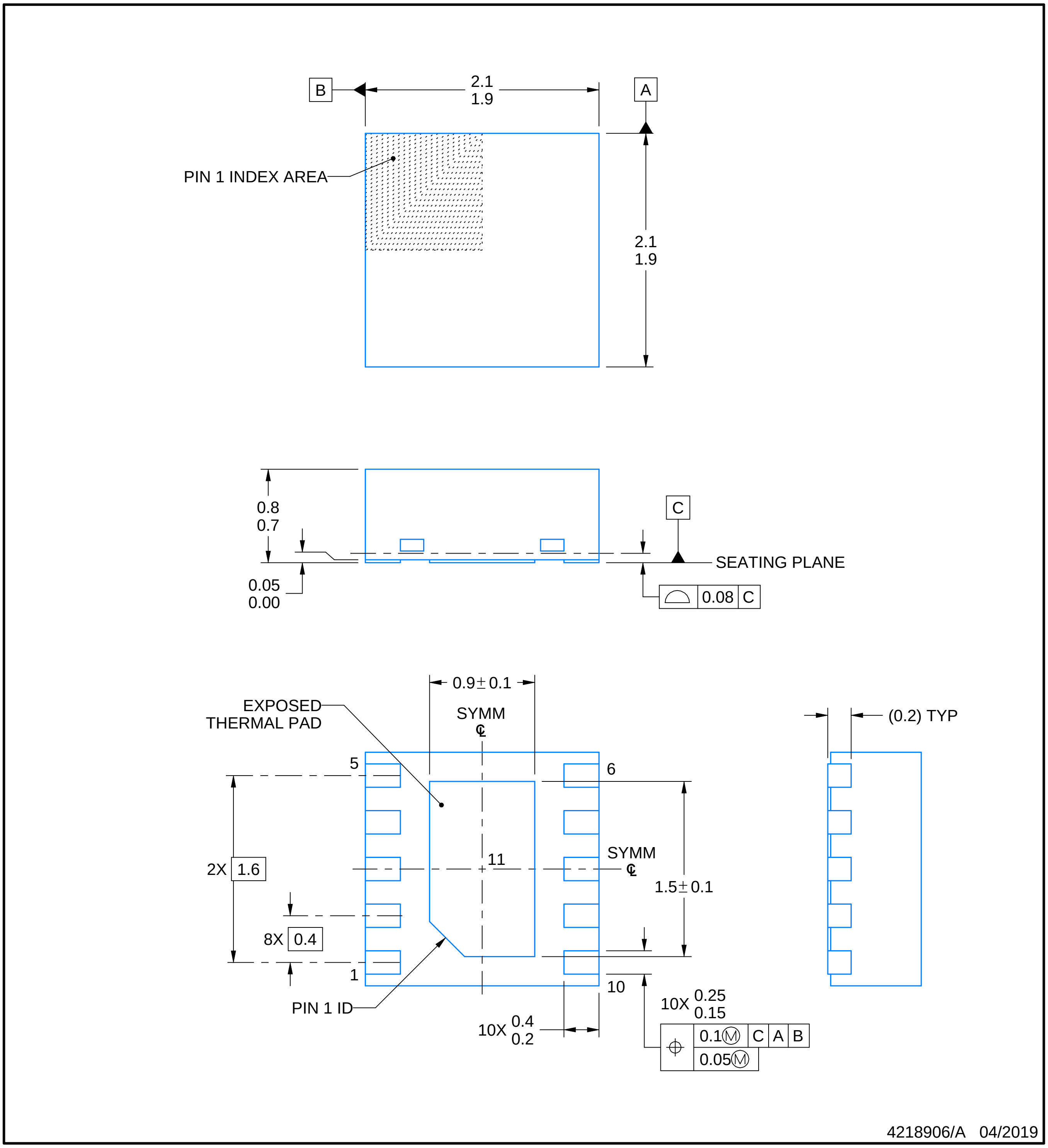
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD4S014DSQR	WSON	DSQ	10	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



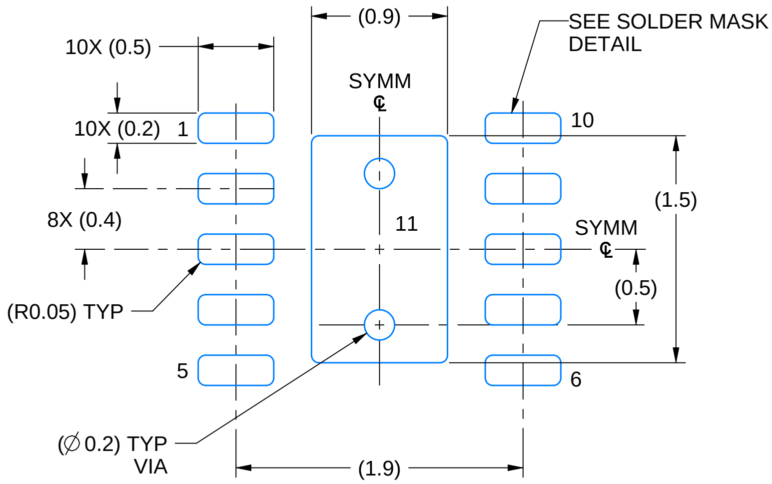
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD4S014DSQR	WSON	DSQ	10	3000	213.0	191.0	35.0

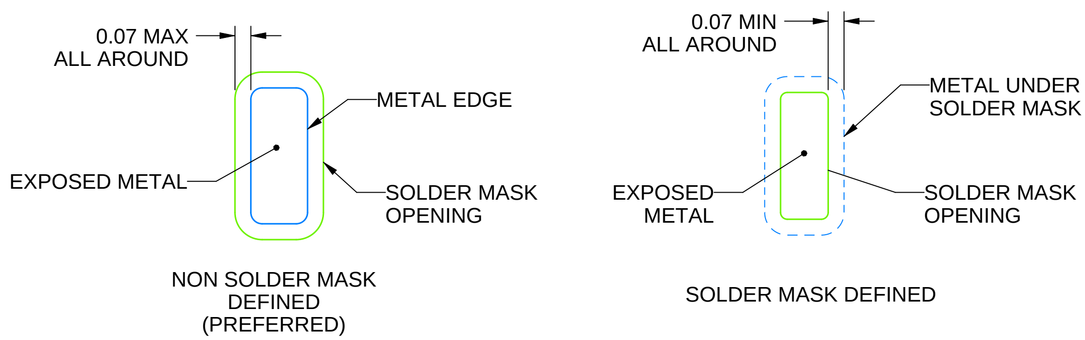


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

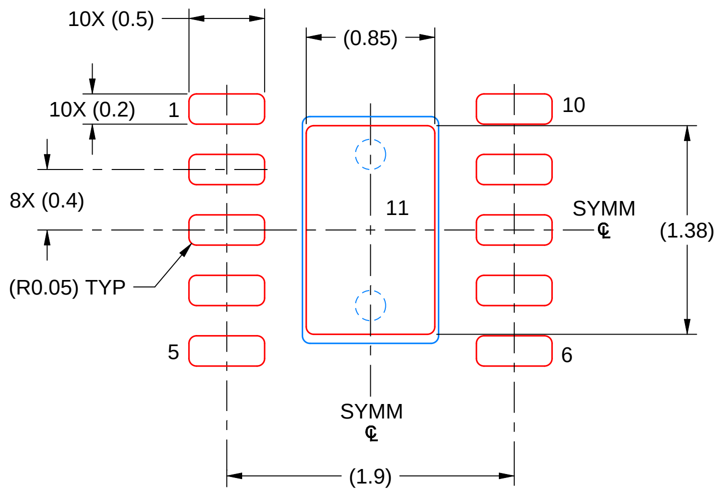


SOLDER MASK DETAILS

4218906/A 04/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 11
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4218906/A 04/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.