参考資料

TPD3S714-Q1 バッテリ短絡および短絡保護機能搭載、車載 USB 2.0 インターフェイス保護

1 特長

- AEC-Q100 認定済み (グレード 1)
  - 動作温度範囲：-40℃～+125℃
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- V_{BUS_CON} のバッテリ短絡保護 (最高 18V) とグランド短絡保護
- VD+、VD– のバッテリ短絡保護 (最高 18V) と V_{BUS} 短絡保護
- V_{BUS_CON}、VD+、VD– の IEC 61000-4-2 ESD 保護
  - 接触放電 ±8kV
  - エアギャップ放電±15kV
- V_{BUS_CON}、VD+、VD– の ISO 10605 (330pF、330Ω) ESD 保護
  - 接触放電 ±8kV
  - エアギャップ放電±15kV
- 低 R_{ON} nFET V_{BUS} スイッチ (標準値 63mΩ)
- 高速データ・ スイッチ (1GHz、–3dB 帯域幅)
- ヒカップ電流制限
  - 過電流制限：550mA (最小値)
- 高速な過電圧応答時間
  - V_{BUS} スイッチ：2μs (標準値)
  - データ・ スイッチ：200ns (標準値)
- V_{BUS}、VD+、VD– の入力イネーブルを内蔵
- フォルト出力信号
- サーマル・ シャットダウン機能
- 16 ピンの SSOP パッケージ (4.9mm × 3.9mm)

2 アプリケーション

- 最終製品
  - ヘッド・ ユニット
  - リアシート用エンターテイメント
  - テレマティクス
  - USB ハブ
  - ナビゲーション・ モジュール
  - メディア・ インターフェイス
- インターフェイス
  - USB 2.0

3 概要

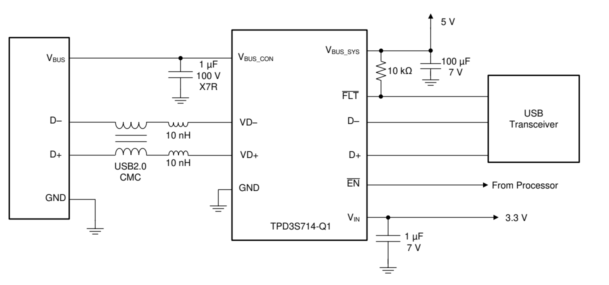
TPD3S714-Q1 は、車載用 USB ハブ、ヘッド・ ユニット、リア・ シート用エンターテインメント、テレマティクス、メディア・ インターフェイス・ アプリケーションにおける USB コネクタの V_{BUS} およびデータ・ ラインのバッテリ短絡、短絡、ESD 保護のためのシングルチップ・ ソリューションです。この統合型データ・ スイッチは、USB のバッテリ短絡イベント中も最小限の信号劣化でクラス最高の帯域幅を提供します。1GHz という広い帯域幅により、車載 USB 環境で一般的な長いキャプティブ・ ケーブルでも USB 2.0 ハイスピード (480Mbps) のクリーンなアイ・ ダイアグラムを得ることができます。

バッテリへの短絡保護機能は、V_{BUS_CON}、VD+、VD– ピンのすべての過電圧条件から内部システム回路を保護します。これらのピンのホットプラグおよび DC イベントのために、TPD3S714-Q1 は最大 18V の過電圧に対応できます。過電圧保護回路は業界でも最も信頼性の高いバッテリ短絡絶縁を行い、スイッチをシャットオフして、危険な電圧や電流スパイクから上流のトランシーバを保護します。V_{BUS_CON} ピンは、最大 0.5A の高精度電流制限付きロード・ スイッチにも使用できます。過電流保護回路は、グランドへの短絡中にアップストリーム・ レールがドループしないように、電流を自動的に制限します。またこのデバイスは、V_{BUS_CON}、VD+、VD– ピンにシステム・ レベルの IEC 61000-4-2 および ISO 10605 ESD 保護を組み込んでいるため、外付けの高耐圧低容量 ESD ダイオードは不要です。

製品情報 (1) (1 ページ)

型番	パッケージ	本体サイズ (公称)
TPD3S714-Q1	SSOP (16)	4.90mm×3.90mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



代表的なアプリケーション回路図

English Data Sheet: SLVSCG4

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (August 2017) to Revision C (August 2020)	Page
• 文書全体にわたって表、図、相互参照の採番方法を更新	1
• *「特長」*セクションに機能安全のリンクを追加	1

Changes from Revision A (April 2016) to Revision B (August 2017)	Page
• Updated *ESD Protection on V_{BUS_CON}, VD+, VD–* section	15

Changes from Revision * (January 2016) to Revision A (April 2016)	Page
• *「代表的なアプリケーション回路図」* 図 7-1 (12 ページ) を更新、 図 7-2 (13 ページ)	1
• *「電気的特性」*表を更新	1
• *バッテリ短絡の許容値に内容を追加*	1
• *「代表特性」の IEC 波形グラフをより見やすいデータで更新*	1

5 Pin Configuration and Functions

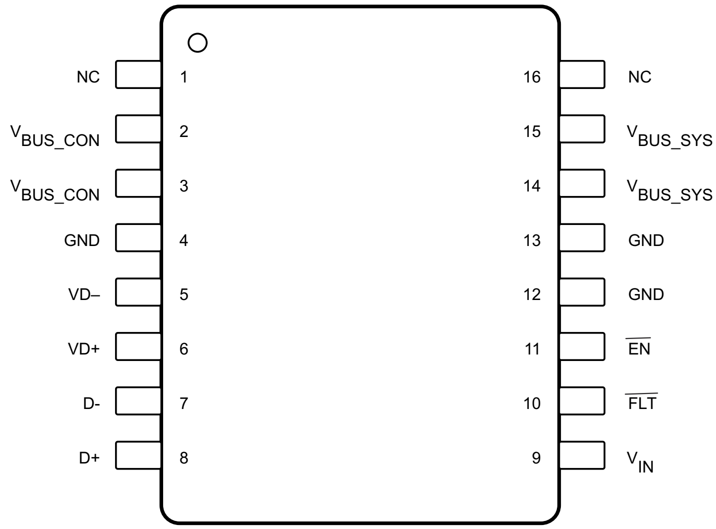


図 5-1. DBQ Package 16-Pin SSOP Top View

Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	NC	NC	No connect, leave floating or connect to ground. Do not connect to V_{BUS_CON}
2	V_{BUS_CON}	O	Connect to USB connector V_{BUS_CON}; provides IEC 61000-4-2 ESD protection
3			
4	GND	Ground	Connect to PCB ground plane
5	VD–	I/O	Connect to USB connector D–; provides IEC 61000-4-2 ESD protection
6	VD+	I/O	Connect to USB connector D+; provides IEC 61000-4-2 ESD protection
7	D–	I/O	Connect to internal D– transceiver
8	VD+	I/O	Connect to internal D+ transceiver
9	V_{IN}	I	Connect to 3.3-V I/O. Controls the OVP threshold for VD+/VD–
10	$\overline{FLT}$	O	Open-Drain fault pin. Refer device description for operation
11	$\overline{EN}$	I	Enable Active-Low Input. Drive $\overline{EN}$ low to enable the device. Drive $\overline{EN}$ high to disable the device
12	GND	Ground	Connect to PCB ground plane
13			
14	V_{BUS_SYS}	I	Connect to internal V_{BUS} plane
15			
16	NC	NC	No connect, leave floating or connect to ground. Do not connect to V_{BUS_CON}

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2)

		MIN	MAX	UNIT
V_{BUS_CON}	Supply voltage from USB connector	–0.3	18	V
V_{BUS_SYS}	Internal supply DC voltage rail on the PCB	–0.3	6	V
VD+, VD–	Voltage range from connector-side USB data lines	–0.3	18	V
D+, D–	Voltage range for internal USB data lines	–0.3	V_{IN} + 0.3	V
V_{IN}	Voltage range for V_{IN} supply input	–0.3	4	V
$\overline{EN}$	Voltage on enable pin		7	V
T_A	Operating free air temperature	–40	125	°C
T_{STG}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

6.2 ESD Ratings—AEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1]	±4000	V
		Charged-device model (CDM), per AEC Q100-011	±1500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 ESD Ratings—IEC Specification

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2, V_{BUS_CON}, VD+, VD– pins	Contact discharge[1]	±8000	V
			Air-gap discharge[1]	±15000	

(1) See the *ESD System Test Setup* diagram for details on system level ESD testing setup.

6.4 ESD Ratings—ISO Specification

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	ISO 10605 (330 pF, 330 Ω), V_{BUS_CON}, VD+, VD– pins	Contact discharge[1]	±8000	V
			Air-gap discharge[1]	±15000	

(1) See the *ESD System Test Setup* diagram for details on system level ESD testing setup.

6.5 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{BUS_CON}	Supply voltage from USB connector				5.25	V
V_{BUS_SYS}	Internal supply DC voltage rail on the PCB		4.75		5.25	V
VD+, VD–	Voltage range from connector-side USB data lines		0		V_{IN} + 0.3	V
D+, D–	Voltage range for internal USB data lines		0		V_{IN} + 0.3	V
V_{IN}	Voltage range for V_{IN} supply		3		3.6	V
I_{BUS}	Current through V_{BUS} switch				500	mA
$\overline{EN}$	Voltage range for enable		0		5.9	V
C_{SYS}	Input capacitance[1]	V_{BUS_SYS} pin		100		µF

6.5 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
C_{LOAD}	Output load capacitance[(1)]	V_{BUS_CON} pin	1			µF
C_{VIN}	V_{IN} capacitance[(1)]	V_{IN} pin	1			µF

(1) See 図 9-1 for configuration details

6.6 Thermal Information

THERMAL METRIC[(1)]		TPD3S714-Q1 DBQ (SSOP) 16 PINS	UNIT
$θ_{JA}$	Junction-to-ambient thermal resistance	98.8	°C/W
$θ_{JCtop}$	Junction-to-case (top) thermal resistance	48	°C/W
$θ_{JB}$	Junction-to-board thermal resistance	41.6	°C/W
$ψ_{JT}$	Junction-to-top characterization parameter	8.5	°C/W
$ψ_{JB}$	Junction-to-board characterization parameter	41.2	°C/W
$θ_{JCbot}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.7 Electrical Characteristics

over operating free-air temperature range, $\overline{EN}$ = 0 V, V_{BUS_SYS} = 5 V, V_{IN} = 3.3 V, VD+/VD–/D+/D–/V_{BUS_CON} = float (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT CONSUMPTION							
I_{VBUS_SLEEP}	V_{BUS} sleep current consumption		Measured at V_{BUS_SYS} pin, $\overline{EN}$ = 5 V		45	150	µA
I_{VBUS}	V_{BUS} operating current consumption		Measured at V_{BUS_SYS} pin		285	380	µA
I_{VIN}	Leakage current for V_{IN}		Measured at V_{IN} pin, V_{IN} = 3.6 V		12	25	µA
$I_{ON(LEAK)}$	Leakage through V_{BUS} while shorted to battery and powered on		Measured flowing in to V_{BUS_SYS} pin, V_{BUS_SYS} = 5 V, V_{BUS_CON} = 18 V			120	µA
$I_{OFF(LEAK)}$	Leakage through V_{BUS} while shorted to battery and unpowered		Measured flowing out of V_{BUS_SYS} pin, V_{BUS_SYS} = 0 V, V_{BUS_CON} = 18 V			50	µA
$I_{VD(OFF\_LEAK)}$	Leakage into data path while shorted to battery and unpowered		Measured flowing in to VD+ or VD– pins, V_{BUS_SYS} = 0 V, VD+ or VD– = 18 V, V_{IN} = 0 V, D+/D– = 0 V			80	µA
$I_{VD(ON\_LEAK)}$	Leakage into data path while shorted to battery and powered on		Measured flowing in to VD+ or VD– pins, V_{BUS_SYS} = 5 V, VD+ or VD– = 18 V, D+/D– = 0 V			80	µA
V_{IN} PIN							
$V_{UVLO(RISING)}$	Undervoltage lockout rising for V_{IN}	V_{IN}	Ramp V_{IN} down until $\overline{FLT}$ is deasserted, $\overline{EN}$ = 5 V	2.6	2.7	2.9	V
$V_{UVLO(FALLING)}$	Undervoltage lockout falling for V_{IN}	V_{IN}	Ramp V_{IN} until $\overline{FLT}$ is asserted, $\overline{EN}$ = 5 V	2.5	2.6	2.8	V
$\overline{EN}$, $\overline{FLT}$ PINS							
V_{IH}	High-level input voltage	$\overline{EN}$	Set $\overline{EN}$ = 0 V; Sweep $\overline{EN}$ to 1.4 V; Measure when $\overline{FLT}$ is asserted	1.2			V
V_{IL}	Low-level input voltage	$\overline{EN}$	Set $\overline{EN}$ = 3.3 V; Sweep $\overline{EN}$ from 3.3 V to 0.5 V; Measure when $\overline{FLT}$ is deasserted			0.8	V
I_{IL}	Input leakage current	$\overline{EN}$	$V_{(EN)}$ = 3.3 V ; Measure Current into EN pin			1	µA
V_{OL}	Low-level output voltage	$\overline{FLT}$	I_{OL} = 3 mA			0.4	V
OCP CIRCUIT—V_{BUS}							
I_{LIM}	Overcurrent limit	V_{BUS}	Progressively load V_{BUS_CON} until device asserts $\overline{FLT}$	550	700	850	mA

6.7 Electrical Characteristics (continued)

over operating free-air temperature range, $\overline{EN}$ = 0 V, V_{BUS_SYS} = 5 V, V_{IN} = 3.3 V, VD+/VD–/D+/D–/V_{BUS_CON} = float (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
OVERTEMPERATURE PROTECTION							
$T_{SD(RISING)}$	The rising overtemperature protection shutdown threshold		V_{BUS_SYS} = 5 V, $\overline{EN}$ = 0 V, No Load on V_{BUS_CON}, T_A stepped up until $\overline{FLT}$ is asserted	150	165	180	℃
$T_{SD(FALLING)}$	The falling overtemperature protection shutdown threshold		V_{BUS_SYS} = 5 V, $\overline{EN}$ = 0 V, No Load on V_{BUS_CON}, T_A stepped down from $T_{SD(RISING)}$ until $\overline{FLT}$ is deasserted	125	130	140	℃
$T_{SD(HYST)}$	The overtemperature protection shutdown threshold hysteresis		$T_{SD(RISING)} - T_{SD(FALLING)}$	10	35	55	℃
OVP CIRCUIT—V_{BUS}							
$V_{OVP(RISING)}$	Input overvoltage protection threshold	V_{BUS_CON}	Increase V_{BUS_CON} from 5 V to 7 V. Measure when $\overline{FLT}$ is asserted	5.4	5.6	5.8	V
$V_{HYS(OVP)}$	Hysteresis on OVP	V_{BUS_CON}	Difference between rising and falling OVP thresholds on V_{BUS_CON}		50		mV
$T_{OVP(FALLING)}$	Input overvoltage protection threshold	V_{BUS_CON}	Decrease V_{BUS_CON} from 7 V to 5 V. Measure when $\overline{FLT}$ is deasserted	5.36		5.74	V
$V_{UVLO(SYS\_RISING)}$	Undervoltage lockout rising for V_{BUS_SYS}	V_{BUS_SYS}	V_{BUS_SYS} voltage rising from 0 V to 5 V	3.1	3.3	3.6	V
$V_{HYS(UVLO\_SYS)}$	V_{BUS_SYS} UVLO hysteresis	V_{BUS_SYS}	Difference between rising and falling UVLO thresholds on V_{BUS_SYS}	50	75	100	mV
$V_{UVLO(SYS\_FALLING)}$	Undervoltage lockout falling for V_{BUS_SYS}	V_{BUS_SYS}	V_{BUS_SYS} voltage falling from 7 V to 3 V	3	3.2	3.5	V
$V_{SHRT(RISING)}$	Short-to-ground comparator rising threshold	V_{BUS_CON}	Increase V_{BUS_CON} voltage from 0 V until the device transitions from the short-circuit to over-current mode of operation	2.5	2.6	2.7	V
$V_{SHRT(FALLING)}$	Short-to-ground comparator falling threshold	V_{BUS_CON}	Set V_{BUS_SYS} = 5 V; V_{IN} = 3.3 V; $\overline{EN}$ = 0 V; Decrease V_{BUS_CON} voltage from 5 V until the device transitions from the overcurrent to short-circuit mode of operation	2.4	2.5	2.6	V
$V_{SHRT(HYST)}$	Short-to-ground comparator hysteresis	V_{BUS_CON}	Difference between $V_{SHRT(RISING)}$ and $V_{SHRT(FALLING)}$	100	125	150	mV
I_{SHRT}	Short-to-ground current source	V_{BUS_CON}	Current sourced from V_{BUS_SYS} when device is in short-circuit mode	150		350	mA
OVP CIRCUIT—VD+/VD–							
$V_{OVP(RISING)}$	Input overvoltage protection threshold	VD+/VD–	Increase VD+ or VD– (with D+ and D–) from 3.3 V to 4.5 V. Measure the value at which $\overline{FLT}$ is asserted	V_{IN} + 0.6	V_{IN} + 0.8	V_{IN} + 1	V
$V_{HYS(OVP)}$	Hysteresis on OVP	VD+/VD–	Difference between rising and falling OVP thresholds on VD+/VD–		50		mV
$V_{OVP(FALLING)}$	Input overvoltage protection threshold	VD+/VD–	Decrease VD+ or VD– (with D+ or D–) from 4.5 V to 2 V. Measure the value at $\overline{FLT}$ is deasserted	V_{IN} + 0.525	V_{IN} + 0.75	V_{IN} + 0.975	V
SHORT-TO-BATTERY							
$V_{(VBUS\_STB)}$	V_{BUS} hotplug short-to-battery tolerance	V_{BUS_CON}	Charge battery-equivalent capacitor to test voltage then discharge to pin under test through a 1-meter, 18-gauge wire. (See 図 7-1 for more details)			18	V
$V_{(DATA\_STB)}$	Data line hotplug short-to-battery tolerance	VD+/VD–				18	V
DATA LINE SWITCHES—VD+ to D+ or VD–to D–							
C_{ON}	Equivalent on capacitance		Capacitance of D+/D– switches when enabled - measure on connector side across bias voltage 0 V to 0.4 V		6.2		pF
R_{ON}	On resistance		Measure resistance between D+ and VD+ or D– and VD–, voltage between 0 and 0.4 V		4	6.5	Ω
$R_{ON(Flat)}$	On resistance flatness		Measure resistance between D+ and VD+ or D– and VD–, sweep voltage between 0 V and 0.4 V		0.2	1	Ω
BW_{ON}	On bandwidth (–3 dB)		Measure S_{21} bandwidth from D+ to VD+ or D– to VD– with voltage swing = 400 mVpp, V_{CM}= 0.2 V		860		MHz

6.7 Electrical Characteristics (continued)

over operating free-air temperature range, $\overline{EN}$ = 0 V, V_{BUS_SYS} = 5 V, V_{IN} = 3.3 V, VD+/VD–/D+/D–/V_{BUS_CON} = float (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BW_{ON_DIFF}	On bandwidth (–3 dB)	Measure S_{DD21} bandwidth from D+ to VD+ and D– to VD– with voltage swing = 800 mVpp differential, V_{CM} = 0.2 V		1050		MHz
X_{talk}	Crosstalk	Measure S_{21} bandwidth from D+ to VD– or D– to VD+ with voltage swing = 400 mVpp. Be sure to terminate open sides to 50 ohms. f = 480 MHz		–34		dB
nFET SWITCH—VBus						
$R_{(DISCHARGE)}$	Output discharge resistance	$\overline{EN}$ = 5 V, Set V_{BUS_CON} = 5 V and measure current flow to ground			12500	Ω
R_{ON}	Switch ON resistance	V_{BUS_CON} = 5 V, I_{OUT} = 0.5 A		63	150	mΩ

6.8 Timing Requirements

over operating free-air temperature range, $\overline{EN}$ = 0 V, V_{BUS_SYS} = 5 V, V_{IN} = 3.3 V, VD+/VD–/D+/D–/V_{BUS_CON} = float (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ENABLE PIN						
t_{ON}	Enable on time	Time between enable device until $\overline{FLT}$ deasserts		13		ms
OVERCURRENT PROTECTION						
t_{BLANK}	Overcurrent blanking time	Time from overcurrent condition until $\overline{FLT}$ assertion and V_{BUS} FET turnoff			2	ms
t_{RETRY}	Overcurrent retry time	Time from overcurrent FET shut off until FET turns back on		100		ms
t_{RECV}	Overcurrent recovery time	Time from end of t_{RETRY} until $\overline{FLT}$ deassertion if overcurrent condition is removed		8		ms
OVERVOLTAGE PROTECTION						
$t_{OVP\_response}$	OVP response time – V_{BUS}	Measured from OVP Condition to FET turnoff		2	4	µs
$t_{OVP\_response}$	OVP response time – data switches	Measured from OVP Condition to FET turnoff		200		ns
SHORT-TO-GROUND PROTECTION						
t_{SHRT}	Short to ground response time	C_{LOAD} = 0 uF, Time from short condition until current falls below 120% of I_{SHRT}		2	4	µs

6.9 Typical Characteristics

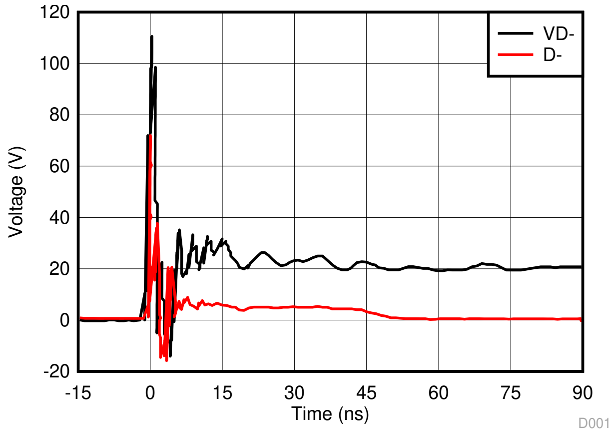


図 6-1. 8-kV IEC Contact Waveform

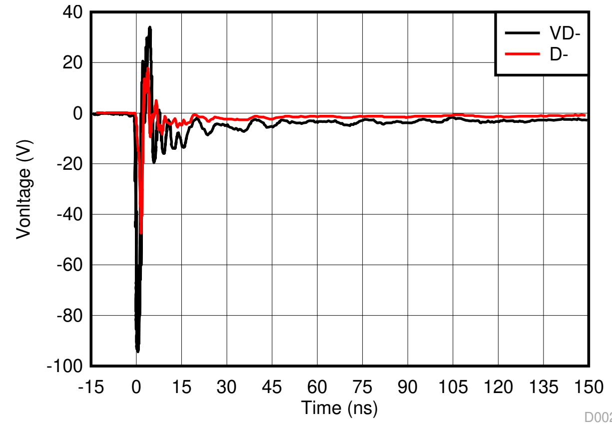


図 6-2. –8-kV IEC Contact Waveform

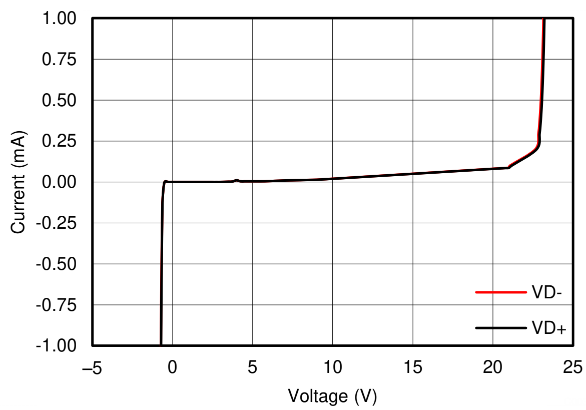


図 6-3. Data Line I-V Curve

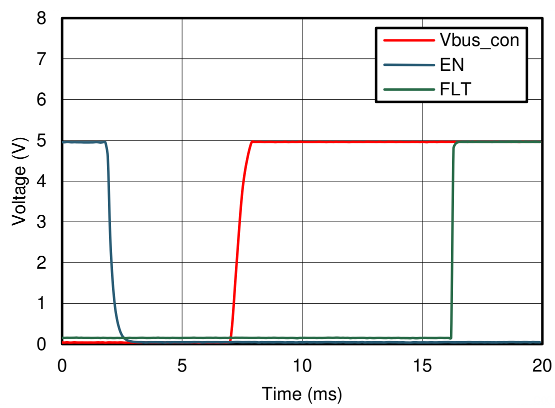


図 6-4. V_{BUS} t_{ON} Time

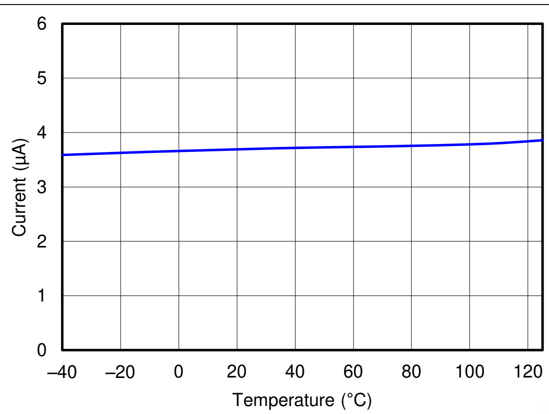


図 6-5. VD± Short-to-5 V (while Enabled) Across Temperature

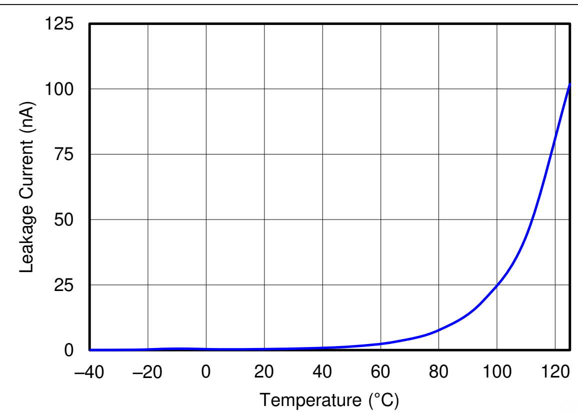


図 6-6. VD± Short-to-5 V (while Unpowered) Across Temperature

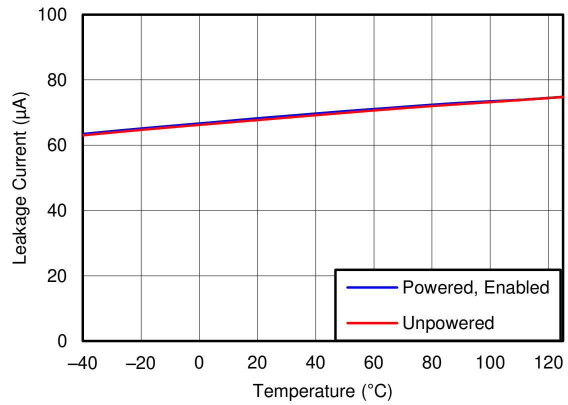


図 6-7. VD± Short-to-18 V Across Temperature

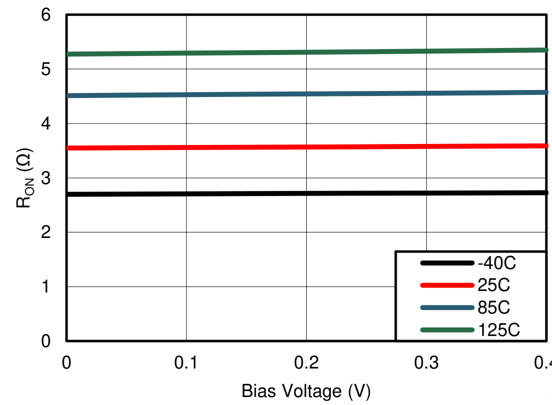


図 6-8. Data Switch R_{ON} vs Bias Voltage

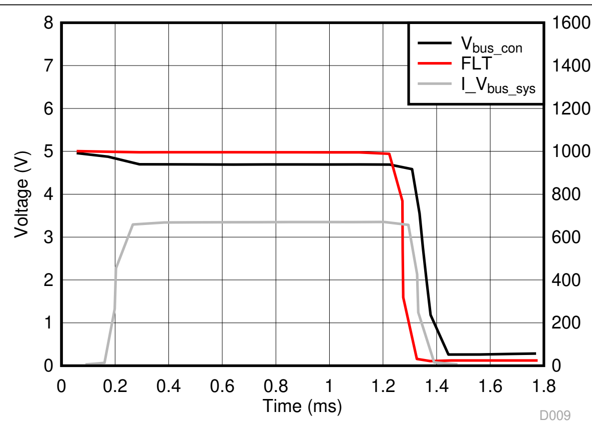


図 6-9. Overcurrent t_{BLANK} Response Waveform

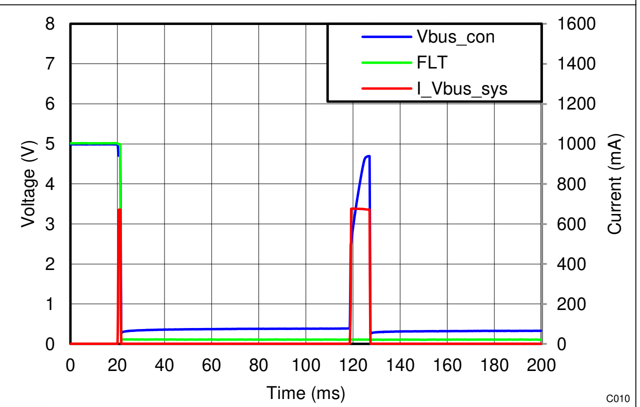


図 6-10. Overcurrent t_{BLANK_RETRY} Response Waveform

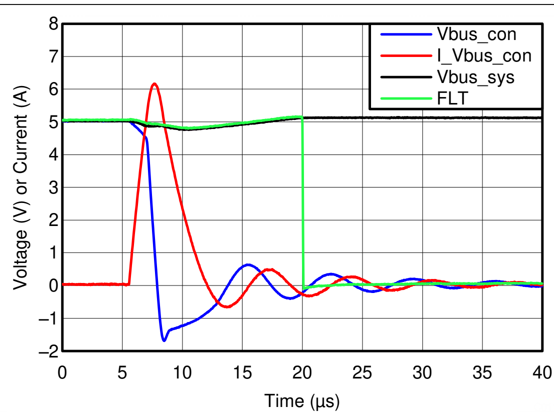


図 6-11. V_{BUS} Short-to-Ground Response Waveform

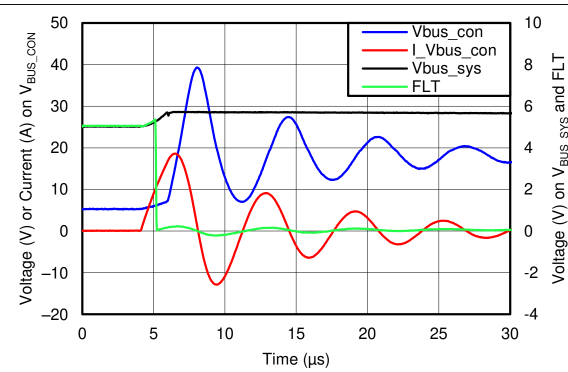


図 6-12. V_{BUS} Short-to-18 V Response Waveform

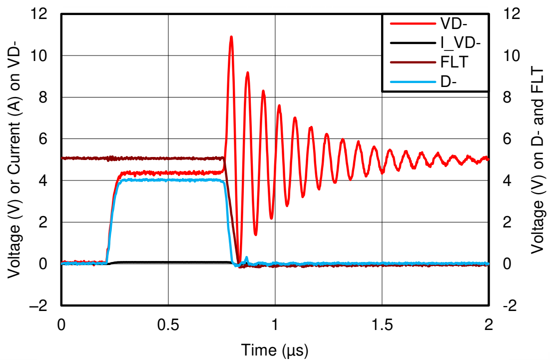


図 6-13. Data Switch Short-to-5 V Response Waveform

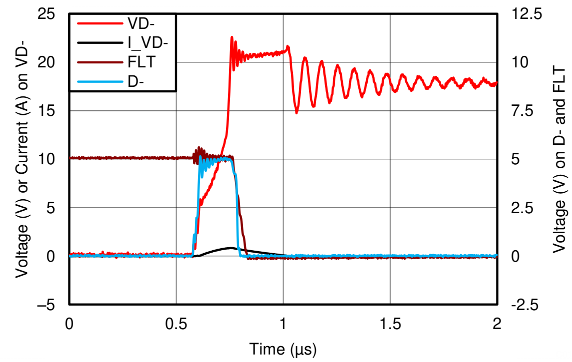


図 6-14. Data Switch Short-to-18 V Response Waveform

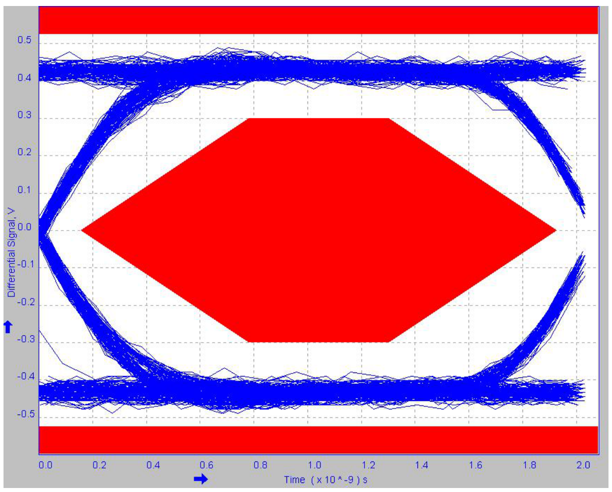


図 6-15. USB2.0 Eye Diagram (No TPD3S714-Q1)

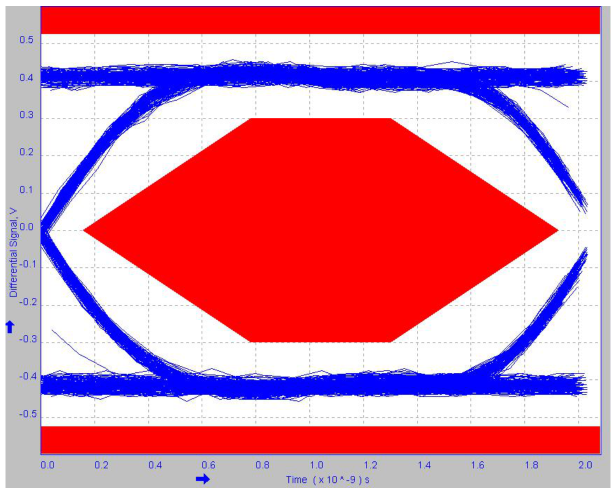


図 6-16. USB2.0 Eye Diagram (With TPD3S714-Q1)

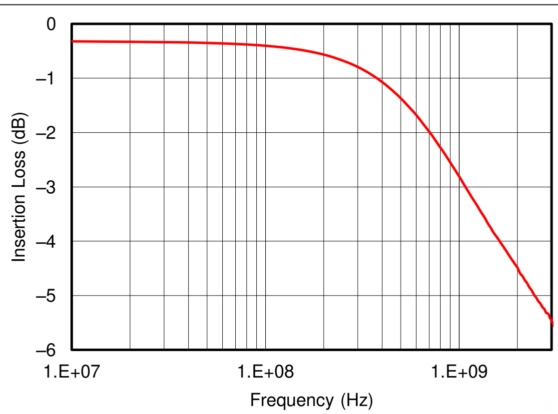


図 6-17. Data Switch Differential Bandwidth

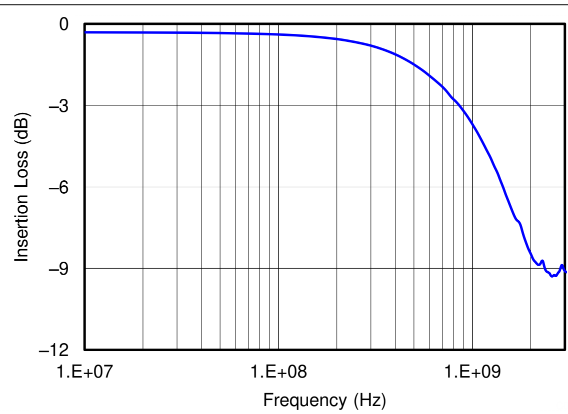


図 6-18. Data Switch Single-Ended Bandwidth

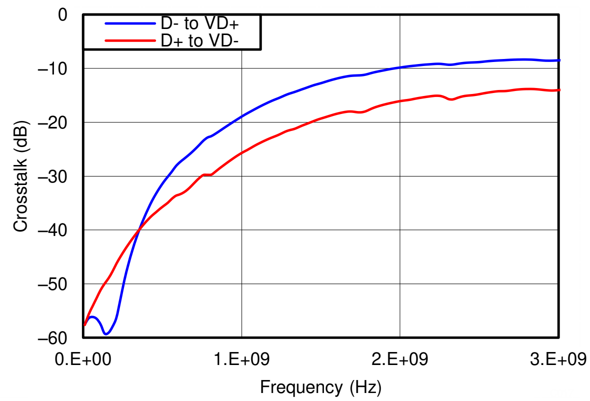


図 6-19. Data Switch Crosstalk

7 Parameter Measurement Information

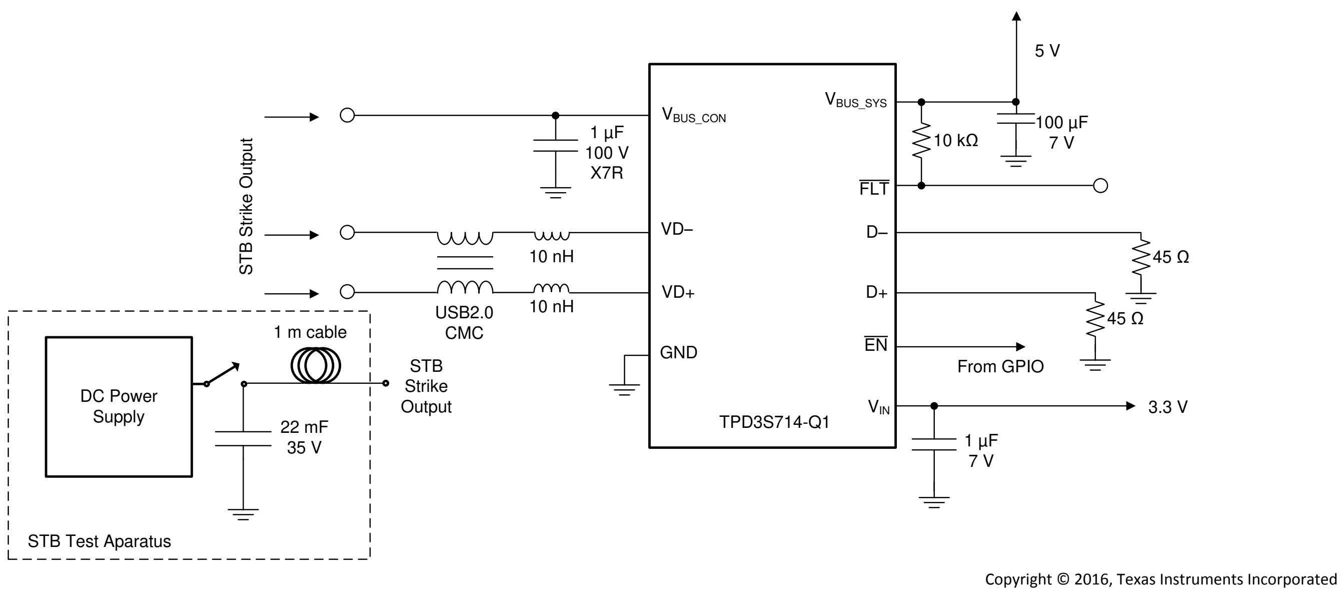


図 7-1. Short-to-Battery System Test Setup

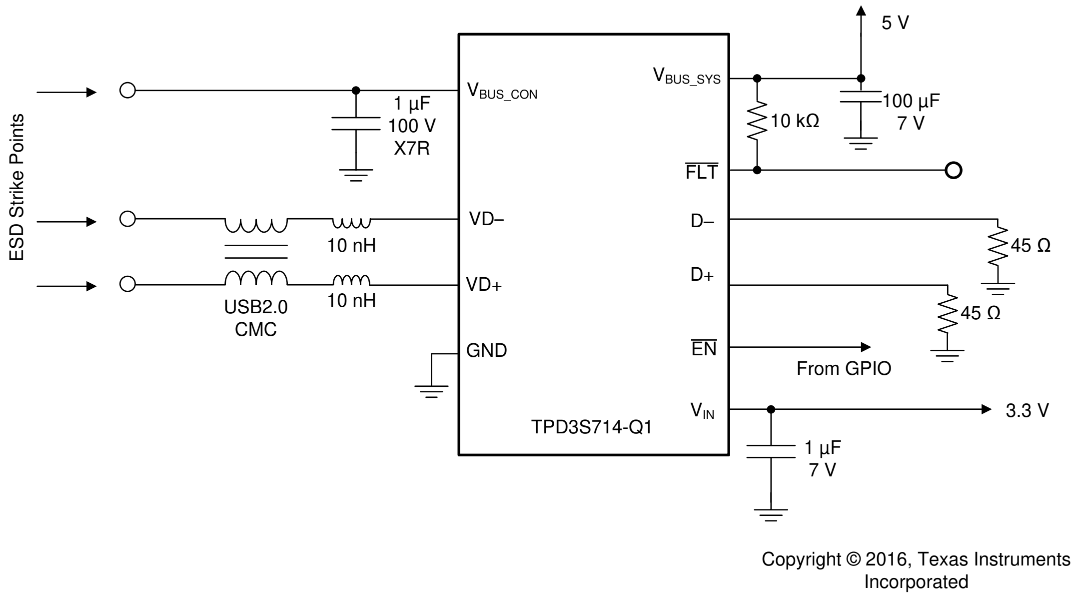


図 7-2. ESD System Test Setup

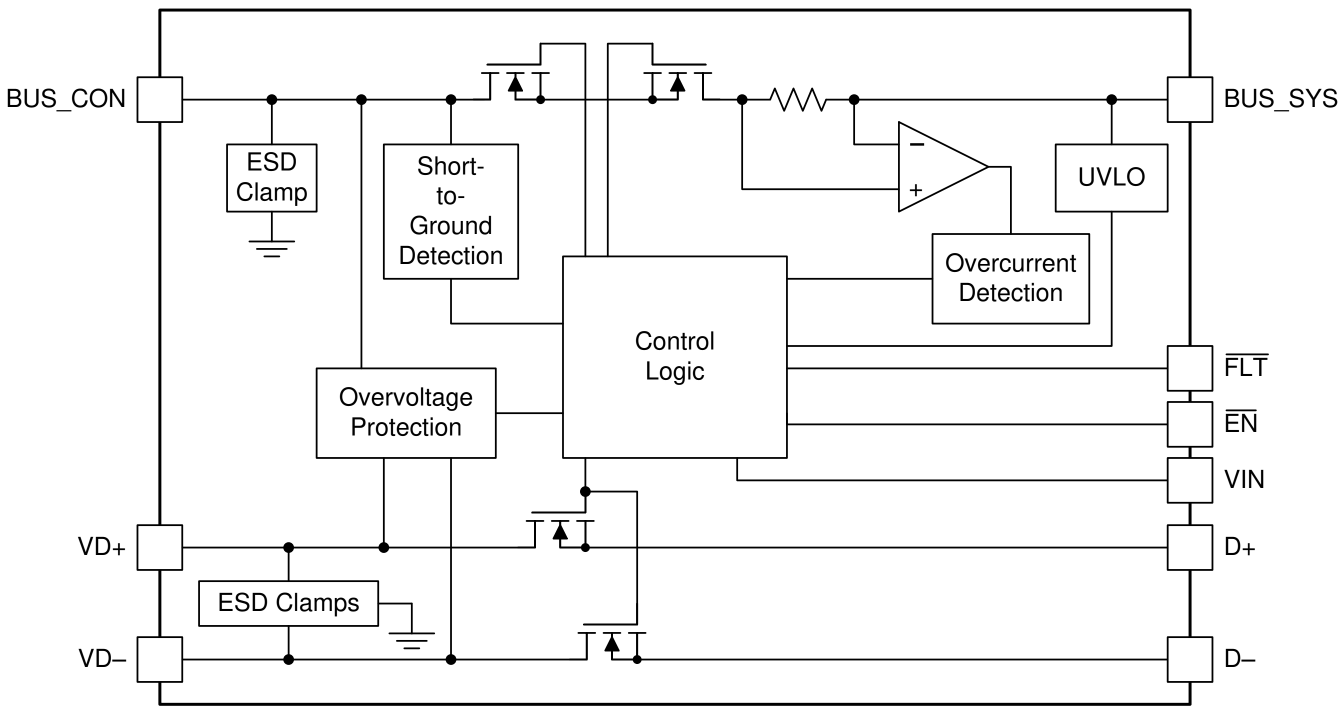
8 Detailed Description

8.1 Overview

The TPD3S714-Q1 provides a single-chip ESD protection and overvoltage protection solution for automotive USB interfaces. It offers short to battery protection up to 18 V and short to ground protection on V_{BUS_CON}. The TPD3S714-Q1 also provides a $\overline{FLT}$ pin that indicates to the system if a fault condition has occurred. The TPD3S714-Q1 offers ESD clamps on the V_{BUS_CON}, VD+, and VD– pins, thus eliminating the need for external TVS clamp circuits in the application.

The TPD3S714-Q1 has internal circuitry that controls the turnon of the internal nFET switches. An internal oscillator controls the timers that enable the switches and resets the open-drain $\overline{FLT}$ output. If V_{BUS_CON} is less than V_{OVP}, the switches are enabled. After an internal delay, the charge-pump starts-up, turns on the internal nFET switch through a soft start. Once the nFET is completely turned ON, TPD3S714-Q1 releases $\overline{FLT}$ pin to HIGH. At any time, if any of the external pins rise above V_{OVP}, $\overline{FLT}$ pin is pulled LOW. The nFET switches are turned OFF.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 AEC-Q100 Qualified

The TPD3S714-Q1 is an automotive qualified device according to the AEC-Q100 standards. This device is qualified to operate from –40 to +125°C ambient temperature.

8.3.2 Short-to-Battery and Short-to-Ground Protection on V_{BUS_CON}

The V_{BUS_CON} pin is protected against shorts to battery and shorts to ground.

Once a voltage on V_{BUS_CON} is detected as too low (below the V_{SHRT} threshold) after the device is enabled, the device enters short-circuit protection mode and assert $\overline{FLT}$. It sources the I_{SHRT} current until it detects the voltage rising above the V_{SHRT} threshold, where it resumes standard operating mode and deassert $\overline{FLT}$.

Once a voltage above the V_{OVP} threshold is detected by the device, it shuts off all FETs and asserts a fault on the $\overline{FLT}$ pin. Once the excessive voltage is removed, the device automatically re-enables and $\overline{FLT}$ deasserts (see the *Timing Requirements* table for more details).

8.3.3 Short-to-Battery and Short-to-V_{BUS} Protection on VD+, VD–

The VD+ and VD– pins are protected against shorts to battery and shorts to bus. The OVP threshold on the VD+ and VD– pins is low enough that it protects against shorts to V_{BUS}.

Once a voltage above the V_{OVP} threshold is detected by the device, it shuts off all FETs and asserts a fault on the $\overline{FLT}$ pin. Once the excessive voltage is removed, the device automatically re-enables and $\overline{FLT}$ deasserts.

8.3.4 ESD Protection on V_{BUS_CON}, VD+, VD–

The protected pins (V_{BUS_CON}, VD+, VD–) are tested to pass the IEC 61000-4-2 ESD standard up to Level 4 ESD protection. Additionally, these pins are tested against ISO 10605 with the 330-pF, 330-Ω equivalent network. This guarantees passing of at least ±8-kV contact discharge and ±15-kV air gap discharge according to both standards using test setup shown in 図 7-2.

8.3.5 Low R_{ON} nFET V_{BUS} Switch

The V_{BUS} switch has a low R_{ON} that provides minimal voltage droop from system to connector. Typical resistance is 63 mΩ and is specified for 150 mΩ at 125°C ambient temperature.

8.3.6 High Speed Data Switches

The D+ and D– switches have a very low capacitance and a high bandwidth (1-GHz typical), allowing for a clean USB 2.0 eye diagram.

8.3.7 Hiccup Current Limit

The V_{BUS} path of this device has an integrated overcurrent protection circuit. Above the overcurrent threshold (550-mA minimum), the device goes into a fault state where it limits current to the threshold. After a short blanking time, the device cycles on and off to try to check if the connected device is still in overcurrent.

8.3.8 Fast Overvoltage Response Time

The overvoltage FETs are designed to have a fast turnoff time to protect the upstream SoC as quickly as possible. Typical response time for complete turnoff is 2 µs for the V_{BUS} path and 200 ns for the data path.

8.3.9 Integrated Input Enable

The TPD3S714-Q1 has an enable input to turn on and off the device. The $\overline{EN}$ pin disables and enables the V_{BUS} and data paths.

8.3.10 Fault Output Signal

The TPD3S714-Q1 has a fault pin, $\overline{FLT}$ that indicates when there is any sort of fault condition because of OVP, OCP, or short-circuit.

8.3.11 Thermal Shutdown Feature

In the event that the device exceeds the maximum allowable junction temperature, it shuts down the device to prevent damage to itself and indicate via the fault pin.

8.3.12 16-pin SSOP Package

This device is packaged in a standard 16-pin SSOP leaded package.

8.4 Device Functional Modes

8.4.1 Normal Operation

The TPD3S714-Q1 operates normally (all FETs on) when enabled, both V_{BUS_SYS} and V_{IN} are above their UVLO thresholds, and the device is not in any fault conditions.

8.4.2 Overvoltage Condition

When the VD+, VD–, or V_{BUS_CON} pins exceed their OVP threshold, the device enters the overvoltage state. All FETs are disabled and the $\overline{\text{FLT}}$ pin is asserted. Once the protected pins drop below their OVP threshold, the device automatically turns back on.

8.4.3 Overcurrent Condition

When the current through the V_{BUS} path exceeds the I_{LIM} current threshold, the device enters into the overcurrent state. The TPD3S714-Q1 limits current to the I_{LIM} threshold by dropping voltage across the V_{BUS} FET to maintain constant current. Once it continues to sense an overcurrent condition for the blanking time t_{BLANK}, the device disables itself for the retry time, t_{RETRY} and then retry automatically for the retry time, t_{BLANK_RETRY}. In the event that the current is below the overcurrent threshold, the device deasserts fault and resumes normal operation.

8.4.4 Short-Circuit Condition

When the voltage on the V_{BUS_CON} side drops below the V_{SHRT} threshold while enabled, the TPD3S714-Q1 enters the short-circuit mode. It sources a constant current of I_{SHRT} until it rises above the V_{SHRT} threshold. Once that occurs, the device automatically re-enters normal operation and deasserts fault.

8.4.5 Device Logic Tables

表 8-1 shows the TPD3S714-Q1 V_{BUS} Logic Table.

表 8-1. TPD3S714-Q1 V_{BUS} Logic Table

VOLTAGE CONDITION			CURRENT CONDITION		
V_{BUS_CON}	V_{BUS_SYS}	$\overline{\text{EN}}$	CURRENT FLOW	COMMENT	$\overline{\text{FLT}}$ PIN
X	<UVLO	X	No Flow	Switch off because of UVLO	High-Z
<OVP and >V_{SHRT}	>UVLO	Low	V_{BUS_SYS} to V_{BUS_CON}	Current flows through the switch, normal host mode	High-Z
X	>UVLO	High	No Flow	Switch off	Low
<V_{SHRT}	>UVLO	Low	V_{BUS_SYS} to V_{BUS_CON}	Current flow through switch, device detects short circuit, current limited to I_{SHRT}	Low
X	X	Low	>OCP	Device switches off because of overcurrent limit, auto-retrys until <OCP or thermal shutdown conditions occur	Low
>OVP	>UVLO	Low	No Flow	Switch off because of OVP	Low
X	X	X	No Flow	Thermal Shutdown Condition	Low

表 8-2 shows the TPD3S714-Q1 Data Line Logic Table

表 8-2. TPD3S714-Q1 Data Line Logic Table

VOLTAGE CONDITION		CURRENT CONDITION		
VD+/VD–	$\overline{\text{EN}}$	SWITCHES ON?	COMMENT	$\overline{\text{FLT}}$ PIN
<OVP	Low	Yes	Device operates normally, data transfer can occur	High-Z
X	High	No	Switches off	Low
>OVP	Low	No	Switches off because of OVP limit	Low
X	X	No	Thermal Shutdown Condition	Low

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPD3S714-Q1 offers fully featured automotive USB2.0 protection including short-to-battery, overcurrent, and ESD protection. Care must be taken during the implementation to make sure the device provides adequate protection to the system.

9.2 Typical Application

図 9-1 shows a fully featured USB2.0 high speed port, with an 18-V short-to-battery requirement on the connector side.

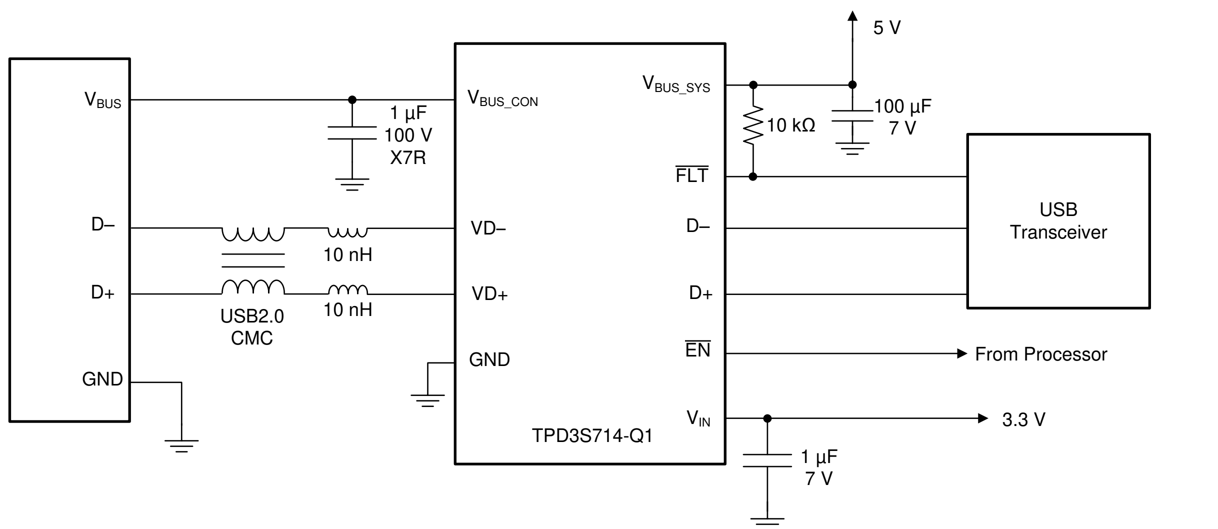


図 9-1. Typical Application Configuration for TPD3S714-Q1

9.2.1 Design Requirements

For this design example, the input parameters shown in 表 9-1 are used:

表 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Short-to-battery tolerance on VD+, VD–, V_{BUS_CON}	18 V
Maximum current in normal operation on V_{BUS}	500 mA
USB data rate	480 Mbps

9.2.2 Detailed Design Procedure

To begin the design process, the designer must know the following parameters:

- Short-to-Battery tolerance on connector pins
- Maximum current in normal operation on V_{BUS}
- USB Data Rate

9.2.2.1 Short-to-Battery Tolerance

The TPD3S714-Q1 is capable of handling up to 18-V DC on the VD+, VD–, and V_{BUS_CON} pins. In the event of a short-to-battery on V_{BUS_CON}, significant ringing is expected because of the hot plug-like nature of the short-to-battery event. In typical ceramic capacitor configurations, a standard RLC response is expected which results in a ringing of nearly two times the applied DC voltage. The TPD3S714-Q1 is capable of withstanding the transient ringing from hot plug-like events, assuming some precautions are taken.

Careful capacitor selection on the V_{BUS_CON} pin must be observed. A capacitor with a low derating percentage under the applied voltages must be used to prevent excess ringing. In the example, a 1-µF 100-V tolerant ceramic X7R capacitor is used. It is best practice to carefully select the capacitors used in this circuit to prevent derating-based voltage spikes under hot plug events. See the application example graphs, 図 9-4 and 図 9-5 to compare ringing of a 100-V capacitor to a 50-V capacitor. 図 9-6 shows the 100-V capacitor with the TPD3S714-Q1 installed.

Another alternative to a high rated ceramic capacitor is to implement either a standard R-C snubber circuit, or a small external TVS diode. Depending on the short-to-battery tolerance needed, no special precautions may be needed.

For more information on this topic, see the white paper *Designing USB for short-to-battery tolerance in automotive environments*.

9.2.2.2 Maximum Current on V_{BUS}

The TPD3S714-Q1 is capable of operating up to 5500 mA of current (minimum) until going into current limit mode. In this example, the maximum current for USB2.0 of 500 mA has been chosen.

9.2.2.3 USB Data Rate

The TPD3S714-Q1 is capable of operating at the maximum USB2.0 High Speed data rate of 480 Mbps because of the high data switch bandwidth of 1 GHz (typical). In this design example the maximum data rate of 480 Mbps has been chosen.

9.2.3 Application Curves

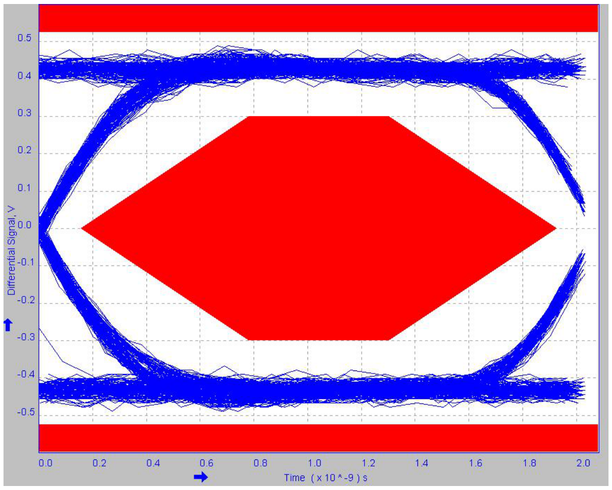


図 9-2. USB2.0 Eye Diagram (Board Only, Through Path)

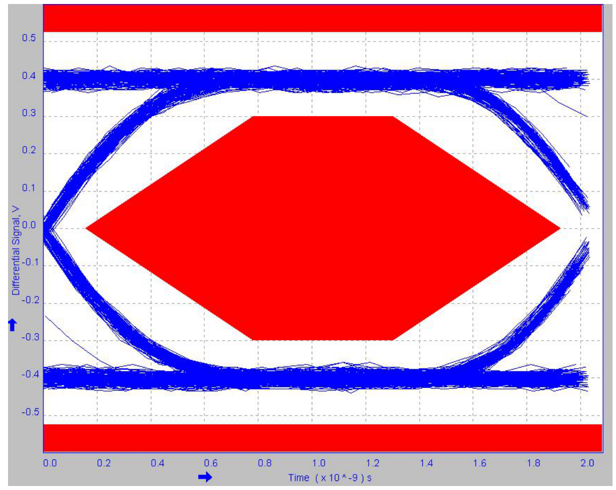


図 9-3. USB2.0 Eye Diagram (System from Typical Application Schematic)

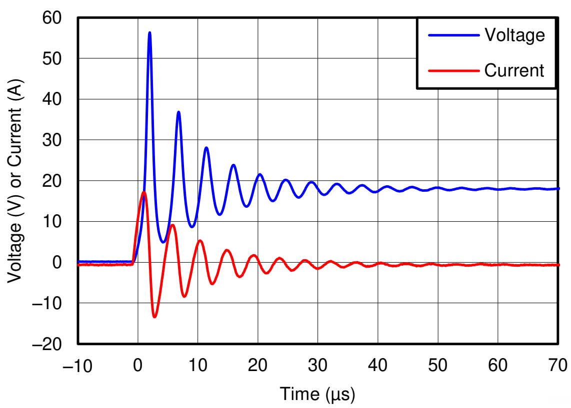


図 9-4. 50-V, 1-µF X7R Ceramic Shorted to 18-V (Not Recommended)

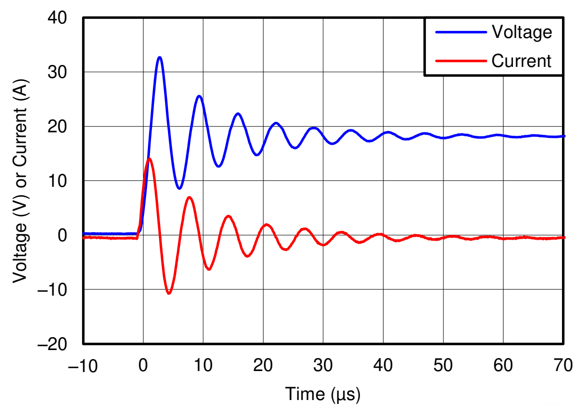


図 9-5. 100-V, 1-µF X7R Ceramic Shorted to 18 V

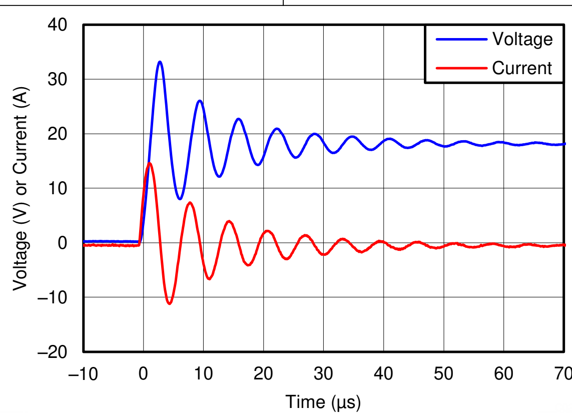


図 9-6. TPD3S714-Q1 and 100-V, 1-µF X7R Shorted to 18 V (Powered Off)

10 Power Supply Recommendations

10.1 V_{BUS} Path

The V_{BUS_SYS} pins provide power to the chip and supply current through the load switch to V_{BUS_CON}. A 100-µF bulk capacitor is recommended on V_{BUS_SYS} to supply the USB port and maintain compliance. A 1-µF capacitor is recommended on the V_{BUS_CON} pin with adequate voltage rating to tolerate short-to-battery conditions. A supply voltage above the UVLO threshold for V_{BUS_SYS} must be supplied for the device to power on.

10.2 V_{IN} Pin

The V_{IN} pin provides a voltage reference for the data switch OVP level as well as a bypass for ESD clamping. A 1-µF capacitor must be placed as close to the pin as possible and the supply must be set to be above the UVLO threshold for V_{IN}.

11 Layout

11.1 Layout Guidelines

Proper routing and placement maintains signal integrity for high-speed signals. The following guidelines apply to the TPD3S714-Q1:

- Place the bypass capacitors as close as possible to the V_{IN}, V_{BUS_SYS}, and V_{BUS_CON} pins. Capacitors must be attached to a solid ground. This minimizes voltage disturbances during transient events such as short-to-battery, ESD, or overcurrent conditions.
- High speed traces (data switch path) must be routed as straight as possible and any sharp bends must be minimized.

Our standard ESD recommendations apply to the VD+, VD–, and V_{BUS_CON} pins as well:

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

11.2 Layout Example

図 11-1 shows a full layout for a standard USB2.0 port. A common mode choke and inductors are used on the high speed data lines, and the requisite bypassing caps are placed on V_{BUS_CON}, V_{BUS_SYS}, and V_{IN}.

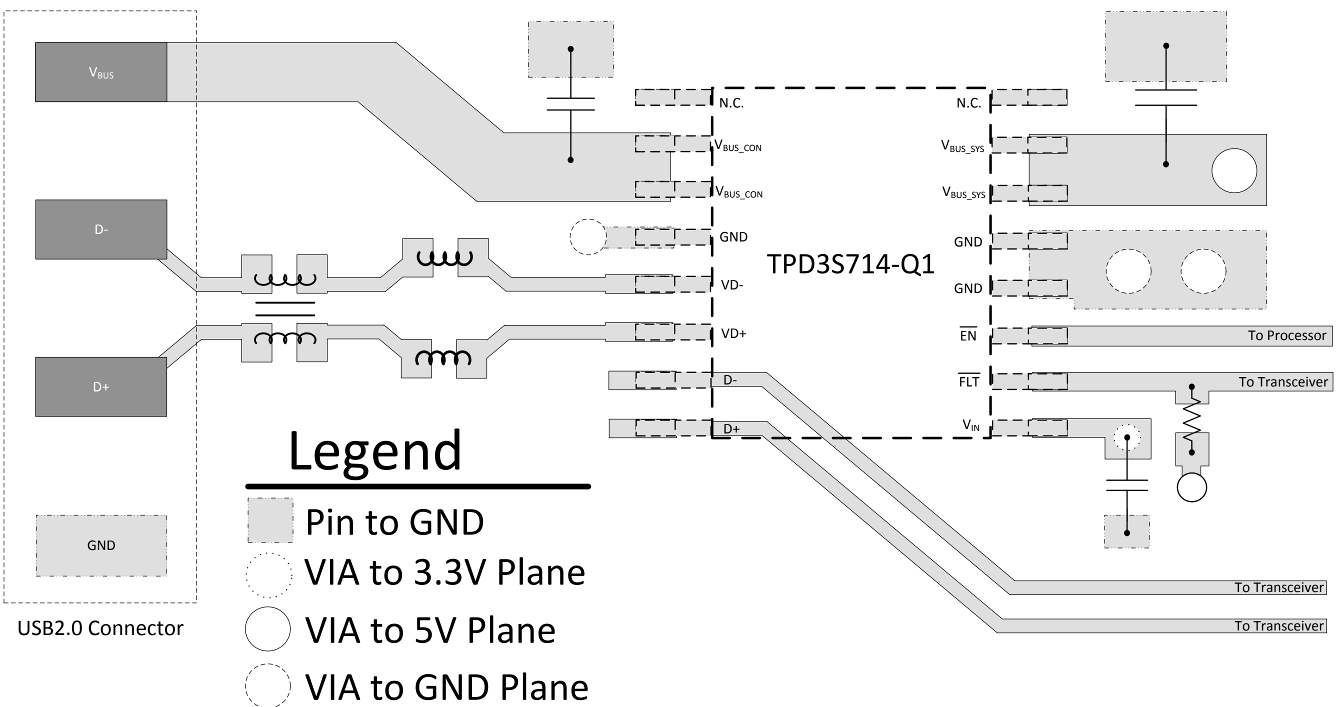


図 11-1. Typical Layout Example for TPD3S714-Q1

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *TPD3S714-Q1EVM User's Guide*
- *Reading and Understanding an ESD Protection Datasheet*
- *ESD Layout Guide*

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

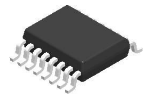
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

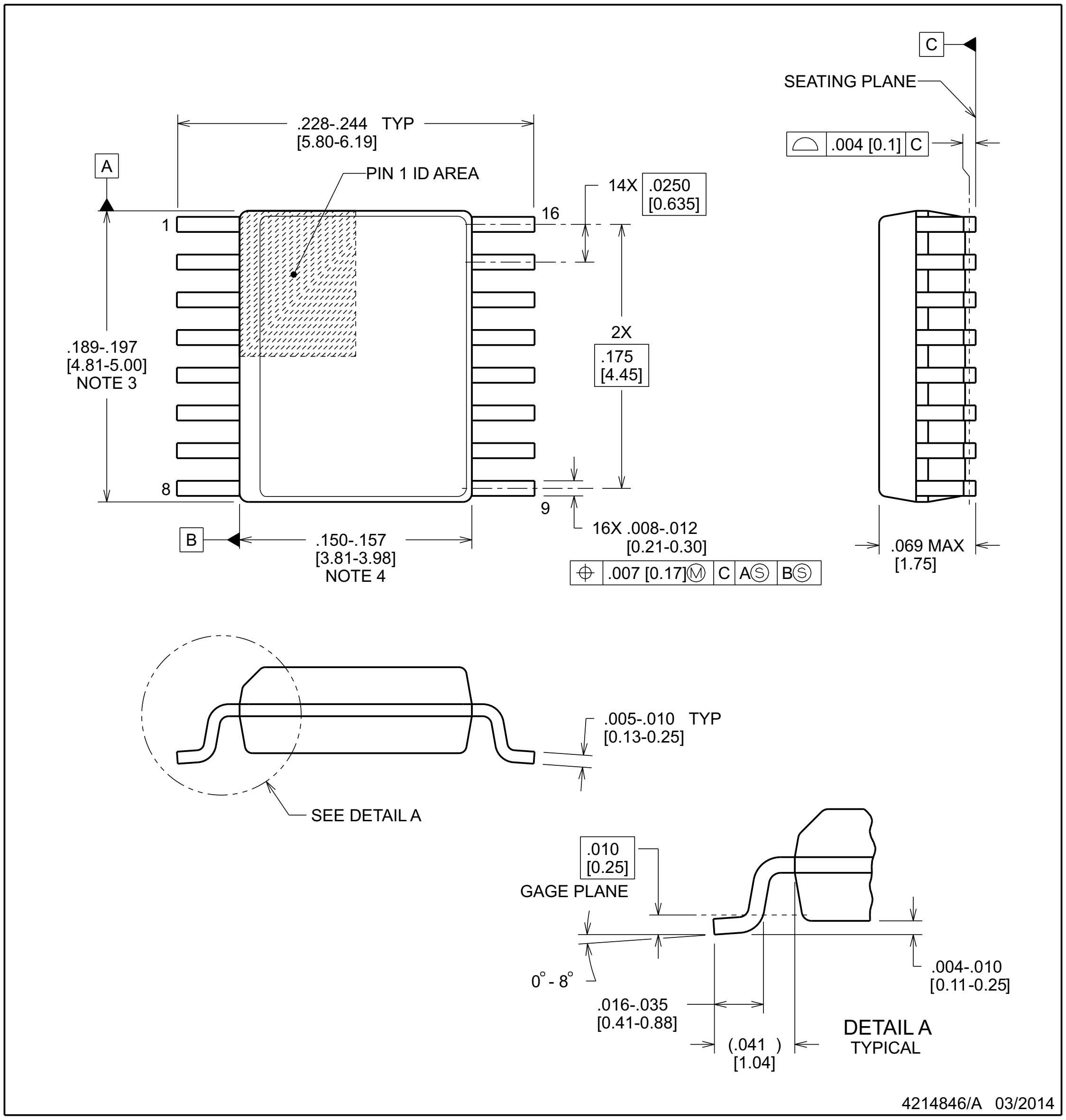


PACKAGE OUTLINE

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.

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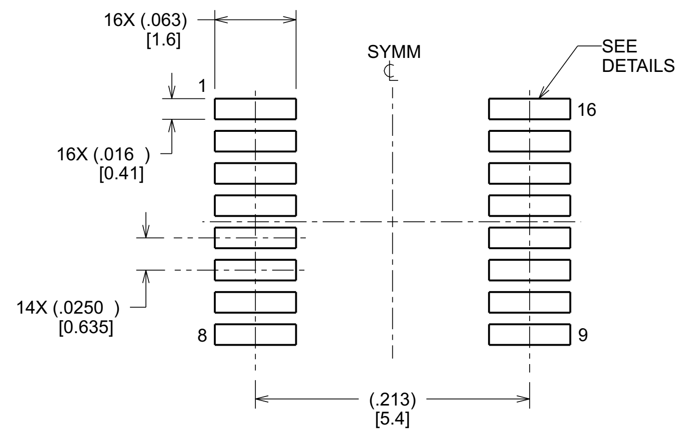
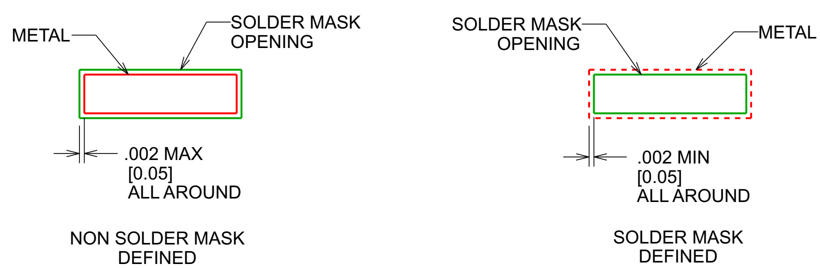
EXAMPLE BOARD LAYOUT

DBQ0016A SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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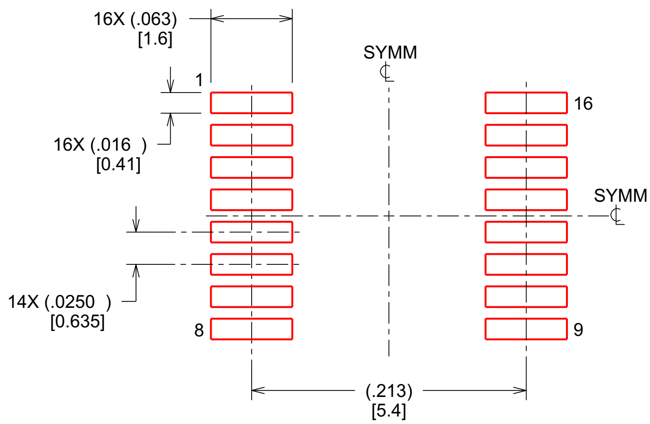
EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPD3S714QDBQRQ1	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	RJ714Q
TPD3S714QDBQRQ1.A	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	RJ714Q
TPD3S714QDBQRQ1.B	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	RJ714Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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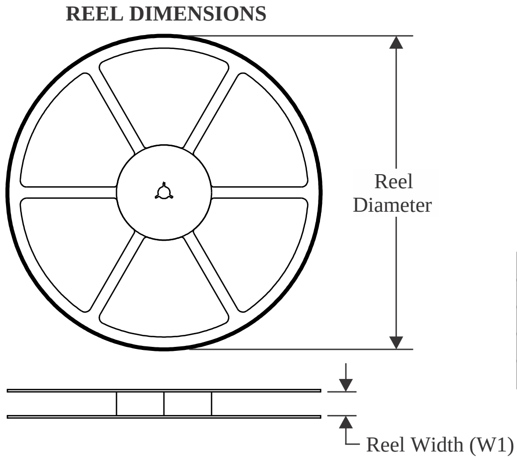
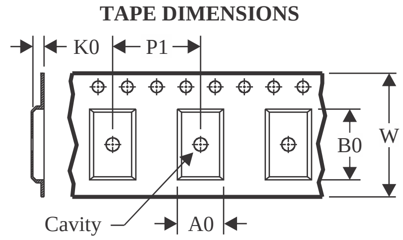
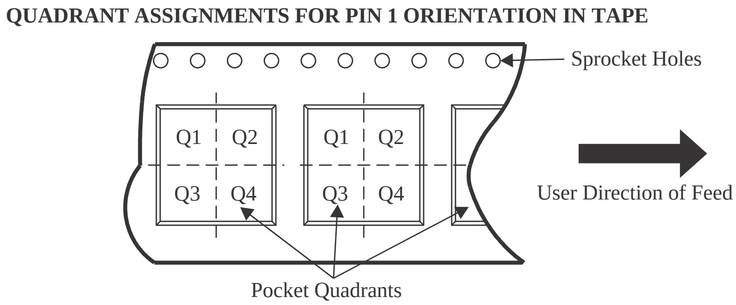
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION





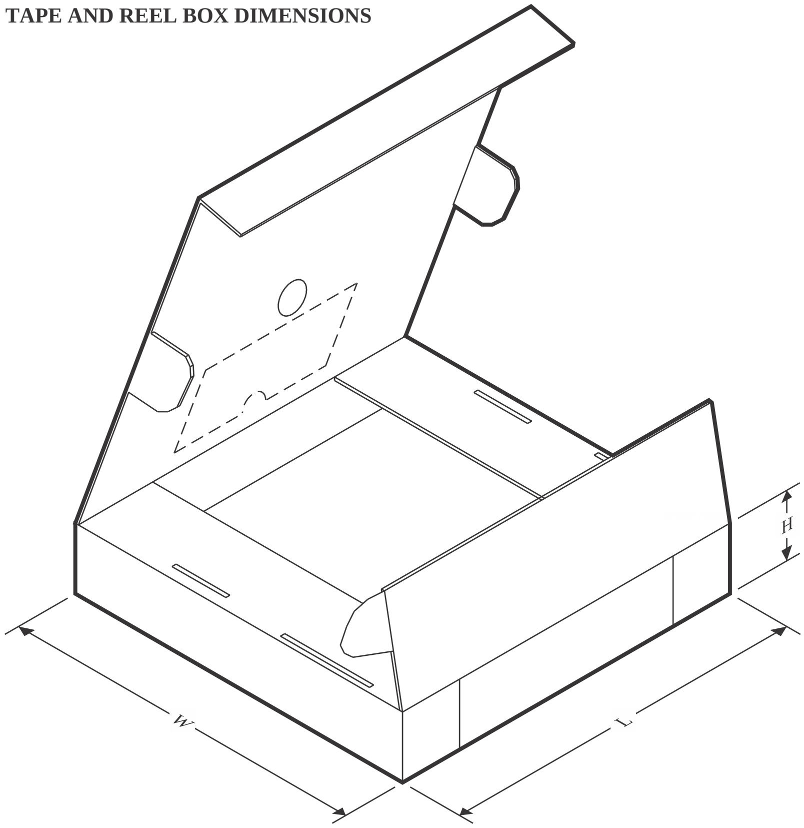
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

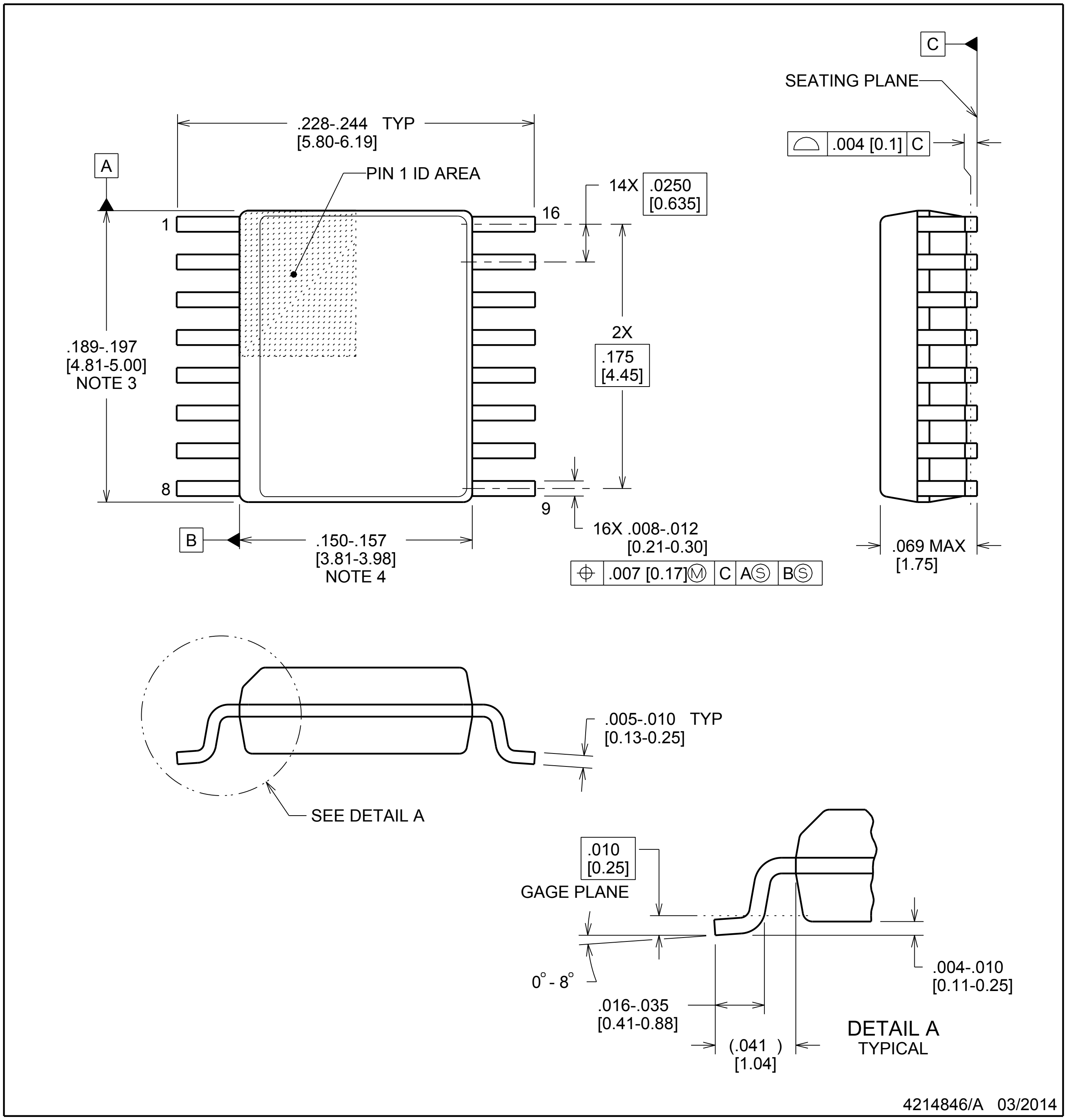
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD3S714QDBQRQ1	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



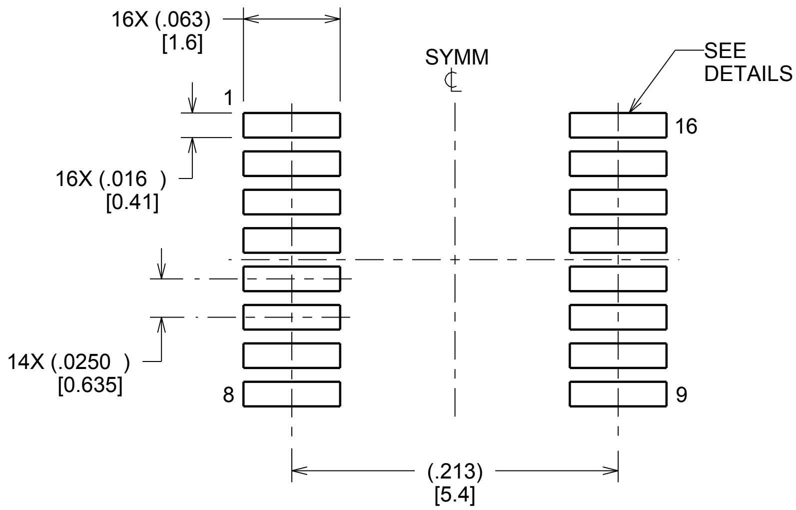
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD3S714QDBQRQ1	SSOP	DBQ	16	2500	353.0	353.0	32.0

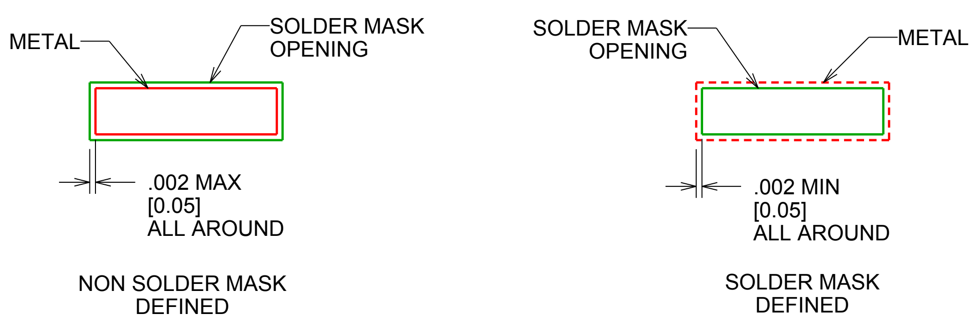


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

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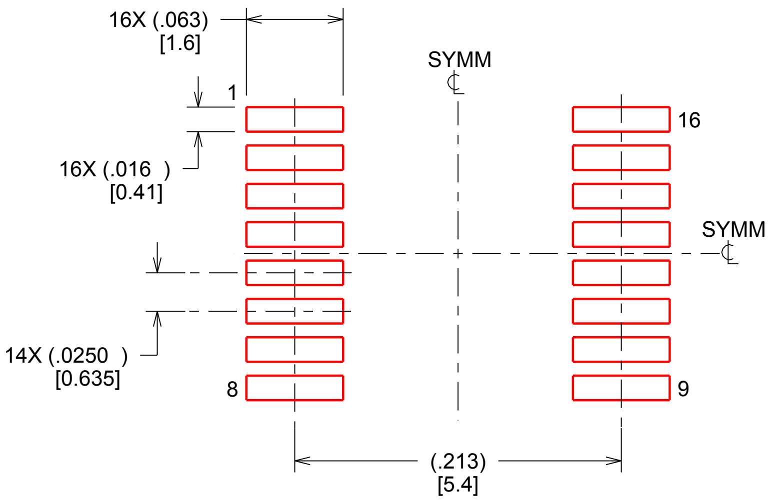
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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