



TPD2S300 USB Type-C VBUS短絡/IEC ESDプロテクタ、CCピン用

1 特長

- 2チャンネルの V_{BUS} への短絡過電圧保護(CC1、CC2): 24V_{DC}許容
- 2チャンネルのIEC 61000-4-2 ESD保護(CC1、CC2)
- 低い静止電流: 3.23 μ A (標準値) (V_{PWR} 、 $V_M = 3.3V$)
- CC1、CC2過電圧保護FET: V_{CONN} 電力用に200mAを供給可能
- CCデッド・バッテリー抵抗の内蔵により、モバイル・デバイスでのデッド・バッテリー状況に対応
- 1.4mm×1.4mmのWCSPパッケージ

2 アプリケーション

- スマートフォン
- ラップトップPC
- タブレット
- 壁面アダプタ
- 外付けバッテリー
- 電動ドリル

3 概要

TPD2S300はシングル・チップのUSB Type-Cポート保護ソリューションで、CC1およびCC2ピンについて、20Vの V_{BUS} への短絡過電圧およびIEC ESD保護を行います。

USB Type-Cコネクタのリリース以降、USB Type-C用でありながら、USB Type-Cの仕様を満たしていない多くの製品やアクセサリがリリースされました。このような例の1つは、USB Type-C電力供給アダプタで、 V_{BUS} ラインが20Vで起動されるものです。USB Type-Cに関する別の懸念として、小さなコネクタのピンが互いに近接して配置されているため、コネクタの機械的なねじれや水平方向のずれによってピン間が短絡することがあります。これによって、20V V_{BUS} がCCピンと短絡するおそれがあります。また、Type-Cコネクタのピンが互いに近接して配置されていることから、破片や湿気により20V V_{BUS} ピンがCCピンと短絡するリスクも高まっています。

これらの理想的でない機器や機械的事象が存在するため、CCピンは5V以下の電圧でのみ動作するにもかかわらず、20V許容にする必要があります。TPD2S300はCCピンの過電圧保護を行うため、通常の動作に影響することなくCCピンを20V許容にできます。このデバイスは、CCラインと直列に高電圧FETを配置します。OVPスレッシュホルドを超える電圧がこれらのラインに検出された場合、高電圧スイッチが開き、システムの他の部分を、コネクタに存在している高電圧の状況から絶縁します。

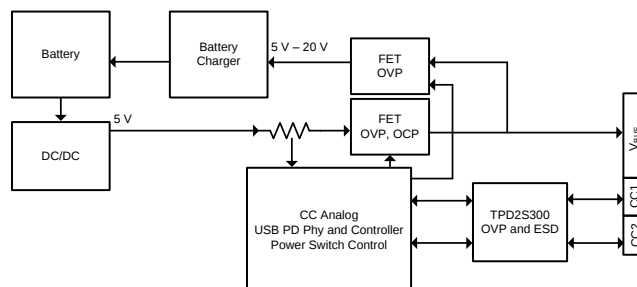
最後に、ほとんどのシステムでは外部ピンについてIEC 61000-4-2システム・レベルのESD保護が必要です。TPD2S300には、CC1およびCC2ピンのIEC 61000-4-2 ESD保護が内蔵されているため、コネクタの外部に高電圧TVSダイオードを配置する必要がありません。

製品情報⁽¹⁾

型番	パッケージ	本体サイズ(公称)
TPD2S300	WCSP (9)	1.40mm×1.40mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

アプリケーション図



Copyright © 2017, Texas Instruments Incorporated



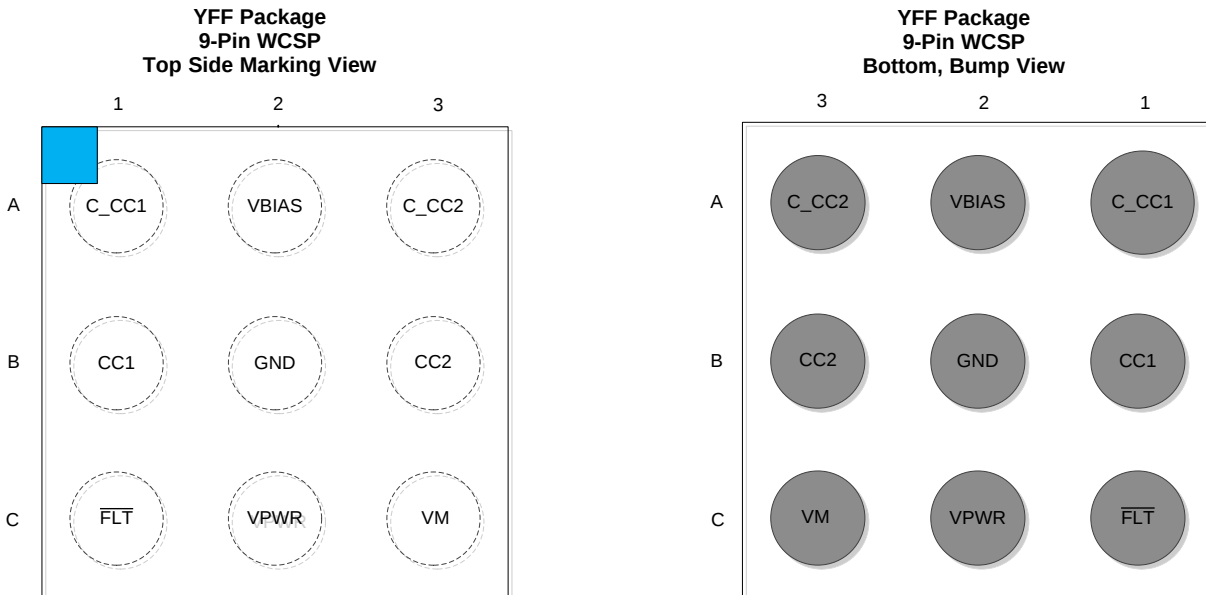
目次

1	特長	1	7.3	Feature Description	13
2	アプリケーション	1	7.4	Device Functional Modes	14
3	概要	1	8	Application and Implementation	15
4	改訂履歴	2	8.1	Application Information	15
5	Pin Configuration and Functions	3	8.2	Typical Application	15
6	Specifications	4	9	Power Supply Recommendations	27
6.1	Absolute Maximum Ratings	4	10	Layout	28
6.2	ESD Ratings—JEDEC Specification	4	10.1	Layout Guidelines	28
6.3	ESD Ratings—IEC Specification	4	10.2	Layout Example	28
6.4	Recommended Operating Conditions	4	11	デバイスおよびドキュメントのサポート	29
6.5	Thermal Information	5	11.1	ドキュメントのサポート	29
6.6	Electrical Characteristics	5	11.2	ドキュメントの更新通知を受け取る方法	29
6.7	Timing Requirements	7	11.3	コミュニティ・リソース	29
6.8	Typical Characteristics	8	11.4	商標	29
7	Detailed Description	12	11.5	静電気放電に関する注意事項	29
7.1	Overview	12	11.6	Glossary	29
7.2	Functional Block Diagram	12	12	メカニカル、パッケージ、および注文情報	30

4 改訂履歴

日付	改訂内容	注
2017年4月	*	初版

5 Pin Configuration and Functions



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
A1	C_CC1	I/O	Connector side of the CC1 OVP FET. Connect to either CC pin of the USB Type-C connector
A2	VBIAS	Power	Pin for ESD support capacitor. Place a 0.1-μF capacitor on this pin to ground
A3	C_CC2	I/O	Connector side of the CC2 OVP FET. Connect to either CC pin of the USB Type-C connector
B1	CC1	I/O	System side of the CC1 OVP FET. Connect to either CC pin of the CC/PD controller
B2	GND	GND	Ground
B3	CC2	I/O	System side of the CC2 OVP FET. Connect to either CC pin of the CC/PD controller
C1	FLT	O	Open drain for fault reporting
C2	VPWR	Power	2.7 V–4.5 V power supply
C3	VM	I	Voltage mode pin. Place 2.7 V–4.5 V on pin to operate for CC, PD, and FRS. Place 8.7 V–22 V on pin to operate the device in low resistance mode as well

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V_I	Input voltage	V_{PWR}	–0.3	5.5	V
		V_M	–0.3	28	V
V_O	Output voltage	$\overline{FLT}$	–0.3	6	V
		V_{BIAS}	–0.3	24	V
V_{IO}	I/O voltage	CC1, CC2	–0.3	6	V
		C_CC1, C_CC2	–0.3	24	V
T_A	Operating free air temperature		–40	85	°C
T_J	Operating junction temperature		–40	105	°C
T_{stg}	Storage temperature		–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings—JEDEC Specification

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2000 V may actually have higher performance.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±500 V may actually have higher performance.

6.3 ESD Ratings—IEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2, C_CC1, C_CC2	Contact discharge	±8000
			Air-gap discharge	±15000

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_I	Input voltage	V_{PWR}	2.7	3.3	4.5	V
		V_M	2.7		22	V
V_O	Output voltage	$\overline{FLT}$ Pull-up resistor power rail	2.7		5.5	V
V_{IO}	I/O voltage	CC1, CC2, C_CC1, C_CC2	0		5.5	V
I_{VCONN}	V_{CONN} current	Current flowing from CCx to C_CCx			200	mA
External components ⁽¹⁾		$\overline{FLT}$ Pull-up resistance	1.7		300	k Ω
		V_{BIAS} capacitance ⁽²⁾		0.1		μ F
		V_{PWR} capacitance, V_M capacitance	0.3	1		μ F

- (1) For recommended values for capacitors and resistors, the typical values assume a component placed on the board near the pin. Minimum and maximum values listed are inclusive of manufacturing tolerances, voltage derating, board capacitance, and temperature variation. The effective value presented must be within the minimum and maximums listed in the table.
- (2) The V_{BIAS} pin requires a minimum 35- V_{DC} rated capacitor. A 50- V_{DC} rated capacitor is recommended to reduce capacitance derating. See the [VBIAS Capacitor Selection](#) section for more details on V_{BIAS} capacitor selection.

6.5 Thermal Information

THERMAL METRIC ⁽¹⁾		TPD2S300	UNIT
		YFF (WCSP)	
		9 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	107.5	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	0.9	°C/W
R _{θJB}	Junction-to-board thermal resistance	28.1	°C/W
ψ _{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ _{JB}	Junction-to-board characterization parameter	28.2	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CC OVP SWITCHES					
R _{ON_VCONN_1}	On resistance of CC OVP FETs VCONN operation VM = 8.7 V, CCx = 3 V, I _{CCx} = 0.6 A, –40°C ≤ T _J ≤ 105°C			0.560	Ω
R _{ON_VCONN_2}	On resistance of CC OVP FETs VCONN operation VM = 8.7 V, CCx = 4.87 V, I _{CCx} = 0.2 A, –40°C ≤ T _J ≤ 105°C			0.608	Ω
R _{ON_FRS}	On resistance of CC OVP FETs fast role swap operation VM = 2.7 V, CCx = 0.49 V, I _{CCx} = 30 mA, –40°C ≤ T _J ≤ 105°C			1.3	Ω
R _{ON_CC_ANA}	On resistance of CC OVP FETs CC analog operation VM = 2.7 V, CCx = 2.45 V, I _{CCx} = 400 μA, –40°C ≤ T _J ≤ 105°C			18.7	Ω
R _{ON_PD}	On resistance of CC OVP FETs CC USB-PD operation VM = 2.7 V, CCx = 1.2 V, I _{CCx} = 250 μA, –20°C ≤ T _J ≤ 105°C			13	Ω
R _{ONFLAT_VC ONN_1}	On resistance flatness of CC OVP FETs VCONN operation VM = 8.7 V, sweep CCx from 0 V to 5.5 V, measure the difference in resistance. I _{CCx} = 0.2 A, –40°C ≤ T _J ≤ 105°C			0.2	Ω
C _{ON_CC}	Equivalent on capacitance for CC pins Capacitance from C _{CCx} or CCx to GND when device is powered. V _{C_{CCx}/V_{CCx}} = 0 V to 1.2 V, f = 400 kHz, –40°C ≤ T _J ≤ 105°C	30		120	pF
V _{TH_DB}	Threshold voltage of the pull-down FET in series with RD during dead battery I _{C_{CCx}} = 80 μA	0.5	0.9	1.2	V
R _D	Dead battery pull-down resistance (only present when device is unpowered). Effective resistance of R _D and FET in series V _{PWR} = 0 V, V _{C_{CCx}} = 2.6 V	4.1	5.1	6.1	kΩ
V _{OVPCC_RISE}	Rising overvoltage protection threshold on C _{CCx} pins Place 5.5 V on C _{CCx} pins. Step up voltage until the FLT pin is asserted. –20°C ≤ T _J ≤ 105°C	5.55		6.18	V
V _{OVPCC_HYS}	OVP threshold hysteresis Place 6.5 V on C _{CCx} . Step down the voltage on C _{CCx} until the FLT pin is deasserted. Measure the difference between rising and falling OVP thresholds		50		mV
BW _{ON}	On bandwidth single ended (–3dB) Measure the –3-dB bandwidth from C _{CCx} to CCx. Single ended measurement, 50-Ω system. V _{cm} = 0 V to 1.2 V		80		MHz
V _{STBUS_CC}	Short-to-VBUS tolerance on the C _{CCx} pins Hot-Plug C _{CCx} with a 1 meter USB Type C Cable. Place a 30-Ω load on CCx			24	V

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{STBUS_CC_CLAMP} Short-to-VBUS system-side clamping voltage on the CCx pins	Hot-Plug C _{CCx} with a 1-meter USB Type C Cable. Hot-plug voltage C _{CCx} = 2.4 V. VPWR = 3.3 V. Place a 30-Ω load on CCx		8		V
POWER SUPPLY AND LEAKAGE CURRENTS					
V _{PWR_UVLO} V _{PWR} undervoltage lockout threshold	Place 1 V on VPWR and raise the voltage until the CC FETs turn ON	1.9	2.3	2.55	V
V _{PWR_UVLO_HYS} V _{PWR} UVLO hysteresis	Place 3 V on VPWR and lower the voltage until the CC FETs turn off. Calculate the difference between the rising and falling UVLO threshold	50	100	200	mV
I _{VPWR_1S} VPWR quiescent current for 1S battery	VPWR = 3.3 V, VM = 3.3 V, C _{CCx} = 3.6 V, -40°C ≤ T _J ≤ 105°C		3.23	7	μA
I _{VM_1S} VM quiescent current for 1S battery	VPWR = 3.3 V, VM = 3.3 V, C _{CCx} = 3.6 V, -40°C ≤ T _J ≤ 105°C			1	μA
I _{VPWR_1S_Max} VPWR quiescent current for 1S battery max	VPWR = 4.5 V, VM = 4.5 V, C _{CCx} = 3.6 V, -40°C ≤ T _J ≤ 105°C			12	μA
I _{VM_1S_Max} VM quiescent current for 1S battery max	VPWR = 4.5 V, VM = 4.5 V, C _{CCx} = 3.6 V, -40°C ≤ T _J ≤ 105°C			1	μA
I _{VPWR_3S} VPWR quiescent current for 3S battery	VPWR = 3.6 V, VM = 13.5 V, C _{CCx} = 3.6 V, -40°C ≤ T _J ≤ 105°C			8	μA
I _{VM_3S} VM quiescent current for 3S battery	VPWR = 3.6 V, VM = 13.5 V, C _{CCx} = 3.6 V, -40°C ≤ T _J ≤ 105°C			3.5	μA
I _{VPWR_4S} VPWR quiescent current for 4S battery	VPWR = 3.6 V, VM = 18 V, C _{CCx} = 3.6 V, -40°C ≤ T _J ≤ 105°C			8	μA
I _{VM_4S} VM quiescent current for 4S battery	VPWR = 3.6 V, VM = 18 V, C _{CCx} = 3.6 V, -40°C ≤ T _J ≤ 105°C			4.5	μA
I _{CC_LEAK} Leakage current for CC pins when device is powered	VPWR = 3.3 V, VM = 3.3 V, VC _{CCx} = 3.6 V, CCx pins are floating, measure leakage into C _{CCx} pins. Result must be same if CCx side is biased and C _{CCx} is left floating			5	μA
I _{C_CC_LEAK_OVP} Leakage current for C _{CCx} pins when device is in OVP	VPWR = VM = 0 V or 3.3 V, VC _{CCx} = 24 V, CCx = 0 V, measure leakage into C _{CCx} pins			1500	μA
I _{CC_LEAK_OVP} Leakage current for CCx pins when device is in OVP	VPWR = VM = 0 V or 3.3 V, VC _{CCx} = 24 V, CCx = 0 V, measure leakage flowing out of CCx pins			40	μA
FLT PIN					
V _{OL} Low-level output voltage for FLT pin	IOL = 3 mA. Measure the voltage at the FLT pin			0.4	V

6.7 Timing Requirements

		MIN	NOM	MAX	UNIT
POWER-ON AND POWER-OFF TIMINGS					
t_{ON}	Time from crossing rising VPWR UVLO until CC OVP FETs are on. VPWR slew rate = 0.347 V/ μ s			200	μ s
dV_{PWR_OFF}/dt	Minimum slew rate allowed to guarantee CC FETs turn off during a power off	–0.5			V/ μ s
OVERVOLTAGE PROTECTION					
$t_{OVP_RESPONSE_CC}$	OVP response time on the CC pins. Time from OVP asserted until OVP FETs turn off. Hot-Plug C _{CCx} to 24 V with a 1-m cable. C _{CCx} slew rate = 4 V/ns. Place a 30- Ω on CCx		145		ns
$t_{OVP_RECOVERY_CC}$	OVP recovery time on the CC pins. Time from OVP removal until FET turns back on. VM = 10.8 V. Step C _{CCx} down from 6.3 V to 3.3 V at a 0.343-V/ μ s slew rate		30		μ s
$t_{OVP_RECOVERY_CC}$	OVP recovery time on the CC pins. Time from OVP removal until FET turns back on. VM = 3.3 V. Step C _{CCx} down from 6.3 V to 0.49 V at a 0.321-V/ μ s slew rate		200		μ s
$t_{OVP_FLT_ASSERTION}$	Time from OVP asserted to $\overline{FLT}$ assertion. $\overline{FLT}$ assertion is when the $\overline{FLT}$ pin reaches 10% of its starting value. C _{CCx} from 0 V to 6.3 V at a 0.645-V/ μ s slew rate		1		μ s
$t_{OVP_FLT_DEASSERTION}$	Time from OVP removal to $\overline{FLT}$ deassertion. $\overline{FLT}$ deassertion is when the $\overline{FLT}$ pin reaches 90% of its final value. C _{CCx} from 6.3 V to 0 V at a 0.696-V/ μ s slew rate		20		μ s

6.8 Typical Characteristics

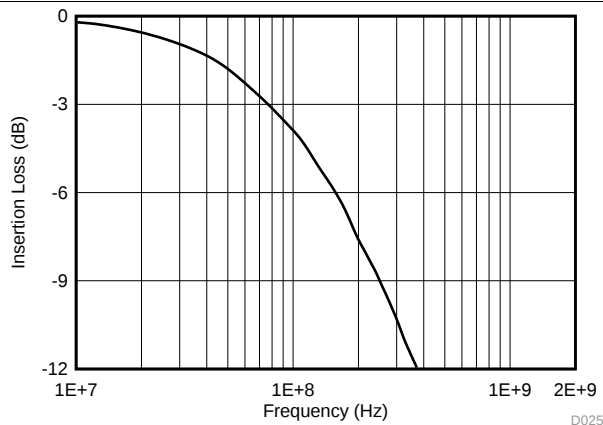


图 1. CC S21 BW

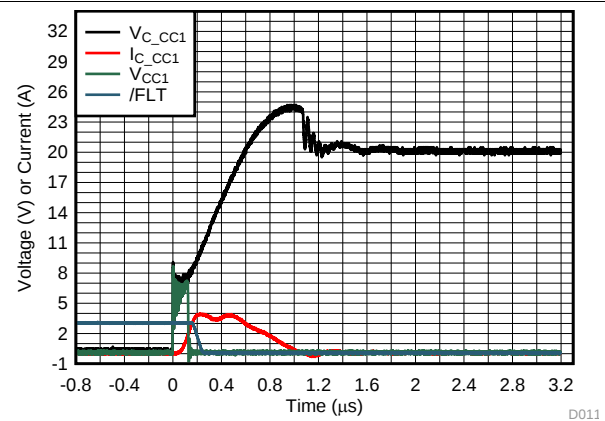


图 2. CC Short-to-V_{BUS} 20-V VM = 3.3 V

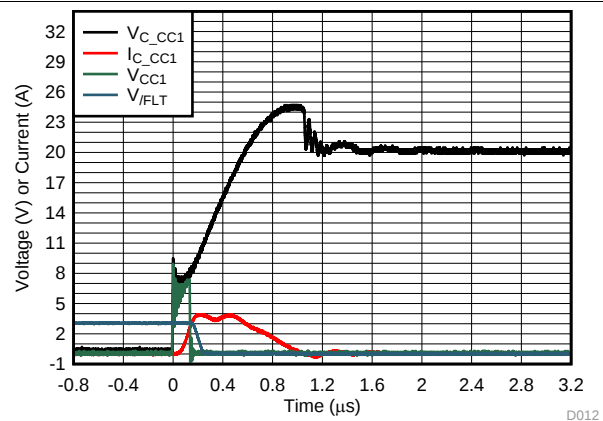


图 3. CC Short-to-V_{BUS} 20-V VM = 13 V

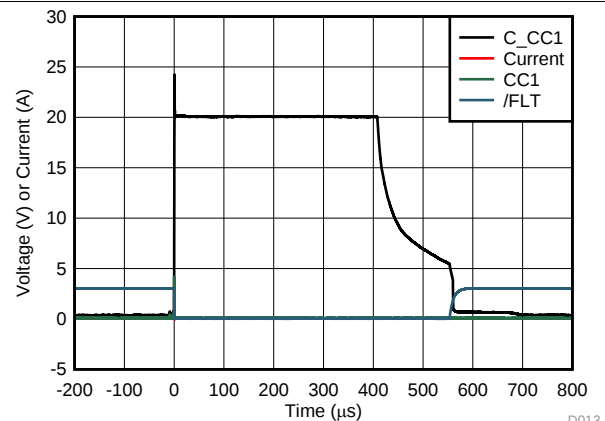


图 4. CC OVP Recovery VM = 3.3 V

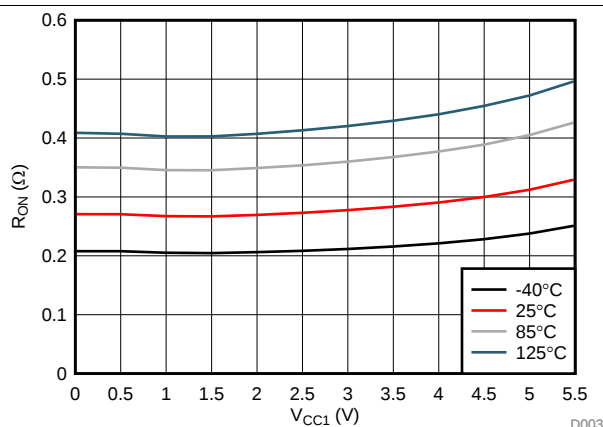


图 5. CC RON Flatness, VM = 8.7 V

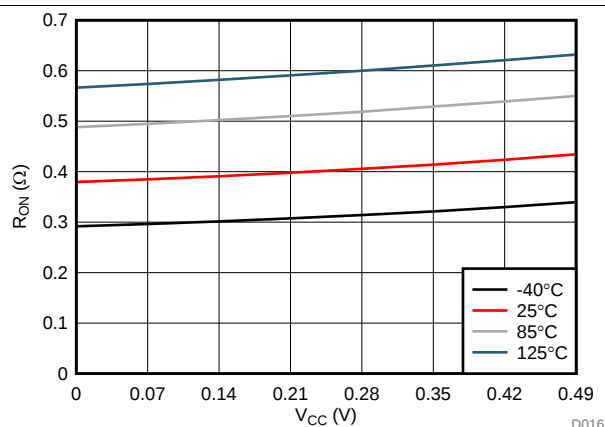


图 6. CC RON Flatness, VM = 2.7 V

Typical Characteristics (continued)

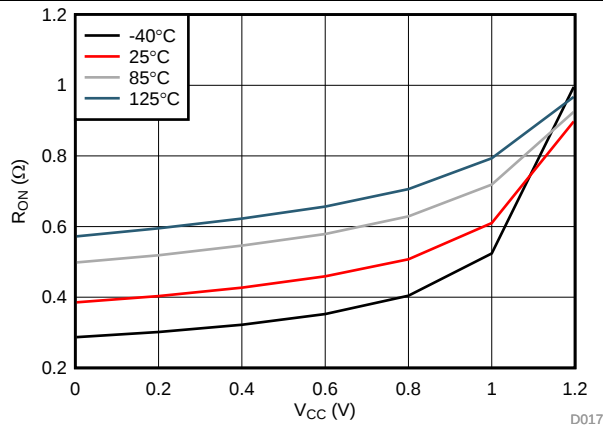


図 7. CC R_{ON} Flatness, $V_M = 2.7$ V

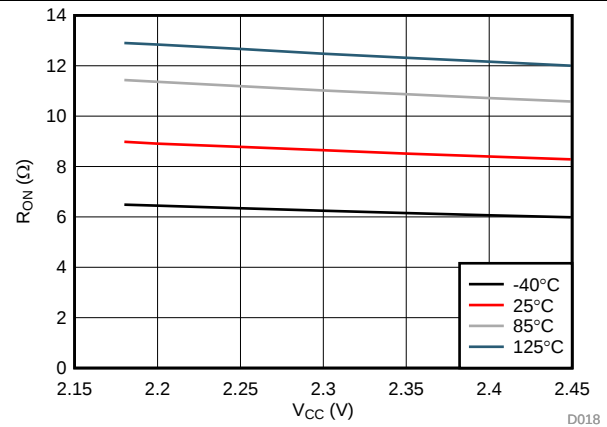


図 8. CC R_{ON} Flatness, $V_M = 2.7$ V

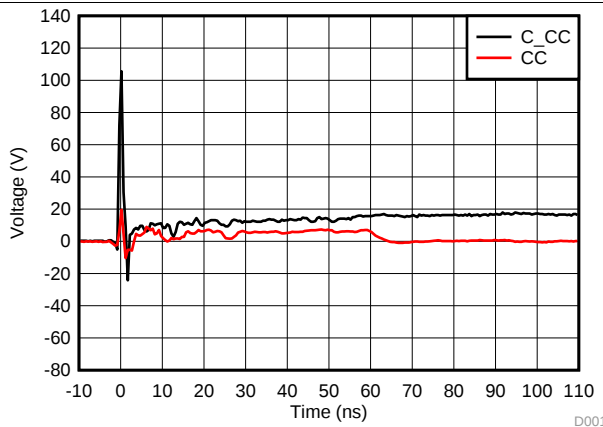


図 9. CC IEC 61000-4-2 8-kV Response Waveform

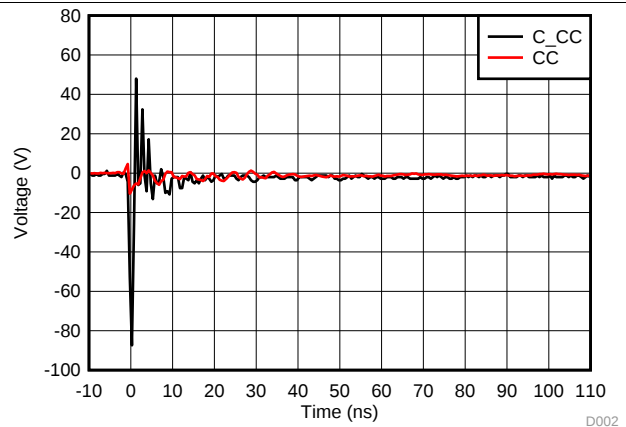


図 10. CC IEC 61000-4-2 -8-kV Response Waveform

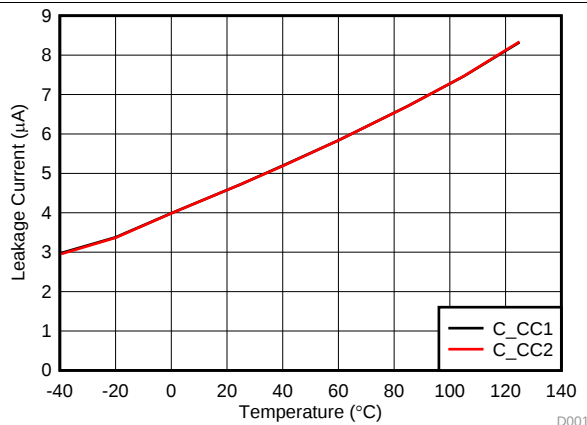


図 11. CC Path Leakage Current vs Ambient Temperature at $C_{CC} = 5.5$ V

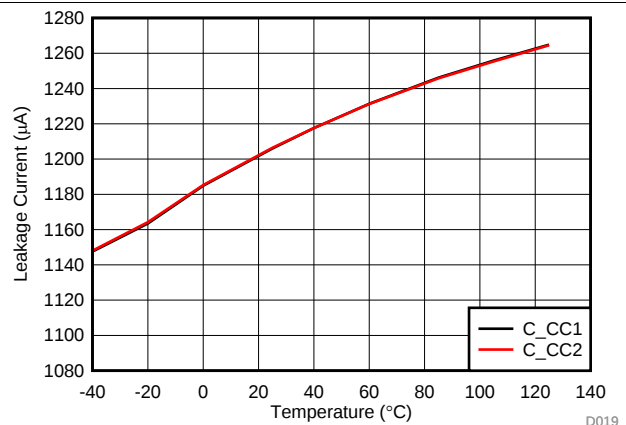


図 12. C_{CC} OVP Leakage Current vs Ambient Temperature at $C_{CC} = 24$ V

Typical Characteristics (continued)

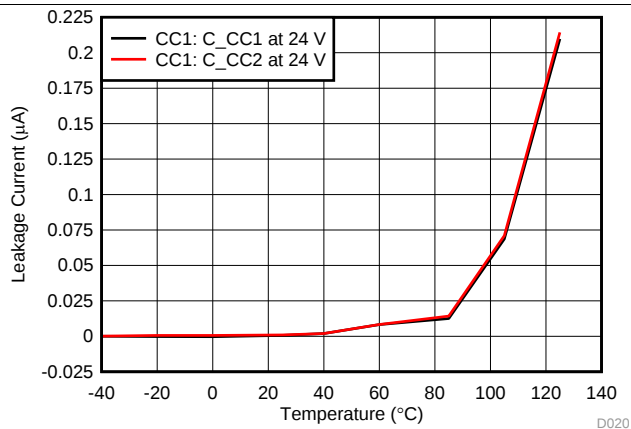


Figure 13. CC OVP Leakage Current vs Ambient Temperature at $C_{CC} = 24\text{ V}$

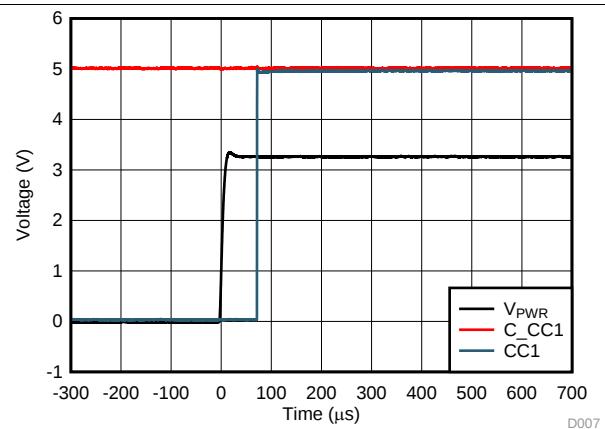


Figure 14. CC FET Turnon Timing

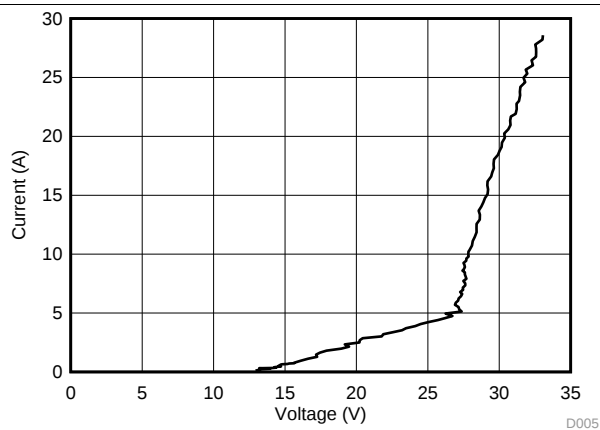


Figure 15. C_{CC} TLP Curve Unpowered

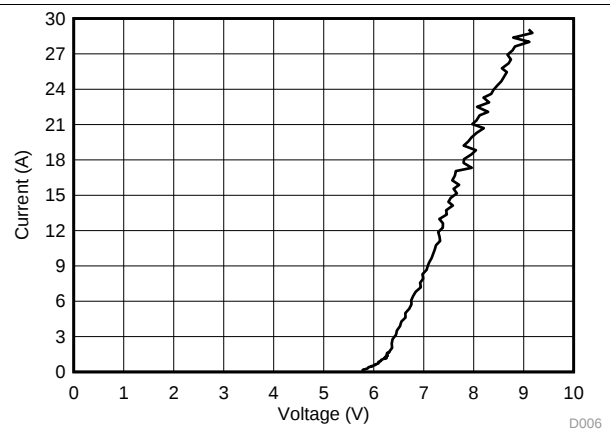


Figure 16. CC TLP Curve Unpowered

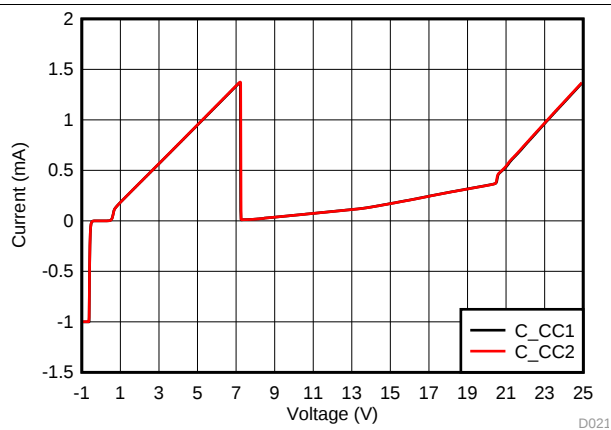


Figure 17. CC IV Curve

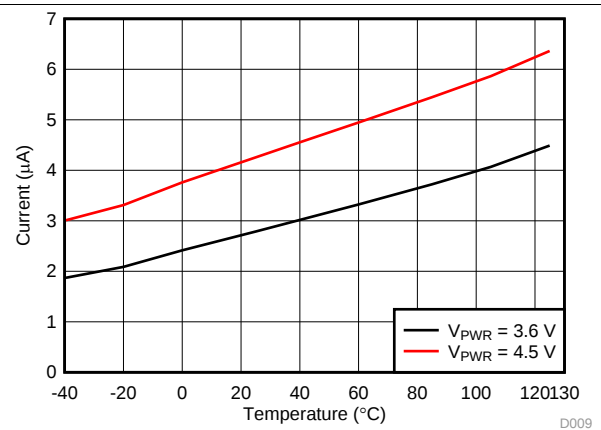


Figure 18. V_{PWR} Supply Leakage vs Ambient Temperature With C_{CC} Floating or GND

Typical Characteristics (continued)

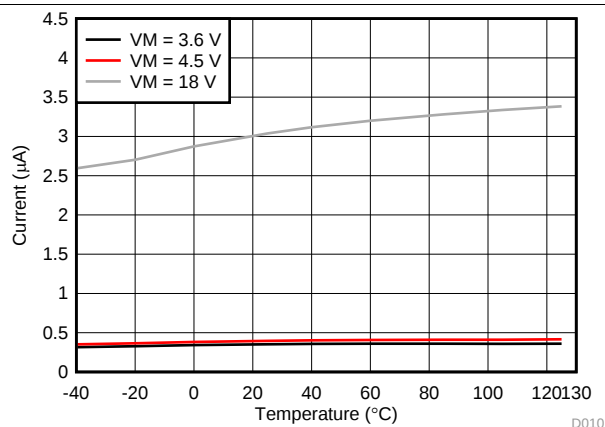


Figure 19. V_M Supply Leakage vs Ambient Temperature With C_{CC} Floating or GND

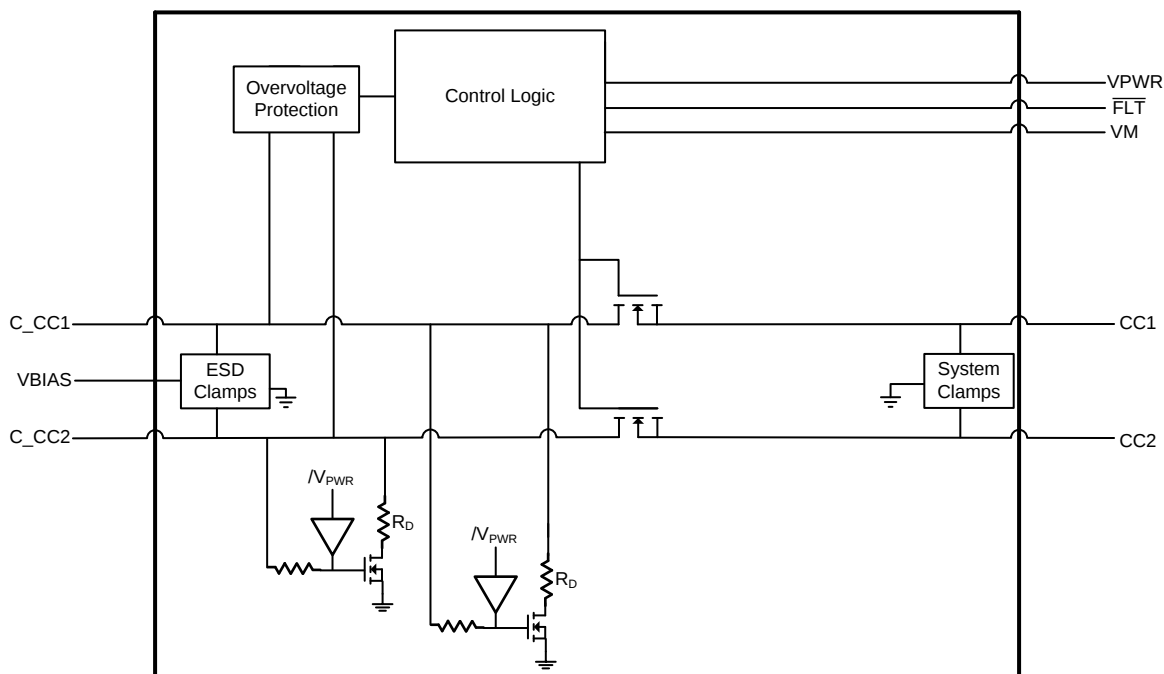
7 Detailed Description

7.1 Overview

The TPD2S300 is a low quiescent current, single chip USB Type-C port protection solution that provides 24-V Short-to- V_{BUS} overvoltage and IEC ESD protection. Due to the small pin pitch of the USB Type-C connector and non-compliant USB Type-C cables and accessories, the V_{BUS} pins can get shorted to the CC pins inside the USB Type-C connector. Because of this Short-to- V_{BUS} event, the CC pins need to be short-to- V_{BUS} tolerant, to support protection on the full USB PD voltage range. Even if a device does not support 20-V operation on V_{BUS} , non-complaint adaptors can start out with 20-V V_{BUS} condition, making it necessary for any USB Type-C device to support 20-V protection. Although the USB-PD specification has a maximum V_{BUS} voltage of 21.5 V, non-complaint adaptors could go outside this maximum. Therefore, the TPD2S300 integrates two channels of 24-V Short-to- V_{BUS} overvoltage protection for the CC1 and CC2 pins of the USB Type-C connector.

Additionally, IEC 61000-4-2 system level ESD protection is required in order to protect a USB Type-C port from ESD strikes generated by end product users. The TPD2S300 integrates two channels of IEC61000-4-2 ESD protection for the CC1 and CC2 pins of the USB Type-C connector. Additionally, high voltage IEC ESD protection that is at least 22-V DC tolerant is required for the CC lines in order to simultaneously support IEC ESD and Short-to- V_{BUS} protection (although 24-V DC tolerant is recommended, which the TPD2S300 integrates); there are not many discrete market solutions that can provide this kind of protection. This high-voltage IEC ESD diode is what the TPD2S300 integrates, specifically designed to guarantee it works in conjunction with the overvoltage protection FETs inside the device. This sort of solution is very hard to generate with discrete components.

7.2 Functional Block Diagram



Copyright © 2017, Texas Instruments Incorporated

图 20. TPD2S300

7.3 Feature Description

7.3.1 2-Channels of Short-to- V_{BUS} Overvoltage Protection (CC1, CC2 Pins): 24- V_{DC} Tolerant

The TPD2S300 provides 2-channels of Short-to- V_{BUS} Overvoltage Protection for the CC1 and CC2 pins of the USB Type-C connector. The TPD2S300 is able to handle 24-V DC on its C_CC1 and C_CC2 pins. This is necessary because according to the USB PD specification, with V_{BUS} set for 20-V operation, the V_{BUS} voltage is allowed to legally swing up to 21 V, and 21.5 V on voltage transitions from a different USB PD V_{BUS} voltage. The TPD2S300 builds in tolerance up to 24- V_{BUS} to provide margin above this 21.5 V specification to be able to support USB PD adaptors that may break the USB PD specification.

When a short-to- V_{BUS} event occurs, ringing happens due to the RLC elements in the hot-plug event. With very low resistance in this RLC circuit, ringing up to twice the settling voltage can appear on the connector. More than 2x ringing can be generated if any capacitor on the line derates in capacitance value during the short-to- V_{BUS} event. This means that more than 44 V could be seen on a USB Type-C pin during a Short-to- V_{BUS} event. The TPD2S300 has built in circuit protection to handle this ringing. The diode clamps used for IEC ESD protection also clamp the ringing voltage during the short-to- V_{BUS} event to limit the peak ringing to around 30 V. Additionally, the overvoltage protection FETs integrated inside the TPD2S300 are 30-V tolerant, therefore being capable of supporting the high voltage ringing waveform that is experienced during the short-to- V_{BUS} event. The well designed combination of voltage clamps and 30-V tolerant OVP FETs insures the TPD2S300 can handle Short-to- V_{BUS} hot-plug events with hot-plug voltages as high as 24- V_{DC} .

The TPD2S300 has an extremely fast turnoff time of 145 ns typical. Furthermore, additional voltage clamps are placed after the OVP FET on the system side (CC1, CC2) pins of the TPD2S300, to further limit the voltage and current that is exposed to the USB Type-C CC/PD controller during the 145 ns interval while the OVP FET is turning off. The combination of connector side voltage clamps, OVP FETs with extremely fast turnoff time, and system side voltage clamps all work together to insure the level of stress seen on the CC1 and CC2 pin during a short-to- V_{BUS} event is comparable to an HBM ESD event. This is done by design, as any USB Type-C CC/PD controller has built in HBM ESD protection.

7.3.2 2-Channels of IEC61000-4-2 ESD Protection (CC1, CC2 Pins)

The TPD2S300 integrates 2-Channels of IEC 61000-4-2 system level ESD protection for the CC1 and CC2 pins of the USB Type-C connector. USB Type-C ports on end-products need system level IEC ESD protection in order to provide adequate protection for the ESD events that the connector can be exposed to from end users. High-voltage IEC ESD protection that is 24-V DC tolerant is required for the CC lines in order to simultaneously support IEC ESD and Short-to- V_{BUS} protection; there are not many discrete market solutions that can provide this kind of protection. The TPD2S300 integrates this type of high-voltage ESD protection so a system designer can meet both IEC ESD and Short-to- V_{BUS} protection requirements in a single device.

7.3.3 Low Quiescent Current: 3.23 μ A (Typical), V_{PWR} , $V_M = 3.3$ V

The TPD2S300 is designed with a very low quiescent current of 3.23 μ A (typical) when $V_{PWR} = 3.3$ V and $V_M = 3.3$ V. The TPD2S300 is designed to have a very low quiescent current to support applications like smart-phones where device battery life is crucial. See the [Electrical Characteristics](#) table for complete range of quiescent currents for different V_{PWR} and V_M voltages.

7.3.4 CC1, CC2 Overvoltage Protection FETs 200 mA Capable for Passing V_{CONN} Power

The CC pins on the USB Type-C connector serve many functions; one of the functions is to be a provider of power to active cables. Active cables are required when desiring to pass greater than 3 A of current on the V_{BUS} line or when the USB Type-C port uses the super-speed lines (TX1+, TX2-, RX1+, RX1-, TX2+, TX2-, RX2+, RX2-). When CC is configured to provide power, it is called V_{CONN} . V_{CONN} is a DC voltage source in the range of 3 V–5.5 V. If supporting V_{CONN} , a V_{CONN} provider must be able to provide 1 W of power to a cable; this translates into a current range of 200 mA at 5-V V_{CONN} . Therefore, the TPD2S300 has been designed to handle 200 mA of DC current and to have an R_{ON} low enough to provide a specification compliant V_{CONN} voltage to the active cable.

7.3.5 CC Dead Battery Resistors Integrated for Handling Dead Battery Use Case in Mobile Devices

An important feature of USB Type-C and USB PD is the ability for this connector to serve as the sole power source to mobile devices. With support up to 100 W, the USB Type-C connector supporting USB PD can be used to power a whole new range of mobile devices not previously possible with legacy USB connectors.

Feature Description (continued)

When the USB Type-C connector is the sole power supply for a battery powered device, the device must be able to charge from the USB Type-C connector even when its battery is dead. In order for a USB Type-C power adaptor to supply power on V_{BUS} , R_D pull-down resistors must be exposed on the CC pins of the sink device. These R_D resistors are typically included inside a USB Type-C CC/PD controller. However, when the TPD2S300 is used to protect the USB Type-C port, the OVP FETs inside the device isolates these R_D resistors in the CC/PD controller when the mobile device has no power. This is because when the TPD2S300 has no power, the OVP FETs are turned off to guarantee overvoltage protection in a dead battery condition. Therefore, the TPD2S300 integrates high voltage, dead battery R_D pull-down resistors to allow dead battery charging simultaneously with high-voltage OVP protection.

When the TPD2S300 is unpowered, and the R_P pull-up resistor is connected from a power adaptor, this R_P pull-up resistor activates the R_D resistor inside the TPD2S300. This enables V_{BUS} to be applied from the power adaptor even in a dead battery condition. Once power is restored back to the system and back to the TPD2S300 on its VPWR pin, the TPD2S300 removes its R_D pull-down resistor and turns on its OVP FETs within 200 μ s. The amount of time the TPD2S300 does not have either its R_D exposed or the PD controller's R_D exposed on the CC lines is even less, around 30 μ s in the worst case, to minimize the probability the USB-C/PD controller in the source device interprets this as a disconnect from the sink. This way connection remains uninterrupted.

If desiring to power the CC/PD controller during dead battery mode and if the CC/PD Controller is configured as a DRP, it is critical that the TPD2S300 be powered before or at the same time that the CC/PD controller is powered. It is also critical that when unpowered, the CC/PD controller also expose its dead battery resistors. When the TPD2S300 gets powered, it exposes the CC pins of the CC/PD controller within 200 μ s. Once the TPD2S300 turns on, the R_D pull-down resistors of the CC/PD controller must be present immediately, in order to guarantee the power adaptor connected to power the dead battery device keeps its V_{BUS} turned on. If the power adaptor sees the CC voltage go high to the SRC.Open region, it can disconnect V_{BUS} . This removes power from the device with its battery still not sufficiently charged, which consequently removes power from the CC/PD controller and the TPD2S300. Then the R_D resistors of the TPD2S300 are exposed again and connect the power adaptor's V_{BUS} to start the cycle over. This creates an infinite loop, never or very slowly charging the mobile device.

If the CC/PD Controller is configured for DRP and has started its DRP toggle before the TPD2S300 turns on, this DRP toggle is unable to guarantee that the power adaptor does not disconnect from the port. Therefore, it is recommended if the CC/PD controller is configured for DRP, that its dead battery resistors be exposed as well, and that they remain exposed until the TPD2S300 turns on. This is typically accomplished by powering the TPD2S300 at the same time as the CC/PD controller when powering the CC/PD controller in dead battery operation.

7.3.6 1.4-mm × 1.4-mm WCSP Package

The TPD2S300 comes in a small, 1.4-mm × 1.4-mm WCSP package, greatly reducing the size of implementing a similar protection solution discretely. Smart-phones and tablets need the smallest package size possible due to the space constraints the PCBs have in these devices.

7.4 Device Functional Modes

表 1 describes all of the functional modes for the TPD2S300. The "X" in the below table are "do not care" conditions, meaning any value can be present within the absolute maximum ratings of the datasheet and maintain that functional mode.

表 1. Device Mode Table

Device Mode Table		Inputs			Outputs		
MODE		VPWR	VM	C_CCx	$\overline{\text{FLT}}$	CC FETs	Dead Battery Resistors
Normal Operating Conditions	Unpowered	<UVLO	X	X	High-Z	OFF	ON
	Powered on	>UVLO	$\geq$ VPWR	<OVP	High-Z	ON	OFF
Fault Conditions	CC overvoltage condition	>UVLO	$\geq$ VPWR	>OVP	Low (Fault Asserted)	OFF	OFF

8 Application and Implementation

注

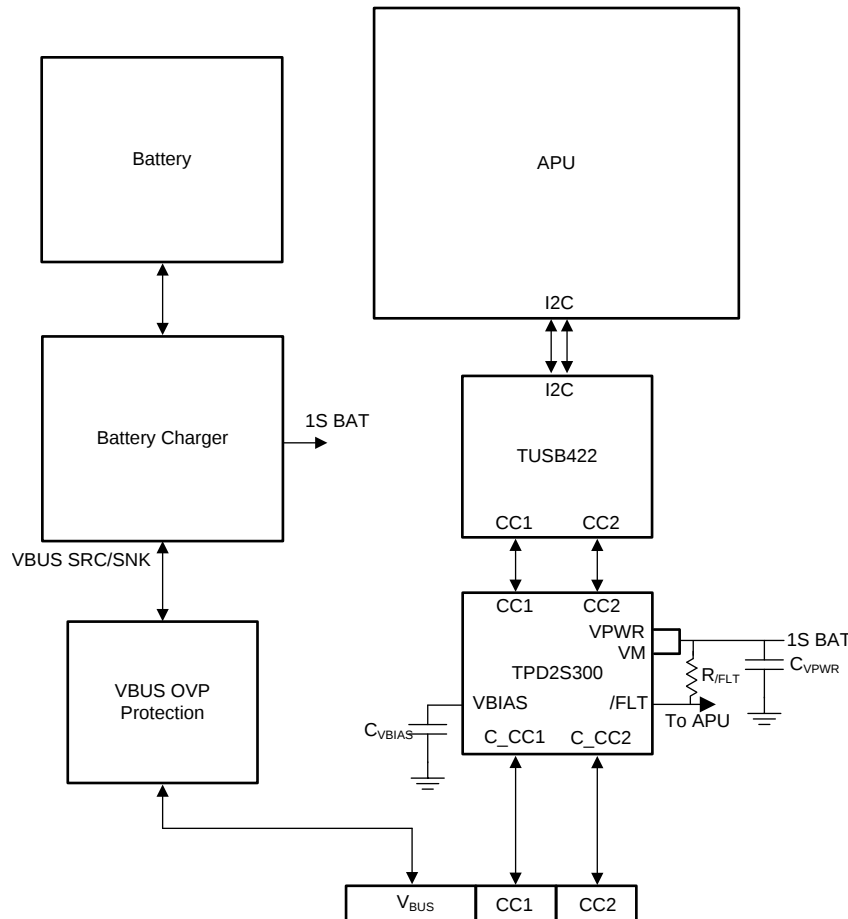
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPD2S300 provides 2-channels of Short-to- V_{BUS} overvoltage protection for the CC1 and CC2 pins of the USB Type-C connector, and 2-channels of IEC ESD protection for the CC1 and CC2 pins of the USB Type-C connector. Care must be taken to insure that the TPD2S300 provides adequate system protection as well as insuring that proper system operation is maintained. The following application examples explain how to properly design the TPD2S300 into a USB Type-C system.

8.2 Typical Application

8.2.1 Smart-Phone Application



Copyright © 2017, Texas Instruments Incorporated

図 21. TPD2S300 Typical Application Diagram

Typical Application (continued)

8.2.1.1 Design Requirements

In this application example, we use the TPD2S300 to protect a USB Type-C port in a smart-phone application. In this application, the smart-phone needs USB2.0 support and 20-V, 2-A charging. Because 20 V is required, USB-PD needs to be used in this application to achieve this, as USB Type-C alone cannot support higher than 5 V. In order to add USB-PD operation in a smart-phone application, the [TUSB422](#) is used. This device is a TCPCi that adds the USB Type C and USB-PD physical layer required to run USB PD over the USB Type-C connector. This device can be connected to the APU in the system through I²C, and the APU can run the USB-PD code.

With USB-C with 20-V PD being used, a Short-to-V_{BUS} event can occur in the system. This short can affect both the CC and SBU pins. However, in this application, since only USB2.0 is required, the SBU pin is not used. Therefore, only CC Short-to-V_{BUS} protection is required to adequately protect the [TUSB422](#) and the system. The CC pins also needs IEC61000-4-2 system level ESD protection. Additionally, with this application being a smart-phone, board space is crucial; a small protection device is required. Therefore, with these application requirements, the TPD2S300 is used, a single-chip solution which integrates all the protection requirements needed for the CC pins in this application.

[表 2](#) shows the TPD2S300 design parameters for this application.

表 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V _{BUS} nominal operating voltage	20 V
Short-to-V _{BUS} tolerance for the CC pins	24 V
VBIAS nominal capacitance	0.1 μF
Dead battery charging	40 W
TPD2S300 VPWR and VM power source	3.3-V LDO or 1S battery
Quiescent current required for protection device	≤ 20 μA
V _{CONN} requirement	V _{CONN} not required
Maximum ambient temperature requirement	85°C

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 VBIAS Capacitor Selection

As noted in the [Recommended Operating Conditions](#) table, a minimum of 35-VBUS rated capacitor is required for the VBIAS pin, and a 50-VBUS capacitor is recommended. The VBIAS capacitor is in parallel with the central IEC diode clamp integrated inside the TPD2S300. A forward biased hiding diode connects the VBIAS pin to the C_{CCx} pins. Therefore, when a Short-to-V_{BUS} event occurs at 20 V, 20-V_{BUS} minus a forward biased diode drop is exposed to the VBIAS pin. Additionally, during the Short-to-V_{BUS} event, ringing can occur almost double the settling voltage of 20 V, allowing a potential 40 V to be exposed to the C_{CCx} pins. However, the internal IEC clamps limits the voltage exposed to the C_{CCx} pins to around 30 V. Therefore, at least 35-VBUS capacitor is required to insure the VBIAS capacitor does not get destroyed during Short-to-V_{BUS} events.

A 50-V, X7R capacitor is recommended, however. This is to further improve the derating performance of the capacitors. When the voltage across a real capacitor is increased, its capacitance value derates. The more the capacitor derates, the greater than 2x ringing can occur in the Short-to-V_{BUS} RLC circuit. 50-V X7R capacitors have great derating performance, allowing for the best Short-to-V_{BUS} performance of the TPD2S300.

Additionally, the VBIAS capacitor helps pass IEC 61000-4-2 ESD strikes. The more capacitance present, the better the IEC performance. So the less the VBIAS capacitor derates, the better the IEC performance. [表 3](#) shows the real capacitors recommended to achieve the best performance with the TPD2S300.

表 3. Design Parameters

CAPACITOR SIZE	PART NUMBER
0402	CC0402KRX7R9BB104
0603	GRM188R71H104KA93D

8.2.1.2.2 Dead Battery Operation

For this application, we want to support 40-W dead battery operation; when the smart-phone is out of battery, we still want to charge the laptop at 20 V and 2 A. This means that the USB PD Controller must receive power in dead battery mode. This means a dead battery LDO must be present in the system to power the TUSB422 and the APU controlling TUSB422 during dead battery. Or, the system PMIC must be able to provide the 1S battery to the APU and TUSB422 during dead battery conditions.

The TPD2S300s OVP FETs remain OFF when it is unpowered in order to insure in a dead battery situation proper protection is still provided to the PD controller or TCPCi in the system, in this case the TUSB422. However, when the OVP FETs are OFF, this isolates the TUSB422's dead battery resistors from the USB Type-C ports CC pins. A USB Type-C power adaptor must see the R_D pull-down dead battery resistors on the CC pins or it does not turn on V_{BUS} to provide power. Since the TUSB422's dead battery resistors are isolated from the USB Type-C connector's CC pins, the TPD2S300 integrates dead battery resistors on its C_CCx pins. The TPD2S300 exposes these pins when it is unpowered.

Once the power adaptor sees the TPD2S300's dead battery resistors, it applies 5 V on the V_{BUS} pin. This provides power to the dead battery LDO or PMIC, allowing power to be applied to the APU and TUSB422 to turn them ON, and allowing the battery to begin to charge. However, this application requires 40-W charging in dead battery mode, so V_{BUS} at 20 V and 2 A is required. USB PD negotiation is required to accomplish this, so the APU through the TUSB422 needs to be able to communicate on the CC pins. This means the TPD2S300 needs to be turned on in dead battery mode as well so the TUSB422 can be exposed to the CC lines. To accomplish this, it is critical that the TPD2S300 is powered by the same dead battery LDO or battery voltage as the APU and TUSB422 during dead battery. This way, the TPD2S300 is turned ON simultaneously with TUSB422.

It is critical that the TUSB422's dead battery resistors are also active on its CC pins for dead battery operation. Once the TPD2S300 receives power, removes its dead battery resistors and turns on its OVP FETs, R_D pull-down resistors must be present on the CC line in order to guarantee the power adaptor stays connected. If R_D is not present and the voltage on CC increases into the SRC.Open range, the power adaptor can interpret this as a port disconnect and remove V_{BUS} .

Once this process has occurred, the APU through the TUSB422 can start negotiating with the power adaptor through USB PD for higher power levels, allowing for 40W operation in dead battery mode.

For more information on the TPD2S300 dead battery operation, see the [CC Dead Battery Resistors Integrated for Handling Dead Battery Use Case in Mobile Devices](#) section in the description section of the datasheet. Also, see [Figure 22](#) for a waveform of the CC line when the TPD2300 is turning on and exposing R_D dead battery resistors to the USB Type-C connector.

8.2.1.2.3 CC Line Capacitance

USB PD has a specification for the total amount of capacitance that is required for proper USB PD BMC operation on the CC lines. The specification from section 5.8.6 of the [USB PD Specification](#) is given in [Table 4](#).

表 4. USB PD cReceiver Specification

NAME	DESCRIPTION	MIN	MAX	UNIT	COMMENT
cReceiver	CC receiver capacitance	200	600	pF	The DFP or UFP system shall have capacitance within this range when not transmitting on the line

Therefore, the capacitance on the CC lines must stay in between 200 pF and 600 pF when USB PD is being used. Therefore, the combination of capacitances added to the system by the TUSB422, the TPD2S300, and any external capacitor must fall within these limits. [Table 5](#) shows that with TUSB422 + TPD2S300, no external capacitor is required to meet the USB-PD specification.

表 5. CC Line Capacitor Calculation

CC Capacitance	MIN	MAX	UNIT	COMMENT
CC line target capacitance	200	600	pF	From the USB PD Specification section (cReceiver, section 5.8.6)
TUSB422 capacitance	200	450	pF	From the TUSB422 Datasheet
TPD2S300 capacitance	30	120	pF	From the Electrical Characteristics table
TUSB422 + TPD2S300	230	570	pF	Meets USB PD cReceiver Specification

8.2.1.2.4 $\overline{\text{FLT}}$ Pin Operation

A $\overline{\text{FLT}}$ pin is provided on the TPD2S300 to give the APU the ability to be notified that a Short-to- V_{BUS} event occurred. Once a Short-to- V_{BUS} occurs on the C_CCx pins, the $\overline{\text{FLT}}$ pin is asserted in 1 μs (typical) so the PD controller can be notified quickly. If V_{BUS} is being shorted to CC, it is recommended to respond to the event by forcing a detach in the USB PD controller to remove V_{BUS} from the port. Although the USB Type-C port using the TPD2S300 is not damaged, as the TPD2S300 provides protection from these events, the other device connected through the USB Type-C Cable or any active circuitry in the cable can be damaged. Although shutting the V_{BUS} off through a detach does not guarantee it stops the other device or cable from being damaged, it can mitigate any high current paths from causing further damage after the initial damage takes place. Additionally, even if the active cable or other device does have proper protection, the Short-to- V_{BUS} event may corrupt a configuration in an active cable or in the other PD controller, so it is best to detach and reconfigure the port. Therefore, in this application it is recommended that the APU monitor the $\overline{\text{FLT}}$ pin for Short-to- V_{BUS} faults.

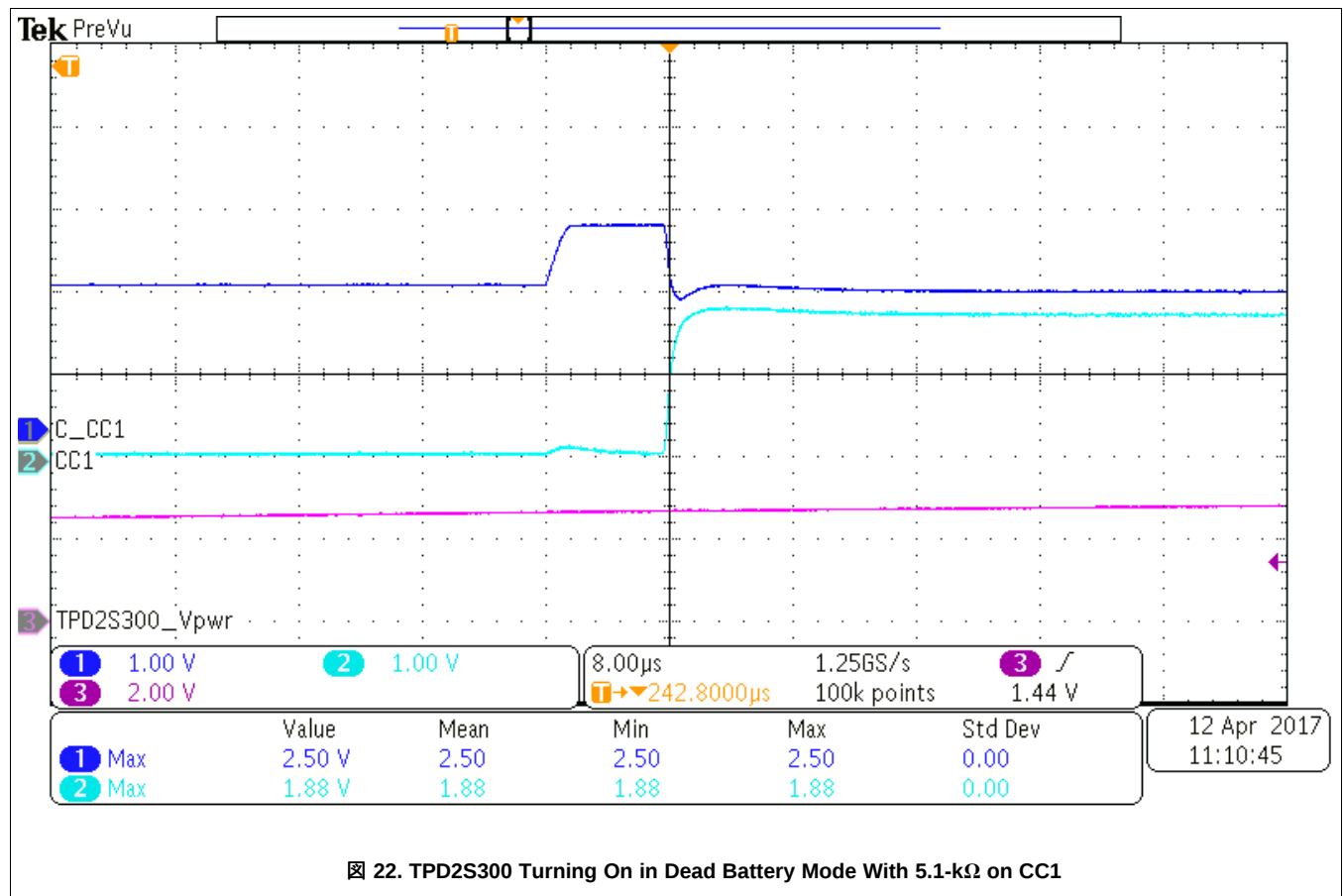
8.2.1.2.5 V_{CONN} Operation

In our current application example, V_{CONN} is not required. Therefore, a 3.3-V source or 1S battery can be connected to the VPWR and VM pins of the TPD2S300 and provide adequate resistance in order to support CC analog and USB PD operation over the CC lines. In fact, the CC OVP FETs resistance specifications are set to optimize the FET size and therefore the TPD2S300 size and still allow proper CC analog and USB PD operation. See the [Electrical Characteristics](#) table for the specific resistances of the CC OVP FETs.

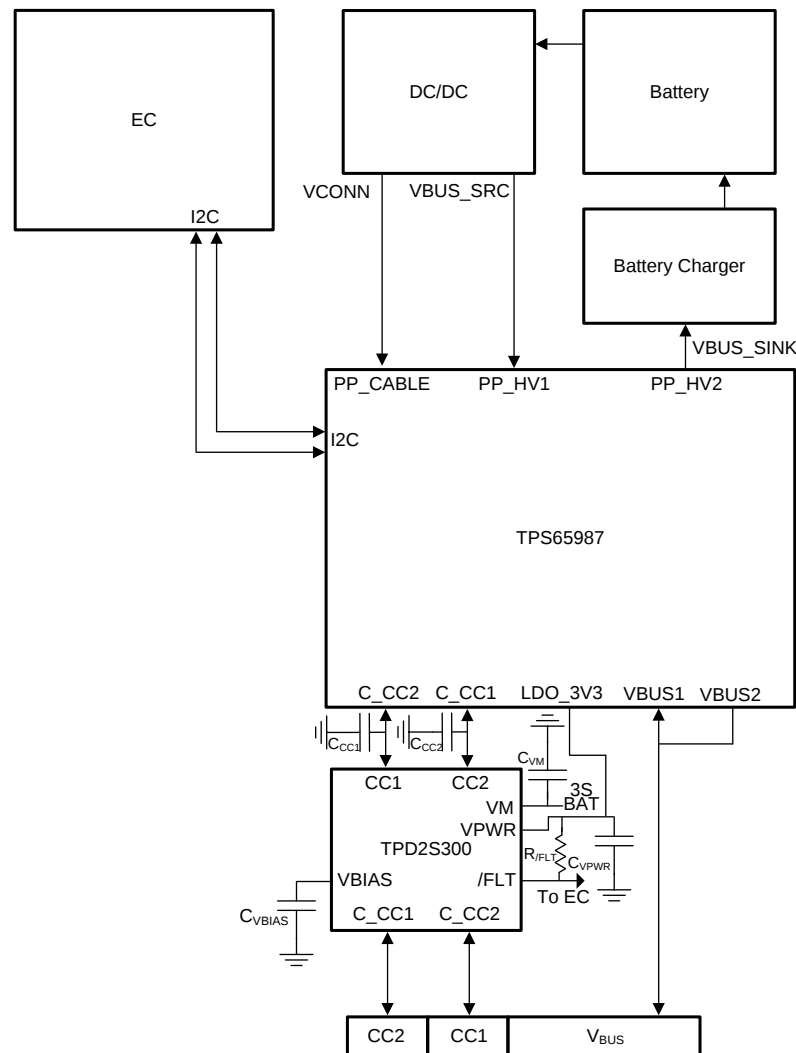
8.2.1.2.6 Low Quiescent Current

Smart-Phone applications require low quiescent current to meet long battery life specifications to provide the best experience to end-users. The TPD2S300 is designed to have very low quiescent current in order to meet these requirements. The lower the voltage kept on the C_CCx lines, and the lower the voltage kept on the VPWR and VM pins, the lower the quiescent current is on the TPD2S300. If an LDO is used that keeps VPWR and VM limited to 3.3 V, then the maximum quiescent current on VPWR is 7 μA , and the maximum current on VM is 1 μA . If the 1S battery is connected to the VPWR and VM pins, such that the maximum voltage applied to VPWR and VM is 4.5 V, then the maximum quiescent current is going to be 12 μA for VPWR, and VM has 1 μA maximum. Therefore, our application can achieve a very low total quiescent current for protection with the TPD2S300, between 8 μA and 13 μA , depending on how the TPD2S300 is powered. For all details on quiescent current values, see the [Electrical Characteristics](#) table.

8.2.1.3 Application Curves



8.2.2 Laptop Application



Copyright © 2017, Texas Instruments Incorporated

图 23. TPD2S300 Typical Application Diagram

8.2.2.1 Design Requirements

In this application example, we use the TPD2S300 to protect a USB Type-C port in a laptop application. In this application, the laptop needs USB3.0 support and 20-V, 5-A charging. Because 20 V is required, USB-PD needs to be used in this application to achieve this, as USB Type-C alone cannot support higher than 5 V. In order to add USB-PD operation in a laptop application, the TPS65987 is used. This device is a full-featured USB Type-C and USB PD controller that integrates all the analog and power paths needed to support 20-V, 5-A charging and USB3.0.

With USB-C with 20-V PD being used, a Short-to- V_{BUS} event can occur in the system. This short can affect both the CC and SBU pins. However, in this application, since only USB3.0 is required, the SBU pin is not used. Therefore, only CC Short-to- V_{BUS} protection is required to adequately protect TPS65987 and the system. The CC pins also need IEC61000-4-2 system level ESD protection. Additionally, with this application being a laptop, board space is crucial; a small protection device is required. Therefore, with these application requirements, the TPD2S300 is used, a single-chip solution which integrates all the protection requirements needed for the CC pins in this application.

表 2 shows the TPD2S300 design parameters for this application.

表 6. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{BUS} nominal operating voltage	20 V
Short-to- V_{BUS} tolerance for the CC pins	24 V
VBIAS nominal capacitance	0.1 μ F
Dead battery charging	100 W
TPD2S300 VPWR power source	3.3-V LDO from TPS65987
TPD2S300 VM power source	3S or 4S Battery
V_{CONN} requirement	1-W V_{CONN} required
Maximum ambient temperature requirement	85°C

8.2.2.2 Detailed Design Procedure

8.2.2.2.1 VBIAS Capacitor Selection

This VBIAS capacitor requirements for this application are identical to the Smart-Phone application; see the [VBIAS Capacitor Selection](#) section for more details.

8.2.2.2.2 Dead Battery Operation

For this application, we want to support 100-W dead battery operation; when the laptop is out of battery, we still want to charge the laptop at 20 V and 5 A. This means that the USB PD Controller must receive power in dead battery mode. The TPS65987 has its own built in LDO in order to supply the TPS65987 power from V_{BUS} in a dead battery condition. The TPS65987 can also provide power to its flash during this condition through its LDO_3V3 pin.

The TPD2S300s OVP FETs remain OFF when it is unpowered in order to insure in a dead battery situation proper protection is still provided to the PD controller in the system, in this case the TPS65987. However, when the OVP FETs are OFF, this isolates the TPS65987's dead battery resistors from the USB Type-C ports CC pins. A USB Type-C power adaptor must see the R_D pull-down dead battery resistors on the CC pins or it does not turn ON V_{BUS} to provide power. Since the TPS65987s dead battery resistors are isolated from the USB Type-C connector's CC pins, the TPD2S300 integrates dead battery resistors on its C_{CCx} pins, and exposes them when the device is unpowered.

Once the power adaptor sees the TPD2S300's dead battery resistors, it applies 5 V on the V_{BUS} pin. This provides power to the TPS65987, turning the PD controller on, and allowing the battery to begin to charge. However, this application requires 100-W charging in dead battery mode, so V_{BUS} at 20 V and 5 A is required. USB PD negotiation is required to accomplish this, so the TPS65987 needs to be able to communicate on the CC pins. This means the TPD2S300 needs to be turned on in dead battery mode as well so the TPD65987's PD controller can be exposed to the CC lines. To accomplish this, it is critical that the TPD2S300 is powered by the TPS65987's internal LDO, the LDO_3V3 pin. This way, when the TPS65987 receives power on V_{BUS} , the TPD2S300 is turned on simultaneously. Additionally, for low resistance VCONN support, the VM pin needs to be connected to the 3S battery, so TPD2S300 needs to be able to receive this voltage in the dead battery condition as well.

It is critical that the TPS65987's dead battery resistors are present; once the TPD2S300 receives power, removes its dead battery resistors and turns on its OVP FETs, R_D pull-down resistors must be present on the CC line in order to guarantee the power adaptor stays connected. If R_D is not present and the voltage on CC increases to Src.Open, the power adaptor can interpret this as a disconnect and remove V_{BUS} .

Also, it is important that the TPS65987's dead battery resistors are present so it properly boots up in dead battery operation with the correct voltages on its CC pins.

Once this process has occurred, the TPS65987 can start negotiating with the power adaptor through USB PD for higher power levels, allowing 100-W operation in dead battery mode.

For more information on the TPD2S300 dead battery operation, see the [CC Dead Battery Resistors Integrated for Handling Dead Battery Use Case in Mobile Devices](#) section in the description section of the datasheet. Also, see [Figure 22](#) for a waveform of the CC line when the TPD2S300 is turning on and exposing the TPS65987's dead battery resistors to the USB Type-C connector.

8.2.2.2.3 CC Line Capacitance

USB PD has a specification for the total amount of capacitance that is required for proper USB PD BMC operation on the CC lines. The specification from section 5.8.6 of the [USB PD Specification](#) is given in [表 4](#).

表 7. USB PD cReceiver Specification

NAME	DESCRIPTION	MIN	MAX	UNIT	COMMENT
cReceiver	CC receiver capacitance	200	600	pF	The DFP or UFP system shall have capacitance within this range when not transmitting on the line

Therefore, the capacitance on the CC lines must stay in between 200 pF and 600 pF when USB PD is being used. Therefore, the combination of capacitances added to the system by the TPS65987, the TPD2S300, and any external capacitor must fall within these limits. [表 5](#) shows the analysis involved in choosing the correct external CC capacitor for this system, and shows that an external CC capacitor is required.

表 8. CC Line Capacitor Calculation

CC Capacitance	MIN	MAX	UNIT	COMMENT
CC line target capacitance	200	600	pF	From the USB PD Specification section (cReceiver, section 5.8.6)
TPS65987 capacitance	70	120	pF	From the TPS65987 Datasheet
TPD2S300 capacitance	30	120	pF	From the Electrical Characteristics table
Proposed capacitor GRM033R71E221KA01D	110	330	pF	CAP, CERM, 220 pF, 25 V, ±10%, X7R, 0201 (For min and max, assume ±50% capacitance change with temperature and voltage derating to be overly conservative)
TPS65987 + TPD2S300 + GRM033R71E221KA01D	210	570	pF	Meets USB PD cReceiver Specification

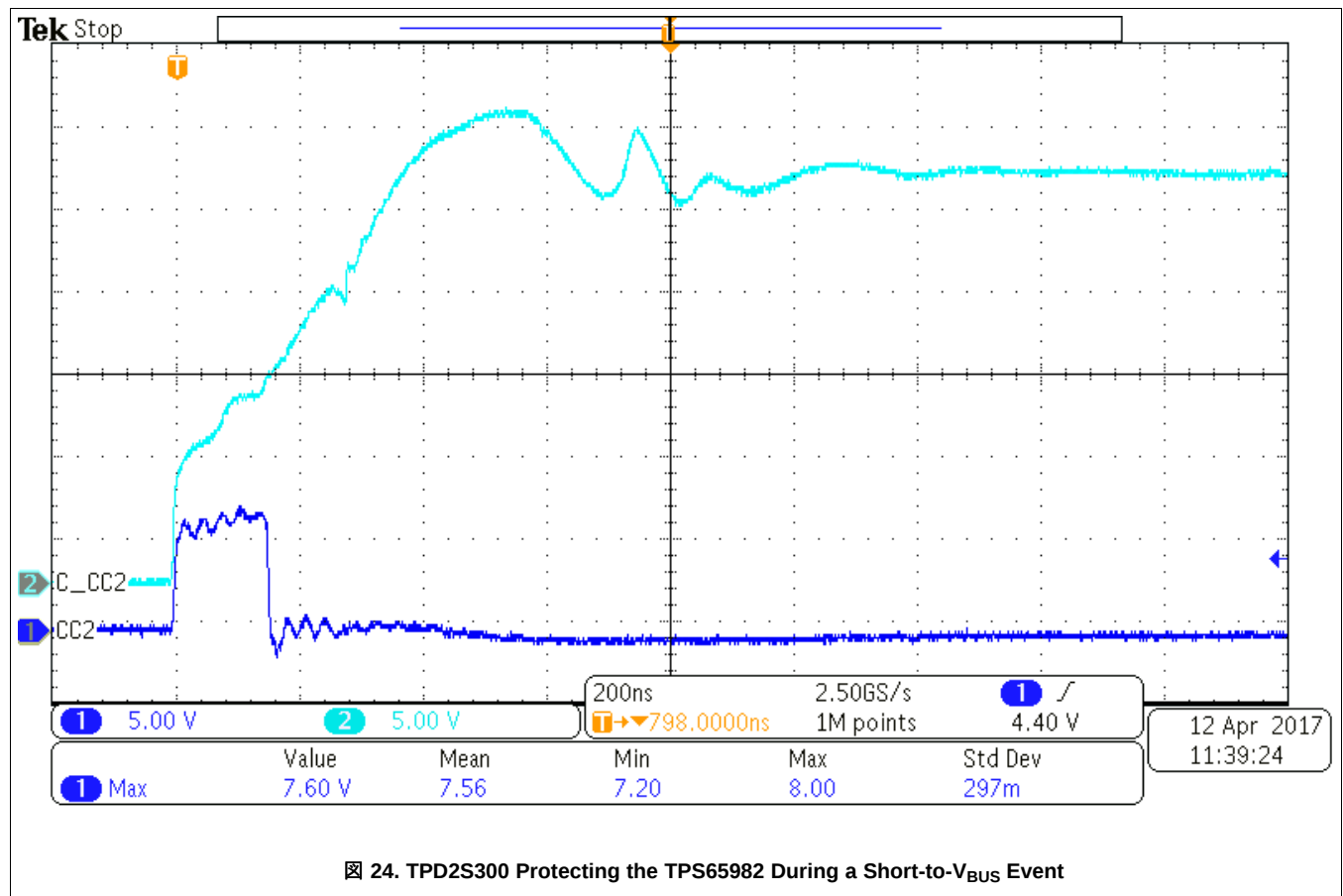
8.2.2.2.4 $\overline{\text{FLT}}$ Pin Operation

This $\overline{\text{FLT}}$ pin recommendation for this application are identical to the Smart-Phone application; see the [\$\overline{\text{FLT}}\$ Pin Operation](#) section for more details.

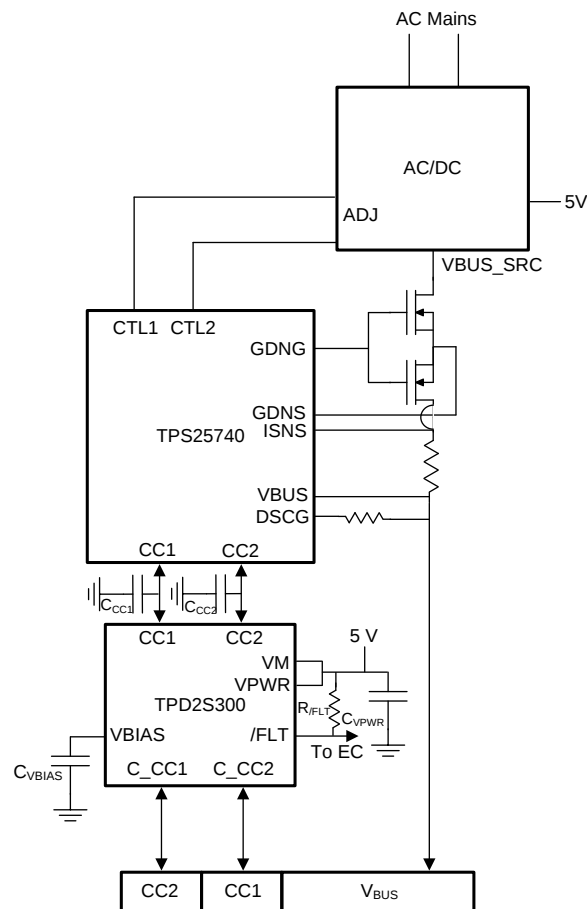
8.2.2.2.5 V_{CONN} Operation

In our current application example, 1-W V_{CONN} is required. With a 5-V source on the TPS65987's PP_CABLE pin, this means 200 mA of current is required. Therefore, it is ideal to put the TPD2S300 in low-resistance mode, which is easy to do in this application because of the presence of a 3S battery in the laptop. Tie the VM pin to the 3S battery voltage. With the VM pin tied to the 3S battery, the worst case resistance of TPD2S300 with 4.87 V on CCx is 608 mΩ. This way with 200 mA flowing through the TPD2S300, voltage drop is much lower across the TPD2S300 and it is easier to achieve the V_{CONN} voltage requirements given in the USB Type-C Specification.

8.2.2.3 Application Curves



8.2.3 Power Adaptor Application



Copyright © 2017, Texas Instruments Incorporated

图 25. TPD2S300 Typical Application Diagram

8.2.3.1 Design Requirements

In this application example, we use the TPD2S300 to protect a USB Type-C port in a power adaptor application. In this application, the power adaptor needs to supply 20 V, 3 A to the device it is charging. Because 20 V is required, USB-PD needs to be used in this application to achieve this, as USB Type-C alone cannot support higher than 5 V. In order to add USB-PD operation in a power adaptor application, the TPS25740 is used. This device is a USB Type-C and USB PD Source Controller.

With USB-C with 20-V PD being used, a Short-to- V_{BUS} event can occur in the system. This short can affect both the CC and SBU pins. However, in this application, since only USB Type-C and PD charging is required, the SBU pin is not used. Therefore, only CC Short-to- V_{BUS} protection is required to adequately protect the TPS25740 and the system. The CC pins also need IEC61000-4-2 system level ESD protection. Additionally, with this application being a power adaptor, board space is crucial; a small protection device is required. Therefore, with these application requirements, the TPD2S300 is used, a single-chip solution which integrates all the protection requirements needed for the CC pins in this application.

表 2 shows the TPD2S300 design parameters for this application.

表 9. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{BUS} nominal operating voltage	20 V
Short-to- V_{BUS} tolerance for the CC pins	24 V
VBIAS nominal capacitance	0.1 μ F

表 9. Design Parameters (continued)

DESIGN PARAMETER	EXAMPLE VALUE
Dead battery charging	No dead battery mode; source only device
TPD2S300 VPWR and VM power source	5-V source
V _{CONN} requirement	V _{CONN} not required
Maximum ambient temperature requirement	85°C

8.2.3.2 Detailed Design Procedure

8.2.3.2.1 VBIAS Capacitor Selection

This VBIAS capacitor requirements for this application are identical to the Smart-Phone application; please see the [VBIAS Capacitor Selection](#) section for more details.

8.2.3.2.2 Dead Battery Operation

This application is source mode only. Therefore, dead battery operation is not required, and R_D resistors must not be exposed on the CC lines. However, because when the TPD2S300 is unpowered it exposes its dead battery resistors, when the wall adaptor is not plugged into the wall, it has RDs present on its CC lines. If it is plugged into a laptop at this point, then the laptop senses a connection and output 5-V V_{BUS}. Therefore, the power switch that sources V_{BUS} in the wall adaptor must be able to block this 5-V V_{BUS} from entering the system when it is unplugged from the wall. If this is maintained, there is not any issue. Once, the wall adaptor is plugged into the wall, it turns ON the TPD2S300. This removes the TPD2S300's RD dead battery resistor, and then the laptop stops sourcing V_{BUS}. Once the laptop starts its DRP toggle, it exposes its RD, which causes a connection with the wall adaptor to occur, and the wall adaptor outputs V_{BUS}, and then PD is negotiated like normal.

8.2.3.2.3 CC Line Capacitance

USB PD has a specification for the total amount of capacitance that is required for proper USB PD BMC operation on the CC lines. The specification from section 5.8.6 of the [USB PD Specification](#) is given in [表 10](#).

表 10. USB PD cReceiver Specification

NAME	DESCRIPTION	MIN	MAX	UNIT	COMMENT
cReceiver	CC receiver capacitance	200	600	pF	The DFP or UFP system shall have capacitance within this range when not transmitting on the line

Therefore, the capacitance on the CC lines must stay in between 200 pF and 600 pF when USB PD is being used. Therefore, the combination of capacitances added to the system by the TPS25740, the TPD2S300, and any external capacitor must fall within these limits. [表 11](#) shows the analysis involved in choosing the correct external CC capacitor for this system, and shows that an external CC capacitor is required.

表 11. CC Line Capacitor Calculation

CC Capacitance	MIN	MAX	UNIT	COMMENT
CC line target capacitance	200	600	pF	From the USB PD Specification section (cReceiver, section 5.8.6)
TPS25740 capacitance	~0	10	pF	From the TPS25740 Datasheet
TPD2S300 capacitance	30	120	pF	From the Electrical Characteristics table
Proposed capacitor GRM033R71E331KA01D	198	462	pF	CAP, CERM, 330 pF, 25 V, ±10%, X7R, 0201 (For min and max, assume ±40% capacitance change with temperature and voltage derating to be overly conservative)
TPS25740 + TPD2S300 + GRM033R71E331KA01D	228	592	pF	Meets USB PD cReceiver specification

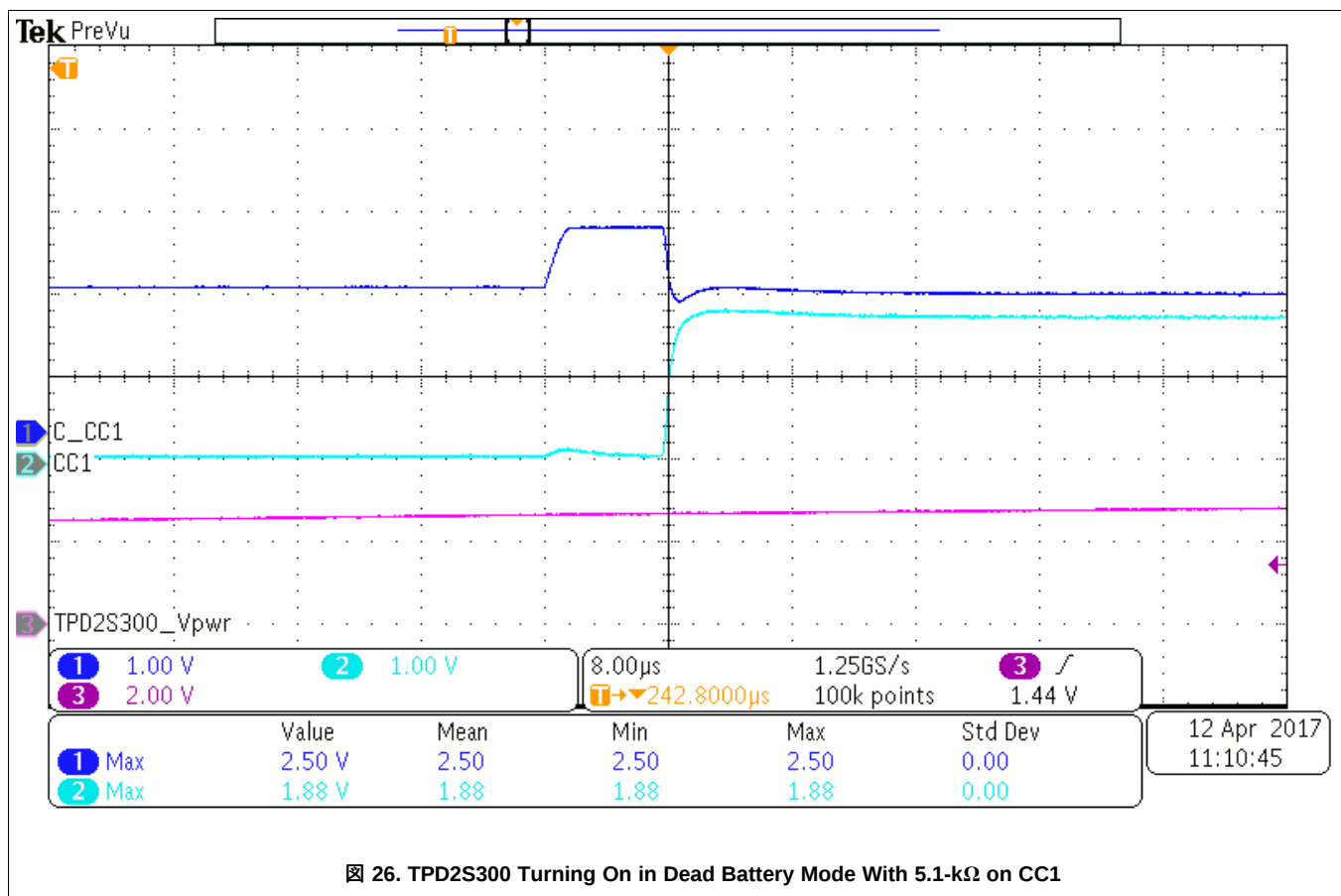
8.2.3.2.4 $\overline{\text{FLT}}$ Pin Operation

The $\overline{\text{FLT}}$ pin recommendation for this application are identical to the Smart-Phone application; see the [FLT Pin Operation](#) section for more details.

8.2.3.2.5 V_{CONN} Operation

In our current application example, V_{CONN} is not required. Therefore, a 3.3-V source or 5-V source can be connected to the VPWR and VM pins of the TPD2S300 to provide adequate resistance in order to support CC analog and USB PD operation over the CC lines. In fact, the CC OVP FETs resistance specifications are set to optimize the FET size and therefore the TPD2S300 size and still allow proper CC analog and USB PD operation. See the [Electrical Characteristics](#) table for the specific resistances of the CC OVP FETs.

8.2.3.3 Application Curves



9 Power Supply Recommendations

The VPWR pin provides power to all the circuitry in the TPD2S300. It is recommended a 1- μ F decoupling capacitor is placed as close as possible to the VPWR pin. If USB PD is desired to be operated in dead battery conditions, it is critical that the TPD2S300 share the same power supply as the PD controller in dead battery boot-up (such as sharing the same dead battery LDO). See the [CC Dead Battery Resistors Integrated for Handling Dead Battery Use Case in Mobile Devices](#) section for more details.

The VM pin is used to control the resistance of the CC OVP FETs. If only CC analog and PD communications are needed over the CC lines, short this pin to VPWR, and no extra capacitor is needed. However, if wanting to use V_{CONN} on CC, and the lower resistance operation of the TPD2S300 is needed, then VM needs to be connected to its own independent voltage source that is $\geq 9\text{ V}$ and $\leq 22\text{ V}$. This is usually the 3S or 4S battery in the system. If connected to its own independent voltage source, then VM will need its own 1- μ F decoupling capacitor; it is recommended to place this capacitor as close as possible to the VM pin.

10 Layout

10.1 Layout Guidelines

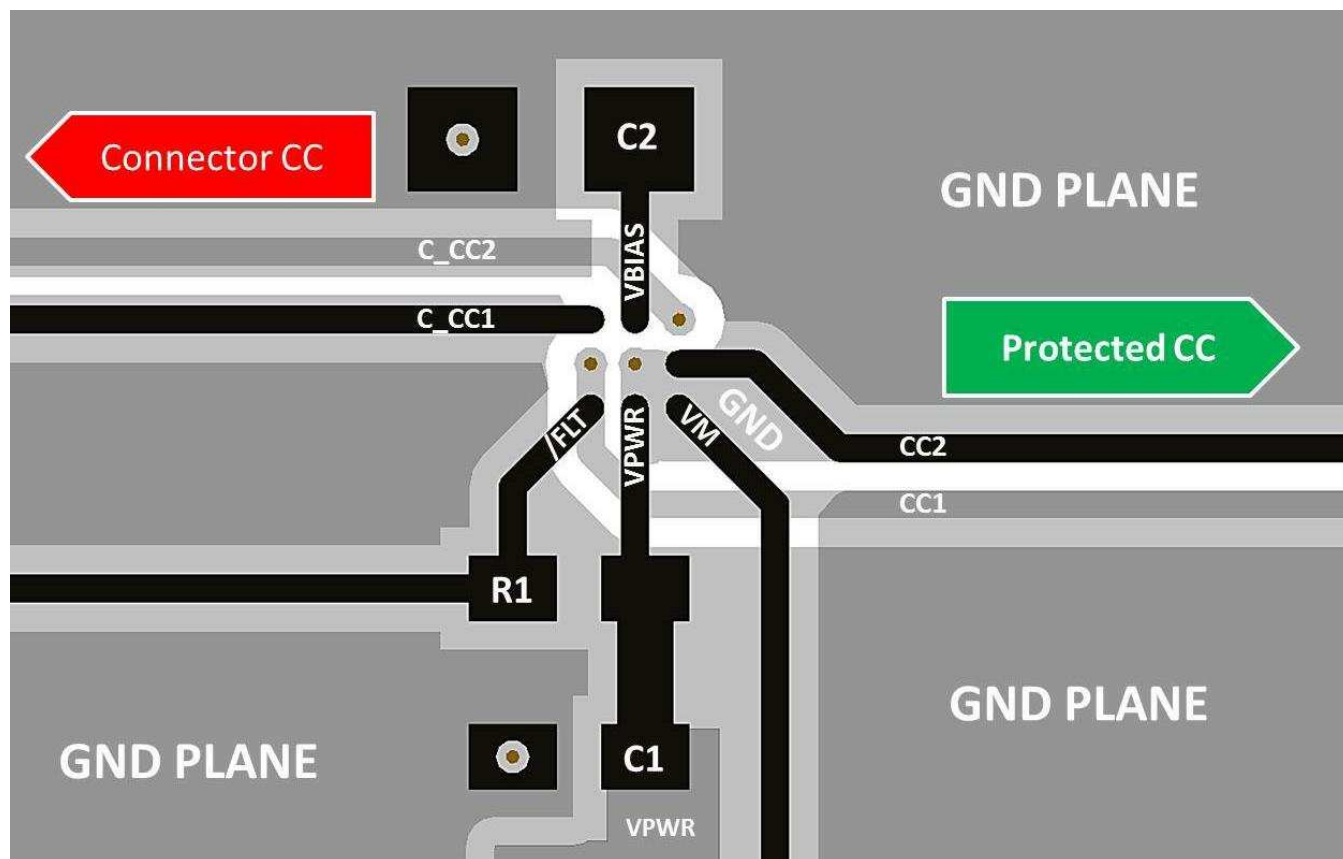
Proper routing and placement is important to maintain the signal integrity the CC line signals. The following guidelines apply to the TPD2S300:

- Place the bypass capacitors as close as possible to the V_{PWR} and V_M pins, and ESD protection capacitor as close as possible to the V_{BIAS} pin. Capacitors must be attached to a solid ground. This minimizes voltage disturbances during transient events such as short-to- V_{BUS} and ESD strikes.

Standard ESD recommendations apply to the C_CC1 and C_CC2 pins:

- The optimum placement for the device is as close to the connector as possible:
 - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
 - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TPD2S300 and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TPD2S300 and the connector by using rounded corners with the largest radii possible.
 - Electric fields tend to build up on corners, increasing EMI coupling.

10.2 Layout Example



✎ 27. TPD2S300 Typical Layout

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントのサポート

11.1.1 関連資料

関連資料については、以下を参照してください。

[『TPD2S300YFF評価モジュール』](#)

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](#)のデバイス製品フォルダを開いてください。右上の隅にある「通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ オンライン・コミュニティ TIのE2E (*Engineer-to-Engineer*) コミュニティ。エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイデアを検討して、問題解決に役立てることができます。

設計サポート TIの設計サポート 役に立つE2Eフォーラムや、設計サポート・ ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

11.4 商標

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

11.5 静電気放電に関する注意事項



すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.6 Glossary

[SLYZ022](#) — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPD2S300YFFR	Active	Production	DSBGA (YFF) 9	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	17W
TPD2S300YFFR.A	Active	Production	DSBGA (YFF) 9	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	17W

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD2S300YFFR	DSBGA	YFF	9	3000	180.0	8.4	1.45	1.45	0.8	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD2S300YFFR	DSBGA	YFF	9	3000	182.0	182.0	20.0

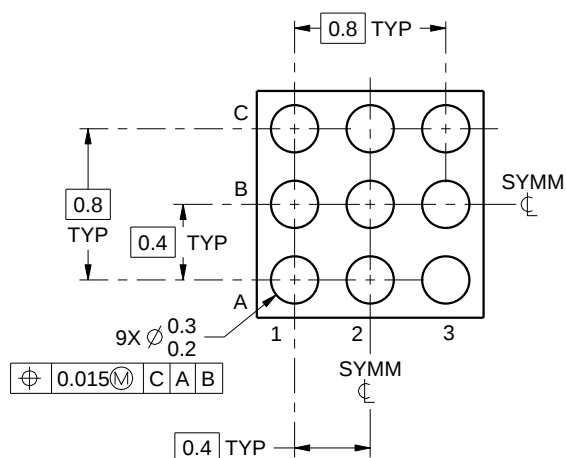
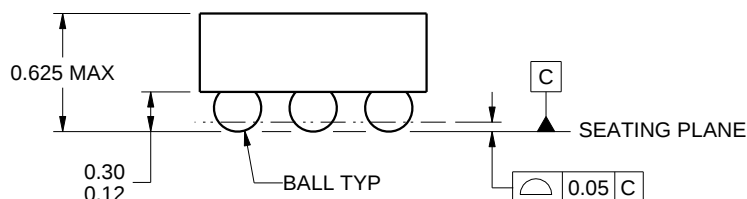
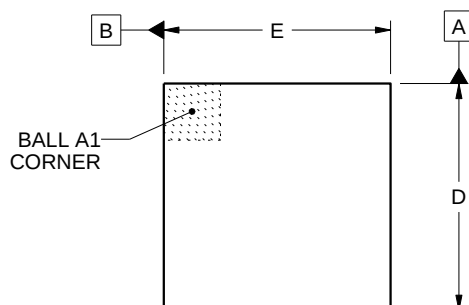
YFF0009



PACKAGE OUTLINE

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 1.39 mm, Min = 1.33 mm

E: Max = 1.39 mm, Min = 1.33 mm

4219552/A 05/2016

NOTES:

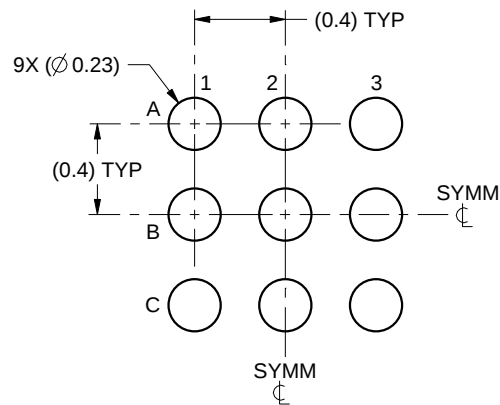
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

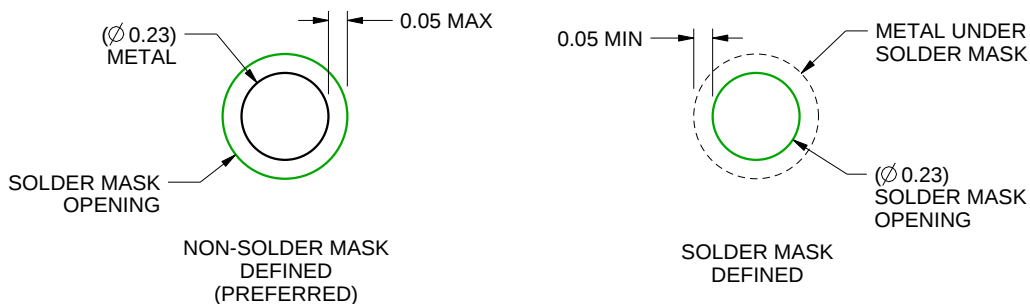
YFF0009

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS
NOT TO SCALE

4219552/A 05/2016

NOTES: (continued)

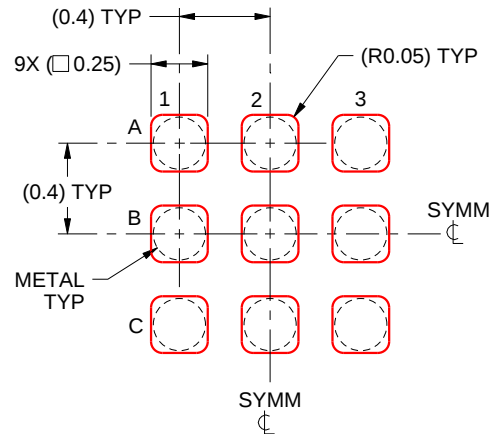
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YFF0009

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4219552/A 05/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適したテキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されているテキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、[テキサス・インスツルメンツの販売条件](#)、または [ti.com](https://www.ti.com) やかかるテキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用されるテキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated