TEXAS INSTRUMENTS
TPD1E01B04-Q1
JAJSL01A – MAY 2021 – REVISED DECEMBER 2021

TPD1E01B04-Q1 車載用 0.2pF、±3.6V、±15kV ESD 保護ダイオード、0402 パッケージ

1 特長

- IEC 61000-4-2 レベル 4 ESD 保護
  - ±15kV 接触放電
  - ±17kV エアギャップ放電
- IEC 61000-4-4 EFT 保護
  - 80A (5/50ns)
- IEC 61000-4-5 サージ保護
  - 2.5A (8/20µs)
- IO 容量:
  - 0.20pF (標準値)
  - 0.23pF (最大値)
- DC ブレークダウン電圧:6.4V (標準値)
- 超低リーク電流:10nA (最大値)
- 低い ESD クランプ電圧:15V (16A TLP の場合)
- 低挿入損失:20GHz
- 最大 20Gbps の高速インターフェイスをサポート
- 業界標準の 0402 フットプリント
- AEC-Q101 準拠
  - デバイス HBM 分類レベル H2
  - デバイス CDM 分類レベル C5
  - デバイスの動作温度範囲:–40℃～+125℃

2 アプリケーション

- 最終製品
  - サラウンド・ビュー・システム
  - ADAS ビジョン・システム
  - リア・ビュー・カメラ
  - インフォテインメントとクラスタ
  - ボディ・コントロール・モジュール
  - ヘッド・ユニット
- インターフェイス
  - 車載用 SerDes:FPD-Link
  - USB Type-C
  - USB 3.1 Gen 2/3.0/2.0
  - HDMI 2.0/1.4
  - 10/100/1000Mbps イーサネット

3 概要

TPD1E01B04-Q1 は、USB Type-C および FPD-Link 回路保護に対応した双方向 TVS ESD 保護ダイオードです。TPD1E01B04-Q1 は、IEC 61000-4-2 国際規格で規定されている最大レベル (レベル 4) の ESD 耐性を備えています。

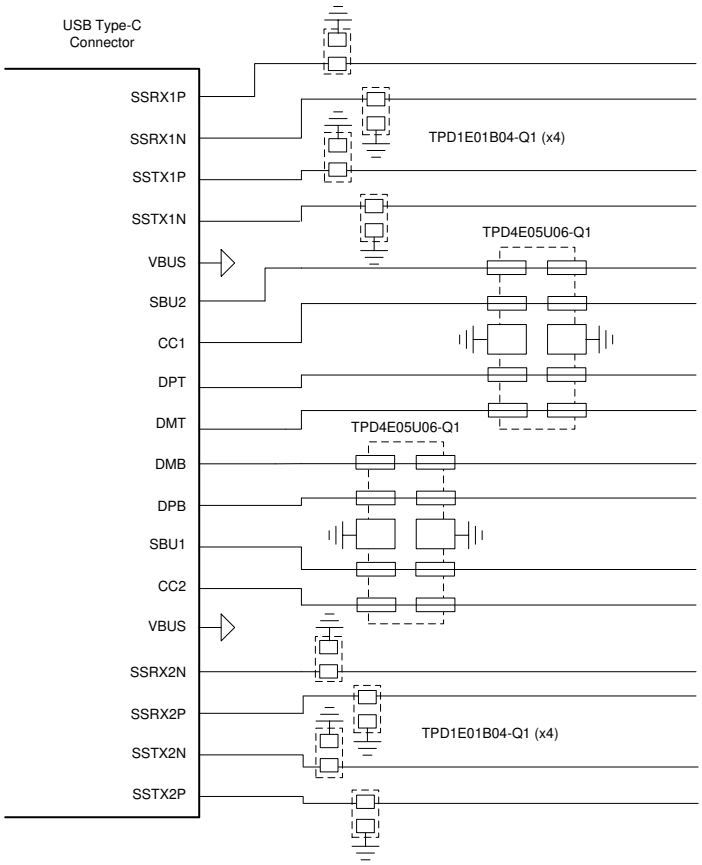
このデバイスは 0.20pF (標準値) の IO 容量を特長としており、USB 3.1 Gen2、FPD-Link などの最大 20Gbps の高速インターフェイスの保護に理想的です。動的抵抗とクランピング電圧が低いため、過渡事象に対してシステム・レベルの保護が保証されます。

TPD1E01B04-Q1 は、業界標準の 0402 (DPY) パッケージで供給されます。

製品情報(1)

部品番号	パッケージ	本体サイズ (公称)
TPD1E01B04-Q1	X1SON (2)	1.00mm × 0.60mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



代表的なアプリケーション

Table of Contents

1 特長 ... 1
2 アプリケーション ... 1
3 概要 ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings—AEC Specification ... 4
6.3 ESD Ratings—IEC Specification ... 4
6.4 ESD Ratings—ISO Specification ... 4
6.5 Recommended Operating Conditions ... 4
6.6 Thermal Information ... 4
6.7 Electrical Characteristics ... 5
6.8 Typical Characteristics ... 6
7 Detailed Description ... 8
7.1 Overview ... 8
7.2 Functional Block Diagram ... 8
7.3 Feature Description ... 8
7.4 Device Functional Modes ... 9
8 Application and Implementation ... 9
8.1 Application Information ... 9
8.2 Typical Application ... 9
9 Power Supply Recommendations ... 10
10 Layout ... 11
10.1 Layout Guidelines ... 11
10.2 Layout Example ... 11
11 Device and Documentation Support ... 12
11.1 Documentation Support ... 12
11.2 Receiving Notification of Documentation Updates ... 12
11.3 サポート・リソース ... 12
11.4 Trademarks ... 12
11.5 Electrostatic Discharge Caution ... 12
11.6 Glossary ... 12
12 Mechanical, Packaging, and Orderable Information ... 12

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (May 2021) to Revision A (December 2021)	Page
• データシートのステータスを事前情報から*量産データに変更*	1

5 Pin Configuration and Functions

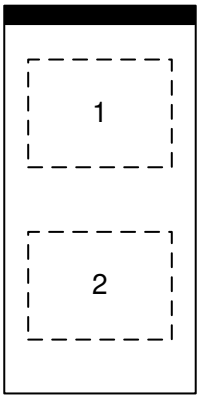


図 5-1. DPY Package 2-Pin X1SON Top View

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	IO	I/O	ESD Protected Channel. If used as ESD IO, connect pin 2 to ground
2	IO	I/O	ESD Protected Channel. If used as ESD IO, connect pin 1 to ground

(1) I = input, O = output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Electrical fast transient	IEC 61000-4-5 (5/50 ns) at 25°C		80	A
Peak pulse	IEC 61000-4-5 power (t_p - 8/20 µs) at 25°C		27	W
	IEC 61000-4-5 current (t_p - 8/20 µs) at 25°C		2.5	A
T_A	Operating free-air temperature	–40	125	°C
T_{stg}	Storage temperature	–65	155	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings—AEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q101-001	±2500	V
		Charged device model (CDM), per AEC Q101-005	±1000	

6.3 ESD Ratings—IEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, all pins	±15000	V
		IEC 61000-4-2 Air-gap Discharge, all pins	±17000	

6.4 ESD Ratings—ISO Specification

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	ISO 10605, 330-pF, 330-Ω, IO	Contact discharge	± 12500	V
			Air-gap discharge	±15000	

6.5 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IO}	Input pin voltage	–3.6		3.6	V
T_A	Operating free-air temperature	–40		125	°C

6.6 Thermal Information

THERMAL METRIC(1)		TPD1E01B04-Q1 DPY (X1SON) 2 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	442.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	243.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	162.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	154.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	163.0	°C/W

6.6 Thermal Information (continued)

THERMAL METRIC(1)		TPD1E01B04-Q1 DPY (X1SON) 2 PINS	UNIT
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.7 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_{IO} < 10 nA	–3.6		3.6	V
V_{BRF}	Breakdown voltage, IO pin to GND	Measured as the maximum voltage before device snaps back into V_{HOLD} voltage		6.4		V
V_{BRR}	Breakdown voltage, GND to IO pin			–6.4		V
V_{HOLD}	Holding voltage	I_{IO} = 1 mA, T_A = 25°C	5	5.9	6.5	V
V_{CLAMP}	Clamping voltage	I_{PP} = 1 A, TLP, from IO to GND		7		V
		I_{PP} = 5 A, TLP, from IO to GND		9.2		
		I_{PP} = 16 A, TLP, from IO to GND		15		
		I_{PP} = 1 A, TLP, from GND to IO		7		
		I_{PP} = 5 A, TLP, from GND to IO		9.2		
		I_{PP} = 16 A, TLP, from GND to IO		15		
I_{LEAK}	Leakage current, IO to GND	V_{IO} = ±2.5 V			10	nA
R_{DYN}	Dynamic resistance	IO to GND		0.57		Ω
		GND to IO		0.57		
C_L	Line capacitance	V_{IO} = 0 V, f = 1 MHz, IO to GND, T_A = 25°C		0.2	0.23	pF

6.8 Typical Characteristics

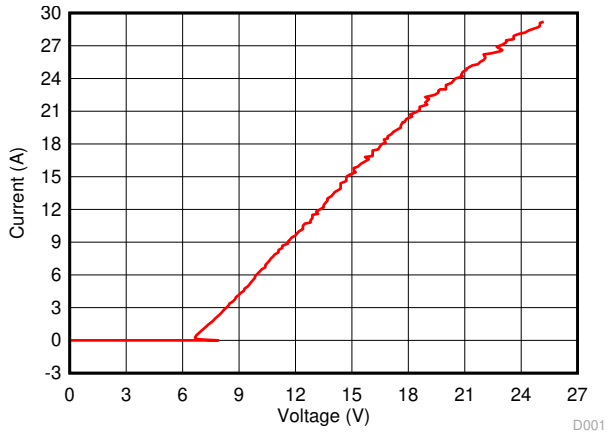


図 6-1. Positive TLP Curve

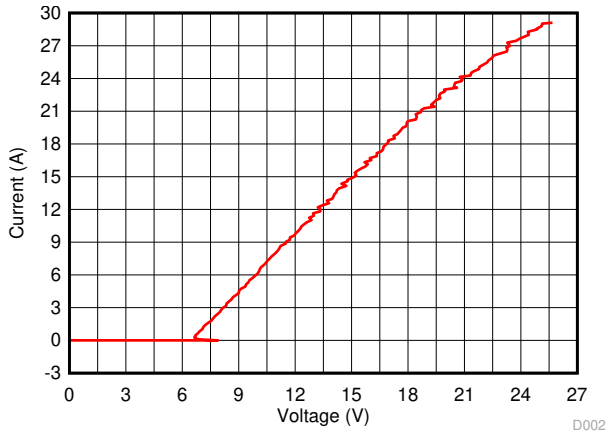


図 6-2. Negative TLP Curve

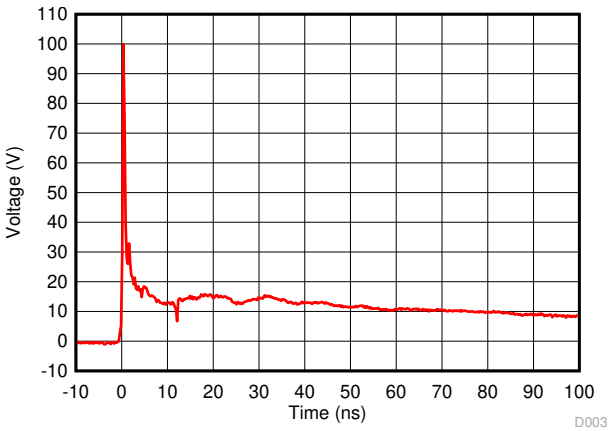


図 6-3. 8-kV IEC Waveform

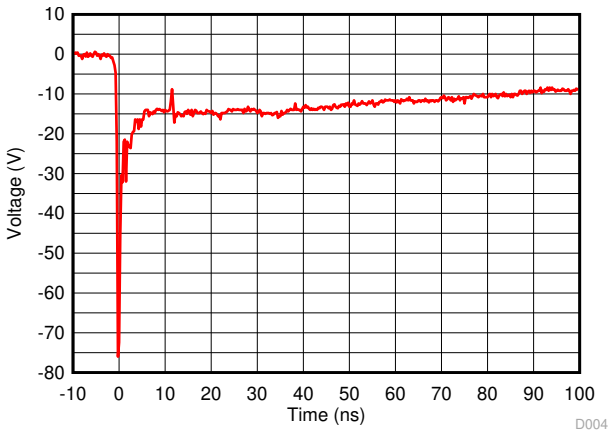


図 6-4. –8-kV IEC Waveform

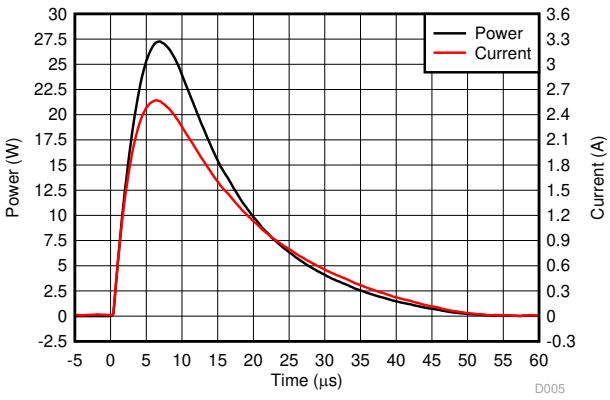


図 6-5. Surge Curve (t_p = 8/20µs), IO pin to GND

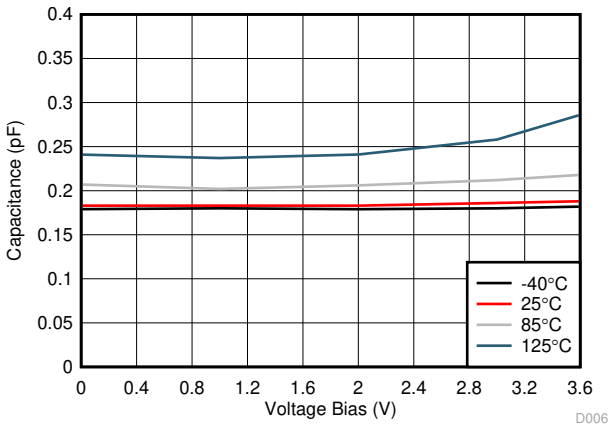


図 6-6. Capacitance vs. Bias Voltage

6.8 Typical Characteristics (continued)

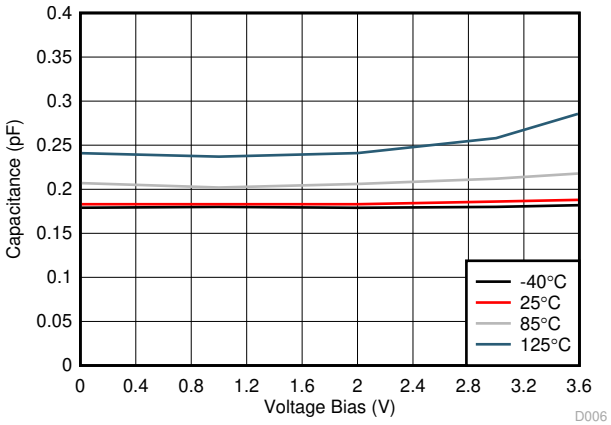


図 6-7. Capacitance vs. Bias Voltage (DPY Package)

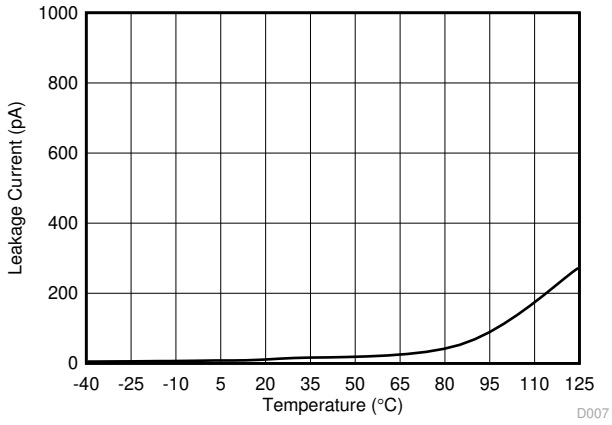


図 6-8. Leakage Current vs. Temperature

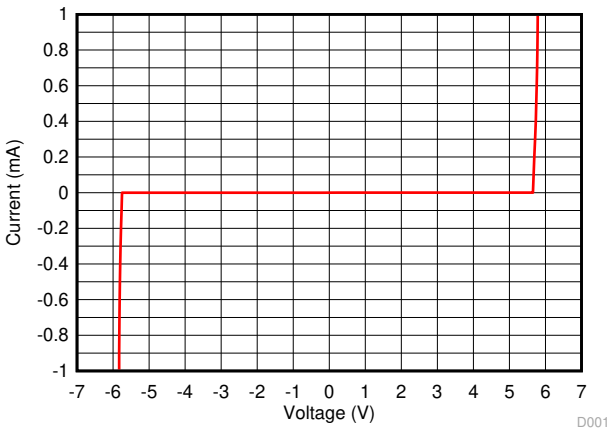


図 6-9. DC Voltage Sweep I-V Curve

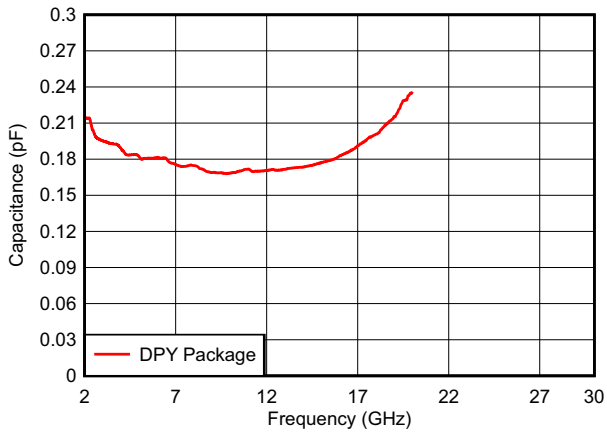


図 6-10. Capacitance vs. Frequency

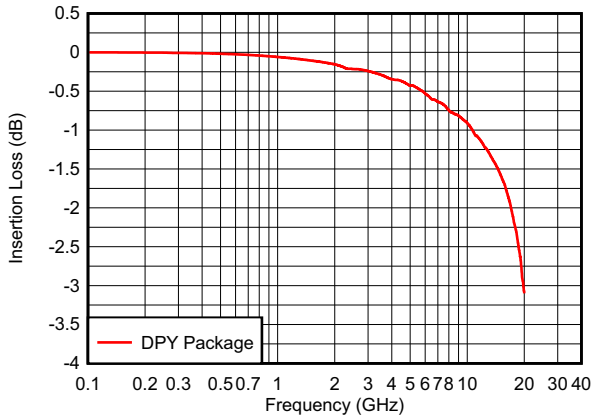


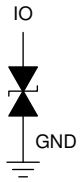
図 6-11. Insertion Loss

7 Detailed Description

7.1 Overview

The TPD1E01B04-Q1 device is a bidirectional ESD Protection Diode with ultra-low capacitance. This device can dissipate ESD strikes above the maximum level specified by the IEC 61000-4-2 International Standard. The ultra-low capacitance makes this device ideal for protecting any super high-speed signal pins including Thunderbolt 3. The low capacitance allows for extremely low losses even at RF frequencies such as USB 3.1 Gen 2, Thunderbolt 3, or antenna applications.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 IEC 61000-4-2 ESD Protection

The I/O pins can withstand ESD events up to ±15-kV contact and ±17-kV air gap. An ESD-surge clamp diverts the current to ground.

7.3.2 IEC 61000-4-4 EFT Protection

The I/O pins can withstand an electrical fast transient burst of up to 80 A (5/50 ns waveform, 4 kV with 50-Ω impedance). An ESD-surge clamp diverts the current to ground.

7.3.3 IEC 61000-4-5 Surge Protection

The I/O pins can withstand surge events up to 2.5 A and 27 W (8/20 µs waveform). An ESD-surge clamp diverts this current to ground.

7.3.4 IO Capacitance

The capacitance between each I/O pin to ground is 0.2 pF (typical) and 0.23 pF (maximum). This device supports data rates up to 20 Gbps.

7.3.5 DC Breakdown Voltage

The DC breakdown voltage of each I/O pin is ±6.4 V (typical). This ensures that sensitive equipment is protected from surges above the reverse standoff voltage of ±3.6 V.

7.3.6 Ultra Low Leakage Current

The I/O pins feature an ultra-low leakage current of 10 nA (maximum) at a bias voltage of ±2.5 V.

7.3.7 Low ESD Clamping Voltage

The I/O pins feature an ESD clamp that is capable of clamping the voltage to 9.2 V (I_{PP} = 5 A).

7.3.8 Supports High Speed Interfaces

This device is capable of supporting high speed interfaces up to 20 Gbps, because of the extremely low IO capacitance.

7.3.9 Industrial Temperature Range

This device features an industrial operating range of –40°C to +125°C.

7.3.10 Easy Flow-Through Routing Package

The layout of this device makes it simple and easy to add protection to an existing layout. The packages offers flow-through routing, requiring minimal modification to an existing layout.

7.4 Device Functional Modes

The TPD1E01B04-Q1 device is a passive integrated circuit that triggers when voltages are above V_{BRF} or below V_{BRR}. During ESD events, voltages as high as ±17 kV (air) can be directed to ground through the internal diode network. When the voltages on the protected line fall below the trigger levels of TPD1E01B04-Q1 (usually within 10s of nano-seconds) the device reverts to passive.

8 Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The TPD1E01B04-Q1 is a diode type TVS which is used to provide a path to ground for dissipating ESD events on high-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a safe level for the protected IC.

8.2 Typical Application

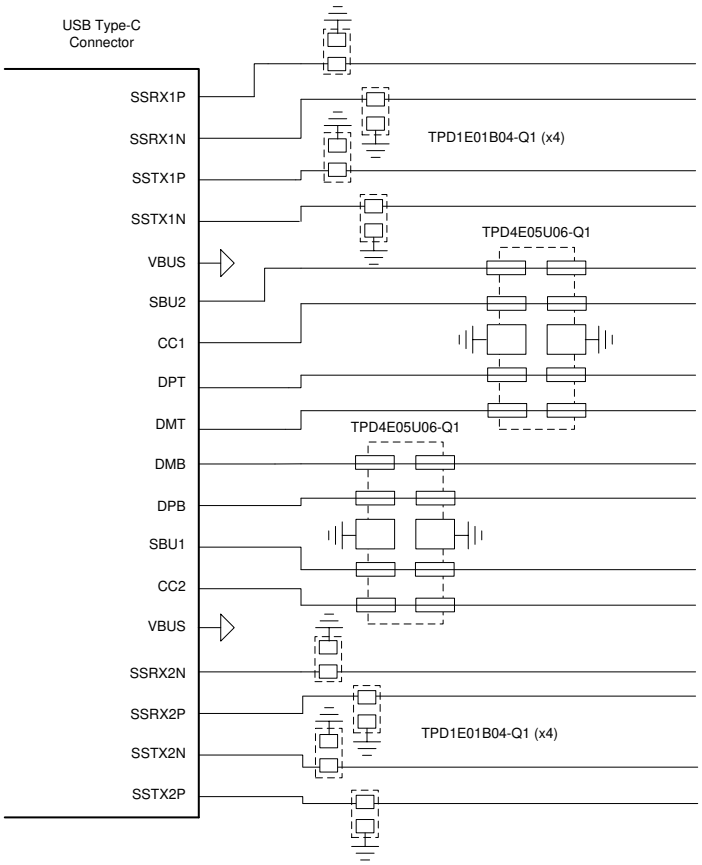


図 8-1. USB Type-C for Thunderbolt 3 ESD Schematic

8.2.1 Design Requirements

For this design example eight TPD1E01B04-Q1 devices and two TPD4E05U06-Q1 devices are being used in a USB Type-C for Thunderbolt 3 application. This provides a complete ESD protection scheme.

Given the Thunderbolt 3 application, the parameters listed in 表 8-1 are known.

表 8-1. Design Parameters

DESIGN PARAMETER	VALUE
Signal range on superspeed Lines	0 V to 3.6 V
Operating frequency on superspeed Lines	up to 10 GHz
Signal range on CC, SBU, and DP/DM Lines	0 V to 5 V
Operating frequency on CC, SBU, and DP/DM Lines	up to 480 MHz

8.2.2 Detailed Design Procedure

8.2.2.1 Signal Range

The TPD1E01B04-Q1 supports signal ranges between –3.6 V and 3.6 V, which supports the SuperSpeed pairs on the USB Type-C application. The TPD4E05U06-Q1 supports signal ranges between 0 V and 5.5 V, which supports the CC, SBU, and DP-DM lines.

8.2.2.2 Operating Frequency

The TPD1E01B04-Q1 has a 0.2 pF (typical) capacitance, which supports the Thunderbolt 3 data rates of 20 Gbps. The TPD4E05U06-Q1 has a 0.5-pF (typical) capacitance, which easily supports the CC, SBU, and DP-DM data rates.

8.2.3 Application Curves

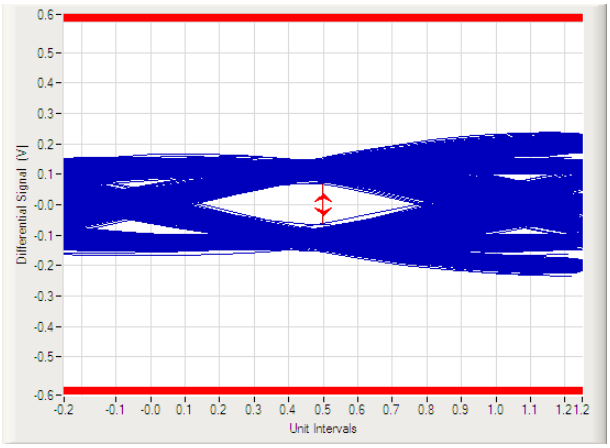


図 8-2. USB 3.1 Gen 2 10-Gbps Eye Diagram (Bare Board)

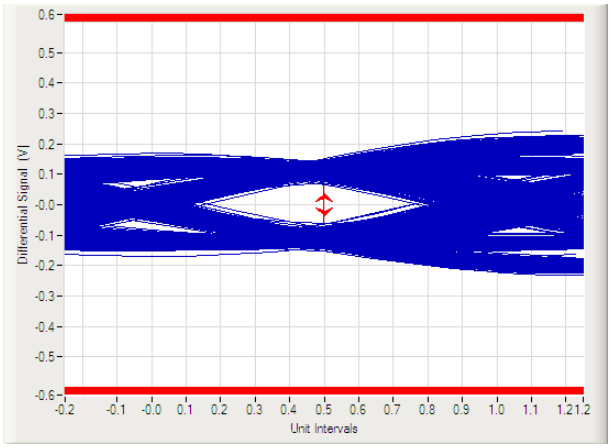


図 8-3. USB 3.1 Gen 2 10-Gbps Eye Diagram (with TPD1E01B04-Q1)

9 Power Supply Recommendations

This device is a passive ESD device so there is no need to power it. Take care not to violate the recommended I/O specification to ensure the device functions properly.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

10.2 Layout Example

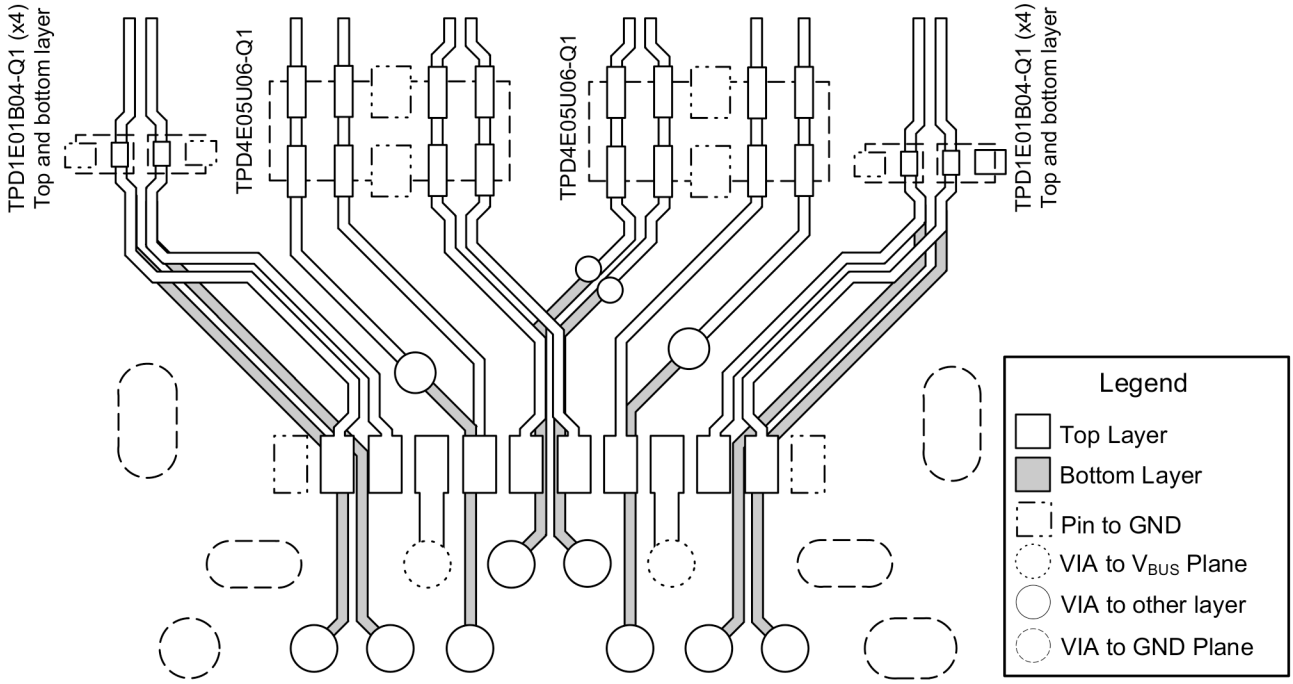


図 10-1. USB Type-C Mid-Mount, Hybrid Connector ESD Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Generic ESD Evaluation Module* user's guide

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPD1E01B04DPYRQ1	Active	Production	X1SON (DPY) | 2	10000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	LR
TPD1E01B04DPYRQ1.B	Active	Production	X1SON (DPY) | 2	10000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	LR

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TPD1E01B04-Q1 :

- Catalog : TPD1E01B04

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件 、 TI の総合的な品質ガイドライン 、 ti.com または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。 TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

最終更新日：2025 年 10 月