参考資料

TPA3221 100Wステレオ、200WモノラルHDオーディオ、アナログ入力、クラスDアンプ

1 特長

- 7V～30Vの広い電源電圧範囲での動作
- ステレオ(2×BTL)およびモノラル(1×PBTL)での動作
- 10%THD+N時の出力電力
  - BTL構成で4Ω～105W (ステレオ)
  - BTL構成で3Ω～112W (ステレオ)
  - PBTL構成で2Ω～208W (モノラル)
- 1%THD+N時の出力電力
  - BTL構成で4Ω～88W (ステレオ)
  - BTL構成で3Ω～100W (ステレオ)
  - PBTL構成で2Ω～170W (モノラル)
- 5Vのゲート・ドライブまたは内蔵されたLDOにより、オプションの単一電源動作に対応
- 閉ループ帰還設計
  - 最高100kHzの信号帯域幅によりHDソースからの高周波数のコンテンツに対応
  - THD+N: 4Ω～1Wで0.02%
  - PSRR 60dB (BTL、入力信号なし)
  - 出力ノイズ75µV未満(Aウェイト)
  - SNR 108dB超(Aウェイト)
  - ADまたはHEAD変調方式
- 低消費電力動作モード
  - スタンバイ・モード: ミュートおよび1mA未満のシャットダウン
  - 低アイドル電流HEAD変調方式
  - シングル・チャネルBTL動作
- 複数の入力オプションにより、プリアンプ設計を簡素化
  - 差動またはシングルエンド・アナログ入力
  - 選択可能なゲイン: 18dB、24dB、30dB、34dB
- 保護機能を統合: 低電圧、過電圧、サイクル単位の電流制限、短絡、クリッピング検出、過熱警告およびシャットダウン、DCスピーカ保護
- 効率90%のクラスD動作(4Ω)
- 電圧および電力レベルを選択できるピン互換デバイス・ファミリ

2 アプリケーション

- ワイヤレスおよびパワード・スピーカ
- サウンドバー
- サブウーファー
- ブックシェルフ・ステレオ・システム
- プロ用および放送設備用(PA)スピーカー

3 概要

TPA3221 はフルパワー、アイドル、およびスタンバイ状態での効率的な動作を実現するハイパワー・クラスDアンプです。最高100kHzの帯域幅による閉ループ帰還を特長としているため、音声帯域全体の歪みが小さく、優れたオーディオ品質を提供します。ADまたは低アイドル電流HEAD (高効率ADモード)変調方式で動作し、4Ω負荷へ最大2×105W、または2Ω負荷へ1×208Wの出力を駆動できます。

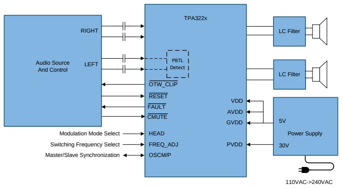
TPA3221はシングルエンドまたは差動アナログ入力インターフェイスを搭載し、最大2V_{RMS}をサポートするほか、4つのゲイン(18dB、24dB、30dB、34dB)から選択することも可能です。また、TPA3221は90%を上回る高効率を達成しており、アイドル時の消費電力が低いだけでなく(0.25W未満)、スタンバイ時の消費電力も極めて低くなっています(0.1W未満)。これは、70mΩ MOSFETと最適化されたゲート・ドライブ方式、低消費電力の動作モードを採用することで可能となりました。TPA3221にはLDOが内蔵されていることから、単一電源システムでの統合が容易です。設計をさらに簡素化するため、低電圧、過電圧、サイクル単位の電流制限、短絡、クリッピング検出、過熱警告およびシャットダウン、DCスピーカ保護といった必須の保護機能も統合されています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TPA3221	HTSSOP (44)	6.10mm×14.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

概略回路図



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4 改訂履歴

Revision A (November 2017) から **Revision B** に変更	**Page**
• Changed OUT_P To: OUT1_P for 1 x BTL in Table 1	4
• Added pins OSCM, OSCP to the Interface pins in the *Absolute Maximun Ratings* table	5
• Changed the T_J MIN value From: 0°C To –40°C in the *Absolute Maximun Ratings* table	5
• Deleted T_J Junction Temperature from the *Recommended Operating Conditions* table	5
• Changed the capacitor on IN1_P, IN2_P and IN1_M, IN2_M From: 10µF To: 1µF in 図 50	30
• Changed the capacitor on IN1_P and IN1_M From: 10µF To: 1µF in 図 51	32
• Changed the capacitor on IN1_P and IN1_M From: 10µF To: 1µF in 図 52	33

2017年9月発行のものから更新	**Page**
• 「事前情報」から「量産データ」に変更	1

5 Device Comparison Table

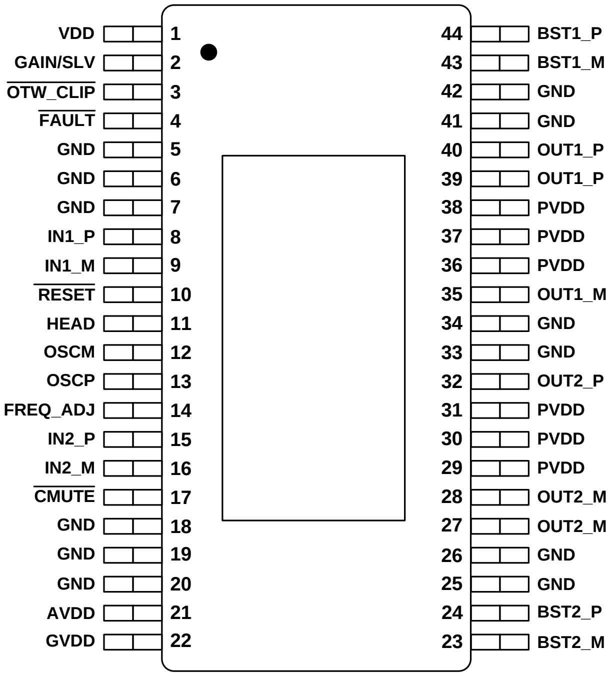
DEVICE NAME	DESCRIPTION	THERMAL PAD LOCATION	TPA3221 PIN-COMPATIBLE
TPA3220	35 W Stereo, 100 W Peak HD-Audio, Analog-Input, Class-D Amplifier	Bottom	Y
TPA3244	40 W Stereo, 100 W Peak Ultra-HD, Analog-Input Class-D Amplifier	Bottom	
TPA3245	100 W Stereo, 200 W Mono Ultra-HD, Analog-Input Class-D Amplifier	Top	
TPA3250	70 W Stereo, 130 W Peak Ultra-HD, Analog-Input Class-D Amplifier	Bottom	
TPA3251	175 W Stereo, 350 W Mono Ultra-HD, Analog-Input Class-D Amplifier	Top	
TPA3255	315 W Stereo, 600 W Mono Ultra-HD, Analog-Input Class-D Amplifier	Top	

6 Pin Configuration and Functions

The TPA3221 is available in a thermally enhanced TSSOP package.

The package type contains a heat slug that is located on the top side of the device for convenient thermal coupling to the heat sink.

DDV Package
HTSSOP 44-Pin
(Top View)



Pin Functions

NAME	NO.	I/O	DESCRIPTION
HEAD	11	I	0 = AD, 1 = HEAD. Refer to: AD-Mode and HEAD-Mode PWM Modulation
AVDD	21	P	AVDD voltage supply. Refer to: Internal LDO, AVDD and GVDD Supplies
BST1_M	43	P	OUT1_M HS bootstrap supply (BST), 0.033 µF capacitor to OUT1_M required. Refer to: BST capacitors
BST1_P	44	P	OUT1_P HS bootstrap supply (BST), 0.033 µF capacitor to OUT1_P required. Refer to: BST capacitors
BST2_M	23	P	OUT2_M HS bootstrap supply (BST), 0.033 µF capacitor to OUT2_M required. Refer to: BST capacitors
BST2_P	24	P	OUT2_P HS bootstrap supply (BST), 0.033 µF capacitor to OUT2_P required. Refer to: BST capacitors
$\overline{\text{CMUTE}}$	17	P	Mute and Startup Timing Capacitor. Connect a 33 nF capacitor to GND. Refer to: Device Reset
$\overline{\text{FAULT}}$	4	O	Shutdown signal, open drain; active low. Refer to: Error Reporting
FREQ_ADJ	14	O	Oscillator frequency programming pin. Refer to: Oscillator
GAIN/SLV	2	I	Closed loop gain and master/slave programming pin. Refer to: Input Configuration, Gain Setting And Master / Slave Operation
GND	5, 6, 7, 18, 19, 20, 25, 26, 33, 34, 41, 42	P	Ground
GVDD	22	P	Gate drive supply. Refer to: Internal LDO, AVDD and GVDD Supplies
IN1_M	9	I	Negative audio input for channel 1
IN1_P	8	I	Positive audio input for channel 1
IN2_M	16	I	Negative audio input for channel 2
IN2_P	15	I	Positive audio input for channel 2
OSCM	12	I/O	Oscillator synchronization interface. Refer to: Input Configuration, Gain Setting And Master / Slave Operation
OSCP	13	I/O	Oscillator synchronization interface. Refer to: Input Configuration, Gain Setting And Master / Slave Operation
$\overline{\text{OTW\_CLIP}}$	3	O	Clipping warning and Over-temperature warning; open drain; active low. Refer to: Error Reporting
OUT1_M	35	O	Negative output for channel 1
OUT1_P	39, 40	O	Positive output for channel 1
OUT2_M	27, 28	O	Negative output for channel 2
OUT2_P	32	O	Positive output for channel 2
PVDD	29, 30, 31, 36, 37, 38	P	PVDD supply. Refer to: PVDD Capacitor Recommendation, PVDD Supply
$\overline{\text{RESET}}$	10	I	Device reset Input; active low. Refer to: Fault Handling, Powering Up, Powering Down
VDD	1	P	Input power supply. Refer to: Internal LDO, VDD Supply
PowerPad™		P	Ground, connect to grounded heatsink. Placed on top side of device.

Table 1. Mode Selection Pins

MODE PINS(1)			INPUT MODE(2)	OUTPUT CONFIGURATION	DESCRIPTION
IN2_M	IN2_P	HEAD			
X	X	0	1N/2N + 1	2 × BTL	Stereo, BTL output configuration, AD mode modulation
X	X	1	1N/2N + 1	2 × BTL	Stereo, BTL output configuration, HEAD mode modulation
0	0	0	1N/2N + 1	1 x PBTL	Mono, Parallelled BTL configuration. Connect OUT1_P to OUT2_P and OUT1_M to OUT2_M, AD mode modulation
0	0	1	1N/2N + 1	1 x PBTL	Mono, Parallelled BTL configuration. Connect OUT1_P to OUT2_P and OUT1_M to OUT2_M, HEAD mode modulation
1	1	0	1N/2N + 1	1 x BTL	Mono, BTL configuration. OUT1_M and OUT1_P active, AD mode modulation
1	1	1	1N/2N + 1	1 x BTL	Mono, BTL configuration. OUT1_M and OUT1_P active, HEAD mode modulation

(1) X refers to inputs connected through AC coupling capacitor, 0 refers to logic low (GND), 1 refers to logic high (AVDD).
(2) 2N refers to differential input signal, 1N refers to single ended input signal. +1 refers to number of logic control ($\overline{\text{RESET}}$) input pins.

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage	PVDD to GND (2)	–0.3	37	V
	BST_X to GVDD (2)	–0.3	37	V
	BST1_M, BST1_P, BST2_M, BST2_P to GND (2)	–0.3	47.8	V
	VDD to GND	–0.3	43	V
	GVDD to GND (2)	–0.3	5.5	V
	AVDD to GND	–0.3	5.5	V
Interface pins	OUT1_M, OUT1_P, OUT2_M, OUT2_P to GND (2)	–0.3	43	V
	IN1_M, IN1_P, IN2_M, IN2_P to GND	–0.3	5.5	V
	HEAD, FREQ_ADJ, GAIN/SLV, $\overline{\text{CMUTE}}$, $\overline{\text{RESET}}$, OSCP, OSCM to GND	–0.3	5.5	V
	$\overline{\text{FAULT}}$, $\overline{\text{OTW\_CLIP}}$ to GND	–0.3	5.5	V
	Continuous sink current, $\overline{\text{FAULT}}$, $\overline{\text{OTW\_CLIP}}$ to GND		9	mA
T_J	Operating junction temperature range	–40	150	°C
T_{stg}	Storage temperature range	–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) These voltages represents the DC voltage + peak AC waveform measured at the terminal of the device in all conditions.

7.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±250	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
PVDD	Power-stage supply	DC supply voltage	7	30	32	V
VDD[1]	Supply voltage for internal LDO regulator to supply GVDD and AVDD	DC supply voltage	7		32	V
	External supply for VDD, GVDD and AVDD. Internal LDO bypassed	DC supply voltage	4.5	5	5.5	V
AVDD	Supply voltage for analog circuits	DC supply voltage	4.5	5	5.5	V
GVDD	Supply voltage for gate-drive circuitry	DC supply voltage	4.5	5	5.5	V
L_{OUT}(BTL)	Output filter inductance	Minimum output inductance at I_{OC}	5	10		µH
L_{OUT}(PBTL)	Output filter inductance, PBTL before the LC filter	Minimum output inductance at I_{OC}	5	10		
	Output filter inductance, PBTL after the LC filter	Minimum output inductance at half I_{OC} , each inductor	5	10		
F_{PWM}	PWM frame rate selectable for AM interference avoidance; 1% Resistor tolerance	Nominal	575	600	625	kHz
		AM1	510	533	555	
		AM2	460	480	500	
$R_{(FREQ\_ADJ)}$	PWM frame rate programming resistor	Nominal; Master mode	49.5	50	50.5	kΩ
		AM1; Master mode	29.7	30	30.3	
		AM2; Master mode	9.9	10	10.1	
C_{PVDD}	PVDD close decoupling capacitors			1.0		µF
$V_{(FREQ\_ADJ)}$	Voltage on FREQ_ADJ pin for slave mode operation	Slave Mode (Connect to AVDD)		5		V

(1) VDD must be connected to a supply of 5V in LDO bypass mode; OR 7V to 30V with LDO active. VDD can be connected directly to PVDD in LDO bypass mode, but must not exceed PVDD voltage.

7.4 Thermal Information

THERMAL METRIC[1]		TPA3221		UNIT
		DDV 44-PINS HTSSOP		
		JEDEC STANDARD 4 LAYER PCB	FIXED 85°C HEATSINK TEMPERATURE[2]	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	44.8	5.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.1	2.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.9	n/a	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	n/a	°C/W
ψ_{JB}	Junction-to-board characterization parameter	14.7	n/a	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

(2) Thermal data are obtained with 85°C heat sink temperature using thermal compound with 0.7W/mK thermal conductivity and 2mil thickness. In this model heat sink temperature is considered to be the ambient temperature and only path for dissipation is to the heatsink.

7.5 Electrical Characteristics

PVDD_X = 30 V, VDD = 5 V, GVDD = 5 V, T_C (Case temperature) = 75 °C, f_S = 600 kHz, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL VOLTAGE REGULATOR AND CURRENT CONSUMPTION						
AVDD	Voltage regulator. Only used as reference node when supplied by internal LDO. Voltage regulator bypassed for VDD = 5 V.	VDD = 30 V		5		V
I_{VDD}	VDD supply current. LDO mode (VDD > 7 V)	Operating, no audio signal		25		mA
		Reset mode		118		µA
	VDD supply current. LDO bypass mode (VDD = 5 V)	Operating, no audio signal		150		
		Reset mode		50		
I_{AVDD}	Gate-supply current. LDO bypass mode (VDD = 5 V)	Operating, no audio signal		10		mA
		Reset mode		1		
I_{GVDD}	Gate-supply current. LDO bypass mode (VDD = 5 V), AD-mode modulation	50% duty cycle		16		
		Reset mode		50		µA
	Gate-supply current. LDO bypass mode (VDD = 5 V), HEAD-mode modulation	HEAD-mode modulation		16		mA
		Reset mode		50		µA
I_{PVDD}	Total PVDD idle current, AD-mode modulation, BTL	50% duty cycle with recommended output filter		15		mA
		50% duty cycle with recommended output filter, T_C = 25 ºC		13		
		Reset mode, No switching		1		
	Total PVDD idle current, HEAD-mode modulation, BTL	HEAD-mode modulation with recommended output filter		10		
		HEAD-mode with recommended output filter, T_C = 25 ºC		9		
		Reset mode, No switching		1		
ANALOG INPUTS						
V_{IN}	Maximum input voltage swing				±2.8	V
I_{IN}	Maximum input current		-1		1	mA
G	Inverting voltage Gain, V_{OUT}/V_{IN}(Master Mode)	R_1 = 5.6 kΩ, R_2 = OPEN		18		dB
		R_1 = 20 kΩ, R_2 = 100 kΩ		24		
		R_1 = 39 kΩ, R_2 = 100 kΩ		30		
		R_1 = 47 kΩ, R_2 = 75 kΩ		34		
	Inverting voltage Gain, V_{OUT}/V_{IN}(Slave Mode)	R_1 = 51 kΩ, R_2 = 51 kΩ		18		
		R_1 = 75 kΩ, R_2 = 47 kΩ		24		
		R_1 = 100 kΩ, R_2 = 39 kΩ		30		
		R_1 = 100 kΩ, R_2 = 16 kΩ		34		
R_{IN}	Input resistance	G = 18 dB		48		kΩ
		G = 24 dB		24		
		G = 30 dB		12		
		G = 34 dB		7.7		
OSCILLATOR						
$f_{OSC(IO)}$ (1)	Nominal, Master Mode	F_{PWM} × 6	3.45	3.6	3.75	MHz
	AM1, Master Mode		3.06	3.198	3.33	
	AM2, Master Mode		2.76	2.88	3	
V_{IH}	High level input voltage		1.88			V
V_{IL}	Low level input voltage				1.65	V
EXTERNAL OSCILLATOR (Slave Mode)						
$f_{OSC(IO)}$	CLK input on OSCM/OSCP (Slave Mode)		2.3		3.78	MHz
OUTPUT-STAGE MOSFETs						
$R_{DS(on)}$	Drain-to-source resistance, low side (LS)	T_J = 25 °C, Excludes metallization resistance, GVDD = 5 V		70		mΩ
	Drain-to-source resistance, high side (HS)			70		mΩ

(1) Nominal, AM1 and AM2 use same internal oscillator with fixed ratio 4 : 4.5 : 5

Electrical Characteristics (continued)

PVDD_X = 30 V, VDD = 5 V, GVDD = 5 V, T_C (Case temperature) = 75 °C, f_S = 600 kHz, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I/O PROTECTION						
$V_{uvp,AVDD}$	Undervoltage protection limit, AVDD			4		V
$V_{uvp,AVDD,hyst}$ (2)	Undervoltage protection hysteresis, AVDD			0.1		V
$V_{uvp,PVDD}$	Undervoltage protection limit, PVDD_x			6.4		V
$V_{uvp,PVDD,hyst}$ (2)	Undervoltage protection hysteresis, PVDD_x			0.45		V
$V_{ovp,PVDD}$	Overvoltage protection limit, PVDD_x			34		V
$V_{ovp,PVDD,hyst}$ (2)	Overvoltage protection hysteresis, PVDD_x			0.45		V
OTW	Overtemperature warning, $\overline{\text{OTW\_CLIP}}$ (2)		115	125	135	°C
OTW_{hyst} (2)	Temperature drop needed below OTW temperature for $\overline{\text{OTW\_CLIP}}$ to be inactive after OTW event.			20		°C
OTE(2)	Overtemperature error		145	155	165	°C
OTE_{hyst} (2)	A reset needs to occur for $\overline{\text{FAULT}}$ to be released following an OTE event			20		°C
OTE-$OTW_{(differential)}$ (2)	OTE-OTW differential			25		°C
OLPC	Overload protection counter	f_{PWM} = 600 kHz (1024 PWM cycles)		1.7		ms
$I_{OC, BTL}$	Overcurrent limit protection, speaker output current	Nominal peak current in 1Ω load		10		A
$I_{OC, PBTL}$				20		A
$I_{DCspkr, BTL}$	DC Speaker Protection Current Threshold	BTL current imbalance threshold		1.8		A
$I_{DCspkr, PBTL}$		PBTL current imbalance threshold		3.6		A
I_{OCT}	Overcurrent response time	Time from switching transition to flip-state induced by overcurrent.		150		ns
I_{PD}	Output pulldown current of each half	Connected when $\overline{\text{RESET}}$ is active to provide bootstrap charge. Not used in SE mode.		3		mA
STATIC DIGITAL SPECIFICATIONS						
V_{IH}	High level input voltage	HEAD, OSCM, OSCP,$\overline{\text{CMUTE}}$, $\overline{\text{RESET}}$	1.9			V
V_{IL}	Low level input voltage				0.8	V
I_{lkg}	Input leakage current				100	μA
OTW/SHUTDOWN (FAULT)						
R_{INT_PU}	Internal pullup resistance, $\overline{\text{OTW\_CLIP}}$ to AVDD, $\overline{\text{FAULT}}$ to AVDD		20	26	32	kΩ
V_{OH}	High level output voltage	Internal pullup resistor	3	3.3	3.6	V
V_{OL}	Low level output voltage	I_O = 4 mA		200	500	mV
Device fanout	$\overline{\text{OTW\_CLIP}}$, $\overline{\text{FAULT}}$	No external pullup		30		devices

(2) Specified by design.

7.6 Audio Characteristics (BTL)

PCB and system configuration are in accordance with recommended guidelines. Audio frequency = 1 kHz, PVDD_X = 30 V, VDD = 5 V, GVDD = 5 V, R_L = 4 Ω, f_S = 600 kHz, T_C = 75°C, Output Filter: L_{DEM} = 10 µH, C_{DEM} = 1 µF, AD-Modulation, AES17 + AUX-0025 measurement filters, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Power output per channel	R_L = 3 Ω, 10% THD+N		112		W
		R_L = 4 Ω, 10% THD+N		105		
		R_L = 3 Ω, 1% THD+N		100		
		R_L = 4 Ω, 1% THD+N		88		
THD+N	Total harmonic distortion + noise	1 W		0.02		%
V_n	Output integrated noise	A-weighted, AES17 filter, Input Capacitor Grounded, Gain = 18 dB		75		µV
$\|V_{OS}\|$	Output offset voltage	Inputs AC coupled to GND		20	60	mV
SNR	Signal-to-noise ratio(1)	A-weighted, Gain = 18 dB		108		dB
DNR	Dynamic range	A-weighted, Gain = 18 dB		109		dB
P_{idle}	Power dissipation due to idle losses (I_{PVDD_X})	P_O = 0, all outputs switching, AD-modulation, T_C = 25°C(2)		0.37		W
		P_O = 0, all outputs switching, HEAD-modulation, T_C = 25°C(2)		0.25		W

(1) SNR is calculated relative to 1% THD+N output level.
(2) Actual system idle losses also are affected by core losses of output inductors.

7.7 Audio Characteristics (PBTL)

PCB and system configuration are in accordance with recommended guidelines. Audio frequency = 1 kHz, PVDD_X = 30 V, VDD = 5 V, GVDD = 5 V, R_L = 2 Ω, f_S = 600 kHz, T_C = 75°C, Output Filter: L_{DEM} = 10 µH, C_{DEM} = 1 µF, Pre-Filter PBTL, AD-Modulation, AES17 + AUX-0025 measurement filters, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Power output per channel	R_L = 2 Ω, 10% THD+N		208		W
		R_L = 3 Ω, 10% THD+N		155		
		R_L = 4 Ω, 10% THD+N		120		
		R_L = 2 Ω, 1% THD+N		170		
		R_L = 3 Ω, 1% THD+N		125		
		R_L = 4 Ω, 1% THD+N		98		
THD+N	Total harmonic distortion + noise	1 W		0.02		%
V_n	Output integrated noise	A-weighted, AES17 filter, Input Capacitor Grounded, Gain = 18 dB		75		µV
$\|V_{OS}\|$	Output offset voltage	Inputs AC coupled to GND		20	60	mV
SNR	Signal to noise ratio(1)	A-weighted, Gain = 18 dB		108		dB
DNR	Dynamic range	A-weighted, Gain = 18 dB		110		dB
P_{idle}	Power dissipation due to idle losses (IPVDD_X)	P_O = 0, all outputs switching, AD-modulation, T_C = 25°C(2)		0.20		W
		P_O = 0, all outputs switching, HEAD-modulation, T_C = 25°C(2)		0.17		W

(1) SNR is calculated relative to 1% THD+N output level.
(2) Actual system idle losses are affected by core losses of output inductors.

7.8 Typical Characteristics, BTL Configuration, AD-mode

All Measurements taken at audio frequency = 1 kHz, PVDD_X = 30 V, VDD = 5 V, GVDD = 5 V, R_L = 4 Ω, f_S = 600 kHz, 18 dB, T_C = 75°C, Output Filter: L_{DEM} = 10 µH, C_{DEM} = 1 µF, AD-Modulation, AES17 + AUX-0025 measurement filters, unless otherwise noted.

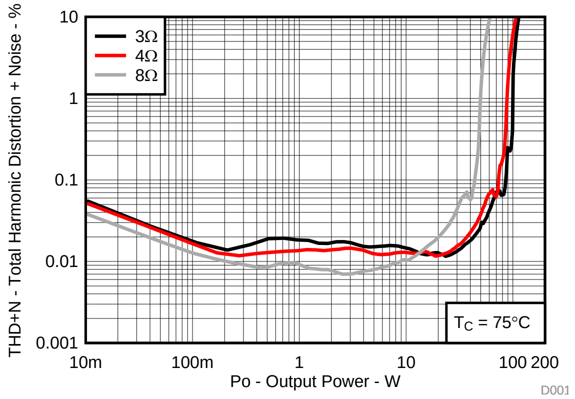


Figure 1. Total Harmonic Distortion + Noise vs Output Power, AD-mode

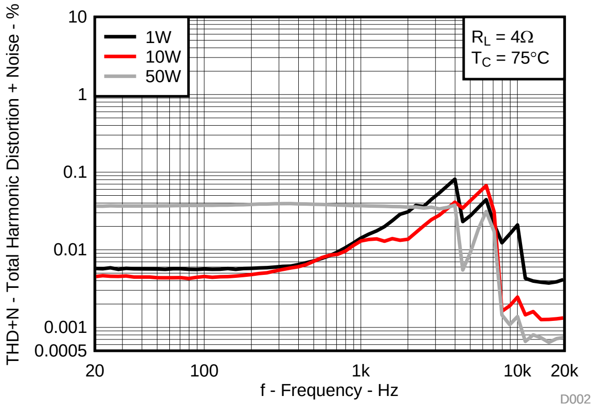


Figure 2. Total Harmonic Distortion+Noise vs Frequency, AD-mode

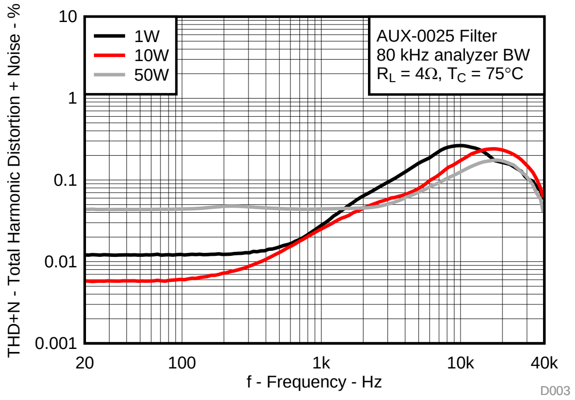


Figure 3. Total Harmonic Distortion+Noise vs Frequency, AD-mode

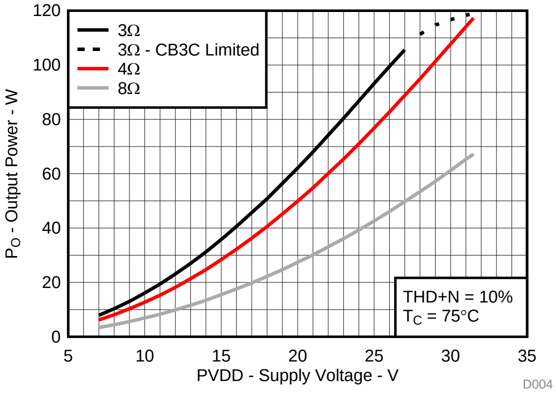


Figure 4. Output Power vs Supply Voltage, AD-mode

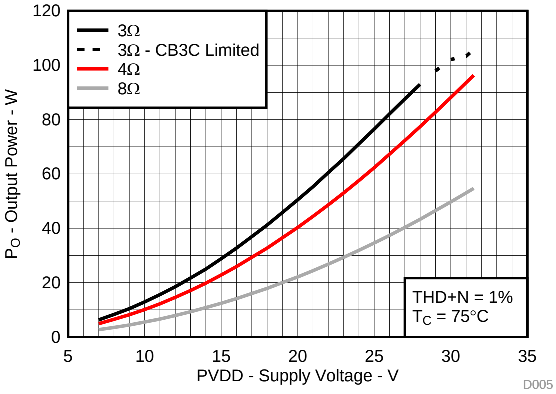


Figure 5. Output Power vs Supply Voltage, AD-mode

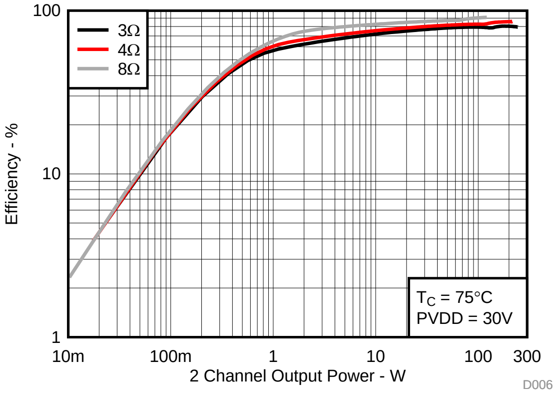


Figure 6. System Efficiency vs Output Power, AD-mode

Typical Characteristics, BTL Configuration, AD-mode (continued)

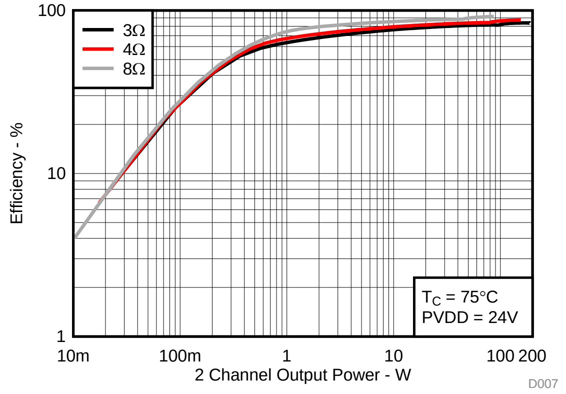


Figure 7. System Efficiency vs Output Power, AD-mode

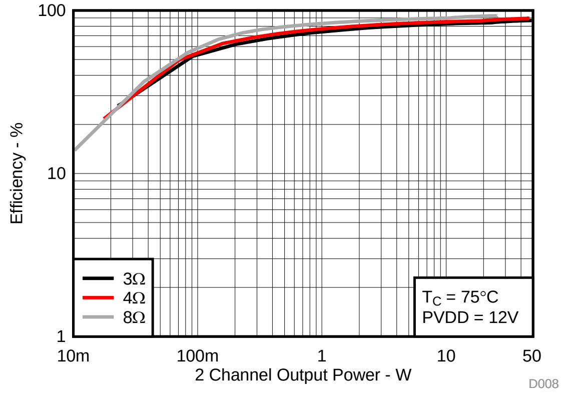


Figure 8. System Efficiency vs Output Power, AD-mode

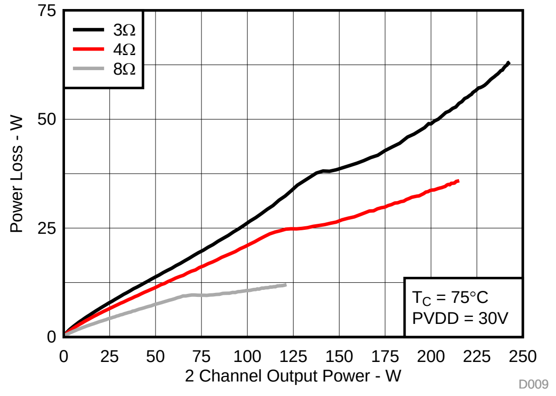


Figure 9. System Power Loss vs Output Power, AD-mode

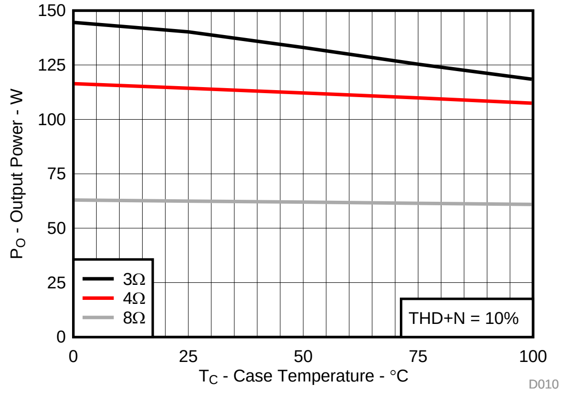


Figure 10. Output Power vs Case Temperature, AD-mode

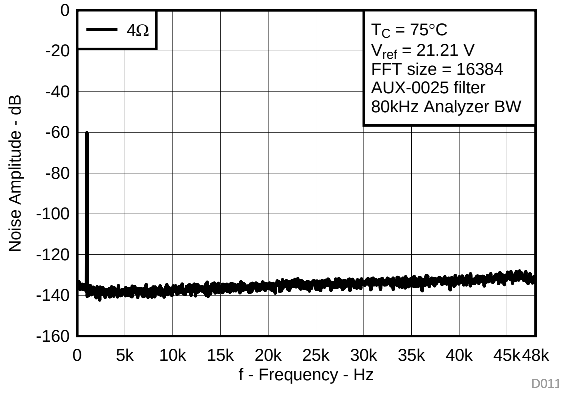


Figure 11. Noise Amplitude vs Frequency, AD-mode

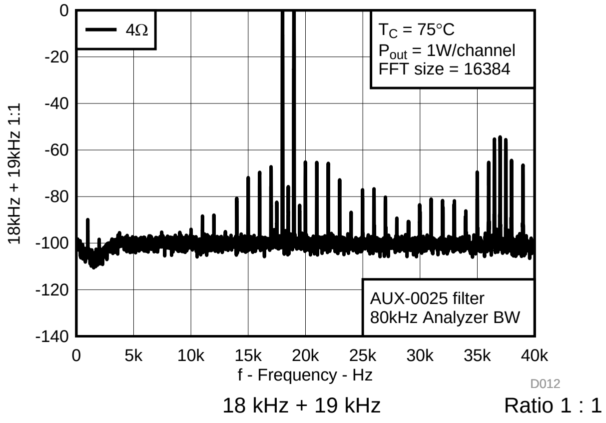


Figure 12. CCIF Intermodulation, AD-mode

Typical Characteristics, BTL Configuration, AD-mode (continued)

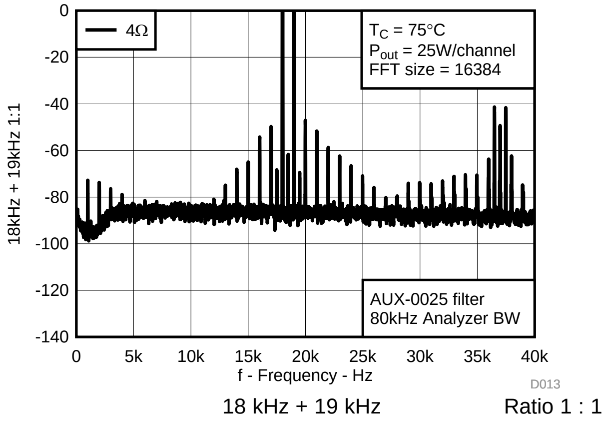


Figure 13. CCIF Intermodulation, AD-mode

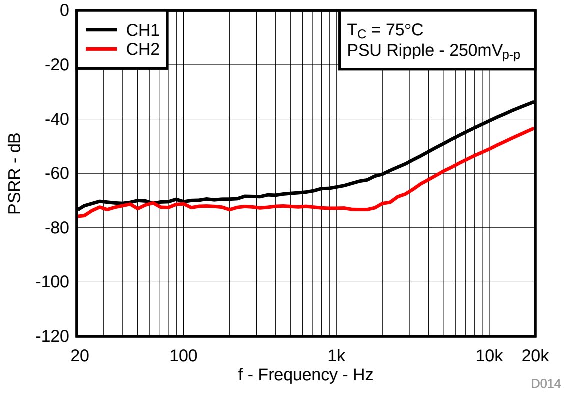


Figure 14. Power Supply Rejection Ratio vs Frequency, AD-mode

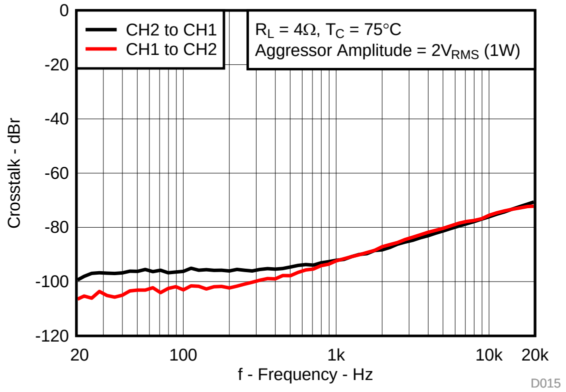


Figure 15. Channel to Channel Crosstalk vs Frequency, AD-mode

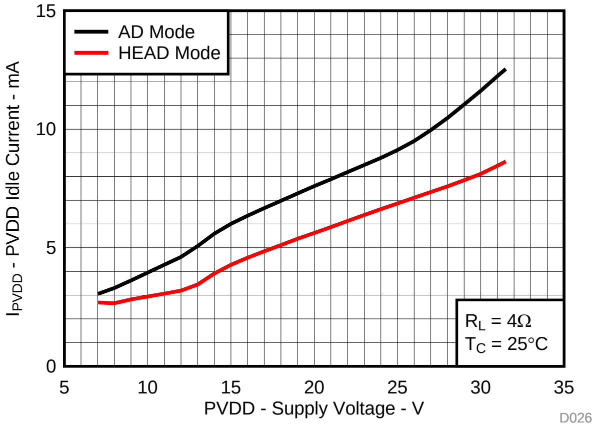


Figure 16. Idle Current vs Supply Voltage

7.9 Typical Characteristics, PBTL Configuration, AD-mode

All Measurements taken at audio frequency = 1 kHz, PVDD_X = 30 V, VDD = 5 V, GVDD = 5 V, R_L = 2 Ω, f_S = 600 kHz, 18 dB, T_C = 75°C, Output Filter: L_{DEM} = 10 µH, C_{DEM} = 1 µF, Pre-Filter PBTL, AD Modulation, AES17 + AUX-0025 measurement filters, unless otherwise noted.

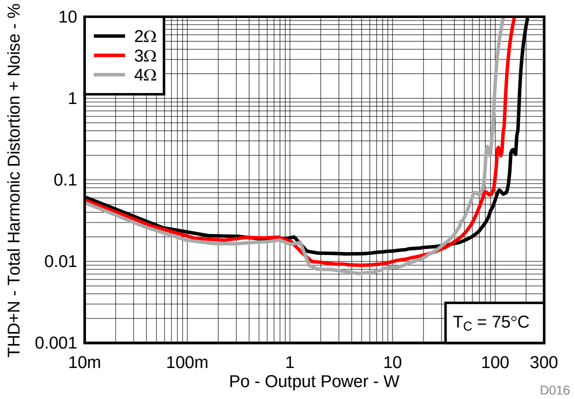


Figure 17. Total Harmonic Distortion+Noise vs Output Power, AD-mode

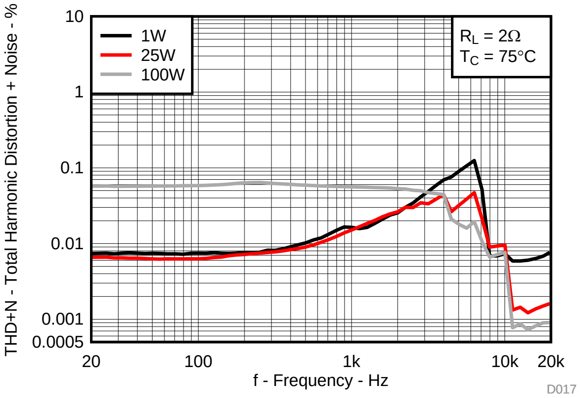


Figure 18. Total Harmonic Distortion + Noise vs Frequency, AD-mode

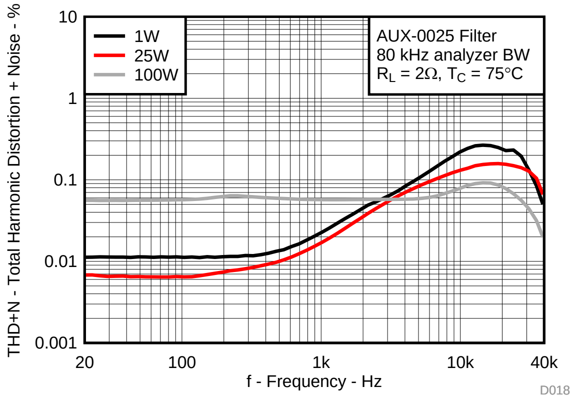


Figure 19. Total Harmonic Distortion+Noise vs Frequency, AD-mode

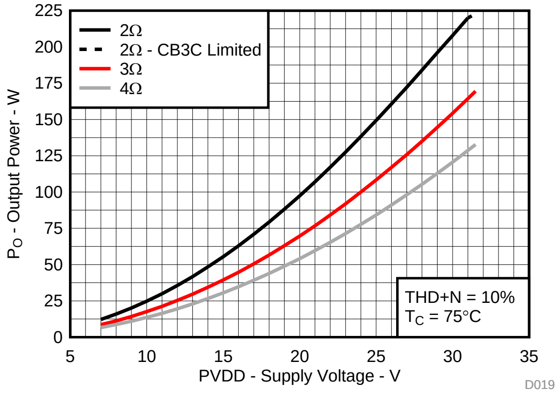


Figure 20. Output Power vs Supply Voltage, AD-mode

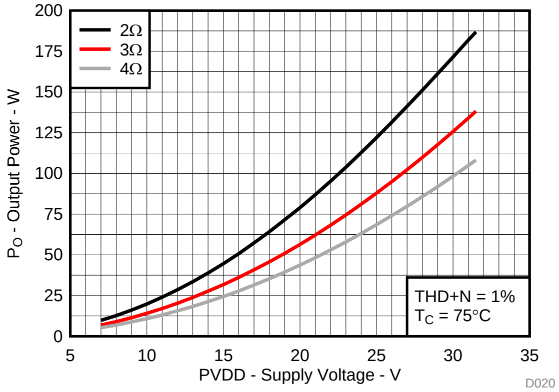


Figure 21. Output Power vs Supply Voltage, AD-mode

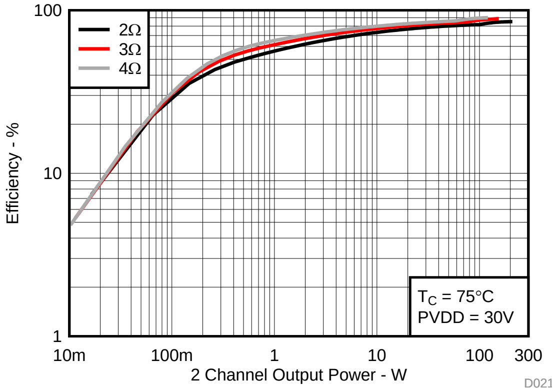


Figure 22. System Efficiency vs Output Power, AD-mode

Typical Characteristics, PBTL Configuration, AD-mode (continued)

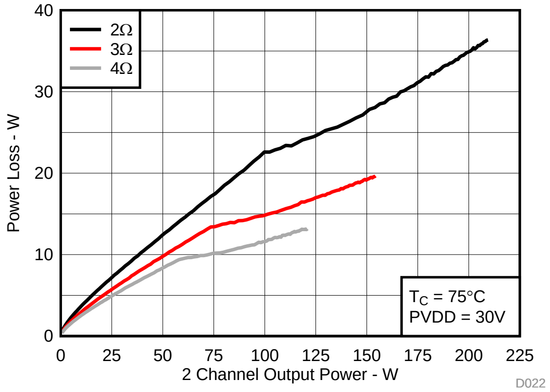


Figure 23. System Power Loss vs Output Power, AD-mode

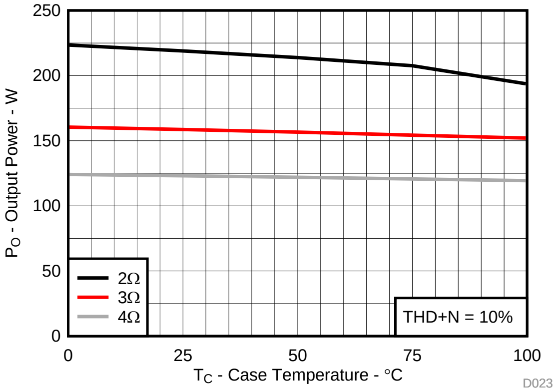
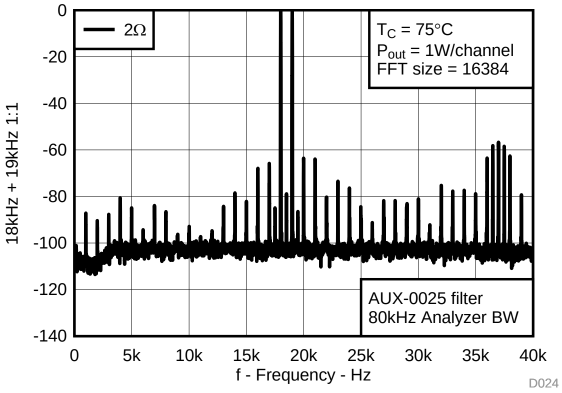
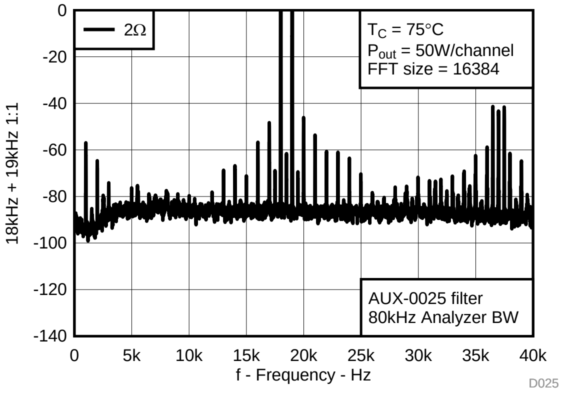


Figure 24. Output Power vs Case Temperature, AD-mode



18 kHz + 19 kHz Ratio 1 : 1

Figure 25. CCIF Intermodulation vs Frequency, AD-mode



18 kHz + 19 kHz Ratio 1 : 1

Figure 26. CCIF Intermodulation vs Frequency, AD-mode

8 Parameter Measurement Information

All parameters are measured according to the conditions described in the *Recommended Operating Conditions*.

Most audio analyzers will not give correct readings of Class-D amplifiers' performance due to their sensitivity to out of band noise present at the amplifier output. AES-17 + AUX-0025 pre-analyzer filters are recommended to use for Class-D amplifier measurements. In absence of such filters, a 30-kHz low-pass filter (10 Ω + 47 nF) can be used to reduce the out of band noise remaining on the amplifier outputs.

9 Detailed Description

9.1 Overview

TPA3221 is designed as a feature-enhanced cost efficient high power Class-D audio amplifier. It has built-in advanced protection circuitry to ensure maximum product robustness as well as a flexible feature set including built in LDO for easy supply of low voltage circuitry, selectable gain, switching frequency, master/slave synchronization of multiple devices, selectable PWM modulation scheme, mute function, temperature and clipping status signals. TPA3221 has a bandwidth up to 100 kHz and low output noise designed for high resolution audio applications and accepts both differential and single ended analog audio inputs at levels from 1 V_{RMS} to 2 V_{RMS}. With its closed loop operation TPA3221 is designed for high audio performance with a system power supply between 7 V and 30 V.

To facilitate system design, the TPA3221 needs only a (typical) 30 V power stage supply. The TPA3221 has an internal voltage regulator supplied from the VDD pin for the analog and digital system blocks and the output stage gate drive respectively. The VDD pin can be connected directly to PVDD in case of only this power supply rail available.

To reduce device power losses external 5 V supplies can be used for the AVDD and VDD supply pins. The internal voltage regulator connected to the VDD pin is automatically turned off if using external 5 V supply for this pin. Although supplied from the same 5 V source, separating AVDD and VDD on the printed-circuit board (PCB) by RC filters (see application diagram for details) is recommended. These RC filters provide the recommended high-frequency isolation. Special attention should be paid to placing all decoupling capacitors as close to their associated pins as possible. In general, the physical loop with the power supply pins, decoupling capacitors and GND return path to the device pins must be kept as short as possible and with as little area as possible to minimize induction (see *Layout Examples* for additional information).

The floating supplies for the output stage high side gate drives are supplied by built-in bootstrap circuitry requiring only an external capacitor for each half-bridge.

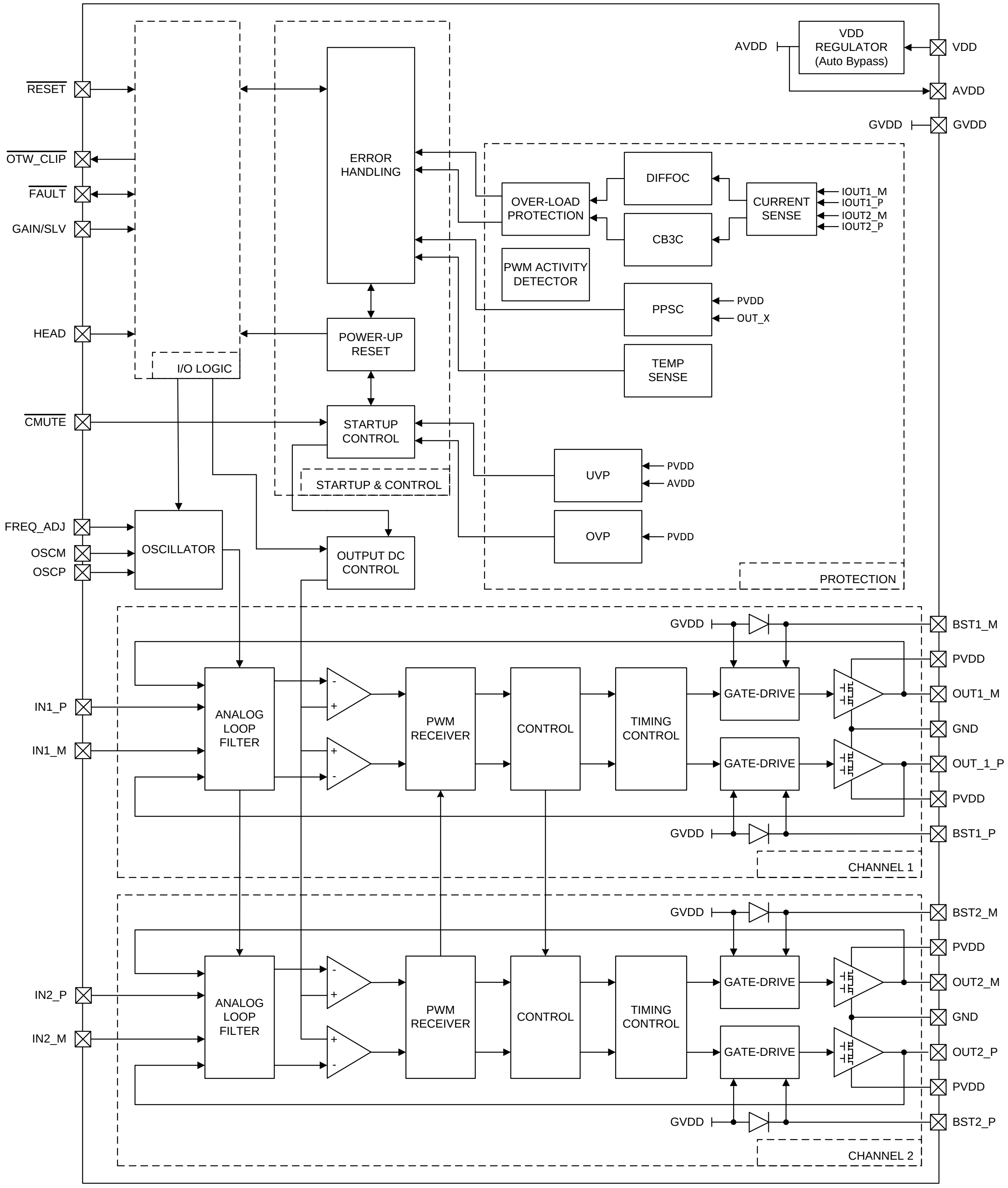
For a properly functioning bootstrap circuit, a small ceramic capacitor must be connected from each bootstrap pin (BST_X) to the power-stage output pin (OUT_X). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive power-supply pin (GVDD) and the bootstrap pins. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides a suitable voltage supply for the high-side gate driver. It is recommended to use 33 nF ceramic capacitors, size 0603 or 0805, for the bootstrap supply. These 33 nF capacitors ensure sufficient energy storage, even during minimal PWM duty cycles, to keep the high-side power stage FET (LDMOS) fully turned on during the remaining part of the PWM cycle.

Special attention should be paid to the power stage power supply; this includes component selection, PCB placement, and routing.

For optimal electrical performance, EMI compliance, and system reliability, it is important that each PVDD_X node is decoupled with 1 μF ceramic capacitors placed as close as possible to the PVDD supply pins. It is recommended to follow the PCB layout of the TPA3221 reference design. For additional information on recommended power supply and required components, see the application diagrams in this data sheet.

If using external power supply for the AVDD and VDD internal regulators, this supply should be from a low-noise, low-output-impedance voltage regulator. Likewise, the 30 V power stage supply is assumed to have low output impedance throughout the entire audio band, and low noise. The power supply sequence is not critical as facilitated by the internal power-on-reset circuit, but it is recommended to release $\overline{\text{RESET}}$ after the power supply is settled for minimum turn on audible artefacts. Moreover, the TPA3221 is fully protected against erroneous power-stage turn on due to parasitic gate charging. Thus, voltage-supply ramp rates (dV/dt) are noncritical within the specified range (see the *Recommended Operating Conditions* table of this data sheet).

9.2 Functional Block Diagrams



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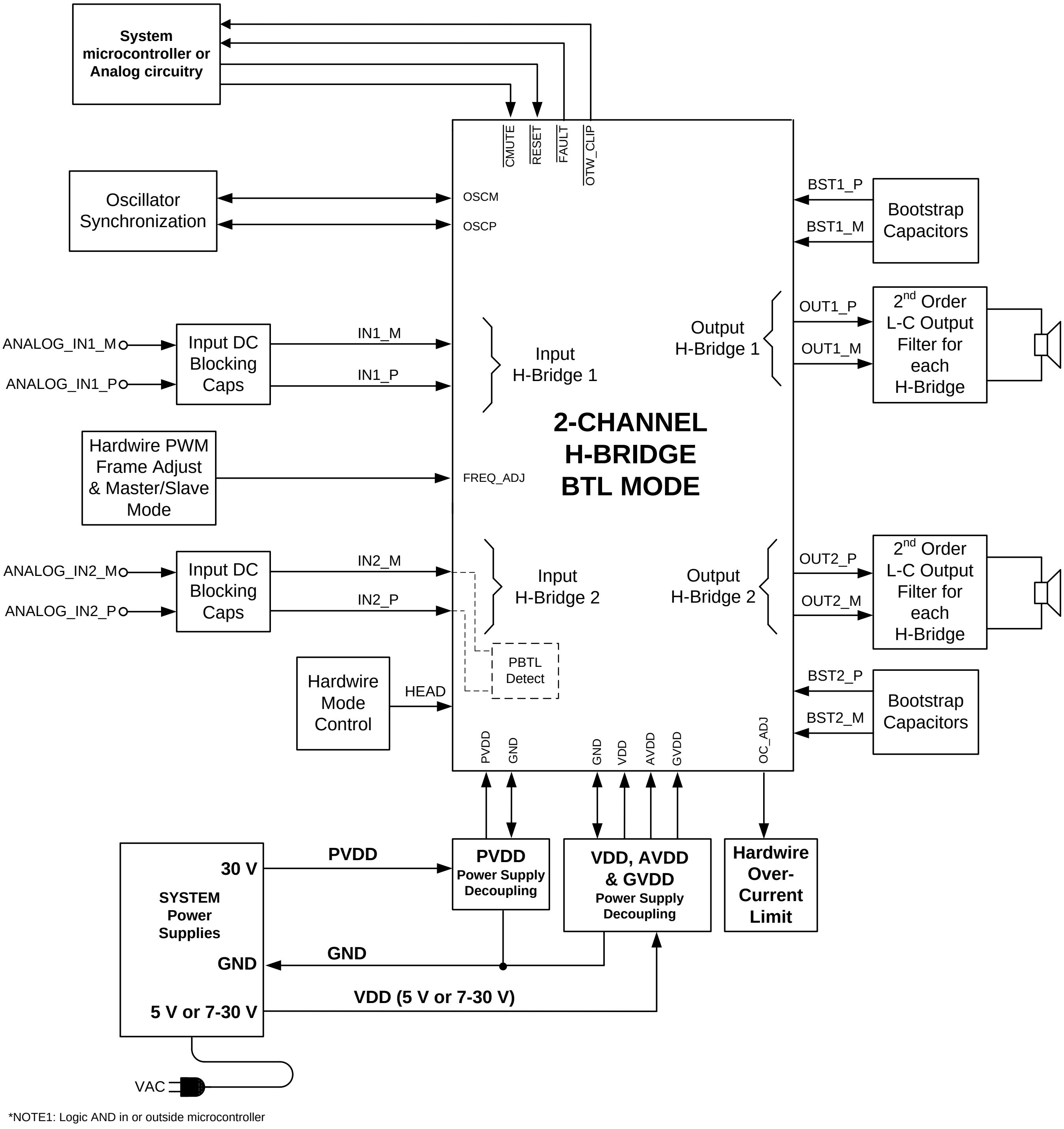
Functional Block Diagrams (continued)



*NOTE1: Logic AND in or outside microcontroller

図 27. System Block Diagram

9.3 Feature Description

9.3.1 Internal LDO

TPA3221 has a built in optional LDO (Low dropout voltage regulator) to supply the analog and digital circuits as well as the gate drive for the output stages. The LDO can be used in systems where only the high voltage power rail is available, hence no additional power supply rails need to be generated for the TPA3221 to operate. As being a linear regulator, the LDO will add to the power losses of the device due to the (PVDD-5V) voltage drop and the supply current for AVDD and GVDD given in the *Electrical Characteristics* table.

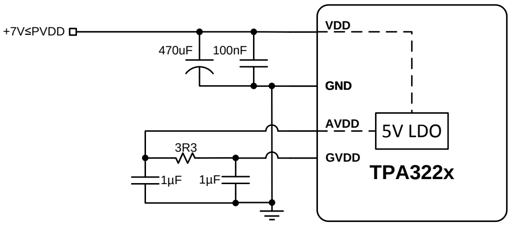


図 28. Internal LDO for Single Supply Systems

When using the internal LDO in TPA3221 the VDD terminal should be connected to a voltage source between 7V and PVDD. In a single supply system the VDD terminal should be connected directly to the PVDD terminal. The LDO output is connected to the AVDD terminal, and can be used to supply the gate drive by supplying the GVDD from AVDD through a RC filter for best noise performance as shown in 図 28.

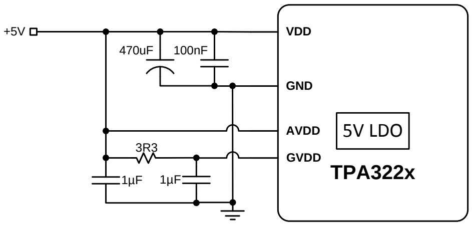


図 29. Internal LDO Bypass for Highest Power Efficiency

For highest system power efficiency the LDO can be bypassed by connecting VDD to an external 5 V supply. In this configuration AVDD and GVDD should be supplied by 5 V from the external power supply. GVDD should be supplied through a RC filter for best noise performance as shown in 図 29.

9.3.1.1 Input Configuration, Gain Setting And Master / Slave Operation

TPA3221 is designed to accept either a differential or a single-ended audio input signal. To accept a wide range of system front ends TPA3221 has selectable input gain that allows full scale output with a wide range of input signal levels.

Best system noise performance is obtained with balanced audio interface. However, to be used in systems with only a single ended audio input signal available, one input terminal can be connected to AC ground, to accept single ended audio input signals.

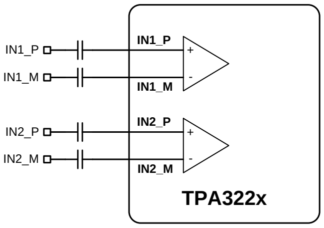


図 30. Balanced Audio Input Configuration

Feature Description (continued)

In systems with single ended audio inputs the device gain will typically need to be set higher than for systems with balanced audio input signals.

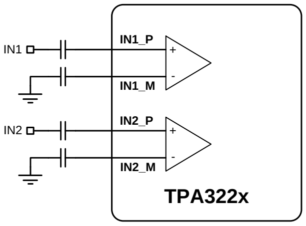


図 31. Single Ended Audio Input Configuration

9.3.2 Gain Setting And Master / Slave Operation

The gain of TPA3221 is set by the voltage divider connected to the GAIN/SLV control pin. Master or Slave mode is also controlled by the same pin. An internal ADC is used to detect the 8 input states. The first four stages sets the GAIN in Master mode in gains of 18, 24, 30, 34 dB respectively, while the next four stages sets the GAIN in Slave mode in gains of 18, 24, 30, 34 dB respectively. The gain setting is latched when $\overline{\text{RESET}}$ goes high and cannot be changed while $\overline{\text{RESET}}$ is high. 表 2 shows the recommended resistor values, the state and gain:

表 2. Gain and Master / Slave

Master / Slave Mode	Gain	R1 (to GND)	R2 (to AVDD)	Differential Input Signal Level (each input pin)	Single Ended Input Signal Level
Master	18 dB	5.6 kΩ	OPEN	2 VRMS	2 VRMS
Master	24 dB	20 kΩ	100 kΩ	1 VRMS	2 VRMS
Master	30 dB	39 kΩ	100 kΩ	0.5 VRMS	1 VRMS
Master	34 dB	47 kΩ	75 kΩ	0.32 VRMS	0.63 VRMS
Slave	18 dB	51 kΩ	51 kΩ	2 VRMS	2 VRMS
Slave	24 dB	75 kΩ	47 kΩ	1 VRMS	2 VRMS
Slave	30 dB	100 kΩ	39 kΩ	0.5 VRMS	1 VRMS
Slave	34 dB	100 kΩ	16 kΩ	0.32 VRMS	0.63 VRMS

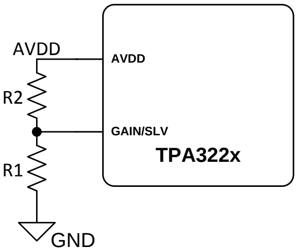


図 32. Gain and Master / Slave Setup

For easy multi-channel system design TPA3221 has a Master / Slave feature that allows automatic synchronization of multiple slave devices operated at the PWM switching frequency of a master device. This benefits system noise performance by eliminating spurious crosstalk sum and difference tones due to unsynchronized channel-to-channel switching frequencies. Furthermore the Master / Slave scheme is designed to interleave switching of the individual channels in a multi-channel system such that the power supply current ripple frequency is moved to a higher frequency which reduces the RMS ripple current in the power supply bulk capacitors.

The Master / Slave scheme and the interleaving of the output stage switching is automatically configured by connecting the OSCx pins between a master and multiple slave devices. Connect the OSCx pins in either positive or negative polarity to configure either a Slave1 or Slave2 device. Connect the OSCM of the Master device to the OSCM of a slave device to configure for Slave1 or OSCP to configure for Slave2. Then connect the remaining OSCx pins between the master and slave devices. The Master, Slave1 and Slave2 PWM switching will be 30 degrees out of phase with each other. All switching channels are automatically synchronized by releasing /RESET on all devices at the same time.

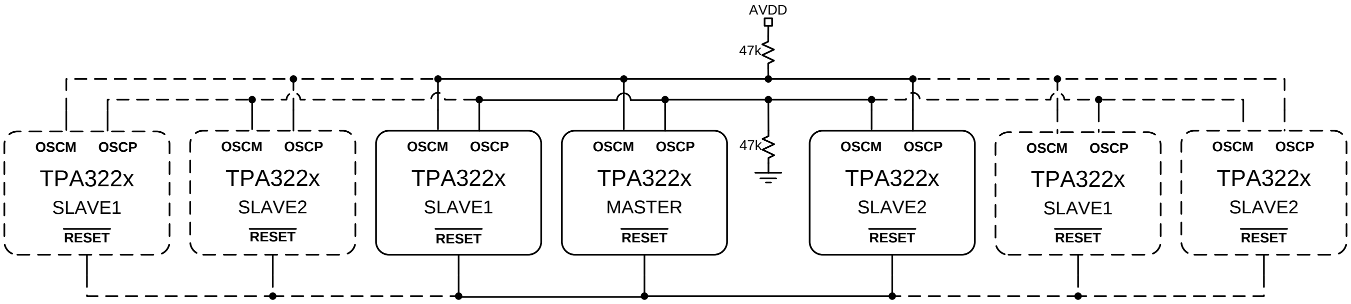


図 33. Gain and Master PCB Implementation

Placement on the PCB and connection of multiple TPA3221 devices in a multi channel system is illustrated in 図 33. Slave devices should be placed on either side of the master device, with a Slave1 device on one side of the Master device, and a Slave2 device on the other. In systems with more than 3 TPA3221 devices, the master should be in the middle, and every second slave devices should be a Slave1 or Slave 2 as illustrated in 図 33. A 47kΩ pull up resistor to AVDD should be connected to the master device OSCM output and a 47kΩ pull down resistor to GND should be connected to the master OSCP CLK outputs.

9.3.3 AD-Mode and HEAD-Mode PWM Modulation

TPA3221 has the option of using either AD-Mode or HEAD-Mode PWM modulation scheme. AD mode has continuous switching of the two half bridge outputs in each BTL output channel. Both half bridge outputs are switching in HEAD mode, but with reduced duty cycle for idle operation and while playing small signals. With higher output levels one half bridge stops switching on HEAD mode operation. HEAD benefits both device power loss and EMI performance, where AD mode is considered to have the highest audio performance.

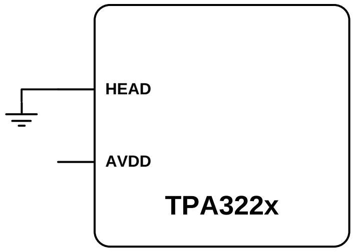


図 34. AD-Mode Configuration

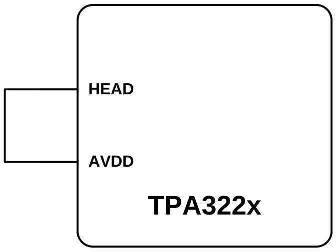


図 35. HEAD-Mode Configuration

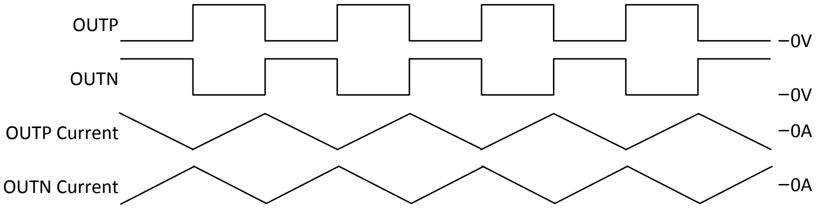


図 36. AD Mode Output Waveforms, Idle

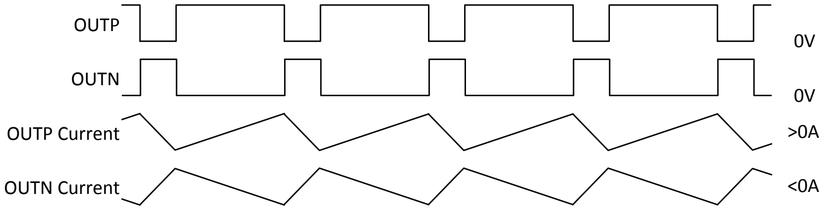


図 37. AD Mode Output Waveforms, High Level Output

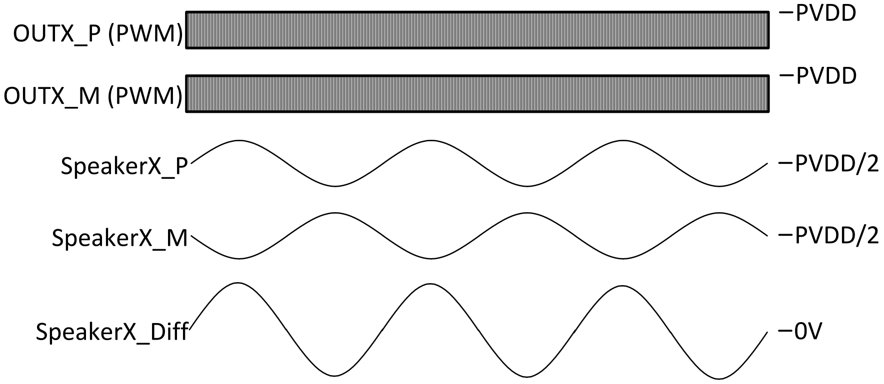


図 38. AD Mode Speaker Output Signals, Low or and High Level Output

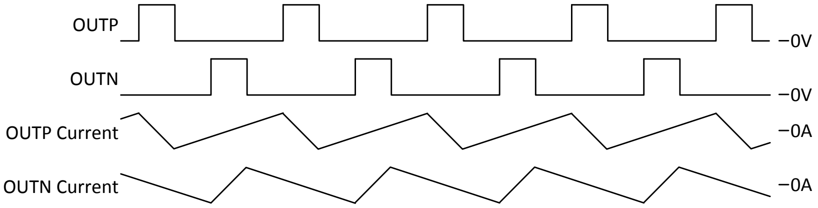


図 39. HEAD Mode Output Waveforms, Idle

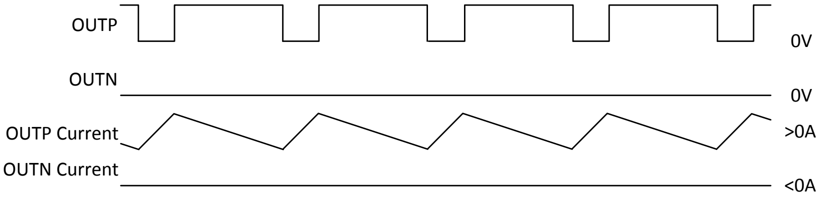


図 40. HEAD Mode Output Waveforms, High Level Output

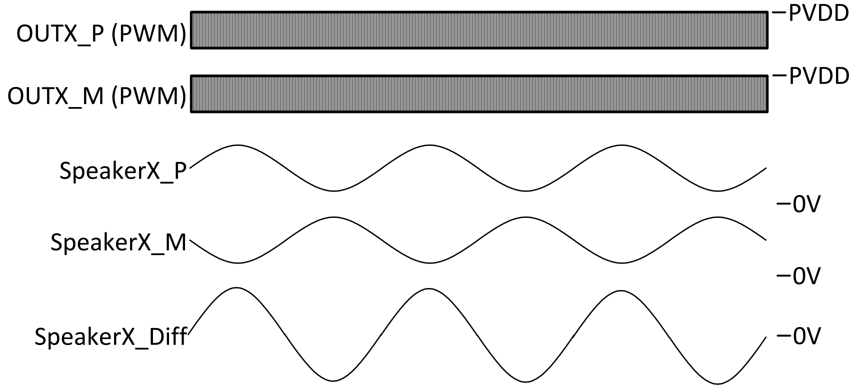


図 41. HEAD Mode Speaker Output Signals, Low Level Output

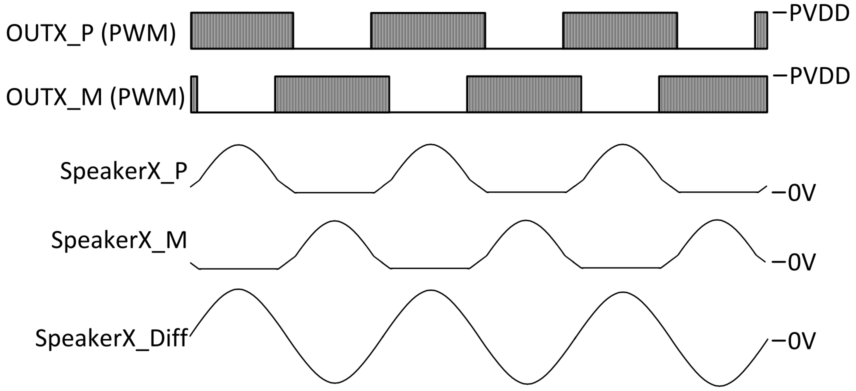


図 42. HEAD Mode Speaker Output Signals, High Level Output

9.3.4 Oscillator

The oscillator frequency can be trimmed by external control of the FREQ_ADJ pin.

To reduce interference problems while using radio receiver tuned within the AM band, the switching frequency can be changed from nominal to higher values. These values should be chosen such that the nominal and the higher value switching frequencies together results in the fewest cases of interference throughout the AM band. The oscillator frequency can be selected by the value of the FREQ_ADJ resistor connected to GND in master mode according to the description in the *Recommended Operating Conditions* table.

For slave mode operation, turn off the oscillator by pulling the FREQ_ADJ pin to AVDD. This configures the OSC_I/O pins as inputs to be slaved from an external differential clock. In a master/slave system inter channel delay is automatically setup between the switching of the audio channels, which can be illustrated by no idle channels switching at the same time. This will not influence the audio output, but only the switch timing to minimize noise coupling between audio channels through the power supply to optimize audio performance and to get better operating conditions for the power supply. The inter channel delay will be setup for a slave device depending on the polarity of the OSC_I/O connection such that a slave mode 1 is selected by connecting the master device OSC_I/O to the slave 1 device OSC_I/O with same polarity (+ to + and - to -), and slave mode 2 is selected with the inverse polarity (+ to - and - to +).

9.3.5 Input Impedance

The TPA3221 input stage is a fully differential input stage and the input impedance changes with the gain setting from 7.7 kΩ at 34 dB gain to 47 kΩ at 18 dB gain. Table 1 lists the values from min to max gain. The tolerance of the input resistor value is ±20 % so the minimum value will be higher than 6.2 kΩ. The inputs need to be AC-coupled to minimize the output DC-offset and ensure correct ramping of the output voltages during power-ON and power-OFF. The input ac-coupling capacitor together with the input impedance forms a high-pass filter with the following cut-off frequency:

If a flat bass response is required down to 20 Hz the recommended cut-off frequency is a tenth of that, 2 Hz. 表 3 lists the recommended ac-couplings capacitors for each gain step. If a -3 dB is accepted at 20 Hz 10 times lower capacitors can used – for example, a 1 µF can be used.

表 3. Recommended Input AC-Coupling Capacitors

Gain	Input Impedance	Input AC-Coupling Capacitance	Input High Pass Filter
18 dB	48 kΩ	4.7 µF	0.7 Hz
24 dB	24 kΩ	10 µF	0.7 Hz
30 dB	12 kΩ	10 µF	1.3 Hz
34 dB	7.7 kΩ	10 µF	2.1 Hz

The input capacitors used should be a type with low leakage, like quality electrolytic, tantalum, film or ceramic. If a polarized type is used the positive connection should face such that the capacitor has a positive DC bias.

9.3.6 Error Reporting

The $\overline{\text{FAULT}}$, and $\overline{\text{OTW\_CLIP}}$, pins are active-low, open-drain outputs. The $\overline{\text{FAULT}}$ function is for protection-mode signaling to a system-control device. Any fault resulting in device shutdown is signaled by the $\overline{\text{FAULT}}$ pin going low. Also, $\overline{\text{OTW\_CLIP}}$ goes low when the device junction temperature exceeds 125°C (see 表 4).

表 4. Error Reporting

$\overline{\text{FAULT}}$	$\overline{\text{OTW\_CLIP}}$	DESCRIPTION
0	0	Overtemperature (OTE), overload (OLP), undervoltage (UVP), or overvoltage (OVP). Junction temperature higher than 125°C (overtemperature warning)
0	1	Overload (OLP), undervoltage (UVP), or overvoltage (OVP). Junction temperature lower than 125°C
1	0	Junction temperature higher than 125°C (overtemperature warning)
1	1	Junction temperature lower than 125°C and no OLP or UVP faults (normal operation)

Note that asserting $\overline{\text{RESET}}$ low forces the $\overline{\text{FAULT}}$ signal high, independent of faults being present. TI recommends monitoring the $\overline{\text{OTW\_CLIP}}$ signal using the system microcontroller and responding to an overtemperature warning signal by turning down the volume to prevent further heating of the device resulting in device shutdown (OTE).

To reduce external component count, an internal pullup resistor to 3.3 V is provided on both $\overline{\text{FAULT}}$ and $\overline{\text{OTW\_CLIP}}$ outputs.

9.4 Device Functional Modes

TPA3221 can be configured in either a stereo BTL (Bridge Tied Load) mode, mono BTL mode (only one output BTL channel active), or in a mono PBTL (Parallel Bridge Tied Load) mode. In PBTL mode the two output BTL channels are parallelled with double output current available. The parallelling of the two BTL outputs can be made either before the output LC filter, or after the output LC filter. For PBTL mode the audio performance will in general be higher when parallelling before the output LC filter, but parallelling after the LC output filter may be preferred in some systems.

See Table 1 for mode configuration setup.

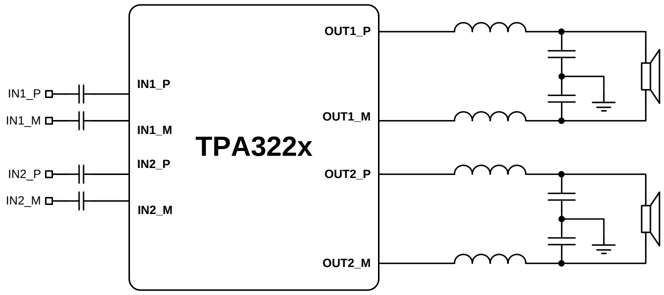


図 43. Stereo BTL

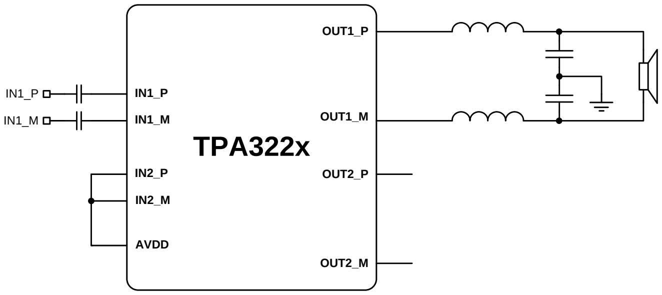


図 44. Mono BTL

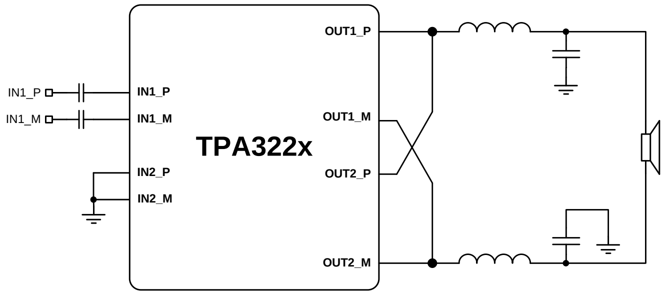


図 45. Mono PBTL, Pre LC Filter

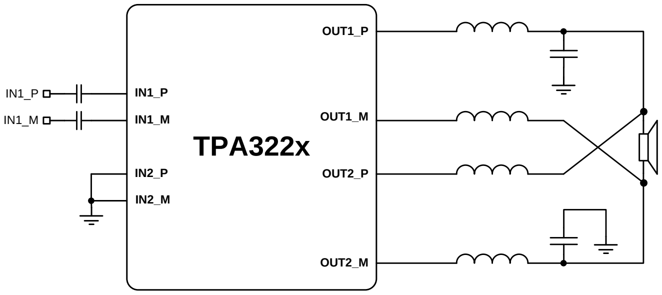


図 46. Mono PBTL, Post LC Filter

9.4.1 Powering Up

The TPA3221 does not require a power-up sequence because of the integrated undervoltage protection (UVP), but it is recommended to hold $\overline{\text{RESET}}$ low until PVDD supply voltage is stable to avoid audio artifacts. The outputs of the H-bridges remain in a high-impedance state until the gate-drive supply (GVDD) and AVDD voltages are above their UVP voltage thresholds (see the *Electrical Characteristics* table of this data sheet). This allows an internal circuit to charge the external bootstrap capacitors by enabling a weak pull-down of the half-bridge output as well as initiating a controlled ramp up sequence of the output voltage.

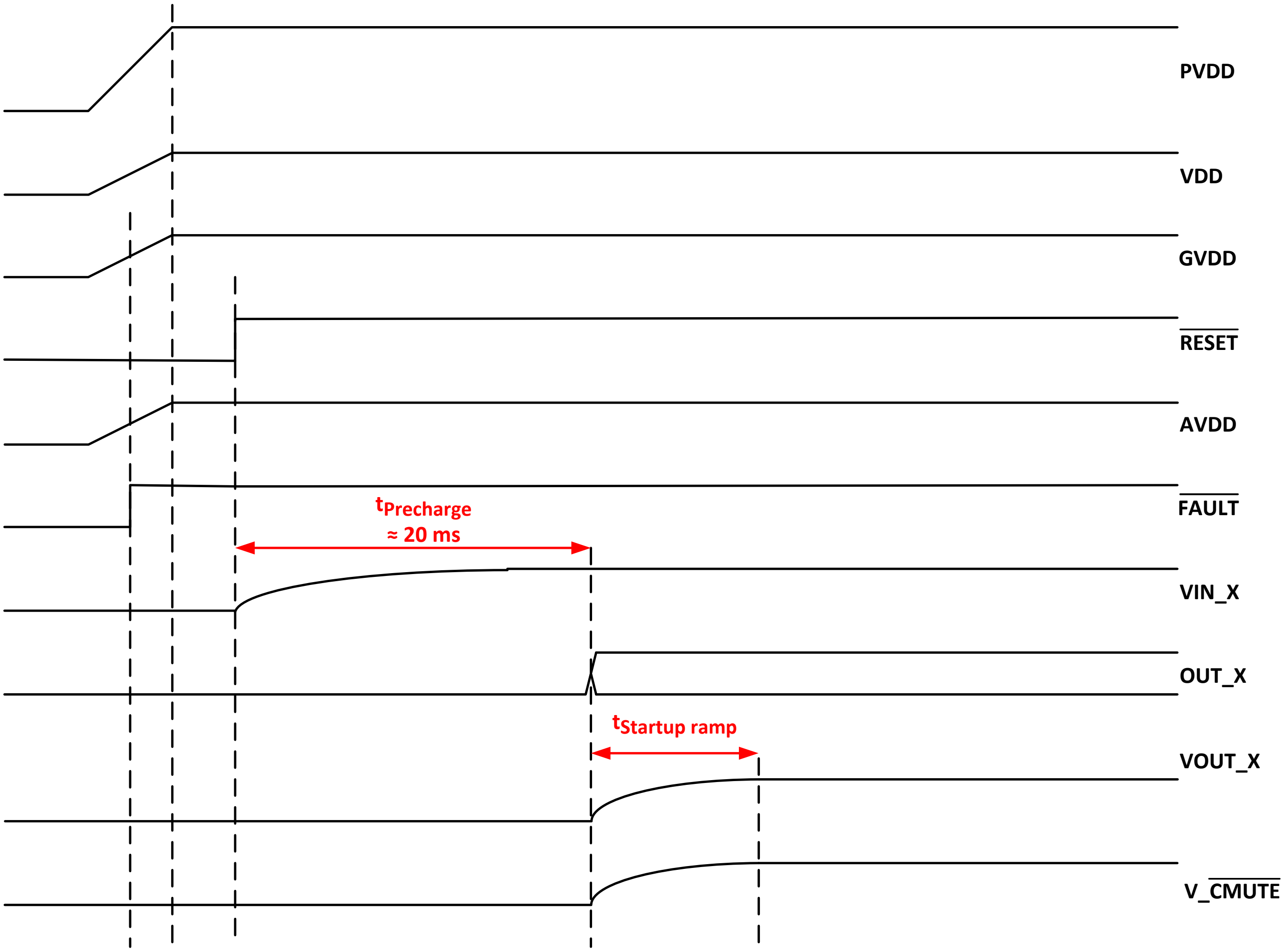


図 47. Startup Timing

When RESET is released to turn on TPA3221, FAULT signal will turn low and AVDD voltage regulator will be enabled. FAULT will stay low until AVDD reaches the undervoltage protection (UVP) voltage threshold (see the Electrical Characteristics table of this data sheet). After a pre-charge time to stabilize the DC voltage across the input AC coupling capacitors, the ramp up sequence starts and completes once the CMUTE node is charged to its final value.

9.4.1.1 Startup Ramp Time

During the startup ramp the CMUTE capacitor is charged by an internal current generator. With use of the recommended 33 nF CMUTE capacitor value, the startup ramp time is approximately 20 ms. Higher CMUTE capacitor value will increase the ramp time, and a lower value will decrease the ramp time. The recommended CMUTE capacitor value is selected for minimum audible artifacts during startup and shutdown ramp.

9.4.2 Powering Down

The TPA3221 does not require a power-down sequence. The device remains fully operational as long as the VDD, AVDD and PVDD voltages are above their undervoltage protection (UVP) voltage thresholds (see the *Electrical Characteristics* table of this data sheet). Although not specifically required, it is a good practice to hold RESET low during power down, thus preventing audible artifacts including pops or clicks by initiating a controlled ramp down sequence of the output voltage. The ramp down sequence will complete once the CMUTE node is discharged.

9.4.2.1 *Power Down Ramp Time*

During the power down ramp the CMUTE capacitor is discharged by internal circuitry. With use of the recommended 33 nF CMUTE capacitor value, the power-down ramp time is approximately 20 ms.

9.4.3 Device Reset

Asserting RESET low initiates the device ramp down. The output FETs go into a Hi-Z state after the ramp down is complete. Output pull downs are active in both BTL mode and PBTL mode with RESET low.

In BTL modes, to accommodate bootstrap charging prior to switching start, asserting the RESET input low enables weak pull-down of the half-bridge outputs.

Asserting RESET low removes any fault information to be signaled on the FAULT output, that is, FAULT is forced high. A rising-edge transition on RESET allows the device to resume operation after a fault. To ensure thermal reliability, the rising edge of RESET must occur no sooner than 4 ms after the falling edge of FAULT.

The TPA3221 will enter a low power state once the ramp down sequence is complete.

9.4.4 Device Soft Mute

Asserting CMUTE low initiates the device soft mute function. The soft mute function initiates a ramp down sequence of the outputs, and the output FETs go into a Hi-Z state after the ramp down is complete. All internal circuits are powered while in soft mute state. External control of the soft mute function must provide high impedance output when not engaged (open drain output) to allow the CMUTE node to charge/discharge during device ramp up and ramp down when de-asserting and asserting RESET.

9.4.5 Device Protection System

The TPA3221 contains advanced protection circuitry carefully designed to facilitate system integration and ease of use, as well as to safeguard the device from permanent failure due to a wide range of fault conditions such as short circuits, overload, overtemperature, overvoltage and undervoltage. The TPA3221 responds to a fault by immediately setting the power stage in a high-impedance (Hi-Z) state and asserting the FAULT pin low. In situations other than overload and overtemperature error (OTE), the device automatically recovers when the fault condition has been removed, that is, the supply voltage has increased. The device will handle errors, as shown in 表 5.

表 5. Device Protection

BTL MODE		PBTL MODE	
LOCAL ERROR IN	TURNS OFF	LOCAL ERROR IN	TURNS OFF
A	A+B	A	A+B+C+D
B		B	
C	C+D	C	
D		D	

Bootstrap UVP does not shutdown according to the table, it shuts down the respective halfbridge (non-latching, does not assert FAULT).

9.4.5.1 *Overload and Short Circuit Current Protection*

TPA3221 has fast reacting current sensors on all high-side and low-side FETs. To prevent output current from increasing beyond the overcurrent threshold, TPA3221 uses current limiting of the output current for each switching cycle (Cycle By Cycle Current Control, CB3C) in case of excess output current. CB3C prevents premature shutdown due to high output current transients caused by high level music transients and a drop of real speaker’s load impedance, and allows the output current to be limited to a maximum programmed level. If the maximum output current persists, i.e. the power stage being overloaded with too low load impedance, the device will shut down the affected output channel and the affected output is put in a high-impedance (Hi- Z) state until a RESET cycle is initiated. CB3C works individually for each full-bridge output. If an over current event is triggered, CB3C performs a state flip of the full-bridged output that is cleared upon beginning of next PWM frame.

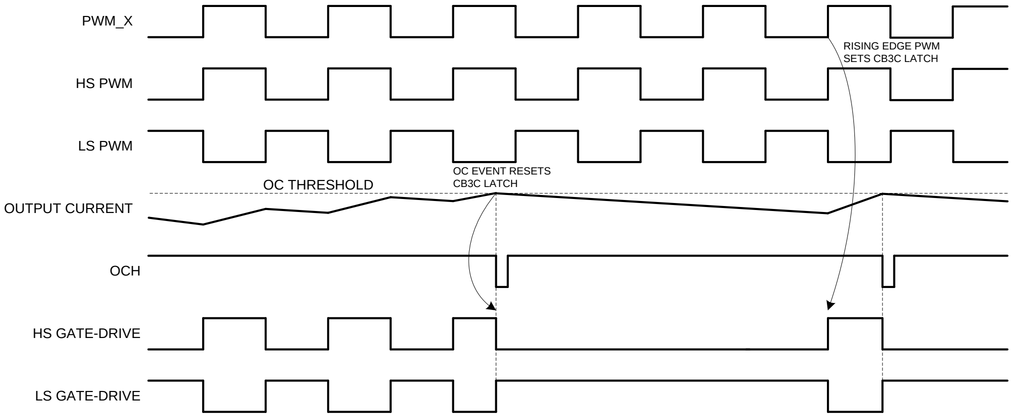


図 48. CB3C Timing Example

9.4.5.2 *Signal Clipping and Pulse Injector*

A built in activity detector monitors the PWM activity of the OUT_X pins. TPA3221 is designed to drive unclipped output signals all the way to PVDD and GND rails. In case of audio signal clipping when applying excessive input signal voltage, or in case of CB3C current protection being active, the amplifier feedback loop of the audio channel will respond to this condition with a saturated state, and the output PWM signals will stop unless special circuitry is implemented to handle this situation. To prevent the output PWM signals from stopping in a clipping or CB3C situation, narrow pulses are injected to the gate drive to maintain output activity. The injected narrow pulses are injected at every 4th PWM frame, and thus the effective switching frequency during this state is reduced to 1/4 of the normal switching frequency.

Signal clipping is signalled on the OTW_CLIP pin and is self clearing when signal level reduces and the device reverts to normal operation. The OTW_CLIP pulses starts at the onset to output clipping, typically at a THD level around 0.01%, resulting in narrow OTW_CLIP pulses starting with a pulse width of ~500ns.

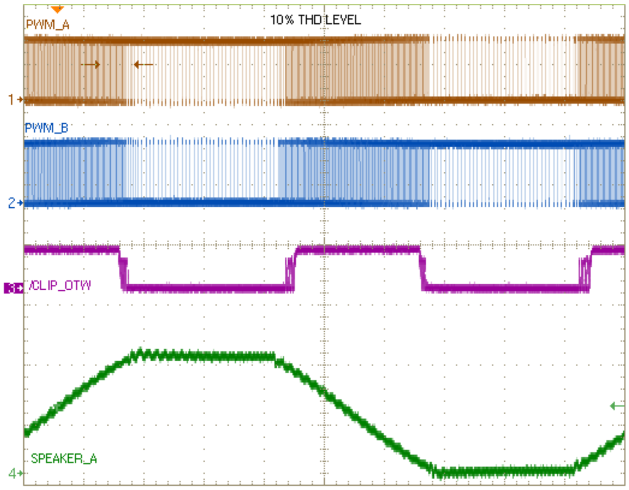


図 49. Signal Clipping PWM and Speaker Output Signals

9.4.5.3 DC Speaker Protection

The output DC protection scheme protects a speaker from excess DC current in case one terminal of the speaker is connected to the amplifier while the other is accidentally shorted to the chassis ground. Such a short circuit results in a DC voltage of PVDD/2 across the speaker, which potentially can result in destructive current levels. The output DC protection detects any unbalance of the output and input current of a BTL or PBTL output configuration (current into/out of one half-bridge equals current out of/into the other half-bridge), and in the event of the unbalance exceeding a programmed threshold, the overload counter increments until its maximum value and the affected output channel is shut down. DC Speaker Protection is enabled in both BTL and PBTL mode operation.

9.4.5.4 Pin-to-Pin Short Circuit Protection (PPSC)

The PPSC detection system protects the device from permanent damage in the case that a power output pin (OUT_X) is shorted to GND_X or PVDD_X. For comparison, the OC protection system detects an overcurrent after the demodulation filter where PPSC detects shorts directly at the pin before the filter. PPSC detection is performed at startup after RESET is pulled high. When PPSC detection is activated by a short on the output, all half-bridges are kept in a Hi-Z state until the short is removed; the device then continues the startup sequence and starts switching. The detection is controlled globally by a two step sequence. The first step ensures that there are no shorts from OUT_X to GND_X, the second step tests that there are no shorts from OUT_X to PVDD_X. The total duration of this process is roughly proportional to the capacitance of the output LC filter. The typical duration is < 15 ms/μF. While the PPSC detection is in progress, FAULT is kept low. If no shorts are present the PPSC detection passes, and FAULT is released. A device reset will start a new PPSC detection. PPSC detection is enabled in both BTL and PBTL output configurations. To make sure not to trip the PPSC detection system it is recommended not to insert a resistive load to GND_X or PVDD_X.

9.4.5.5 Overtemperature Protection OTW and OTE

TPA3221 has a two-level temperature-protection system that asserts an active-low warning signal (OTW_CLIP) when the device junction temperature exceeds 125°C (typical) and, if the device junction temperature exceeds 155°C (typical), the device is put into thermal shutdown, resulting in all half-bridge outputs being set in the high-impedance (Hi-Z) state and FAULT being asserted low. OTE is latched in this case. To clear the OTE latch, RESET must be asserted. Thereafter, the device resumes normal operation.

9.4.5.6 Undervoltage Protection (UVP), Overvoltage Protection (OVP) and Power-on Reset (POR)

The UVP, OVP and POR circuits of the TPA3221 fully protect the device in any power-up/down, and brownout situation, and also in overvoltage situation with PVDD not exceeding the values stated in Absolute Maximum Ratings. While powering up, the POR circuit ensures that all circuits are fully operational when the AVDD supply voltage reaches the value stated in the *Electrical Characteristics* table. Although AVDD is independently monitored, a supply voltage drop below the UVP threshold on AVDD pin results in all half-bridge outputs immediately being set in the high-impedance (Hi-Z) state and FAULT being asserted low. The device automatically resumes operation when all supply voltages have increased above their UVP threshold. In case of an OVP event, all half-bridge outputs are immediately set in the high-impedance (Hi-Z) state and FAULT is asserted low until PVDD is below the OVP threshold.

9.4.5.7 Fault Handling

If a fault situation occurs while in operation, the device acts accordingly to the fault being a global or a channel fault. A global fault is a chip-wide fault situation and causes all PWM activity of the device to be shut down, and will assert $\overline{\text{FAULT}}$ low. A global fault is a latching fault and clearing $\overline{\text{FAULT}}$ and restarting operation requires resetting the device by toggling $\overline{\text{RESET}}$. De-asserting $\overline{\text{RESET}}$ should never be allowed with excessive system temperature, so it is advised to monitor $\overline{\text{RESET}}$ with a system microcontroller and only release $\overline{\text{RESET}}$ ($\overline{\text{RESET}}$ high) if the $\overline{\text{OTW\_CLIP}}$ signal is cleared (high). A channel fault results in shutdown of the PWM activity of the affected channel(s). Note that asserting $\overline{\text{RESET}}$ low forces the $\overline{\text{FAULT}}$ signal high, independent of faults being present.

表 6. Error Reporting

Fault/Event	Fault/Event Description	Global or Channel	Reporting Method	Latched/Self Clearing	Action needed to Clear	Output FETs
PVDD_X UVP	Voltage Fault	Global	$\overline{\text{FAULT}}$ pin	Self Clearing	Increase affected supply voltage	HI-Z
PVDD_X OVP						
AVDD UVP						
POR (AVDD UVP)	Power On Reset	Global	$\overline{\text{FAULT}}$ pin	Self Clearing	Allow AVDD to rise	HI-Z
OTW	Thermal Warning	Global	$\overline{\text{OTW}}$ pin	Self Clearing	Cool below OTW threshold	Normal operation
OTE	Thermal Shutdown	Global	$\overline{\text{FAULT}}$ pin	Latched	Toggle $\overline{\text{RESET}}$	HI-Z
OLP (CB3C>1.7 ms)	OC Shutdown	Channel	$\overline{\text{FAULT}}$ pin	Latched	Toggle $\overline{\text{RESET}}$	HI-Z
CB3C	OC Limiting	Channel	None	Self Clearing	Reduce signal level or remove short	Flip state, cycle by cycle at fs/3
Stuck at Fault(1)	No OSC_IO activity in Slave Mode	Global	None	Self Clearing	Resume OSC_IO activity	HI-Z

(1) Stuck at Fault occurs when input OSC_IO input signal frequency drops below minimum frequency given in the *Electrical Characteristics* table of this data sheet.

10 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

TPA3221 can be configured either in stereo BTL, mono BTL or mono PBTL mode depending on output power conditions and system design.

10.2 Typical Applications

10.2.1 Stereo BTL Application

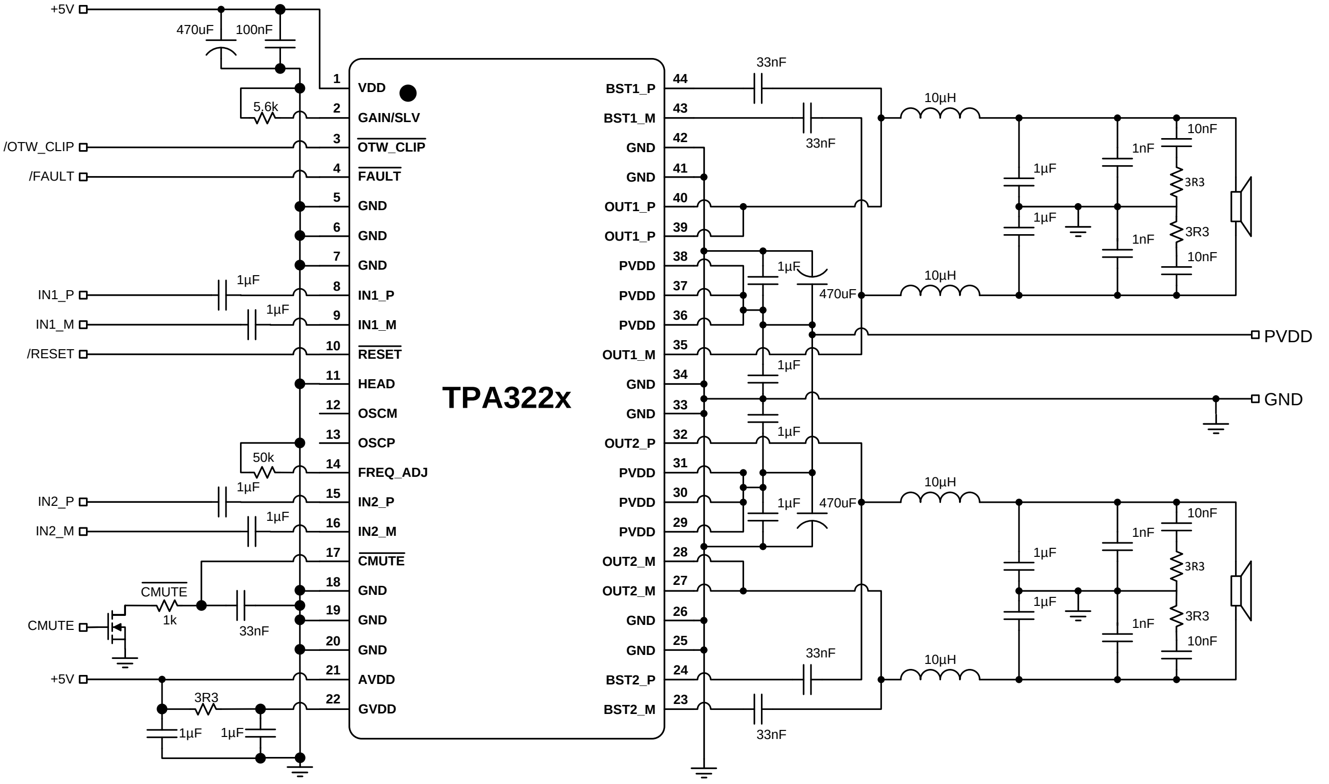


図 50. Typical Differential (2N) AD-Mode BTL Application

Typical Applications (continued)

10.2.1.1 Design Requirements

For this design example, use the parameters in 表 7.

表 7. Design Requirements, BTL Application

DESIGN PARAMETER	EXAMPLE
ExternalLow Power Supply	5 V
High Power Supply	7 - 30 V
Analog Inputs	IN1_M = ±2.8V (peak, max)
	IN1_P = ±2.8V (peak, max)
	IN2_M = ±2.8V (peak, max)
	IN2_P = ±2.8V (peak, max)
Output Filters	Inductor-Capacitor Low Pass FIlter (10 µH + 1 µF)
Speaker Impedance	3 - 8 Ω

10.2.1.2 Detailed Design Procedures

A rising-edge transition on $\overline{\text{RESET}}$ input allows the device to execute the startup sequence and starts switching.

A toggling $\overline{\text{OTW\_CLIP}}$ signal is indicating that the output is approaching clipping. The signal can be used either to decrease audio volume or to control an intelligent power supply nominally operating at a low rail adjusting to a higher supply rail.

The device inverts the audio signal from input to output.

The AVDD pin is not recommended to be used as a voltage source for external circuitry when internal LDO is enabled (VDD ≥ 7 V).

10.2.1.2.1 Decoupling Capacitor Recommendations

In order to design an amplifier that has robust performance, passes regulatory requirements, and exhibits good audio performance, good quality decoupling capacitors should be used. In practice, X7R should be used in this application.

The voltage of the decoupling capacitors should be selected in accordance with good design practices. Temperature, ripple current, and voltage overshoot must be considered. This fact is particularly true in the selection of the 1µF that is placed on the power supply to each full-bridge. It must withstand the voltage overshoot of the PWM switching, the heat generated by the amplifier during high power output, and the ripple current created by high power output. A minimum voltage rating of 50 V is required for use with a 30 V power supply.

10.2.1.2.2 PVDD Capacitor Recommendation

The large capacitors used in conjunction with each full-bridge, are referred to as the PVDD Capacitors. These capacitors should be selected for proper voltage margin and adequate capacitance to support the power requirements. In practice, with a well designed system power supply, 470 µF, 50 V supports most applications. The PVDD capacitors should be low ESR type because they are used in a circuit associated with high-speed switching.

10.2.1.2.3 BST capacitors

To ensure large enough bootstrap energy storage for the high side gate drive to work correctly with all audio source signals, 33 nF / 50V X7R BST capacitors are recommended.

10.2.1.2.4 PCB Material Recommendation

FR-4 Glass Epoxy material with 2 oz. (70 µm) copper is recommended for use with the TPA3221. The use of this material can provide for higher power output, improved thermal performance, and better EMI margin (due to lower PCB trace inductance.

10.2.2 Typical Application, Differential (2N), AD-Mode PBTL (Outputs Paralleled before LC filter)

TPA3221 can be configured in mono PBTL mode by paralleling the outputs before the LC filter or after the LC filter (see *Typical Application, Differential (2N), AD-Mode PBTL (Outputs Paralleled after LC filter)*). Paralleled outputs before the LC filter is recommended for better performance and limiting the number of output LC filter inductors,

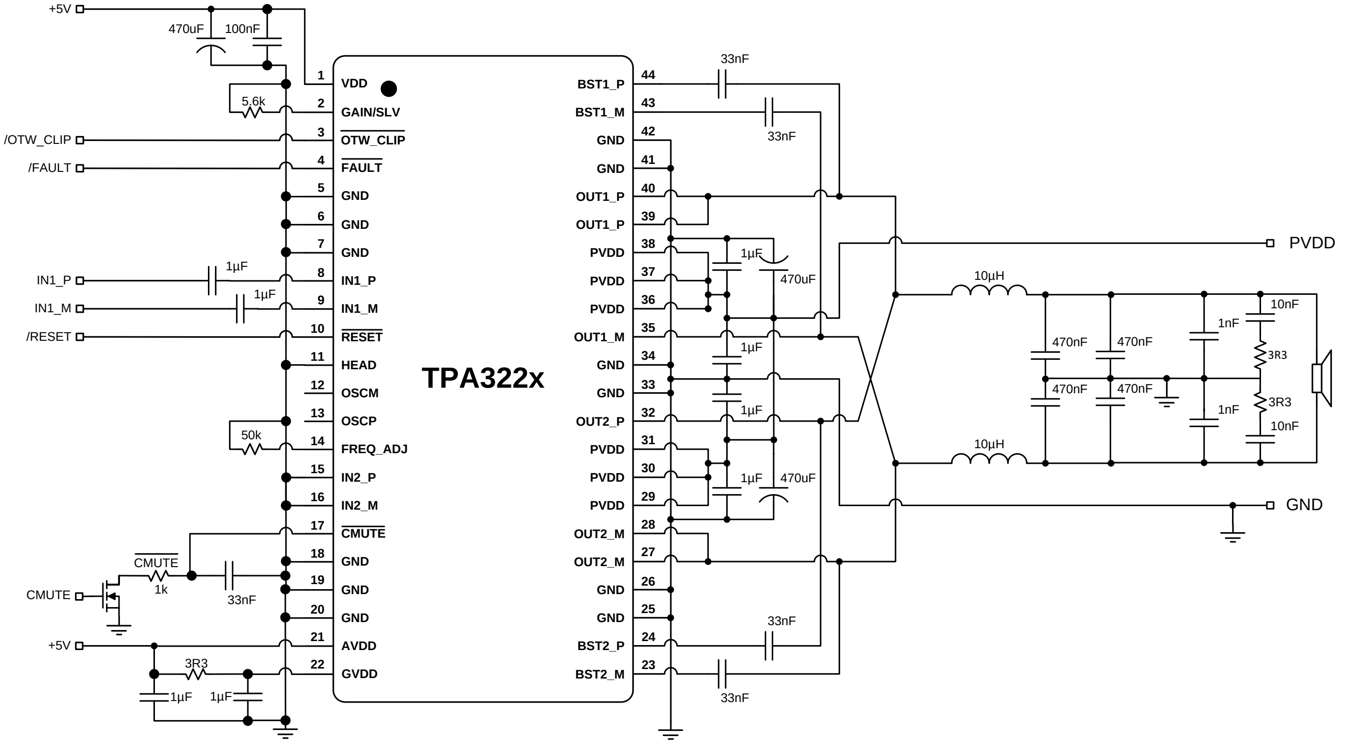


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図 51. Typical Differential (2N) AD-Mode PBTL Application

10.2.2.1 Design Requirements

Refer to *Stereo BTL Application* for the Design Requirements.

表 8. Design Requirements, PBTL Application

DESIGN PARAMETER	EXAMPLE
Low Power Supply	5 V
High Power Supply	7 - 30 V
Analog Inputs	IN1_M = ±2.8 V (peak, max)
	IN1_P = ±2.8 V (peak, max)
	IN2_M = Grounded
	IN2_P = Grounded
Output Filters	Inductor-Capacitor Low Pass FIlter (10 µH + 1 µF)
Speaker Impedance	2 - 4 Ω

10.2.3 Typical Application, Differential (2N), AD-Mode PBTL (Outputs Paralleled after LC filter)

TPA3221 can be configured in mono PBTL mode by paralleling the outputs before the LC filter (see *Typical Application, Differential (2N), AD-Mode PBTL (Outputs Paralleled before LC filter)*) or after the LC filter. Paralleled outputs after the LC filter may be preferred if: a single board design must support both PBTL and BTL, or in the case multiple, smaller paralleled inductors are preferred due to size or cost. Paralleling after the LC filter requires four inductors, one for each OUT_x. This section shows an example of paralleled outputs after the LC filter.

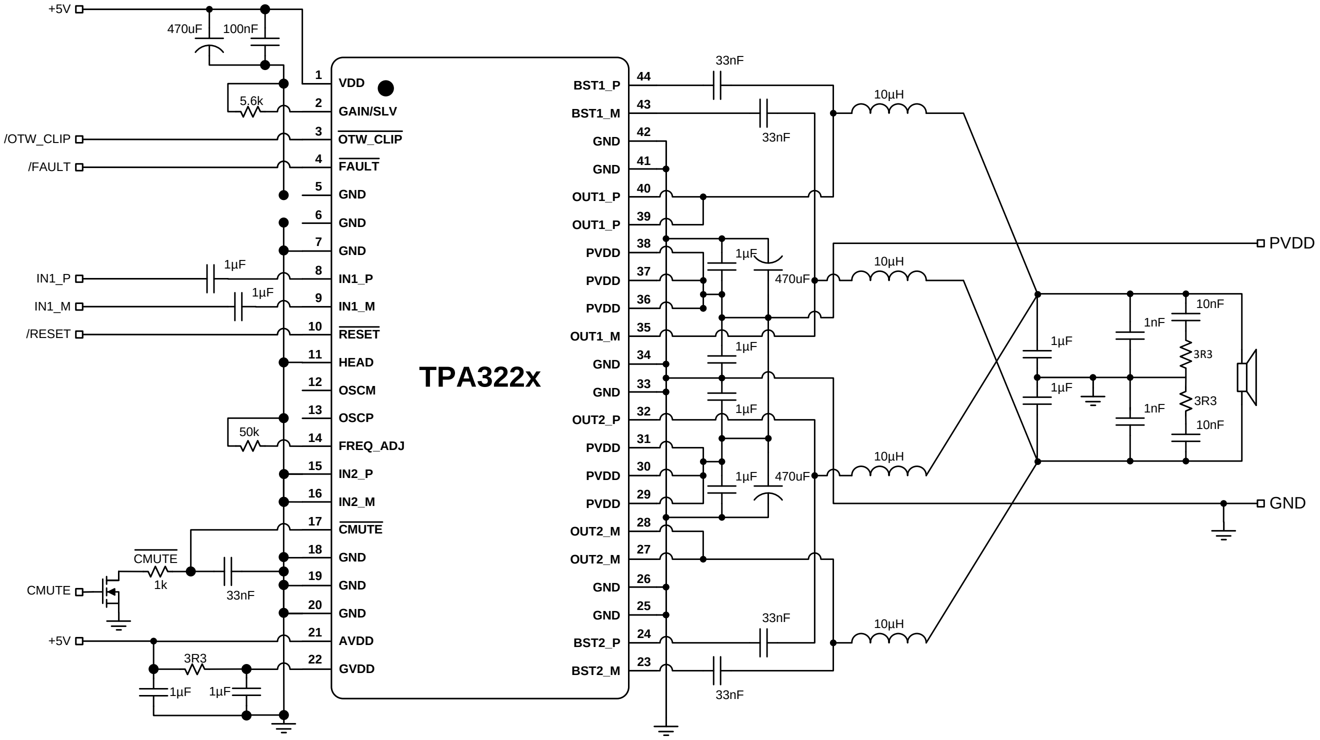


図 52. Typical Differential (2N) AD-Mode PBTL Application

10.2.3.1 Design Requirements

Refer to *Stereo BTL Application* for the Design Requirements.

表 9. Design Requirements, PBTL Application

DESIGN PARAMETER	EXAMPLE
Low Power Supply	5 V
High Power Supply	7 - 30 V
Analog Inputs	IN1_M = ±2.8 V (peak, max)
	IN1_P = ±2.8 V (peak, max)
	IN2_M = Grounded
	IN2_P = Grounded
Output Filters	Inductor-Capacitor Low Pass FIlter (10 µH + 1 µF)
Speaker Impedance	2 - 4 Ω

11 Power Supply Recommendations

11.1 Power Supplies

The TPA3221 device requires a single external power supply for proper operation. A high-voltage supply, PVDD, is required to power the output stage of the speaker amplifier and its associated circuitry. PVDD can be used to supply an internal LDO to supply 5 V to AVDD and GVDD (connect VDD to PVDD).

Additionally, in LDO bypass mode an external power supply should be connected to VDD, AVDD and GVDD to power the gate-drive and other internal digital and analog circuit blocks in the device.

The allowable voltage range for both the PVDD and VDD/AVDD/GVDD supplies are listed in the *Recommended Operating Conditions* table. Ensure both the PVDD and the VDD/AVDD/GVDD supplies can deliver more current than listed in the *Electrical Characteristics* table.

11.1.1 VDD Supply

VDD can be connected to PVDD in systems using only a single power supply. VDD is connected to an internal LDO that is then used to supply AVDD and GVDD for digital and analog circuits as well as to supply the gate drive.

To reduce device power consumption, the internal LDO can be bypassed by connecting VDD, AVDD and GVDD to an external 5 V power supply.

Proper connection, routing, and decoupling techniques are highlighted in the TPA3221 device EVM User's Guide (as well as the *Application Information* section and *Layout Examples* section) and must be followed as closely as possible for proper operation and performance. Deviation from the guidance offered in the TPA3221 device EVM User's Guide, which followed the same techniques as those shown in the *Application Information* section, may result in reduced performance, errant functionality, or even damage to the TPA3221 device. To simplify the power supply requirements for the system, the TPA3221 device includes a integrated low-dropout (LDO) linear regulator to create a 5V rail for AVDD and GVDD supplies. The linear regulator is internally connected to the VDD supply and its output is present on the AVDD pin, providing a connection point for an external bypass capacitors. It is important to note that the linear regulator integrated in the device has only been designed to support the current requirements of the internal circuitry, and should not be used to power any additional external circuitry. Additional loading on these pins could cause the voltage to sag and increase noise injection, which negatively affects the performance and operation of the device.

11.1.2 AVDD and GVDD Supplies

AVDD and GVDD can be supplied either through the internal LDO or from external 5 V power supply to power internal analog and digital circuits and the gate-drives for the output H-bridges. Proper connection, routing, and decoupling techniques are highlighted in the TPA3221 device EVM User's Guide (as well as the *Application Information* section and *Layout Examples* section) and must be followed as closely as possible for proper operation and performance. Deviation from the guidance offered in the TPA3221 device EVM User's Guide, which followed the same techniques as those shown in the *Application Information* section, may result in reduced performance, errant functionality, or even damage to the TPA3221 device.

11.1.3 PVDD Supply

The output stage of the speaker amplifier drives the load using the PVDD supply. This is the power supply which provides the drive current to the load during playback. Proper connection, routing, and decoupling techniques are highlighted in the TPA3221 device EVM User's Guide (as well as the *Application Information* section and *Layout Examples* section) and must be followed as closely as possible for proper operation and performance. Due the high-voltage switching of the output stage, it is particularly important to properly decouple the output power stages in the manner described in the TPA3221 device EVM User's Guide. The lack of proper decoupling, like that shown in the EVM User's Guide, can results in voltage spikes which can damage the device, or cause poor audio performance and device shutdown faults.

Power Supplies (continued)

11.1.4 BST Supply

TPA3221 has built-in bootstrap supply for each half bridge gate drive to supply the high side MOSFETs, only requiring a single capacitor per half bridge. The capacitors are connected to each half bridge output, and are charged by the GVDD supply via an internal diode while the PWM outputs are in low state. The high side gate drive is supplied by the voltage across the BST capacitor while the output PWM is high. It is recommended to place the BST capacitors close to the TPA3221 device, and to keep PCB routing traces at minimum length.

12 Layout

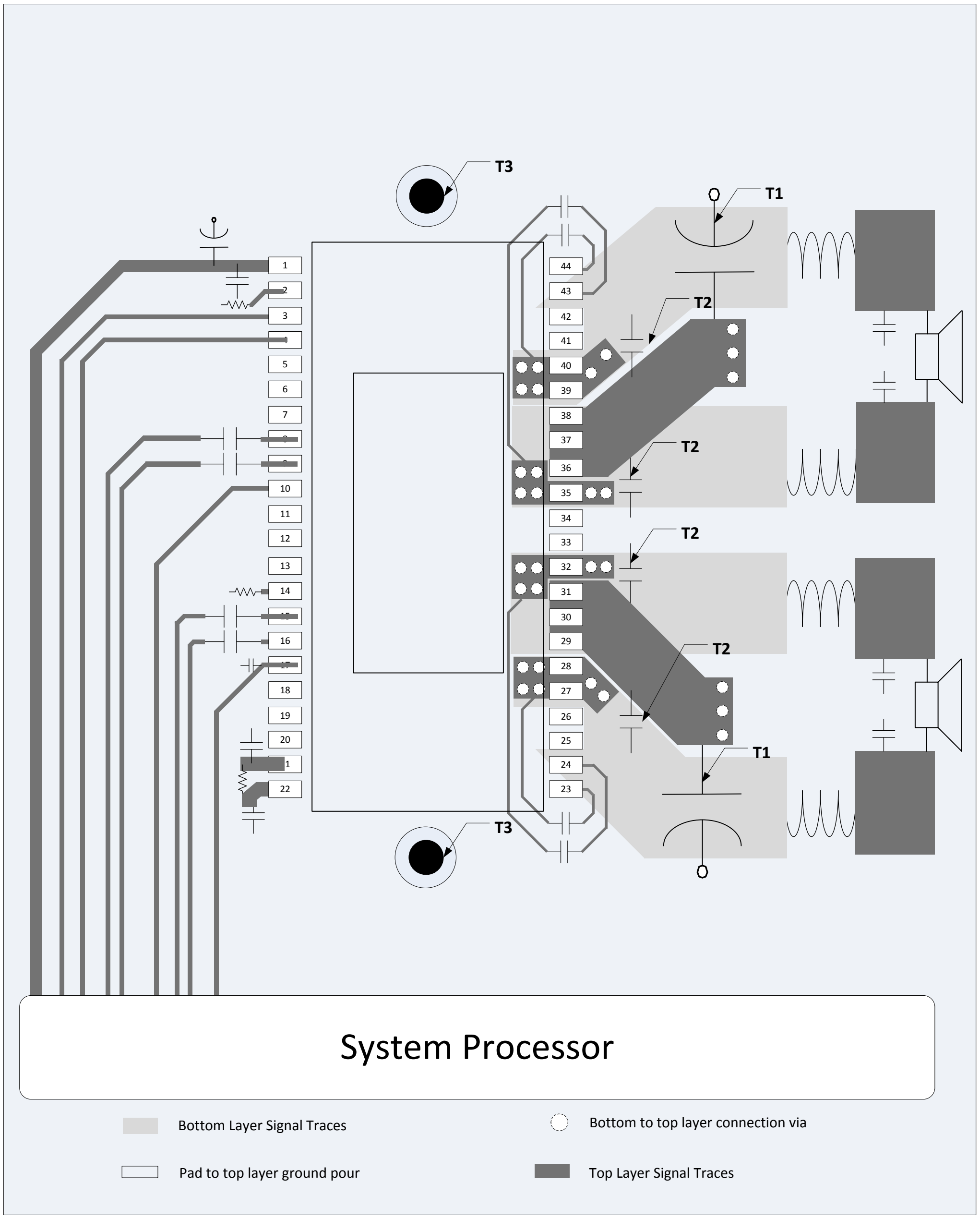
12.1 Layout Guidelines

- Use an unbroken ground plane to have good low impedance and inductance return path to the power supply for power and audio signals.
- Maintain a contiguous ground plane from the ground pins to the PCB area surrounding the device for as many of the ground pins as possible, since the ground pins are the best conductors of heat in the package.
- PCB layout, audio performance and EMI are linked closely together.
- Routing the audio input should be kept short and together with the accompanied audio source ground.
- The small bypass capacitors on the PVDD lines should be placed as close the PVDD pins as possible.
- A local ground area underneath the device is important to keep solid to minimize ground bounce.
- Orient the passive component so that the narrow end of the passive component is facing the TPA3221 device, unless the area between two pads of a passive component is large enough to allow copper to flow in between the two pads.
- Avoid placing other heat producing components or structures near the TPA3221 device.
- Avoid cutting off the flow of heat from the TPA3221 device to the surrounding ground areas with traces or via strings, especially on output side of device.

Netlist for this printed circuit board is generated from the schematic in 図 53.

12.2 Layout Examples

12.2.1 BTL Application Printed Circuit Board Layout Example



A. Note: PCB layout example shows composite layout. Dark grey: Top layer copper traces, light gray: Bottom layer copper traces. All PCB area not used for traces should be GND copper pour (transparent on example image)

B. **Note T1**: PVDD decoupling bulk capacitors should be as close as possible to the PVDD and GND_X pins, the heat sink sets the distance. Wide traces should be routed on the top layer with direct connection to the pins and without going through vias. No vias or traces should be blocking the current path.

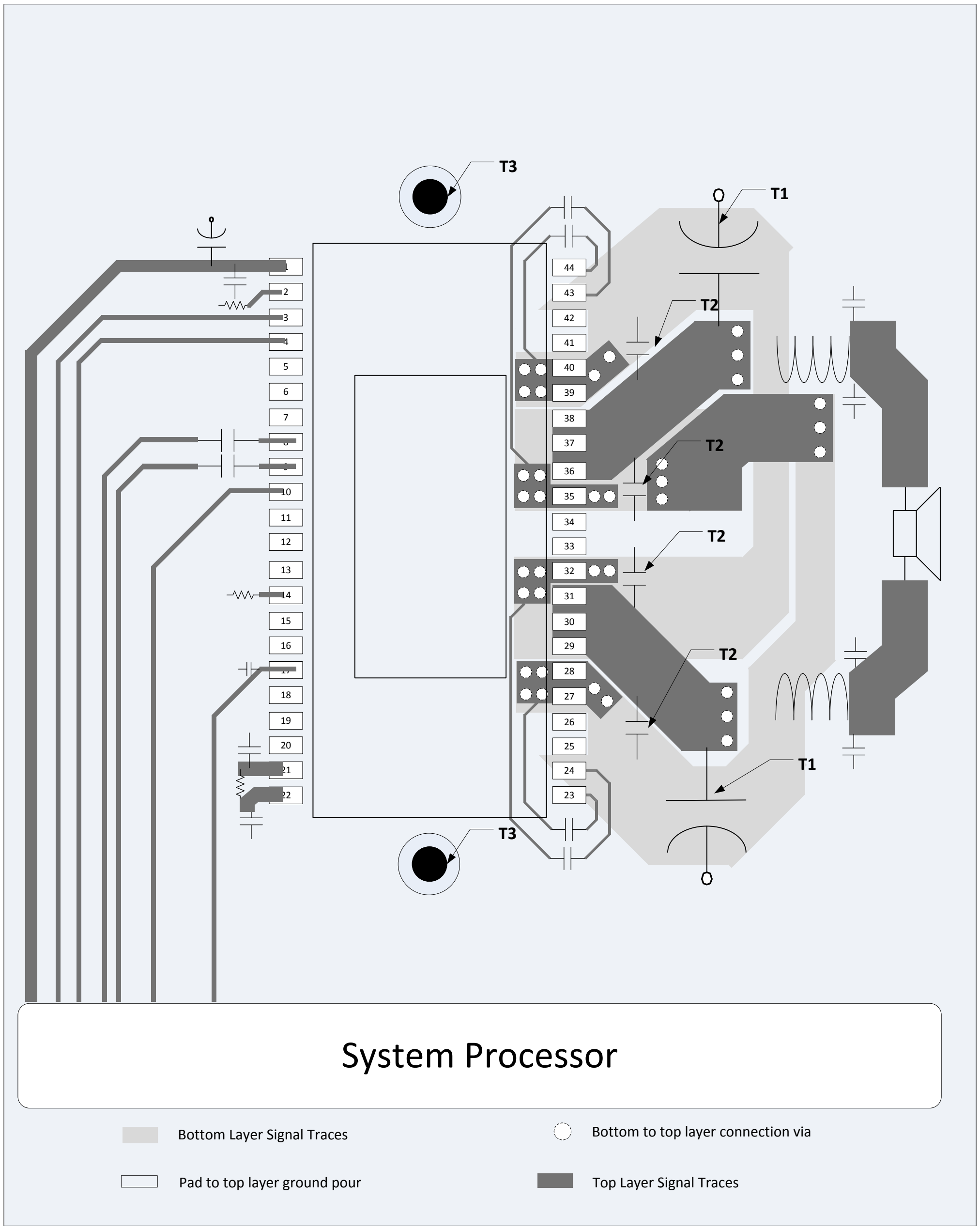
C. **Note T2**: Close decoupling of PVDD with low impedance X7R ceramic capacitors is placed under the heat sink and close to the pins.

D. **Note T3**: Heat sink needs to have a good connection to PCB ground.

図 53. BTL Application Printed Circuit Board - Composite

Layout Examples (continued)

12.2.2 PBTL (Outputs Paralleled before LC filter) Application Printed Circuit Board Layout Example



A. Note: PCB layout example shows composite layout. Dark grey: Top layer copper traces, light gray: Bottom layer copper traces. All PCB area not used for traces should be GND copper pour (transparent on example image)

B. **Note T1**: PVDD decoupling bulk capacitors should be as close as possible to the PVDD and GND_X pins, the heat sink sets the distance. Wide traces should be routed on the top layer with direct connection to the pins and without going through vias. No vias or traces should be blocking the current path.

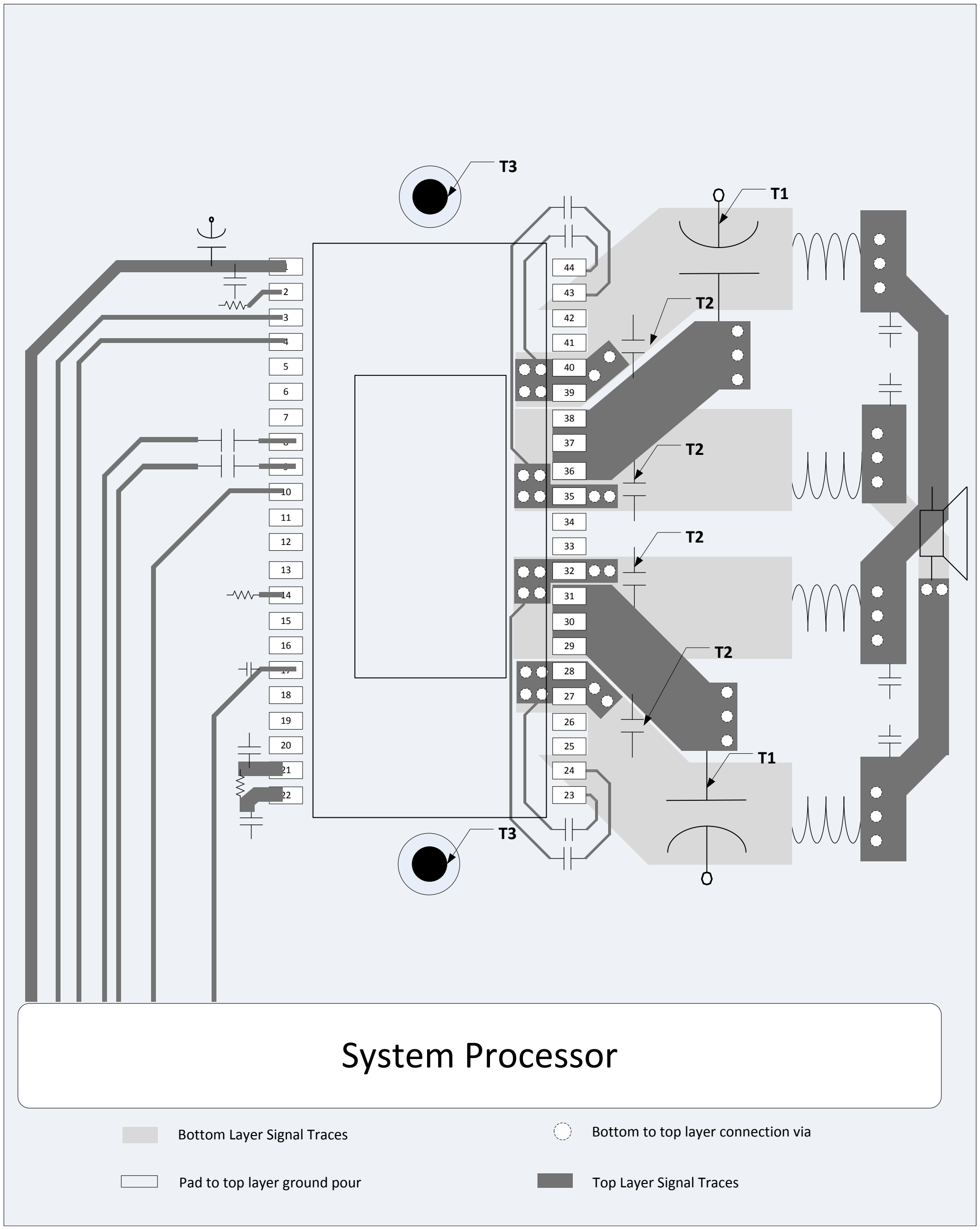
C. **Note T2**: Close decoupling of PVDD with low impedance X7R ceramic capacitors is placed under the heat sink and close to the pins.

D. **Note T3**: Heat sink needs to have a good connection to PCB ground.

図 54. PBTL (Outputs Paralleled before LC filter) Application Printed Circuit Board - Composite

Layout Examples (continued)

12.2.3 PBTL (Outputs Paralleled after LC filter) Application Printed Circuit Board Layout Example



A. Note: PCB layout example shows composite layout. Dark grey: Top layer copper traces, light gray: Bottom layer copper traces. All PCB area not used for traces should be GND copper pour (transparent on example image)

B. **Note T1**: PVDD decoupling bulk capacitors should be as close as possible to the PVDD and GND_X pins, the heat sink sets the distance. Wide traces should be routed on the top layer with direct connection to the pins and without going through vias. No vias or traces should be blocking the current path.

C. **Note T2**: Close decoupling of PVDD with low impedance X7R ceramic capacitors is placed under the heat sink and close to the pins.

D. **ote T3**: Heat sink needs to have a good connection to PCB ground.

図 55. PBTL (Outputs Paralleled after LC filter) Application Printed Circuit Board - Composite

13 デバイスおよびドキュメントのサポート

13.1 ドキュメントのサポート

『TPA3221評価モジュール・ユーザー・ガイド』

13.2 ドキュメントの更新通知を受け取る方法

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13.3 コミュニティ・リソース

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13.4 商標

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13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPA3221DDV	Active	Production	HTSSOP (DDV) | 44	35 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	3221
TPA3221DDV.A	Active	Production	HTSSOP (DDV) | 44	35 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	3221
TPA3221DDVR	Active	Production	HTSSOP (DDV) | 44	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	3221
TPA3221DDVR.A	Active	Production	HTSSOP (DDV) | 44	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	3221

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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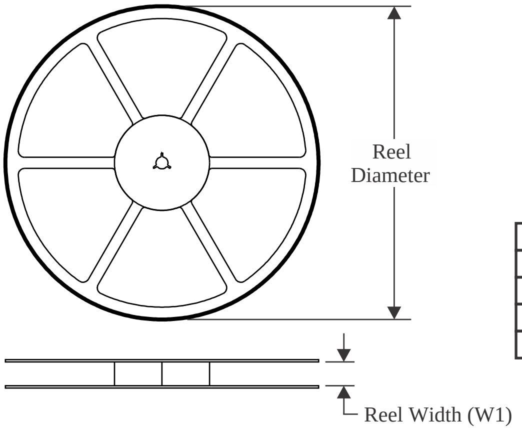
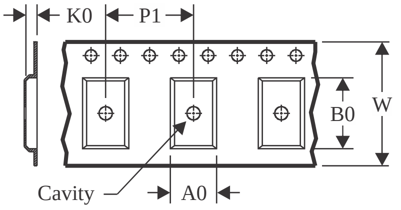
TAPE AND REEL INFORMATION

REEL DIMENSIONS

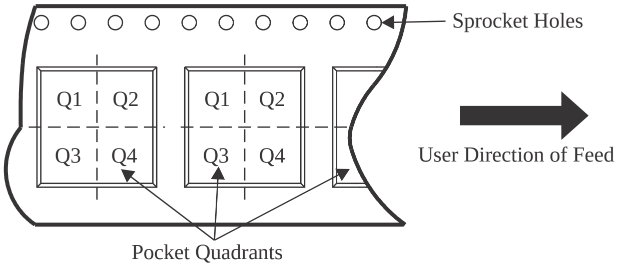


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

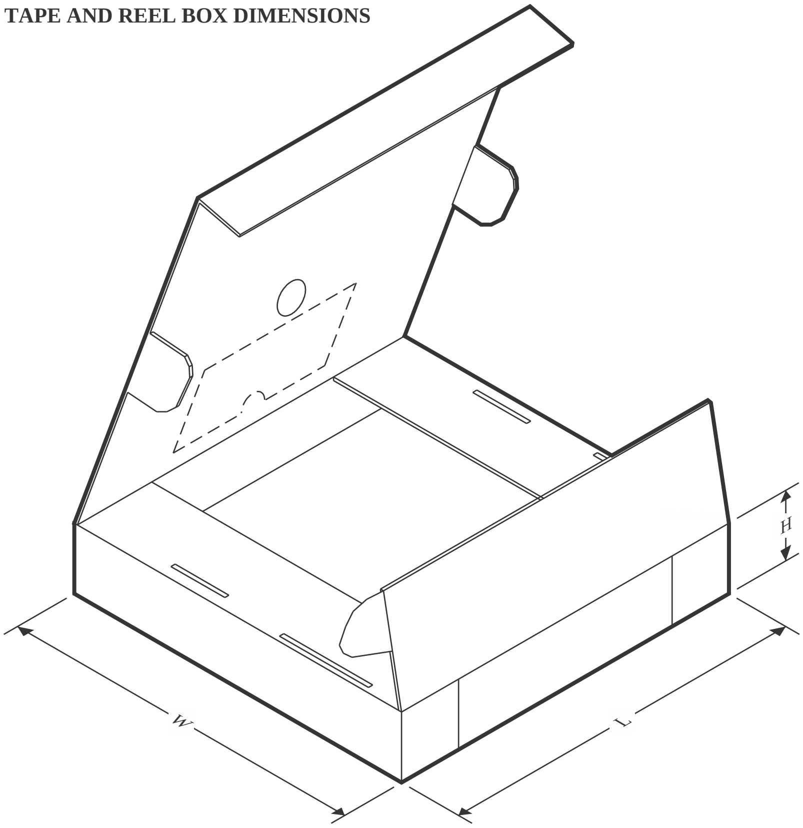
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA3221DDVR	HTSSOP	DDV	44	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1

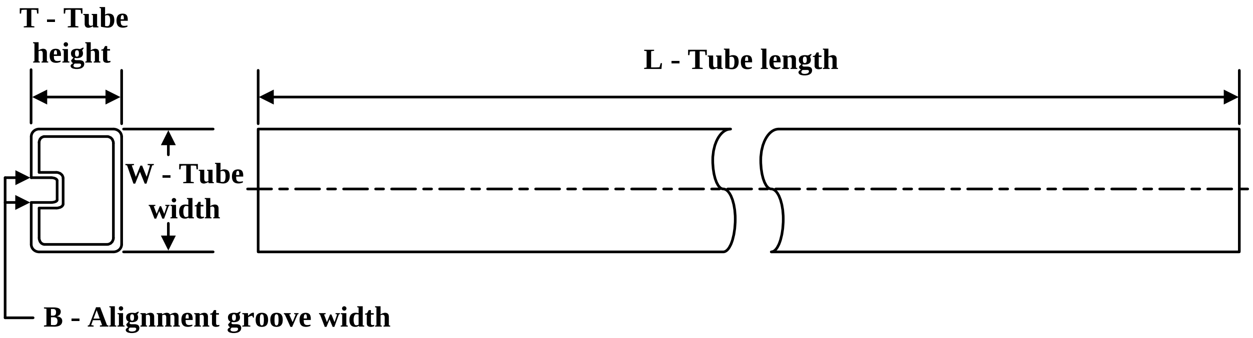
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA3221DDVR	HTSSOP	DDV	44	2000	350.0	350.0	43.0

TUBE



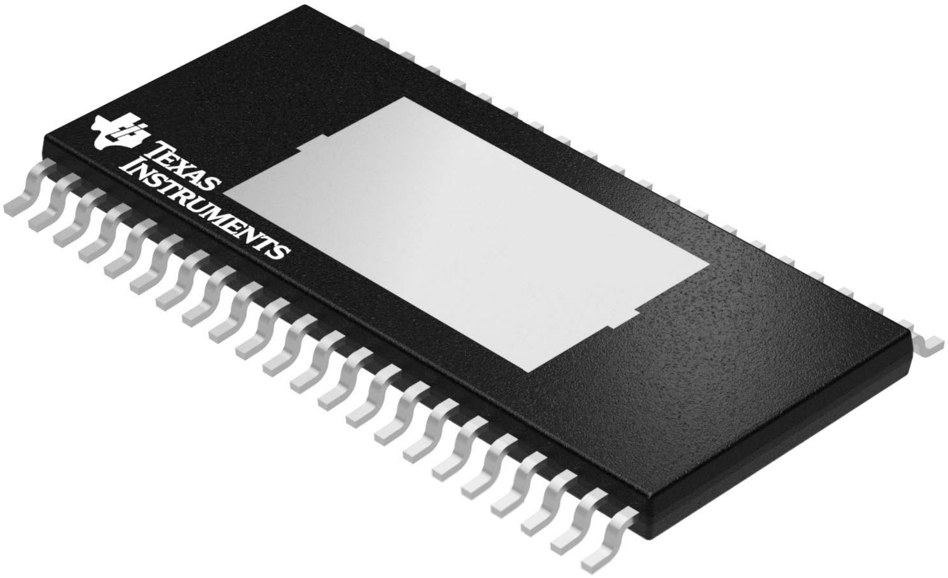
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPA3221DDV	DDV	HTSSOP	44	35	530	11.89	3600	4.9
TPA3221DDV.A	DDV	HTSSOP	44	35	530	11.89	3600	4.9

GENERIC PACKAGE VIEW

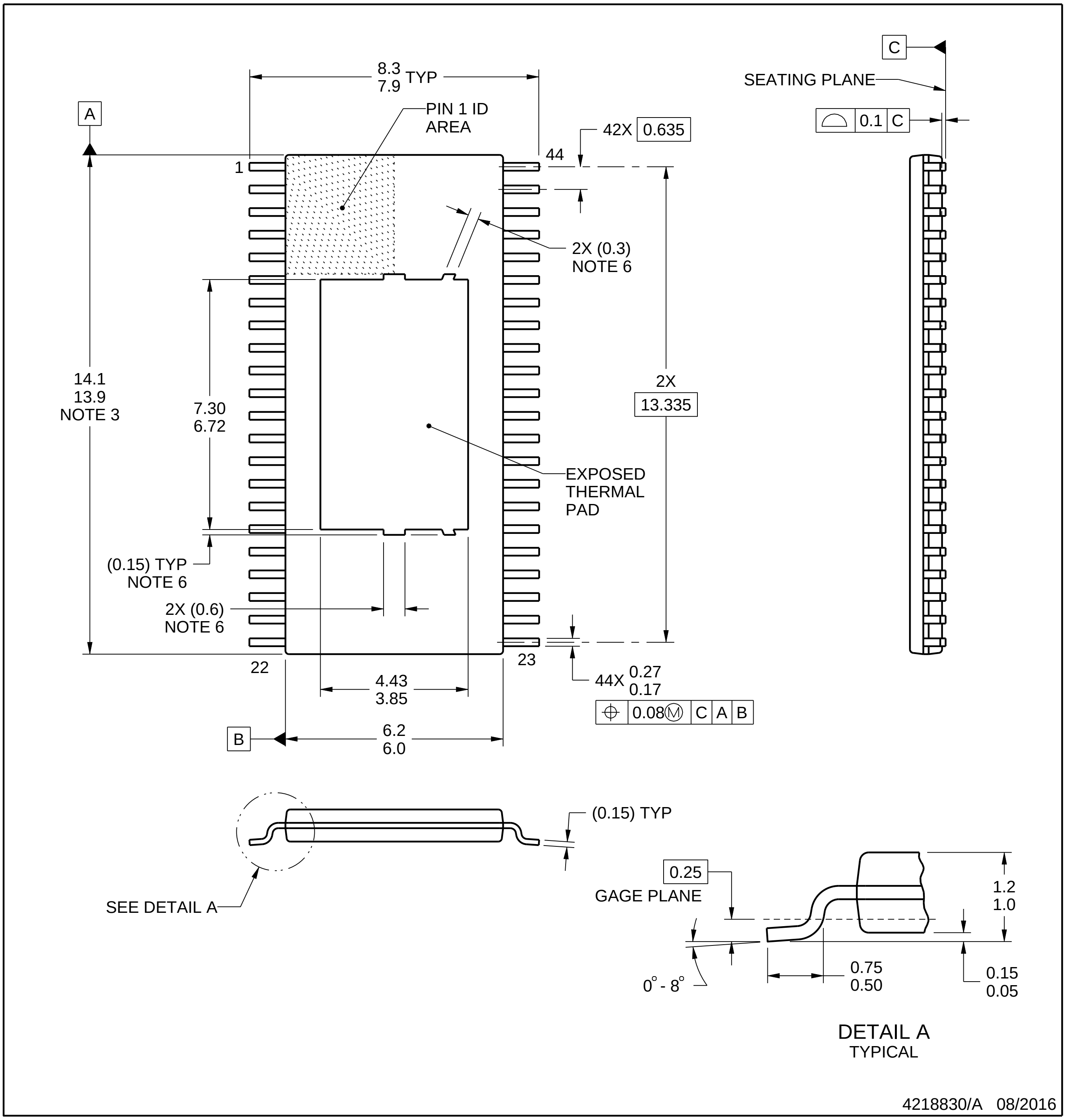
DDV 44 PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4206011/H

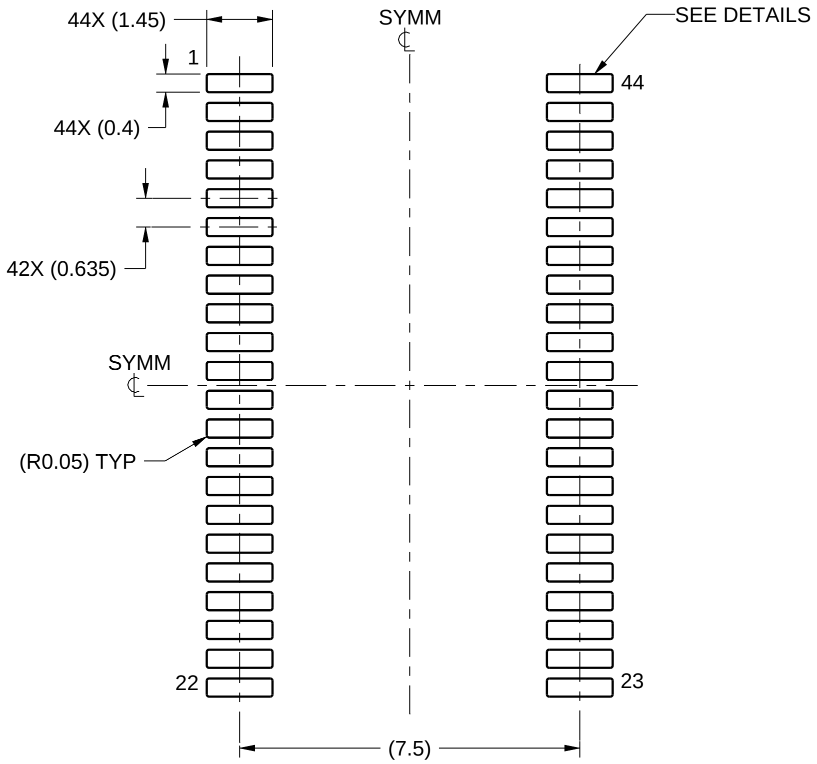


4218830/A 08/2016

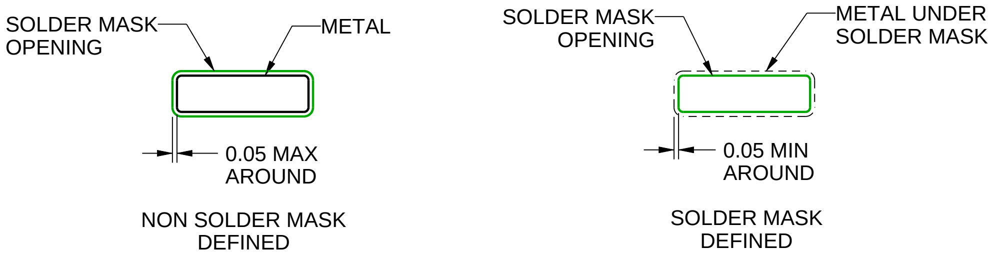
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. The exposed thermal pad is designed to be attached to an external heatsink.
6. Features may differ or may not be present.



LAND PATTERN EXAMPLE
SCALE:6X

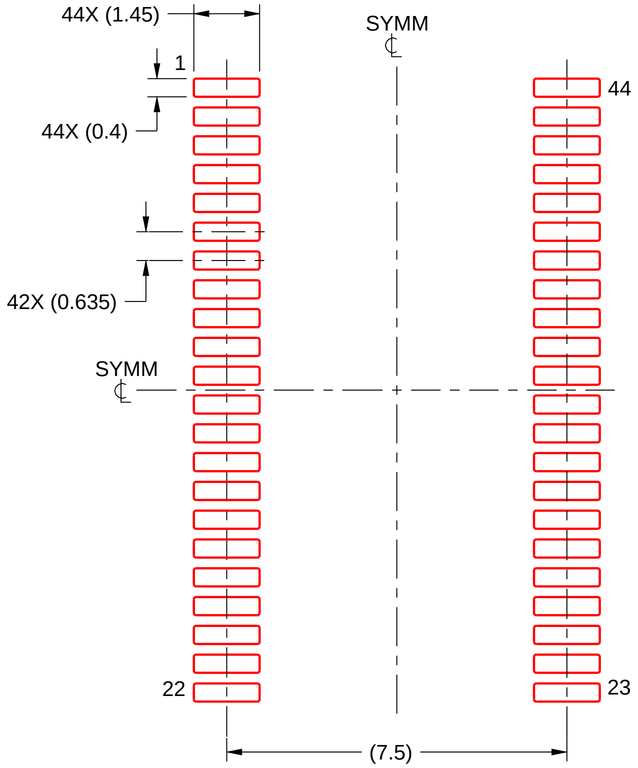


SOLDER MASK DETAILS
NOT TO SCALE

4218830/A 08/2016

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE :6X

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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