

TMUXHS4512 1.8V 6 チャンネル 20Gbps、差動 2:1 マルチプレクサ / 1:2 デマルチプレクサ

1 特長

- USB4 で最大 20Gbps、DisplayPort 1.4/2.1 で最大 UHBR20 をサポート
- 最大 20Gbps のデータ伝送能力
- 高速パスは 0V~1.0V の同相電圧範囲をサポート
- 高速データピン用に 8.8Ω (標準値) の低い R_{ON}
- 高速データピン用 13.0GHz の -3dB 差動 BW
- 優れた動的特性 (10GHz 時):
 - 挿入損失: -2.5dB
 - 反射損失: -13dB
 - クロストーク: -30dB
- すべてのサイドバンド信号は、最大 1.8V レベルのパススルーが可能で 5.5V に対応
- 1.2V、1.8V、3.3V の制御ロジックをサポート
- 1.8V の単一電源電圧
- アクティブ時 (500μA)、スタンバイ時 (2μA) の低消費電流
- 電源レールが消失 ($V_{CC} = 0V$) した場合の電流リークを防止する I_{OFF} 保護
- 温度範囲: -40°C ~ 125°C
- パッケージ: 40 ピン、3mm × 6mm、0.4mm ピッチの WQFN

2 アプリケーション

- PC とノート PC
- ゲーム、ホームシアター、エンターテインメント、TV
- データセンターおよびエンタープライズコンピューティング
- 医療用アプリケーション
- 試験および測定機器
- ファクトリオートメーション / 制御
- 航空宇宙および防衛
- 電子 POS (EPOS)
- ワイヤレスインフラ

3 概要

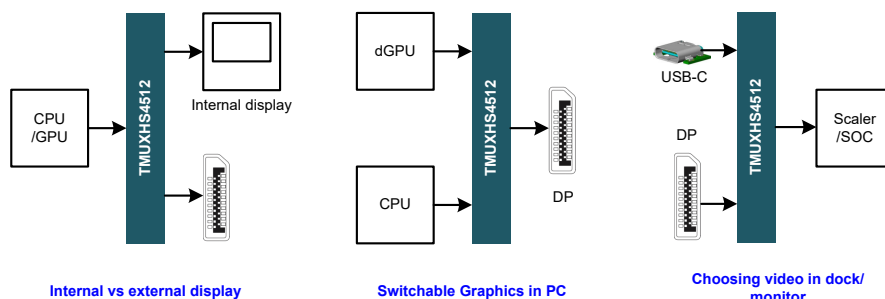
TMUXHS4512 は、マルチプレクサまたはデマルチプレクサ構成の高速、双方向パッシブスイッチです。このデバイスはプロトコルに依存せず、USB4、Thunderbolt3/4、DisplayPort 1.4/2.1 など多くのアプリケーションをサポートします。TMUXHS4512 は、最高 20Gbps のデータレートの多数の高速差動インターフェイスに使用できる汎用アナログ差動パッシブマルチプレクサ / デマルチプレクサです。TMUXHS4512 高速チャンネルは、シングルエンド信号が V_{P-N_ABSMAX} パラメータに違反しない限り、差動信号とシングルエンド信号をサポートします。サイドバンドチャンネルは 5V に対応し、I²C、UART、DisplayPort AUX、USB2 などのシングルエンド信号と差動信号をサポートしています。高速チャンネルの動的特性により、信号アイダイアグラムの最小限の減衰で高速スイッチングが可能であり、発生するジッタも非常に低いレベルに抑えられます。このデバイスのシリコン設計は、高い周波数の信号帯域でも優れた周波数応答が得られるように最適化されています。このデバイスは、Dxx データパスで 0V~1.0V の同相電圧範囲 (CMV) を持つ差動信号をサポートしています。

TMUXHS4512 は、アクティブ状態において 500μA という非常に低い消費電力を実現しています。本デバイスにはパワーダウンモードも備わっており、このモードでは、すべてのチャンネルがハイインピーダンス状態となり、デバイスはわずか 2μA の最小電力で動作します。

パッケージ情報

部品番号	温度	パッケージ ⁽¹⁾	パッケージサイズ ⁽²⁾
TMUXHS4512	$T_A = 0^{\circ}\text{C} \sim 105^{\circ}\text{C}$	RET (WQFN、40)	6mm × 3mm
TMUXHS4512I	$T_A = -40^{\circ}\text{C} \sim 125^{\circ}\text{C}$		

- (1) 供給されているすべてのパッケージについては、[セクション 11](#) を参照してください。
- (2) パッケージサイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



概略使用事例



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4 Pin Configuration and Functions

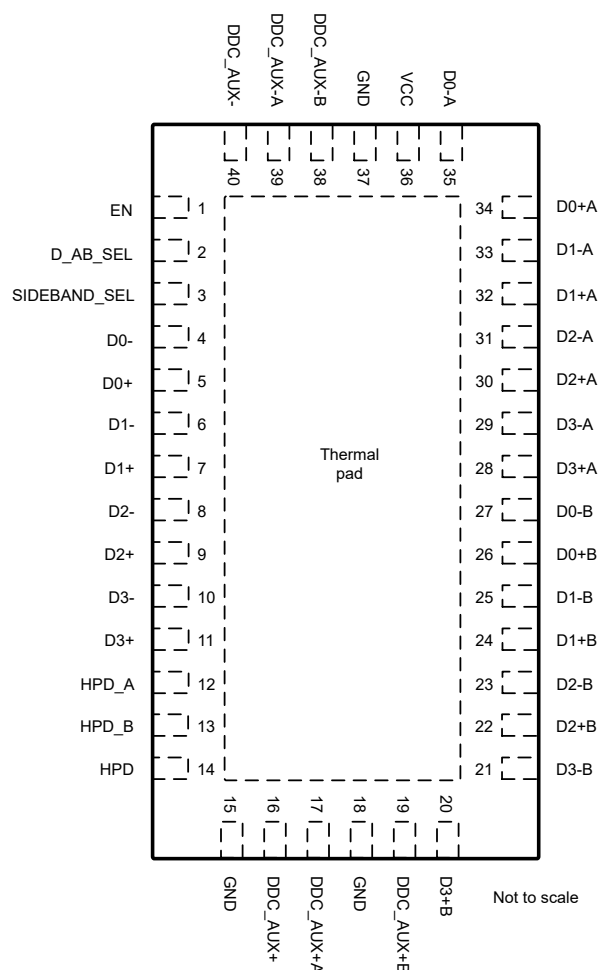


図 4-1. RET Package 40-Pin WQFN With Exposed Thermal Pad (Top View)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
EN	1	I	Device Enable L: Device Disabled. All data and sideband signals in Hi-Z. H: Device Enabled. All data and sideband signals selected by D_AB_SEL and SIDEBAND_SEL are enabled.
D_AB_SEL	2	I	Selects between high-speed datapath A and B. L: High-speed datapath A H: High-speed datapath B
SIDEBAND_SEL	3	I	Selects between sideband path A and B L: Sideband path A H: Sideband path B
D0–	4	I/O	Common Port, Channel 0, –ve signal
D0+	5	I/O	Common Port, Channel 0, +ve signal
D1–	6	I/O	Common Port, Channel 1, –ve signal
D1+	7	I/O	Common Port, Channel 1, +ve signal

表 4-1. Pin Functions (続き)

PIN		TYPE	DESCRIPTION
NAME	NO.		
D2–	8	I/O	Common Port, Channel 2, –ve signal
D2+	9	I/O	Common Port, Channel 2, +ve signal
D3–	10	I/O	Common Port, Channel 3, –ve signal
D3+	11	I/O	Common Port, Channel 3, +ve signal
HPD_A	12	I/O	Port A, Hot Plug Detect sideband signal
HPD_B	13	I/O	Port B, Hot Plug Detect sideband signal
HPD	14	I/O	Common Port, Hot Plug Detect sideband signal
GND	15	GND	Ground
DDC_AUX+	16	I/O	Common Port, DDC or AUX sideband signal
DDC_AUX+A	17	I/O	Port A, DDC or AUX sideband signal
GND	18	GND	Ground
DDC_AUX+B	19	I/O	Port B, DDC or AUX sideband signal
D3+B	20	I/O	Port B, Channel 3, +ve signal
D3–B	21	I/O	Port B, Channel 3, –ve signal
D2+B	22	I/O	Port B, Channel 2, +ve signal
D2–B	23	I/O	Port B, Channel 2, –ve signal
D1+B	24	I/O	Port B, Channel 1, +ve signal
D1–B	25	I/O	Port B, Channel 1, –ve signal
D0+B	26	I/O	Port B, Channel 0, +ve signal
D0–B	27	I/O	Port B, Channel 0, –ve signal
D3+A	28	I/O	Port A, Channel 3, +ve signal
D3–A	29	I/O	Port A, Channel 3, –ve signal
D2+A	30	I/O	Port A, Channel 2, +ve signal
D2–A	31	I/O	Port A, Channel 2, –ve signal
D1+A	32	I/O	Port A, Channel 1, +ve signal
D1–A	33	I/O	Port A, Channel 1, –ve signal
D0+A	34	I/O	Port A, Channel 0, +ve signal
D0–A	35	I/O	Port A, Channel 0, –ve signal
VCC	36	Power	Supply Voltage
GND	37	GND	Ground
DDC_AUX-B	38	I/O	Port B, DDC or AUX sideband signal
DDC_AUX-A	39	I/O	Port A, DDC or AUX sideband signal
DDC_AUX-	40	I/O	Common Port, DDC or AUX sideband signal
GND	PowerPad	GND	Ground

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC} _{ABSM} AX	Supply voltage range		−0.5	2.5	V
V _{I/O} - ABSMAX	Analog voltage range ^{(2) (3) (4)}	All high-speed data I/O pins	−0.5	4.0	V
V _{I/O} - ABSMAX	Analog voltage range ^{(2) (3) (4)}	All sideband ⁽⁵⁾ pins	−0.5	6.0	V
V _{IN} - ABSMAX	Digital input voltage range ^{(2) (3)}	All control pins ⁽⁶⁾	−0.5	5.0	V
V _P - N_ABSMAX	Absolute value of positive pin minus negative pin	All high-speed data I/O pins		0.8	V
T _{Jmax}	Maximum junction temperature TMUXHS4512		0	105	°C
T _{Jmax}	Maximum junction temperature TMUXHS4512I		−40	125	°C
T _{stg}	Storage temperature range		−65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltages are with respect to ground, unless otherwise specified.
- (3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (4) V_I and V_O are used to denote specific conditions for V_{I/O}.
- (5) Sideband pins: DDC_AUX+A, DDC_AUX-A, HPD_A, DDC_AUX+B, DDC_AUX-B, HPD_B, DDC_AUX+, DDC_AUX-, HPD
- (6) Control pins: D_AB_SEL, SIDEBAND_SEL, EN

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, ⁽¹⁾	±1500	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, ⁽²⁾	±750	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	TYP	MAX	UNIT
V _{CC}	Supply voltage	1.62	1.8	1.98	V
V _{I/O,CM}	Input/Output common mode voltage (data pins)	0		1	V
V _{I/O}	Input/Output voltage data pins	0		1.4	V
V _{I/O}	Input/Output voltage sideband ⁽²⁾ pins	0		1.8	V
V _{IN}	Digital input voltage (control ⁽³⁾ pins)	0		V _{CC}	V
DR	Data rate for differential signals			20	Gbps
T _A	Operating ambient temperature TMUXHS4512	0		105	°C
T _A	Operating ambient temperature TMUXHS4512I	−40		125	°C
T _J	Operating junction temperature TMUXHS4512	0		110	°C
T _J	Operating junction temperature TMUXHS4512I	−40		125	°C

- (1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. For more information, see [Implications of Slow or Floating CMOS Inputs](#) application note.
- (2) Sideband pins: DDC_AUX+A, DDC_AUX-A, HPD_A, DDC_AUX+B, DDC_AUX-B, HPD_B, DDC_AUX+, DDC_AUX-, HPD
- (3) Control pins: D_AB_SEL, SIDEBAND_SEL, EN

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TMUXHS4512	UNIT
		RET	
		40 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	25.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	12.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	12.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.1	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER ^{(3) (4)}			TEST CONDITIONS ⁽¹⁾	MIN	TYP ⁽²⁾	MAX	UNIT
DC Characteristics (data and sideband)							
R_{ON-D}	ON-state resistance	All data pins;	$V_{CM} = 0V$ to $1V$; $I_{I/O} = -10mA$; $V_{CC} = 1.8V \pm 10\%$; 0 to $85^{\circ}C$;	8.8	11		Ω
			$V_{CM} = 0V$ to $1V$; $I_{I/O} = -10mA$; $V_{CC} = 1.8V \pm 10\%$; -40 to $125^{\circ}C$;	8.8	12		Ω
R_{ON-SB}	ON-state resistance	All sideband pins;	$V_{I/O} = 0V$ to V_{CC} ; $I_{I/O} = -10mA$; $V_{CC} = 1.8V \pm 10\%$; 0 to $85^{\circ}C$;	8.5	12.5		Ω
			$V_{I/O} = 0V$ to V_{CC} ; $I_{I/O} = -10mA$; $V_{CC} = 1.8V \pm 10\%$; -40 to $125^{\circ}C$;	8.5	13		Ω
$R_{ON-SB-3P6V}$	ON-state resistance	All sideband pins;	$V_{I/O} = 3.6V$; $I_{I/O} = -10mA$; $V_{CC} = 1.8V \pm 10\%$; -40 to $125^{\circ}C$;	120	160		Ω
$C_{ON-SB-1M}$	Sideband ON capacitance to GND		$f = 1MHz$;		7		pF
$C_{OFF-SB-1M}$	Sideband Off capacitance to GND		$f = 1MHz$;		4.5		pF
I_{IH-D}	Input current for high-speed data pair	All selected data pins. Leakage for each high-speed pair.	$EN = H$; $V_{I/O} = 1.4V$; $V_{CC} = 1.8V \pm 10\%$;		1.5		μA
		All non-selected data pins. Leakage for each high-speed pair.	$EN = H$; $V_{I/O} = 1.4V$; $V_{CC} = 1.8V \pm 10\%$;		35		μA
I_{IH-SB}	Input current for sideband	All selected sideband pins.	$EN = H$; $V_{I/O} = 1.8V$; $V_{CC} = 1.8V \pm 10\%$;		2.5		μA
		All non-selected sideband pins.	$EN = H$; $V_{I/O} = 1.8V$; $V_{CC} = 1.8V \pm 10\%$;		1		μA
$I_{OFF-DAB}$	Leakage under power off (failsafe current)	All data pins	$V_{CC} = 0V$; $V_{I/O} = 0V$ to $1.4V$;	-8	15		μA
I_{OFF-SB}	Leakage under power off (failsafe current)	All sideband pins	$V_{CC} = 0V$; $V_{I/O} = 0V$ to $5.5V$;	-1	5		μA
Control Inputs (SIDE_BAND_SEL, D_AB_SEL, EN)							
$V_{IH-CTRL}$	High-level input voltage for control pins	Per pin for all control pins.	$V_{CC} = 1.8V \pm 10\%$;	1.0			V
$V_{IL-CTRL}$	Low-level input voltage for control pins	Per pin for all control pins.	$V_{CC} = 1.8V \pm 10\%$;		0.3		V
$I_{IH-CTRL}$	Input high leakage current for control pins	Per pin for all control pins.	$V_{CC} = 1.98V$; $V_{IN} = 1.98V$;	-0.1	0.1		μA
$I_{IL-CTRL}$	Input low leakage current for control pins	Per pin for all control pins.	$V_{CC} = 1.98V$; $V_{IN} = 0V$;	-0.1	0.1		μA
$I_{OFF-CTRL}$	Leakage under power off (failsafe current)	Per pin for all control pins.	$V_{CC} = 0V$; $V_{IN} = 0V$ or $1.98V$;	-0.1	0.1		μA
$C_{IN-CTRL}$	Input capacitance	Per pin for all control pins.	$f = 1MHz$;		5		pF
Power Supply							

over operating free-air temperature range (unless otherwise noted)

PARAMETER ^{(3) (4)}			TEST CONDITIONS ⁽¹⁾	MIN	TYP ⁽²⁾	MAX	UNIT
I _{CC}	VCC supply current in active mode	VCC supply current in active mode	EN = H; V _{CM} = 1V			500	μA
I _{CC-PD}	VCC supply current in power-down mode	VCC supply current in power-down mode	EN = L; V _{CM} = 1V		0.07	2	μA

(1) V_I, V_O, I_I, and I_O refer to data and sideband I/O pins. V_{IN} refers to the control inputs.

(2) All typical values are at V_{CC} = 1.8V (unless otherwise noted), T_A = 25°C.

(3) Sideband pins: DDC_AUX+A, DDC_AUX-A, HPD_A, DDC_AUX+B, DDC_AUX-B, HPD_B, DDC_AUX+, DDC_AUX-, HPD

(4) Control pins: D_AB_SEL, SIDEBAND_SEL, EN

5.6 High-Speed Performance Parameters

over recommended operation free-air temperature range, (unless otherwise noted). For all data pins. R_L = 50Ω where applicable.

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
BW _{SB}	Sideband pins differential bandwidth (–3dB from DC)			2.0		GHz
BW _{HS}	High-speed pins differential bandwidth (–3dB from DC)			13		GHz
IL _{DAB}	Differential insertion loss	At 100MHz; VCM = 0V;		–0.7		dB
		At 1.7GHz; VCM = 0V;		–1.0		dB
		At 2.7GHz; VCM = 0V;		–1.1		dB
		At 4.0GHz; VCM = 0V;		–1.2		dB
		At 6.0GHz; VCM = 0V;		–1.6		dB
		At 10.0GHz; VCM = 0V;		–2.5		dB
RL _{DAB}	Differential return loss	At 100MHz; VCM = 0V;		–23		dB
		At 1.7GHz; VCM = 0V;		–22		dB
		At 2.7GHz; VCM = 0V;		–20		dB
		At 4.0GHz; VCM = 0V;		–19		dB
		At 6.0GHz; VCM = 0V;		–18		dB
		At 10.0GHz; VCM = 0V;		–13		dB
Xtalk	Differential crosstalk	At 100MHz; VCM = 0V;		–66		dB
		At 1.7GHz; VCM = 0V;		–40		dB
		At 2.7GHz; VCM = 0V;		–37		dB
		At 4.0GHz; VCM = 0V;		–44		dB
		At 6.0GHz; VCM = 0V;		–45		dB
		At 10.0GHz; VCM = 0V;		–30		dB
OISO	Differential off isolation	At 100MHz; VCM = 0V;		–65		dB
		At 1.7GHz; VCM = 0V;		–37		dB
		At 2.7GHz; VCM = 0V;		–33		dB
		At 4.0GHz; VCM = 0V;		–30		dB
		At 6.0GHz; VCM = 0V;		–27		dB
		At 10.0GHz; VCM = 0V;		–23		dB

(1) All Typical Values are at V_{CC} = 1.8V (unless otherwise noted), T_A = 25°C.

5.7 Switching Characteristics

PARAMETER		MIN	TYP	MAX	UNIT
Device Switching Time					
t _{SW_POWER_ON}	Device power ON time	EN pin from L to H;		200	μs
t _{SW_POWER_OFF}	Device power OFF time	EN pin from H to L;		550	ns
High Speed Pins					
t _{PD}	Switch differential propagation delay	f = 1GHz	60		ps

PARAMETER			MIN	TYP	MAX	UNIT
t _{SW_AB}	Switching time from A to B	Measured from 50% of select to 50% of VOH/VOL			60	μs
t _{SW_BA}	Switching time from B to A	Measured from 50% of select to 50% of VOH/VOL			60	μs
t _{SK_INTRA}	Intra-pair output skew between + and - pins for same channel	f = 1GHz		1.8	6	ps
t _{SK_INTER}	Inter-pair output skew between channels	f = 1GHz			9	ps
Sideband Pins						
t _{PD-SB}	Switch single-ended propagation delay	f = 1MHz			250	ps
t _{SW-SB_AB}	Switching time from A to B	Measured from 50% of select to 50% of VOH/VOL			20	μs
t _{SW-SB_BA}	Switching time from B to A	Measured from 50% of select to 50% of VOH/VOL			20	μs
t _{SK-SB}	Output skew between DDC_AUX+ and DDC_AUX- pins	f = 1MHz			8	ps

5.8 Typical Characteristics

Data taken from a single unit under nominal power supply and temperature conditions with $V_{I/O,CM}$ at 0V.

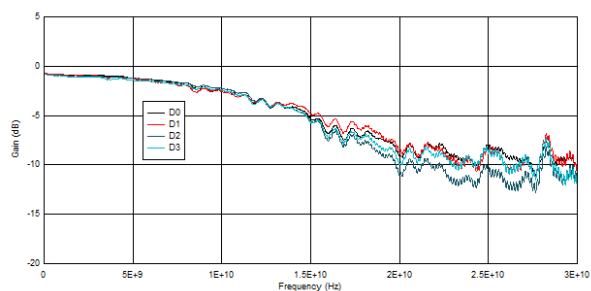


図 5-1. Differential Insertion Loss for port A

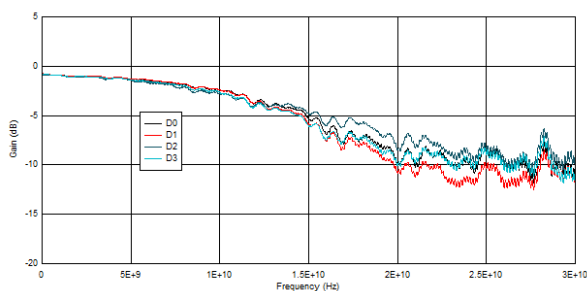


図 5-2. Differential Insertion Loss for port B

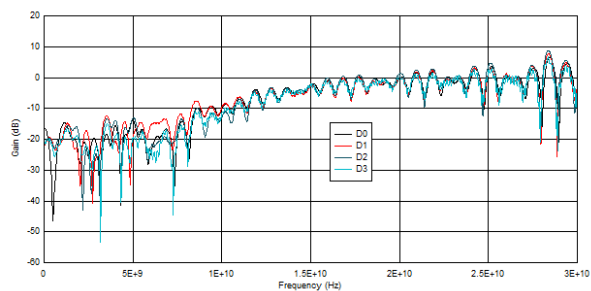


図 5-3. Input Differential Return Loss when port A is selected

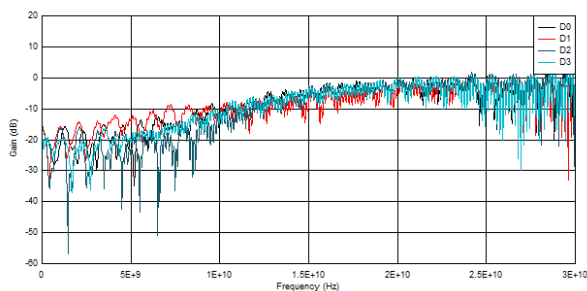


図 5-4. Output Differential Return Loss when port A is selected

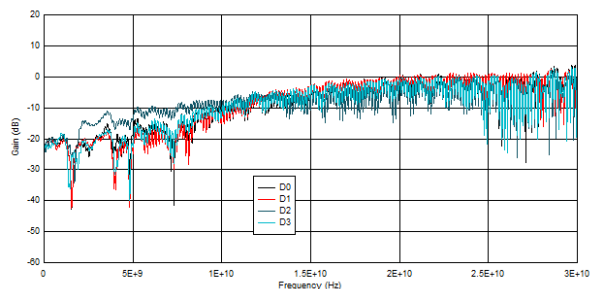


図 5-5. Output Differential Return Loss when port B is selected

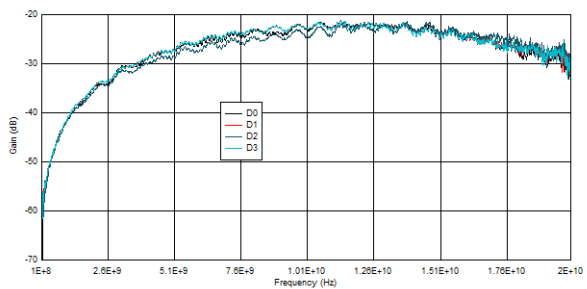


図 5-6. Off-State Isolation (OISO) for port A

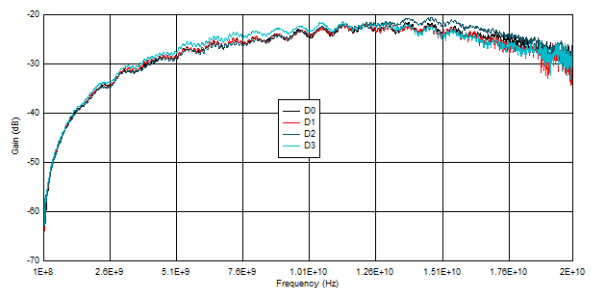


図 5-7. Off-State Isolation (OISO) for port B

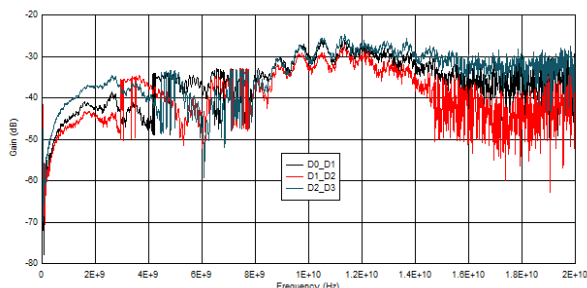
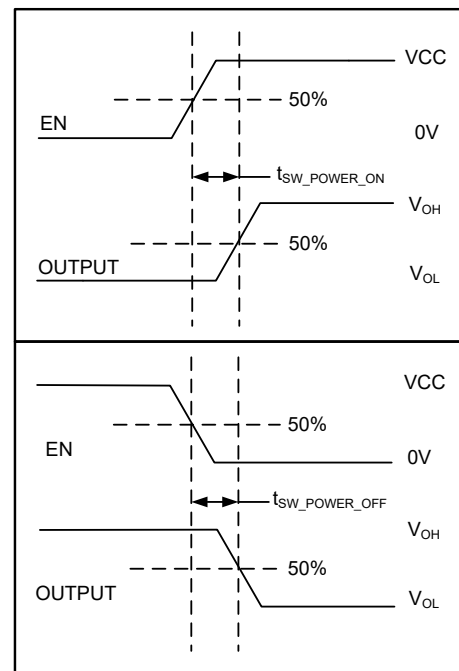
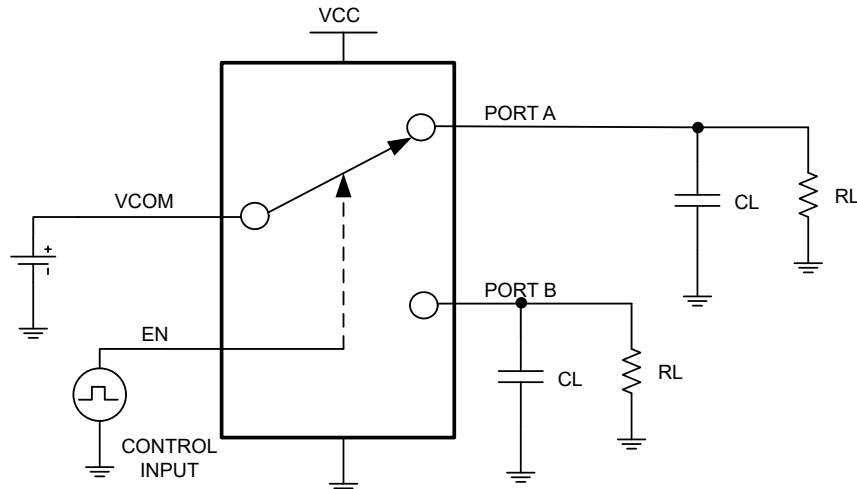


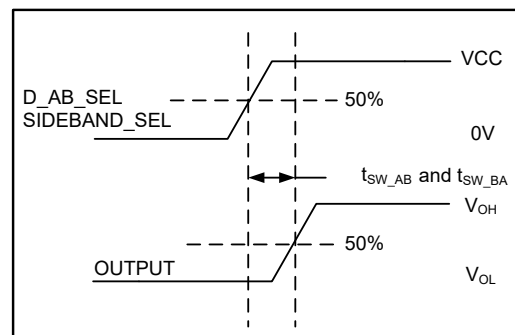
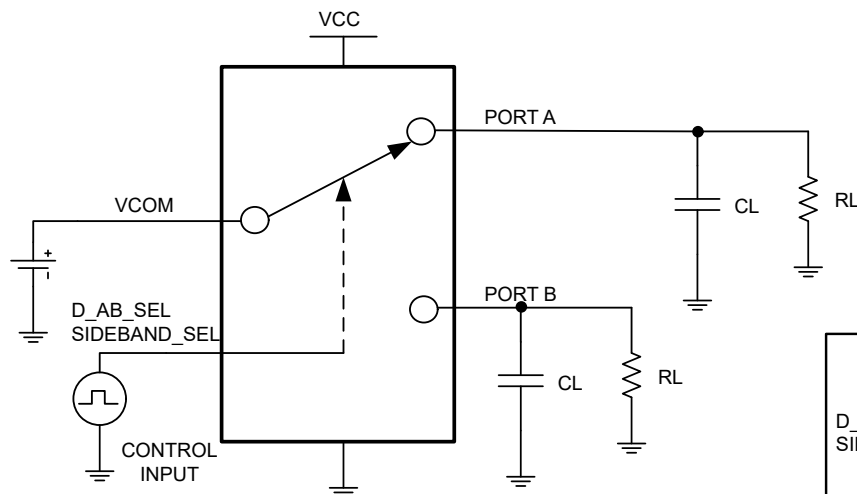
図 5-8. Crosstalk (Xtalk) between channels on common port side

6 Parameter Measurement Information



NOTE: $R_L = 10k\Omega$; $V_{COM} = V_{CC}$; $C_L = 1pF$

图 6-1. Switch Turn-On Time ($t_{SW_POWER_ON}$ and $t_{SW_POWER_OFF}$)



$R_L = 10k\Omega$; $V_{COM} = V_{CC}$; $C_L = 1pF$

图 6-2. Switching Time Between Channels (t_{SW_AB} and t_{SW_BA})

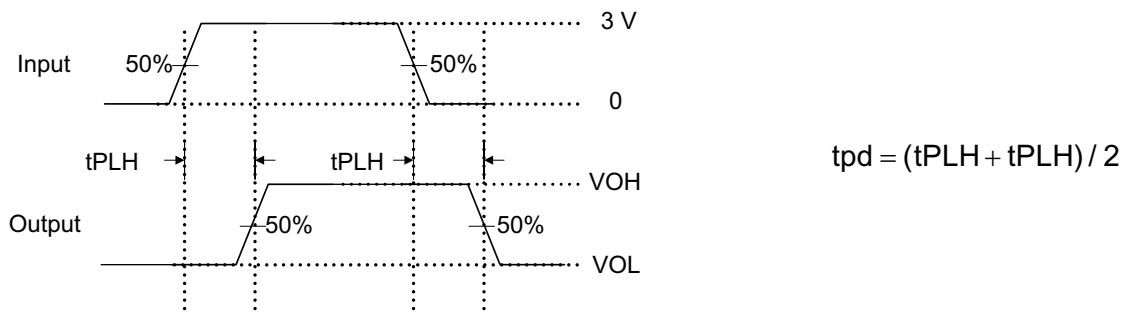


図 6-3. Propagation Delay (t_{pd})

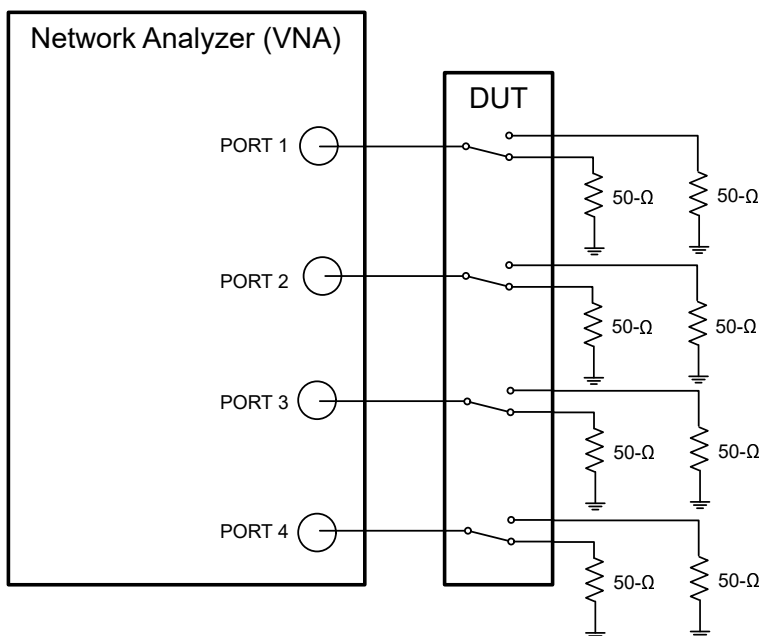


図 6-4. Crosstalk (Xtalk)

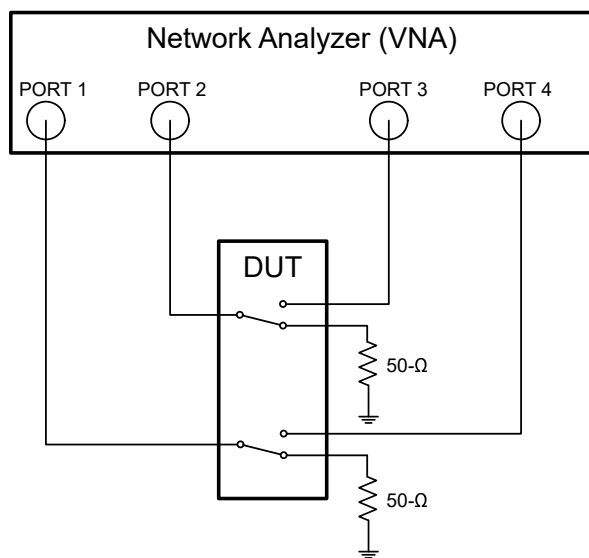
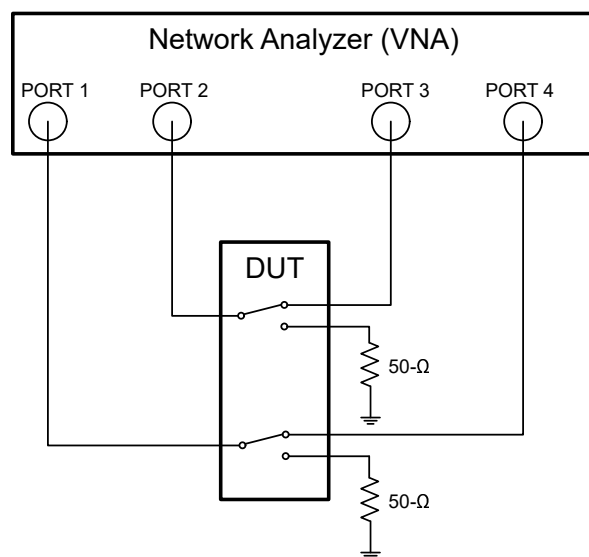


図 6-5. Differential Off-Isolation (OISO)



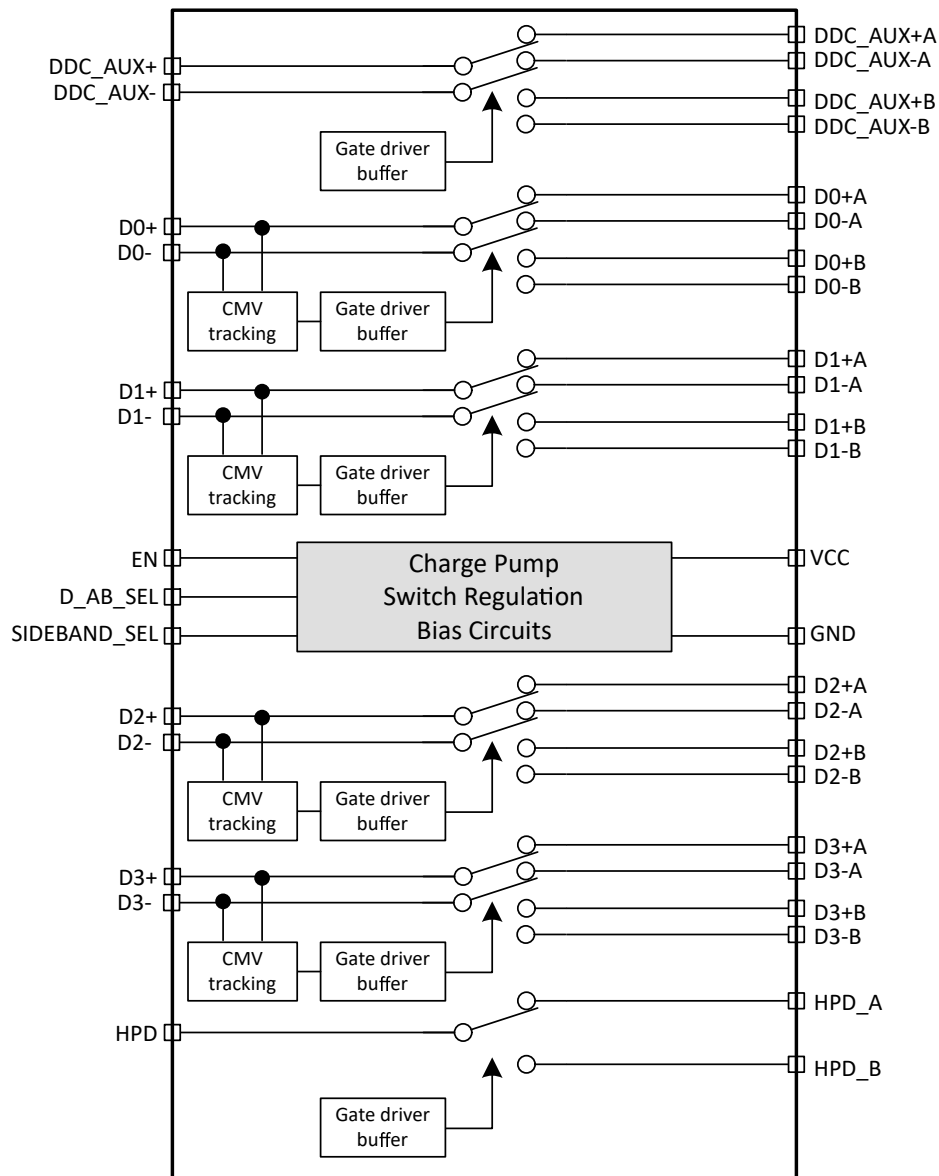
📐 6-6. Differential Bandwidth (BW), Insertion Loss, and Return Loss

7 Detailed Description

7.1 Overview

The TMUXHS4512 is a protocol agnostic bidirectional multiplexer/demultiplexer that offers low on-state resistance as well as low I/O capacitance, which allows the device to achieve a high bandwidth of 13.0GHz typical for differential channels. The TMUXHS4512 is a passive mux that is recommended for data rates up to 20Gbps. However, the device can be used for interfaces with higher data rates if overall electrical link loss permits. The high-speed data channels of the device provide the high bandwidth necessary for many interfaces to handle differential as well as single-ended signals as long as the single-ended signals do not violate V_{P-N_ABSMAX} . The high-speed channels of the device support differential signaling with common-mode voltage range (CMV) of 0V to 1.0V. The sideband channels are 5V tolerant. The sideband channels support 0V to 1.8V CMOS signals with a typical R_{ON} of 8.5Ω.

7.2 Functional Block Diagram



7.3 Feature Description

The TMUXHS4512 is based on proprietary TI technology which uses FET switches driven by a high-voltage generated from an integrated charge-pump to achieve a low on-state resistance. The TMUXHS4512's low power technology uses only 500µA in active and just 2µA in powerdown (EN = L) mode. The device has integrated ESD that can support up to 1.5kV Human-Body Model (HBM) and 750V Charge Device Model (CDM). The TMUXHS4512 also has a special feature that prevents the device from back-powering when the V_{CC} supply is not available and an analog signal is applied on the I/O pin. In this situation this special feature prevents leakage current in the device. The TMUXHS4512 is not designed for passing signals with negative swings.

7.4 Device Functional Modes

表 7-1 lists the device functions for the TMUXHS4512 device.

表 7-1. Functional Table

EN	D_AB_SEL	SIDEHAND_SEL	FUNCTION
L	X	X	Switch disabled. All channels are Hi-Z.
H	L	L	All A channels are enabled. All B channels are Hi-Z.
H	L	H	All A data high-speed channels are enabled and B sideband channels are enabled. All other channels are Hi-Z.
H	H	L	All B data high-speed channels are enabled and A sideband channels are enabled. All other channels are Hi-Z.
H	H	H	All B channels are enabled. All A channels are Hi-Z.

8 Application and Implementation

注

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8.1 Application Information

The TMUXHS4512 is a generic analog differential passive mux or demux that works for many high-speed differential interfaces with data rates up to 20Gbps. The TMUXHS4512 supports differential signaling with common-mode voltage range (CMV) of 0V to 1.0V and with differential amplitude up to 1600mVpp in Dxx channels. The device can be also used for single-ended CMOS signals with swing limited to 0V to 1.8V in sideband channels. The TMUXHS4512 can be used as mux or demux switch for:

- DisplayPort (DP) for up to UHBR20 for data rates up to 20Gbps
- USB4 and Thunderbolt (TBT) 3 or 4 for data rates up to 20Gbps

8.2 Typical Application - DisplayPort

The TMUXHS4512 can be used to switch DisplayPort signals in both source and sink applications. In source applications DisplayPort port from a graphics processor can be demultiplexed into one of the two connectors or DisplayPort sinks. In a PC the TMUXHS4512 can be used to switch integrated graphics versus discrete graphics to a connector or sink. In a sink application the device also can be used to select between two connectors or DisplayPort sources to provide DisplayPort signals into a scaler (SOC) in sink application. This section provides detailed design implementation for a sink application where TMUXHS4512 provides 2:1 demultiplexing function.

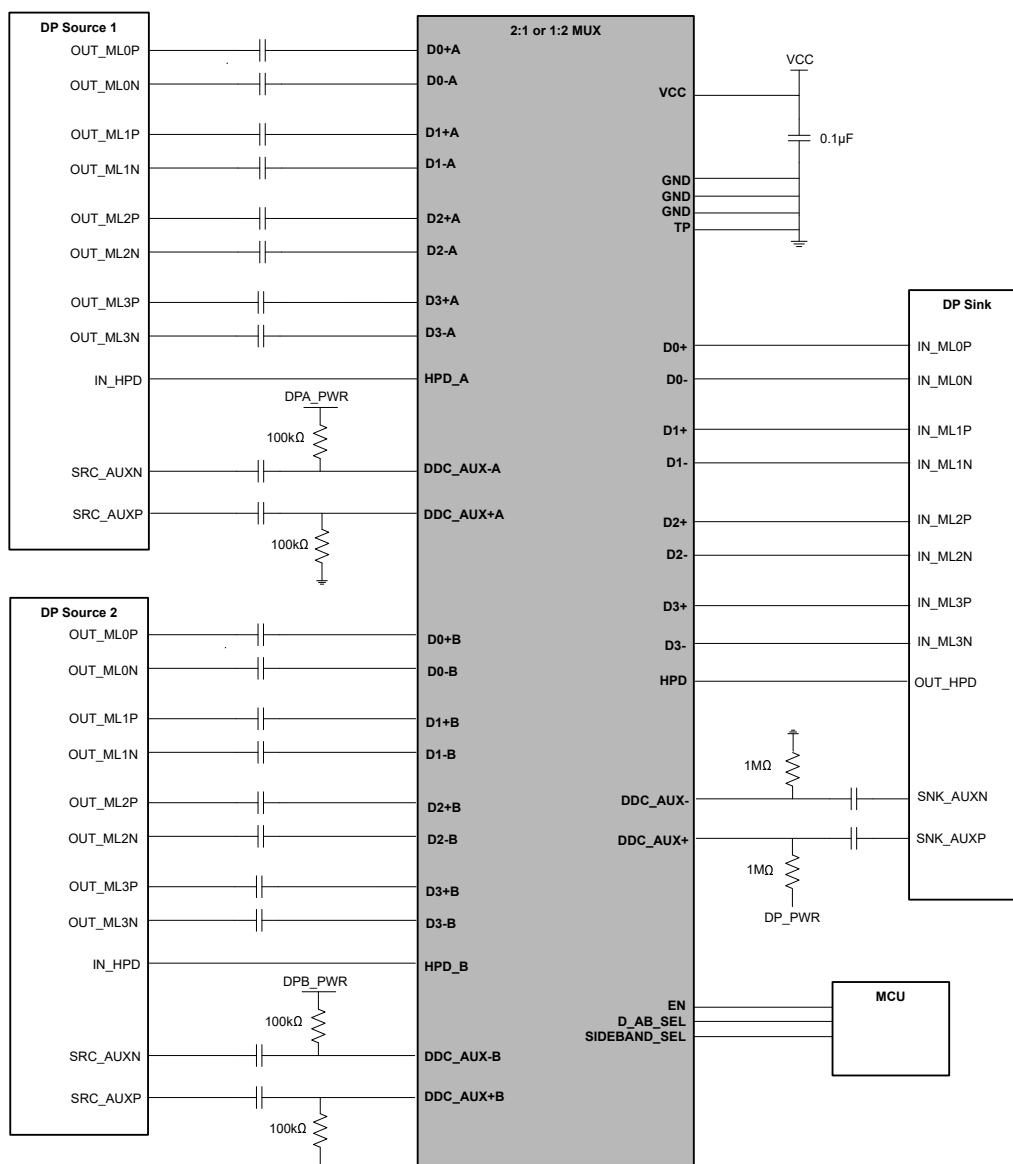


図 8-1. Choosing One of Two DisplayPorts - Application Schematic

8.2.1 Design Requirements

表 8-1 lists the design parameters for this DisplayPort example.

表 8-1. Design Parameters for DisplayPort Application

Design parameter	Example value
V _{CC}	1.62V to 1.98V
VCC decoupling capacitor	0.1μF
AUXp resistors	Sink Side: 1MΩ to 3.3V Source Side: 100kΩ to GND
AUXn resistors	Sink Side: 1MΩ to GND Source Side: 100kΩ to 3.3V

8.2.2 Detailed Design Procedure

The TMUXHS4512 is designed to operate with 1.62V to 1.98V power supply. Decoupling capacitors can be used to reduce noise and improve power supply integrity. AUX pullup resistors to 3.3V and pull-down resistors to GND must be placed on the source and sink according to DisplayPort standard.

8.2.3 Application Curves

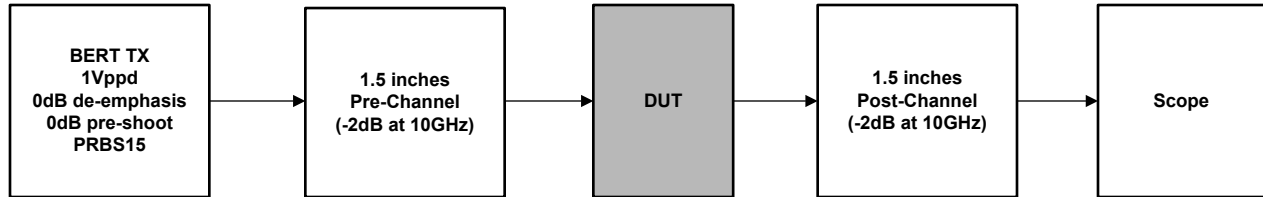


図 8-2. Test Setup

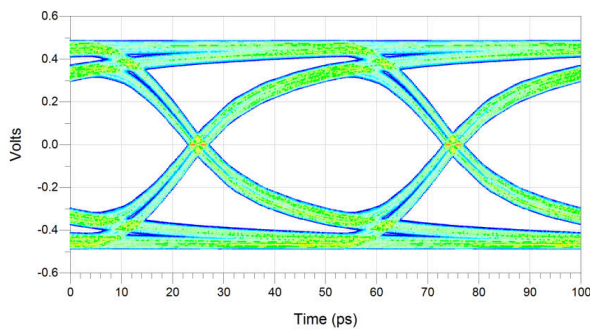


図 8-3. Eye Pattern: 20Gbps, No Device Through Path (Only One Channel Measured at a Time)

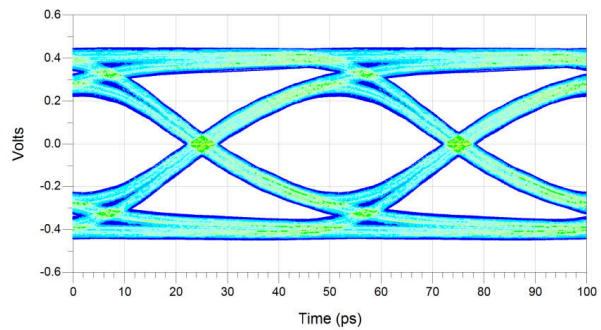


図 8-4. Eye Pattern: 20Gbps Port B, D0+ to D0+B, D0- to D0-B (Only One Channel Measured at a Time)

8.3 Power Supply Recommendations

Keep the V_{CC} in the range of 1.62V to 1.98V. Do not use voltage levels above those listed in the *Absolute Maximum Ratings* table. Use decoupling capacitors to reduce noise and improve power supply integrity. There are no power sequence requirements for the TMUXHS4512.

8.4 Layout

8.4.1 Layout Guidelines

To ensure reliability of the device, the following commonly used printed circuit board layout guidelines are recommended:

- Use decoupling capacitors between power supply pin and ground pin to ensure low impedance to reduce noise. To achieve a low impedance over a wide frequency range use capacitors with a high self-resonance frequency.
- Place ESD and EMI protection devices (if used) as close as possible to the connector.
- Use short trace lengths to avoid excessive loading.
- Keep traces at least two times the trace width apart to minimize the effects of crosstalk on adjacent traces.
- Separate high-speed signals from low-speed signals and digital from analog signals
- Avoid right-angle bends in a trace and try to route them at least with two 45° corners.
- Route the high-speed differential signal traces parallel to each other as much as possible. The traces are recommended to be symmetrical.
- Place a solid ground plane next to the high-speed signal layer. This also provides an excellent low-inductance path for the return current flow.

8.4.2 Layout Example

The TMUXHS4512 application with a single controller interfacing between a common port and two separate ports.

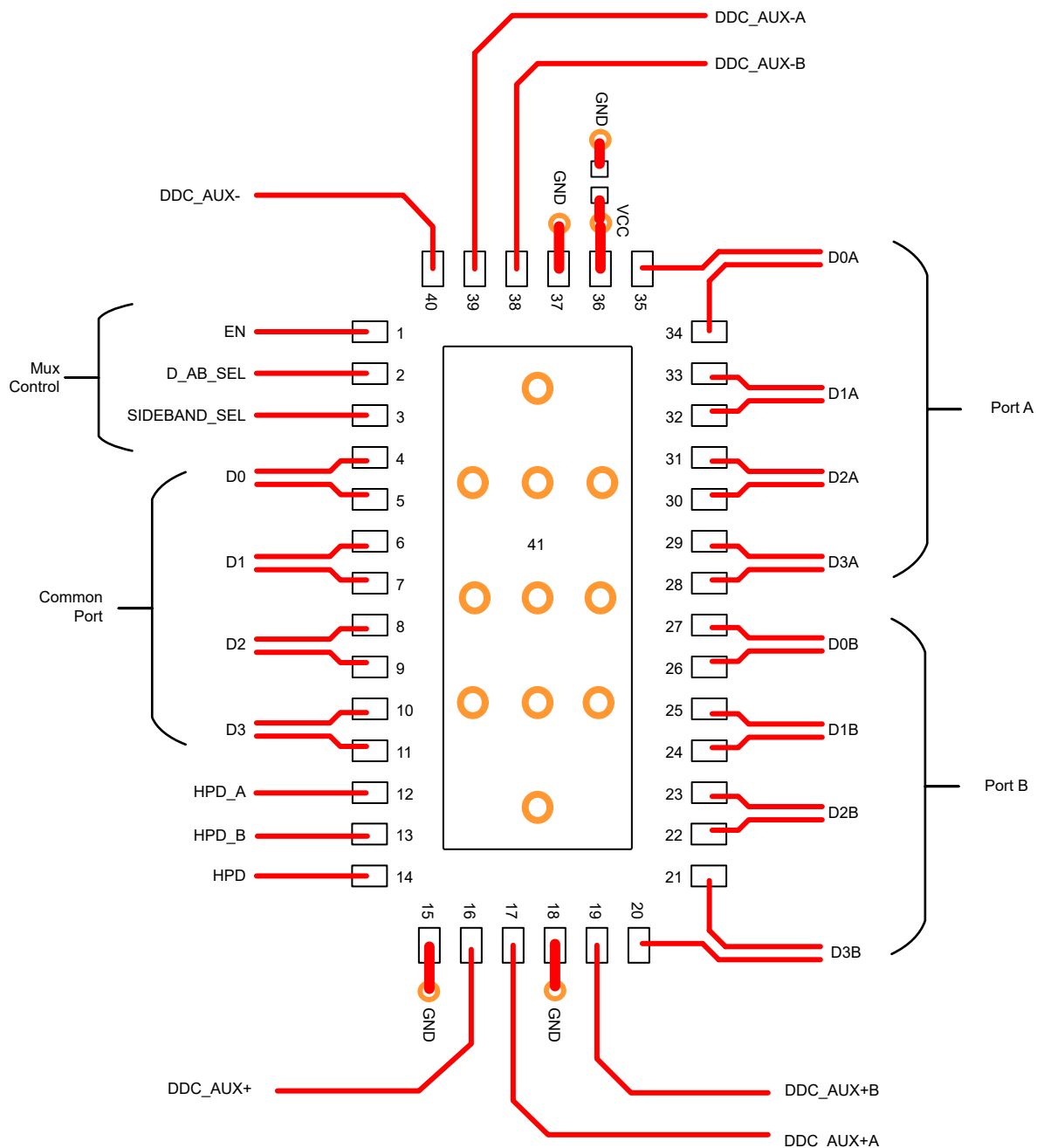


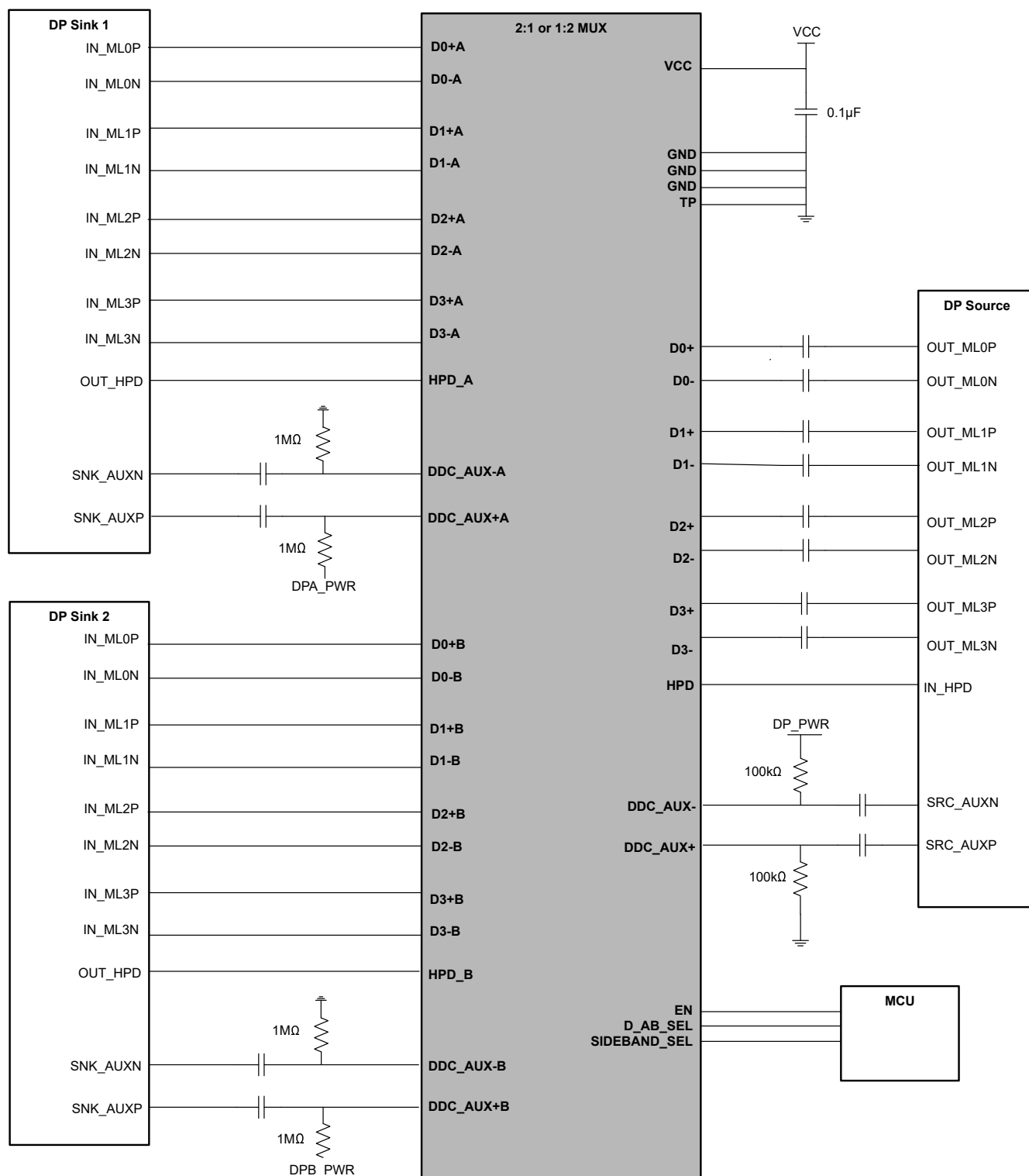
図 8-5. Layout Example

8.5 Systems Examples

8.5.1 DisplayPort 1:2 Multiplexing

The TMUXHS4512 supports AC-coupled interfaces such as DisplayPort. External AC-coupling capacitors must be used on either the common side or the non-common side of the device. In this particular example, the external AC-coupling capacitors are placed on the common side. The non-common side is DC-coupled to the DP

sinks. The choice of DC-coupling the non-common side or the common side is based on which DP source or DP sink meets the $V_{IO,CM}$ requirements of the device. If the DP source does not comply to the $V_{IO,CM}$ requirement, then place the AC-coupling capacitors between the DP source and TMUXHS4512. If the DP sink does not comply to the $V_{IO,CM}$ requirement, then place the AC-coupling capacitors between the DP sink and TMUXHS4512.



8-6. DisplayPort 1:2 Switching

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Implications of Slow or Floating CMOS Inputs application note](#).

9.2 ドキュメントの更新通知を受け取る方法

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[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
November 2024	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMUXHS4512IRETR	Active	Production	WQFN (RET) 40	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TMX412
TMUXHS4512IRETR.A	Active	Production	WQFN (RET) 40	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	See TMUXHS4512IRETR	TMX412
TMUXHS4512IRETT	Active	Production	WQFN (RET) 40	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TMX412
TMUXHS4512IRETT.A	Active	Production	WQFN (RET) 40	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	See TMUXHS4512IRETT	TMX412
TMUXHS4512RETR	Active	Production	WQFN (RET) 40	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 105	TMX412
TMUXHS4512RETR.A	Active	Production	WQFN (RET) 40	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	See TMUXHS4512RETR	TMX412
TMUXHS4512RETT	Active	Production	WQFN (RET) 40	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 105	TMX412
TMUXHS4512RETT.A	Active	Production	WQFN (RET) 40	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	See TMUXHS4512RETT	TMX412

(1) Status: For more details on status, see our [product life cycle](#).

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

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(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

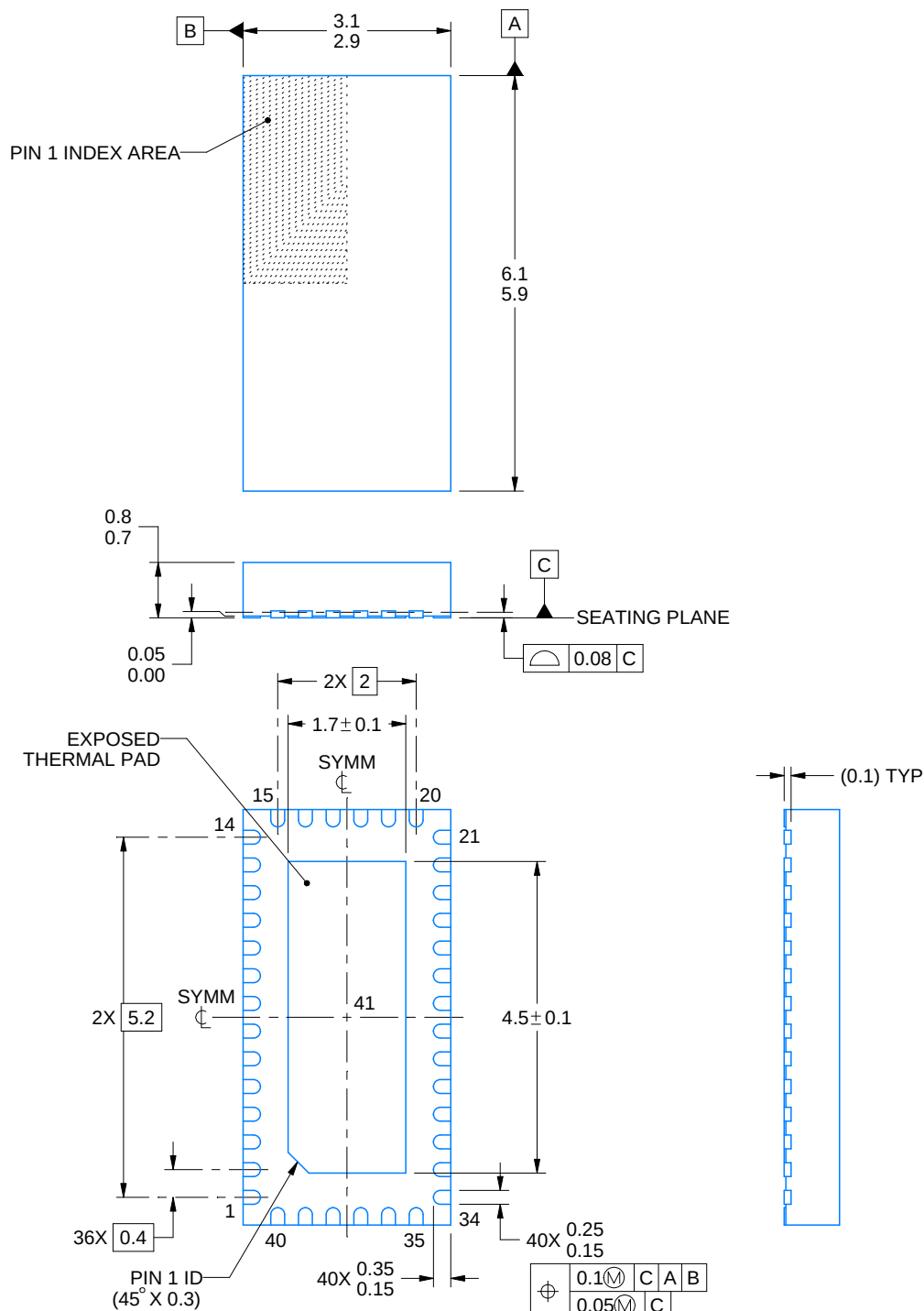
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WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4229203/A 11/2022

NOTES:

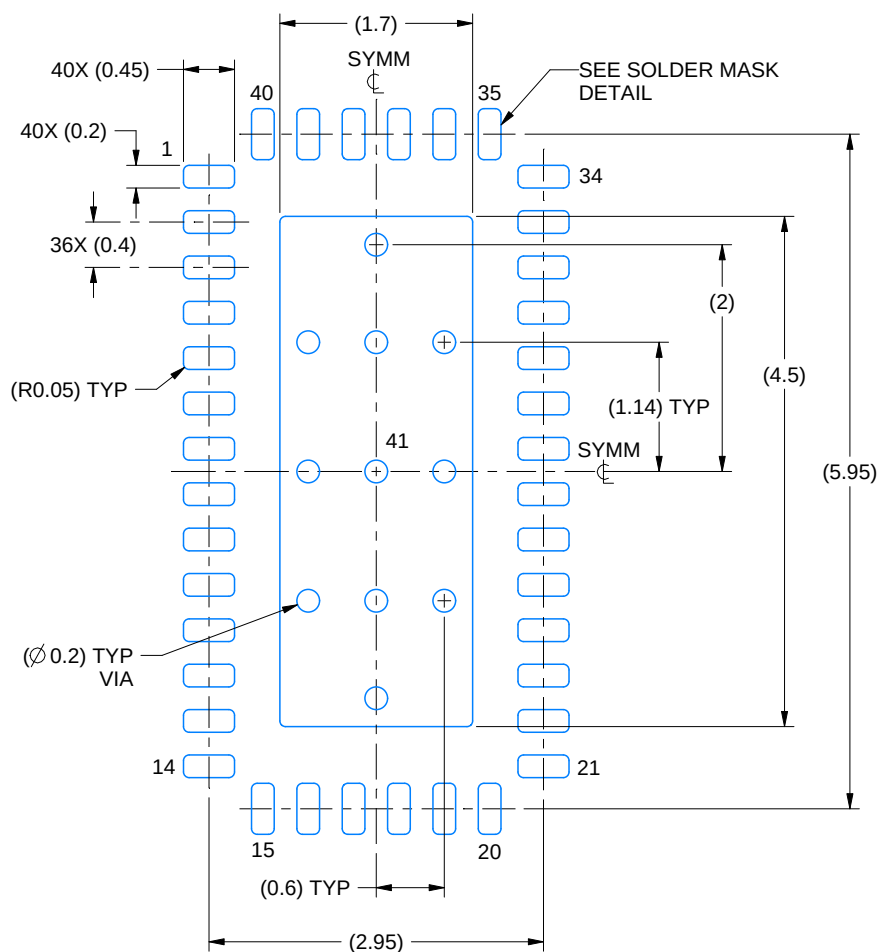
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

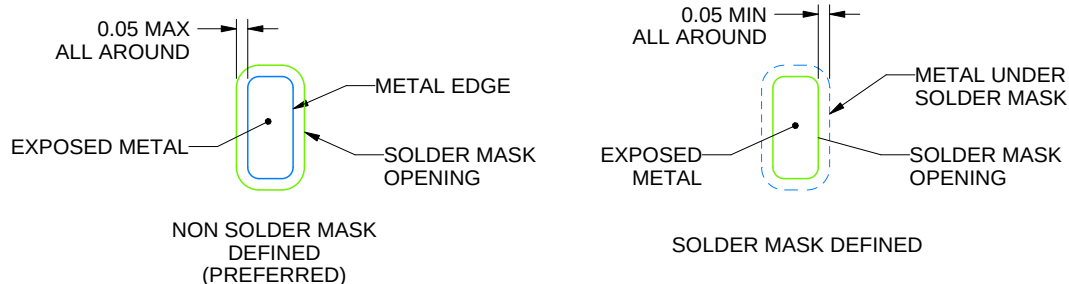
RET0040A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4229203/A 11/2022

NOTES: (continued)

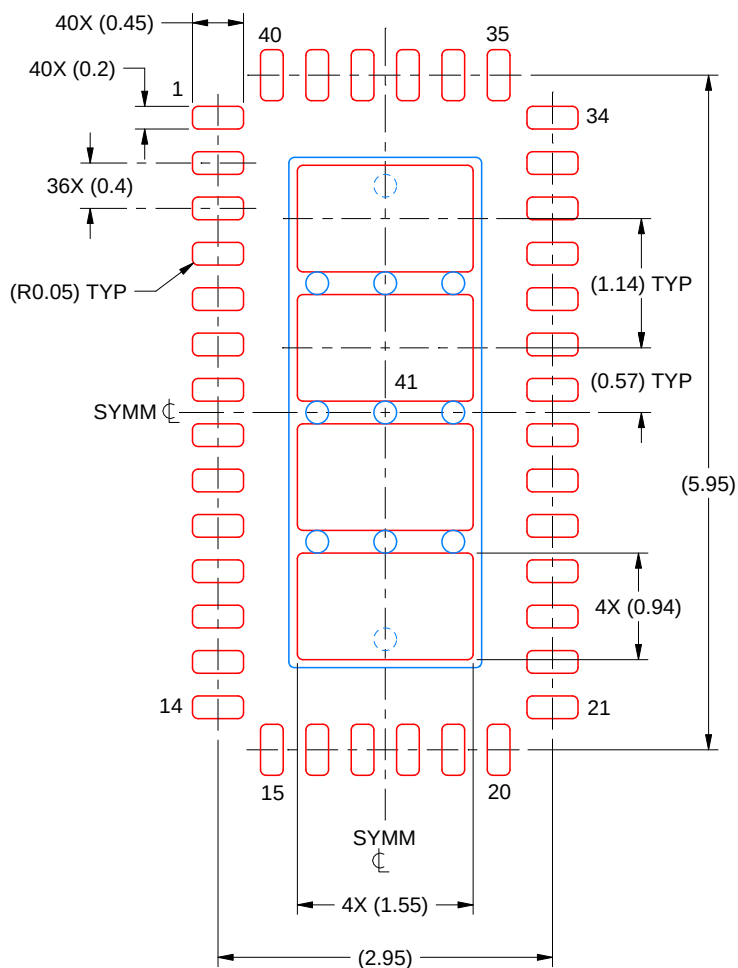
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RET0040A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 41
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4229203/A 11/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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