TEXAS INSTRUMENTS
TMUXHS4212
JAJSIE6A – MAY 2020 – REVISED MAY 2022

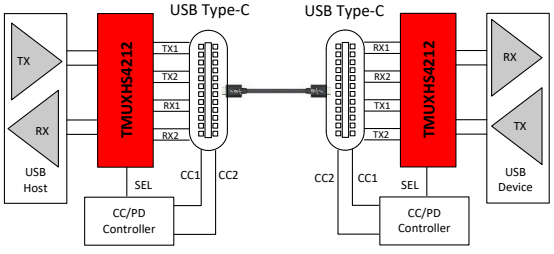
TMUXHS4212 2 チャネル差動 2:1 マルチプレクサ / 1:2 デマルチプレクサ

1 特長

- 双方向の 2:1 マルチプレクサ / 1:2 デマルチプレクサ
- 最高 10Gbps の USB 3.2 (Gen 2.0)、最高 16Gbps の PCI Express (Gen 4.0) をサポート
- SATA、SAS、Mipi® DSI/CSI、FPD-Link III、LVDS、SFI、イーサネット® インターフェイスにも対応
- 13GHz の -3dB 差動帯域幅
- 動的特性
  - 挿入損失:-1.3dB (5GHz)、-1.8dB (8GHz)
  - 反射損失:-13dB (5GHz)、-12dB (8GHz)
  - オフ・アイソレーション:-22dB (5GHz)、-20dB (8GHz)
- 適応型同相電圧トラッキング
- 0～1.8V の同相電圧をサポート
- 単一 V_{CC} 電源電圧:3.3 または 1.8V
- 超低消費電力:180µA (アクティブ時)、2µA 未満 (スタンバイ時)
- 産業用温度範囲 (–40℃～105℃) のオプション
- 2.5mm × 4.5mm の QFN パッケージで供給

2 アプリケーション

- PC とノート PC
- スマートフォン、タブレット、テレビ
- ゲーム、ホーム・シアター、およびエンターテインメント
- データ・センターおよびエンタープライズ・コンピューティング
- 医療用アプリケーション
- 試験および測定機器
- ファクトリ・オートメーション / 制御
- 航空宇宙 / 防衛
- 電子 POS (EPOS)
- ワイヤレス・インフラ



USB-C DFP Port with USB 3.2　　USB-C UFP Port with USB 3.2

3 概要

TMUXHS4212 は、マルチプレクサまたはデマルチプレクサ構成の高速、双方向パッシブ・スイッチです。USB Type-C™ や PCI Express などの多くのアプリケーションに適しています。TMUXHS4212 は、最高 16Gbps のデータ・レートの各種高速差動インターフェイスに使用できる汎用アナログ差動パッシブ・マルチプレクサ / デマルチプレクサです。電気的チャネルのシグナル・インテグリティに余裕がある場合には、さらに高いデータ・レートで使用できます。TMUXHS4212 は、同相電圧範囲 (CMV) が最大 0～1.8V、差動振幅が最大 1800mVpp の差動信号をサポートしています。適応型 CMV トラッキングにより、デバイスを通るチャネルが同相電圧範囲全体にわたって変化しないようにしています。

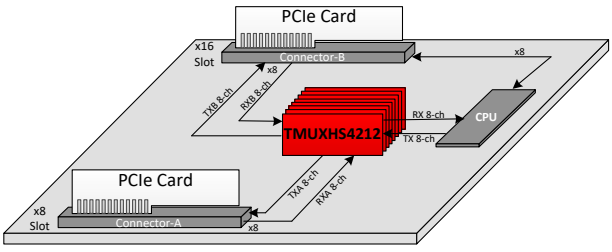
TMUXHS4212 の動的特性は、高速なスイッチング、信号アイ・ダイアグラムの減衰の最小化、超低ジッタを可能にしています。このデバイスのシリコン設計は、高い周波数の信号帯域でも優れた周波数応答が得られるように最適化されています。このデバイスのシリコン信号トレースとスイッチ・ネットワークは、最良のペア内スキュー性能が得られるように整合されています。

TMUXHS4212 は、産業用および高信頼性用途などの各種の堅牢なアプリケーションに適した拡張産業用温度範囲で動作します。

製品情報(1)

部品番号	パッケージ	本体サイズ (公称)
TMUXHS4212	VQFN (20)	2.50mm × 4.50mm、0.5mm ピッチ
TMUXHS4212I		

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



PCIe 3.0/4.0 Lane Switching

アプリケーション使用事例

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (May 2020) to Revision A (May 2022)	Page
• 文書全体にわたって表、図、相互参照の採番方法を更新	1
• 「特長」セクションの単一 V_{CC} 電源電圧を更新	1
• Updated the *RSVD1* and *RSVD2* description	3
• Changed single supply voltage V_{CC} from: *3.3 V* to: *3.3 or 1.8 V*	3

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5 Pin Configuration and Functions

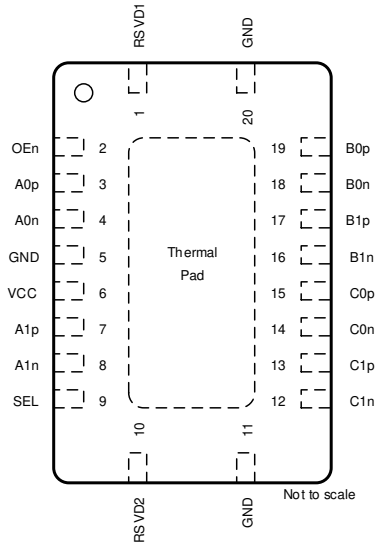

図 5-1. RKS Package, 20-Pin VQFN (Top View)

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
A0n	4	I/O	Port A, channel 0, high-speed negative signal
A0p	3	I/O	Port A, channel 0, high-speed positive signal
A1n	8	I/O	Port A, channel 1, high-speed negative signal
A1p	7	I/O	Port A, channel 1, high-speed positive signal
B0n	18	I/O	Port B, channel 0, high-speed negative signal (connector side)
B0p	19	I/O	Port B, channel 0, high-speed positive signal (connector side)
B1n	16	I/O	Port B, channel 1, high-speed negative signal
B1p	17	I/O	Port B, channel 1, high-speed positive signal
C0n	14	I/O	Port C, channel 0, high-speed negative signal
C0p	15	I/O	Port C, channel 0, high-speed positive signal
C1n	12	I/O	Port C, channel 1, high-speed negative signal
C1p	13	I/O	Port C, channel 1, high-speed positive signal
GND	5, 11, 20	G	Ground
OEn	2	I	Active-low chip enable. The pin can be connected to GND if always on functional behavior is desired. L: Normal operation, H: Shutdown. If always ON, behavior of the device is desired. The pin can be permanently connected to GND.
RSVD1	1	NA	Reserved pins. Connect both pins to V_{CC}
RSVD2	10	NA	
SEL	9	I	Port select pin. L: Port A to Port B, H: Port A to Port C
V_{CC}	6	P	3.3 V or 1.8 V power

(1) I = input, O = output, G = ground, P = power

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
$V_{CC-ABSMAX}$	Supply voltage		–0.5	4	V
$V_{HS-ABSMAX}$	Voltage	Differential I/O	–0.5	2.4	V
$V_{CTR-ABSMAX}$	Voltage	Control pins	–0.5	V_{CC}+0.4	V
T_{STG}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Theseare stress ratings only, which do not imply functional operation of the device at these or anyother conditions beyond those indicated under *Recommended OperatingConditions*. Exposure to absolute-maximum-rated conditions for extended periods mayaffect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	1.8 V mode	1.71	1.8	1.98	V
		3.3 V mode	3.0	3.3	3.6	V
$V_{CC-RAMP}$	Supply voltage ramp time		0.1		100	ms
V_{IH}	Input high voltage	SEL, OEn pins	0.75 V_{CC}			V
V_{IL}	Input low voltage	SEL, OEn pins			0.25 V_{CC}	V
V_{DIFF}	High-speed signal pins differential voltage		0		1.8	V_{pp}
V_{CM}	High speed signal pins common mode voltage	VCC 1.8 V mode	0		1.2	V
		VCC 3.3 V mode	0		1.8	V
T_A	Operating free-air/ambient temperature	TMUXHS4212	0		70	°C
		TMUXHS4212I	-40		105	°C

6.4 Thermal Information

THERMAL METRIC(1)		TMUXHS4212 RKS (VQFN) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance - High K	53.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	27.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	26.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	11.1	°C/W

(1) For more information about traditional and new thermalmetrics, see the Semiconductor and IC Package ThermalMetrics application report.

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6.5 Electrical Characteristics

over operating free-air temperature and supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Device active current	OEn = 0; 0 V ≤ V_{CM} ≤ 1.8; SEL = 0 or V_{CC}		180	250	µA
I_{STDN}	Device shutdown current	OEn = V_{CC}		2	5	µA
C_{ON}	Output ON capacitance to GND	OEn = 0			0.6	pF
R_{ON}	Output ON resistance	0 V ≤ V_{CM} ≤ 1.8 V; I_O = –8 mA		5	8.4	Ω
ΔR_{ON}	On-resistance match between pairs for the same channel at same V_{CM}, V_{CC} and T_A				0.5	Ω
R_{FLAT_ON}	On-resistance flatness R_{ON}(MAX) – R_{ON}(MIN) over V_{CM} range for the same channel at same V_{CC} and T_A				0.75	Ω
$I_{IH,CTRL}$	Input high current, control pins (SEL, OEn)	V_{IN} = V_{CC}			2	µA
$I_{IL,CTRL}$	Input low current, control pins (SEL, OEn)	V_{IN} = 0 V			1	µA
$R_{CM,HS}$	Common mode resistance to ground on Ax pins	Each pin to GND		1.0	1.6	MΩ
$I_{IH,HS,SEL}$	Input high current, high-speed pins [Ax/Bx/Cx][p/n]	V_{IN} = 1.8 V for selected port - A and B with SEL = 0, and A and C with SEL = V_{CC}			8	µA
$I_{IH,HS,NSEL}$	Input high current, high-speed pins [Ax/Bx/Cx][p/n]	V_{IN} = 1.8 V for non-selected port - C with SEL = 0, and B with SEL = V_{CC} (1)			150	µA
$I_{IL,HS}$	Input low current, high-speed pins [Ax/Bx/Cx][p/n]	V_{IN} = 0 V			1	µA
$I_{HIZ,HS}$	Leakage current through turned off switch between Ax[p/n] to [B]x[p/n] and [C]x[p/n]	OEn = VCC; Ax[p/n] = 1.8 V, [B and C]x[p/n] = 0 V and Ax[p/n] = 0 V, [B and C]x[p/n] = 1.8 V			5	µA
$R_{A,p2n}$	DC Impedance between p and n for Ax pins	OEn = 0 and V_{CC}		20		KΩ

(1) There is a 20-kΩ pull-down in non-selected port.

6.6 High-Speed Performance Parameters

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
I_L	Differential insertion loss	f = 10 MHz		-0.5		dB
		f = 2.5 GHz		-0.8		
		f = 4 GHz		-1.1		
		f = 5 GHz		-1.3		
		f = 8 GHz		-1.8		
		f = 10 GHz		-2.1		
BW	–3-dB bandwidth			13		GHz
R_L	Differential return loss	f = 10 MHz		-28		dB
		f = 2.5 GHz		-17		
		f = 4 GHz		-13		
		f = 5 GHz		-13		
		f = 8 GHz		-12		
		f = 10 GHz		-12		
O_{IRR}	Differential OFF isolation	f = 10 MHz		-55		dB
		f = 2.5 GHz		-27		
		f = 4 GHz		-24		
		f = 5 GHz		-22		
		f = 8 GHz		-20		
		f = 10 GHz		-18		
X_{TALK}	Differential crosstalk	f = 10 MHz		-65		dB
		f = 2.5 GHz		-40		
		f = 4 GHz		-35		
		f = 5 GHz		-32		
		f = 8 GHz		-30		
		f = 10 GHz		-27		

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6.6 High-Speed Performance Parameters (continued)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
SCD11,22	Mode conversion - differential to common mode	f = 5 GHz		-29		dB
SCD21,12	Mode conversion - differential to common mode	f = 5 GHz		-27		dB
SDC11,22	Mode conversion - common mode to differential	f = 5 GHz		-29		dB
SDC21,12	Mode conversion - common mode to differential	f = 5 GHz		-26		dB

6.7 Switching Characteristics

PARAMETER			MIN	TYP	MAX	UNIT
t_{PD}	Switch propagation delay	f = 1 Ghz			70	ps
$t_{SW_ON_CM_SHIFT}$	Switching time SEL-to-Switch ON	For different CMV			5	us
t_{SW_ON}	Switching time SEL-to-Switch ON	For same CMV			100	ns
$t_{SW_OFF_CM_SHIFT}$	Switching time SEL-to-Switch OFF	For different CMV			1	us
t_{SW_OFF}	Switching time SEL-to-Switch OFF	For same CMV			100	ns
t_{SK_INTRA}	Intra-pair output skew between P and N pins for same channel	f = 1 Ghz			8	ps
t_{SK_INTER}	Inter-pair output skew between channels	f = 1 Ghz			10	ps

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6.8 Typical Characteristics

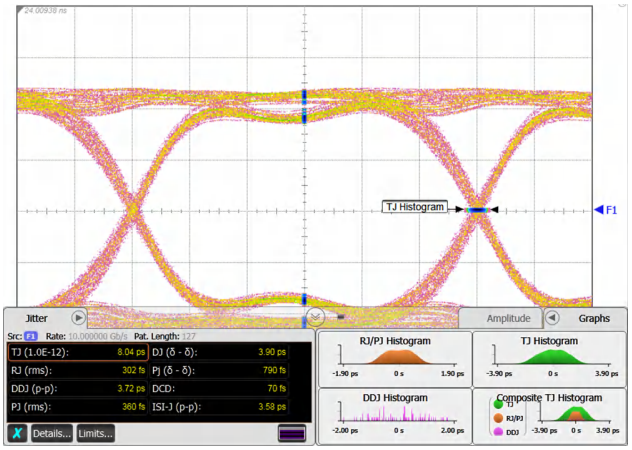

図 6-1. Jitter Decomposition of 10 Gbps PRBS-7 Signals Through Calibration Traces in TI Evaluation Board

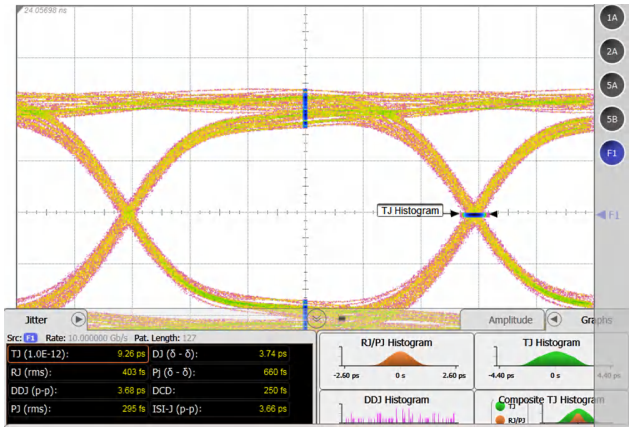

図 6-2. Jitter Decomposition of 10 Gbps PRBS-7 Signals Through a Typical TMUXHS4212 Channel in TI Evaluation Board

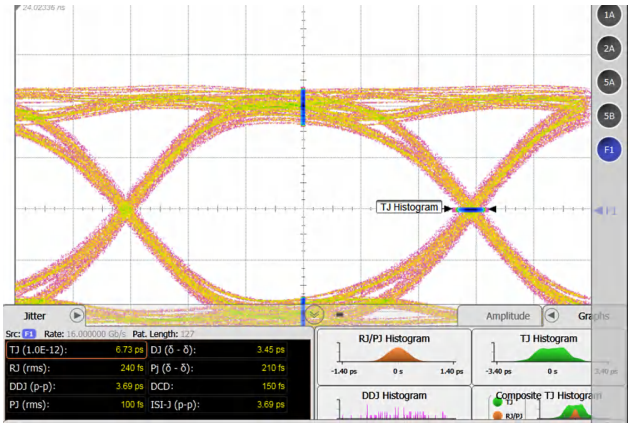

図 6-3. Jitter Decomposition of 16 Gbps PRBS-7 Signals Through Calibration Traces in TI Evaluation Board

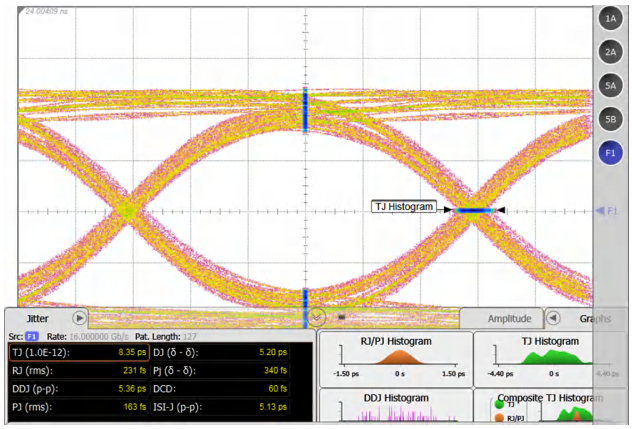

図 6-4. Jitter Decomposition of 16 Gbps PRBS-7 Signals Through a Typical TMUXHS4212 Channel in TI Evaluation Board

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7 Parameter Measurement Information

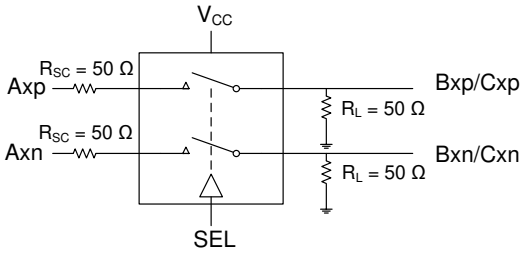

図 7-1. Test Setup

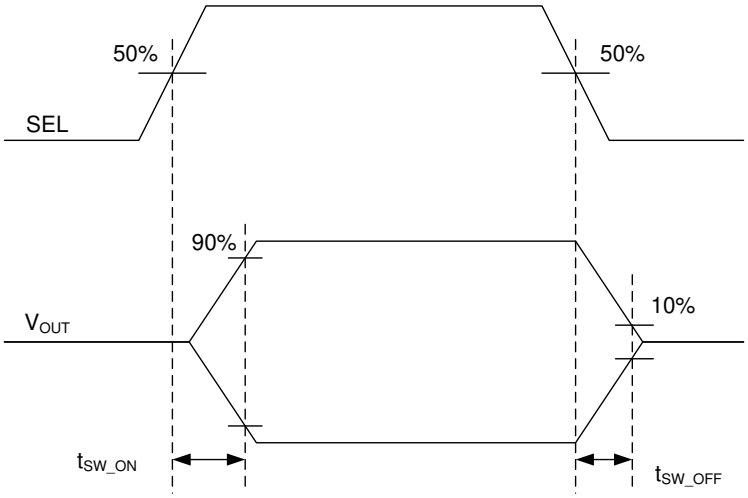

図 7-2. Switch On and Off Timing Diagram

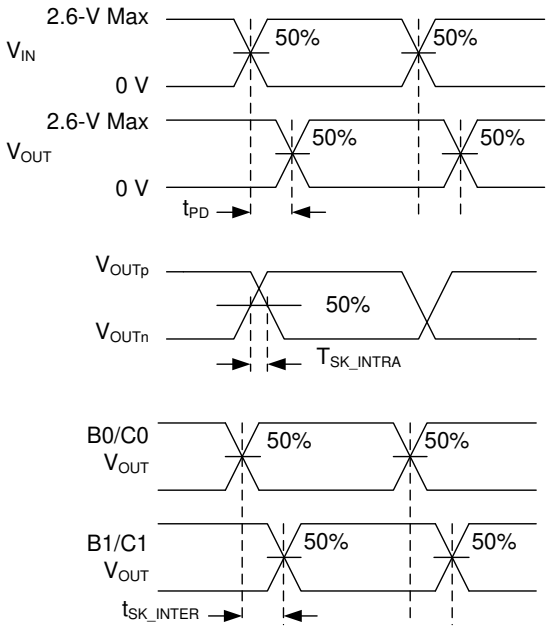

図 7-3. Timing Diagrams and Test Setup

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8 Detailed Description

8.1 Overview

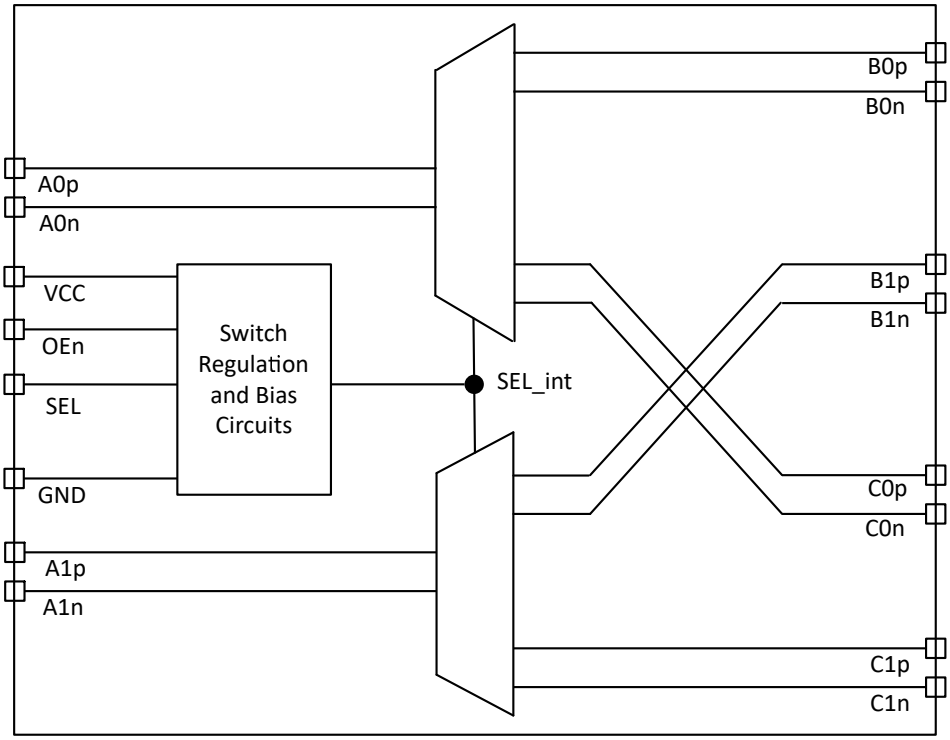
The TMUXHS4212 is a generic analog differential passive mux or demux that can work for any high-speed interface with differential signaling where common mode voltage (CMV) and differential amplitude up to 1800 mVpp. It employs adaptive input voltage tracking that ensures the channel remains unchanged for the entire common mode voltage range. Two channels of the device can be used for electrical signals that have different CMV between them. Two channels can also be used in such a way that the device switches two different interface signals with different data and electrical characteristics.

Excellent dynamic characteristics of the device allow high speed switching with minimum attenuation to the signal eye diagram with very little added jitter. While the device is recommended for the interfaces up to 16 Gbps, actual data rate where the device can be used highly depends on the electrical channels. For low loss channels where adequate margin is maintained, the device can potentially be used for higher data rates.

The TMUXHS4212 is only recommended for differential signaling. However, certain low voltage single ended signaling (such as, Mipi DPHY LP signaling) can pass through the device. It is recommended to analyze the data line biasing of the device for such single ended use cases.

The TMUXHS4212 comes in two different pinout options that provide layout implementation choices.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Output Enable and Power Savings

The TMUXHS4212 has two power modes, active/normal operating mode and standby/shutdown mode. During standby mode, the device consumes very-little current to achieve ultra low power in systems where power saving is critical. To enter standby mode, the OEn control pin is pulled high through a resistor and must remain high. For active/normal operation, the OEn control pin should be pulled low to GND or dynamically controlled to switch between H or L.

The TMUXHS4212 consumes 180 µA of power when operational and has a shutdown mode exercisable by the OEn pin resulting < 2 µA.

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8.3.2 Data Line Biasing

The TMUXHS4212 has a weak pull-down of 1 MΩ from A[0/1][p/n] pins to GND. While these resistors biases the device data channels to common mode voltage (CMV) of 0 V with very weak strength, it is recommended that the device is biased by a stronger impedance from either side of the device to a valid value in the range of 0 – 1.8 V. To avoid double biasing, ensure that the appropriate ac coupling capacitors are on either side of the device.

In certain use cases, if both sides of the TMUXHS4212 are ac coupled, then it is recommended to use appropriate CMV biasing for the device. 10 kΩ to GND or any other bias voltage in the CMV range for each A[0/1][p/n] pin will suffice for most use cases.

The high-speed data ports incorporate 20 kΩ pull-down resistors that are switched in when a port is not selected and switched out when the port is selected. For example, when SEL = L, the C[0/1][p/n] pins have 20 kΩ resistors to GND. The feature ensures that the unselected port is always biased to a known voltage for long term reliability of the device and the electrical channel.

The positive and negative terminals of data pins A[0/1] have a weak (20 kΩ) differential resistor for device switch regulation operation. This does not impact signal integrity or functionality of high speed differential signaling that typically has much stronger differential impedance (such as 100 Ω).

8.4 Device Functional Modes

表 8-1. Port Select Control Logic(1)

PORT A CHANNEL	PORT B OR PORT C CHANNEL CONNECTED TO PORT A CHANNEL	
	SEL = L	SEL = H
A0p	B0p	C0p
A0n	B0n	C0n
A1p	B1p	C1p
A1n	B1n	C1n

(1) The TMUXHS4212 can tolerate polarity inversions for all differential signals on Ports A, B, and C. Ensure that the same polarity is maintained on Port A versus Ports B or C in such flexible implementation.

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9 Application and Implementation

Note

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9.1 Application Information

The TMUXHS4212 is a generic 2-channel high-speed mux or demux type of switch that can be used for routing high-speed signals between two different locations on a circuit board. The TMUXHS4212 supports many high-speed data protocols, provided the signals' differential amplitude and common mode voltage are within <1800 mVpp and a common mode voltage is <1.8 V. The TMUXHS4212 can be used for many high speed interfaces including the following:

- Universal Serial Bus (USB) 3.2 Gen 1.0 and 2.0
- USB Type-C
- Peripheral Component Interconnect Express (PCIe™) Gen 1.0, 2.0, 3.0, and 4.0
- Serial ATA (SATA/eSATA)
- Serial Attached SCSI (SAS)
- DisplayPort (DP) 1.4 and 2.0
- Thunderbolt™ (TBT) 3.0
- Mipi Camera Serial Interface (CSI-2), Display Serial Interface (DSI)
- Low Voltage Differential Signalling (LVDS)
- Serdes Framer Interface (SFI)
- Ethernet Interfaces

The device’s mux or demux selection pin SEL can easily be controlled by an available GPIO pin of a controller or hard tie to voltage level H or L as an application requires.

The TMUXHS4212 with adaptive voltage tracking technology can support applications where the common mode is different between the RX and TX pair. The switch paths of the TMUXHS4212 have internal weak pull-down resistors of 1 MΩ on the A port pins. While these resistors bias the device data channels to common mode voltage (CMV) of 0 V with a weak strength, it is recommended that the device is biased from either side of the device to a valid value in the range of 0 – 1.8 V. It is expected that the system/host controller and Device/End point common mode bias impedances are much stronger (smaller) than the TMUXHS4212 internal pull-down resistors; therefore, they are not impacted.

Many interfaces require ac coupling between the transmitter and receiver. The 0201 or 0402 capacitors are the preferred option to provide ac coupling. Avoid the 0603 and 0805 size capacitors and C-packs. When placing ac coupling capacitors, symmetric placement is best. The capacitor value must be chosen according to the specific interface the device is being used. The value of the capacitor should match for the positive and negative signal pair. For many interfaces (such as, USB 3.2 and PCIe) the designer should place them along the TX pairs on the system board, which are usually routed on the top layer of the board. Depending upon the application and interface specifications, use the appropriate value for ac coupling capacitors.

The ac coupling capacitors have several placement options. Typical use cases warrant that the capacitors are placed on one side of the TMUXHS4212. In certain use cases, if both sides of the TMUXHS4212 are ac coupled, then it is recommended to use appropriate CMV biasing for the device. 10 kΩ to GND or any other bias voltage in the range of 0 – 1.8 V for each A[0/1][p/n] pin will suffice for most use cases. 図 9-1 shows a few placement options. Some interfaces such as USB SS and PCIe recommends ac coupling capacitors on the TX signals before it goes to a connector. Option (a) features TX ac coupling capacitors on the connector side of the TMUXHS4212. Option (b) illustrates the capacitors on the host of the TMUXHS4212. Option (c) showcases where the TMUXHS4212 is ac coupled on both sides. Range for V_{BIAS} is range of 0 – 1.8 V.

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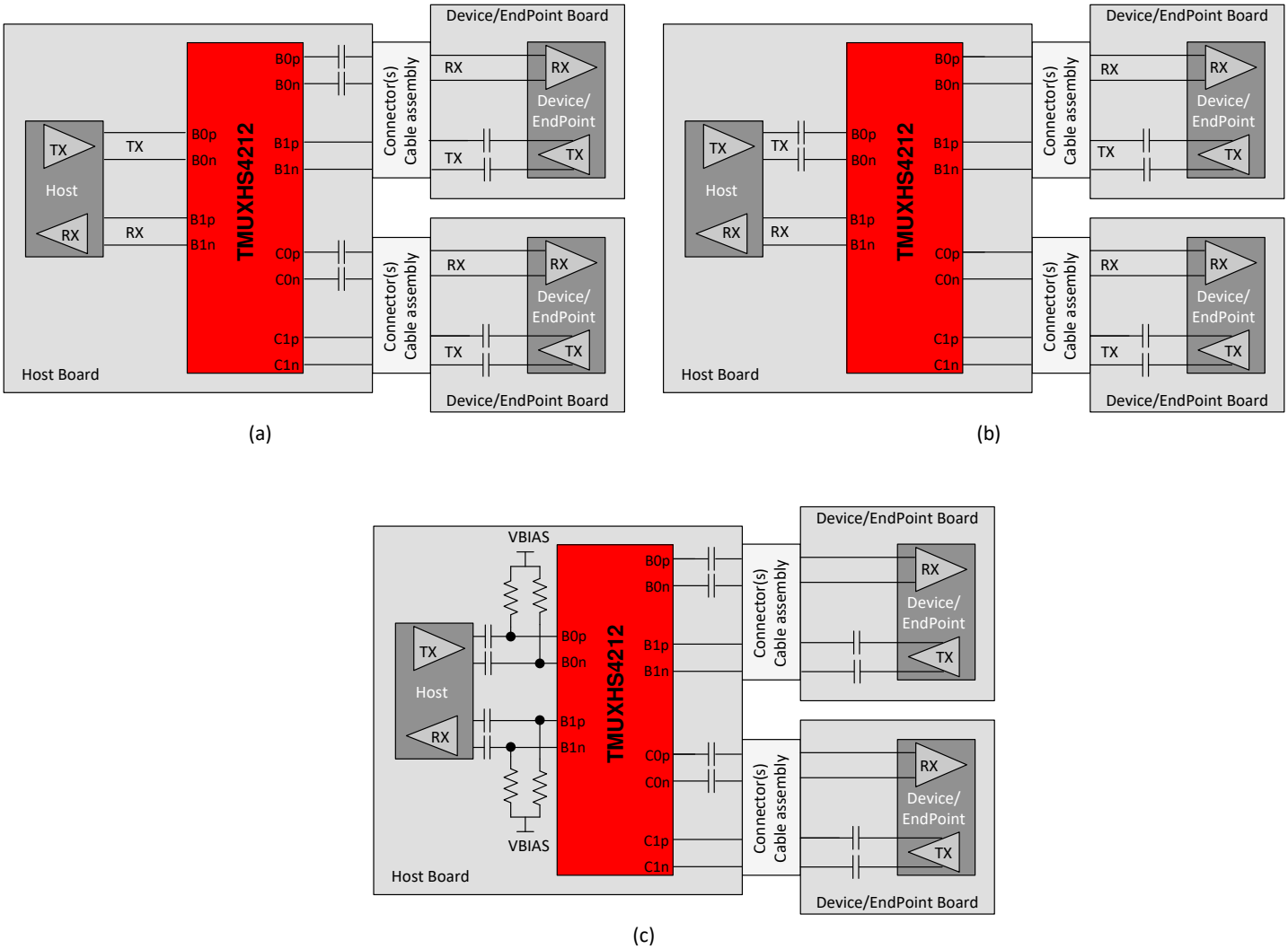

図 9-1. AC Coupling Capacitors Placement Options Between Host and Device/Endpoint Through TMUXHS4212

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9.2 Typical Applications

9.2.1 USB 3.2 Implementation for USB Type-C

The TMUXHS4212 can be used in USB Type-C implementation to mux USB 3.2 superspeed signals (TX1 and RX1 pairs versus TX2 and RX2 pairs) to accommodate plug flips. In typical use cases, the mux selection is done by a USB Type-C Channel Configuration (CC) or Power Delivery (PD) controller. The device can used on a USB Type-C DFP, UFP, or DRP port. 図 9-2 shows two USB Type-C connector applications with both a host and device side. The cable between the two connectors swivels the pairs to properly route the signals to the correct pin. The other applications are more generic because different connectors can be used.

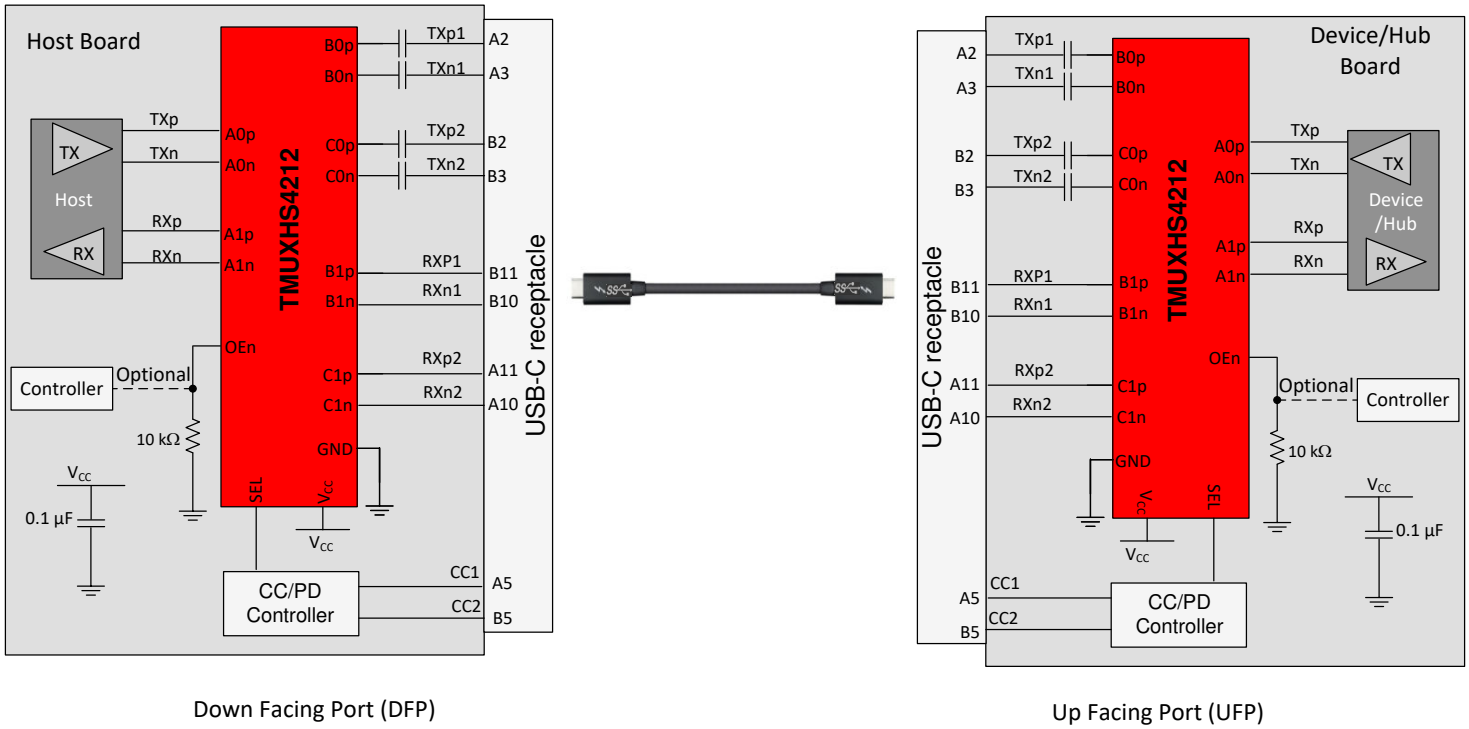

図 9-2. USB 3.2 Implementation for USB Type-C Connector

9.2.1.1 Design Requirements

The TMUXHS4212 can be designed into many different applications. All the applications have certain requirements for the system to work properly. The TMUXHS4212 requires 3.3 V ±10% V_{CC} rail. The OEn pin must be low for the device to work; otherwise, it disables the outputs. A processor can drive the OEn pin. The expectation is that one side of the device has ac coupling capacitors. 表 9-1 provides information on expected values to perform properly.

表 9-1. Design Parameters

DESIGN PARAMETER	VALUE
V_{CC}	3.3 V
AXp/n, BXp/n, CXp/n CM input voltage	0 V to 1.8 V
Control/OEn pin max voltage for low	0.5 V
Control/OEn pin min voltage for high	1.42 V
ac coupling capacitor	75 nF to 265 nF
R_{BIAS} (図 9-2) when needed	1 kΩ to 100 kΩ

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9.2.1.2 Detailed Design Procedure

The TMUXHS4212 is a high-speed passive switch device that can behave as a mux or demux. Because this is a passive switch, signal integrity is important because the device provides no signal conditioning capability. The device can support 2 to 3 inches of board trace and a connector on either end.

To design in the TMUXHS4212, the designer needs to understand the following:

- Determine the loss profile between circuits that are to be muxed or demuxed.
- Provide clean impedance and electrical length matched board traces.
- Provide a control signal for the SEL and OEn pins.
- The thermal pad must be connected to ground.
- See the application schematics on recommended decouple capacitors from V_{CC} pins to ground.

9.2.1.3 Application Curves

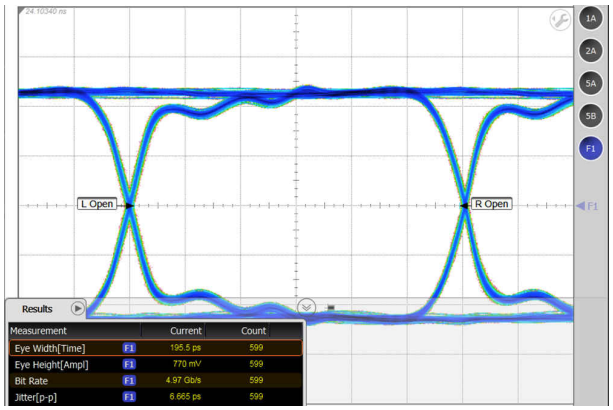

図 9-3. 5 Gbps PRBS-7 Signals Through Calibration Traces in TI Evaluation Board

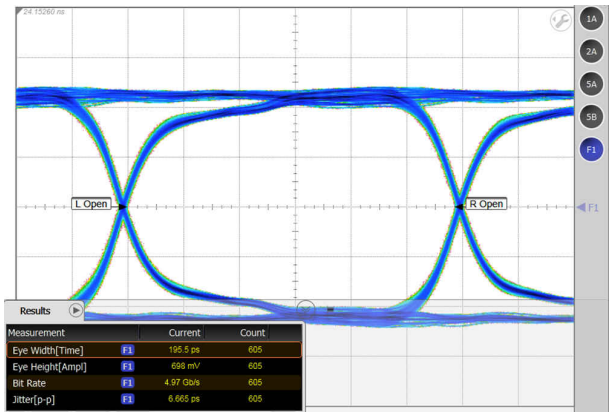

図 9-4. 5 Gbps PRBS-7 Signals Through a Typical TMUXHS4212 Channel in TI Evaluation Board

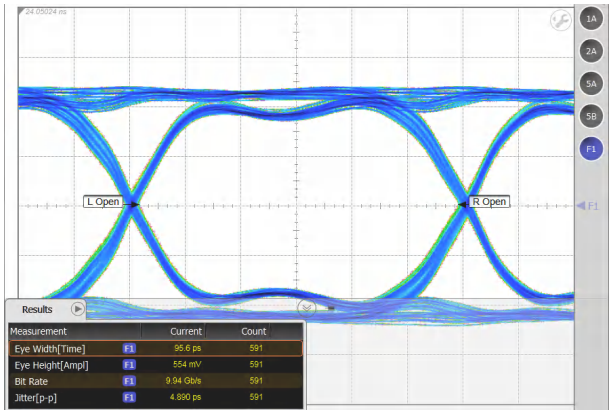

図 9-5. 10 Gbps PRBS-7 Signals Through Calibration Traces in TI Evaluation Board

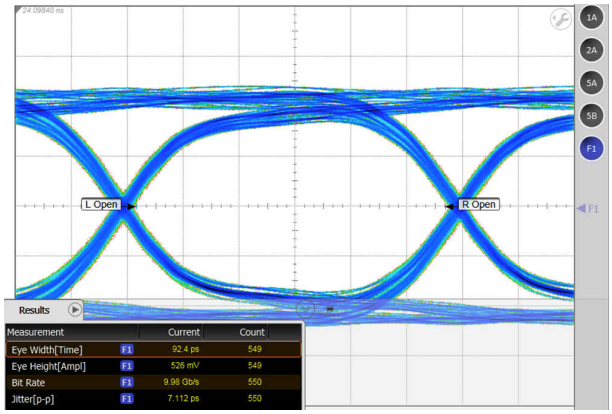

図 9-6. 10 Gbps PRBS-7 Signals Through a Typical TMUXHS4212 Channel in TI Evaluation Board

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9.2.2 PCIe Lane Muxing

The TMUXHS4212 can be used to switch PCIe lanes between two slots. In many PC and server motherboards, the CPU does not have enough PCIe lanes to provide desired system flexibility for end customers. In such applications, the TMUXHS4212 can be used to switch PCIe TX and RX lanes between two slots. 図 9-7 provides a schematic where eight TMUXHS4212 devices are used to switch eight PCIe TX and eight RX lanes. Note: the common mode voltage (CMV) bias for the TMUXHS4212 must be within the range of 0 – 1.8 V. In implementations where receiver CMV bias of a PCIe root complex or an end point can not be ensured within the CMV range, additional DC blocking capacitors and appropriate CMV biasing must be implemented.

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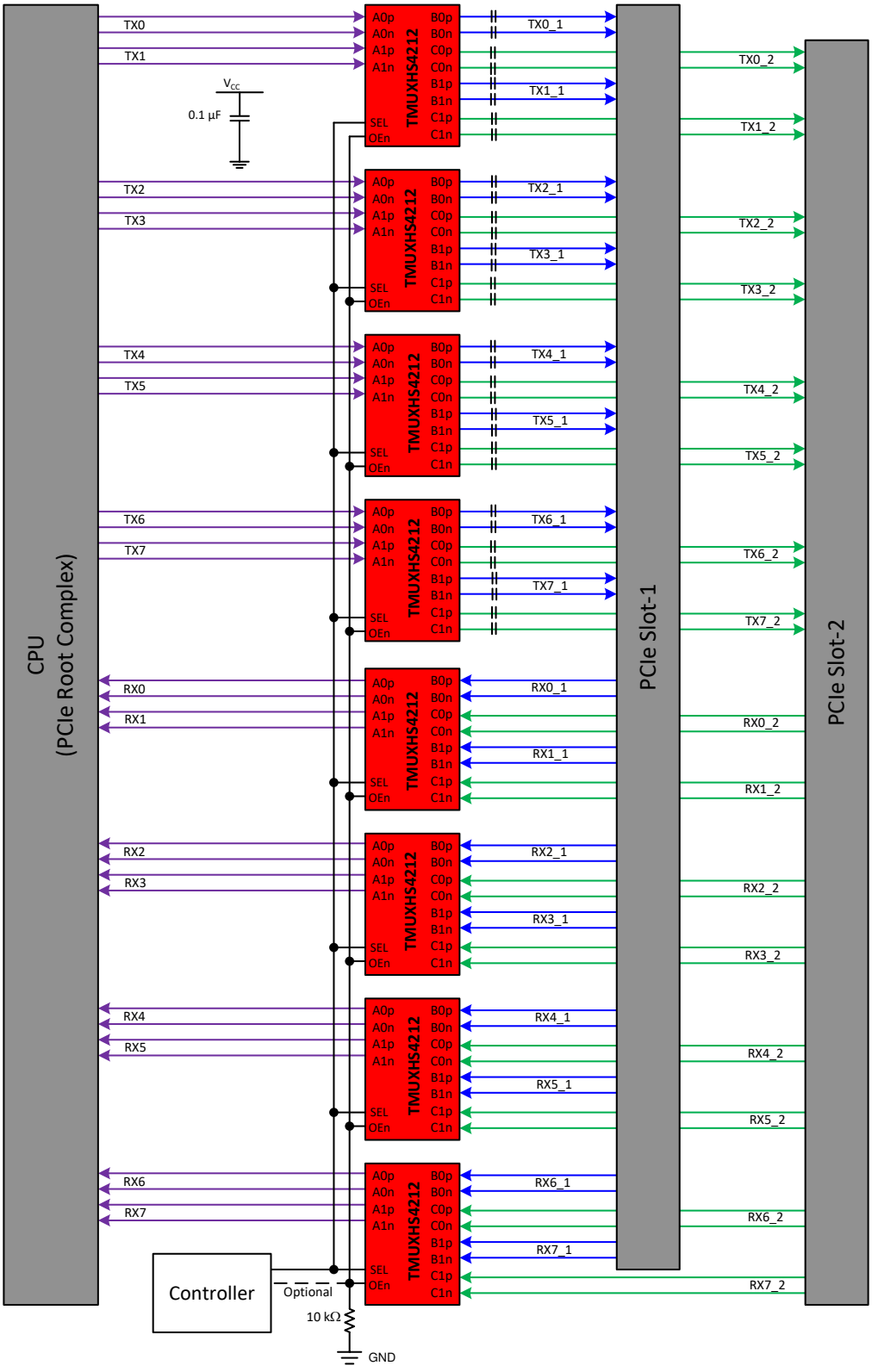

図 9-7. PCIe Lane Muxing

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9.2.2.1 Application Curves

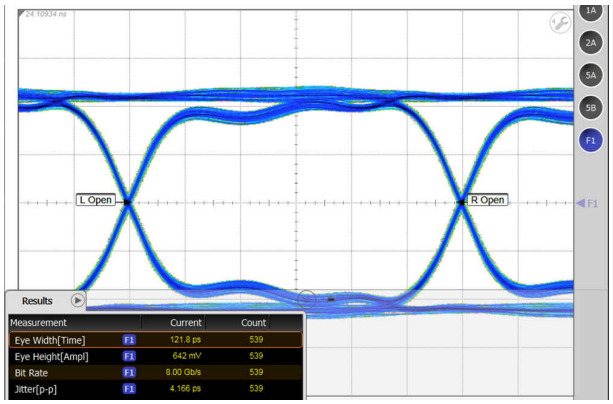

図 9-8. 8 Gbps PRBS-7 Signals Through Calibration Traces in TI Evaluation Board

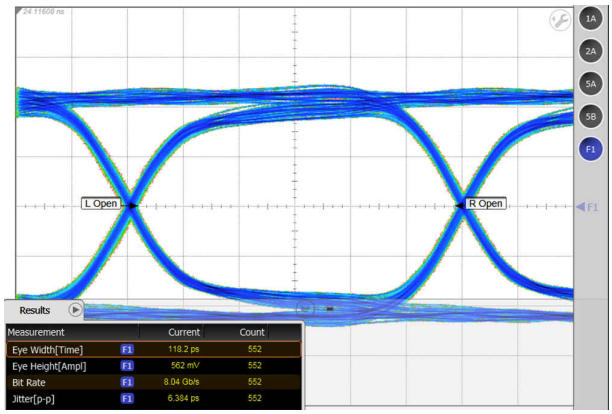

図 9-9. 8 Gbps PRBS-7 Signals Through a Typical TMUXHS4212 Channel in TI Evaluation Board

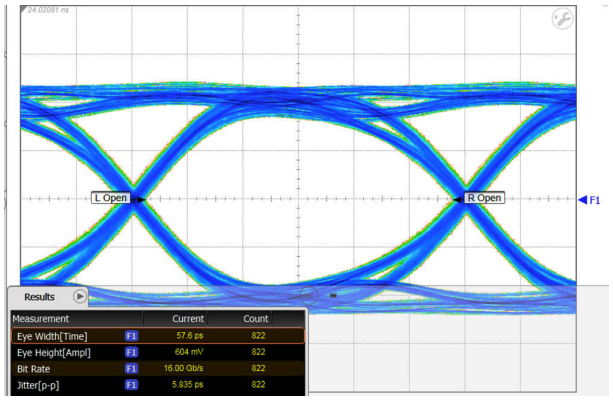

図 9-10. 16 Gbps PRBS-7 Signals Through Calibration Traces in TI Evaluation Board

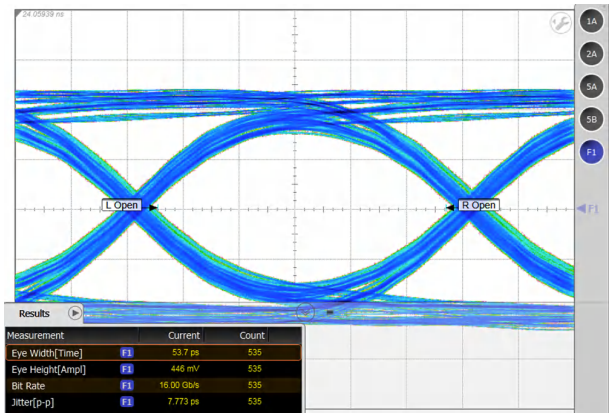

図 9-11. 16 Gbps PRBS-7 Signals Through a Typical TMUXHS4212 Channel in TI Evaluation Board

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9.3 Systems Examples

9.3.1 USB/eSATA

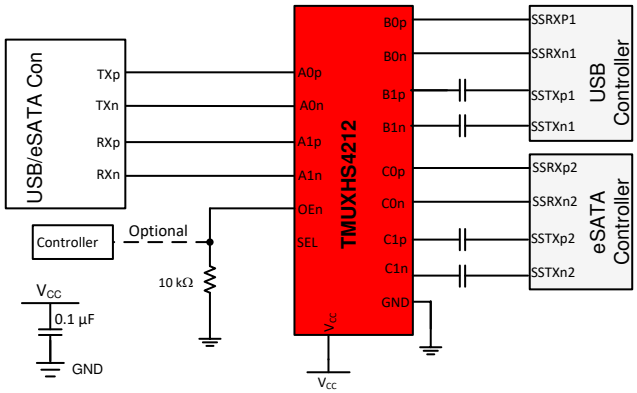

図 9-12. eSATA and USB 3.2 Combo Connector

9.3.2 MIPI Camera Serial Interface

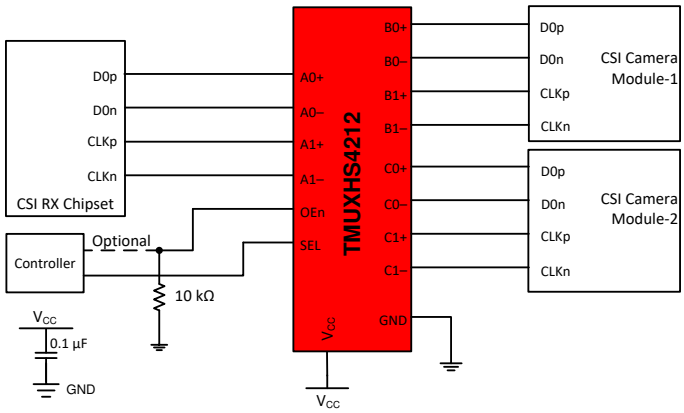

図 9-13. CSI Camera Selection

10 Power Supply Recommendations

The TMUXHS4212 does not require a power supply sequence. TI, however, recommends that OEn is asserted low after the device supply V_{CC} is stable and in specification. TI also recommends to place ample decoupling capacitors at the device V_{CC} near the pin.

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11 Layout

11.1 Layout Guidelines

On a high-K board, TI always recommends to solder the Power-pad™ onto the thermal land. A thermal land is the area of solder-tinned-copper underneath the Power-pad package. On a high-K board, the TMUXHS4212 can operate over the full temperature range by soldering the Power-pad onto the thermal land without vias.

For high speed layout guidelines, refer to *High-Speed Layout Guidelines for Signal Conditioners and USB Hubs*.

The designer must use a 1-oz Cu trace connecting the GND pins to the thermal land for the device to operate across the temperature range on a low-K board. A general PCB design guide for Power-pad packages is provided in *Power-pad Thermally-Enhanced Package*.

11.2 Layout Example

図 11-1 shows a basic layout example for the application shown in セクション 9.2.1

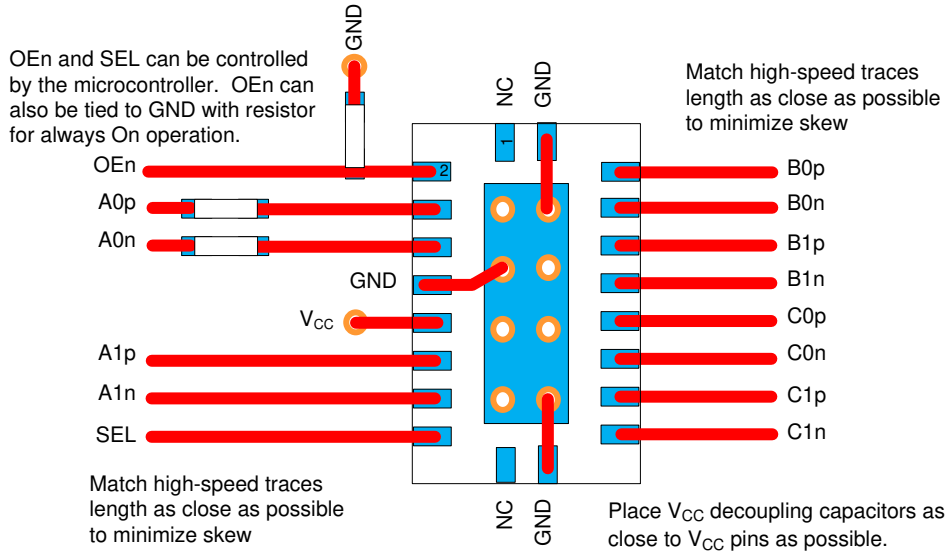

図 11-1. TMUXHS4212 Layout Example

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 サポート・リソース

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PCIe™ is a trademark of PCI-SIG.
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イーサネット® is a registered trademark of Fuji Xerox Co., Ltd.
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12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMUXHS4212IRKSR	Active	Production	VQFN (RKS) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	HS4212
TMUXHS4212IRKSR.A	Active	Production	VQFN (RKS) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	HS4212
TMUXHS4212IRKSRG4	Active	Production	VQFN (RKS) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	HS4212
TMUXHS4212IRKSRG4.A	Active	Production	VQFN (RKS) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	HS4212
TMUXHS4212IRKST	Active	Production	VQFN (RKS) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	HS4212
TMUXHS4212IRKST.A	Active	Production	VQFN (RKS) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	HS4212
TMUXHS4212RKSR	Active	Production	VQFN (RKS) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	HS4212
TMUXHS4212RKSR.A	Active	Production	VQFN (RKS) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	HS4212
TMUXHS4212RKST	Active	Production	VQFN (RKS) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	HS4212
TMUXHS4212RKST.A	Active	Production	VQFN (RKS) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	HS4212

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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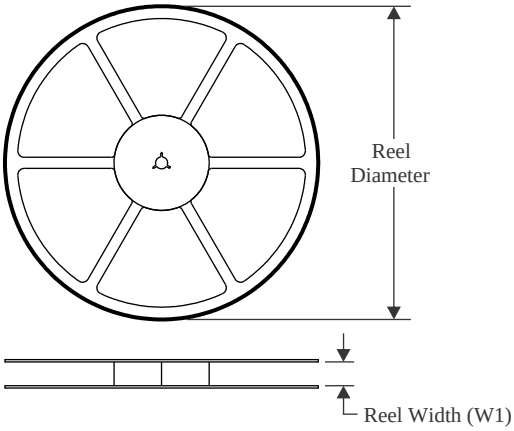
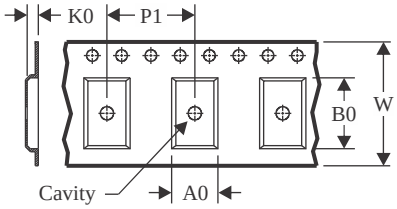
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

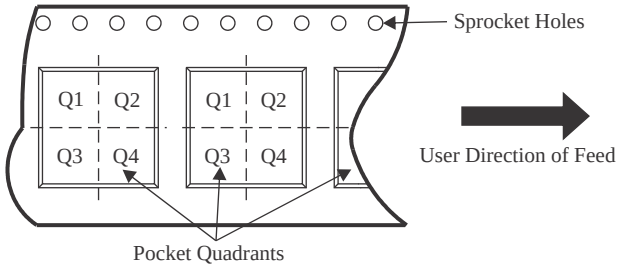


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

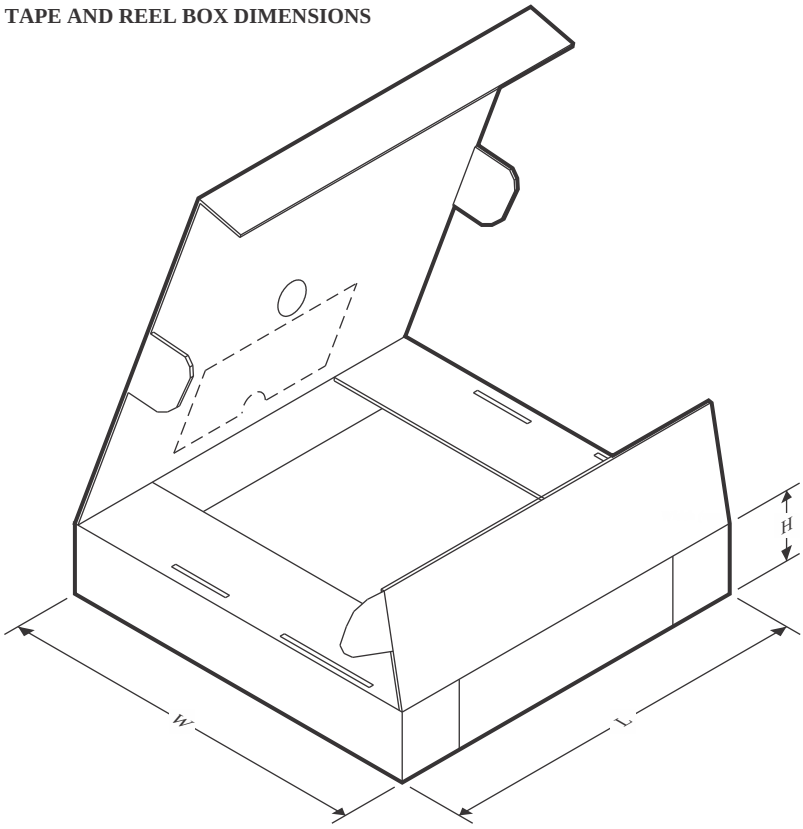
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUXHS4212IRKSR	VQFN	RKS	20	3000	180.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1
TMUXHS4212IRKSRG4	VQFN	RKS	20	3000	180.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1
TMUXHS4212IRKST	VQFN	RKS	20	250	180.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1
TMUXHS4212RKSR	VQFN	RKS	20	3000	180.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1
TMUXHS4212RKST	VQFN	RKS	20	250	180.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUXHS4212IRKSR	VQFN	RKS	20	3000	210.0	185.0	35.0
TMUXHS4212IRKSRG4	VQFN	RKS	20	3000	210.0	185.0	35.0
TMUXHS4212IRKST	VQFN	RKS	20	250	210.0	185.0	35.0
TMUXHS4212RKSR	VQFN	RKS	20	3000	210.0	185.0	35.0
TMUXHS4212RKST	VQFN	RKS	20	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

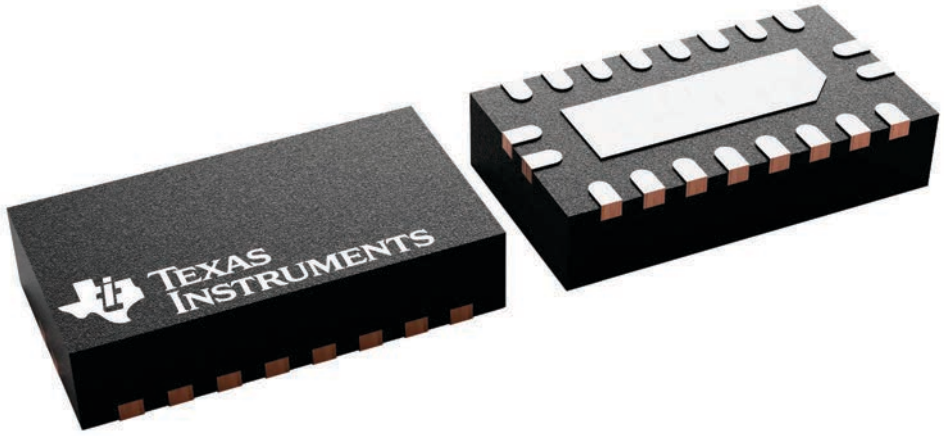
RKS 20

VQFN - 1 mm max height

2.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



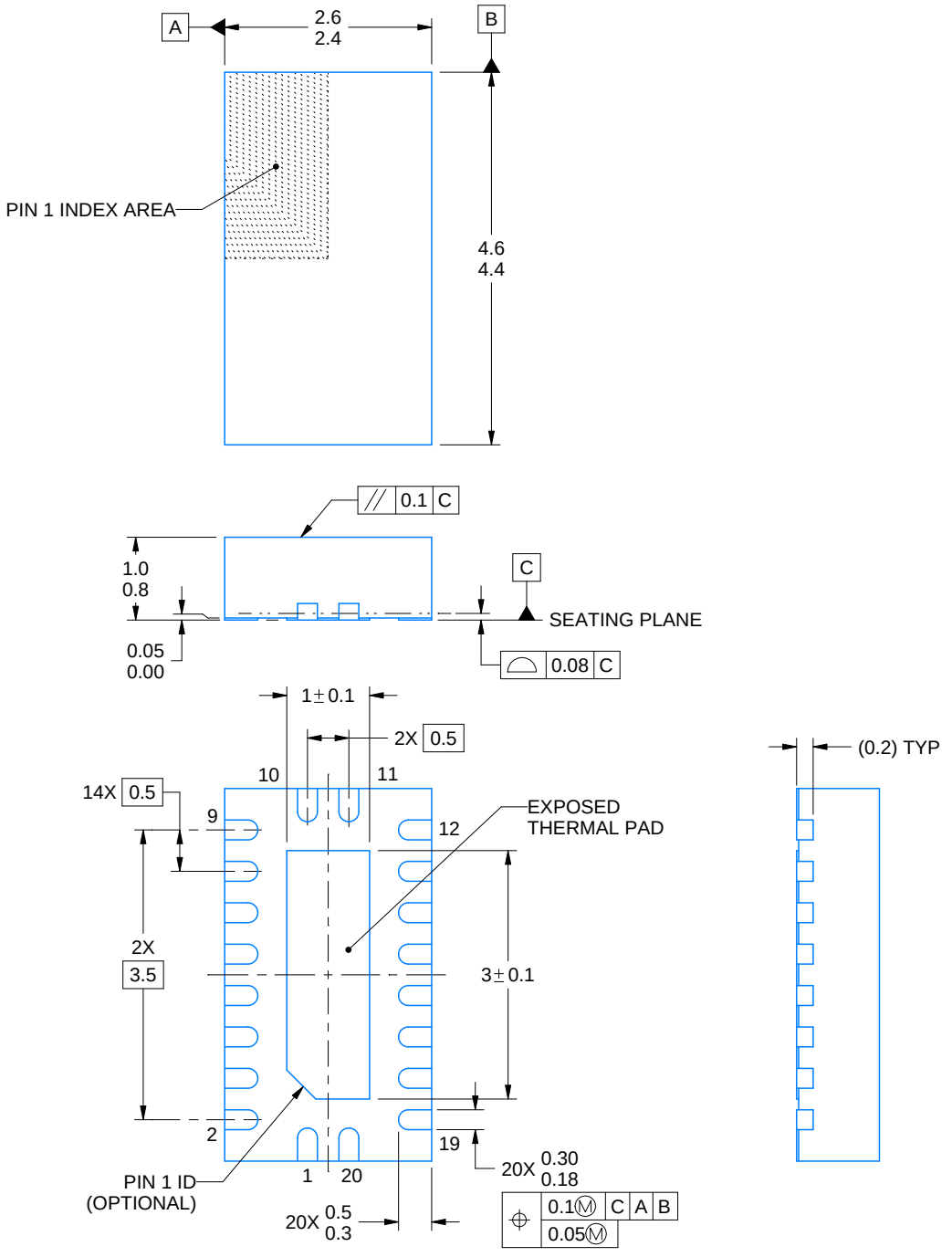
4226872/A

PACKAGE OUTLINE

RKS0020A

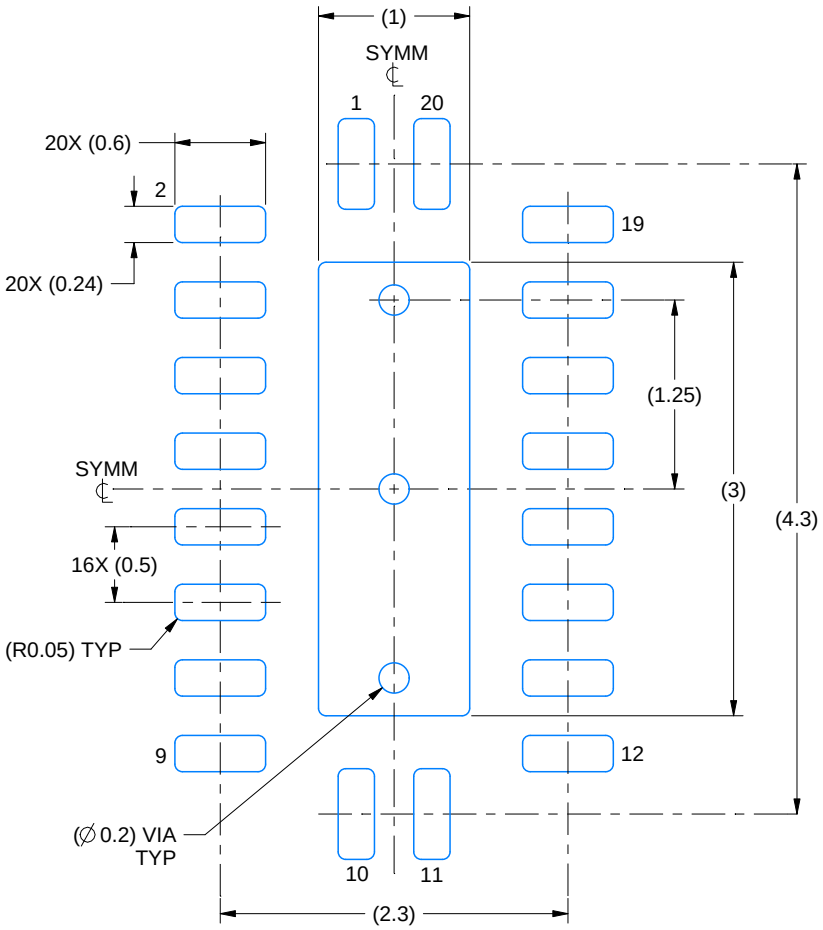
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

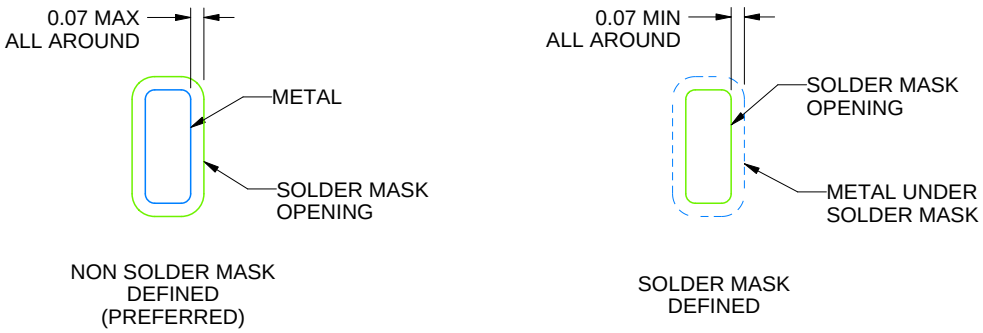


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

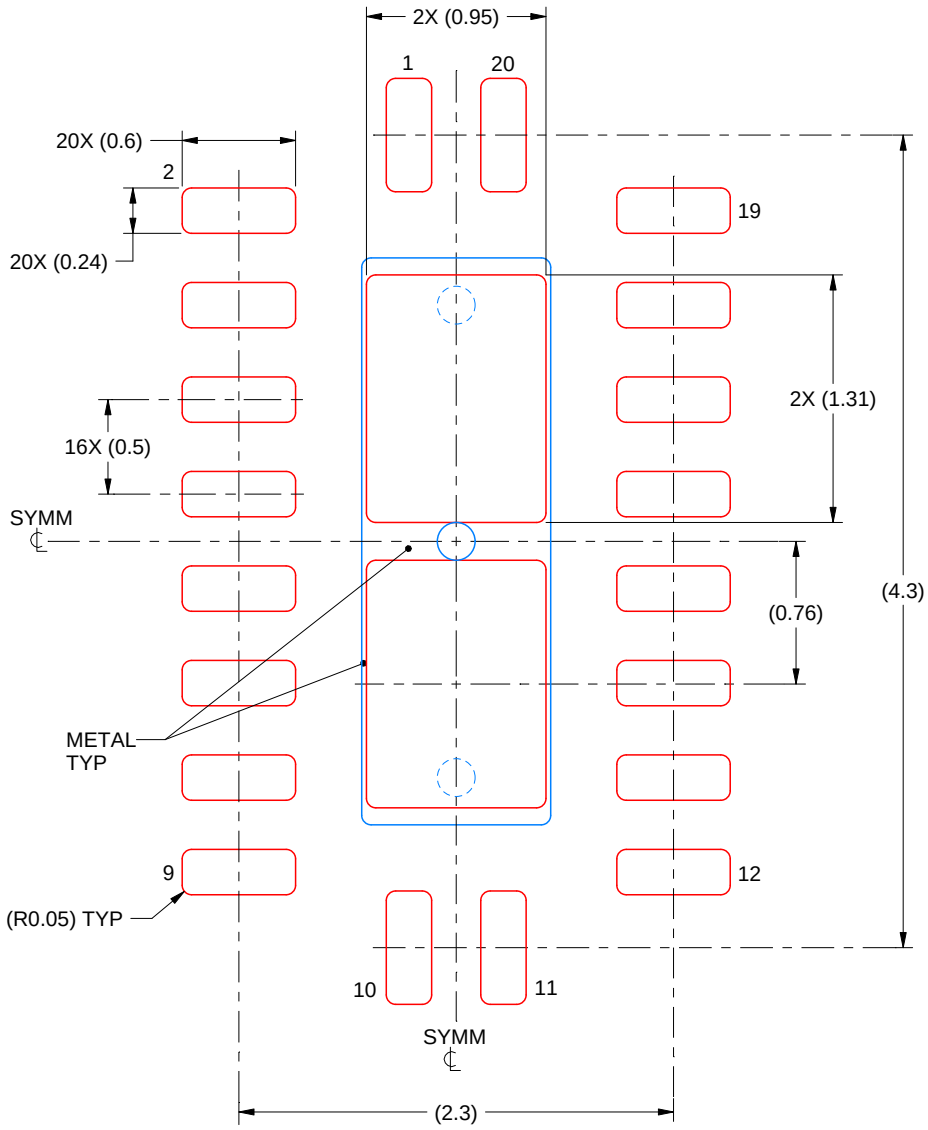


SOLDER MASK DETAILS

4222490/B 02/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
83% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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