

TMUX9616x ラッチアップ耐性付き、220V 高電圧 1:1、16 チャンネル・スイッチ

1 特長

- 広い電源電圧範囲または入力信号範囲:
 - 両電源: $\pm 20V \sim \pm 110V$ 、 $220V_{PP}$
 - $240V_{PP}$ の絶対最大値
- 低いオフ容量: 5pF
- 低いオン容量: 10pF
- 低いオン抵抗 (R_{ONL}): 12 Ω
- 高速ターンオン時間: 3 μs (最大値)
- 最大 72MHz のデータシフトクロック周波数
- ロジックレベル: 1.8V $\sim$ 5V
- 非常に優れたオフ絶縁性能: 5MHz 時に -70dB
- 出力にブリード抵抗を内蔵
- デバイス構造に基づくラッチアップ耐性
- 拡張温度範囲: -40°C $\sim$ 125°C
- 業界標準の 7mm $\times$ 7mm (本体サイズ) LQFP パッケージによるピン互換の実現

2 アプリケーション

- 医療用超音波画像処理
- 非破壊試験 (NDT) による金属の欠陥検出
- 圧電性のトランスデューサ・ドライバ
- 超音波流量トランスミッタ
- プリンタ
- 光 MEMS モジュール

3 概要

TMUX9616x は、ラッチアップ耐性を備えた、16 チャンネル、低抵抗、低静電容量、高電圧のアナログ スイッチ集積回路 (IC) です。各デバイスは、独立して選択可能な 16

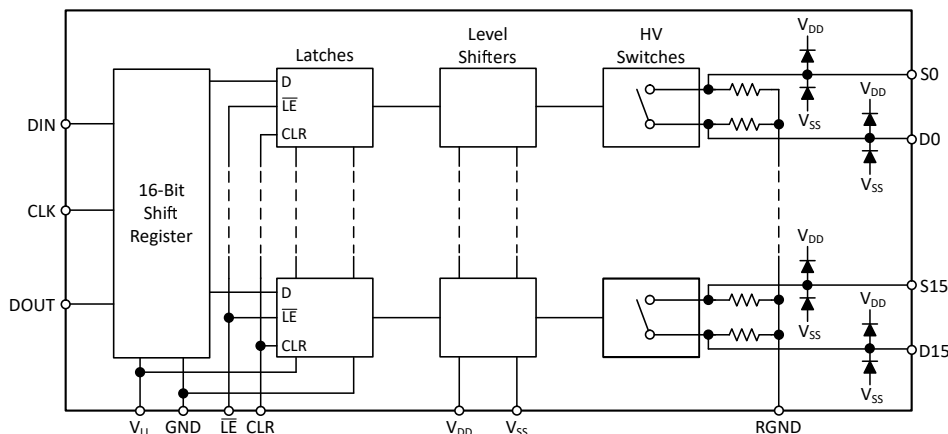
個の 1:1 単極単投 (SPST) スイッチ チャンネルを備えています。このデバイスは、 $\pm 110V$ までのデュアル電源で適切に動作します。推奨電源範囲内では、非対称の電源バイアスもサポートされています。TMUX9616x は、ソース (Sx) およびドレイン (Dx) ピンで、 V_{SS} から V_{DD} までの範囲の双方向アナログおよびデジタル信号をサポートします。TMUX9616x はまた、ソース (Sx) ピンとドレイン (Dx) ピンにブリード抵抗を内蔵しており、圧電トランスデューサなどの容量性負荷を放電します。TMUX9616x は、医療用超音波イメージングやその他の圧電トランスデューサドライバアプリケーション向けの優れた選択肢になります。

TMUX9616x は、カスケード接続可能な 16 ビット シフトレジスタを内蔵し、16 個の各スイッチを制御するためのラッチを搭載しています。デジタイゼーション機能により、デバイスごとに個別のチップ セレクトを必要とせず、多くの TMUX9616x デバイスを制御できます。潜在的なクロックフィードスルーによる信号パスのノイズを低減するために、データがシフトレジスタにロードされている間、アクティブローのラッチ イネーブルを High に保持することができます。16 ビット シフトレジスタは、1.8V $\sim$ 5V の電源で動作できます。16 ビット シフトレジスタは、最高 72MHz のクロック速度をサポートできます。

パッケージ情報

部品番号	ブリード抵抗を内蔵	パッケージ (1)	パッケージサイズ (2)
TMUX9616	あり	PT (LQFP, 48)	9mm $\times$ 9mm
TMUX9616N	なし	PT (LQFP, 48)	9mm $\times$ 9mm

- 詳細については、[セクション 11](#) を参照してください。
- パッケージサイズ (長さ $\times$ 幅) は公称値で、該当する場合はピンも含まれます。



概略回路図



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4 Pin Configuration and Functions

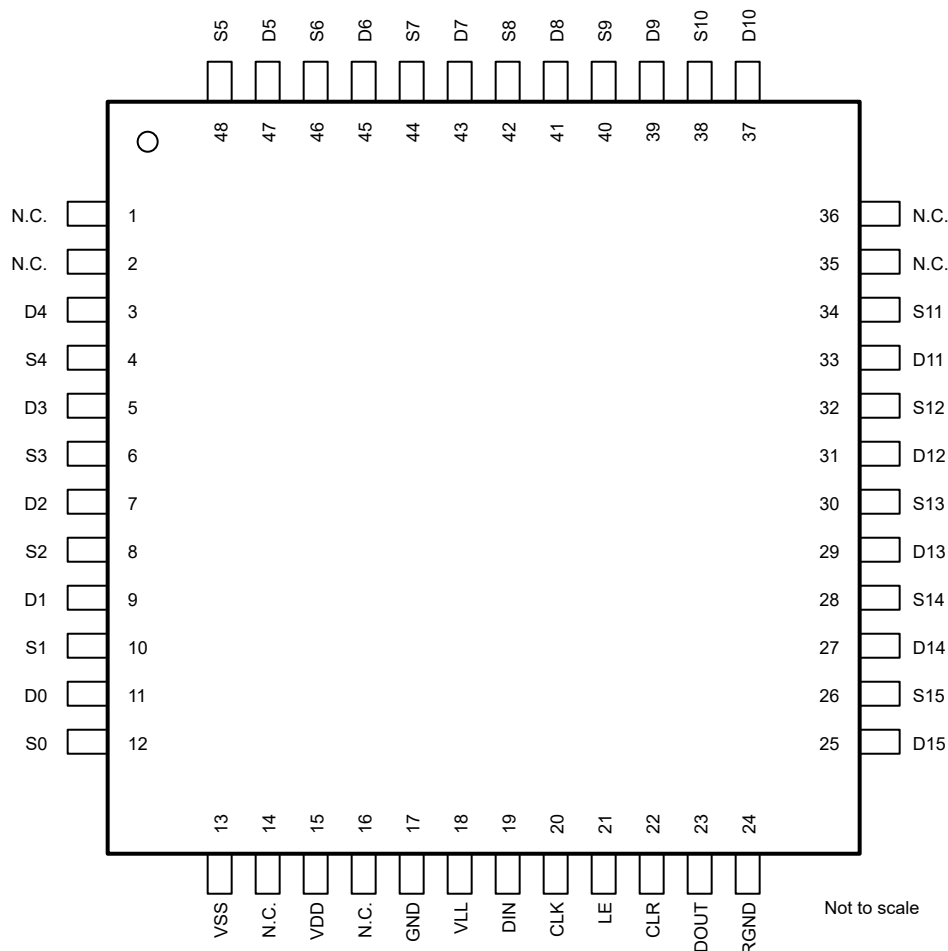


図 4-1. PT Package, 48-Pin LQFP (Top View)

表 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
N.C.	1	—	No internal connection. Leave floating or connect to GND.
N.C.	2	—	No internal connection. Leave floating or connect to GND.
D4	3	I/O	Drain pin 4. Can be an input or an output.
S4	4	I/O	Source pin 4. Can be an input or an output.
D3	5	I/O	Drain pin 3. Can be an input or an output.
S3	6	I/O	Source pin 3. Can be an input or an output.
D2	7	I/O	Drain pin 2. Can be an input or an output.
S2	8	I/O	Source pin 2. Can be an input or an output.
D1	9	I/O	Drain pin 1. Can be an input or an output.
S1	10	I/O	Source pin 1. Can be an input or an output.
D0	11	I/O	Drain pin 0. Can be an input or an output.
S0	12	I/O	Source pin 0. Can be an input or an output.
V _{SS}	13	P	Negative power supply. This pin is the most negative power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V _{SS} and GND.
N.C.	14	—	No internal connection. Leave floating or connect to GND.

表 4-1. Pin Functions (続き)

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
V _{DD}	15	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 μ F to 10 μ F between V _{DD} and GND.
N.C.	16	—	No internal connection. Leave floating or connect to GND.
GND	17	P	Ground (0 V) reference.
V _{LL}	18	P	1.8 V – 5 V SPI power supply. For reliable operation, connect a decoupling capacitor ranging from 0.1 μ F to 1 μ F between V _{LL} and GND.
DIN	19	I	SPI (Daisy Chain) Data Input.
CLK	20	I	SPI (Daisy Chain) Clock Input.
$\overline{\text{LE}}$	21	I	Latch enable input, active low.
CLR	22	I	Latch clear input, active high.
DOUT	23	O	SPI (Daisy Chain) Data Output.
RGND	24	P	Bleed Resistor GND. Connect to ground (0 V) reference.
D15	25	I/O	Drain pin 15. Can be an input or an output.
S15	26	I/O	Source pin 15. Can be an input or an output.
D14	27	I/O	Drain pin 14. Can be an input or an output.
S14	28	I/O	Source pin 14. Can be an input or an output.
D13	29	I/O	Drain pin 13. Can be an input or an output.
S13	30	I/O	Source pin 13. Can be an input or an output.
D12	31	I/O	Drain pin 12. Can be an input or an output.
S12	32	I/O	Source pin 12. Can be an input or an output.
D11	33	I/O	Drain pin 11. Can be an input or an output.
S11	34	I/O	Source pin 11. Can be an input or an output.
N.C.	35	—	No internal connection. Leave floating or connect to GND.
N.C.	36	—	No internal connection. Leave floating or connect to GND.
D10	37	I/O	Drain pin 10. Can be an input or an output.
S10	38	I/O	Source pin 10. Can be an input or an output.
D9	39	I/O	Drain pin 9. Can be an input or an output.
S9	40	I/O	Source pin 9. Can be an input or an output.
D8	41	I/O	Drain pin 8. Can be an input or an output.
S8	42	I/O	Source pin 8. Can be an input or an output.
D7	43	I/O	Drain pin 7. Can be an input or an output.
S7	44	I/O	Source pin 7. Can be an input or an output.
D6	45	I/O	Drain pin 6. Can be an input or an output.
S6	46	I/O	Source pin 6. Can be an input or an output.
D5	47	I/O	Drain pin 5. Can be an input or an output.
S5	48	I/O	Source pin 5. Can be an input or an output.

(1) I = input, O = output, P = power

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)^{(1) (2) (3)}

		MIN	MAX	UNIT
V _{DD} –V _{SS}	Supply voltage		240	V
V _{DD}		–0.5	120	V
V _{SS}		–120	0.5	V
V _{LL}	SPI/Logic supply voltage	–0.5	6	V
V _L	Logic control pin voltage (DIN, DOUT, CLK, $\overline{\text{LE}}$, CLR)	–0.5	V _{LL}	V
I _L	Logic control pin current (DIN, DOUT, CLK, $\overline{\text{LE}}$, CLR)	–30	30	mA
V _S or V _D	Source or drain voltage (Sx, D)	V _{SS}	V _{DD}	V
I _{PK}	Analog Signal Peak Current/Channel		3	A
T _A	Ambient temperature	–40	125	°C
T _{stg}	Storage temperature	–65	150	°C
T _J	Junction temperature	–40	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
- (3) All voltages are with respect to ground, unless otherwise specified.

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins ⁽¹⁾	±1000	V
		Charged device model (CDM), per ANSI/ESDA/ JEDEC JS-002, all pins ⁽²⁾	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Thermal Information

THERMAL METRIC ⁽¹⁾		TMUX9616x	UNIT
		PT (LQFP)	
		48 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	60.8	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	15.4	°C/W
R _{θJB}	Junction-to-board thermal resistance	26.9	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	0.5	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	26.6	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{DD} - V_{SS}$	Power supply voltage differential	40	200	220	V
V_{DD}	Positive power supply voltage	20	100	110	V
V_{SS}	Negative power supply voltage	–110	–100	0	V
V_S or V_D	Signal path input/output voltage (source or drain pin) (S_x , D) ⁽¹⁾	$V_{SS} + 10$		$V_{DD} - 10$	V
V_{LL}	SPI/Logic power supply voltage	1.7		5.5	V
V_L	Logic control pin voltage (DIN, DOUT, CLK, $\overline{LE}$, CLR)	0		V_{LL}	V
V_{IH}	Logic control pin high-level input voltage (DIN, DOUT, CLK, $\overline{LE}$, CLR)	$0.9 \times V_{LL}$			V
V_{IL}	Logic control pin low-level input voltage (DIN, DOUT, CLK, $\overline{LE}$, CLR)			$0.1 \times V_{LL}$	V
T_A	Ambient temperature	–40		85	°C
T_J	Junction temperature	–40		125	°C

- (1) V_S , V_D operation up to V_{SS} and V_{DD} is acceptable for recommended operation. $R_{ON\ FLAT}$ may increase when operating beyond $V_{SS} + 10V$ and $V_{DD} - 10V$

5.5 Electrical Characteristics: TMUX9616

$V_{DD} = +110\text{ V}$, $V_{SS} = -110\text{ V}$, $V_{LL} = 1.7\text{ V} - 5.5\text{ V}$, $GND = 0\text{ V}$ (unless otherwise noted)
 Typical at $V_{DD} = +110\text{ V}$, $V_{SS} = -110\text{ V}$, $V_{LL} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T _A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R _{ON}	On-resistance	V _S = −100 V to +100 V I _D = −5 mA	25°C		14	19	Ω
			−40°C to +85°C			24	Ω
R _{ON}	On-resistance	V _S = −100 V to +100 V I _D = −200 mA	25°C		13	17	Ω
			−40°C to +85°C			19	Ω
ΔR _{ON}	On-resistance mismatch between channels	V _S = −100 V to +100 V I _D = −5 mA	25°C		2		%
			−40°C to +85°C			20	%
R _{ONL}	Large-Signal On-resistance	I _D = -1A	25°C		12		Ω
I _{SWPK}	Switch Peak Output Current	t _{PW} ≤100ns, duty cycle ≤ 0.1%, current into source or drain.	25°C		3		A
I _{SWPK_DIO DE}	Switch Peak Isolation Diode Current	t _{PW} ≤300ns, duty cycle ≤ 2%	25°C		300		mA
V _{DC_OFFS ET}	Switch DC Offset Voltage	Switch ON or OFF, R _L = No load (Integrated Bleed Resistors), R _L = 35kΩ (Bleed Resistors not integrated).	25°C		1.6		mV
			−40°C to +85°C	−60		30	mV
R _{INT}	Output Bleed Resistor	Source or Drain Output to GND, I _{RINT} = 20μA. Switch is OFF	25°C	20	35	50	kΩ
I _{S(OFF)_N}	Source off leakage current ⁽¹⁾	No Bleed Resistor (9616N only) V _{DD} = 110 V, V _{SS} = −110 V Switch state is off V _S = +100 V / −100 V V _D = −100 V / + 100 V	25°C		0.0002		μA
			−40°C to +85°C	−0.015		0.015	μA
I _{S(OFF)}	Source off leakage current ⁽¹⁾	Integrated Bleed Resistor (9616 only) V _{DD} = 110 V, V _{SS} = −110 V Switch state is off V _S = +100 V / −100 V V _D = −100 V / + 100 V	25°C		0.07		μA
			−40°C to +85°C	−4		4	μA
I _{D(OFF)_N}	Drain off leakage current ⁽¹⁾	No Bleed Resistor (9616N only) V _{DD} = 110 V, V _{SS} = −110 V Switch state is off V _S = +100 V / −100 V V _D = −100 V / + 100 V	25°C		0.0002		μA
			−40°C to +85°C	−0.015		0.015	
I _{D(OFF)}	Drain off leakage current ⁽¹⁾	Integrated Bleed Resistor (9616 only) V _{DD} = 110 V, V _{SS} = −110 V Switch state is off V _S = +100 V / −100 V V _D = −100 V / + 100 V	25°C		0.07		μA
			−40°C to +85°C	−4		4	μA
DIGITAL LOGIC (DIN, DOUT, CLK, $\overline{\text{LE}}$, CLR Pins)							
V _{IH}	Logic voltage high	V _{LL} = 1.7V - 5.5V	−40°C to +85°C		0.66 x V _{LL}		V
V _{IL}	Logic voltage low	V _{LL} = 1.7V - 5.5V	−40°C to +85°C			0.33 x V _{LL}	V
I _{IH}	Input leakage current		−40°C to +85°C			1.0	μA
I _{IL}	Input leakage current		−40°C to +85°C	−1.0			μA
C _{IN}	Logic input capacitance		−40°C to +85°C		3	10	pF
V _{OH}	Logic high output voltage	I _{SOURCE} = 1mA	−40°C to +85°C		V _{LL} - 0.1		V

5.5 Electrical Characteristics: TMUX9616 (続き)

$V_{DD} = +110\text{ V}$, $V_{SS} = -110\text{ V}$, $V_{LL} = 1.7\text{ V} - 5.5\text{ V}$, $GND = 0\text{ V}$ (unless otherwise noted)

Typical at $V_{DD} = +110\text{ V}$, $V_{SS} = -110\text{ V}$, $V_{LL} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{OL}	Logic low output voltage $I_{SINK} = 1\text{ mA}$, includes open drain / THERM pin	-40°C to $+85^\circ\text{C}$			0.1	V
POWER SUPPLY						
I_{DDQ_OFF}	V_{DD} quiescent supply current $V_{DD} = 110\text{ V}$, $V_{SS} = -110\text{ V}$ $I_D = -5\text{ mA}$ Switches OFF	25°C -40°C to $+85^\circ\text{C}$		15		μA μA
I_{DDQ_ON}	V_{DD} quiescent supply current $V_{DD} = 110\text{ V}$, $V_{SS} = -110\text{ V}$ $I_D = -5\text{ mA}$ Switches ON	25°C -40°C to $+85^\circ\text{C}$		40		μA μA
I_{SSQ_OFF}	V_{SS} quiescent supply current $V_{DD} = 110\text{ V}$, $V_{SS} = -110\text{ V}$ $I_D = -5\text{ mA}$ Switches OFF	25°C -40°C to $+85^\circ\text{C}$		10		μA μA
I_{SSQ_ON}	V_{SS} quiescent supply current $V_{DD} = 110\text{ V}$, $V_{SS} = -110\text{ V}$ $I_D = -5\text{ mA}$ Switches ON	25°C -40°C to $+85^\circ\text{C}$		22		μA μA
I_{DD}	V_{DD} dynamic supply current $V_{DD} = 110\text{ V}$, $V_{SS} = -110\text{ V}$ All switches turned ON and OFF at $f = 50\text{ kHz}$	25°C -40°C to $+85^\circ\text{C}$		2.4		mA mA
I_{SS}	V_{SS} dynamic supply current $V_{DD} = 110\text{ V}$, $V_{SS} = -110\text{ V}$ All switches turned ON and OFF at $f = 50\text{ kHz}$	25°C -40°C to $+85^\circ\text{C}$		3.1		mA mA
I_{LLQ}	V_{LL} quiescent supply current	25°C -40°C to $+85^\circ\text{C}$		3.8		μA μA
I_{LL}	V_{LL} dynamic supply current $f_{CLK} = 5\text{ MHz}$, $V_{LL} = 5\text{ V}$	25°C -40°C to $+85^\circ\text{C}$		0.20		mA mA

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.

5.6 Switching Characteristics: TMUX9616

$V_{DD} = +110\text{ V}$, $V_{SS} = -110\text{ V}$, $V_{LL} = 1.7\text{ V} - 5.5\text{ V}$, $GND = 0\text{ V}$ (unless otherwise noted)

Typical at $V_{DD} = +110\text{ V}$, $V_{SS} = -110\text{ V}$, $V_{LL} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{ON}	Turn-on time from enable $V_S = 100\text{ V}$ $R_L = 10\text{ k}\Omega$	25°C -40°C to $+85^\circ\text{C}$		1.5		μs μs
t_{OFF}	Turn-off time from enable $V_S = 100\text{ V}$ $R_L = 10\text{ k}\Omega$	25°C -40°C to $+85^\circ\text{C}$		0.8		μs μs
dV/dt_{MAX}	Maximum Analog Signal Slew Rate	-40°C to $+85^\circ\text{C}$			20	V/ns
O_{ISO_TX}	Off-isolation TX $R_L = 50\text{ }\Omega$ $V_S = 0\text{ V}_{BIAS}$, 10 V_{PP} , $f = 5\text{ MHz}$ Refer to Off Isolation	25°C		-70		dB
O_{ISO_TX}	Off-isolation TX $R_L = 1\text{ k}\Omega$, $C_L = 15\text{ pF}$ $V_S = 0\text{ V}_{BIAS}$, 10 V_{PP} , $f = 5\text{ MHz}$ Refer to Off Isolation	25°C		-54		dB
O_{ISO_RX}	Off-isolation RX $R_L = 50\text{ }\Omega$ $V_D = 0\text{ V}_{BIAS}$, 10 V_{PP} , $f = 5\text{ MHz}$ Refer to Off Isolation	25°C		-70		dB
O_{ISO_RX}	Off-isolation RX $R_L = 1\text{ k}\Omega$, $C_L = 15\text{ pF}$ $V_D = 0\text{ V}_{BIAS}$, 10 V_{PP} , $f = 5\text{ MHz}$ Refer to Off Isolation	25°C		-54		dB

5.6 Switching Characteristics: TMUX9616 (続き)

$V_{DD} = +110\text{ V}$, $V_{SS} = -110\text{ V}$, $V_{LL} = 1.7\text{ V} - 5.5\text{ V}$, $GND = 0\text{ V}$ (unless otherwise noted)
 Typical at $V_{DD} = +110\text{ V}$, $V_{SS} = -110\text{ V}$, $V_{LL} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
X_{TALK_TX}	Crosstalk TX	$R_L = 50\ \Omega$ $V_S = 0\text{ V}_{BIAS}$, 10 V_{PP} , $f = 5\text{ MHz}$	25°C		-75		dB
X_{TALK_RX}	Crosstalk RX	$R_L = 50\ \Omega$ $V_D = 0\text{ V}_{BIAS}$, 10 V_{PP} , $f = 5\text{ MHz}$	25°C		-75		dB
BW_{SS_TX}	-3dB Bandwidth (Small Signal) TX	$R_L = 50\ \Omega$ $V_S = 0\text{ V}$, $V_{pp} = 200\text{ mV}$	25°C		500		MHz
BW_{SS_RX}	-3dB Bandwidth (Small Signal) RX	$R_L = 50\ \Omega$ $V_D = 0\text{ V}$, $V_{pp} = 200\text{ mV}$	25°C		500		MHz
$HD2PC_LL_TX$	Second Harmonic Distortion Pulse Cancellation (Large Signal) TX	$V_{pp} = 200\text{ V}$, $V_S = 0\text{ V}$ $R_L = 100\ \Omega \parallel 100\text{ pF}$ $f = 5\text{ MHz}$, 2 Cycles, dv/dt : 7.1 V/ns	25°C		54		dBc
$C_{S(OFF)}$	Source off capacitance	$V_S = 0\text{ V}_{BIAS}$, 100 mV_{PP} , $f = 1\text{ MHz}$	25°C		5		pF
$C_{D(OFF)}$	Drain off capacitance	$V_D = 0\text{ V}_{BIAS}$, 100 mV_{PP} , $f = 1\text{ MHz}$	25°C		5		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance	$V_S/V_D = 0\text{ V}_{BIAS}$, 100 mV_{PP} , $f = 1\text{ MHz}$	25°C		10		pF
V_{SPK}	Output voltage spike	$R_{L_Source} = 1\text{ k}\Omega$, $R_{L_Drain} = 50\ \Omega$ Enable and Disable Switch	25°C	-45		18	mV
V_{SPK}	Output voltage spike	$R_{L_Source} = 1\text{ k}\Omega$, $R_{L_Drain} = 50\ \Omega$ Enable and Disable Switch	-40°C to $+85^\circ\text{C}$	-55		25	mV

5.7 Digital Timings: TMUX9616

$V_{DD} = 4.5\text{ V} - 5.5\text{ V}$, $V_{LL} = 1.7\text{ V} - 5.5\text{ V}$, $GND = 0\text{ V}$ (unless otherwise noted)
 Typical at $V_{DD} = 5\text{ V}$, $V_{LL} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
f_{CLK_SPI}	SPI Clock Frequency (including daisy chain mode)	$V_{LL} = 5\text{ V}$	-40°C to $+85^\circ\text{C}$			72	MHz
f_{CLK_SPI}	SPI Clock Frequency (including daisy chain mode)	$V_{LL} = 3.3\text{ V}$	-40°C to $+85^\circ\text{C}$			54	MHz
f_{CLK_SPI}	SPI Clock Frequency (including daisy chain mode)	$V_{LL} = 1.8\text{ V}$	-40°C to $+85^\circ\text{C}$			24	MHz
t_R , t_F SPI	SPI Clock Rise and Fall Times		-40°C to $+85^\circ\text{C}$			50	ns
t_{CLK_SPI}	CLK SPI Period	$V_{LL} = 5\text{ V}$	-40°C to $+85^\circ\text{C}$	11.76			ns
t_{CLK_SPI}	CLK SPI Period	$V_{LL} = 3.3\text{ V}$	-40°C to $+85^\circ\text{C}$	16.67			ns
t_{CLK_SPI}	CLK SPI Period	$V_{LL} = 1.8\text{ V}$	-40°C to $+85^\circ\text{C}$	41.67			ns
$t_{CLK_H_SPI}$	CLK High Time SPI	$V_{LL} = 5\text{ V}$	-40°C to $+85^\circ\text{C}$	5.29			ns
$t_{CLK_H_SPI}$	CLK High Time SPI	$V_{LL} = 3.3\text{ V}$	-40°C to $+85^\circ\text{C}$	7.5			ns
$t_{CLK_H_SPI}$	CLK High Time SPI	$V_{LL} = 1.8\text{ V}$	-40°C to $+85^\circ\text{C}$	18.75			ns
$t_{CLK_L_SPI}$	CLK Low Time SPI	$V_{LL} = 5\text{ V}$	-40°C to $+85^\circ\text{C}$	5.29			ns
$t_{CLK_L_SPI}$	CLK Low Time SPI	$V_{LL} = 3.3\text{ V}$	-40°C to $+85^\circ\text{C}$	7.5			ns
$t_{CLK_L_SPI}$	CLK Low Time SPI	$V_{LL} = 1.8\text{ V}$	-40°C to $+85^\circ\text{C}$	18.75			ns
t_{SU_SPI}	Set Up Time Data to Clock SPI	$V_{LL} = 5\text{ V}$	-40°C to $+85^\circ\text{C}$	1.0			ns
t_{SU_SPI}	Set Up Time Data to Clock SPI	$V_{LL} = 3.3\text{ V}$	-40°C to $+85^\circ\text{C}$	2			ns
t_{SU_SPI}	Set Up Time Data to Clock SPI	$V_{LL} = 1.8\text{ V}$	-40°C to $+85^\circ\text{C}$	5			ns
t_H SPI	Hold Time Data to Clock SPI	$V_{LL} = 5\text{ V}$	-40°C to $+85^\circ\text{C}$	1.0			ns

5.7 Digital Timings: TMUX9616 (続き)

$V_{DD} = 4.5V - 5.5V$, $V_{LL} = 1.7V - 5.5V$, $GND = 0V$ (unless otherwise noted)

Typical at $V_{DD} = 5V$, $V_{LL} = 3.3V$, $T_A = 25^\circ C$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{H_SPI}	Hold Time Data to Clock SPI	$V_{LL} = 3.3V$	–40°C to +85°C	1.2		ns
t_{H_SPI}	Hold Time Data to Clock SPI	$V_{LL} = 1.8V$	–40°C to +85°C	3		ns
t_{DO}	Clock Delay Time to Data Out	$V_{LL} = 5V$	–40°C to +85°C	3	12.8	ns
t_{DO}	Clock Delay Time to Data Out	$V_{LL} = 3.3V$	–40°C to +85°C	4	16.3	ns
t_{DO}	Clock Delay Time to Data Out	$V_{LL} = 1.8V$	–40°C to +85°C	7	34	ns
$t_{S/LE}$	Set Up Time Before $\overline{LE}$ Rises		–40°C to +85°C	25		ns
$t_{W/LE}$	Time Width of $\overline{LE}$		–40°C to +85°C	12		ns
t_{WCLR}	Time Width of CLR		–40°C to +85°C	55		ns

5.8 Timing Diagrams

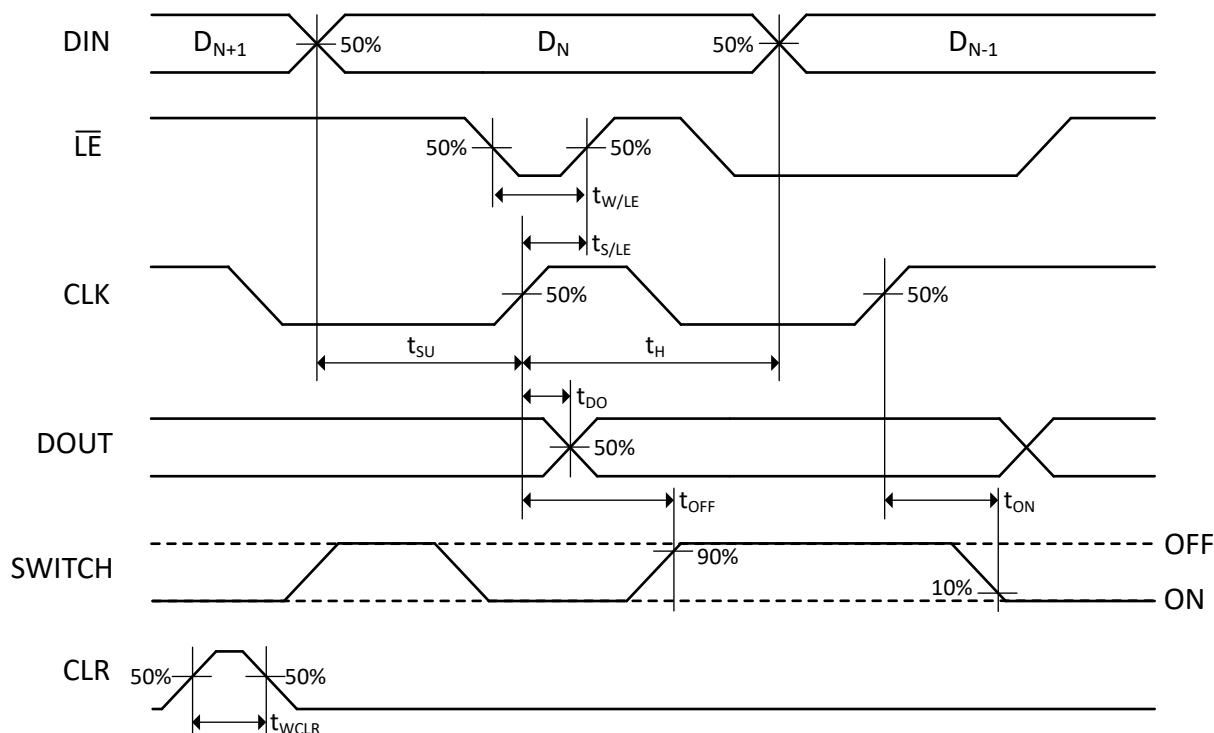


図 5-1. Logic Timing Diagram

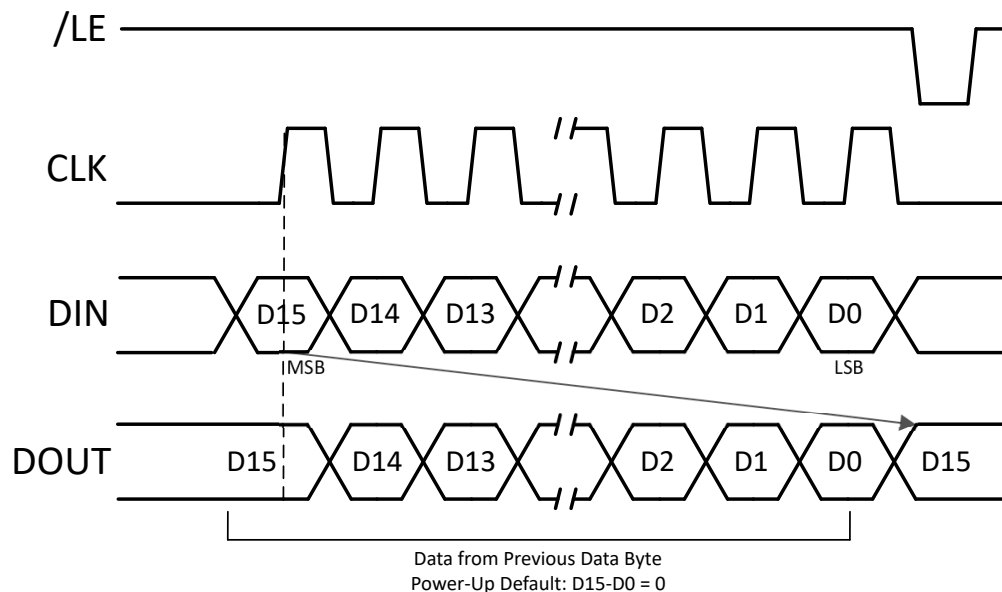


図 5-2. Latch Enable Timing Diagram

5.9 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $V_{DD} = 110\text{ V}$, $V_{SS} = -110\text{ V}$, and $V_{LL} = 3.3\text{ V}$ (unless otherwise noted)

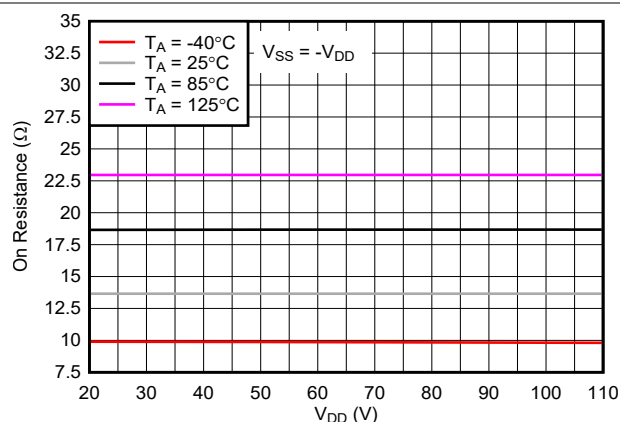


図 5-3. On-Resistance vs V_{DD}/V_{SS} Supply Voltage

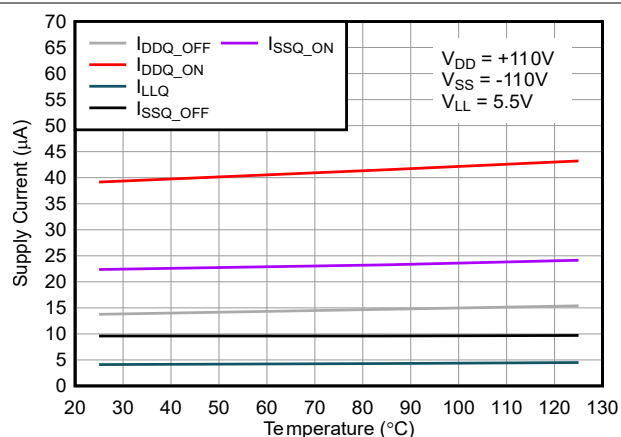


図 5-4. Supply Quiescent Current vs Temperature

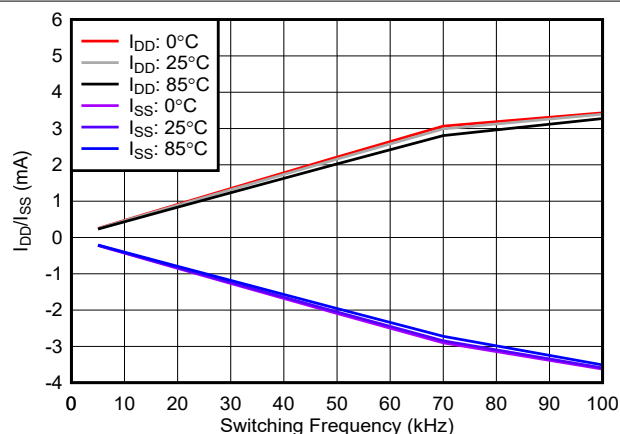


図 5-5. High Voltage Supply Current vs Switching Frequency

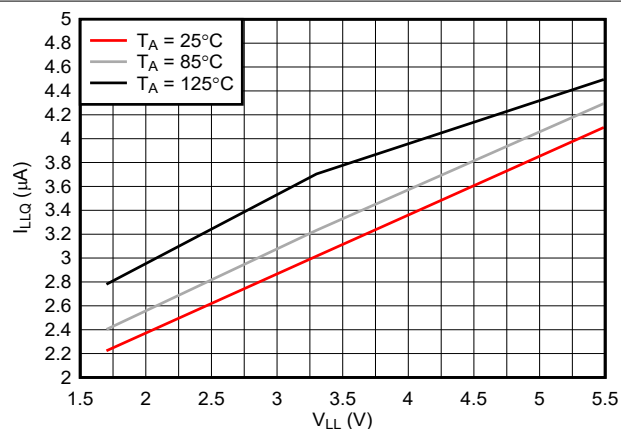


図 5-6. I_{LLQ} vs V_{LL}

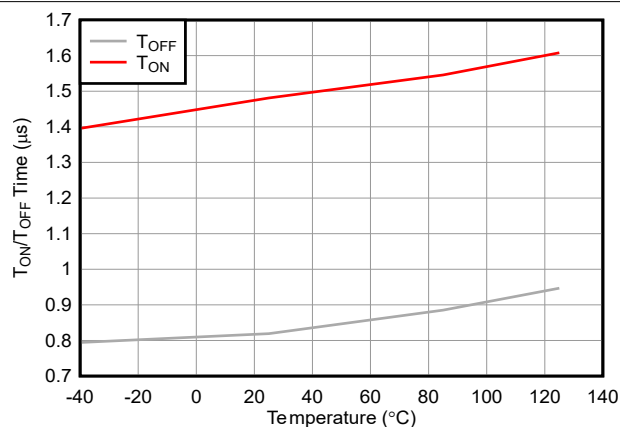


図 5-7. Turn ON and Turn OFF Time vs Temperature

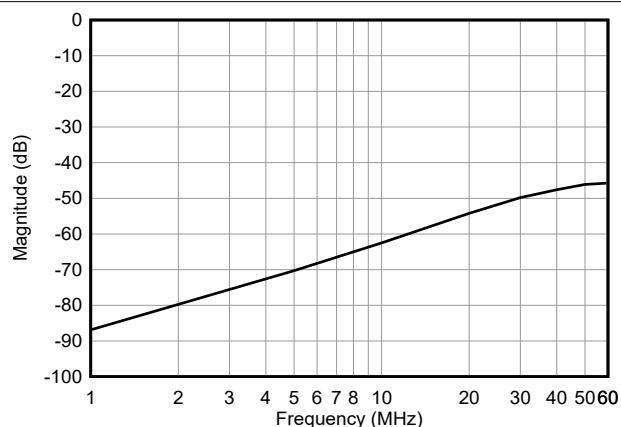


図 5-8. Large Signal Off Isolation vs Frequency

5.9 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_{DD} = 110\text{ V}$, $V_{SS} = -110\text{ V}$, and $V_{LL} = 3.3\text{ V}$ (unless otherwise noted)

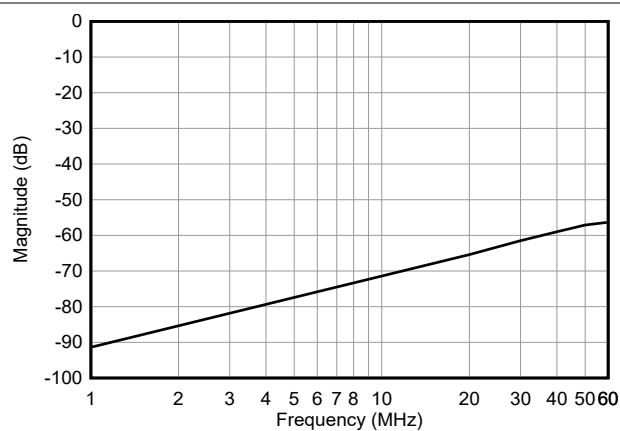


図 5-9. Large Signal Crosstalk vs Frequency

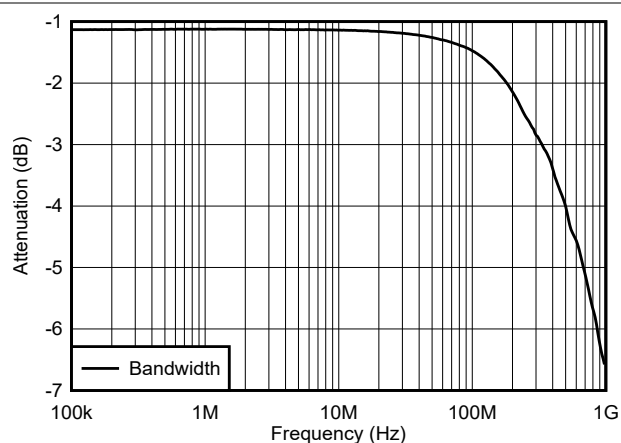


図 5-10. Small Signal Insertion Loss vs Frequency

6 Parameter Measurement Information

6.1 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

1. Source off-leakage current $I_{S(OFF)}$: the leakage current flowing into or out of the source pin when the switch is off.
2. Drain off-leakage current $I_{D(OFF)}$: the leakage current flowing into or out of the drain pin when the switch is off.

The setup used to measure both off-leakage currents is shown in 図 6-1.

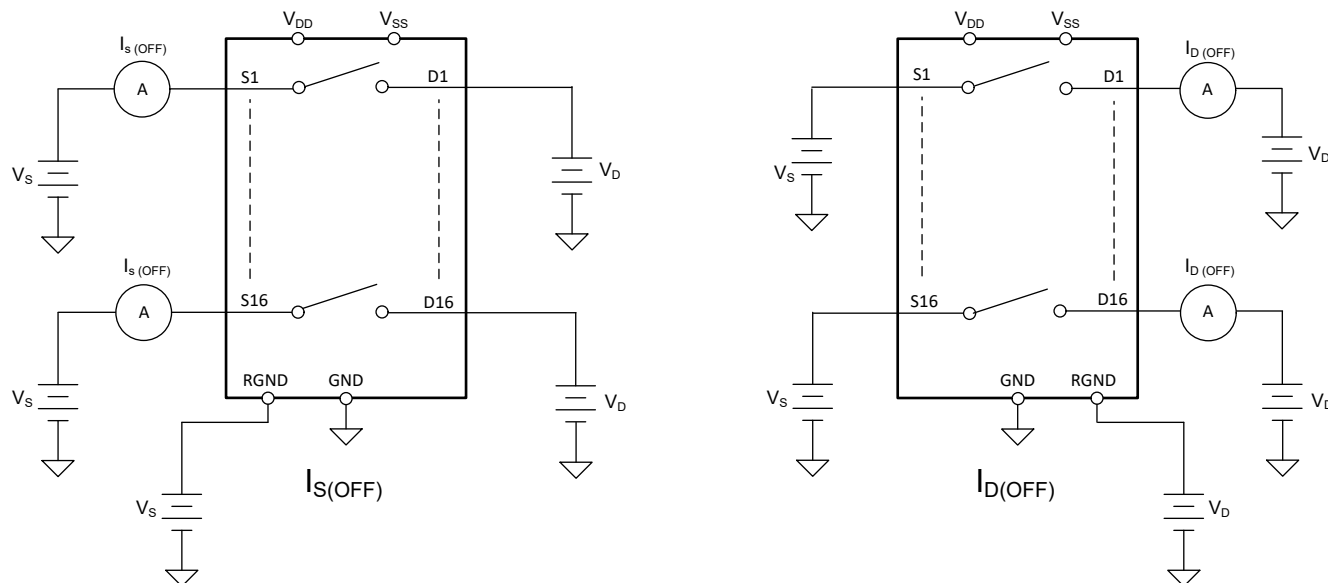


図 6-1. Off-Leakage Measurement Setup

6.2 Device Turn On/Off Time

Turn-off time (t_{OFF}) is defined as the time taken by the Sx pin of the TMUX9616x to rise to a 90% final value after the CLK signal has risen to 50% of its final value. Turn-on time (t_{ON}) is defined as the time taken by the output of the TMUX9616x to fall to a 10% initial value after the CLK signal has risen to 50% of its final value. 図 6-2 shows the setup used to measure t_{ON} and t_{OFF} .

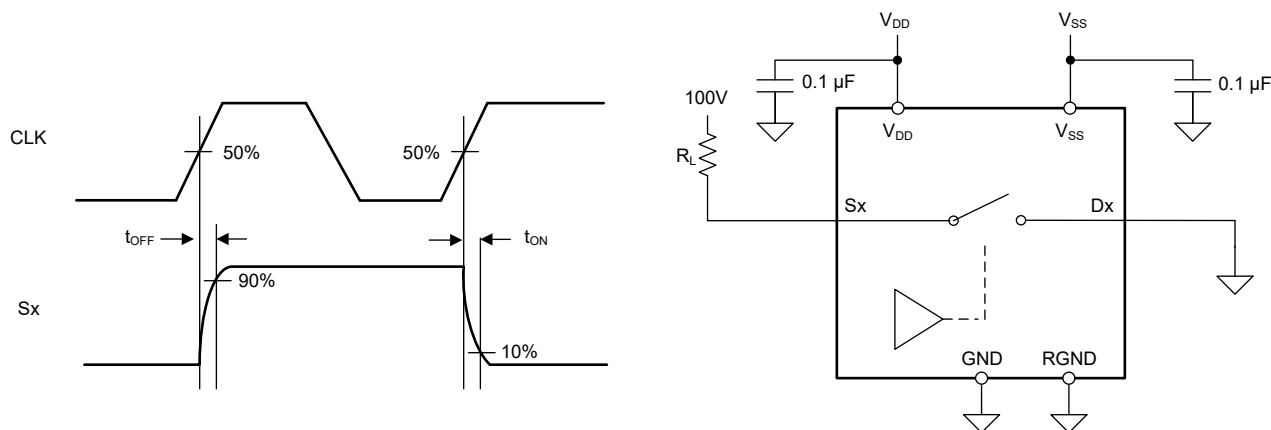
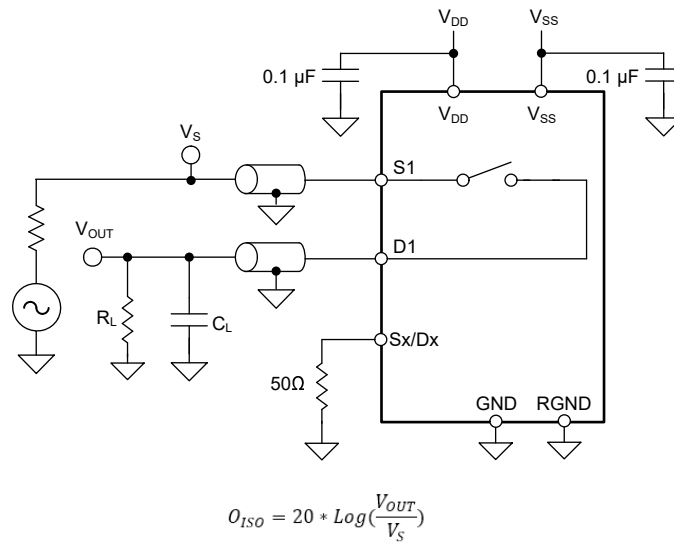


図 6-2. Turn-on/off Measurement Setup

6.3 Off Isolation

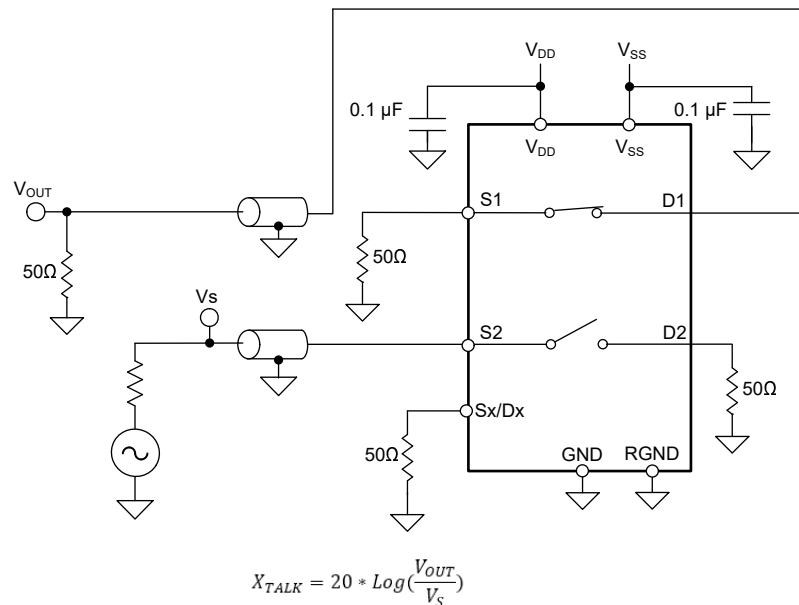
Off isolation is defined as the ratio of the signal at the drain pin (Dx) of the device when a signal is applied to the source pin (Sx) of an off-channel. 6-3 shows the setup used to measure off isolation.



6-3. Off Isolation Measurement Setup

6.4 Inter-Channel Crosstalk

Crosstalk (X_{TALK}) is defined as the ratio of the output signal at the Dx pin of an on-channel to the input signal at the Sx pin of an off-channel, as shown in 6-4.



6-4. Crosstalk Measurement Setup

6.5 Output Voltage Spike

Output Voltage Spike (V_{SPIKE} or V_{SPK}) is the magnitude of the transient output voltage spike which occurs on an input or output pin when turning the switch channel ON or OFF. When measuring V_{SPK} on the Dx pin, $50\ \Omega$ is placed on the Dx pin and $1\ \text{k}\Omega$ is placed on the Sx pin. Likewise, when measuring V_{SPK} on the Sx pin, $50\ \Omega$ is placed on the Sx pin and $1\ \text{k}\Omega$ is placed on the Dx pin. [Figure 6-5](#) shows the setup used to measure the V_{SPK} of the switch.

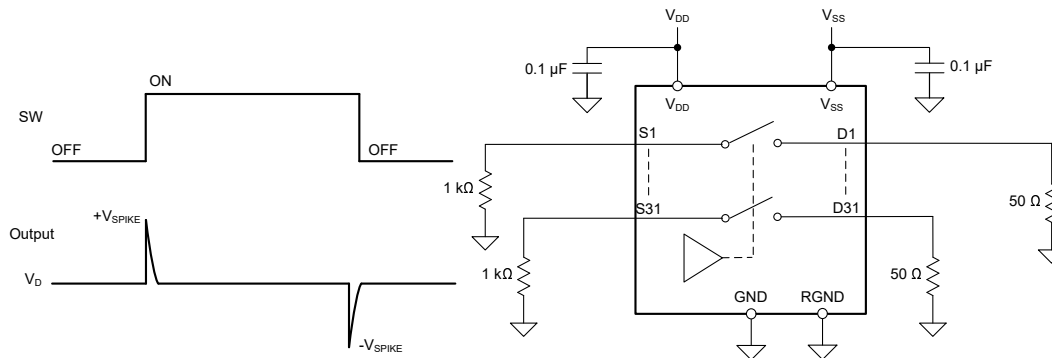


Figure 6-5. V_{SPK} Measurement Setup

6.6 Switch DC Offset Voltage

The switch DC offset voltage ($V_{\text{DC_OFFSET}}$) is the DC offset voltage that can be present on an Sx or Dx pin when the switch channel is ON or OFF. [Figure 6-6](#) shows the setup used to measure the $V_{\text{DC_OFFSET}}$ voltage of the device.

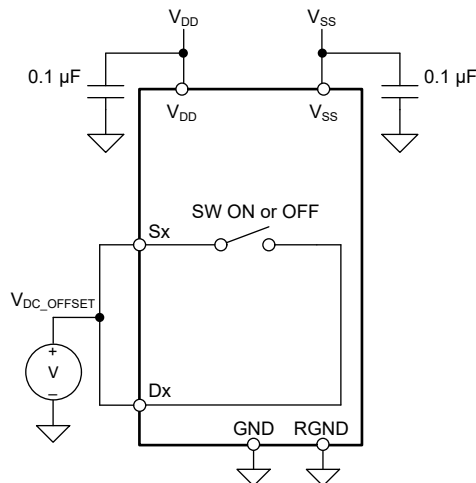


Figure 6-6. $V_{\text{DC_OFFSET}}$ Measurement Setup

6.7 Isolation Diode Current

The switch peak isolation diode current ($I_{\text{SWPK_DIODE}}$) is the maximum peak current the isolation diodes on each channel can sustain. Figure 6-7 shows the set-up used to measure $I_{\text{SWPK_DIODE}}$.

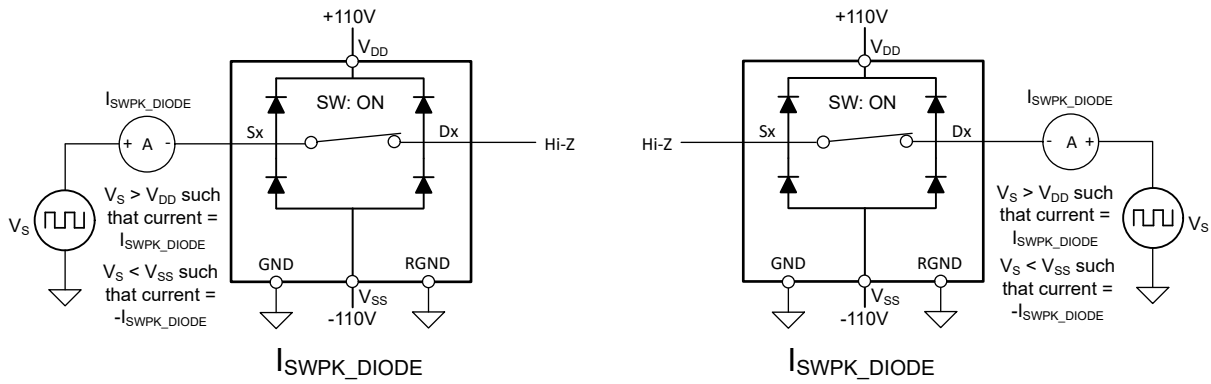


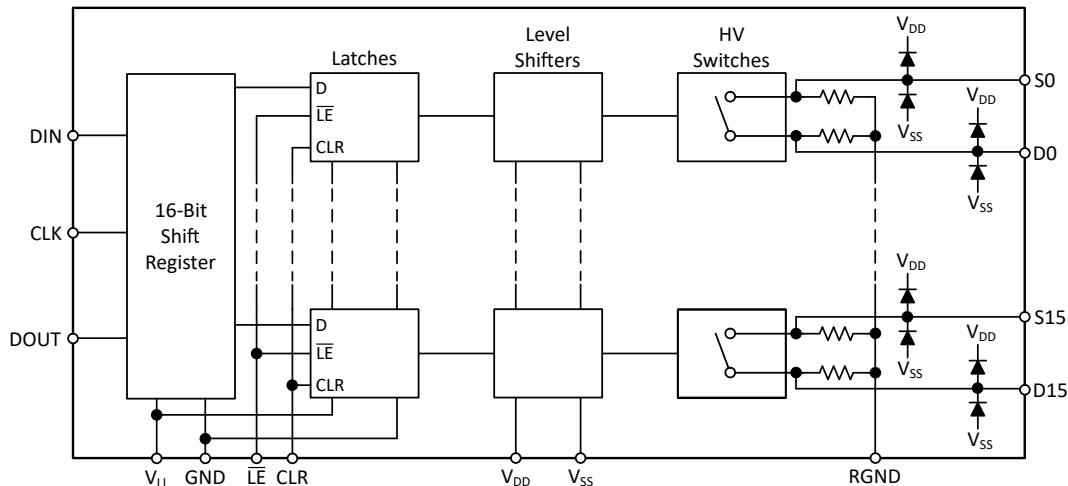
Figure 6-7. Isolation Diode Current Measurement Setup

7 Detailed Description

7.1 Overview

The TMUX9616x is a 16-channel low resistance, low capacitance high-voltage analog switch integrated circuit (IC) with latch-up immunity. Each device has 16 independently selectable 1:1, single-pole, single-throw (SPST) switch channels. The device works well with dual supplies up to ± 110 V. Asymmetric supply biasing is also supported within the recommended supply range. The TMUX9616x supports bidirectional analog and digital signals on the source (Sx) and drain (Dx) pins ranging from V_{SS} to V_{DD} . TMUX9616x also integrates bleed resistors on its source (Sx) and drain (Dx) pins to discharge capacitive loads, like piezoelectric transducers.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Wide Input Signal Range (up to ± 110 V, 220 V_{PP})

TMUX9616x can pass a wide input signal range, up to V_{DD}/V_{SS} of ± 110 V (220 V_{PP}), which is very beneficial as many high voltage transmitters are designed to transmit up to ± 100 V. The extra headroom above ± 100 V that TMUX9616x provides is critical for operating the high voltage transmitters in systems up to ± 100 V for a few reasons. First, with high voltage supply multiplexers (± 110 V V_{DD}/V_{SS}), typically as the V_S pin approaches V_{DD} ($V_S > V_{DD} - (5 \text{ V to } 10 \text{ V})$), the R_{ON} of the switch starts to rapidly increase. With a large change in R_{ON} when V_S is near V_{DD} , this can cause the harmonic distortion performance of the system to degrade (HD2PC, so fourth). Setting the high voltage supplies 10 V above the pulser operating voltage, allows V_S to stay $\leq (V_{DD} - 10 \text{ V})$, keeping the switch in its flat R_{ON} operating region for the intended TX signal, and therefore greatly improving system harmonic distortion performance.

Second, various system parasitics (or even intentionally added tuning inductors) and transmission line reflections in the system (due to cables, long PCB traces, and so forth) can cause some temporary peaking of the maximum voltage that the TMUX9616x receives above the ± 100 V maximum output voltage of the high voltage transmitter. Having the high voltage multiplexer in the system have voltage tolerance above the high voltage transmitter (up to $V_{DD} = +110$ V and $V_{SS} = -110$ V per *Recommended Operating Conditions*) is crucial for being able to run the system at the high voltage transmitters maximum voltage output capability.

7.3.2 Bidirectional Operation

The devices conduct equally well from source (Sx) to drain (Dx) or from drain (Dx) to source (Sx). Each signal path has very similar characteristics in both directions.

7.3.3 Device Digital Logic Control

The TMUX9616x is controlled by a SPI interface to a 16-bit shift register, and a CLR pin. The SPI interface can run at speeds up to 72 MHz. It can also be run with 1.8 V – 5 V logic levels (set by logic supply V_{LL}). The DIN pin will take in the data for the 16-bit register, and CLK will take in the clock signal. Data is shifted in on the DIN pin with the most-significant bit (MSB) first. After writing in 16 bits into the shift register using DIN and CLK, $\overline{LE}$ is then used to latch the state of the switches in the shift register to change the state of the switches in analog. The switches go to a state of retaining their present state on the rising edge of the $\overline{LE}$ pin. When $\overline{LE}$ is high, updates to the shift register does not change the condition of the 16 switches until $\overline{LE}$ is made low again. When $\overline{LE}$ is low, the shift register data flows through the latch and the condition of the 16 switches will be changed as the shift register is updated.

TMUX9616x 16-bit shift register can be used in daisy chain mode. This is done by connecting the DOUT pin of the first TMUX9616x device to the DIN pin of the next TMUX9616x device in the chain. All TMUX9616x in the daisy chain will share the same source CLK signal (the CLK pin of each device in the daisy chain will be shorted together). DOUT is the data output pin of the 16th bit of the shift register, which is the data on DIN clock shifted by 16 clock cycles. The $\overline{LE}$ pin of each device in the chain will be shorted together, using the same $\overline{LE}$ source.

Assuming N number of TMUX9616x devices in the daisy chain, the standard method of writing to the shift registers is to write $16 * N$ bits of data, corresponding to each switch in the daisy chain, with $\overline{LE}$ set high. Once all $16 * N$ bits are written into the shift register, $\overline{LE}$ is pulsed low for at least t_{WLE} to update the condition of the $16 * N$ switches in the daisy chain to the new state recorded in the shift register. Then $\overline{LE}$ is set high again so that the state of the switches will not change until the next $16 * N$ bits are written into the shift register (and $\overline{LE}$ is pulsed low again following the $16 * N$ bit write).

The CLR pin, when asserted high, causes all the 16 switches in TMUX9616x to turn OFF, regardless of the state of the bits in the 16-bit shift register. When the CLR pin asserted low, the switches will then use the shift register again to set its values.

For more details on programming the shift register and the logic state of each switch, see the [Device Logic Table](#) section. For more details of programming the shift register with the correct digital timings, see the [Timing Diagrams](#) section and the [Digital Timings](#) table. For more details on the maximum speeds obtainable in daisy chain mode depending on device configuration, see the [Switching Characteristics](#) table. [Figure 7-1](#) shows more details on how to connect the TMUX9616x device's in daisy chain mode.

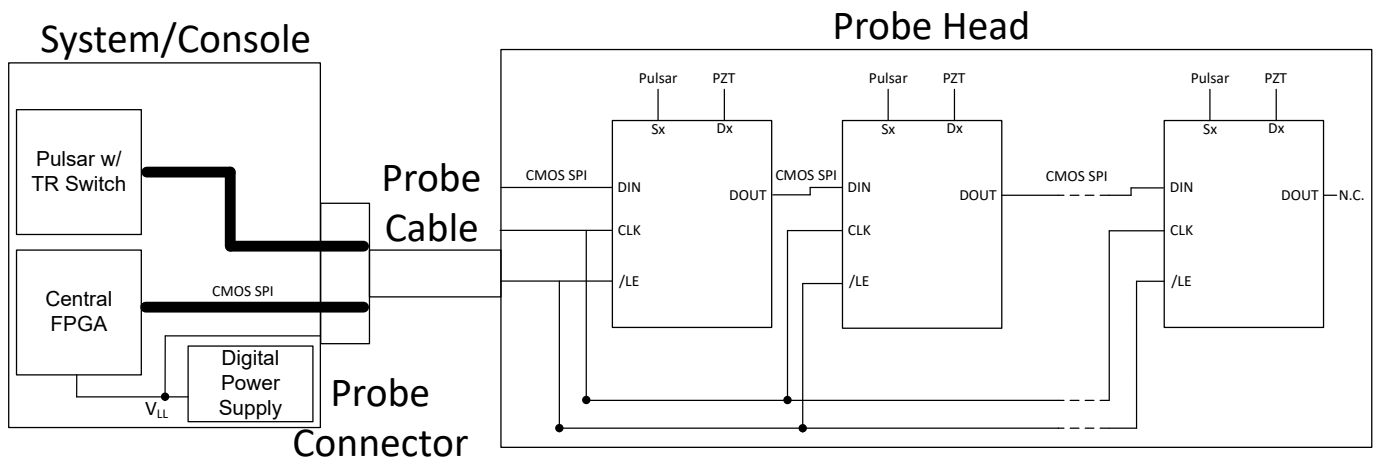


Figure 7-1. Daisy Chain System Block Diagram

7.3.4 Latch-Up Immunity by Device Construction

Latch-up is a condition where a low impedance path is created between a supply pin and ground. This condition is caused by a trigger (current injection or overvoltage), but once activated, the low impedance path remains even after the trigger is no longer present. This low impedance path may cause system upset or catastrophic damage due to excessive current levels. The latch-up condition typically requires a power cycle to eliminate the low impedance path.

The TMUX9616x is constructed on silicon on insulator (SOI) based process where an oxide layer is added between the PMOS and NMOS transistor of each CMOS switch to prevent parasitic structures from forming. The oxide layer is also known as an insulating trench and prevents triggering of latch up events due to overvoltage, fast voltage slew rates, and current injections. The latch-up immunity feature allows the TMUX9616x to be used in harsh environments. For more information on latch-up immunity, refer to [Using Latch Up Immune Multiplexers to Help Improve System Reliability](#).

7.4 Device Functional Modes

7.4.1 Normal Mode

In normal mode operation, TMUX9616x is controlled by its digital logic, which is detailed in the [Device Digital Logic Control](#) section. In normal mode, switches are available to be used to pass high voltage ± 110 V signals (signals from V_{SS} to V_{DD}). More details of the device operation in normal mode can be found in the [Feature Description](#) and [Device Logic Table](#) sections.

7.4.2 Device Power Up

TMUX9616x will be powered up once V_{LL} , V_{DD} , and V_{SS} reach their final voltage. V_{LL} , V_{DD} , and V_{SS} can be powered up in any order (there is no power sequencing requirement). The device digital logic control will not receive updates until both V_{LL} , V_{DD} , and V_{SS} are powered up. Additionally, after V_{LL} , V_{DD} , and V_{SS} are powered up, the system FPGA or controller should wait at least 500 μ s until writing to the device digital logic control. For more details on the device digital logic control, see the [Device Digital Logic Control](#) section.

On power-up, all 16 switches in TMUX9616x will be in the OFF state.

7.5 Device Logic Table

表 7-1. Device Logic Table (1) (2) (3) (4) (5) (6) (7)

Inputs						Outputs			
D0	D1	...	D15	LE	CLR	SW0	SW1	...	SW15
0	—	...	—	L	L	OFF	—	...	—
1	—		—	L	L	ON	—		—
—	0		—	L	L	—	OFF		—
—	1		—	L	L	—	ON		—
—	—		—	L	L	—	—		—
—	—		—	L	L	—	—		—
—	—		0	L	L	—	—		OFF
—	—		1	L	L	—	—		ON
X	X	X	X	H	L	HOLD PREVIOUS STATE			
X	X	X	X	X	H	OFF	OFF	OFF	OFF

- (1) All 16 switches operate independently.
- (2) Serial data is clocked in on the rising edge of CLK. Data is shifted in on the DIN pin with the most-significant bit (MSB) first.
- (3) The switches go to a state of retaining their present state on the rising edge of the LE pin. Once the LE pin is high, updates to the shift register no longer change the condition of the 16 switches until the LE pin is made low again. When the LE is low, the shift register data flows through the latch.
- (4) Shift register clocking has no effect on the switch states if the LE pin is high.
- (5) DOUT is the data output pin of the 16 bit shift register for daisy chaining multiple muxes together. It is the data of the DIN clock shifted by the 16 clock cycles.
- (6) The CLR input overrides all other inputs.
- (7) While LE = H or CLR = H, if the CLK pin still receiving a valid clock signal, DIN will still function and input data into the shift register, and DOUT will still output the contents on the shift register. However, while LE = H or CLR = H, the state of the analog switches is no longer dependent on the contents of the shift register, but rather takes the state per this logic table.

8 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TMUX9616x is a 16-channel low harmonic distortion, low resistance, low capacitance, high-voltage analog switch integrated circuit (IC) with latch-up immunity. Each device has 16 independently selectable 1:1, single-pole, single-throw (SPST) switch channels. The device can support high voltage supplies and signals up to $\pm 110\text{V}$. It comes in popular, pin-to-pin (P2P) 48-pin QFP package for 16CH SPST multiplexers. This makes TMUX9616x a great replacement in an existing design with fixed foot print, where improvement is needed on harmonic distortion performance of the system. Also, TMUX9616x a great solution any time the application may require a leaded package.

8.2 Typical Application

Figure 8-1 shows a multiplexer configuration that is found in a variety of ultrasound applications. Two TX7516 are used to provide 32 TX/RX channels, and 8x TMUX9616x are used to multiplex the 32 TX/RX channels to 128 piezoelectric (PZT) elements, making a 4:1 multiplexer configuration. An FPGA controls both the TX7516 and TMUX9616x using SPI.

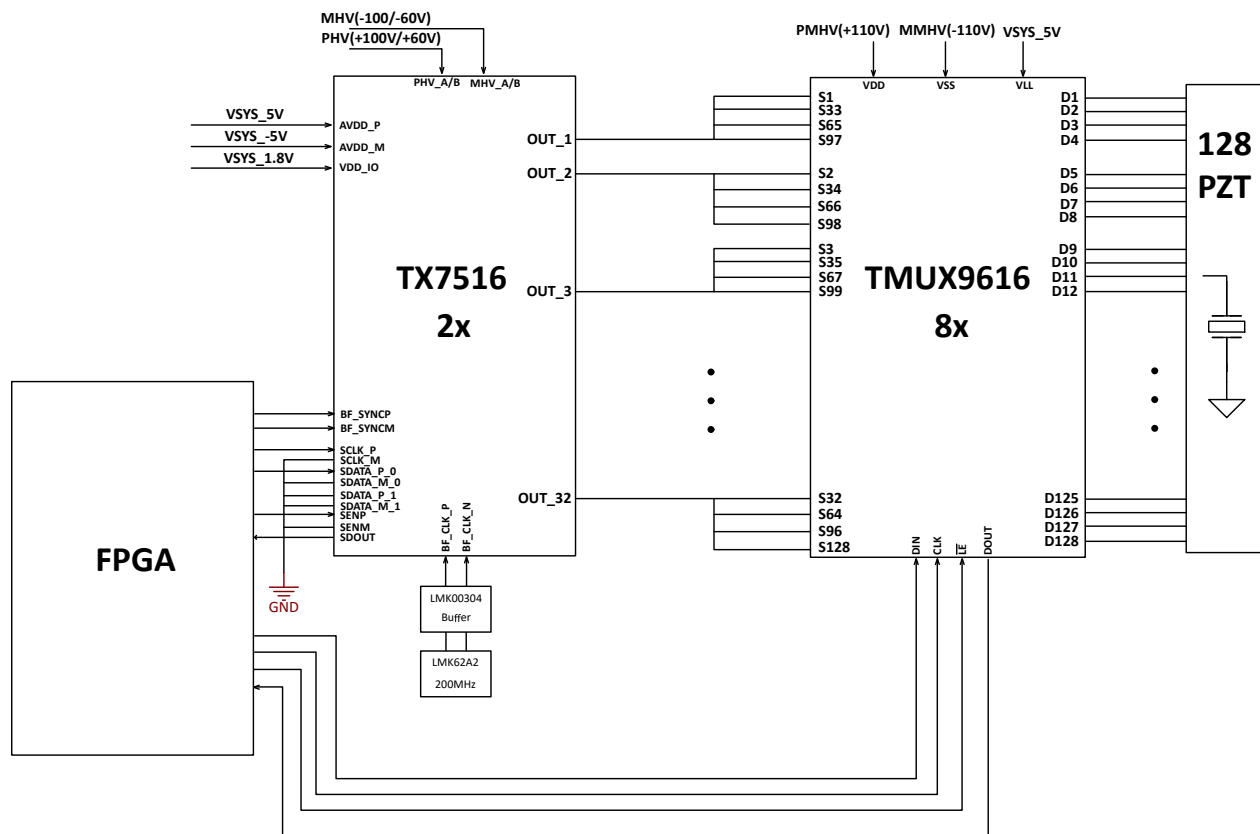


Figure 8-1. TMUX9616x Application Schematic

8.2.1 Design Requirements

表 8-1. Design Parameters

PARAMETERS	VALUES
Positive analog supply (V_{DD}) TMUX9616x	+110 V
Negative analog supply (V_{SS}) TMUX9616x	-110 V
Logic supply (V_{LL}) TMUX9616x	5 V
Pulser supply A (PHV_A/MHV_A) TX7516	+100 V/-100 V
Pulser supply B (PHV_B/MHV_B) TX7516	+60 V/-60 V
Analog signal support TMUX9616x	± 110 V
Maximum SPI speed supported TMUX9616x	72 MHz
System level HD2PC target requirement	≥ 40 dB
System level HD1PC target requirement	≥ 40 dB
System test load	100 Ω 100 pF

8.2.2 Detailed Design Procedure

図 8-1 shows a system configuration found in a variety of ultrasound applications. The TX7516 has two supply rails A (PHV_A/MHV_A) and B (PHV_B/MHV_B) that enable switching between multiple TX levels for 3-Level mode, and also enable transmitting 5-Level mode. Each supply channel (A or B) can both provide up to 2 A output current, and the two channels can be operated in parallel for a 4 A output mode. Two TX7516 are used to provide 32 TX channels, and eight TMUX9616x are used to multiplex the 32 TX channels to the 128 PZT elements (4:1 mux configuration). Supply A will transmit at ± 100 V, and supply B will transmit ± 60 V.

A very important system level requirement for good image quality is to target ≥ 40 dB for both HD2PC and HD1PC (harmonic distortion pulse cancellation). The entire system, including both the TX7516 pulser and TMUX9616x mux, must output a TX signal at ≥ 40 dB. TX7516 is a pulser with excellent output signal performance, performing higher than the ≥ 40 dB target. Additionally, TMUX9616x is an excellent multiplexer, having minimal and in many cases negligible impact on the HD2PC/HD1PC performance, keeping the output signal performance high for good image quality while also allowing to increase the number of PZT elements in the system without increasing the number of pulser TX channels.

An example system use case using the TX7516EVM with the TMUX9616x EVM was performed first with the TMUX9616x removed and replaced with a pass through connection. Second, the same system level use case was performed by removing the pass through connection and adding the TMUX9616x back into the signal path. For a ± 100 V pulser supply in this system use case, transmitting in 3-level mode with 5 cycles at 5 MHz with a 100 Ω || 100 pF test load, TX7516 alone performed with an HD2PC of 49 dB and an HD1PC of 67 dB. For the same use case, adding in TMUX9616x into the signal path, the system performed with an HD2PC of 54 dB and an HD1PC of 60 dB. Therefore, in this use case the TMUX9616x has negligible impact on the system level HD2PC/HD1PC performance; TX7516, by itself, and TX7516 with TMUX9616x in its signal path perform at an HD2PC/HD1PC performance level well above 40 dB.

For more details on the HD2PC and HD1PC performance of TX7516 and TMUX9616x across multiple supply levels, see the [Application Curves](#). Additionally, some example use cases are plotted in the time domain and frequency domain for observation.

8.2.3 Application Curves

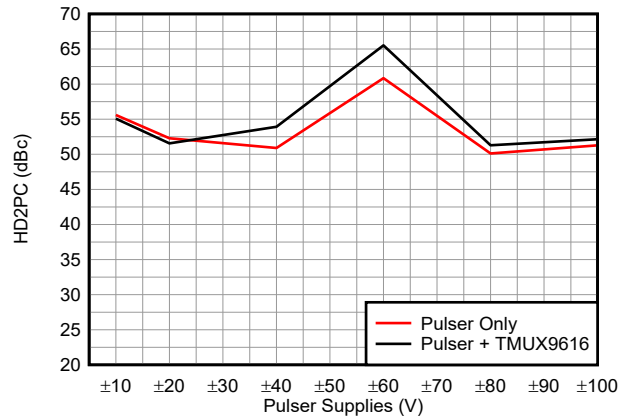


Figure 8-2. HD2PC TMUX9616 Input, 5MHz, 5 Cycles, 100Ω || 100pF Load

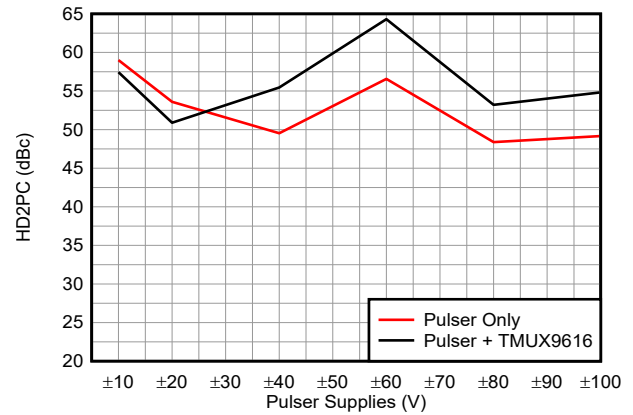


Figure 8-3. HD2PC TMUX9616 Output, 5MHz, 5 Cycles, 100Ω || 100pF Load

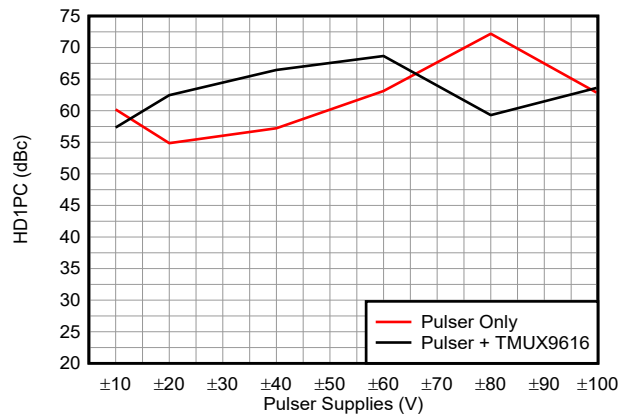


Figure 8-4. HD1PC TMUX9616 Input, 5MHz, 5 Cycles, 100Ω || 100pF Load

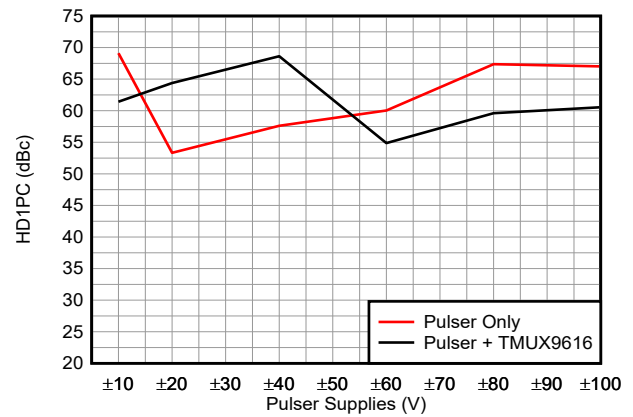


Figure 8-5. HD1PC TMUX9616 Output, 5MHz, 5 Cycles, 100Ω || 100pF Load

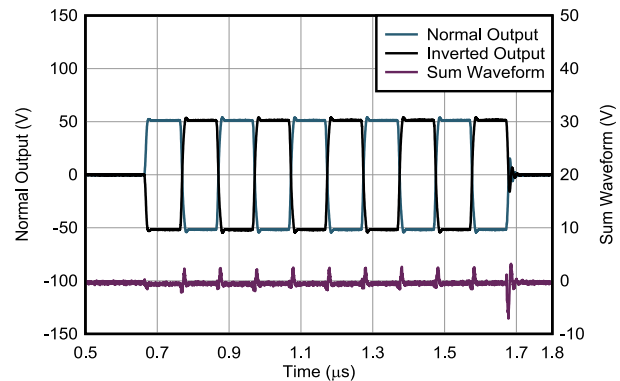


Figure 8-6. Pulser Only, Mux Input Side, ±60V Pulser Supplies, 5MHz, 5 Cycles, 100Ω || 100pF Load

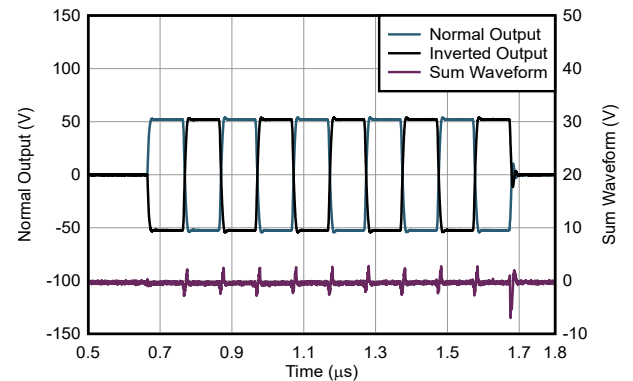
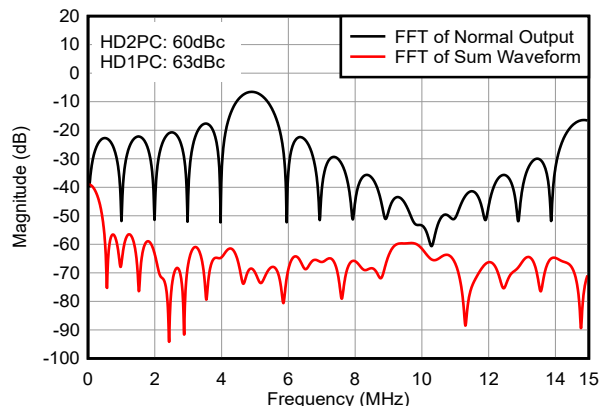
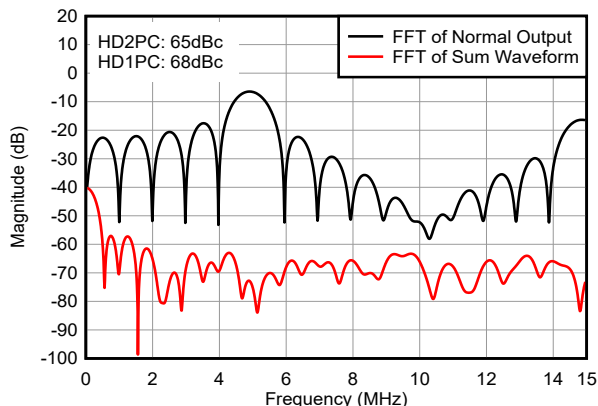


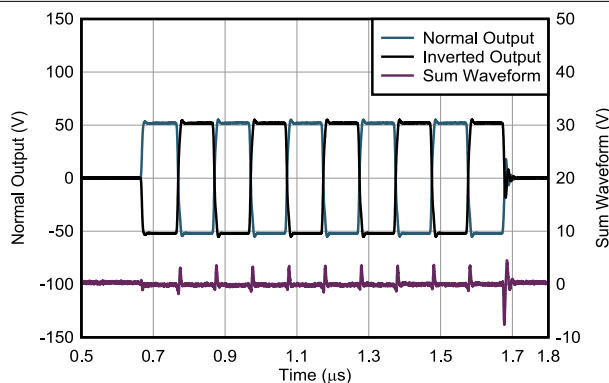
Figure 8-7. Pulser + TMUX9616, Mux Input Side, ±60V Pulser Supplies, 5MHz, 5 Cycles, 100Ω || 100pF Load



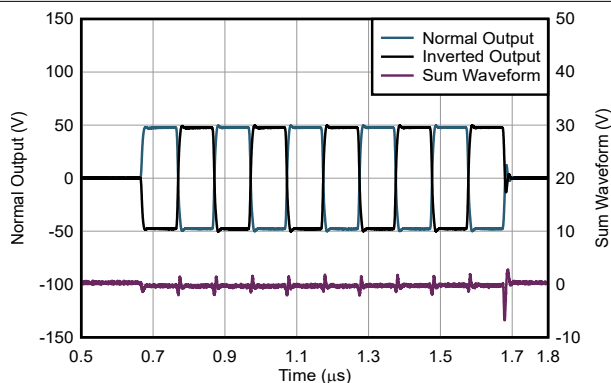
8-8. Pulser Only, Mux Input Side, $\pm 60V$ Pulser Supplies, 5MHz, 5 Cycles, $100\Omega \parallel 100pF$ Load



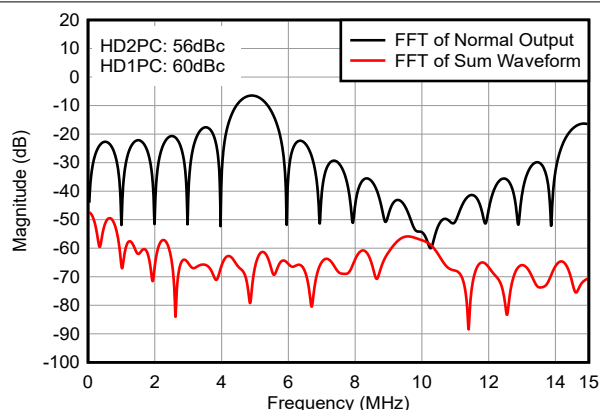
8-9. Pulser + TMUX9616, Mux Input Side, $\pm 60V$ Pulser Supplies, 5MHz, 5 Cycles, $100\Omega \parallel 100pF$ Load



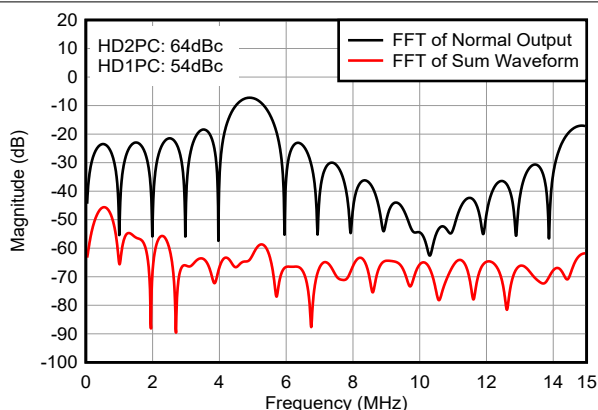
8-10. Pulser Only, Mux Output Side, $\pm 60V$ Pulser Supplies, 5MHz, 5 Cycles, $100\Omega \parallel 100pF$ Load



8-11. Pulser + TMUX9616, Mux Output Side, $\pm 60V$ Pulser Supplies, 5MHz, 5 Cycles, $100\Omega \parallel 100pF$ Load



8-12. Pulser Only, Mux Output Side, $\pm 60V$ Pulser Supplies, 5MHz, 5 Cycles, $100\Omega \parallel 100pF$ Load



8-13. Pulser + TMUX9616, Mux Output Side, $\pm 60V$ Pulser Supplies, 5MHz, 5 Cycles, $100\Omega \parallel 100pF$ Load

8.3 Power Supply Recommendations

The TMUX9616x supports a wide signal range of $\pm 110V$ (signals from V_{SS} to V_{DD}). It is recommended to use a supply decoupling capacitor of at least $0.1\mu F$ at the V_{DD} pin to ground and at the V_{SS} pin to ground. It is also recommended to use a supply decoupling capacitor for the logic supply V_{LL} of at least $0.1\mu F$ (V_{LL} pin to ground).

The TMUX9616x EVM uses 1 μF capacitor in parallel with a 0.1 μF capacitor for both the V_{DD} , V_{SS} , and V_{LL} supply pins.

There are no specific power sequencing requirements between the V_{DD} , V_{SS} , and V_{LL} supplies.

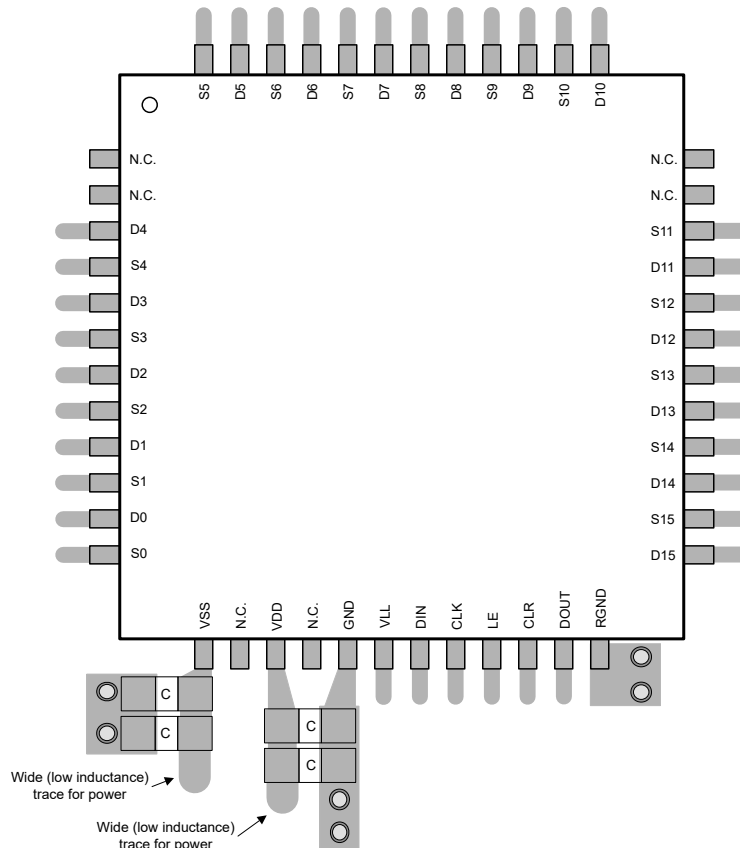
8.4 Layout

8.4.1 Layout Guidelines

The following image shows an example of a PCB layout with the TMUX9616x. Some key considerations are as follows:

- For reliable operation, connect at least one decoupling capacitor of at least 0.1 μF of capacitance between V_{DD} and V_{SS} to GND. The TMUX9616 EVM uses a 0.1 μF in parallel with a 1 μF capacitor. It is recommended to place the lowest value capacitor as close to the pin as possible. Ensure that the capacitor voltage rating is sufficient for the supply voltage.
- Keep the input lines as short as possible.
- Use a solid ground plane to help distribute heat and reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

8.4.2 Layout Example



8-14. TMUX9616 Layout Example

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Using Latch Up Immune Multiplexers to Help Improve System Reliability](#)

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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9.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (September 2023) to Revision A (December 2024)	Page
• TMUX9616N を追加.....	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMUX9616NPTR	Active	Production	LQFP (PT) 48	1000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TM9616N
TMUX9616PTR	Active	Production	LQFP (PT) 48	1000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TM9616
TMUX9616PTR.B	Active	Production	LQFP (PT) 48	1000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TM9616

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUX9616NPTR	LQFP	PT	48	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2
TMUX9616PTR	LQFP	PT	48	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUX9616NPTR	LQFP	PT	48	1000	336.6	336.6	31.8
TMUX9616PTR	LQFP	PT	48	1000	336.6	336.6	31.8



LQFP - 1.6 mm max height

Technical drawing of a square electronic component, likely a microchip, showing dimensions and feature callouts.

Top View Dimensions:

- Overall width: 9.2
- Overall height: 9.2
- Distance from top edge to center of top pins: 8.8
- Distance from left edge to center of left pins: 7.2
- Distance from right edge to center of right pins: 6.8
- Distance from bottom edge to center of bottom pins: 7.2
- Distance from left edge to center of left pins: 6.8

Pin Dimensions:

- Pin pitch: 0.5
- Pin width: 0.27
- Pin thickness: 0.17
- Pin length: 48X
- Pin width: 44X
- Pin thickness: 4X

Feature Callouts:

- SEE DETAIL A:** Points to a circular feature on the top surface.
- 1.6 MAX:** Dimension for the circular feature.
- SEATING PLANE:** Dimension for the bottom surface.
- 0.1 C:** Dimension for the bottom surface.
- 0.25 GAGE PLANE:** Dimension for the bottom surface.
- 0° - 7°:** Angle for the bottom surface.
- 0.75 0.45:** Dimension for the bottom surface.
- 1.45 1.35:** Dimension for the bottom surface.
- 0.05 MIN:** Dimension for the bottom surface.

DETAIL A: A circular feature on the top surface, likely a mounting hole or a test point.

NOTES:

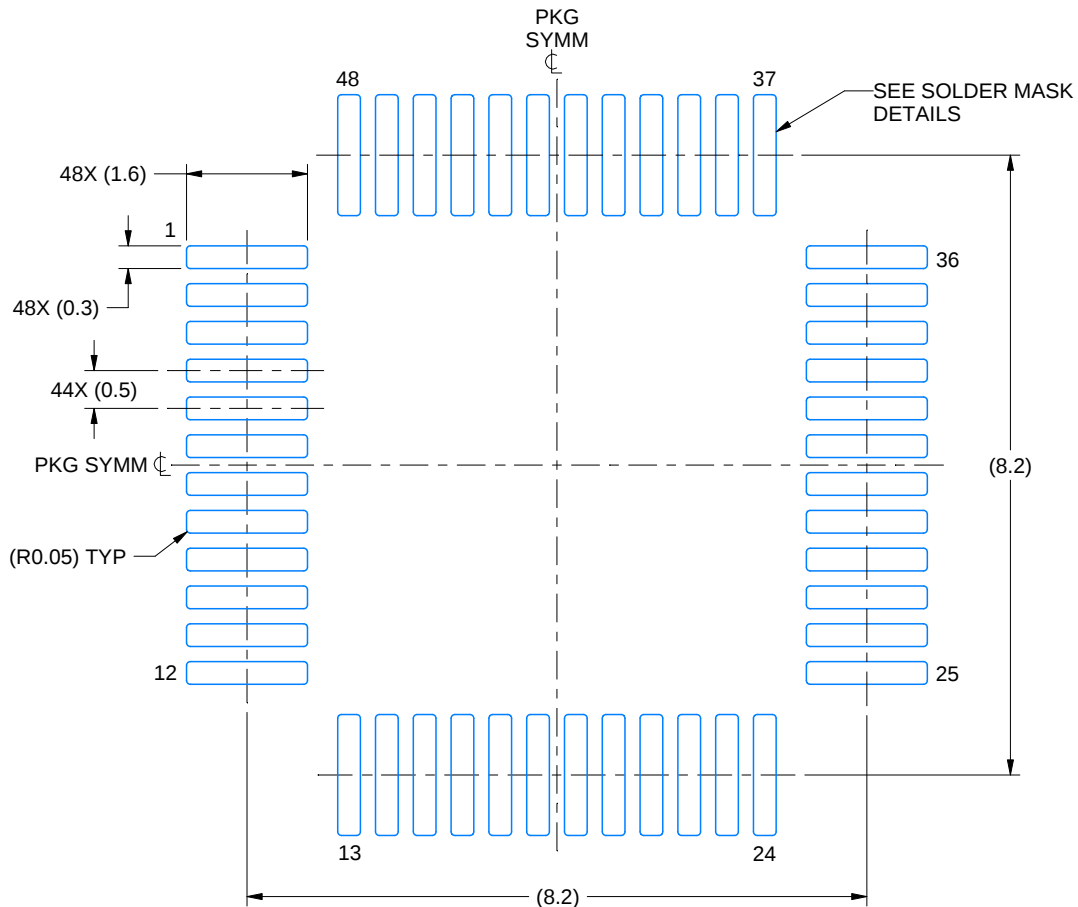
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.
4. This may also be a thermally enhanced plastic package with leads connected to the die pads.

EXAMPLE BOARD LAYOUT

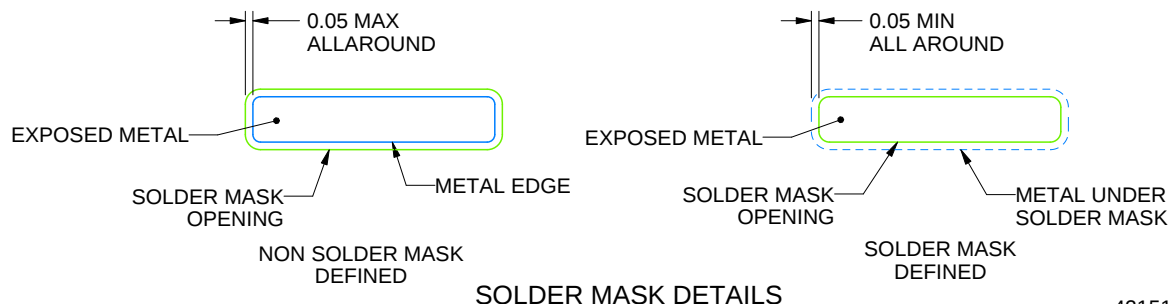
PT0048A

LQFP - 1.6 mm max height

LOW PROFILE QUAD FLATPACK



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE 10.000



SOLDER MASK DETAILS

4215159/B 11/2023

NOTES: (continued)

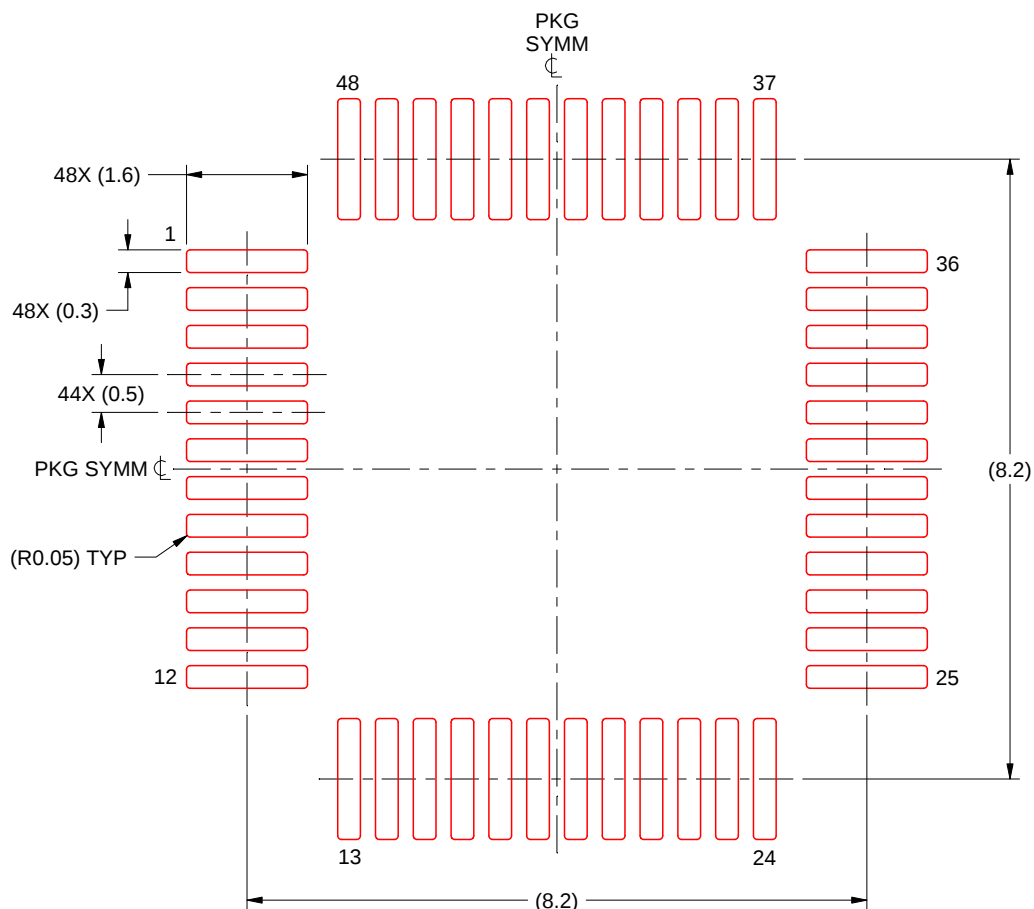
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PT0048A

LQFP - 1.6 mm max height

LOW PROFILE QUAD FLATPACK



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 10X

4215159/B 11/2023

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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