

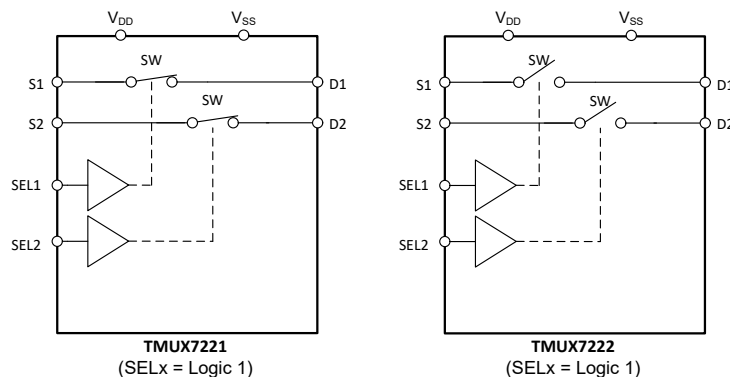
# TMUX722x 44 V、低 RON、1 : 1 (SPST)、2 チャンネル高精度スイッチ、ラッチアップ・フリー、1.8V ロジック対応

## 1 特長

- ラッチアップ・フリー
- 両電源電圧範囲:  $\pm 4.5\text{V} \sim \pm 22\text{V}$
- 単電源電圧範囲:  $4.5\text{V} \sim 44\text{V}$
- 低オン抵抗:  $2.1\Omega$
- 動作温度範囲:  $-40^\circ\text{C} \sim +125^\circ\text{C}$
- 1.8V ロジック互換
- ロジック・ピンにプルダウン抵抗を内蔵
- フェイルセーフ・ロジック
- レール・ツー・レール動作
- 双方向動作

## 2 アプリケーション

- 光学ネットワーク機器
- 光学テスト機器
- HVAC コントローラ
- 超音波スキャナ
- アクティブ・オシロスコープ・プローブ
- ファクトリ・オートメーションと産業用制御
- プログラマブル・ロジック・コントローラ (PLC)
- アナログ入力モジュール
- 半導体試験装置
- 医療的監視と診断
- 有線ネットワーク
- データ・アキュイジション・システム



ブロック図

## 3 概要

TMUX722x は、デュアル チャンネル、1:1 (SPST) 構成、ラッチアップ フリーの相補型金属酸化膜半導体 (CMOS) スイッチです。これらのデバイスは、単電源 ( $4.5\text{V} \sim 44\text{V}$ )、両電源 ( $\pm 4.5\text{V} \sim \pm 22\text{V}$ )、または非対称電源 ( $V_{DD} = 12\text{V}$ ,  $V_{SS} = -5\text{V}$  など) で動作します。TMUX722x は、ソース (Sx) およびドレイン (D) ピンで、 $V_{SS}$  から  $V_{DD}$  までの範囲の双方向アナログおよびデジタル信号をサポートします。

TMUX722x は、SEL ピンを制御して信号パス 1 (S1 から D1) または信号パス 2 (S2 から D2) をオンにすることで、イネーブルまたはディセーブルにできます。すべてのロジック制御入力は、 $1.8\text{V} \sim V_{DD}$  のロジックレベルをサポートしており、有効な電源電圧範囲で動作している場合、TTL ロジックと CMOS ロジックの両方の互換性を確保できます。フェイルセーフ ロジック回路により、電源ピンよりも先に制御ピンに電圧が印加されるため、デバイスへの損傷の可能性が避けられます。詳細については、[セクション 7.3.5](#) を参照してください。

TMUX72xx ファミリーはラッチアップ フリーであるため、一般的に過電圧イベントによって発生するデバイス内の寄生構造間の好ましくない大電流イベントを防止できます。ラッチアップ状態は通常、電源レールがオフにされるまで継続するため、デバイスの障害の原因となる場合があります。このラッチアップ フリーという特長により、TMUX72xx スイッチおよびマルチプレクサ ファミリーは過酷な環境でも使用できます。

### パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ (2)
TMUX7221 TMUX7222	DGS (VSSOP, 10)	3 mm × 4.9 mm

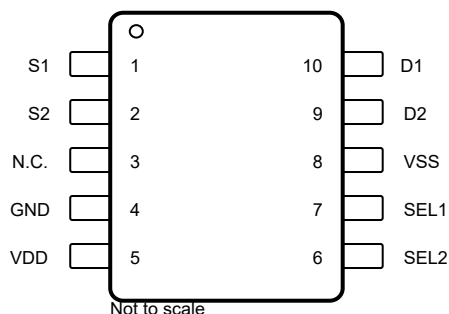
- 詳細については、[セクション 11](#) を参照してください。
- パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



## Table of Contents

<b>1 特長</b> .....	<b>1</b>	6.8 Off Isolation.....	<b>22</b>
<b>2 アプリケーション</b> .....	<b>1</b>	6.9 Crosstalk.....	<b>23</b>
<b>3 概要</b> .....	<b>1</b>	6.10 Bandwidth.....	<b>23</b>
<b>4 Pin Configuration and Functions</b> .....	<b>3</b>	6.11 THD + Noise.....	<b>24</b>
<b>5 Specifications</b> .....	<b>4</b>	6.12 Power Supply Rejection Ratio (PSRR).....	<b>24</b>
5.1 Absolute Maximum Ratings.....	4	<b>7 Detailed Description</b> .....	<b>25</b>
5.2 ESD Ratings.....	4	7.1 Overview.....	25
5.3 Thermal Information.....	5	7.2 Functional Block Diagram.....	25
5.4 Recommended Operating Conditions.....	5	7.3 Feature Description.....	25
5.5 Source or Drain Continuous Current.....	5	7.4 Device Functional Modes.....	27
5.6 $\pm 15$ V Dual Supply: Electrical Characteristics .....	6	7.5 Truth Tables.....	27
5.7 $\pm 15$ V Dual Supply: Switching Characteristics .....	7	<b>8 Application and Implementation</b> .....	<b>28</b>
5.8 $\pm 20$ V Dual Supply: Electrical Characteristics.....	8	8.1 Application Information.....	28
5.9 $\pm 20$ V Dual Supply: Switching Characteristics.....	9	8.2 Typical Applications.....	28
5.10 44 V Single Supply: Electrical Characteristics .....	10	8.3 Power Supply Recommendations.....	30
5.11 44 V Single Supply: Switching Characteristics .....	11	8.4 Layout.....	30
5.12 12 V Single Supply: Electrical Characteristics .....	12	<b>9 Device and Documentation Support</b> .....	<b>32</b>
5.13 12 V Single Supply: Switching Characteristics .....	13	9.1 Documentation Support.....	32
5.14 Typical Characteristics.....	14	9.2 Receiving Notification of Documentation Updates....	32
<b>6 Parameter Measurement Information</b> .....	<b>19</b>	9.3 サポート・リソース.....	32
6.1 On-Resistance.....	19	9.4 Trademarks.....	32
6.2 Off-Leakage Current.....	19	9.5 静電気放電に関する注意事項.....	32
6.3 On-Leakage Current.....	20	9.6 用語集.....	32
6.4 $t_{ON(EN)}$ and $t_{OFF(EN)}$ .....	20	<b>10 Revision History</b> .....	<b>32</b>
6.5 $t_{ON(VDD)}$ Time.....	21	<b>11 Mechanical, Packaging, and Orderable Information</b> .....	<b>33</b>
6.6 Propagation Delay.....	21		
6.7 Charge Injection.....	22		

## 4 Pin Configuration and Functions



**図 4-1. DGS Package,  
10-Pin VSSOP  
(Top View)**

**表 4-1. Pin Functions**

PIN		TYPE <sup>(1)</sup>	DESCRIPTION <sup>(2)</sup>
NAME	NO.		
S1	1	I/O	Source pin 1. Can be an input or output.
S2	2	I/O	Source pin 2. Can be an input or output.
N.C.	3	—	No internal connection. Can be shorted to GND or left floating.
GND	4	P	Ground (0 V) reference
V <sub>DD</sub>	5	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V <sub>DD</sub> and GND.
SEL2	6	I	Logic control input, has internal pull-down resistor. Controls the switch connection. For more information, see <a href="#">セクション 7.5</a> .
SEL1	7	I	Logic control input, has internal pull-down resistor. Controls the switch connection. For more information, see <a href="#">セクション 7.5</a> .
V <sub>SS</sub>	8	P	Negative power supply. This pin is the most negative power-supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V <sub>SS</sub> and GND.
D2	9	I/O	Drain pin 2. Can be an input or output.
D1	10	I/O	Drain pin 1. Can be an input or output.

(1) I = input, O = output, I/O = input and output, P = power.

(2) For what to do with unused pins, refer to [セクション 7.4](#).

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1) (2)</sup>

		MIN	MAX	UNIT
$V_{DD} - V_{SS}$	Supply voltage		48	V
$V_{DD}$		–0.5	48	V
$V_{SS}$		–48	0.5	V
$V_{SEL}$ or $V_{EN}$	Logic control input pin voltage (SELx)	–0.5	48	V
$I_{SEL}$ or $I_{EN}$	Logic control input pin current (SELx)	–30	30	mA
$V_S$ or $V_D$	Source or drain voltage (Sx, Dx)	$V_{SS}-0.5$	$V_{DD}+0.5$	V
$I_{IK}$	Diode clamp current <sup>(3)</sup>	–30	30	mA
$I_S$ or $I_D$ (CONT)	Source or drain continuous current (Sx, Dx)		$I_{DC} + 10\%$ <sup>(4)</sup>	mA
$T_A$	Ambient temperature	–55	150	°C
$T_{stg}$	Storage temperature	–65	150	°C
$T_J$	Junction temperature		150	°C
$P_{tot}$	Total power dissipation (VSSOP) <sup>(5)</sup>		450	mW

- (1) Operation outside the *Absolute Maximum Rating* may cause permanent device damage. *Absolute Maximum Rating* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Condition*. If used outside the *Recommended Operating Condition* but within the *Absolute Maximum Rating*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltages are with respect to ground, unless otherwise specified.
- (3) Pins are diode-clamped to the power-supply rails. Over voltage signals must be voltage and current limited to maximum ratings.
- (4) Refer to *Source or Drain Continuous Current* table for  $I_{DC}$  specifications.
- (5) For VSSOP package:  $P_{tot}$  derates linearly above  $T_A = 70^\circ\text{C}$  by  $6.7\text{mW}/^\circ\text{C}$ .

### 5.2 ESD Ratings

			VALUE	UNIT
<b>TMUX722x</b>				
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins <sup>(1)</sup>	±2000	V
		Charged device model (CDM), per ANSI/ESDA/ JEDEC JS-002, all pins <sup>(2)</sup>	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TMUX722x	UNIT
		DGS (VSSOP)	
		10 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	154.3	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	52.9	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	75.3	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	5.9	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	73.9	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

### 5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>DD</sub> – V <sub>SS</sub> <sup>(1)</sup>	Power supply voltage differential	4.5		44	V
V <sub>DD</sub>	Positive power supply voltage	4.5		44	V
V <sub>S</sub> or V <sub>D</sub>	Signal path input/output voltage (source or drain pin) (Sx, D)	V <sub>SS</sub>		V <sub>DD</sub>	V
V <sub>SEL</sub> or V <sub>EN</sub>	Address or enable pin voltage	0		44	V
I <sub>S</sub> or I <sub>D</sub> (CONT)	Source or drain continuous current (Sx, D)			I <sub>DC</sub> <sup>(2)</sup>	mA
T <sub>A</sub>	Ambient temperature	–40		125	°C

(1) V<sub>DD</sub> and V<sub>SS</sub> can be any value as long as 4.5 V ≤ (V<sub>DD</sub> – V<sub>SS</sub>) ≤ 44 V, and the minimum V<sub>DD</sub> is met.

(2) Refer to *Source or Drain Continuous Current* table for I<sub>DC</sub> specifications.

### 5.5 Source or Drain Continuous Current

at supply voltage of V<sub>DD</sub> ± 10%, V<sub>SS</sub> ± 10 % (unless otherwise noted)

CONTINUOUS CURRENT PER CHANNEL (I <sub>DC</sub> ) <sup>(2)</sup>		T <sub>A</sub> = 25°C	T <sub>A</sub> = 85°C	T <sub>A</sub> = 125°C	UNIT
PACKAGE	TEST CONDITIONS				
DGS (VSSOP)	+44 V Single Supply <sup>(1)</sup>	380	260	130	mA
	±15 V Dual Supply	380	260	130	mA
	+12 V Single Supply	280	190	100	mA
	±5 V Dual Supply	240	160	90	mA

(1) Specified for nominal supply voltage only.

(2) Refer to Total power dissipation (P<sub>tot</sub>) limits in *Absolute Maximum Ratings* table that must be followed with max continuous current specification.

## 5.6 ±15 V Dual Supply: Electrical Characteristics

$V_{DD} = +15\text{ V} \pm 10\%$ ,  $V_{SS} = -15\text{ V} \pm 10\%$ , GND = 0 V (unless otherwise noted)

Typical at  $V_{DD} = +15\text{ V}$ ,  $V_{SS} = -15\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T <sub>A</sub>	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R <sub>ON</sub>	On-resistance	V <sub>S</sub> = −10 V to +10 V I <sub>D</sub> = −10 mA	25°C		2.1	2.9	Ω
			−40°C to +85°C			3.8	Ω
			−40°C to +125°C			4.5	Ω
ΔR <sub>ON</sub>	On-resistance mismatch between channels	V <sub>S</sub> = −10 V to +10 V I <sub>D</sub> = −10 mA	25°C		0.05	0.25	Ω
			−40°C to +85°C			0.3	Ω
			−40°C to +125°C			0.35	Ω
R <sub>ON FLAT</sub>	On-resistance flatness	V <sub>S</sub> = −10 V to +10 V I <sub>S</sub> = −10 mA	25°C		0.5	0.6	Ω
			−40°C to +85°C			0.7	Ω
			−40°C to +125°C			0.85	Ω
R <sub>ON DRIFT</sub>	On-resistance drift	V <sub>S</sub> = 0 V, I <sub>S</sub> = −10 mA	−40°C to +125°C		0.01		Ω/°C
I <sub>S(OFF)</sub>	Source off leakage current <sup>(1)</sup>	V <sub>DD</sub> = 16.5 V, V <sub>SS</sub> = −16.5 V Switch state is off V <sub>S</sub> = +10 V / −10 V V <sub>D</sub> = −10 V / + 10 V	25°C	−0.15	0.05	0.15	nA
			−40°C to +85°C	−1.6		1.6	nA
			−40°C to +125°C	−15		15	nA
I <sub>D(OFF)</sub>	Drain off leakage current <sup>(1)</sup>	V <sub>DD</sub> = 16.5 V, V <sub>SS</sub> = −16.5 V Switch state is off V <sub>S</sub> = +10 V / −10 V V <sub>D</sub> = −10 V / + 10 V	25°C	−0.15	0.05	0.15	nA
			−40°C to +85°C	−1.6		1.6	nA
			−40°C to +125°C	−15		15	nA
I <sub>S(ON)</sub> I <sub>D(ON)</sub>	Channel on leakage current <sup>(2)</sup>	V <sub>DD</sub> = 16.5 V, V <sub>SS</sub> = −16.5 V Switch state is on V <sub>S</sub> = V <sub>D</sub> = ±10 V	25°C	−0.15	0.05	0.15	nA
			−40°C to +85°C	−1.6		1.6	nA
			−40°C to +125°C	−15		15	nA
LOGIC INPUTS (SEL / EN pins)							
V <sub>IH</sub>	Logic voltage high		−40°C to +125°C	1.3		44	V
V <sub>IL</sub>	Logic voltage low		−40°C to +125°C	0		0.8	V
I <sub>IH</sub>	Input leakage current		−40°C to +125°C		1	2.5	μA
I <sub>IL</sub>	Input leakage current		−40°C to +125°C	−0.1	−0.005		μA
C <sub>IN</sub>	Logic input capacitance		−40°C to +125°C		3.5		pF
POWER SUPPLY							
I <sub>DD</sub>	V <sub>DD</sub> supply current	V <sub>DD</sub> = 16.5 V, V <sub>SS</sub> = −16.5 V Logic inputs = 0 V, 5 V, or V <sub>DD</sub>	25°C		30	47	μA
			−40°C to +85°C			55	μA
			−40°C to +125°C			72	μA
I <sub>SS</sub>	V <sub>SS</sub> supply current	V <sub>DD</sub> = 16.5 V, V <sub>SS</sub> = −16.5 V Logic inputs = 0 V, 5 V, or V <sub>DD</sub>	25°C		7	15	μA
			−40°C to +85°C			20	μA
			−40°C to +125°C			30	μA

(1) When  $V_S$  is positive,  $V_D$  is negative, or when  $V_S$  is negative,  $V_D$  is positive.

(2) When  $V_S$  is at a voltage potential,  $V_D$  is floating, or when  $V_D$  is at a voltage potential,  $V_S$  is floating.

## 5.7 ±15 V Dual Supply: Switching Characteristics

$V_{DD} = +15\text{ V} \pm 10\%$ ,  $V_{SS} = -15\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$  (unless otherwise noted)

Typical at  $V_{DD} = +15\text{ V}$ ,  $V_{SS} = -15\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A$	MIN	TYP	MAX	UNIT
$t_{ON}$	Turn-on time from control input	$V_S = 10\text{ V}$ $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$	$25^\circ\text{C}$		145	180	ns
			$-40^\circ\text{C}$ to $+85^\circ\text{C}$			190	ns
			$-40^\circ\text{C}$ to $+125^\circ\text{C}$			200	ns
$t_{OFF}$	Turn-off time from control input	$V_S = 10\text{ V}$ $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$	$25^\circ\text{C}$		100	180	ns
			$-40^\circ\text{C}$ to $+85^\circ\text{C}$			195	ns
			$-40^\circ\text{C}$ to $+125^\circ\text{C}$			210	ns
$t_{ON(VDD)}$	Device turn on time ( $V_{DD}$ to output)	$V_{DD}$ rise time = $1\ \mu\text{s}$ $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$	$25^\circ\text{C}$		0.19		ms
			$-40^\circ\text{C}$ to $+85^\circ\text{C}$		0.2		ms
			$-40^\circ\text{C}$ to $+125^\circ\text{C}$		0.2		ms
$t_{PD}$	Propagation delay	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$	$25^\circ\text{C}$		500		ps
$Q_{INJ}$	Charge injection	$V_S = 0\text{ V}$ , $C_L = 100\text{ pF}$	$25^\circ\text{C}$		-15		pC
$O_{ISO}$	Off-isolation	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $V_S = 0\text{ V}$ , $f = 100\text{ kHz}$	$25^\circ\text{C}$		-70		dB
$O_{ISO}$	Off-isolation	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $V_S = 0\text{ V}$ , $f = 1\text{ MHz}$	$25^\circ\text{C}$		-50		dB
$X_{TALK}$	Crosstalk	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $V_S = 0\text{ V}$ , $f = 100\text{ kHz}$	$25^\circ\text{C}$		-114		dB
$X_{TALK}$	Crosstalk	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $V_S = 0\text{ V}$ , $f = 1\text{ MHz}$	$25^\circ\text{C}$		-93		dB
BW	-3dB Bandwidth	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $V_S = 0\text{ V}$	$25^\circ\text{C}$		45		MHz
$I_L$	Insertion loss	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $V_S = 0\text{ V}$ , $f = 1\text{ MHz}$	$25^\circ\text{C}$		-0.18		dB
ACPSRR	AC Power Supply Rejection Ratio	$V_{PP} = 0.62\text{ V}$ on $V_{DD}$ and $V_{SS}$ $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$	$25^\circ\text{C}$		-71		dB
THD+N	Total Harmonic Distortion + Noise	$V_{PP} = 15\text{ V}$ , $V_{BIAS} = 0\text{ V}$ $R_L = 10\text{ k}\Omega$ , $C_L = 5\text{ pF}$ , $f = 20\text{ Hz}$ to $20\text{ kHz}$	$25^\circ\text{C}$		0.0005		%
$C_{S(OFF)}$	Source off capacitance	$V_S = 0\text{ V}$ , $f = 1\text{ MHz}$	$25^\circ\text{C}$		25		pF
$C_{D(OFF)}$	Drain off capacitance	$V_S = 0\text{ V}$ , $f = 1\text{ MHz}$	$25^\circ\text{C}$		33		pF
$C_{S(ON)}$ , $C_{D(ON)}$	On capacitance	$V_S = 0\text{ V}$ , $f = 1\text{ MHz}$	$25^\circ\text{C}$		120		pF

## 5.8 ±20 V Dual Supply: Electrical Characteristics

$V_{DD} = +20\text{ V} \pm 10\%$ ,  $V_{SS} = -20\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$  (unless otherwise noted)

Typical at  $V_{DD} = +20\text{ V}$ ,  $V_{SS} = -20\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T <sub>A</sub>	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R <sub>ON</sub>	On-resistance	V <sub>S</sub> = −15 V to +15 V I <sub>D</sub> = −10 mA	25°C		1.9	2.7	Ω
			−40°C to +85°C			3.5	Ω
			−40°C to +125°C			4.2	Ω
ΔR <sub>ON</sub>	On-resistance mismatch between channels	V <sub>S</sub> = −15 V to +15 V I <sub>D</sub> = −10 mA	25°C		0.04	0.22	Ω
			−40°C to +85°C			0.28	Ω
			−40°C to +125°C			0.3	Ω
R <sub>ON FLAT</sub>	On-resistance flatness	V <sub>S</sub> = −15 V to +15 V I <sub>S</sub> = −10 mA	25°C		0.3	0.75	Ω
			−40°C to +85°C			0.9	Ω
			−40°C to +125°C			1.2	Ω
R <sub>ON DRIFT</sub>	On-resistance drift	V <sub>S</sub> = 0 V, I <sub>S</sub> = −10 mA	−40°C to +125°C		0.009		Ω/°C
I <sub>S(OFF)</sub>	Source off leakage current <sup>(1)</sup>	V <sub>DD</sub> = 22 V, V <sub>SS</sub> = −22 V Switch state is off V <sub>S</sub> = +15 V / −15 V V <sub>D</sub> = −15 V / +15 V	25°C	−1.5	0.05	1.5	nA
			−40°C to +85°C	−4		4	nA
			−40°C to +125°C	−24		24	nA
I <sub>D(OFF)</sub>	Drain off leakage current <sup>(1)</sup>	V <sub>DD</sub> = 22 V, V <sub>SS</sub> = −22 V Switch state is off V <sub>S</sub> = +15 V / −15 V V <sub>D</sub> = −15 V / +15 V	25°C	−1.5	0.05	1.5	nA
			−40°C to +85°C	−4		4	nA
			−40°C to +125°C	−24		24	nA
I <sub>S(ON)</sub> I <sub>D(ON)</sub>	Channel on leakage current <sup>(2)</sup>	V <sub>DD</sub> = 22 V, V <sub>SS</sub> = −22 V Switch state is on V <sub>S</sub> = V <sub>D</sub> = ±15 V	25°C	−1.5	0.05	1.5	nA
			−40°C to +85°C	−4		4	nA
			−40°C to +125°C	−24		24	nA
LOGIC INPUTS (SEL / EN pins)							
V <sub>IH</sub>	Logic voltage high		−40°C to +125°C	1.3		44	V
V <sub>IL</sub>	Logic voltage low		−40°C to +125°C	0		0.8	V
I <sub>IH</sub>	Input leakage current		−40°C to +125°C		0.5	2	μA
I <sub>IL</sub>	Input leakage current		−40°C to +125°C	−0.1	−0.005		μA
C <sub>IN</sub>	Logic input capacitance		−40°C to +125°C		3.5		pF
POWER SUPPLY							
I <sub>DD</sub>	V <sub>DD</sub> supply current	V <sub>DD</sub> = 22 V, V <sub>SS</sub> = −22 V Logic inputs = 0 V, 5 V, or V <sub>DD</sub>	25°C		38	55	μA
			−40°C to +85°C			61	μA
			−40°C to +125°C			81	μA
I <sub>SS</sub>	V <sub>SS</sub> supply current	V <sub>DD</sub> = 22 V, V <sub>SS</sub> = −22 V Logic inputs = 0 V, 5 V, or V <sub>DD</sub>	25°C		8	15	μA
			−40°C to +85°C			19	μA
			−40°C to +125°C			37	μA

(1) When  $V_S$  is positive,  $V_D$  is negative, or when  $V_S$  is negative,  $V_D$  is positive.

(2) When  $V_S$  is at a voltage potential,  $V_D$  is floating, or when  $V_D$  is at a voltage potential,  $V_S$  is floating.



## 5.9 ±20 V Dual Supply: Switching Characteristics

$V_{DD} = +20\text{ V} \pm 10\%$ ,  $V_{SS} = -20\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$  (unless otherwise noted)

Typical at  $V_{DD} = +20\text{ V}$ ,  $V_{SS} = -20\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A$	MIN	TYP	MAX	UNIT
$t_{ON}$	Turn-on time from control input	$V_S = 10\text{ V}$ $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$	$25^\circ\text{C}$		110	170	ns
			$-40^\circ\text{C}$ to $+85^\circ\text{C}$			185	ns
			$-40^\circ\text{C}$ to $+125^\circ\text{C}$			200	ns
$t_{OFF}$	Turn-off time from control input	$V_S = 10\text{ V}$ $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$	$25^\circ\text{C}$		90	180	ns
			$-40^\circ\text{C}$ to $+85^\circ\text{C}$			190	ns
			$-40^\circ\text{C}$ to $+125^\circ\text{C}$			200	ns
$t_{ON(VDD)}$	Device turn on time ( $V_{DD}$ to output)	$V_{DD}$ rise time = $1\ \mu\text{s}$ $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$	$25^\circ\text{C}$		0.18		ms
			$-40^\circ\text{C}$ to $+85^\circ\text{C}$		0.2		ms
			$-40^\circ\text{C}$ to $+125^\circ\text{C}$		0.2		ms
$t_{PD}$	Propagation delay	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$	$25^\circ\text{C}$		500		ps
$Q_{INJ}$	Charge injection	$V_S = 0\text{ V}$ , $C_L = 100\text{ pF}$	$25^\circ\text{C}$		-20		pC
$O_{ISO}$	Off-isolation	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $V_S = 0\text{ V}$ , $f = 100\text{ kHz}$	$25^\circ\text{C}$		-70		dB
$O_{ISO}$	Off-isolation	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $V_S = 0\text{ V}$ , $f = 1\text{ MHz}$	$25^\circ\text{C}$		-50		dB
$X_{TALK}$	Crosstalk	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $V_S = 0\text{ V}$ , $f = 100\text{ kHz}$	$25^\circ\text{C}$		-112		dB
$X_{TALK}$	Crosstalk	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $V_S = 0\text{ V}$ , $f = 1\text{ MHz}$	$25^\circ\text{C}$		-93		dB
BW	-3dB Bandwidth	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $V_S = 0\text{ V}$	$25^\circ\text{C}$		45		MHz
$I_L$	Insertion loss	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $V_S = 0\text{ V}$ , $f = 1\text{ MHz}$	$25^\circ\text{C}$		-0.16		dB
ACPSRR	AC Power Supply Rejection Ratio	$V_{PP} = 0.62\text{ V}$ on $V_{DD}$ and $V_{SS}$ $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$	$25^\circ\text{C}$		-69		dB
THD+N	Total Harmonic Distortion + Noise	$V_{PP} = 20\text{ V}$ , $V_{BIAS} = 0\text{ V}$ $R_L = 10\text{ k}\Omega$ , $C_L = 5\text{ pF}$ , $f = 20\text{ Hz}$ to $20\text{ kHz}$	$25^\circ\text{C}$		0.0005		%
$C_{S(OFF)}$	Source off capacitance	$V_S = 0\text{ V}$ , $f = 1\text{ MHz}$	$25^\circ\text{C}$		25		pF
$C_{D(OFF)}$	Drain off capacitance	$V_S = 0\text{ V}$ , $f = 1\text{ MHz}$	$25^\circ\text{C}$		32		pF
$C_{S(ON)}$ , $C_{D(ON)}$	On capacitance	$V_S = 0\text{ V}$ , $f = 1\text{ MHz}$	$25^\circ\text{C}$		120		pF

## 5.10 44 V Single Supply: Electrical Characteristics

$V_{DD} = +44\text{ V}$ ,  $V_{SS} = 0\text{ V}$ , GND = 0 V (unless otherwise noted)

Typical at  $V_{DD} = +44\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T <sub>A</sub>	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R <sub>ON</sub>	On-resistance	V <sub>S</sub> = 0 V to 40 V I <sub>D</sub> = −10 mA	25°C		2.2	2.8	Ω
			−40°C to +85°C			3.6	Ω
			−40°C to +125°C			4.2	Ω
ΔR <sub>ON</sub>	On-resistance mismatch between channels	V <sub>S</sub> = 0 V to 40 V I <sub>D</sub> = −10 mA	25°C		0.1	0.23	Ω
			−40°C to +85°C			0.3	Ω
			−40°C to +125°C			0.35	Ω
R <sub>ON FLAT</sub>	On-resistance flatness	V <sub>S</sub> = 0 V to 40 V I <sub>D</sub> = −10 mA	25°C		0.2	1	Ω
			−40°C to +85°C			1.3	Ω
			−40°C to +125°C			1.5	Ω
R <sub>ON DRIFT</sub>	On-resistance drift	V <sub>S</sub> = 22 V, I <sub>S</sub> = −10 mA	−40°C to +125°C		0.008		Ω/°C
I <sub>S(OFF)</sub>	Source off leakage current <sup>(1)</sup>	V <sub>DD</sub> = 44 V, V <sub>SS</sub> = 0 V Switch state is off V <sub>S</sub> = 40 V / 1 V V <sub>D</sub> = 1 V / 40 V	25°C	−5	0.05	5	nA
			−40°C to +85°C	−10		10	nA
			−40°C to +125°C	−35		35	nA
I <sub>D(OFF)</sub>	Drain off leakage current <sup>(1)</sup>	V <sub>DD</sub> = 44 V, V <sub>SS</sub> = 0 V Switch state is off V <sub>S</sub> = 40 V / 1 V V <sub>D</sub> = 1 V / 40 V	25°C	−5	0.05	5	nA
			−40°C to +85°C	−10		10	nA
			−40°C to +125°C	−35		35	nA
I <sub>S(ON)</sub> I <sub>D(ON)</sub>	Channel on leakage current <sup>(2)</sup>	V <sub>DD</sub> = 44 V, V <sub>SS</sub> = 0 V Switch state is on V <sub>S</sub> = V <sub>D</sub> = 40 V or 1 V	25°C	−5	0.05	5	nA
			−40°C to +85°C	−10		10	nA
			−40°C to +125°C	−35		35	nA
LOGIC INPUTS (SEL / EN pins)							
V <sub>IH</sub>	Logic voltage high		−40°C to +125°C	1.3		44	V
V <sub>IL</sub>	Logic voltage low		−40°C to +125°C	0		0.8	V
I <sub>IH</sub>	Input leakage current		−40°C to +125°C		0.5	2.75	μA
I <sub>IL</sub>	Input leakage current		−40°C to +125°C	−0.1	−0.005		μA
C <sub>IN</sub>	Logic input capacitance		−40°C to +125°C		3.5		pF
POWER SUPPLY							
I <sub>DD</sub>	V <sub>DD</sub> supply current	V <sub>DD</sub> = 44 V, V <sub>SS</sub> = 0 V Logic inputs = 0 V, 5 V, or V <sub>DD</sub>	25°C		40	62	μA
			−40°C to +85°C			70	μA
			−40°C to +125°C			90	μA

(1) When  $V_S$  is positive,  $V_D$  is negative, or when  $V_S$  is negative,  $V_D$  is positive.

(2) When  $V_S$  is at a voltage potential,  $V_D$  is floating, or when  $V_D$  is at a voltage potential,  $V_S$  is floating.

## 5.11 44 V Single Supply: Switching Characteristics

$V_{DD} = +44\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $GND = 0\text{ V}$  (unless otherwise noted)

Typical at  $V_{DD} = +44\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A$	MIN	TYP	MAX	UNIT
$t_{ON}$	Turn-on time from control input	$V_S = 18\text{ V}$ $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$	$25^\circ\text{C}$		120	168	ns
			$-40^\circ\text{C}$ to $+85^\circ\text{C}$			185	ns
			$-40^\circ\text{C}$ to $+125^\circ\text{C}$			195	ns
$t_{OFF}$	Turn-off time from control input	$V_S = 18\text{ V}$ $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$	$25^\circ\text{C}$		120	180	ns
			$-40^\circ\text{C}$ to $+85^\circ\text{C}$			200	ns
			$-40^\circ\text{C}$ to $+125^\circ\text{C}$			205	ns
$t_{ON(VDD)}$	Device turn on time ( $V_{DD}$ to output)	$V_{DD}$ rise time = $1\ \mu\text{s}$ $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$	$25^\circ\text{C}$		0.15		ms
			$-40^\circ\text{C}$ to $+85^\circ\text{C}$		0.17		ms
			$-40^\circ\text{C}$ to $+125^\circ\text{C}$		0.17		ms
$t_{PD}$	Propagation delay	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$	$25^\circ\text{C}$		500		ps
$Q_{INJ}$	Charge injection	$V_S = 22\text{ V}$ , $C_L = 100\text{ pF}$	$25^\circ\text{C}$		-16		pC
$O_{ISO}$	Off-isolation	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $V_S = 6\text{ V}$ , $f = 100\text{ kHz}$	$25^\circ\text{C}$		-70		dB
$O_{ISO}$	Off-isolation	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $V_S = 6\text{ V}$ , $f = 1\text{ MHz}$	$25^\circ\text{C}$		-50		dB
$X_{TALK}$	Crosstalk	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $V_S = 6\text{ V}$ , $f = 100\text{ kHz}$	$25^\circ\text{C}$		-112		dB
$X_{TALK}$	Crosstalk	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $V_S = 6\text{ V}$ , $f = 1\text{ MHz}$	$25^\circ\text{C}$		-93		dB
BW	-3dB Bandwidth	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $V_S = 6\text{ V}$	$25^\circ\text{C}$		45		MHz
$I_L$	Insertion loss	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $V_S = 6\text{ V}$ , $f = 1\text{ MHz}$	$25^\circ\text{C}$		-0.18		dB
ACPSRR	AC Power Supply Rejection Ratio	$V_{PP} = 0.62\text{ V}$ on $V_{DD}$ and $V_{SS}$ $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$	$25^\circ\text{C}$		-70		dB
THD+N	Total Harmonic Distortion + Noise	$V_{PP} = 22\text{ V}$ , $V_{BIAS} = 22\text{ V}$ $R_L = 10\text{ k}\Omega$ , $C_L = 5\text{ pF}$ , $f = 20\text{ Hz}$ to $20\text{ kHz}$	$25^\circ\text{C}$		0.0004		%
$C_{S(OFF)}$	Source off capacitance	$V_S = 22\text{ V}$ , $f = 1\text{ MHz}$	$25^\circ\text{C}$		25		pF
$C_{D(OFF)}$	Drain off capacitance	$V_S = 22\text{ V}$ , $f = 1\text{ MHz}$	$25^\circ\text{C}$		34		pF
$C_{S(ON)}$ , $C_{D(ON)}$	On capacitance	$V_S = 22\text{ V}$ , $f = 1\text{ MHz}$	$25^\circ\text{C}$		120		pF

## 5.12 12 V Single Supply: Electrical Characteristics

$V_{DD} = +12\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $GND = 0\text{ V}$  (unless otherwise noted)

Typical at  $V_{DD} = +12\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T <sub>A</sub>	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R <sub>ON</sub>	On-resistance	V <sub>S</sub> = 0 V to 10 V I <sub>D</sub> = −10 mA	25°C		4.6	6	Ω
			−40°C to +85°C			7.5	Ω
			−40°C to +125°C			8.4	Ω
ΔR <sub>ON</sub>	On-resistance mismatch between channels	V <sub>S</sub> = 0 V to 10 V I <sub>D</sub> = −10 mA	25°C		0.08	0.2	Ω
			−40°C to +85°C			0.32	Ω
			−40°C to +125°C			0.35	Ω
R <sub>ON FLAT</sub>	On-resistance flatness	V <sub>S</sub> = 0 V to 10 V I <sub>S</sub> = −10 mA	25°C		1.2	2	Ω
			−40°C to +85°C			2.2	Ω
			−40°C to +125°C			2.4	Ω
R <sub>ON DRIFT</sub>	On-resistance drift	V <sub>S</sub> = 6 V, I <sub>S</sub> = −10 mA	−40°C to +125°C		0.017		Ω/°C
I <sub>S(OFF)</sub>	Source off leakage current <sup>(1)</sup>	V <sub>DD</sub> = 13.2 V, V <sub>SS</sub> = 0 V Switch state is off V <sub>S</sub> = 10 V / 1 V V <sub>D</sub> = 1 V / 10 V	25°C	−0.5	0.05	0.5	nA
			−40°C to +85°C	−2		2	nA
			−40°C to +125°C	−12		12	nA
I <sub>D(OFF)</sub>	Drain off leakage current <sup>(1)</sup>	V <sub>DD</sub> = 13.2 V, V <sub>SS</sub> = 0 V Switch state is off V <sub>S</sub> = 10 V / 1 V V <sub>D</sub> = 1 V / 10 V	25°C	−0.5	0.05	0.5	nA
			−40°C to +85°C	−2		2	nA
			−40°C to +125°C	−12		12	nA
I <sub>S(ON)</sub> I <sub>D(ON)</sub>	Channel on leakage current <sup>(2)</sup>	V <sub>DD</sub> = 13.2 V, V <sub>SS</sub> = 0 V Switch state is on V <sub>S</sub> = V <sub>D</sub> = 10 V or 1 V	25°C	−0.5	0.05	0.5	nA
			−40°C to +85°C	−2		2	nA
			−40°C to +125°C	−12		12	nA
LOGIC INPUTS (SEL / EN pins)							
V <sub>IH</sub>	Logic voltage high		−40°C to +125°C	1.3		44	V
V <sub>IL</sub>	Logic voltage low		−40°C to +125°C	0		0.8	V
I <sub>IH</sub>	Input leakage current		−40°C to +125°C		0.5	2	μA
I <sub>IL</sub>	Input leakage current		−40°C to +125°C	−0.1	−0.005		μA
C <sub>IN</sub>	Logic input capacitance		−40°C to +125°C		3.5		pF
POWER SUPPLY							
I <sub>DD</sub>	V <sub>DD</sub> supply current	V <sub>DD</sub> = 13.2 V, V <sub>SS</sub> = 0 V Logic inputs = 0 V, 5 V, or V <sub>DD</sub>	25°C		30	40	μA
			−40°C to +85°C			50	μA
			−40°C to +125°C			62	μA

(1) When  $V_S$  is positive,  $V_D$  is negative, or when  $V_S$  is negative,  $V_D$  is positive.

(2) When  $V_S$  is at a voltage potential,  $V_D$  is floating, or when  $V_D$  is at a voltage potential,  $V_S$  is floating.

### 5.13 12 V Single Supply: Switching Characteristics

$V_{DD} = +12\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $GND = 0\text{ V}$  (unless otherwise noted)

Typical at  $V_{DD} = +12\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A$	MIN	TYP	MAX	UNIT
$t_{ON}$	Turn-on time from control input	$V_S = 8\text{ V}$ $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$	$25^\circ\text{C}$		120	180	ns
			$-40^\circ\text{C}$ to $+85^\circ\text{C}$			210	ns
			$-40^\circ\text{C}$ to $+125^\circ\text{C}$			230	ns
$t_{OFF}$	Turn-off time from control input	$V_S = 8\text{ V}$ $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$	$25^\circ\text{C}$		130	210	ns
			$-40^\circ\text{C}$ to $+85^\circ\text{C}$			235	ns
			$-40^\circ\text{C}$ to $+125^\circ\text{C}$			250	ns
$t_{ON(VDD)}$	Device turn on time ( $V_{DD}$ to output)	$V_{DD}$ rise time = $1\ \mu\text{s}$ $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$	$25^\circ\text{C}$		0.19		ms
			$-40^\circ\text{C}$ to $+85^\circ\text{C}$		0.2		ms
			$-40^\circ\text{C}$ to $+125^\circ\text{C}$		0.2		ms
$t_{PD}$	Propagation delay	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$	$25^\circ\text{C}$		500		ps
$Q_{INJ}$	Charge injection	$V_S = 6\text{ V}$ , $C_L = 100\text{ pF}$	$25^\circ\text{C}$		–6		pC
$O_{ISO}$	Off-isolation	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $V_S = 6\text{ V}$ , $f = 100\text{ kHz}$	$25^\circ\text{C}$		–70		dB
$O_{ISO}$	Off-isolation	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $V_S = 6\text{ V}$ , $f = 1\text{ MHz}$	$25^\circ\text{C}$		–50		dB
$X_{TALK}$	Crosstalk	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $V_S = 6\text{ V}$ , $f = 100\text{ kHz}$	$25^\circ\text{C}$		–112		dB
$X_{TALK}$	Crosstalk	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $V_S = 6\text{ V}$ , $f = 1\text{ MHz}$	$25^\circ\text{C}$		–93		dB
BW	–3dB Bandwidth	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $V_S = 6\text{ V}$	$25^\circ\text{C}$		60		MHz
$I_L$	Insertion loss	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $V_S = 6\text{ V}$ , $f = 1\text{ MHz}$	$25^\circ\text{C}$		–0.3		dB
ACPSRR	AC Power Supply Rejection Ratio	$V_{PP} = 0.62\text{ V}$ on $V_{DD}$ and $V_{SS}$ $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$	$25^\circ\text{C}$		–76		dB
THD+N	Total Harmonic Distortion + Noise	$V_{PP} = 6\text{ V}$ , $V_{BIAS} = 6\text{ V}$ $R_L = 10\text{ k}\Omega$ , $C_L = 5\text{ pF}$ , $f = 20\text{ Hz}$ to $20\text{ kHz}$	$25^\circ\text{C}$		0.0009		%
$C_{S(OFF)}$	Source off capacitance	$V_S = 6\text{ V}$ , $f = 1\text{ MHz}$	$25^\circ\text{C}$		30		pF
$C_{D(OFF)}$	Drain off capacitance	$V_S = 6\text{ V}$ , $f = 1\text{ MHz}$	$25^\circ\text{C}$		38		pF
$C_{S(ON)}$ , $C_{D(ON)}$	On capacitance	$V_S = 6\text{ V}$ , $f = 1\text{ MHz}$	$25^\circ\text{C}$		110		pF

## 5.14 Typical Characteristics

at  $T_A = 25^\circ\text{C}$

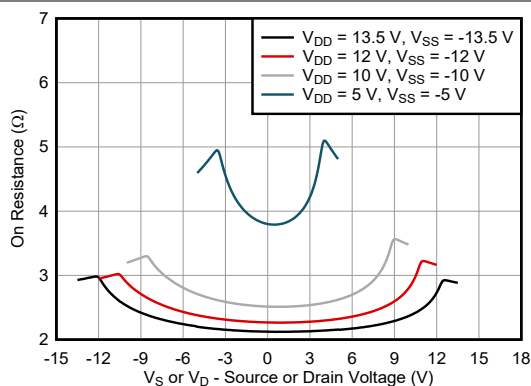


図 5-1. On-Resistance vs Source or Drain Voltage – Dual Supply

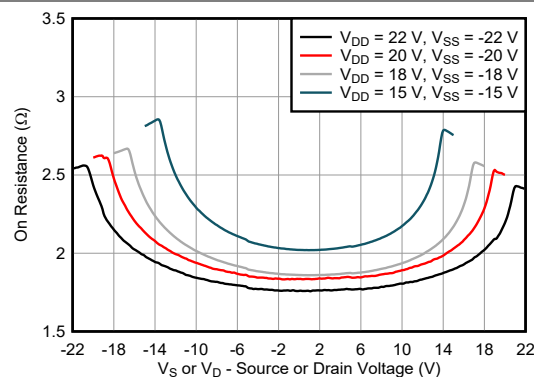


図 5-2. On-Resistance vs Source or Drain Voltage – Dual Supply

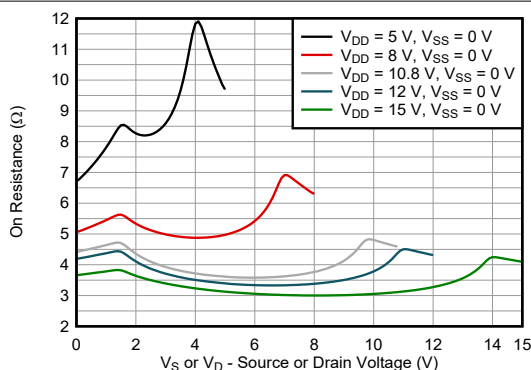


図 5-3. On-Resistance vs Source or Drain Voltage – Single Supply

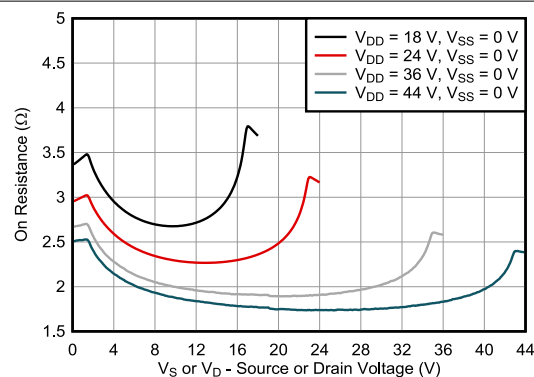


図 5-4. On-Resistance vs Source or Drain Voltage – Single Supply

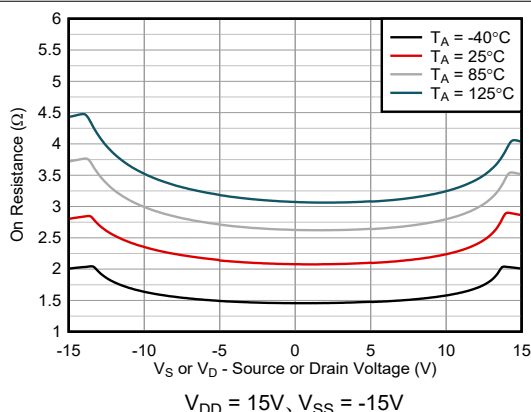


図 5-5. On-Resistance vs Temperature

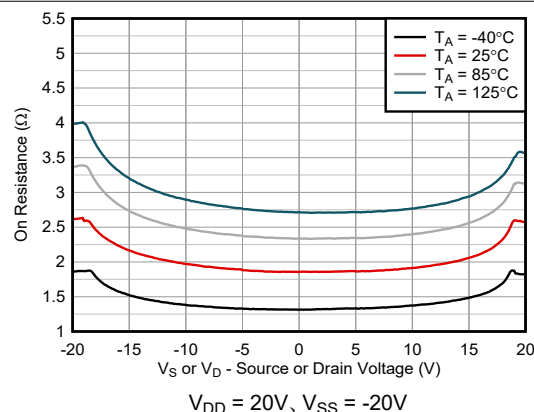


図 5-6. On-Resistance vs Temperature

## 5.14 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$

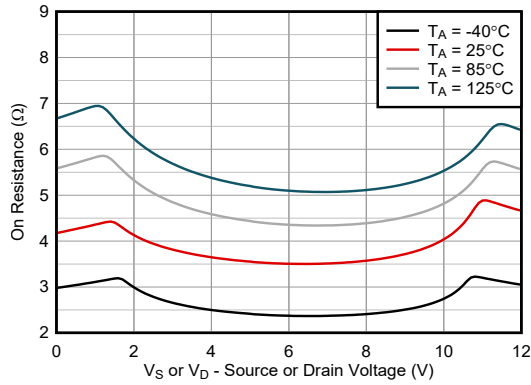


Figure 5-7. On-Resistance vs Temperature

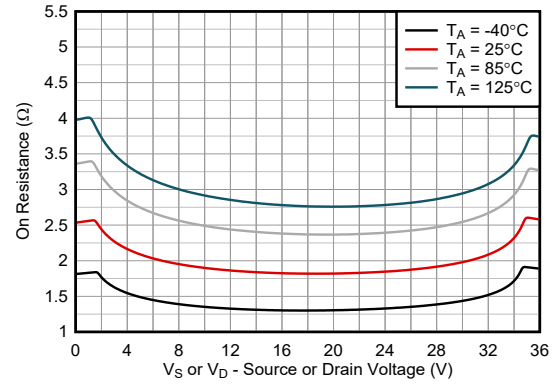


Figure 5-8. On-Resistance vs Temperature

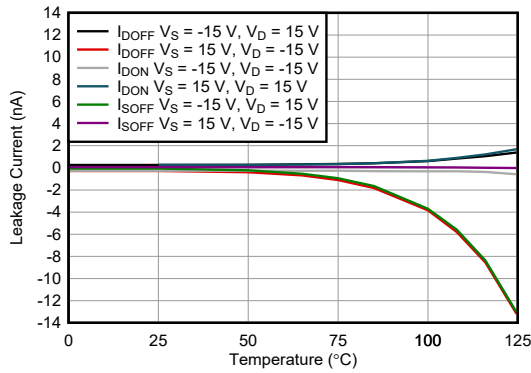


Figure 5-9. Leakage Current vs Temperature

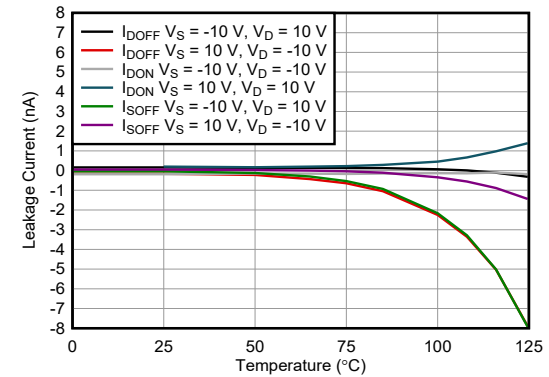


Figure 5-10. Leakage Current vs Temperature

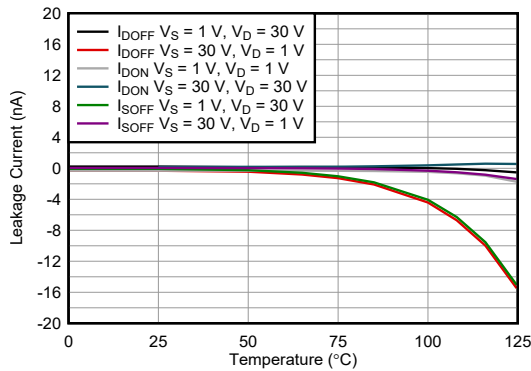


Figure 5-11. Leakage Current vs Temperature

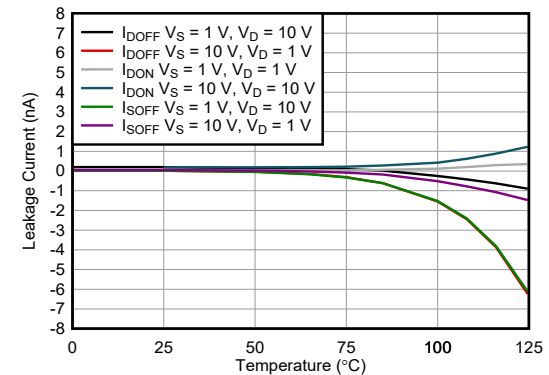
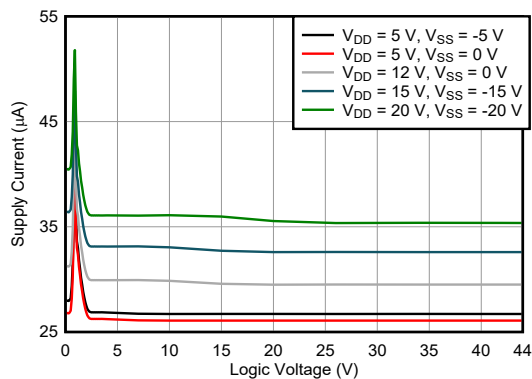


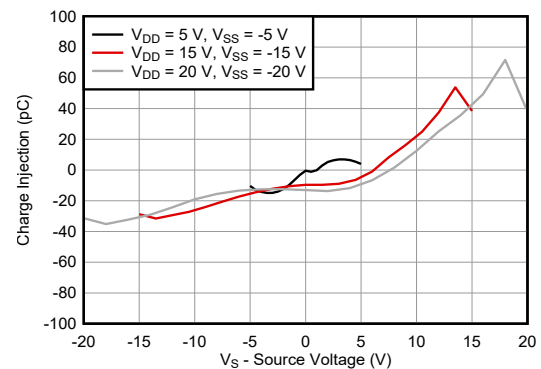
Figure 5-12. Leakage Current vs Temperature

## 5.14 Typical Characteristics (continued)

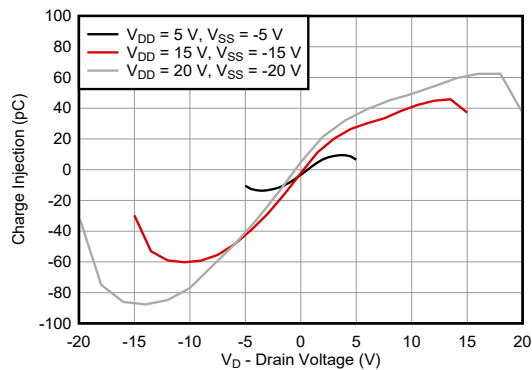
at  $T_A = 25^\circ\text{C}$



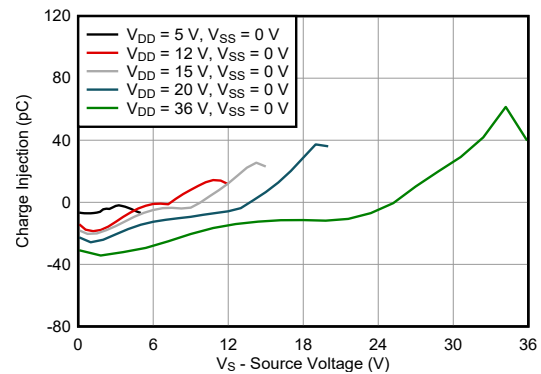
5-13. Supply Current vs Logic Voltage



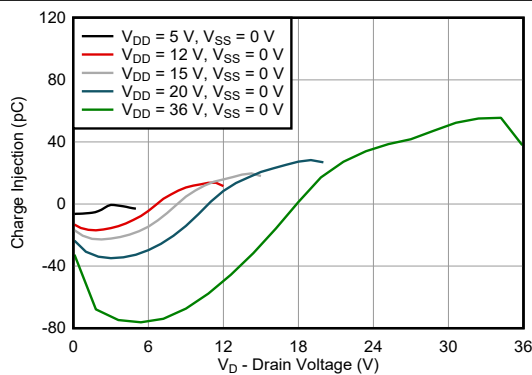
5-14. Charge Injection vs Source Voltage – Dual Supplies



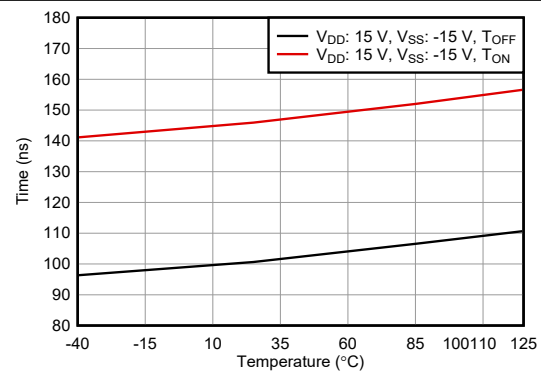
5-15. Charge Injection vs Drain Voltage – Dual Supplies



5-16. Charge Injection vs Source Voltage – Single Supplies



5-17. Charge Injection vs Drain Voltage – Single Supplies



5-18.  $T_{ON}$  and  $T_{OFF}$  vs Temperature



## 5.14 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$

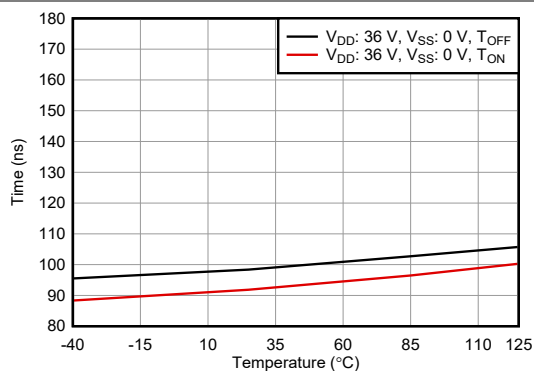


図 5-19.  $T_{ON}$  and  $T_{OFF}$  vs Temperature

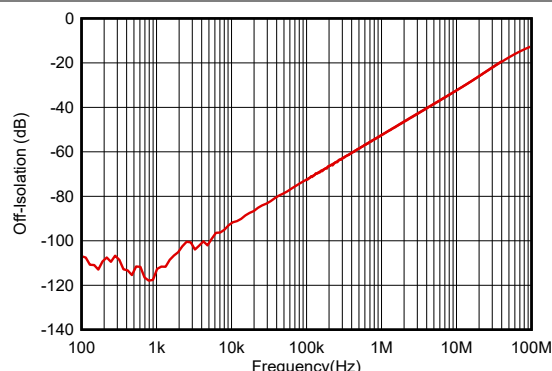


図 5-20. Off-Isolation vs Frequency

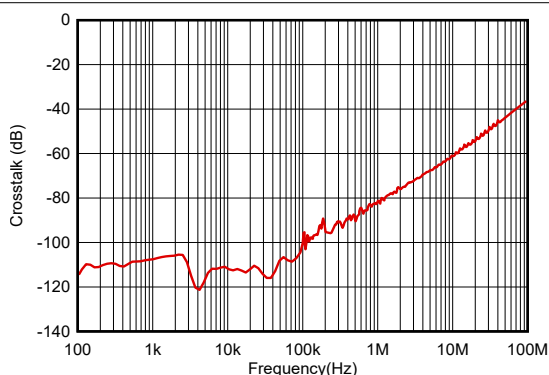


図 5-21. Crosstalk vs Frequency

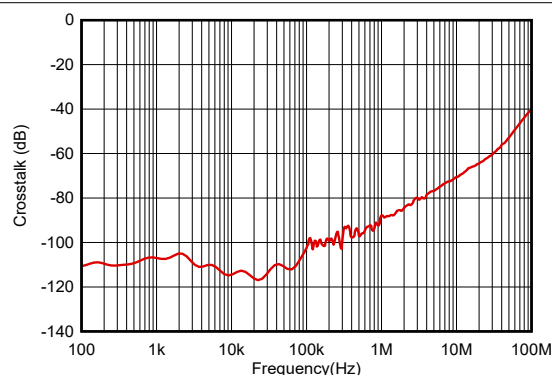


図 5-22. Crosstalk vs Frequency

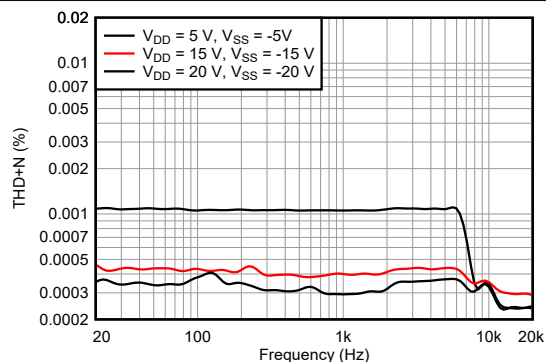


図 5-23. THD+N vs Frequency (Dual Supplies)

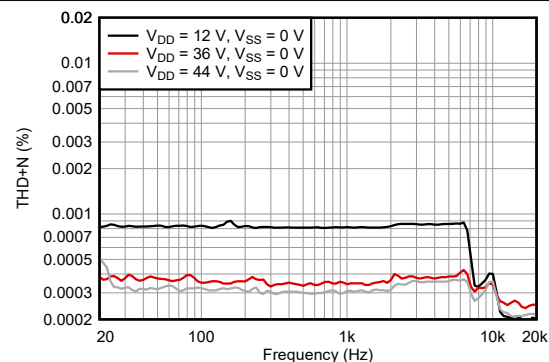
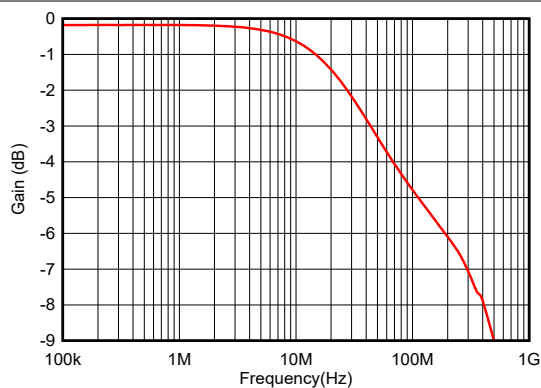


図 5-24. THD+N vs Frequency (Single Supplies)

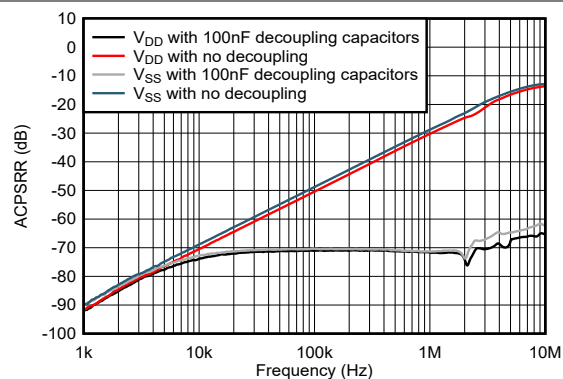
## 5.14 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$



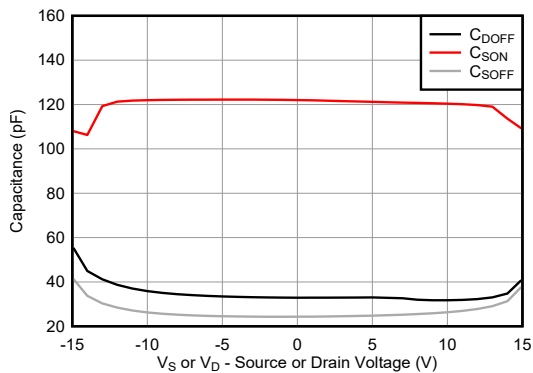
$V_{DD} = 15\text{V}$ ,  $V_{SS} = -15\text{V}$

図 5-25. On Response vs Frequency



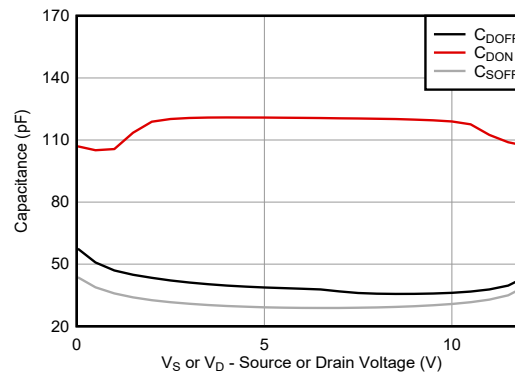
$V_{DD} = +15\text{V}$ ,  $V_{SS} = -15\text{V}$

図 5-26. ACPSRR vs Frequency



$V_{DD} = +15\text{V}$ ,  $V_{SS} = -15\text{V}$

図 5-27. Capacitance vs Source Voltage or Drain Voltage



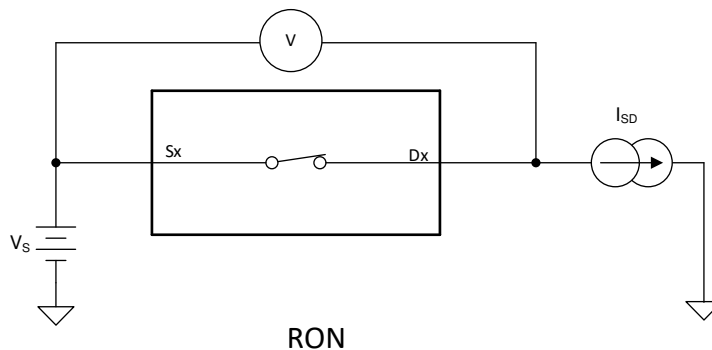
$V_{DD} = 12\text{V}$ ,  $V_{SS} = 0\text{V}$

図 5-28. Capacitance vs Source Voltage or Drain Voltage

## 6 Parameter Measurement Information

### 6.1 On-Resistance

The on-resistance of a device is the ohmic resistance between the source (Sx) and drain (D) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol  $R_{ON}$  is used to denote on-resistance. 6-1 shows the measurement setup used to measure  $R_{ON}$ . Voltage (V) and current ( $I_{SD}$ ) are measured using the following setup, where  $R_{ON}$  is computed as  $R_{ON} = V / I_{SD}$ :



6-1. On-Resistance

### 6.2 Off-Leakage Current

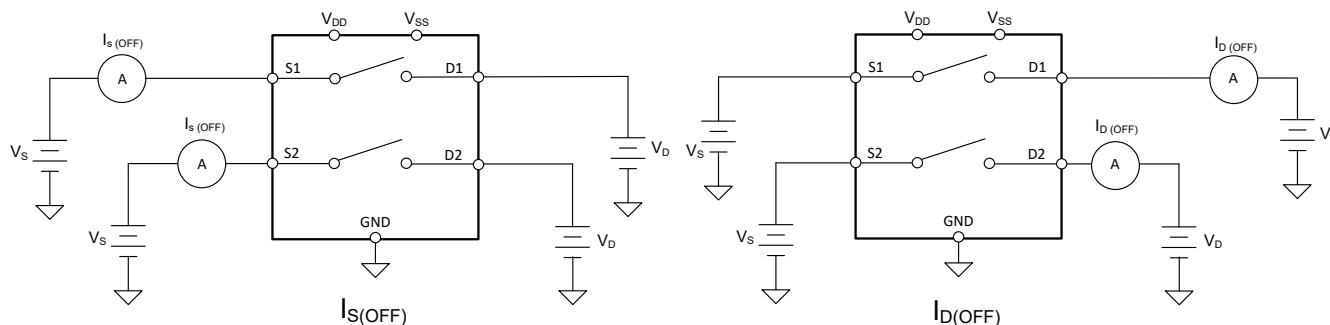
There are two types of leakage currents associated with a switch during the off state:

1. Source off-leakage current.
2. Drain off-leakage current.

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol  $I_{S(OFF)}$ .

Drain leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol  $I_{D(OFF)}$ .

6-2 shows the setup used to measure both off-leakage currents.

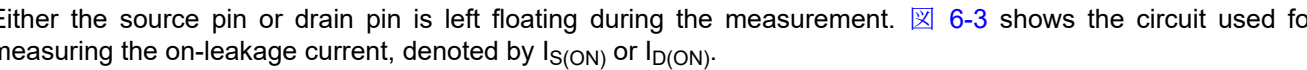


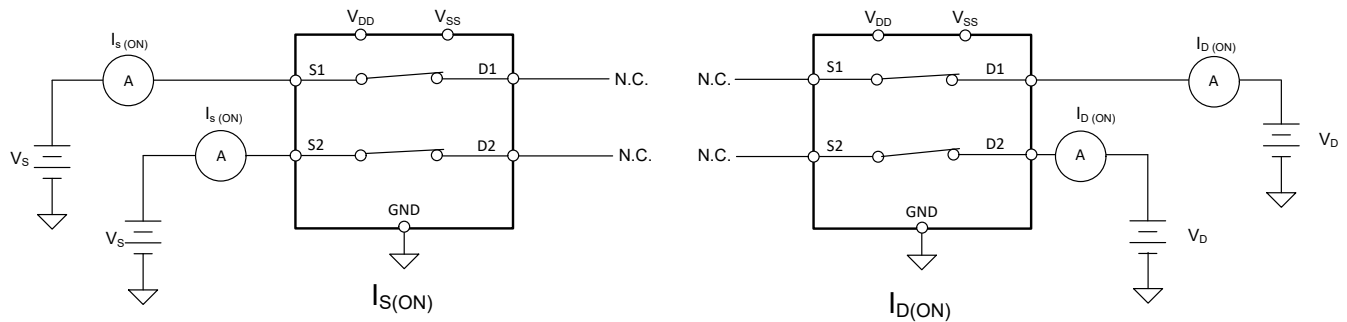
6-2. Off-Leakage Measurement Setup

### 6.3 On-Leakage Current

Source on-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is on. This current is denoted by the symbol  $I_{S(ON)}$ .

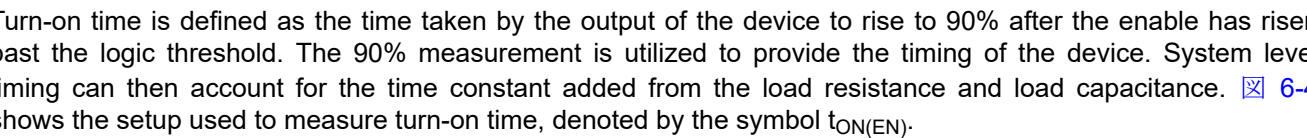
Drain on-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is on. This current is denoted by the symbol  $I_{D(ON)}$ .

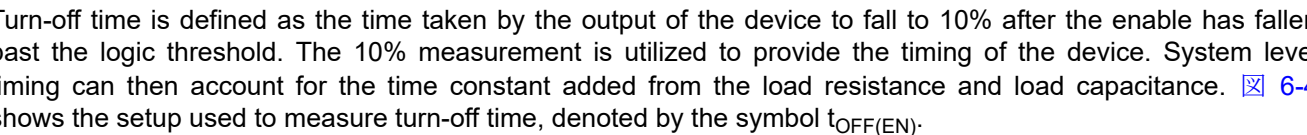
Either the source pin or drain pin is left floating during the measurement.  6-3 shows the circuit used for measuring the on-leakage current, denoted by  $I_{S(ON)}$  or  $I_{D(ON)}$ .

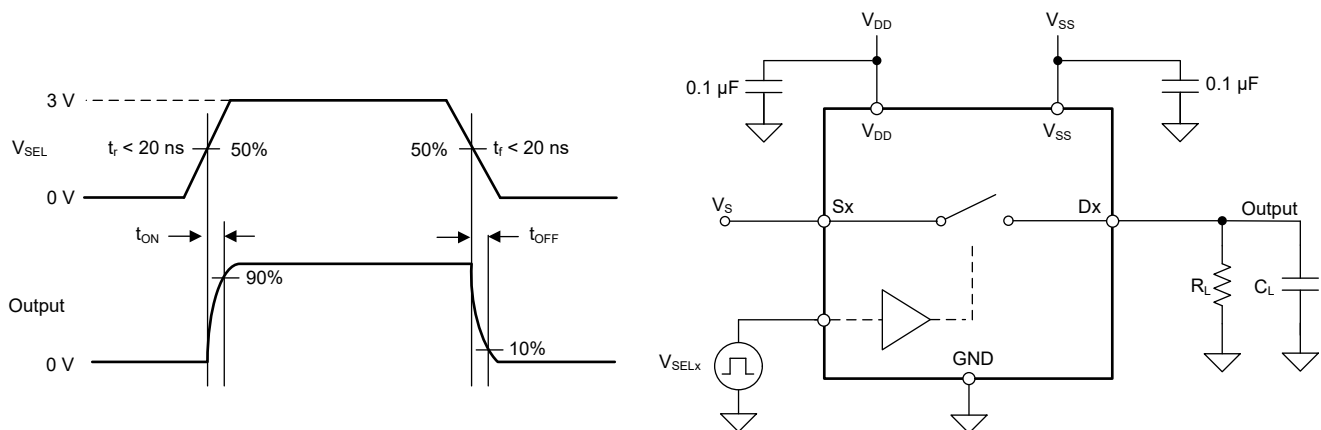


 6-3. On-Leakage Measurement Setup

### 6.4 $t_{ON(EN)}$ and $t_{OFF(EN)}$

Turn-on time is defined as the time taken by the output of the device to rise to 90% after the enable has risen past the logic threshold. The 90% measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance.  6-4 shows the setup used to measure turn-on time, denoted by the symbol  $t_{ON(EN)}$ .

Turn-off time is defined as the time taken by the output of the device to fall to 10% after the enable has fallen past the logic threshold. The 10% measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance.  6-4 shows the setup used to measure turn-off time, denoted by the symbol  $t_{OFF(EN)}$ .



 6-4. Turn-On and Turn-Off Time Measurement Setup

## 6.5 $t_{ON}(V_{DD})$ Time

The  $t_{ON}(V_{DD})$  time is defined as the time taken by the output of the device to rise to 90% after the supply has risen past the supply threshold. The 90% measurement is used to provide the timing of the device turning on in the system. 図 6-5 shows the setup used to measure turn on time, denoted by the symbol  $t_{ON}(V_{DD})$ .

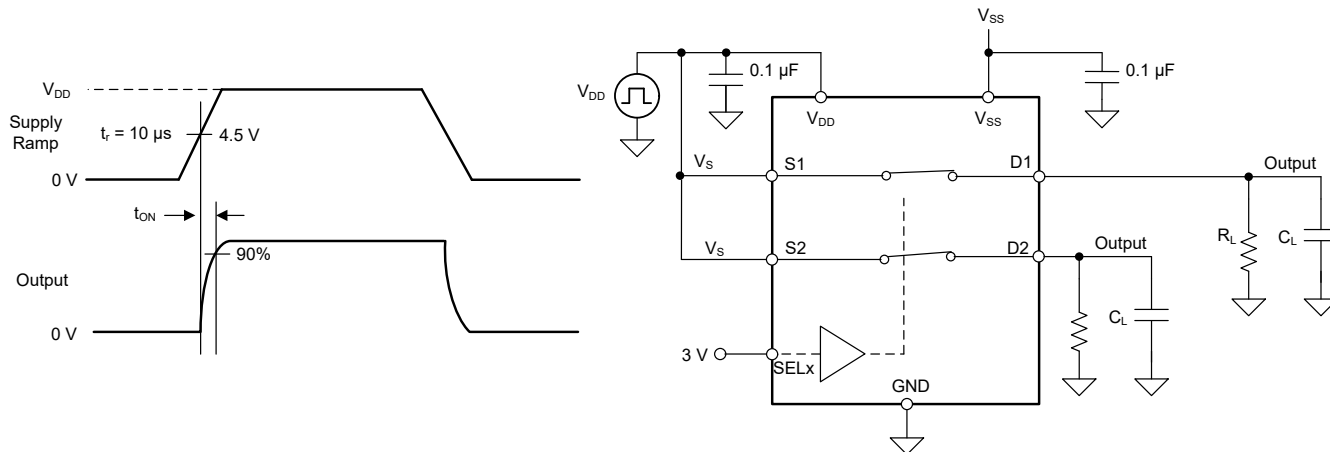


図 6-5.  $t_{ON}(V_{DD})$  Time Measurement Setup

## 6.6 Propagation Delay

Propagation delay is defined as the time taken by the output of the device to rise or fall 50% after the input signal has risen or fallen past the 50% threshold. 図 6-6 shows the setup used to measure propagation delay, denoted by the symbol  $t_{PD}$ .

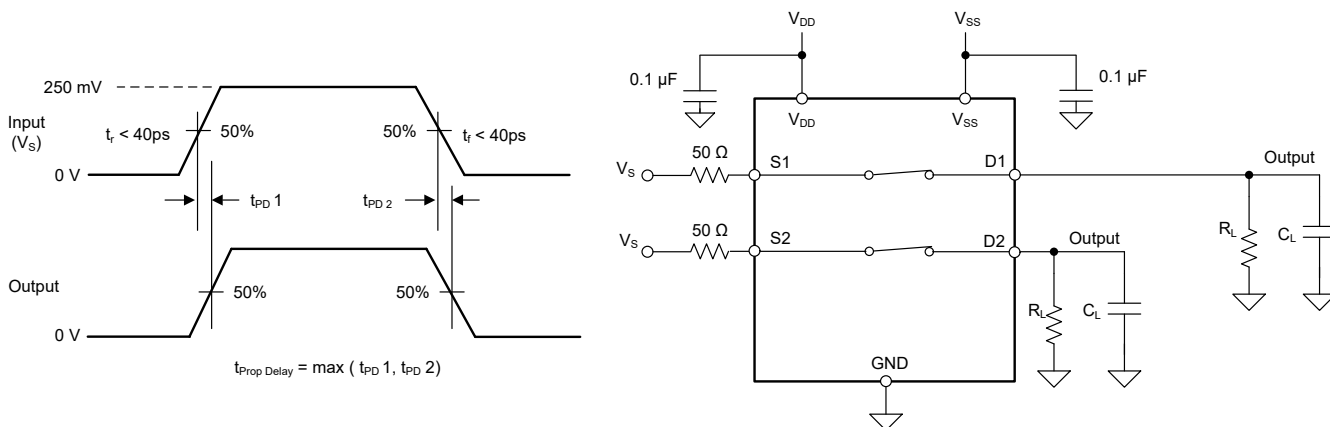
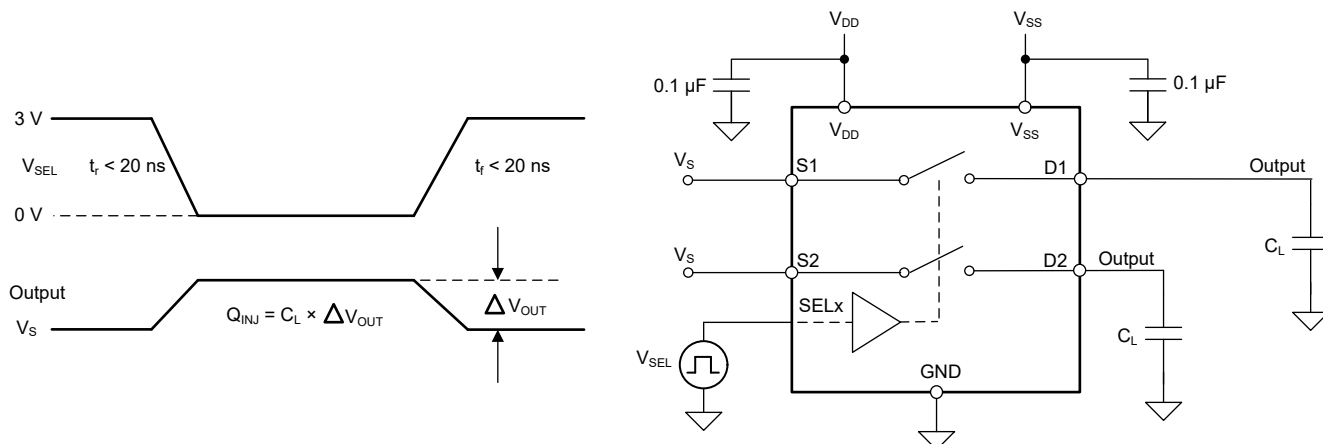


図 6-6. Propagation Delay Measurement Setup

## 6.7 Charge Injection

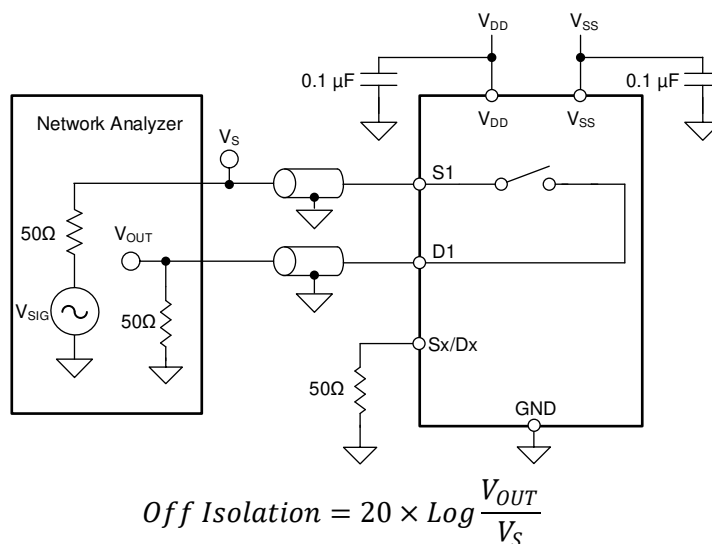
The TMUX722x has a transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol  $Q_C$ . [Figure 6-7](#) shows the setup used to measure charge injection from source (Sx) to drain (D).



**Figure 6-7. Charge-Injection Measurement Setup**

## 6.8 Off Isolation

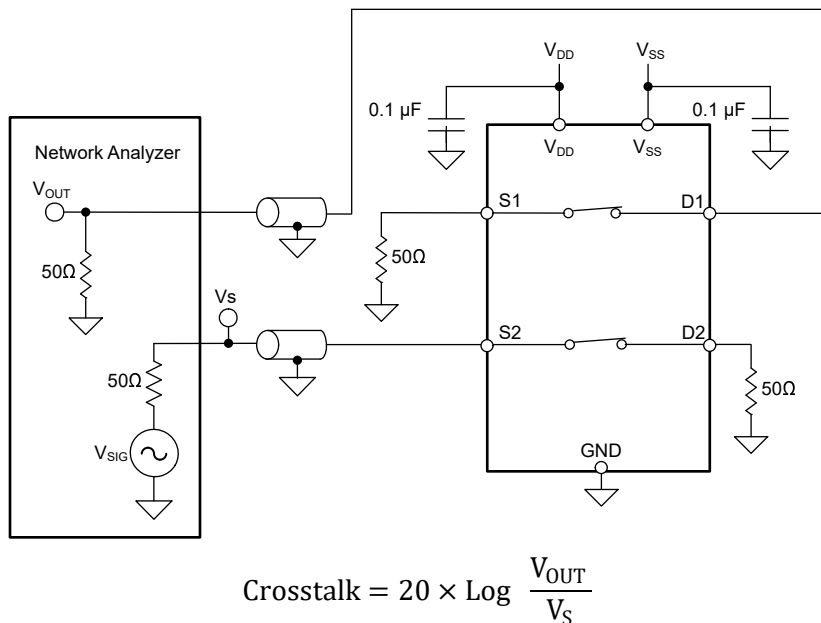
Off isolation is defined as the ratio of the signal at the drain pin (Dx) of the device when a signal is applied to the source pin (Sx) of an off-channel. The characteristic impedance,  $Z_0$ , for the measurement is 50 Ω. [Figure 6-8](#) shows the setup used to measure off isolation. Use off isolation equation to compute off isolation.



**Figure 6-8. Off Isolation Measurement Setup**

## 6.9 Crosstalk

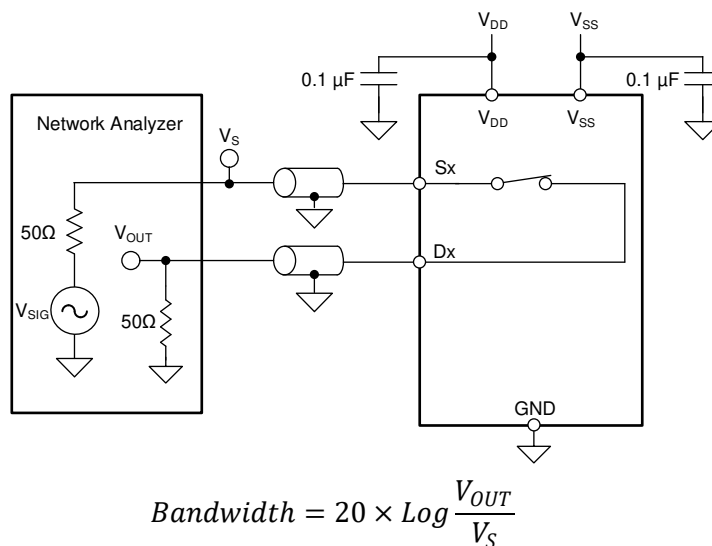
Crosstalk is defined as the ratio of the signal at the drain pin (D) of a different channel, when a signal is applied at the source pin (Sx) of an on-channel. [Figure 6-9](#) shows the setup used to measure, and the equation used to calculate crosstalk.



**Figure 6-9. Crosstalk Measurement Setup**

## 6.10 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (Dx) of the device. The characteristic impedance,  $Z_0$ , for the measurement is 50 Ω. [Figure 6-10](#) shows the setup used to measure bandwidth.



**Figure 6-10. Bandwidth Measurement Setup**

## 6.11 THD + Noise

The total harmonic distortion (THD) of a signal is a measurement of the harmonic distortion, and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency at the mux output. The on-resistance of the device varies with the amplitude of the input signal and results in distortion when the drain pin is connected to a low-impedance load. Total harmonic distortion plus noise is denoted as THD + N.

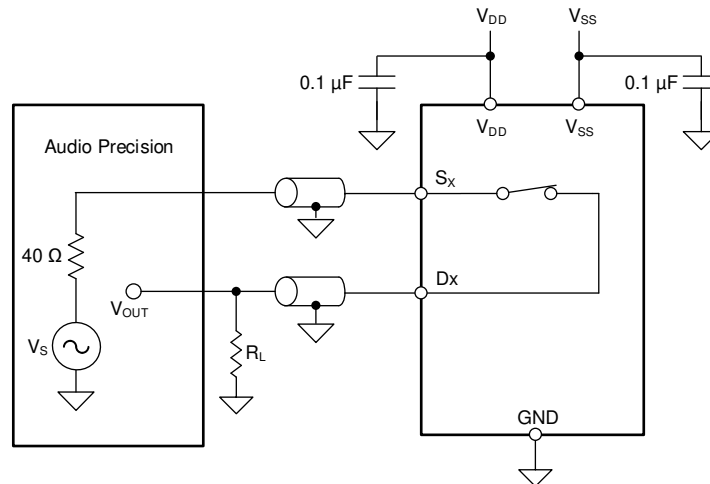


Figure 6-11. THD + N Measurement Setup

## 6.12 Power Supply Rejection Ratio (PSRR)

PSRR measures the ability of a device to prevent noise and spurious signals that appear on the supply voltage pin from coupling to the output of the switch. The DC voltage on the device supply is modulated by a sine wave of 100 mV<sub>PP</sub>. The ratio of the amplitude of signal on the output to the amplitude of the modulated signal is the AC PSRR.

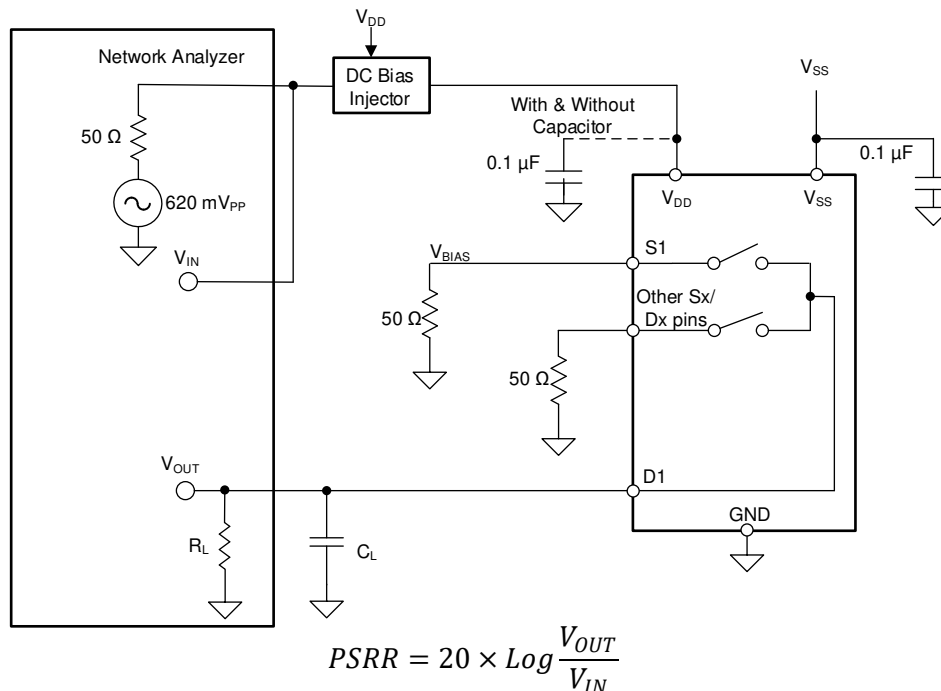


Figure 6-12. AC PSRR Measurement Setup



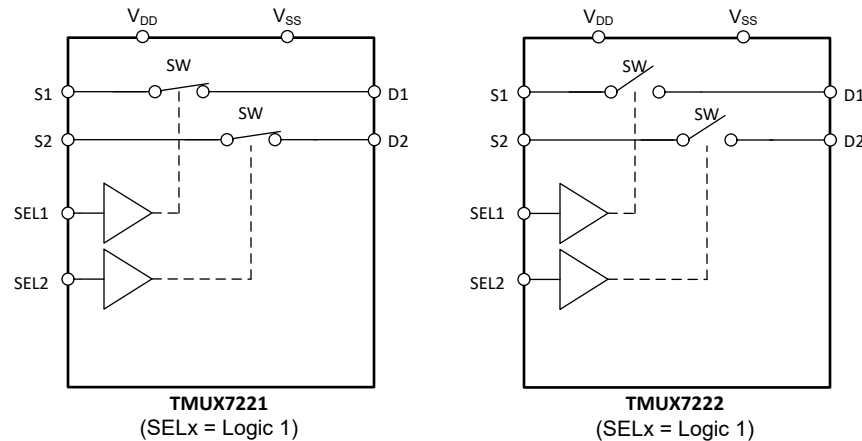
## 7 Detailed Description

### 7.1 Overview

The TMUX722x is a 1:1, 2-channel switch. Each input is turned on or turned off based on the state of the select line and enable pin.

### 7.2 Functional Block Diagram

Figure 7-1 shows the functional block diagram of the TMUX722x.



**Figure 7-1. TMUX722x Functional Block Diagram**

### 7.3 Feature Description

#### 7.3.1 Bidirectional Operation

The TMUX722x conducts equally well from source (Sx) to drain (D) or from drain (D) to source (Sx). Each channel has very similar characteristics in both directions and supports both analog and digital signals.

#### 7.3.2 Rail-to-Rail Operation

The valid signal path input and output voltage for TMUX722x ranges from  $V_{SS}$  to  $V_{DD}$ .

#### 7.3.3 1.8 V Logic Compatible Inputs

The TMUX722x has 1.8 V logic compatible control for all logic control inputs. 1.8 V logic level inputs allows the device to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and BOM cost. For more information on 1.8 V logic implementations, refer to [Simplifying Design with 1.8 V logic Muxes and Switches](#).

#### 7.3.4 Integrated Pull-Down Resistor on Logic Pins

The TMUX722x have internal weak pull-down resistors to GND so that the logic pins are not left floating. The value of this pull-down resistor is approximately 4 MΩ, but is clamped to about 1 μA at higher voltages. This feature integrates up to four external components and reduces system size and cost.

#### 7.3.5 Fail-Safe Logic

The TMUX722x supports Fail-Safe Logic on the control input pins (EN, SEL) allowing for operation up to 44 V above ground, regardless of the state of the supply pins. This feature allows voltages on the control pins to be applied before the supply pin, protecting the device from potential damage. Fail-Safe Logic minimizes system complexity by removing the need for power supply sequencing on the logic control pins. For example, the Fail-Safe Logic feature allows the logic input pins of the TMUX722x to be ramped to +44 V while  $V_{DD}$  and  $V_{SS}$  = 0 V. The logic control inputs are protected against positive faults of up to +44 V in powered-off condition, but do not offer protection against negative overvoltage conditions.

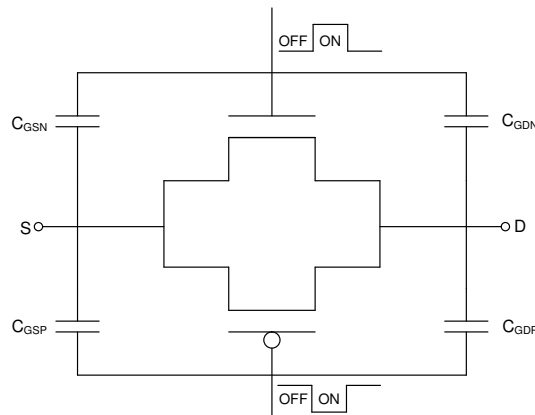
### 7.3.6 Latch-Up Immune

Latch-Up is a condition where a low impedance path is created between a supply pin and ground. This condition is caused by a trigger (current injection or overvoltage), but once activated, the low impedance path remains even after the trigger is no longer present. This low impedance path may cause system upset or catastrophic damage due to excessive current levels. The Latch-Up condition typically requires a power cycle to eliminate the low impedance path.

The TMUX722x family of devices are constructed on Silicon on Insulator (SOI) based process where an oxide layer is added between the PMOS and NMOS transistor of each CMOS switch to prevent parasitic structures from forming. The oxide layer is also known as an insulating trench and prevents triggering of latch up events due to overvoltage or current injections. The latch-up immunity feature allows the TMUX722x family of switches and multiplexers to be used in harsh environments.

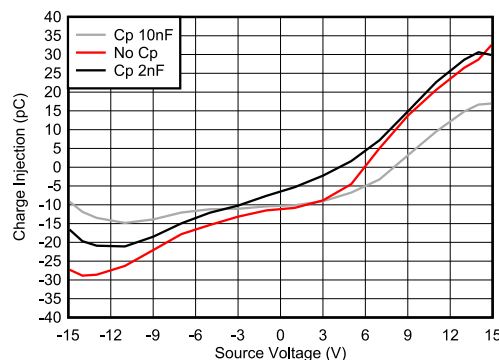
### 7.3.7 Ultra-Low Charge Injection

The TMUX722x has a transmission gate topology, as shown in [Figure 7-2](#). Any mismatch in the stray capacitance associated with the NMOS and PMOS causes an output level change whenever the switch is opened or closed.



**Figure 7-2. Transmission Gate Topology**

The TMUX722x contains specialized architecture to reduce charge injection on the Drain (Dx). To further reduce charge injection in a sensitive application, a compensation capacitor ( $C_p$ ) can be added on the Source (Sx). Doing this will push excess charge from the switch transition into the compensation capacitor on the Source (Sx) instead of the Drain (Dx). As a general rule,  $C_p$  should be 20x larger than the equivalent load capacitance on the Drain (Dx). [Figure 7-3](#) shows charge injection variation with different compensation capacitors on the Source side. This plot was captured on the TMUX7219 as part of the TMUX72xx family with a 100 pF load capacitance.



**Figure 7-3. Charge Injection Compensation**

## 7.4 Device Functional Modes

The TMUX722x devices have two independently selectable single-pole, single-throw switches that are turned-on or turned-off based on the state of the corresponding select pin. The control pins can be as high as 44 V.

The TMUX722x devices can be operated without any external components except for the supply decoupling capacitors. The SEL pins has internal pull-down resistor of 4 MΩ. If unused, tie the SEL pins to GND so that the device does not consume additional current as highlighted in [Implications of Slow or Floating CMOS Inputs](#). Connect unused signal path inputs (S1, S2, D1, or D2) to GND.

## 7.5 Truth Tables

表 7-1 provides the truth tables for the TMUX722x.

**表 7-1. TMUX7221 Truth Table**

SEL x	CHANNEL x
0	Channel x OFF
1	Channel x ON

**表 7-2. TMUX7222 Truth Table**

SEL x	CHANNEL x
0	Channel x ON
1	Channel x OFF

## 8 Application and Implementation

### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

TMUX722x is part of the precision switches and multiplexers family of devices. TMUX722x offers low  $R_{ON}$ , low on and off leakage currents and ultra-low charge injection performance. These properties make TMUX722x ideal for implementing high precision industrial systems requiring selection of one of two inputs or outputs.

### 8.2 Typical Applications

#### 8.2.1 Switched Gain Amplifier - Discrete PGA

Switches and multiplexers are commonly used in the feedback path of amplifier circuits to provide configurable gain control. By using various resistor values on each switch path the TMUX722x allows the system to have multiple gain settings. An external resistor, ensures the amplifier isn't operating in an open loop configuration, and gives up to 4 gain settings. The leakage current, on-resistance, and charge injection performance of the TMUX722x are key specifications to evaluate when selecting a device for gain control.

Figure 8-1 shows the TMUX722x configured to select the gain of an op-amp, creating a discrete PGA.

For more information on how to use TI's analog switches in Discrete Programmable Gain Amplifier (PGA) such as the impact of On-Capacitance, see [Choosing the Right Multiplexer for a Discrete Programmable Gain Amplifier \(PGA\)](#)

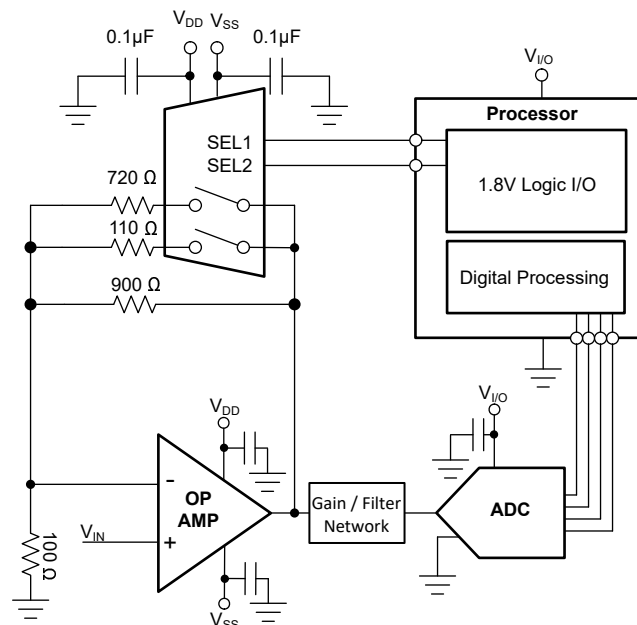


図 8-1. Gain Switching

### 8.2.1.1 Design Requirements

For this design example, use the parameters listed in [セクション 8.2.1.1](#).

**表 8-1. Design Parameters**

PARAMETERS	VALUES
Supply ( $V_{DD}$ )	15 V
Supply ( $V_{SS}$ )	-15 V
Input / Output signal range	-15 V to 15 V (Rail-to-Rail)
Control logic thresholds	1.8 V compatible

### 8.2.1.2 Detailed Design Procedure

The TMUX722x device can be operated without any external components except for the supply decoupling capacitors. All inputs signals passing through the switch must fall within the recommend operating conditions of the TMUX722x including signal range and continuous current. For this design example, with a supply of +15 V and -15 V, the signals can range from +15 V to -15 V when the device is powered.

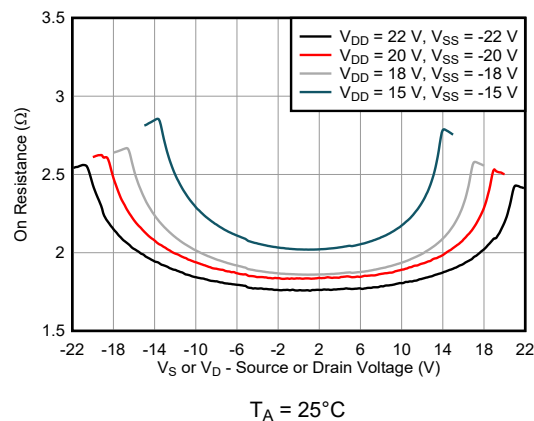
The application shown in [Switching Gain Settings](#) demonstrates how to use the TMUX722x to control the feedback gain of a precision op-amp. This feedback design can very sensitive to induced voltage and current offsets. The TMUX722x has a typical On-leakage current of 100 pA which would lead to an accuracy well within 1% of a full scale 1  $\mu$ A signal, thus minimizing errors from current offsets. The low On-Resistance of the TMUX722x leads to a low error in the feedback resistance and resulting gain, and also minimizes any voltage offsets.

**表 8-2. Programmable Gain and Error**

SEL1	SEL2	Gain	Gain Error
0	0	10x	0%
1	0	5x	0.13%
0	1	2x	0.16%

### 8.2.1.3 Application Curve

The TMUX722x is capable of switching signals with minimal distortion because of the ultra-low leakage currents and excellent on-resistance flatness. [図 8-2](#) shows how the on-resistance for the TMUX722x varies with different supply voltages.



**図 8-2. On-Resistance vs Source or Drain Voltage**

### 8.3 Power Supply Recommendations

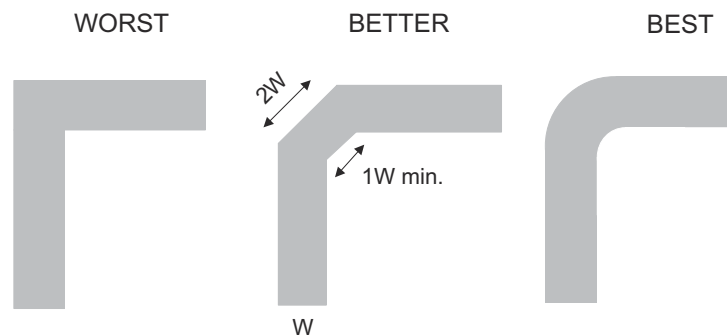
The TMUX722x operates across a wide supply range of  $\pm 4.5\text{ V}$  to  $\pm 22\text{ V}$  (4.5 V to 44 V in single-supply mode). The device also performs well with asymmetrical supplies such as  $V_{DD} = 12\text{ V}$  and  $V_{SS} = -5\text{ V}$ .

Power-supply bypassing improves noise margin and prevents switching noise propagation from the supply rails to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1  $\mu\text{F}$  to 10  $\mu\text{F}$  at both the  $V_{DD}$  and  $V_{SS}$  pins to ground. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground and power planes. Always ensure the ground (GND) connection is established before supplies are ramped.

## 8.4 Layout

### 8.4.1 Layout Guidelines

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. [Figure 8-3](#) shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.



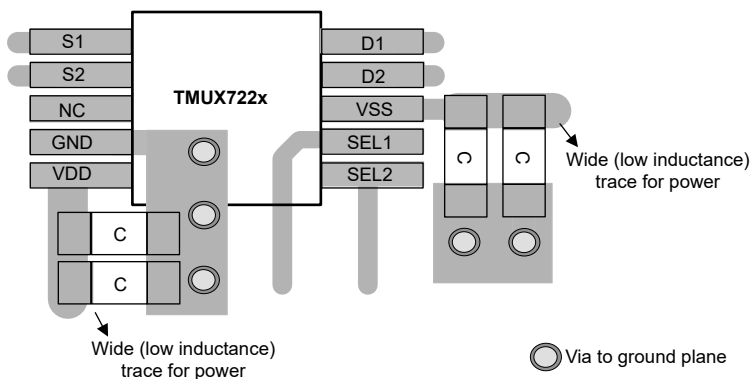
**Figure 8-3. Trace Example**

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

Some key considerations are:

- For reliable operation, connect a decoupling capacitor ranging from 0.1  $\mu\text{F}$  to 10  $\mu\text{F}$  between  $V_{DD}/V_{SS}$  and GND. We recommend a 0.1  $\mu\text{F}$  and 1  $\mu\text{F}$  capacitor, placing the lowest value capacitor as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the supply voltage.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.
- Using multiple vias in parallel will lower the overall inductance and is beneficial for connection to ground planes.

### 8.4.2 Layout Example



**8-4. TMUX722x Layout Example**

## 9 Device and Documentation Support

### 9.1 Documentation Support

#### 9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Improve Stability Issues with Low CON Multiplexers](#).
- Texas Instruments, [Improving Signal Measurement Accuracy in Automated Test Equipment](#).
- Texas Instruments, [Multiplexers and Signal Switches Glossary](#).
- Texas Instruments, [QFN/SON PCB Attachment](#).
- Texas Instruments, [Quad Flat pack No-Lead Logic Packages](#).
- Texas Instruments, [Simplifying Design with 1.8 V logic Muxes and Switches](#).
- Texas Instruments, [System-Level Protection for High-Voltage Analog Multiplexers](#).
- Texas Instruments, [True Differential, 4 x 2 MUX, Analog Front End, Simultaneous-Sampling ADC Circuit](#).

### 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの[使用条件](#)を参照してください。

### 9.4 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

### 9.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

### 9.6 用語集

#### テキサス・インスツルメンツ用語集

この用語集には、用語や略語の一覧および定義が記載されています。

## 10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

### Changes from Revision A (April 2023) to Revision B (May 2024)

Page

- Updated the *Pin Configuration* section to accurately reflect the correct pin number for SEL1 and SEL2.....3



**Changes from Revision \* (February 2023) to Revision A (April 2023)**
**Page**

- データシートのステータスを以下のように変更:「事前情報」から「量産データ」へ変更 ..... **1**

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## 重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、[テキサス・インスツルメンツの販売条件](#)、または [ti.com](https://www.ti.com) やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用されるテキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2024, Texas Instruments Incorporated

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TMUX7221DGSR</a>	Active	Production	VSSOP (DGS)   10	2500   LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	TM221
TMUX7221DGSR.B	Active	Production	VSSOP (DGS)   10	2500   LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	TM221
<a href="#">TMUX7222DGSR</a>	Active	Production	VSSOP (DGS)   10	2500   LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	TM222
TMUX7222DGSR.B	Active	Production	VSSOP (DGS)   10	2500   LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	TM222

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

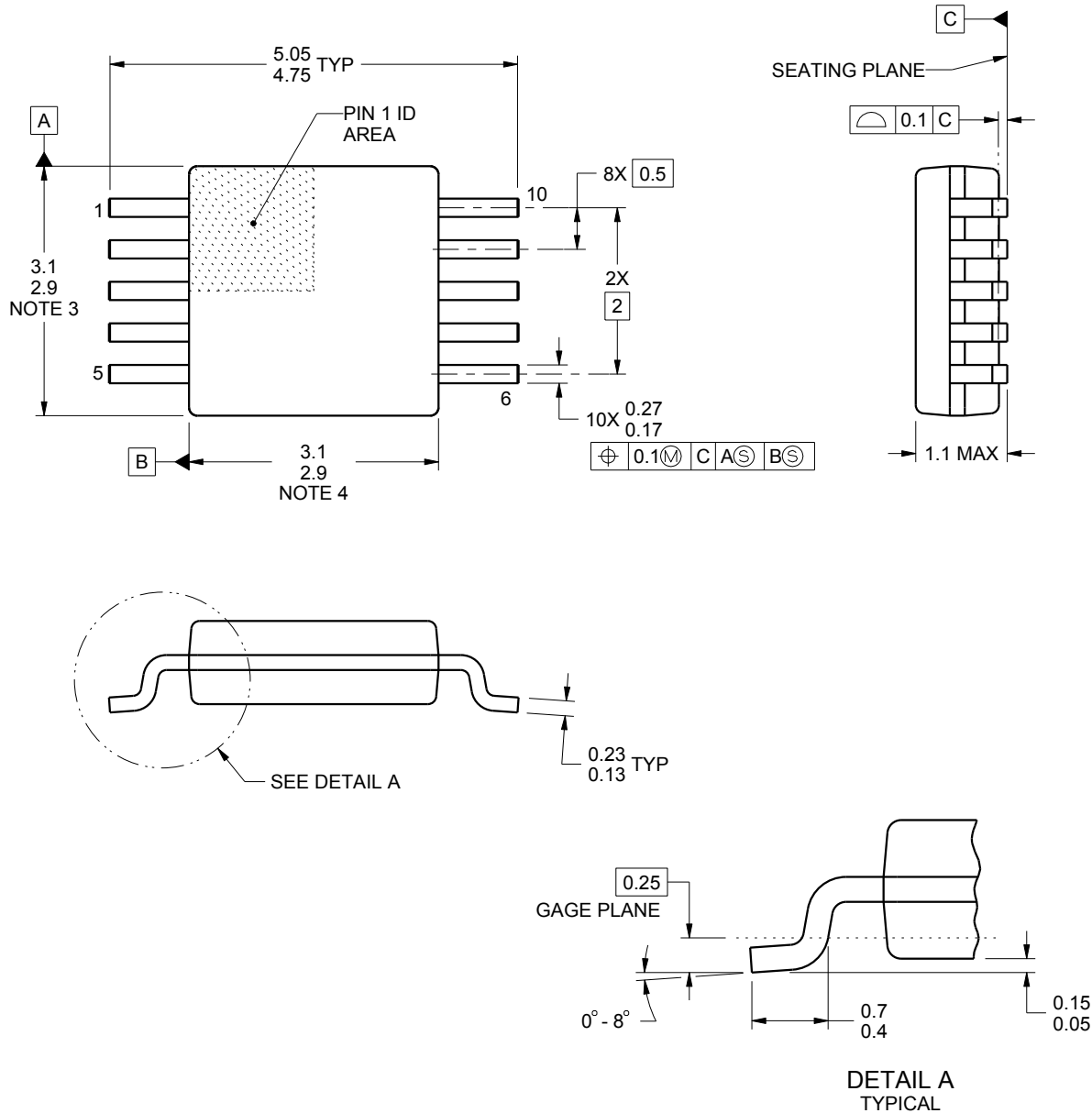
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUX7221DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
TMUX7222DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUX7221DGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
TMUX7222DGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0



4221984/A 05/2015

**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.

# EXAMPLE BOARD LAYOUT

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



## 重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとしします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、[TI の総合的な品質ガイドライン](#)、[ti.com](https://www.ti.com) または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

Copyright © 2025, Texas Instruments Incorporated

最終更新日：2025 年 10 月