

TMUX7219-Q1 1.8V ロジック対応、44V、ラッチアップフリー、2 : 1 (SPDT) 高精度スイッチ

1 特長

- 車載アプリケーション向けに AEC-Q100 認証済み
 - デバイス温度グレード 1: -40°C ~ 125°C の動作時周囲温度
- 機能安全対応
 - 機能安全システムの設計に役立つ資料を利用可能
- ラッチアップフリー
- 両電源電圧範囲: $\pm 4.5\text{V}$ ~ $\pm 22\text{V}$
- 単電源電圧範囲: 4.5V ~ 44V
- 低いオン抵抗: $2.1\ \Omega$
- 少ない電荷注入: -10pC
- 大電流のサポート: 330mA (最大値)
- 1.8V ロジック互換
- フェイルセーフ ロジック
- レール ツー レール動作
- 双方向の信号パス
- ブレイク ビフォー メイクのスイッチング動作

2 アプリケーション

- EV 充電ステーション向け電源モジュール
- 先進運転支援システム (ADAS)
- 車載ゲートウェイ
- アナログおよびデジタルの多重化 / 多重分離
- 車載ヘッド・ユニット
- テレマティクス制御ユニット
- 緊急通話 (eCall)
- インフォテインメント
- 車体制御モジュール (BCM)
- ボディ・エレクトロニクス / 照明
- バッテリー管理システム (BMS)
- HVAC コントローラ・モジュール
- ADAS ドメイン・コントローラ

3 概要

TMUX7219-Q1 は、シングル チャネル、2:1 (SPDT) 構成、ラッチアップ フリーの CMOS スイッチです。このデバイスは、シングル電源 (4.5V ~ 44V)、デュアル電源 ($\pm 4.5\text{V}$ ~ $\pm 22\text{V}$)、または非対称電源 ($V_{\text{DD}} = 12\text{V}$ 、 $V_{\text{SS}} = -5\text{V}$ など) で動作します。TMUX7219-Q1 は、ソース (S_x) およびドレイン (D) ピンで、 V_{SS} から V_{DD} までの範囲の双方向アナログおよびデジタル信号をサポートします。

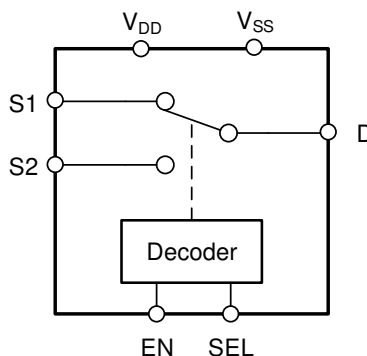
TMUX7219-Q1 は、EN ピンの制御によりイネーブルまたはディスエーブルにできます。ディスエーブルのときは、両方の信号経路のスイッチがオフになります。イネーブルのとき、SEL ピンを使用して信号経路 1 (S_1 から D へ) または信号経路 2 (S_2 から D へ) をオンにできます。すべてのロジック制御入力は、 1.8V ~ V_{DD} のロジックレベルをサポートしており、有効な電源電圧範囲で動作している場合、TTL ロジックと CMOS ロジックの両方の互換性を確保できます。フェイルセーフ ロジック回路により、電源ピンよりも先に制御ピンに電圧が印加されるため、デバイスへの損傷の可能性が避けられます。

TMUX72xx ファミリーはラッチアップ フリーであるため、一般的に過電圧イベントによって発生するデバイス内の寄生構造間の好ましくない大電流イベントを防止できます。ラッチアップ状態は通常、電源レールがオフにされるまで継続するため、デバイスの障害の原因となる場合があります。このラッチアップ フリーという特長により、TMUX72xx スイッチおよびマルチプレクサ ファミリーは過酷な環境でも使用できます。

パッケージ情報

部品番号	パッケージ ⁽¹⁾	本体サイズ (公称)
TMUX7219-Q1	VSSOP (8) DGK	3.00mm × 3.00mm

(1) 利用可能なパッケージについては、データシートの末尾にあるパッケージ オプションについての付録を参照してください。



機能ブロック図



Table of Contents

1 特長	1	6.9 Charge Injection.....	24
2 アプリケーション	1	6.10 Off Isolation.....	24
3 概要	1	6.11 Crosstalk.....	25
4 Pin Configuration and Functions	3	6.12 Bandwidth.....	25
5 Specifications	4	6.13 THD + Noise.....	26
5.1 Absolute Maximum Ratings.....	4	6.14 Power Supply Rejection Ratio (PSRR).....	26
5.2 ESD Ratings.....	4	7 Detailed Description	27
5.3 Thermal Information.....	4	7.1 Overview.....	27
5.4 Recommended Operating Conditions.....	5	7.2 Functional Block Diagram.....	27
5.5 Source or Drain Continuous Current.....	5	7.3 Feature Description.....	27
5.6 ± 15 V Dual Supply: Electrical Characteristics	6	7.4 Device Functional Modes.....	30
5.7 ± 15 V Dual Supply: Switching Characteristics	7	7.5 Truth Tables.....	30
5.8 ± 20 V Dual Supply: Electrical Characteristics.....	8	8 Application and Implementation	31
5.9 ± 20 V Dual Supply: Switching Characteristics.....	9	8.1 Application Information.....	31
5.10 44 V Single Supply: Electrical Characteristics	10	8.2 Typical Applications.....	31
5.11 44 V Single Supply: Switching Characteristics	11	8.3 Power Supply Recommendations.....	32
5.12 12 V Single Supply: Electrical Characteristics	12	8.4 Layout.....	32
5.13 12 V Single Supply: Switching Characteristics	13	9 Device and Documentation Support	34
5.14 Typical Characteristics.....	14	9.1 Documentation Support.....	34
6 Parameter Measurement Information	20	9.2 Receiving Notification of Documentation Updates....	34
6.1 On-Resistance.....	20	9.3 サポート・リソース.....	34
6.2 Off-Leakage Current.....	20	9.4 Trademarks.....	34
6.3 On-Leakage Current.....	21	9.5 静電気放電に関する注意事項.....	34
6.4 Transition Time.....	21	9.6 用語集.....	34
6.5 $t_{ON(EN)}$ and $t_{OFF(EN)}$	22	10 Revision History	34
6.6 Break-Before-Make.....	22	11 Mechanical, Packaging, and Orderable Information	35
6.7 $t_{ON(VDD)}$ Time.....	23		
6.8 Propagation Delay.....	23		

4 Pin Configuration and Functions

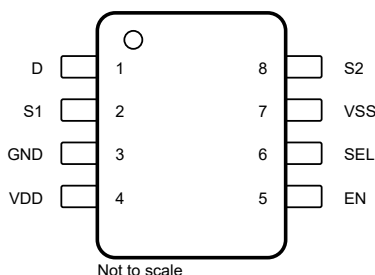


図 4-1. DGK Package, 8-Pin VSSOP (Top View)

表 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION ⁽²⁾
NAME	DGK		
D	1	I/O	Drain pin. Can be an input or output.
S1	2	I/O	Source pin 1. Can be an input or output.
GND	3	P	Ground (0 V) reference
V _{DD}	4	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 μ F to 10 μ F between V _{DD} and GND.
EN	5	I	Active high logic enable, has internal pull-up resistor. When this pin is low, all switches are turned off. When this pin is high, the SEL logic input determine which switch is turned on.
SEL	6	I	Logic control input, has internal pull-down resistor. Controls the switch connection as shown in セクション 7.5 .
V _{SS}	7	P	Negative power supply. This pin is the most negative power-supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 0.1 μ F to 10 μ F between V _{SS} and GND.
S2	8	I/O	Source pin 2. Can be an input or output.
Thermal Pad	—	—	The thermal pad is not connected internally. There is no requirement to electrically connect this pad. If connected, it is recommended that the pad be left floating or tied to GND.

(1) I = input, O = output, I/O = input and output, P = power.

(2) Refer to [セクション 7.4](#) for what to do with unused pins.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾ ⁽²⁾

		MIN	MAX	UNIT
$V_{DD} - V_{SS}$	Supply voltage		48	V
V_{DD}		–0.5	48	V
V_{SS}		–48	0.5	V
V_{SEL} or V_{EN}	Logic control input pin voltage (SEL, EN) ⁽³⁾	–0.5	48	V
I_{SEL} or I_{EN}	Logic control input pin current (SEL, EN) ⁽³⁾	–30	30	mA
V_S or V_D	Source or drain voltage (Sx, D) ⁽³⁾	$V_{SS}-0.5$	$V_{DD}+0.5$	V
I_{IK}	Diode clamp current ⁽³⁾	–30	30	mA
I_S or I_D (CONT)	Source or drain continuous current (Sx, D)		$I_{DC} + 10\%$ ⁽⁴⁾	mA
T_A	Ambient temperature	–55	150	°C
T_{stg}	Storage temperature	–65	150	°C
T_J	Junction temperature		150	°C
P_{tot}	Total power dissipation (DGK Package) ⁽⁵⁾		460	mW

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltages are with respect to ground, unless otherwise specified.
- (3) Pins are diode-clamped to the power-supply rails. Over voltage signals must be voltage and current limited to maximum ratings.
- (4) Refer to *Source or Drain Continuous Current* table for I_{DC} specifications.
- (5) For DGK package: P_{tot} derates linearly above $T_A = 70^\circ\text{C}$ by 6.7mW/°C.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins ⁽¹⁾	±2000	V
		Charged device model (CDM), ANSI/ESDA/ JEDEC JS-002, all pins ⁽²⁾	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Thermal Information

THERMAL METRIC ⁽¹⁾		TMUX7219	UNIT
		DGK (VSSOP)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	152.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	48.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	73.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	71.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{DD} - V_{SS}$ ⁽¹⁾	Power supply voltage differential	4.5		44	V
V_{DD}	Positive power supply voltage	4.5		44	V
V_S or V_D	Signal path input/output voltage (source or drain pin) (Sx, D)	V_{SS}		V_{DD}	V
V_{SEL} or V_{EN}	Address or enable pin voltage	0		44	V
I_S or I_D (CONT)	Source or drain continuous current (Sx, D)			I_{DC} ⁽²⁾	mA
T_A	Ambient temperature	–40		125	°C

(1) V_{DD} and V_{SS} can be any value as long as $4.5\text{ V} \leq (V_{DD} - V_{SS}) \leq 44\text{ V}$, and the minimum V_{DD} is met.

(2) Refer to *Source or Drain Continuous Current* table for I_{DC} specifications.

5.5 Source or Drain Continuous Current

at supply voltage of $V_{DD} \pm 10\%$, $V_{SS} \pm 10\%$ (unless otherwise noted)

CONTINUOUS CURRENT PER CHANNEL (I_{DC})		$T_A = 25^\circ\text{C}$	$T_A = 85^\circ\text{C}$	$T_A = 125^\circ\text{C}$	UNIT
PACKAGE	TEST CONDITIONS				
DGK (VSSOP)	+44 V Single Supply ⁽¹⁾	330	210	120	mA
	$\pm 15\text{ V}$ Dual Supply	330	210	120	mA
	+12 V Single Supply	240	160	100	mA
	$\pm 5\text{ V}$ Dual Supply	240	160	100	mA
	+5 V Single Supply	180	120	80	mA

(1) Specified for nominal supply voltage only.

5.6 ±15 V Dual Supply: Electrical Characteristics

$V_{DD} = +15\text{ V} \pm 10\%$, $V_{SS} = -15\text{ V} \pm 10\%$, GND = 0 V (unless otherwise noted)

Typical at $V_{DD} = +15\text{ V}$, $V_{SS} = -15\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T _A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R _{ON}	On-resistance	V _S = −10 V to +10 V I _D = −10 mA Refer to On-Resistance	25°C		2.1	2.9	Ω
			−40°C to +85°C			3.8	Ω
			−40°C to +125°C			4.5	Ω
ΔR _{ON}	On-resistance mismatch between channels	V _S = −10 V to +10 V I _D = −10 mA Refer to On-Resistance	25°C		0.05	0.25	Ω
			−40°C to +85°C			0.3	Ω
			−40°C to +125°C			0.35	Ω
R _{ON FLAT}	On-resistance flatness	V _S = −10 V to +10 V I _S = −10 mA Refer to On-Resistance	25°C		0.5	0.6	Ω
			−40°C to +85°C			0.7	Ω
			−40°C to +125°C			0.85	Ω
R _{ON DRIFT}	On-resistance drift	V _S = 0 V, I _S = −10 mA Refer to On-Resistance	−40°C to +125°C		0.01		Ω/°C
I _{S(OFF)}	Source off leakage current ⁽¹⁾	V _{DD} = 16.5 V, V _{SS} = −16.5 V Switch state is off V _S = +10 V / −10 V V _D = −10 V / +10 V Refer to Off-Leakage Current	25°C	−0.15	0.05	0.15	nA
			−40°C to +85°C	−1.6		1.6	nA
			−40°C to +125°C	−15		15	nA
I _{D(OFF)}	Drain off leakage current ⁽¹⁾	V _{DD} = 16.5 V, V _{SS} = −16.5 V Switch state is off V _S = +10 V / −10 V V _D = −10 V / +10 V Refer to Off-Leakage Current	25°C	−1	0.05	1	nA
			−40°C to +85°C	−3		3	nA
			−40°C to +125°C	−26		26	nA
I _{S(ON)} I _{D(ON)}	Channel on leakage current ⁽²⁾	V _{DD} = 16.5 V, V _{SS} = −16.5 V Switch state is on V _S = V _D = ±10 V Refer to On-Leakage Current	25°C	−1	0.04	1	nA
			−40°C to +85°C	−1.8		1.8	nA
			−40°C to +125°C	−18		18	nA
LOGIC INPUTS (SEL / EN pins)							
V _{IH}	Logic voltage high		−40°C to +125°C	1.3		44	V
V _{IL}	Logic voltage low		−40°C to +125°C	0		0.8	V
I _{IH}	Input leakage current		−40°C to +125°C		0.005	2	μA
I _{IL}	Input leakage current		−40°C to +125°C	−1	−0.005		μA
C _{IN}	Logic input capacitance		−40°C to +125°C		3		pF
POWER SUPPLY							
I _{DD}	V _{DD} supply current	V _{DD} = 16.5 V, V _{SS} = −16.5 V Logic inputs = 0 V, 5 V, or V _{DD}	25°C		30	40	μA
			−40°C to +85°C			48	μA
			−40°C to +125°C			62	μA
I _{SS}	V _{SS} supply current	V _{DD} = 16.5 V, V _{SS} = −16.5 V Logic inputs = 0 V, 5 V, or V _{DD}	25°C		3	10	μA
			−40°C to +85°C			15	μA
			−40°C to +125°C			25	μA

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.

(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

5.7 ±15 V Dual Supply: Switching Characteristics

$V_{DD} = +15\text{ V} \pm 10\%$, $V_{SS} = -15\text{ V} \pm 10\%$, $GND = 0\text{ V}$ (unless otherwise noted)

Typical at $V_{DD} = +15\text{ V}$, $V_{SS} = -15\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{TRAN}	Transition time from control input	$V_S = 10\text{ V}$ $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ Refer to Transition Time	25°C		120	175	ns
			-40°C to $+85^\circ\text{C}$			190	ns
			-40°C to $+125^\circ\text{C}$			210	ns
$t_{\text{ON (EN)}}$	Turn-on time from enable	$V_S = 10\text{ V}$ $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ Refer to Turn-on and Turn-off Time	25°C		100	170	ns
			-40°C to $+85^\circ\text{C}$			185	ns
			-40°C to $+125^\circ\text{C}$			200	ns
$t_{\text{OFF (EN)}}$	Turn-off time from enable	$V_S = 10\text{ V}$ $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ Refer to Turn-on and Turn-off Time	25°C		100	180	ns
			-40°C to $+85^\circ\text{C}$			195	ns
			-40°C to $+125^\circ\text{C}$			210	ns
t_{BBM}	Break-before-make time delay	$V_S = 10\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ Refer to Break-Before-Make	25°C		50		ns
			-40°C to $+85^\circ\text{C}$	1			ns
			-40°C to $+125^\circ\text{C}$	1			ns
$T_{\text{ON (VDD)}}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 100ns $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ Refer to Turn-on (VDD) Time	25°C		0.19		ms
			-40°C to $+85^\circ\text{C}$		0.2		ms
			-40°C to $+125^\circ\text{C}$		0.2		ms
t_{PD}	Propagation delay	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ Refer to Propagation Delay	25°C		700		ps
Q_{INJ}	Charge injection	$V_D = 0\text{ V}$, $C_L = 1\text{ nF}$ Refer to Charge Injection	25°C		-10		pC
O_{ISO}	Off-isolation	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ $V_S = 0\text{ V}$, $f = 100\text{ kHz}$ Refer to Off Isolation	25°C		-75		dB
O_{ISO}	Off-isolation	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ $V_S = 0\text{ V}$, $f = 1\text{ MHz}$ Refer to Off Isolation	25°C		-55		dB
X_{TALK}	Crosstalk	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ $V_S = 0\text{ V}$, $f = 100\text{ kHz}$ Refer to Crosstalk	25°C		-117		dB
X_{TALK}	Crosstalk	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ $V_S = 0\text{ V}$, $f = 1\text{ MHz}$ Refer to Crosstalk	25°C		-106		dB
BW	-3dB Bandwidth	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ $V_S = 0\text{ V}$ Refer to Bandwidth	25°C		40		MHz
I_L	Insertion loss	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ $V_S = 0\text{ V}$, $f = 1\text{ MHz}$	25°C		-0.18		dB
ACPSRR	AC Power Supply Rejection Ratio	$V_{PP} = 0.62\text{ V}$ on V_{DD} and V_{SS} $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$ Refer to ACPSRR	25°C		-64		dB
THD+N	Total Harmonic Distortion + Noise	$V_{PP} = 15\text{ V}$, $V_{\text{BIAS}} = 0\text{ V}$ $R_L = 10\text{ k}\Omega$, $C_L = 5\text{ pF}$, $f = 20\text{ Hz}$ to 20 kHz Refer to THD + Noise	25°C		0.0005		%
$C_{\text{S(OFF)}}$	Source off capacitance	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$	25°C		33		pF
$C_{\text{D(OFF)}}$	Drain off capacitance	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$	25°C		48		pF
$C_{\text{S(ON)}}$, $C_{\text{D(ON)}}$	On capacitance	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$	25°C		148		pF

5.8 ±20 V Dual Supply: Electrical Characteristics

$V_{DD} = +20\text{ V} \pm 10\%$, $V_{SS} = -20\text{ V} \pm 10\%$, GND = 0 V (unless otherwise noted)

Typical at $V_{DD} = +20\text{ V}$, $V_{SS} = -20\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T _A	MIN	TYP	MAX	UNIT		
ANALOG SWITCH									
R _{ON}	On-resistance	V _S = −15 V to +15 V I _D = −10 mA Refer to On-Resistance	25°C		1.9	2.7	Ω		
			−40°C to +85°C			3.5	Ω		
			−40°C to +125°C			4.2	Ω		
ΔR _{ON}	On-resistance mismatch between channels	V _S = −15 V to +15 V I _D = −10 mA Refer to On-Resistance	25°C		0.04	0.22	Ω		
			−40°C to +85°C			0.28	Ω		
			−40°C to +125°C			0.3	Ω		
R _{ON FLAT}	On-resistance flatness	V _S = −15 V to +15 V I _S = −10 mA Refer to On-Resistance	25°C		0.3	0.75	Ω		
			−40°C to +85°C			0.9	Ω		
			−40°C to +125°C			1.2	Ω		
R _{ON DRIFT}	On-resistance drift	V _S = 0 V, I _S = −10 mA Refer to On-Resistance	−40°C to +125°C		0.009		Ω/°C		
I _{S(OFF)}	Source off leakage current ⁽¹⁾	V _{DD} = 22 V, V _{SS} = −22 V Switch state is off V _S = +15 V / −15 V V _D = −15 V / +15 V Refer to Off-Leakage Current	25°C	−1.5	0.05	1.5	nA		
			−40°C to +85°C		−4		4	nA	
			−40°C to +125°C		−24		24	nA	
I _{D(OFF)}	Drain off leakage current ⁽¹⁾	V _{DD} = 22 V, V _{SS} = −22 V Switch state is off V _S = +15 V / −15 V V _D = −15 V / +15 V Refer to Off-Leakage Current	25°C	−2	0.1	2	nA		
			−40°C to +85°C		−8		8	nA	
			−40°C to +125°C		−44		44	nA	
I _{S(ON)} I _{D(ON)}	Channel on leakage current ⁽²⁾	V _{DD} = 22 V, V _{SS} = −22 V Switch state is on V _S = V _D = ±15 V Refer to On-Leakage Current	25°C	−2	0.1	2	nA		
			−40°C to +85°C		−5		5	nA	
			−40°C to +125°C		−29		29	nA	
LOGIC INPUTS (SEL / EN pins)									
V _{IH}	Logic voltage high		−40°C to +125°C		1.3		44	V	
V _{IL}	Logic voltage low		−40°C to +125°C		0		0.8	V	
I _{IH}	Input leakage current		−40°C to +125°C			0.005		2	μA
I _{IL}	Input leakage current		−40°C to +125°C		−1	−0.005			μA
C _{IN}	Logic input capacitance		−40°C to +125°C			3			pF
POWER SUPPLY									
I _{DD}	V _{DD} supply current	V _{DD} = 22 V, V _{SS} = −22 V Logic inputs = 0 V, 5 V, or V _{DD}	25°C			34		44	μA
			−40°C to +85°C					50	μA
			−40°C to +125°C					65	μA
I _{SS}	V _{SS} supply current	V _{DD} = 22 V, V _{SS} = −22 V Logic inputs = 0 V, 5 V, or V _{DD}	25°C			4		9	μA
			−40°C to +85°C					12	μA
			−40°C to +125°C					25	μA

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.

(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

5.9 ±20 V Dual Supply: Switching Characteristics

$V_{DD} = +20\text{ V} \pm 10\%$, $V_{SS} = -20\text{ V} \pm 10\%$, GND = 0 V (unless otherwise noted)

Typical at $V_{DD} = +20\text{ V}$, $V_{SS} = -20\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{TRAN}	Transition time from control input	$V_S = 10\text{ V}$ $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ Refer to Transition Time	25°C		110	175	ns
			-40°C to $+85^\circ\text{C}$			190	ns
			-40°C to $+125^\circ\text{C}$			205	ns
$t_{\text{ON (EN)}}$	Turn-on time from enable	$V_S = 10\text{ V}$ $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ Refer to Turn-on and Turn-off Time	25°C		110	170	ns
			-40°C to $+85^\circ\text{C}$			185	ns
			-40°C to $+125^\circ\text{C}$			200	ns
$t_{\text{OFF (EN)}}$	Turn-off time from enable	$V_S = 10\text{ V}$ $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ Refer to Turn-on and Turn-off Time	25°C		90	180	ns
			-40°C to $+85^\circ\text{C}$			190	ns
			-40°C to $+125^\circ\text{C}$			200	ns
t_{BBM}	Break-before-make time delay	$V_S = 10\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ Refer to Break-Before-Make	25°C		55		ns
			-40°C to $+85^\circ\text{C}$	1			ns
			-40°C to $+125^\circ\text{C}$	1			ns
$T_{\text{ON (VDD)}}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 100ns $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ Refer to Turn-on (VDD) Time	25°C		0.18		ms
			-40°C to $+85^\circ\text{C}$		0.2		ms
			-40°C to $+125^\circ\text{C}$		0.2		ms
t_{PD}	Propagation delay	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ Refer to Propagation Delay	25°C		715		ps
Q_{INJ}	Charge injection	$V_D = 0\text{ V}$, $C_L = 1\text{ nF}$ Refer to Charge Injection	25°C		-15		pC
O_{ISO}	Off-isolation	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ $V_S = 0\text{ V}$, $f = 100\text{ kHz}$ Refer to Off Isolation	25°C		-75		dB
O_{ISO}	Off-isolation	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ $V_S = 0\text{ V}$, $f = 1\text{ MHz}$ Refer to Off Isolation	25°C		-55		dB
X_{TALK}	Crosstalk	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ $V_S = 0\text{ V}$, $f = 100\text{ kHz}$ Refer to Crosstalk	25°C		-117		dB
X_{TALK}	Crosstalk	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ $V_S = 0\text{ V}$, $f = 1\text{ MHz}$ Refer to Crosstalk	25°C		-106		dB
BW	-3dB Bandwidth	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ $V_S = 0\text{ V}$, Refer to Bandwidth	25°C		38		MHz
I_L	Insertion loss	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ $V_S = 0\text{ V}$, $f = 1\text{ MHz}$	25°C		-0.16		dB
ACPSRR	AC Power Supply Rejection Ratio	$V_{PP} = 0.62\text{ V}$ on V_{DD} and V_{SS} $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$ Refer to ACPSRR	25°C		-63		dB
THD+N	Total Harmonic Distortion + Noise	$V_{PP} = 20\text{ V}$, $V_{\text{BIAS}} = 0\text{ V}$ $R_L = 10\text{ k}\Omega$, $C_L = 5\text{ pF}$, $f = 20\text{ Hz}$ to 20 kHz Refer to THD + Noise	25°C		0.0005		%
$C_{\text{S(OFF)}}$	Source off capacitance	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$	25°C		32		pF
$C_{\text{D(OFF)}}$	Drain off capacitance	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$	25°C		45		pF
$C_{\text{S(ON)}}$, $C_{\text{D(ON)}}$	On capacitance	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$	25°C		146		pF

5.10 44 V Single Supply: Electrical Characteristics

$V_{DD} = +44\text{ V}$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$ (unless otherwise noted)

Typical at $V_{DD} = +44\text{ V}$, $V_{SS} = 0\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T _A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R _{ON}	On-resistance	V _S = 0 V to 40 V I _D = −10 mA Refer to On-Resistance	25°C		2.2	2.8	Ω
			−40°C to +85°C			3.6	Ω
			−40°C to +125°C			4.2	Ω
ΔR _{ON}	On-resistance mismatch between channels	V _S = 0 V to 40 V I _D = −10 mA Refer to On-Resistance	25°C		0.1	0.2	Ω
			−40°C to +85°C			0.3	Ω
			−40°C to +125°C			0.35	Ω
R _{ON FLAT}	On-resistance flatness	V _S = 0 V to 40 V I _D = −10 mA Refer to On-Resistance	25°C		0.2	1	Ω
			−40°C to +85°C			1.3	Ω
			−40°C to +125°C			1.5	Ω
R _{ON DRIFT}	On-resistance drift	V _S = 22 V, I _S = −10 mA Refer to On-Resistance	−40°C to +125°C		0.008		Ω/°C
I _{S(OFF)}	Source off leakage current ⁽¹⁾	V _{DD} = 44 V, V _{SS} = 0 V Switch state is off V _S = 40 V / 1 V V _D = 1 V / 40 V Refer to Off-Leakage Current	25°C	−5	0.05	5	nA
			−40°C to +85°C	−10		10	nA
			−40°C to +125°C	−35		35	nA
I _{D(OFF)}	Drain off leakage current ⁽¹⁾	V _{DD} = 44 V, V _{SS} = 0 V Switch state is off V _S = 40 V / 1 V V _D = 1 V / 40 V Refer to Off-Leakage Current	25°C	−8	0.05	8	nA
			−40°C to +85°C	−12		12	nA
			−40°C to +125°C	−70		70	nA
I _{S(ON)} I _{D(ON)}	Channel on leakage current ⁽²⁾	V _{DD} = 44 V, V _{SS} = 0 V Switch state is on V _S = V _D = 40 V or 1 V Refer to On-Leakage Current	25°C	−8	0.05	8	nA
			−40°C to +85°C	−10		10	nA
			−40°C to +125°C	−45		45	nA
LOGIC INPUTS (SEL / EN pins)							
V _{IH}	Logic voltage high		−40°C to +125°C	1.3		44	V
V _{IL}	Logic voltage low		−40°C to +125°C	0		0.8	V
I _{IH}	Input leakage current		−40°C to +125°C		0.005	2	μA
I _{IL}	Input leakage current		−40°C to +125°C	−1	−0.005		μA
C _{IN}	Logic input capacitance		−40°C to +125°C		3		pF
POWER SUPPLY							
I _{DD}	V _{DD} supply current	V _{DD} = 44 V, V _{SS} = 0 V Logic inputs = 0 V, 5 V, or V _{DD}	25°C		17	50	μA
			−40°C to +85°C			60	μA
			−40°C to +125°C			75	μA

(1) When V_S is 40 V , V_D is 1 V , or when V_S is 1 V , V_D is 40 V .

(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

5.11 44 V Single Supply: Switching Characteristics

$V_{DD} = +44\text{ V}$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$ (unless otherwise noted)
Typical at $V_{DD} = +44\text{ V}$, $V_{SS} = 0\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{TRAN}	Transition time from control input	$V_S = 18\text{ V}$ $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ Refer to Transition Time	25°C		120	175	ns
			-40°C to $+85^\circ\text{C}$			190	ns
			-40°C to $+125^\circ\text{C}$			205	ns
$t_{\text{ON (EN)}}$	Turn-on time from enable	$V_S = 18\text{ V}$ $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ Refer to Turn-on and Turn-off Time	25°C		120	168	ns
			-40°C to $+85^\circ\text{C}$			185	ns
			-40°C to $+125^\circ\text{C}$			195	ns
$t_{\text{OFF (EN)}}$	Turn-off time from enable	$V_S = 18\text{ V}$ $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ Refer to Turn-on and Turn-off Time	25°C		120	180	ns
			-40°C to $+85^\circ\text{C}$			200	ns
			-40°C to $+125^\circ\text{C}$			205	ns
t_{BBM}	Break-before-make time delay	$V_S = 18\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ Refer to Break-Before-Make	25°C		45		ns
			-40°C to $+85^\circ\text{C}$	1			ns
			-40°C to $+125^\circ\text{C}$	1			ns
$T_{\text{ON (VDD)}}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = $1\ \mu\text{s}$ $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ Refer to Turn-on (VDD) Time	25°C		0.15		ms
			-40°C to $+85^\circ\text{C}$		0.17		ms
			-40°C to $+125^\circ\text{C}$		0.17		ms
t_{PD}	Propagation delay	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ Refer to Propagation Delay	25°C		930		ps
Q_{INJ}	Charge injection	$V_D = 22\text{ V}$, $C_L = 1\text{ nF}$ Refer to Charge Injection	25°C		-16		pC
O_{ISO}	Off-isolation	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ $V_S = 6\text{ V}$, $f = 100\text{ kHz}$ Refer to Off Isolation	25°C		-75		dB
O_{ISO}	Off-isolation	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ $V_S = 6\text{ V}$, $f = 1\text{ MHz}$ Refer to Off Isolation	25°C		-55		dB
X_{TALK}	Crosstalk	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ $V_S = 6\text{ V}$, $f = 100\text{ kHz}$ Refer to Crosstalk	25°C		-117		dB
X_{TALK}	Crosstalk	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ $V_S = 6\text{ V}$, $f = 1\text{ MHz}$ Refer to Crosstalk	25°C		-106		dB
BW	-3dB Bandwidth	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ $V_S = 6\text{ V}$ Refer to Bandwidth	25°C		37		MHz
I_L	Insertion loss	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ $V_S = 6\text{ V}$, $f = 1\text{ MHz}$	25°C		-0.18		dB
ACPSRR	AC Power Supply Rejection Ratio	$V_{PP} = 0.62\text{ V}$ on V_{DD} and V_{SS} $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$ Refer to ACPSRR	25°C		-60		dB
THD+N	Total Harmonic Distortion + Noise	$V_{PP} = 22\text{ V}$, $V_{\text{BIAS}} = 22\text{ V}$ $R_L = 10\text{ k}\Omega$, $C_L = 5\text{ pF}$, $f = 20\text{ Hz}$ to 20 kHz Refer to THD + Noise	25°C		0.0004		%
$C_{S(\text{OFF})}$	Source off capacitance	$V_S = 6\text{ V}$, $f = 1\text{ MHz}$	25°C		34		pF
$C_{D(\text{OFF})}$	Drain off capacitance	$V_S = 6\text{ V}$, $f = 1\text{ MHz}$	25°C		48		pF
$C_{S(\text{ON})}$, $C_{D(\text{ON})}$	On capacitance	$V_S = 6\text{ V}$, $f = 1\text{ MHz}$	25°C		146		pF

5.12 12 V Single Supply: Electrical Characteristics

$V_{DD} = +12\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$ (unless otherwise noted)

Typical at $V_{DD} = +12\text{ V}$, $V_{SS} = 0\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T _A	MIN	TYP	MAX	UNIT		
ANALOG SWITCH									
R _{ON}	On-resistance	V _S = 0 V to 10 V I _D = −10 mA Refer to On-Resistance	25°C		4.6	6	Ω		
			−40°C to +85°C			7.5	Ω		
			−40°C to +125°C			8.4	Ω		
ΔR _{ON}	On-resistance mismatch between channels	V _S = 0 V to 10 V I _D = −10 mA Refer to On-Resistance	25°C		0.08	0.2	Ω		
			−40°C to +85°C			0.32	Ω		
			−40°C to +125°C			0.35	Ω		
R _{ON FLAT}	On-resistance flatness	V _S = 0 V to 10 V I _S = −10 mA Refer to On-Resistance	25°C		1.2	2	Ω		
			−40°C to +85°C			2.2	Ω		
			−40°C to +125°C			2.4	Ω		
R _{ON DRIFT}	On-resistance drift	V _S = 6 V, I _S = −10 mA Refer to On-Resistance	−40°C to +125°C		0.017		Ω/°C		
I _{S(OFF)}	Source off leakage current ⁽¹⁾	V _{DD} = 13.2 V, V _{SS} = 0 V Switch state is off V _S = 10 V / 1 V V _D = 1 V / 10 V Refer to Off-Leakage Current	25°C	−0.5	0.05	0.5	nA		
			−40°C to +85°C			−2	2	nA	
			−40°C to +125°C			−12	12	nA	
I _{D(OFF)}	Drain off leakage current ⁽¹⁾	V _{DD} = 13.2 V, V _{SS} = 0 V Switch state is off V _S = 10 V / 1 V V _D = 1 V / 10 V Refer to Off-Leakage Current	25°C	−0.5	0.05	0.5	nA		
			−40°C to +85°C			−3	3	nA	
			−40°C to +125°C			−23	23	nA	
I _{S(ON)} I _{D(ON)}	Channel on leakage current ⁽²⁾	V _{DD} = 13.2 V, V _{SS} = 0 V Switch state is on V _S = V _D = 10 V or 1 V Refer to On-Leakage Current	25°C	−1.5	0.05	1.5	nA		
			−40°C to +85°C			−3	3	nA	
			−40°C to +125°C			−15	15	nA	
LOGIC INPUTS (SEL / EN pins)									
V _{IH}	Logic voltage high		−40°C to +125°C		1.3		44	V	
V _{IL}	Logic voltage low		−40°C to +125°C		0		0.8	V	
I _{IH}	Input leakage current		−40°C to +125°C		0.005		2	μA	
I _{IL}	Input leakage current		−40°C to +125°C		−1	−0.005		μA	
C _{IN}	Logic input capacitance		−40°C to +125°C			3		pF	
POWER SUPPLY									
I _{DD}	V _{DD} supply current	V _{DD} = 13.2 V, V _{SS} = 0 V Logic inputs = 0 V, 5 V, or V _{DD}	25°C		10	35		μA	
			−40°C to +85°C				45		μA
			−40°C to +125°C					55	

(1) When V_S is 10 V , V_D is 1 V , or when V_S is 1 V , V_D is 10 V .

(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

5.13 12 V Single Supply: Switching Characteristics

$V_{DD} = +12\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$ (unless otherwise noted)
Typical at $V_{DD} = +12\text{ V}$, $V_{SS} = 0\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{TRAN}	Transition time from control input	$V_S = 8\text{ V}$ $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ Refer to Transition Time	25°C		180	185	ns
			-40°C to $+85^\circ\text{C}$			215	ns
			-40°C to $+125^\circ\text{C}$			235	ns
$t_{\text{ON (EN)}}$	Turn-on time from enable	$V_S = 8\text{ V}$ $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ Refer to Turn-on and Turn-off Time	25°C		120	180	ns
			-40°C to $+85^\circ\text{C}$			210	ns
			-40°C to $+125^\circ\text{C}$			230	ns
$t_{\text{OFF (EN)}}$	Turn-off time from enable	$V_S = 8\text{ V}$ $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ Refer to Turn-on and Turn-off Time	25°C		130	210	ns
			-40°C to $+85^\circ\text{C}$			235	ns
			-40°C to $+125^\circ\text{C}$			250	ns
t_{BBM}	Break-before-make time delay	$V_S = 8\text{ V}$, $R_L = 50\ \Omega$, $C_L = 35\text{ pF}$ Refer to Break-Before-Make	25°C		40		ns
			-40°C to $+85^\circ\text{C}$	1			ns
			-40°C to $+125^\circ\text{C}$	1			ns
$T_{\text{ON (VDD)}}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 100ns $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ Refer to Turn-on (VDD) Time	25°C		0.19		ms
			-40°C to $+85^\circ\text{C}$		0.2		ms
			-40°C to $+125^\circ\text{C}$		0.2		ms
t_{PD}	Propagation delay	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ Refer to Propagation Delay	25°C		740		ps
Q_{INJ}	Charge injection	$V_D = 6\text{ V}$, $C_L = 1\text{ nF}$ Refer to Charge Injection	25°C		–6		pC
O_{ISO}	Off-isolation	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ $V_S = 6\text{ V}$, $f = 100\text{ kHz}$ Refer to Off Isolation	25°C		–75		dB
O_{ISO}	Off-isolation	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ $V_S = 6\text{ V}$, $f = 1\text{ MHz}$ Refer to Off Isolation	25°C		–55		dB
X_{TALK}	Crosstalk	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ $V_S = 6\text{ V}$, $f = 100\text{ kHz}$ Refer to Crosstalk	25°C		–117		dB
X_{TALK}	Crosstalk	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ $V_S = 6\text{ V}$, $f = 1\text{ MHz}$ Refer to Crosstalk	25°C		–106		dB
BW	–3dB Bandwidth	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ $V_S = 6\text{ V}$ Refer to Bandwidth	25°C		42		MHz
I_L	Insertion loss	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ $V_S = 6\text{ V}$, $f = 1\text{ MHz}$	25°C		–0.3		dB
ACPSRR	AC Power Supply Rejection Ratio	$V_{PP} = 0.62\text{ V}$ on V_{DD} and V_{SS} $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$ Refer to ACPSRR	25°C		–65		dB
THD+N	Total Harmonic Distortion + Noise	$V_{PP} = 6\text{ V}$, $V_{\text{BIAS}} = 6\text{ V}$ $R_L = 10\text{ k}\Omega$, $C_L = 5\text{ pF}$, $f = 20\text{ Hz}$ to 20 kHz Refer to THD + Noise	25°C		0.0009		%
$C_{\text{S(OFF)}}$	Source off capacitance	$V_S = 6\text{ V}$, $f = 1\text{ MHz}$	25°C		38		pF
$C_{\text{D(OFF)}}$	Drain off capacitance	$V_S = 6\text{ V}$, $f = 1\text{ MHz}$	25°C		56		pF
$C_{\text{S(ON)}}$, $C_{\text{D(ON)}}$	On capacitance	$V_S = 6\text{ V}$, $f = 1\text{ MHz}$	25°C		150		pF

5.14 Typical Characteristics

at $T_A = 25^\circ\text{C}$

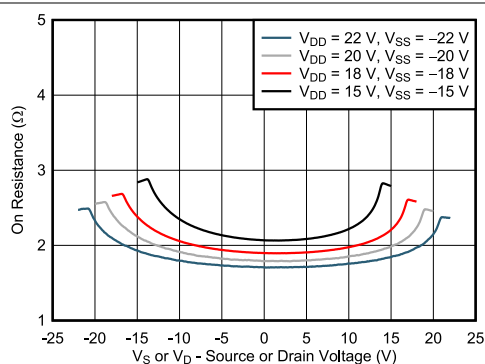


Figure 5-1. On-Resistance vs Source or Drain Voltage – Dual Supply

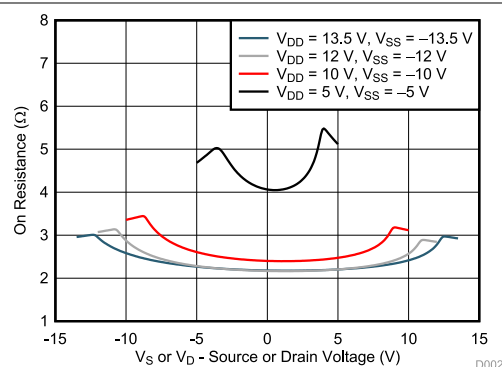


Figure 5-2. On-Resistance vs Source or Drain Voltage – Dual Supply

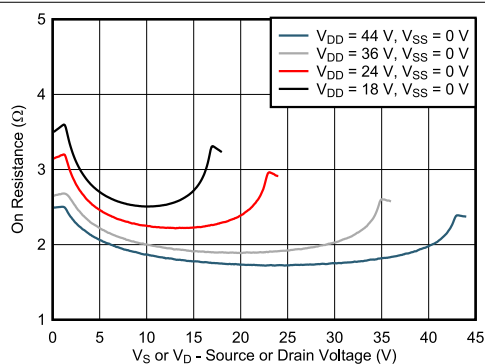


Figure 5-3. On-Resistance vs Source or Drain Voltage – Single Supply

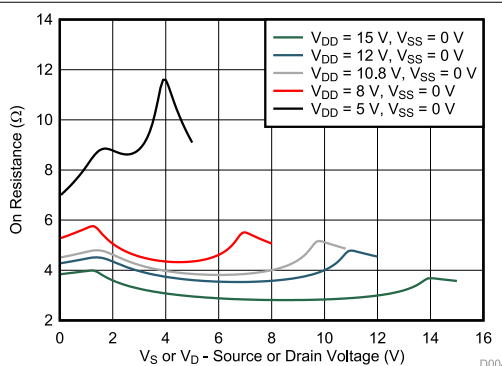


Figure 5-4. On-Resistance vs Source or Drain Voltage – Single Supply

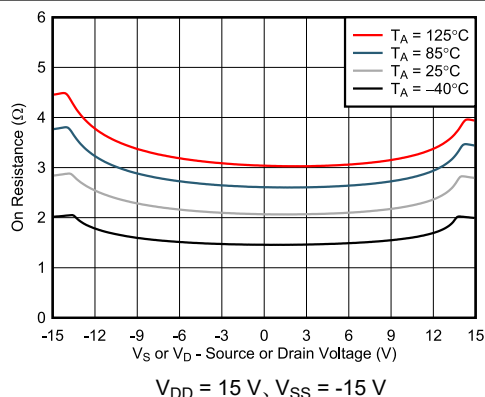


Figure 5-5. On-Resistance vs Temperature

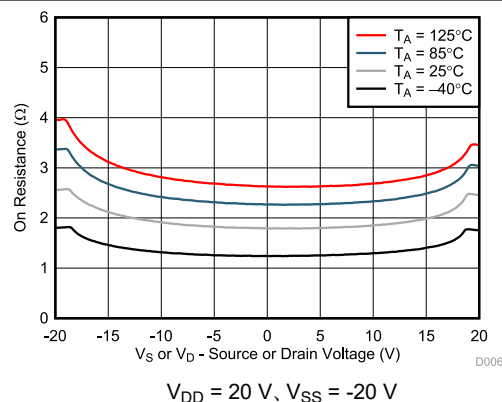


Figure 5-6. On-Resistance vs Temperature

5.14 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$

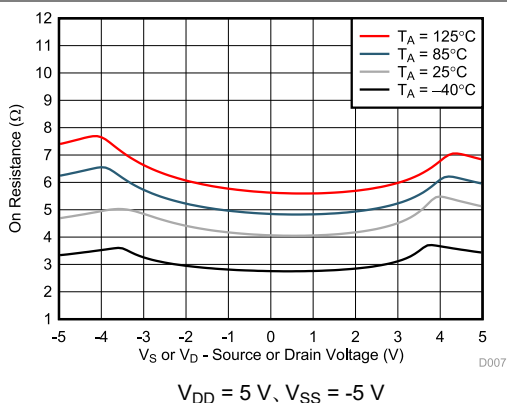


図 5-7. On-Resistance vs Temperature

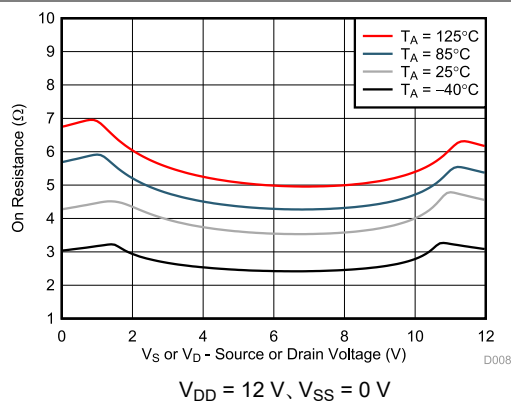


図 5-8. On-Resistance vs Temperature

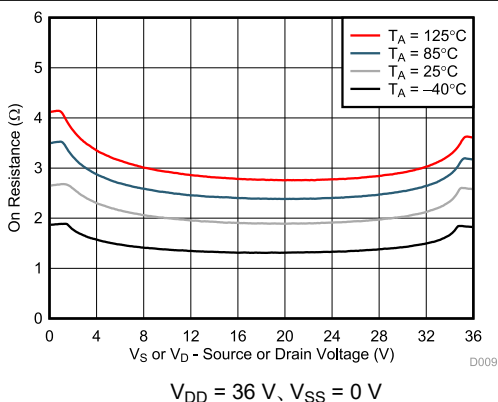


図 5-9. On-Resistance vs Temperature

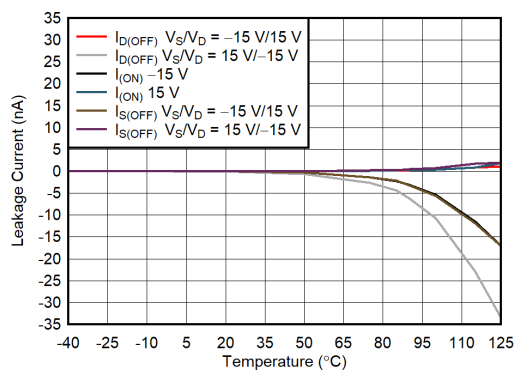


図 5-10. Leakage Current vs Temperature

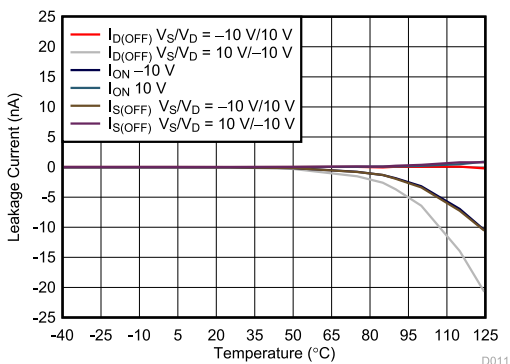


図 5-11. Leakage Current vs Temperature

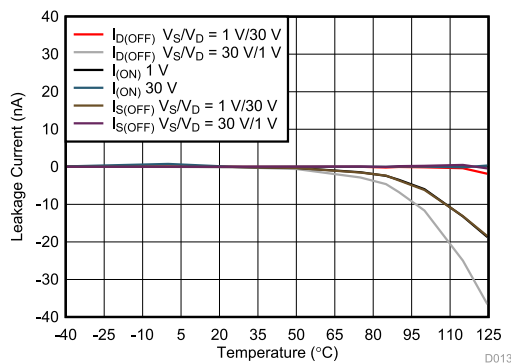
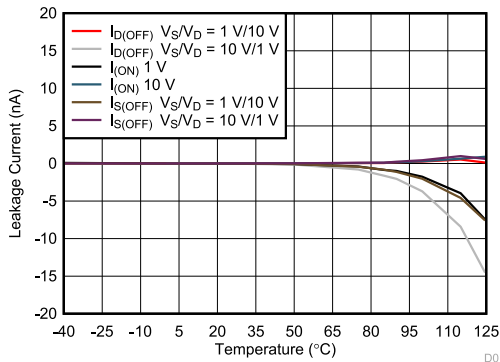


図 5-12. Leakage Current vs Temperature

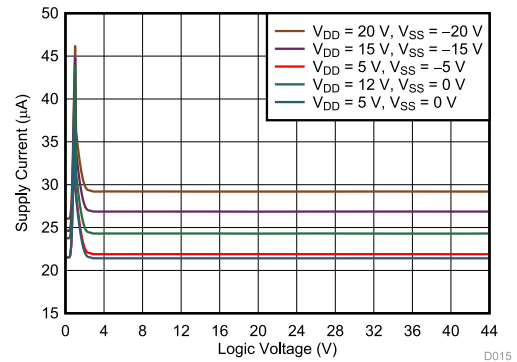
5.14 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$

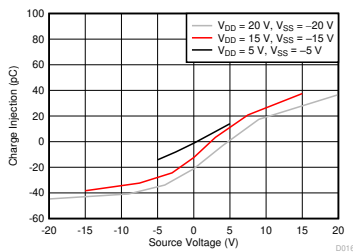


$V_{DD} = 12\text{ V}$, $V_{SS} = 0\text{ V}$

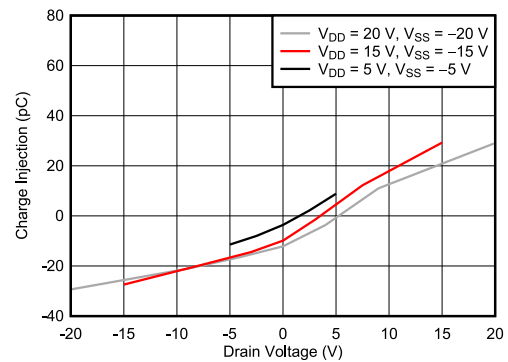
5-13. Leakage Current vs Temperature



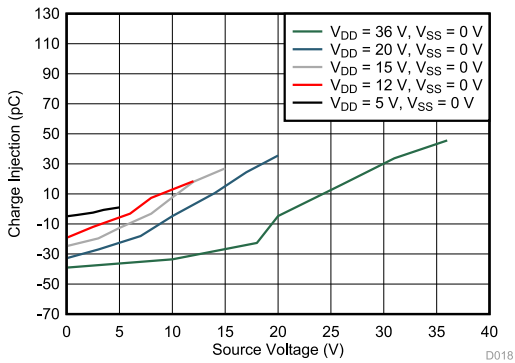
5-14. Supply Current vs Logic Voltage



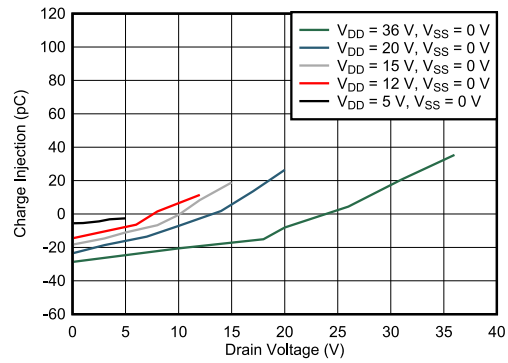
5-15. Charge Injection vs Source Voltage – Dual Supply



5-16. Charge Injection vs Drain Voltage – Dual Supply



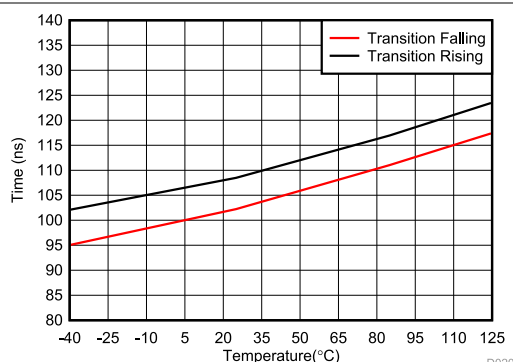
5-17. Charge Injection vs Source Voltage – Single Supply



5-18. Charge Injection vs Drain Voltage – Single Supply

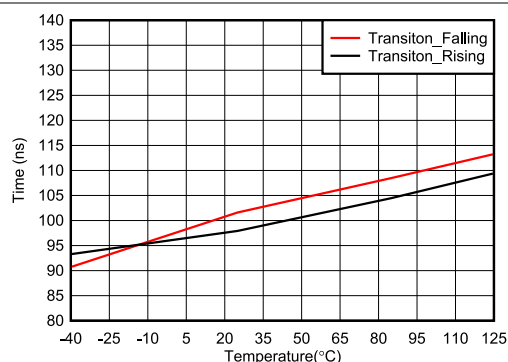
5.14 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$



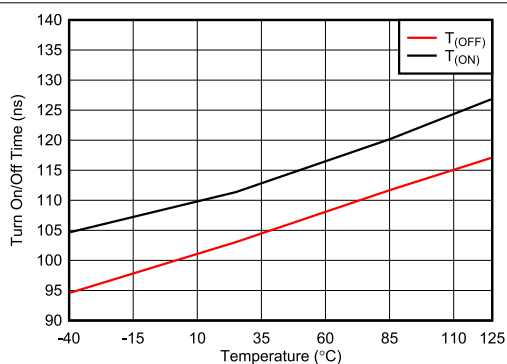
$V_{DD} = 15\text{ V}$, $V_{SS} = -15\text{ V}$

図 5-19. $T_{\text{TRANSITION}}$ vs Temperature



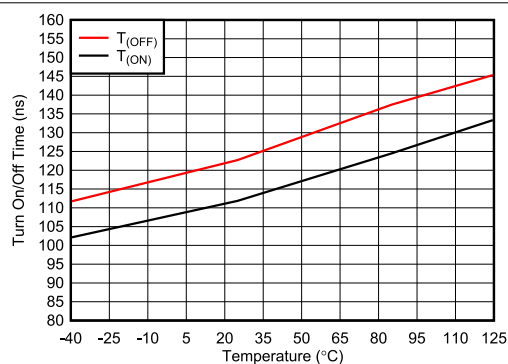
$V_{DD} = 44\text{ V}$, $V_{SS} = 0\text{ V}$

図 5-20. $T_{\text{TRANSITION}}$ vs Temperature



$V_{DD} = 15\text{ V}$, $V_{SS} = -15\text{ V}$

図 5-21. T_{ON} and T_{OFF} vs Temperature



$V_{DD} = 44\text{ V}$, $V_{SS} = 0\text{ V}$

図 5-22. T_{ON} and T_{OFF} vs Temperature

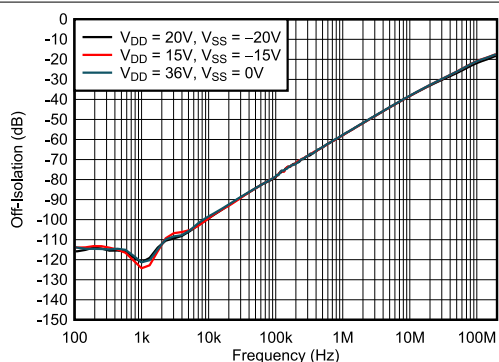
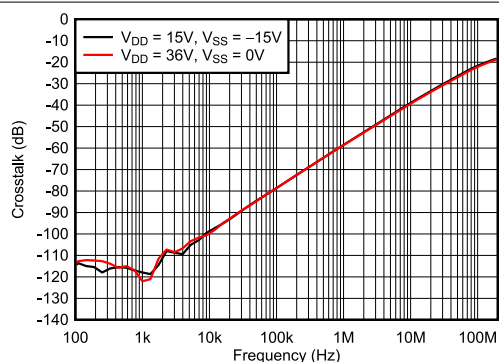


図 5-23. Off-Isolation vs Frequency

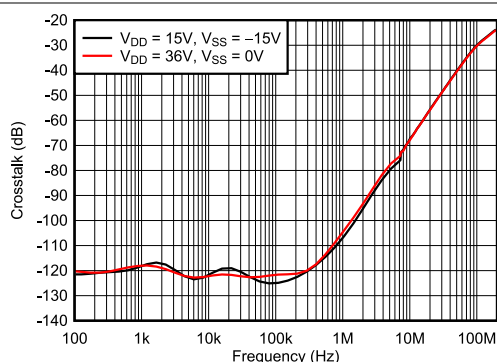


スイッチ オン ($EN = 1$)

図 5-24. Crosstalk vs Frequency

5.14 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$



スイッチ オフ (EN = 0)

図 5-25. Crosstalk vs Frequency

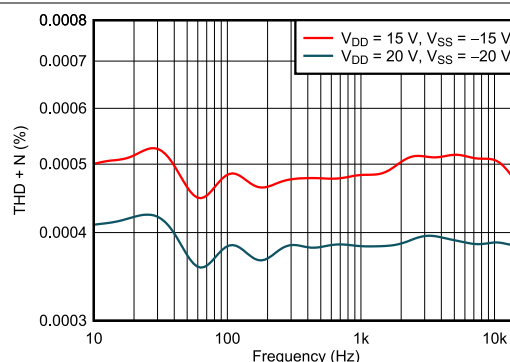


図 5-26. THD+N vs Frequency (Dual Supply)

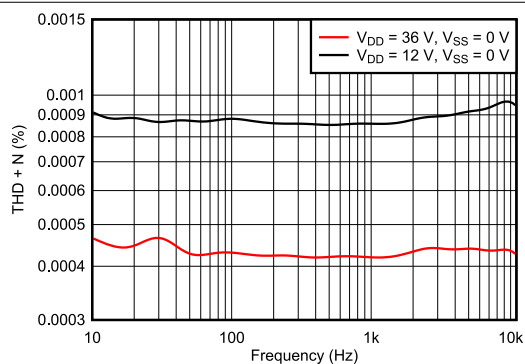
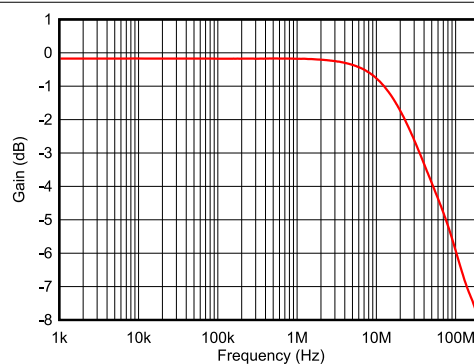
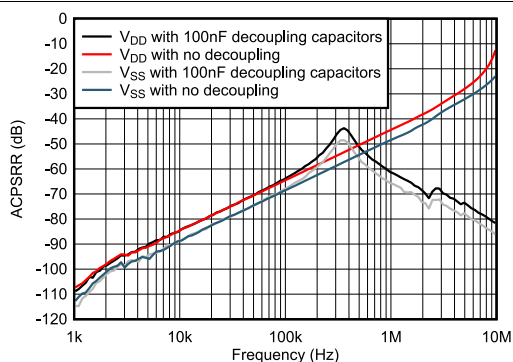


図 5-27. THD+N vs Frequency (Single Supply)



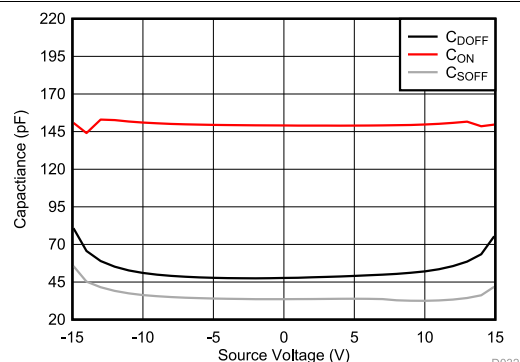
$V_{DD} = 15\text{ V}$, $V_{SS} = -15\text{ V}$

図 5-28. On Response vs Frequency



$V_{DD} = +15\text{ V}$, $V_{SS} = -15\text{ V}$

図 5-29. ACPSRR vs Frequency

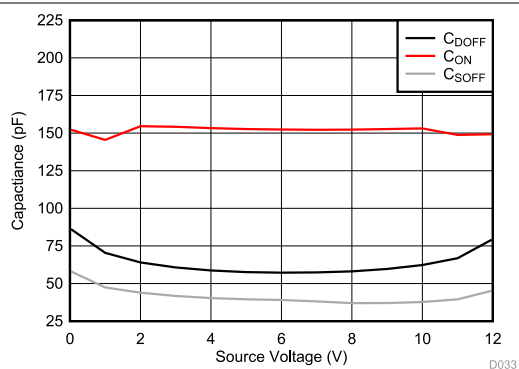


$V_{DD} = +15\text{ V}$, $V_{SS} = -15\text{ V}$

図 5-30. Capacitance vs Source Voltage or Drain Voltage

5.14 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$

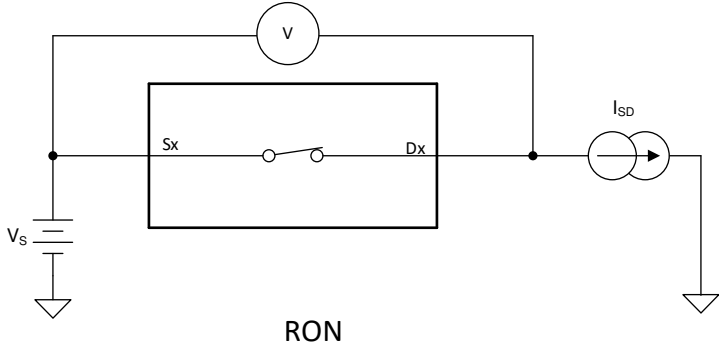


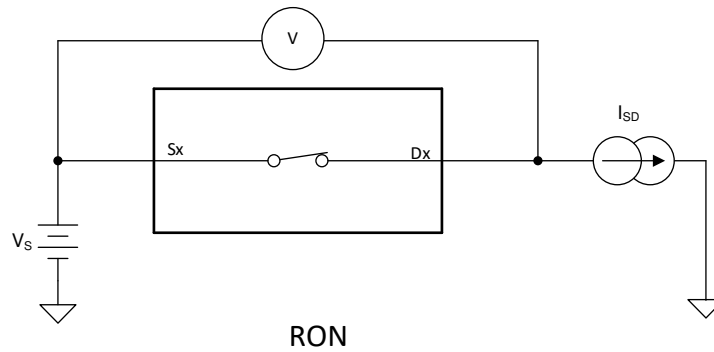
$V_{DD} = 12\text{ V}$, $V_{SS} = 0\text{ V}$

図 5-31. Capacitance vs Source Voltage or Drain Voltage

6 Parameter Measurement Information

6.1 On-Resistance

The on-resistance of a device is the ohmic resistance between the source (Sx) and drain (D) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance.  shows the measurement setup used to measure R_{ON} . Voltage (V) and current (I_{SD}) are measured using the following setup, where R_{ON} is computed as $R_{ON} = V / I_{SD}$:



 **6-1. On-Resistance**


6.2 Off-Leakage Current

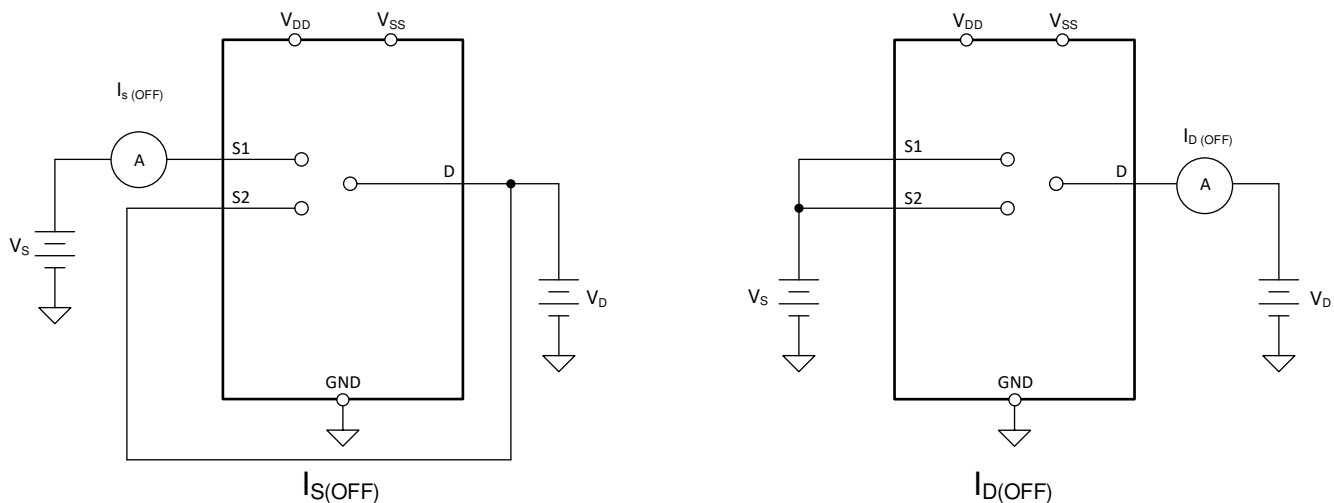
There are two types of leakage currents associated with a switch during the off state:

1. Source off-leakage current.
2. Drain off-leakage current.

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

Drain leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol $I_{D(OFF)}$.

 **6-2** shows the setup used to measure both off-leakage currents.



 **6-2. Off-Leakage Measurement Setup**

6.3 On-Leakage Current

Source on-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is on. This current is denoted by the symbol $I_{S(ON)}$.

Drain on-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is on. This current is denoted by the symbol $I_{D(ON)}$.

Either the source pin or drain pin is left floating during the measurement. Figure 6-3 shows the circuit used for measuring the on-leakage current, denoted by $I_{S(ON)}$ or $I_{D(ON)}$.

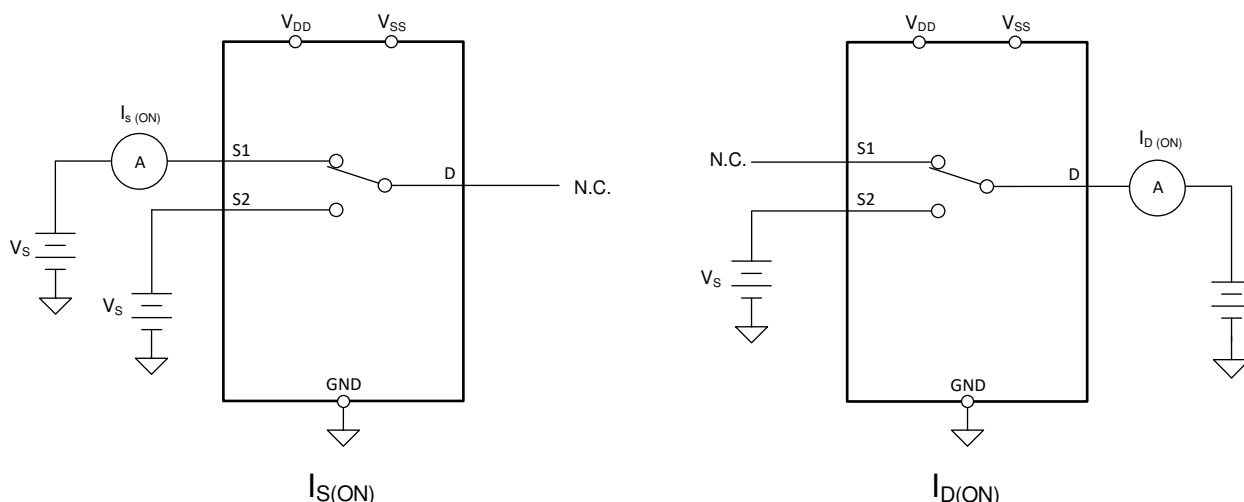


Figure 6-3. On-Leakage Measurement Setup

6.4 Transition Time

Transition time is defined as the time taken by the output of the device to rise or fall 90% after the address signal has risen or fallen past the logic threshold. The 90% transition measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. Figure 6-4 shows the setup used to measure transition time, denoted by the symbol $t_{\text{TRANSITION}}$.

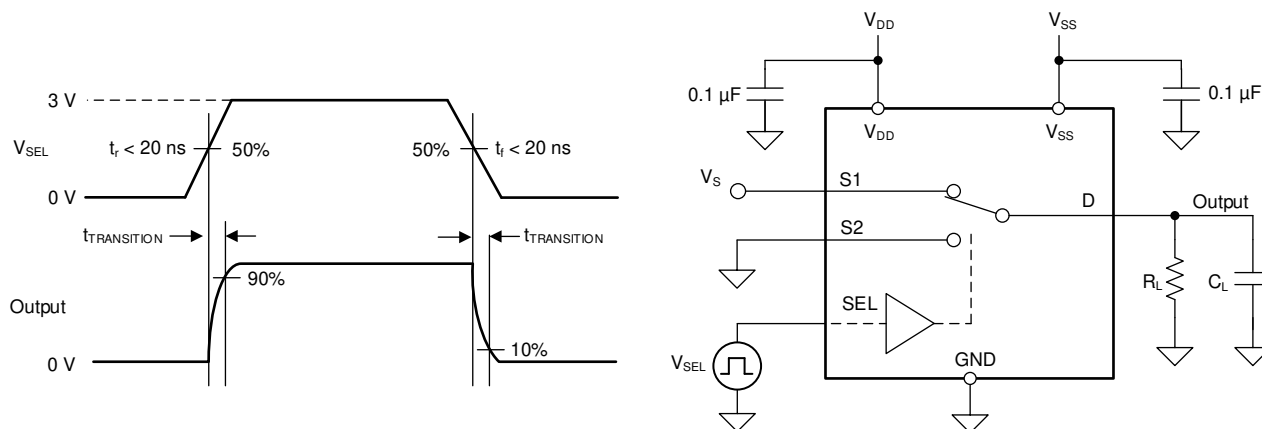


Figure 6-4. Transition-Time Measurement Setup

6.5 $t_{ON(EN)}$ and $t_{OFF(EN)}$

Turn-on time is defined as the time taken by the output of the device to rise to 90% after the enable has risen past the logic threshold. The 90% measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. [Figure 6-5](#) shows the setup used to measure turn-on time, denoted by the symbol $t_{ON(EN)}$.

Turn-off time is defined as the time taken by the output of the device to fall to 10% after the enable has fallen past the logic threshold. The 10% measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. [Figure 6-5](#) shows the setup used to measure turn-off time, denoted by the symbol $t_{OFF(EN)}$.

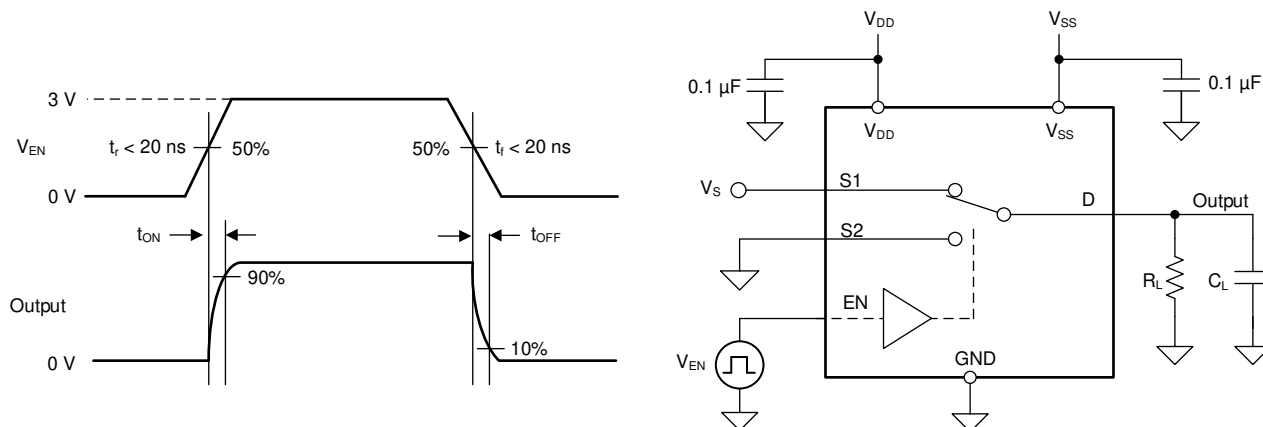


Figure 6-5. Turn-On and Turn-Off Time Measurement Setup

6.6 Break-Before-Make

Break-before-make delay is a safety feature that prevents two inputs from connecting when the device is switching. The output first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the *break* and the *make* is known as break-before-make delay. [Figure 6-6](#) shows the setup used to measure break-before-make delay, denoted by the symbol $t_{OPEN(BBM)}$.

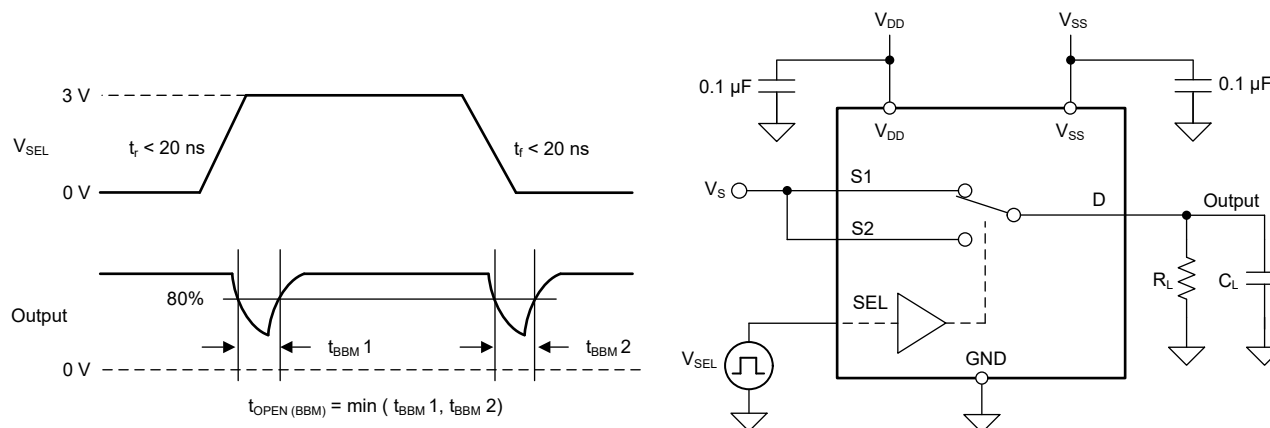


Figure 6-6. Break-Before-Make Delay Measurement Setup

6.7 $t_{ON}(V_{DD})$ Time

The $t_{ON}(V_{DD})$ time is defined as the time taken by the output of the device to rise to 90% after the supply has risen past the supply threshold. The 90% measurement is used to provide the timing of the device turning on in the system. Figure 6-7 shows the setup used to measure turn on time, denoted by the symbol $t_{ON}(V_{DD})$.

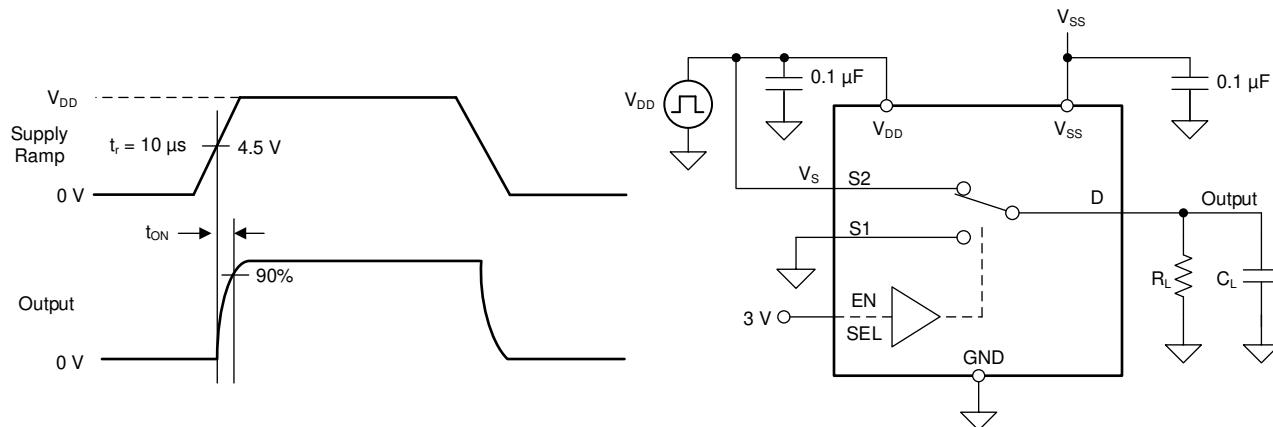


Figure 6-7. $t_{ON}(V_{DD})$ Time Measurement Setup

6.8 Propagation Delay

Propagation delay is defined as the time taken by the output of the device to rise or fall 50% after the input signal has risen or fallen past the 50% threshold. Figure 6-8 shows the setup used to measure propagation delay, denoted by the symbol t_{PD} .

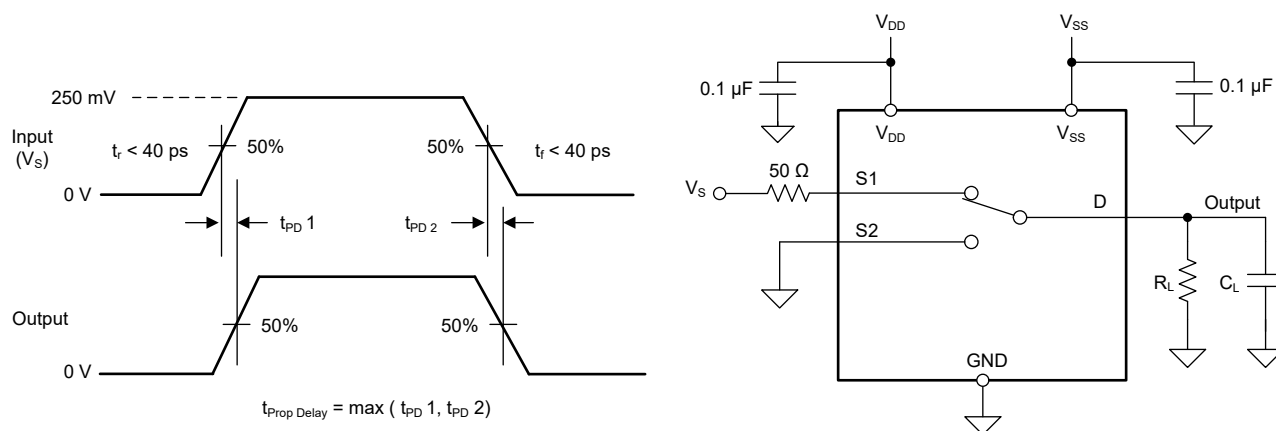
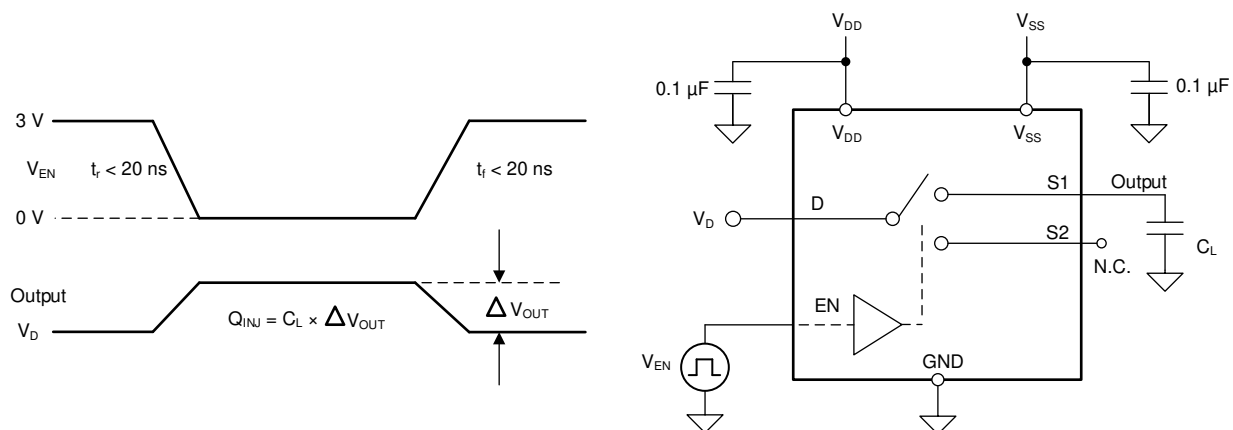


Figure 6-8. Propagation Delay Measurement Setup

6.9 Charge Injection

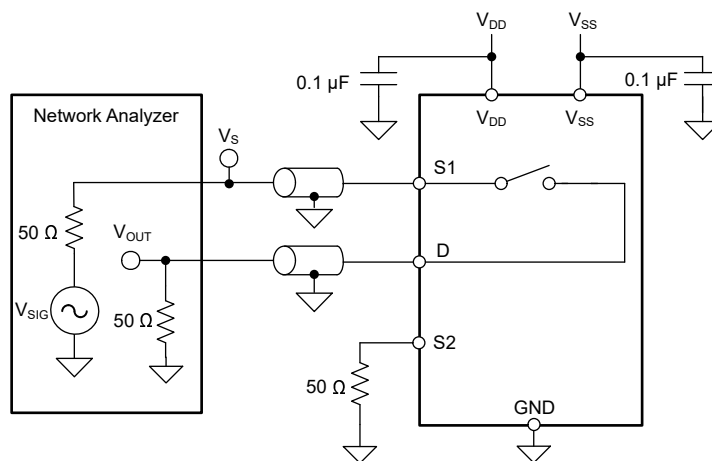
The TMUX7219-Q1 has a transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_C . 6-9 shows the setup used to measure charge injection from source (Sx) to drain (D).



6-9. Charge-Injection Measurement Setup

6.10 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (D) of the device when a signal is applied to the source pin (Sx) of an off-channel. 6-10 shows the setup used to measure, and the equation used to calculate off isolation.



$$\text{Off Isolation} = 20 \times \text{Log} \frac{V_{\text{OUT}}}{V_S}$$

6-10. Off Isolation Measurement Setup

6.11 Crosstalk

Crosstalk is defined as the ratio of the signal at the drain pin (D) of a different channel, when a signal is applied at the source pin (Sx) of an on-channel. [Figure 6-11](#) shows the setup used to measure, and the equation used to calculate crosstalk.

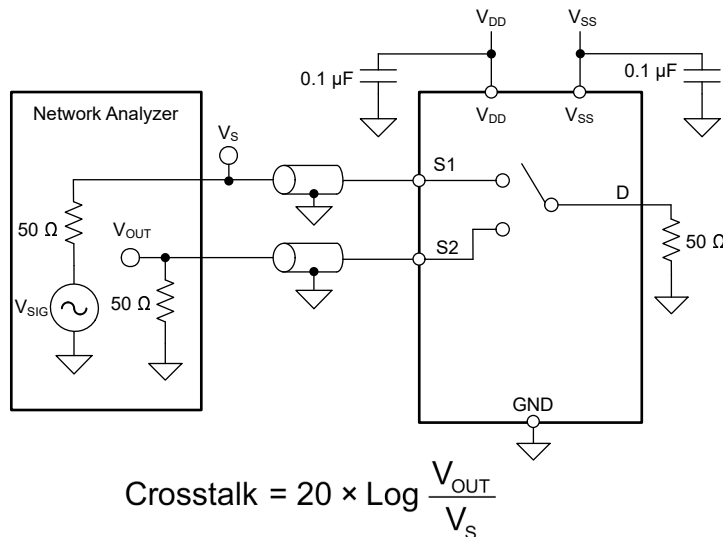


Figure 6-11. Crosstalk Measurement Setup

6.12 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (D) of the device. [Figure 6-12](#) shows the setup used to measure bandwidth.

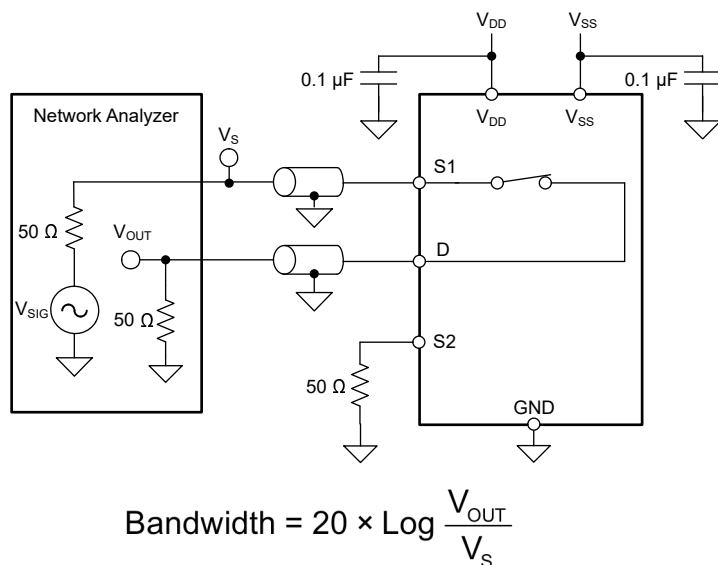


Figure 6-12. Bandwidth Measurement Setup

6.13 THD + Noise

The total harmonic distortion (THD) of a signal is a measurement of the harmonic distortion, and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency at the mux output.

The on-resistance of the device varies with the amplitude of the input signal and results in distortion when the drain pin is connected to a low-impedance load. Total harmonic distortion plus noise is denoted as THD + N.

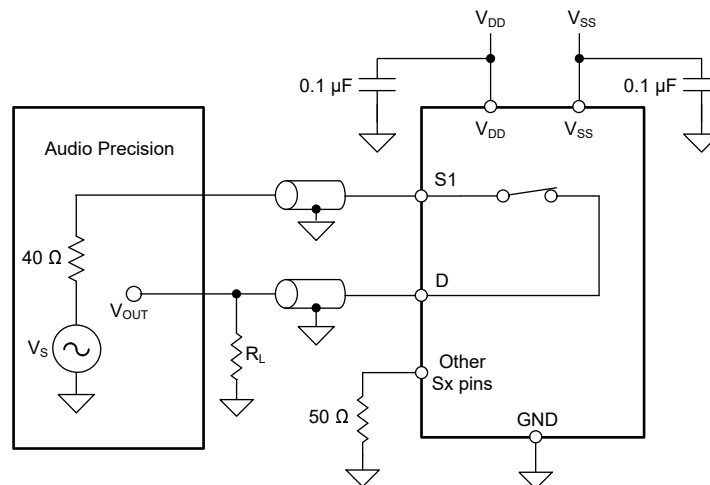
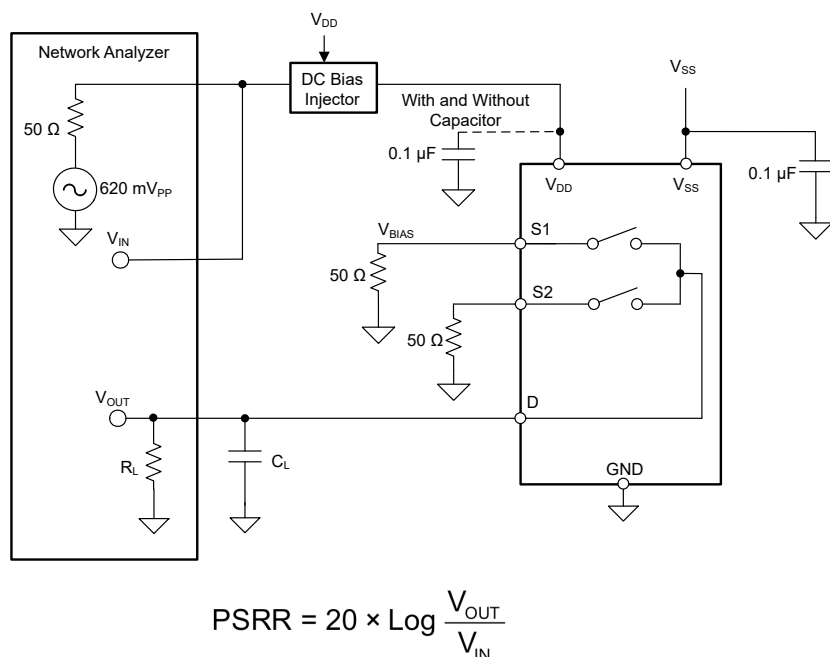


图 6-13. THD + N Measurement Setup

6.14 Power Supply Rejection Ratio (PSRR)

PSRR measures the ability of a device to prevent noise and spurious signals that appear on the supply voltage pin from coupling to the output of the switch. The DC voltage on the device supply is modulated by a sine wave of 620 mV_{PP}. The ratio of the amplitude of signal on the output to the amplitude of the modulated signal is the ACPSRR. A high ratio represents a high degree of tolerance to supply rail variation.

This helps stabilize the supply and immediately filter as much of the supply noise as possible.



6-14. ACPSRR Measurement Setup

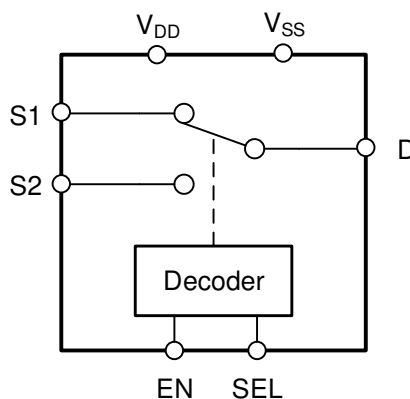
7 Detailed Description

7.1 Overview

The TMUX7219-Q1 is a 2:1, 1-channel switch. Each input is turned on or turned off based on the state of the select line and enable pin.

7.2 Functional Block Diagram

The following figure shows the functional block diagram of the TMUX7219-Q1.



7.3 Feature Description

7.3.1 Bidirectional Operation

The TMUX7219-Q1 conducts equally well from source (Sx) to drain (D) or from drain (D) to source (Sx). Each channel has very similar characteristics in both directions and supports both analog and digital signals.

7.3.2 Rail-to-Rail Operation

The valid signal path input and output voltage for TMUX7219-Q1 ranges from VSS to VDD.

7.3.3 1.8 V Logic Compatible Inputs

The TMUX7219-Q1 has 1.8 V logic compatible control for all logic control inputs. 1.8 V logic level inputs allows the device to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and BOM cost. For more information on 1.8 V logic implementations refer to [Simplifying Design with 1.8 V logic Muxes and Switches](#).

7.3.4 Integrated Pull-Up and Pull-Down Resistor on Logic Pins

The TMUX7219-Q1 has internal weak pull-up and pull-down resistors to GND to ensure the logic pins are not left floating. The value of this pull-down resistor is approximately 4 MΩ, but is clamped to about 1 μA at higher voltages. The EN pin integrates a pull-up resistor to V_{DD} and the SEL pin integrates a pull-down resistor. This feature integrates up to two external components and reduces system size and cost.

7.3.5 Fail-Safe Logic

The TMUX7219-Q1 supports Fail-Safe Logic on the control input pins (EN and SEL) allowing for operation up to 44 V above ground, regardless of the state of the supply pins. This feature allows voltages on the control pins to be applied before the supply pin, protecting the device from potential damage. Fail-Safe Logic minimizes system complexity by removing the need for power supply sequencing on the logic control pins. For example, the Fail-Safe Logic feature allows the logic input pins of the TMUX7219-Q1 to be ramped to +44 V while V_{DD} and $V_{SS} = 0$ V. The logic control inputs are protected against positive faults of up to +44 V in powered-off condition, but do not offer protection against negative overvoltage conditions.

7.3.6 Latch-Up Immune

Latch-up is a condition where a low impedance path is created between a supply pin and ground. This condition is caused by a trigger (current injection or overvoltage), but once activated, the low impedance path remains even after the trigger is no longer present. This low impedance path may cause system upset or catastrophic damage due to excessive current levels. The latch-up condition typically requires a power cycle to eliminate the low impedance path.

The TMUX72xx-Q1 family of devices are constructed on Silicon on Insulator (SOI) based process where an oxide layer is added between the PMOS and NMOS transistor of each CMOS switch to prevent parasitic structures from forming. The oxide layer is also known as an insulating trench and prevents triggering of latch up events due to overvoltage or current injections. The latch-up immunity feature allows the TMUX72xx-Q1 family of switches and multiplexers to be used in harsh environments. For more information on latch-up immunity refer to [Using Latch Up Immune Multiplexers to Help Improve System Reliability](#).

7.3.7 Ultra-Low Charge Injection

Figure 7-1 shows how the TMUX7219-Q1 has a transmission gate topology. Any mismatch in the stray capacitance associated with the NMOS and PMOS causes an output level change whenever the switch is opened or closed.

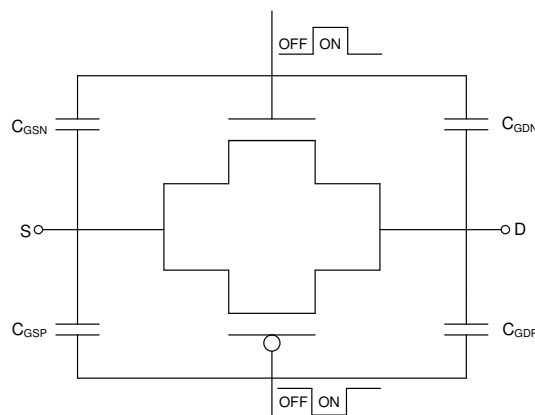
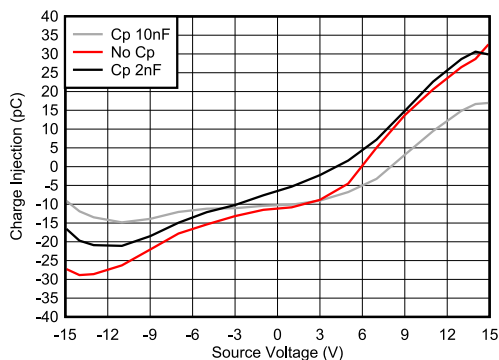


Figure 7-1. Transmission Gate Topology

The TMUX7219-Q1 contains specialized architecture to reduce charge injection on the source (Sx). To further reduce charge injection in a sensitive application, a compensation capacitor (Cp) can be added on the drain (D). This will ensure that excess charge from the switch transition will be pushed into the compensation capacitor on the drain (D) instead of the source (Sx). As a general rule, Cp should be 20× larger than the equivalent load capacitance on the source (Sx). ☒ 7-2 shows charge injection variation with source voltage with different compensation capacitors on the drain side.



☒ 7-2. Charge Injection Compensation

7.4 Device Functional Modes

When the EN pin of the TMUX7219-Q1 is pulled high, one of the switches is closed based on the state of the SEL pin. When the EN pin is pulled low, both of the switches are in an open state regardless of the state of the SEL pin. The control pins can be as high as 44 V.

The TMUX7219-Q1 can operate without any external components except for the supply decoupling capacitors. The EN pin has an internal pull-up resistor of 4 MΩ, and SEL pin has internal pull-down resistor of 4 MΩ. If unused, EN pin must be tied to V_{DD} and SEL pin must be tied to GND to ensure the device does not consume additional current as highlighted in [Implications of Slow or Floating CMOS Inputs](#). Unused signal path inputs (S1, S2, or D) should be connected to GND.

7.5 Truth Tables

表 7-1 show the truth tables for the TMUX7219-Q1.

表 7-1. TMUX7219-Q1 Truth Table

EN	SEL	Selected Source Connected To Drain (D) Pin
0	X ⁽¹⁾	All sources are off (HI-Z)
1	0	S1
1	1	S2

(1) X denotes *do not care*.

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

TMUX7219-Q1 is part of the precision switches and multiplexers family of devices. TMUX7219-Q1 offers low RON, low on and off leakage currents, and ultra-low charge injection performance. These properties make TMUX7219-Q1 ideal for implementing high precision industrial systems requiring selection of one of two inputs or outputs.

8.2 Typical Applications

8.2.1 Data Acquisition Calibration

One application of the TMUX7219-Q1 is in Data Acquisition systems (DAQ). To account for system loss and ensure the lowest possible noise floor, a calibration path is needed. To minimize board space and automate this procedure, many applications utilize a 2:1 (SPDT) switch. 図 8-1 shows the TMUX7219-Q1 configured for switching a calibration path on a precision measurement module.

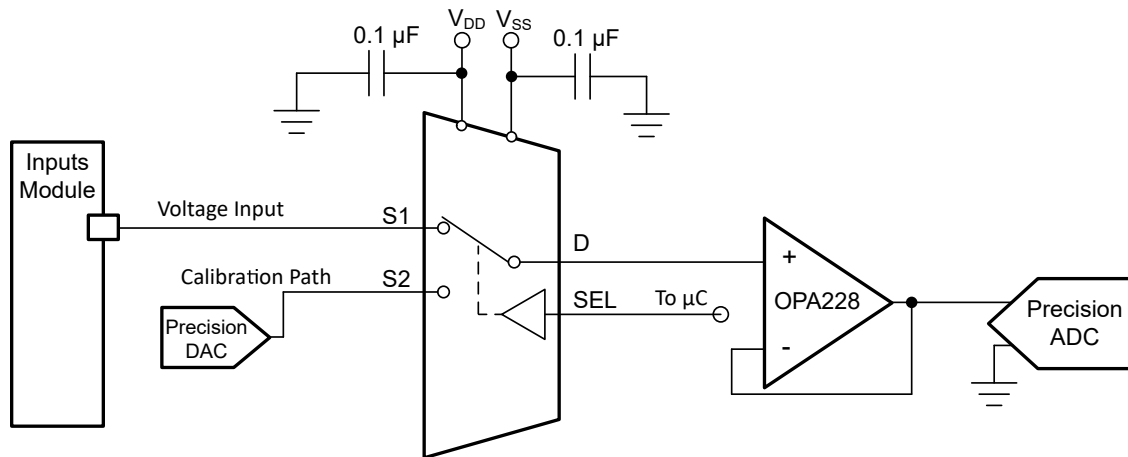


図 8-1. Calibration Path Switching for Data Acquisition

8.2.2 Design Requirements

For the design example, use the parameters listed in 表 8-1.

表 8-1. Design Parameters

PARAMETERS	VALUES
Supply (V _{DD})	12 V
Supply (V _{SS})	-12 V
MUX I/O signal range	-12 V to 12 V (Rail-to-Rail)
Control logic thresholds	1.8 V compatible (up to V _{DD})
EN	EN pulled high to enable the switch

8.2.3 Detailed Design Procedure

The application shown in [図 8-1](#) demonstrates how to generate a $\pm 12\text{V}$ PWM signal that is created by toggling the TMUX7219-Q1. This PWM signal generated by the EVSE on the control pilot line signals to the car the available current of the charger, and the car will respond with a charging status. This handshake results in a safe method for supplying power to vehicle. The TMUX7219-Q1 can support 1.8V logic signals on the control input, allowing the device to interface with low logic controls of an FPGA or MCU. The TMUX7219-Q1 can be operated without any external components except for the supply decoupling capacitors. The select pin has an internal pull-down resistor to prevent floating input logic. All inputs to the switch must fall within the recommend operating conditions of the TMUX7219-Q1 including signal range and continuous current. For this design with a positive supply of 12V on V_{DD} , and negative supply of -12V on V_{SS} , the signal range can be 12V to -12V . The max continuous current (I_{DC}) can be up to 330mA as shown in [セクション 5.4](#) for wide-range current measurement.

8.3 Power Supply Recommendations

The TMUX7219-Q1 operates across a wide supply range of $\pm 4.5\text{ V}$ to $\pm 22\text{ V}$ (4.5 V to 44 V in single-supply mode). The device also performs well with asymmetrical supplies such as $V_{DD} = 12\text{ V}$ and $V_{SS} = -5\text{ V}$.

Power-supply bypassing improves noise margin and prevents switching noise propagation from the supply rails to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1 μF to 10 μF at both the V_{DD} and V_{SS} pins to ground. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground and power planes. Always ensure the ground (GND) connection is established before supplies are ramped.

8.4 Layout

8.4.1 Layout Guidelines

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. [図 8-2](#) shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

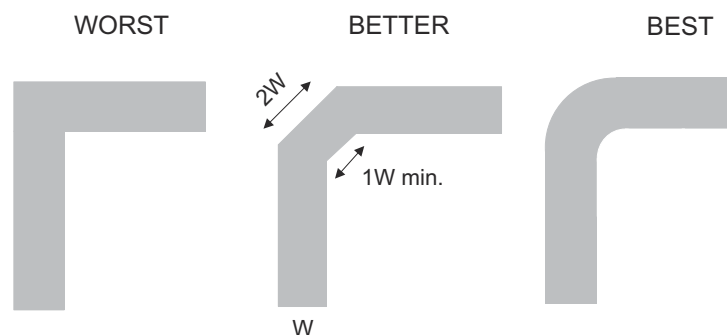


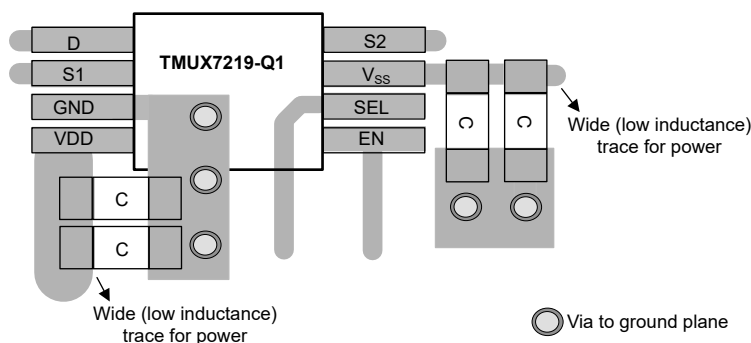
図 8-2. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

☒ 8-3 shows an example of a PCB layout with the TMUX7219-Q1. Some key considerations are as follows:

- For reliable operation, connect a decoupling capacitor ranging from 0.1 μ F to 10 μ F between VDD/VSS and GND. We recommend a 0.1 μ F and 1 μ F capacitor, placing the lowest value capacitor as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the supply voltage.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.
- Using multiple vias in parallel will lower the overall inductance and is beneficial for connection to ground planes.

8.4.2 Layout Example



☒ 8-3. TMUX7219-Q1DGK Layout Example

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Improve Stability Issues with Low CON Multiplexers](#) application brief
- Texas Instruments, [Improving Signal Measurement Accuracy in Automated Test Equipment](#) application brief
- Texas Instruments, [Multiplexers and Signal Switches Glossary](#) application report
- Texas Instruments, [QFN/SON PCB Attachment](#) application report
- Texas Instruments, [Quad Flatpack No-Lead Logic Packages](#) application report
- Texas Instruments, [Simplifying Design with 1.8 V logic Muxes and Switches](#) application brief
- Texas Instruments, [System-Level Protection for High-Voltage Analog Multiplexers](#) application report
- Texas Instruments, [TMUX7219-Q1 Functional Safety, FIT Rate, Failure Mode Distribution and Pin FMA functional safety FIT rate, FMD and Pin-FMA](#)

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの[使用条件](#)を参照してください。

9.4 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

9.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.6 用語集

テキサス・インスツルメンツ用語集

この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (July 2024) to Revision C (December 2024)	Page
• データシート全体で RQX パッケージへのすべての言及を削除.....	1
• Added the <i>Integrated Pull-Down Resistor on Logic Pins</i> section.....	28

Changes from Revision A (June 2021) to Revision B (July 2024)	Page
• Updated IIH specification.....	6

Changes from Revision * (January 2021) to Revision A (June 2021)	Page
• データシートのステータスを以下のように変更:「事前情報」から「量産データ」	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMUX7219DGKRQ1	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(X219, X219Q) Q
TMUX7219DGKRQ1.B	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(X219, X219Q) Q

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TMUX7219-Q1 :

- Catalog : [TMUX7219](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUX7219DGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUX7219DGKRQ1	VSSOP	DGK	8	2500	353.0	353.0	32.0

DGK0008A**PACKAGE OUTLINE****VSSOP - 1.1 mm max height**

SMALL OUTLINE PACKAGE



4214862/A 04/2023

NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、[テキサス・インスツルメンツの販売条件](#)、または [ti.com](https://www.ti.com) やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用される テキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated