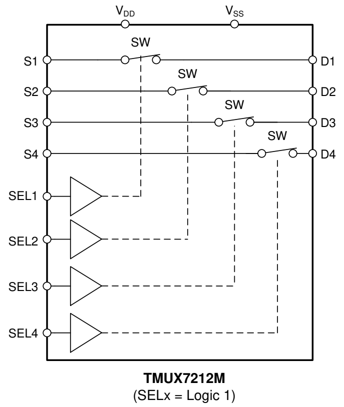
TMUX7212M 44 V 低 RON、1:1 (SPST)、4 チャネル高精度スイッチ、ラッチアップ フリー、1.8V ロジック

1 特長

- ラッチアップ耐性
- デュアル電源電圧範囲：±4.5V ~ ±22 V
- 単電源電圧範囲：4.5V ~ 44 V
- -55℃ ~ +125℃の動作温度範囲
- 低いオン抵抗：2Ω
- 大電流のサポート：220mA (最大値)
- 1.8V ロジック互換
- ロジック ピンにプルダウン抵抗を内蔵
- フェイルセーフ ロジック
- レール ツー レール動作
- 双方向動作

2 アプリケーション

- 航空用フライト コントロール ユニット
- 航空機のコックピット ディスプレイ
- スタンドアロンの航空用高精度フライト コントロール
- インターコネクト ディストリビューション ボックス
- 航空宇宙および防衛



TMUX7212M ブロック図

3 概要

TMUX7212M は、独立して選択できる 4 つの 1：1 単極単投 (SPST) スイッチ チャネルを備えた相補型金属酸化膜半導体 (CMOS) スイッチです。これらのデバイスは、単一電源 (4.5V ~ 44 V)、デュアル電源 (±4.5V ~ ±22 V)、または非対称電源(V_{DD} = 12V、V_{SS} = -5V など) で動作します。TMUX7212M は、ソース (Sx) およびドレイン (Dx) ピンで、V_{SS} から V_{DD} までの範囲の双方向アナログおよびデジタル信号をサポートします。

TMUX7212M の各スイッチは、SELx ピンで適切なロジック制御入力を使用して制御します。TMUX7212M は高精度スイッチおよびマルチプレクサ デバイス ファミリの製品であり、オンおよびオフ時のリーク電流が非常に小さいため、高精度の測定用途に使用できます。

TMUX7212M ファミリはラッチアップ フリーであるため、過電圧イベントによってよく発生するデバイス内の寄生構造間の好ましくない大電流イベントを防止できます。ラッチアップ状態は通常、電源レールがオフにされるまで継続するため、デバイスの故障の原因となる場合があります。このラッチアップ フリーという特長により、TMUX7212M スイッチおよびマルチプレクサ ファミリは過酷な環境でも使用できます。さらに、TMUX7212M は、最低 -55℃までの拡張温度範囲での使用が定格内であるため、過酷な産業用および航空宇宙のアプリケーションの優れた選択肢です。

パッケージ情報

部品番号(1)	パッケージ (2)	パッケージ サイズ(3)
TMUX7212M	PW (TSSOP、16)	5mm × 6.4mm

(1) セクション 4 を参照
(2) 詳細については、セクション 12 を参照してください。
(3) パッケージ サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。

English Data Sheet: SCDS456

Table of Contents

4 Device Comparison Table

PRODUCT	DESCRIPTION
TMUX7212M	Low-Leakage-Current, Precision, 4-Channel, 1:1 (SPST) Switches (Logic High)

5 Pin Configuration and Functions

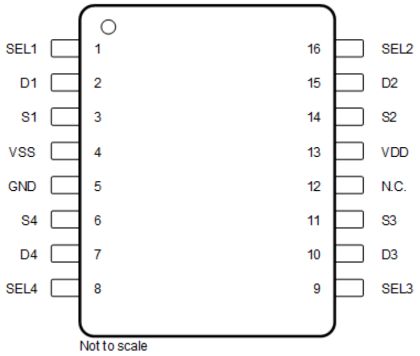


図 5-1. PW Package 16-Pin TSSOP (Top View)

表 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION[2]
NAME	NO.		
D1	2	I/O	Drain pin 1. Can be an input or output.
D2	15	I/O	Drain pin 2. Can be an input or output.
D3	10	I/O	Drain pin 3. Can be an input or output.
D4	7	I/O	Drain pin 4. Can be an input or output.
GND	5	P	Ground (0V) reference
N.C.	12	—	No internal connection. Can be shorted to GND or left floating.
S1	3	I/O	Source pin 1. Can be an input or output.
S2	14	I/O	Source pin 2. Can be an input or output.
S3	11	I/O	Source pin 3. Can be an input or output.
S4	6	I/O	Source pin 4. Can be an input or output.
SEL1	1	I	Logic control input 1, has internal 4MΩ pull-down resistor. Controls channel 1 state as shown in セクション 8.5.
SEL2	16	I	Logic control input 2, has internal 4MΩ pull-down resistor. Controls channel 2 state as shown in セクション 8.5.
SEL3	9	I	Logic control input 3, has internal 4MΩ pull-down resistor. Controls channel 3 state as shown in セクション 8.5.
SEL4	8	I	Logic control input 4, has internal 4MΩ pull-down resistor. Controls channel 4 state as shown in セクション 8.5.
VDD	13	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1µF to 10µF between V_{DD} and GND.
VSS	4	P	Negative power supply. This pin is the most negative power-supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 0.1µF to 10µF between V_{SS} and GND.

(1) I = input, O = output, I/O = input and output, P = power.
(2) Refer to セクション 8.4 for what to do with unused pins.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
$V_{DD} - V_{SS}$	Supply voltage		48	V
V_{DD}		–0.5	48	V
V_{SS}		–48	0.5	V
V_{SEL} or V_{EN}	Logic control input pin voltage (SELx)	–0.5	48	V
I_{SEL} or I_{EN}	Logic control input pin current (SELx)	–30	30	mA
V_S or V_D	Source or drain voltage (Sx, Dx)	V_{SS}–0.5	V_{DD}+0.5	V
I_{IK}	Diode clamp current(3)	–30	30	mA
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (Sx, Dx)		I_{DC} + 10 %(4)	mA
T_A	Ambient temperature	–55	150	°C
T_{stg}	Storage temperature	–65	150	°C
T_J	Junction temperature		150	°C
P_{tot}	Total power dissipation (QFN)(5)		1650	mW
	Total power dissipation (TSSOP)(5)		700	mW

(1) Operation outside the *Absolute Maximum Rating* may cause permanent device damage. *Absolute Maximum Rating* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Condition*. If used outside the *Recommended Operating Condition* but within the *Absolute Maximum Rating*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) Pins are diode-clamped to the power-supply rails. Over voltage signals must be voltage and current limited to maximum ratings.
(4) Refer to *Source or Drain Continuous Current* table for I_{DC} specifications.
(5) For QFN package: P_{tot} derates linearly above T_A = 70°C by 24.2mW/°C.
For TSSOP package: P_{tot} = 700 mW (max) and derates linearly above T_A = 70°C by 10.7mW/°C.

6.2 ESD Ratings

			VALUE	UNIT
TMUX7212				
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1500	V
		Charged device model (CDM), per JEDEC JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Thermal Information

THERMAL METRIC(1)		TMUX7212	UNIT
		PW (TSSOP)	
		16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	94.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	25.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	41.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	40.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{DD} – V_{SS}$ (1)	Power supply voltage differential	4.5		44	V
V_{DD}	Positive power supply voltage	4.5		44	V
V_S or V_D	Signal path input/output voltage (source or drain pin) (Sx, D)	V_{SS}		V_{DD}	V
V_{SEL} or V_{EN}	Address or enable pin voltage	0		44	V
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (Sx, D)			I_{DC} (2)	mA
T_A	Ambient temperature	–55		125	°C

(1) V_{DD} and V_{SS} can be any value as long as 4.5V ≤ ($V_{DD} – V_{SS}$) ≤ 44 V, and the minimum V_{DD} is met.
(2) Refer to *Source or Drain Continuous Current* table for I_{DC} specifications.

6.5 Source or Drain Continuous Current

at supply voltage of V_{DD} ± 10%, V_{SS} ± 10 % (unless otherwise noted)

CONTINUOUS CURRENT PER CHANNEL (I_{DC}) (2)		T_A = 25°C	T_A = 85°C	T_A = 125°C	UNIT
PACKAGE	TEST CONDITIONS				
PW (TSSOP)	+44 V Dual Supply(1)	220	160	100	mA
	±15 V Dual Supply	220	160	100	mA
	+12 V Single Supply	190	130	90	mA
	±5V Dual Supply	170	120	80	mA
	+5V Single Supply	130	90	60	mA

(1) Specified for nominal supply voltage only.
(2) Refer to Total power dissipation (P_{tot}) limits in *Absolute Maximum Ratings* table that must be followed with maximum continuous current specification.

±15 V Dual Supply: Electrical Characteristics

V_{DD} = +15 V ± 10%, V_{SS} = –15 V ±10%, GND = 0V (unless otherwise noted)
Typical at V_{DD} = +15 V, V_{SS} = –15 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = –10 V to +10 V I_D = –10mA Refer to On-Resistance	25°C		2	2.7	Ω
			–40°C to +85°C			3.4	Ω
			–55°C to +125°C			4	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = –10 V to +10 V I_D = –10mA Refer to On-Resistance	25°C		0.1	0.18	Ω
			–40°C to +85°C			0.19	Ω
			–55°C to +125°C			0.21	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = –10 V to +10 V I_S = –10mA Refer to On-Resistance	25°C		0.2	0.46	Ω
			–40°C to +85°C			0.65	Ω
			–55°C to +125°C			0.7	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0V, I_S = –10mA Refer to On-Resistance	–55°C to +125°C		0.008		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 16.5V, V_{SS} = –16.5V Switch state is off V_S = +10 V / –10 V V_D = –10 V / + 10 V Refer to Off-Leakage Current	25°C	–0.25	0.05	0.25	nA
			–40°C to +85°C	–3		3	nA
			–55°C to +125°C	–20		20	nA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 16.5V, V_{SS} = –16.5V Switch state is off V_S = +10 V / –10 V V_D = –10 V / + 10 V Refer to Off-Leakage Current	25°C	–0.25	0.05	0.25	nA
			–40°C to +85°C	–3		3	nA
			–55°C to +125°C	–20		20	nA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	V_{DD} = 16.5V, V_{SS} = –16.5V Switch state is on V_S = V_D = ±10 V Refer to On-Leakage Current	25°C	–0.4	0.1	0.4	nA
			–40°C to +85°C	–1		1	nA
			–55°C to +125°C	–3		3	nA
LOGIC INPUTS (SEL / EN pins)							
V_{IH}	Logic voltage high		–55°C to +125°C	1.3		44	V
V_{IL}	Logic voltage low		–55°C to +125°C	0		0.8	V
I_{IH}	Input leakage current		–55°C to +125°C		0.4	1.2	µA
I_{IL}	Input leakage current		–55°C to +125°C	–0.1	–0.005		µA
C_{IN}	Logic input capacitance		–55°C to +125°C		3.5		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 16.5V, V_{SS} = –16.5V Logic inputs = 0V, 5V, or V_{DD}	25°C		35	56	µA
			–40°C to +85°C			65	µA
			–55°C to +125°C			80	µA
I_{SS}	V_{SS} supply current	V_{DD} = 16.5V, V_{SS} = –16.5V Logic inputs = 0V, 5V, or V_{DD}	25°C		5	20	µA
			–40°C to +85°C			24	µA
			–55°C to +125°C			35	µA

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

±15 V Dual Supply: Switching Characteristics

V_{DD} = +15 V ± 10%, V_{SS} = –15 V ± 10%, GND = 0V (unless otherwise noted)
Typical at V_{DD} = +15 V, V_{SS} = –15 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{ON}	Turn-on time from control input	V_S = 10 V R_L = 300 Ω, C_L = 35pF Refer to Turn-on and Turn-off Time	25°C		100	175	ns
			–40°C to +85°C			205	ns
			–55°C to +125°C			225	ns
t_{OFF}	Turn-off time from control input	V_S = 10 V R_L = 300 Ω, C_L = 35pF Refer to Turn-on and Turn-off Time	25°C		80	205	ns
			–40°C to +85°C			225	ns
			–55°C to +125°C			240	ns
$t_{ON\ (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 1 µs R_L = 300 Ω, C_L = 35pF Refer to Turn-on (VDD) Time	25°C		0.17		ms
			–40°C to +85°C		0.18		ms
			–55°C to +125°C		0.18		ms
t_{PD}	Propagation delay	R_L = 50 Ω , C_L = 5pF Refer to Propagation Delay	25°C		260		ps
Q_{INJ}	Charge injection	V_S = 0V, C_L = 100pF Refer to Charge Injection	25°C		60		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5pF V_S = 0V, f = 100kHz Refer to Off Isolation	25°C		–70		dB
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5pF V_S = 0V, f = 1MHz Refer to Off Isolation	25°C		–50		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5pF V_S = 0V, f = 100kHz Refer to Crosstalk	25°C		–114		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5pF V_S = 0V, f = 1MHz Refer to Crosstalk	25°C		–93		dB
BW	–3dB Bandwidth	R_L = 50 Ω , C_L = 5pF V_S = 0V Refer to Bandwidth	25°C		56		MHz
I_L	Insertion loss	R_L = 50 Ω , C_L = 5pF V_S = 0V, f = 1MHz	25°C		–0.15		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50 Ω , C_L = 5pF, f = 1MHz Refer to ACPSRR	25°C		–68		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 15 V, V_{BIAS} = 0V R_L = 10kΩ , C_L = 5pF, f = 20Hz to 20kHz Refer to THD + Noise	25°C		0.0004		%
$C_{S(OFF)}$	Source off capacitance	V_S = 0V, f = 1MHz	25°C		28		pF
$C_{D(OFF)}$	Drain off capacitance	V_S = 0V, f = 1MHz	25°C		45		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance	V_S = 0V, f = 1MHz	25°C		145		pF

±20 V Dual Supply: Electrical Characteristics

V_{DD} = +20 V ± 10%, V_{SS} = –20 V ±10%, GND = 0V (unless otherwise noted)
Typical at V_{DD} = +20 V, V_{SS} = –20 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = –15 V to +15 V I_D = –10mA Refer to On-Resistance	25°C		1.7	2.5	Ω
			–40°C to +85°C			3	Ω
			–55°C to +125°C			3.6	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = –15 V to +15 V I_D = –10mA Refer to On-Resistance	25°C		0.1	0.18	Ω
			–40°C to +85°C			0.19	Ω
			–55°C to +125°C			0.21	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = –15 V to +15 V I_S = –10mA Refer to On-Resistance	25°C		0.3	0.6	Ω
			–40°C to +85°C			0.8	Ω
			–55°C to +125°C			0.95	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0V, I_S = –10mA Refer to On-Resistance	–55°C to +125°C		0.008		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 22 V, V_{SS} = –22 V Switch state is off V_S = +15 V / –15 V V_D = –15 V / + 15 V Refer to Off-Leakage Current	25°C	–1	0.05	1	nA
			–40°C to +85°C	–4.5		4.5	nA
			–55°C to +125°C	–33		33	nA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 22 V, V_{SS} = –22 V Switch state is off V_S = +15 V / –15 V V_D = –15 V / + 15 V Refer to Off-Leakage Current	25°C	–1	0.1	1	nA
			–40°C to +85°C	–4.5		4.5	nA
			–55°C to +125°C	–33		33	nA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	V_{DD} = 22 V, V_{SS} = –22 V Switch state is on V_S = V_D = ±15 V Refer to On-Leakage Current	25°C	–1	0.1	1	nA
			–40°C to +85°C	–1.5		1.5	nA
			–55°C to +125°C	–8		8	nA
LOGIC INPUTS (SEL / EN pins)							
V_{IH}	Logic voltage high		–55°C to +125°C	1.3		44	V
V_{IL}	Logic voltage low		–55°C to +125°C	0		0.8	V
I_{IH}	Input leakage current		–55°C to +125°C		0.4	1.2	µA
I_{IL}	Input leakage current		–55°C to +125°C	–0.1	–0.005		µA
C_{IN}	Logic input capacitance		–55°C to +125°C		3.5		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 22 V, V_{SS} = –22 V Logic inputs = 0V, 5V, or V_{DD}	25°C		33	65	µA
			–40°C to +85°C			74	µA
			–55°C to +125°C			90	µA
I_{SS}	V_{SS} supply current	V_{DD} = 22 V, V_{SS} = –22 V Logic inputs = 0V, 5V, or V_{DD}	25°C		7	26	µA
			–40°C to +85°C			30	µA
			–55°C to +125°C			45	µA

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

±20 V Dual Supply: Switching Characteristics

V_{DD} = +20 V ± 10%, V_{SS} = –20 V ±10%, GND = 0V (unless otherwise noted)
Typical at V_{DD} = +20 V, V_{SS} = –20 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{ON}	Turn-on time from control input	V_S = 10 V R_L = 300 Ω, C_L = 35pF Refer to Turn-on and Turn-off Time	25°C		100	185	ns
			–40°C to +85°C			210	ns
			–55°C to +125°C			230	ns
t_{OFF}	Turn-off time from control input	V_S = 10 V R_L = 300 Ω, C_L = 35pF Refer to Turn-on and Turn-off Time	25°C		90	210	ns
			–40°C to +85°C			225	ns
			–55°C to +125°C			235	ns
$t_{ON (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 1 µs R_L = 300 Ω, C_L = 35pF Refer to Turn-on (VDD) Time	25°C		0.17		ms
			–40°C to +85°C		0.18		ms
			–55°C to +125°C		0.18		ms
t_{PD}	Propagation delay	R_L = 50 Ω , C_L = 5pF Refer to Propagation Delay	25°C		260		ps
Q_{INJ}	Charge injection	V_S = 0V, C_L = 100pF Refer to Charge Injection	25°C		92		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5pF V_S = 0V, f = 100kHz Refer to Off Isolation	25°C		–70		dB
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5pF V_S = 0V, f = 1MHz Refer to Off Isolation	25°C		–50		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5pF V_S = 0V, f = 100kHz Refer to Crosstalk	25°C		–112		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5pF V_S = 0V, f = 1MHz Refer to Crosstalk	25°C		–93		dB
BW	–3dB Bandwidth	R_L = 50 Ω , C_L = 5pF V_S = 0V Refer to Bandwidth	25°C		48		MHz
I_L	Insertion loss	R_L = 50 Ω , C_L = 5pF V_S = 0V, f = 1MHz	25°C		–0.14		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50 Ω , C_L = 5pF, f = 1MHz Refer to ACPSRR	25°C		–68		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 20 V, V_{BIAS} = 0V R_L = 10kΩ , C_L = 5pF, f = 20Hz to 20kHz Refer to THD + Noise	25°C		0.0003		%
$C_{S(OFF)}$	Source off capacitance	V_S = 0V, f = 1MHz	25°C		28		pF
$C_{D(OFF)}$	Drain off capacitance	V_S = 0V, f = 1MHz	25°C		45		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance	V_S = 0V, f = 1MHz	25°C		145		pF

44 V Single Supply: Electrical Characteristics

V_{DD} = +44 V, V_{SS} = 0V, GND = 0V (unless otherwise noted)
Typical at V_{DD} = +44 V, V_{SS} = 0V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0V to 40 V I_D = –10mA Refer to On-Resistance	25°C		2	2.4	Ω
			–40°C to +85°C			3.2	Ω
			–55°C to +125°C			3.8	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = 0V to 40 V I_D = –10mA Refer to On-Resistance	25°C		0.1	0.18	Ω
			–40°C to +85°C			0.19	Ω
			–55°C to +125°C			0.21	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = 0V to 40 V I_D = –10mA Refer to On-Resistance	25°C		0.65	0.8	Ω
			–40°C to +85°C			1.1	Ω
			–55°C to +125°C			1.2	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 22 V, I_S = –10mA Refer to On-Resistance	–55°C to +125°C		0.007		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 44 V, V_{SS} = 0V Switch state is off V_S = 40 V / 1V V_D = 1V / 40 V Refer to Off-Leakage Current	25°C	–1	0.05	1	nA
			–40°C to +85°C	–7		7	nA
			–55°C to +125°C	–50		50	nA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 44 V, V_{SS} = 0V Switch state is off V_S = 40 V / 1V V_D = 1V / 40 V Refer to Off-Leakage Current	25°C	–1	0.05	1	nA
			–40°C to +85°C	–7		7	nA
			–55°C to +125°C	–50		50	nA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	V_{DD} = 44 V, V_{SS} = 0V Switch state is on V_S = V_D = 40 V or 1V Refer to On-Leakage Current	25°C	–1	0.05	1	nA
			–40°C to +85°C	–3.5		3.5	nA
			–55°C to +125°C	–5		5	nA
LOGIC INPUTS (SEL / EN pins)							
V_{IH}	Logic voltage high		–55°C to +125°C	1.3		44	V
V_{IL}	Logic voltage low		–55°C to +125°C	0		0.8	V
I_{IH}	Input leakage current		–55°C to +125°C		0.6	1.2	µA
I_{IL}	Input leakage current		–55°C to +125°C	–0.1	–0.005		µA
C_{IN}	Logic input capacitance		–55°C to +125°C		3.5		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 44 V, V_{SS} = 0V Logic inputs = 0V, 5V, or V_{DD}	25°C		44	79	µA
			–40°C to +85°C			88	µA
			–55°C to +125°C			105	µA

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

44 V Single Supply: Switching Characteristics

V_{DD} = +44 V, V_{SS} = 0V, GND = 0V (unless otherwise noted)
Typical at V_{DD} = +44 V, V_{SS} = 0V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{ON}	Turn-on time from control input	V_S = 18 V R_L = 300 Ω, C_L = 35pF Refer to Turn-on and Turn-off Time	25°C		80	185	ns
			–40°C to +85°C			205	ns
			–55°C to +125°C			225	ns
t_{OFF}	Turn-off time from control input	V_S = 18 V R_L = 300 Ω, C_L = 35pF Refer to Turn-on and Turn-off Time	25°C		90	205	ns
			–40°C to +85°C			220	ns
			–55°C to +125°C			228	ns
$t_{ON\ (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 1 µs R_L = 300 Ω, C_L = 35pF Refer to Turn-on (VDD) Time	25°C		0.14		ms
			–40°C to +85°C		0.15		ms
			–55°C to +125°C		0.15		ms
t_{PD}	Propagation delay	R_L = 50 Ω , C_L = 5pF Refer to Propagation Delay	25°C		270		ps
Q_{INJ}	Charge injection	V_S = 22 V, C_L = 100pF Refer to Charge Injection	25°C		104		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5pF V_S = 6V, f = 100kHz Refer to Off Isolation	25°C		–70		dB
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5pF V_S = 6V, f = 1MHz Refer to Off Isolation	25°C		–50		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5pF V_S = 6V, f = 100kHz Refer to Crosstalk	25°C		–112		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5pF V_S = 6V, f = 1MHz Refer to Crosstalk	25°C		–93		dB
BW	–3dB Bandwidth	R_L = 50 Ω , C_L = 5pF V_S = 6V Refer to Bandwidth	25°C		46		MHz
I_L	Insertion loss	R_L = 50 Ω , C_L = 5pF V_S = 6V, f = 1MHz	25°C		–0.15		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50 Ω , C_L = 5pF, f = 1MHz Refer to ACPSRR	25°C		–66		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 22 V, V_{BIAS} = 22 V R_L = 10kΩ , C_L = 5pF, f = 20Hz to 20kHz Refer to THD + Noise	25°C		0.0003		%
$C_{S(OFF)}$	Source off capacitance	V_S = 22 V, f = 1MHz	25°C		28		pF
$C_{D(OFF)}$	Drain off capacitance	V_S = 22 V, f = 1MHz	25°C		45		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance	V_S = 22 V, f = 1MHz	25°C		145		pF

12 V Single Supply: Electrical Characteristics

V_{DD} = +12 V ± 10%, V_{SS} = 0V, GND = 0V (unless otherwise noted)
Typical at V_{DD} = +12 V, V_{SS} = 0V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0V to 10 V I_D = –10mA Refer to On-Resistance	25°C		2.8	5.4	Ω
			–40°C to +85°C			6.8	Ω
			–55°C to +125°C			7.4	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = 0V to 10 V I_D = –10mA Refer to On-Resistance	25°C		0.13	0.21	Ω
			–40°C to +85°C			0.23	Ω
			–55°C to +125°C			0.25	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = 0V to 10 V I_S = –10mA Refer to On-Resistance	25°C		1	1.7	Ω
			–40°C to +85°C			1.9	Ω
			–55°C to +125°C			2	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 6V, I_S = –10mA Refer to On-Resistance	–55°C to +125°C		0.015		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 13.2V, V_{SS} = 0V Switch state is off V_S = 10 V / 1V V_D = 1V / 10 V Refer to Off-Leakage Current	25°C	–0.25	0.01	0.25	nA
			–40°C to +85°C	–2		2	nA
			–55°C to +125°C	–16		16	nA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 13.2V, V_{SS} = 0V Switch state is off V_S = 10 V / 1V V_D = 1V / 10 V Refer to Off-Leakage Current	25°C	–0.25	0.05	0.25	nA
			–40°C to +85°C	–2		2	nA
			–55°C to +125°C	–16		16	nA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	V_{DD} = 13.2V, V_{SS} = 0V Switch state is on V_S = V_D = 10 V or 1V Refer to On-Leakage Current	25°C	–0.5	0.05	0.5	nA
			–40°C to +85°C	–1		1	nA
			–55°C to +125°C	–3		3	nA
LOGIC INPUTS (SEL / EN pins)							
V_{IH}	Logic voltage high		–55°C to +125°C	1.3		44	V
V_{IL}	Logic voltage low		–55°C to +125°C	0		0.8	V
I_{IH}	Input leakage current		–55°C to +125°C		0.4	1.2	μA
I_{IL}	Input leakage current		–55°C to +125°C	–0.1	–0.005		μA
C_{IN}	Logic input capacitance		–55°C to +125°C		3.5		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 13.2V, V_{SS} = 0V Logic inputs = 0V, 5V, or V_{DD}	25°C		30	44	μA
			–40°C to +85°C			52	μA
			–55°C to +125°C			62	μA

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

12 V Single Supply: Switching Characteristics

V_{DD} = +12 V ± 10%, V_{SS} = 0V, GND = 0V (unless otherwise noted)
Typical at V_{DD} = +12 V, V_{SS} = 0V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{ON}	Turn-on time from control input	V_S = 8V R_L = 300 Ω, C_L = 35pF Refer to Turn-on and Turn-off Time	25°C		170	225	ns
			–40°C to +85°C			276	ns
			–55°C to +125°C			315	ns
t_{OFF}	Turn-off time from control input	V_S = 8V R_L = 300 Ω, C_L = 35pF Refer to Turn-on and Turn-off Time	25°C		75	248	ns
			–40°C to +85°C			285	ns
			–55°C to +125°C			310	ns
$t_{ON\ (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 1 µs R_L = 300 Ω, C_L = 35pF Refer to Turn-on (VDD) Time	25°C		0.17		ms
			–40°C to +85°C		0.18		ms
			–55°C to +125°C		0.18		ms
t_{PD}	Propagation delay	R_L = 50 Ω , C_L = 5pF Refer to Propagation Delay	25°C		270		ps
Q_{INJ}	Charge injection	V_S = 6V, C_L = 100pF Refer to Charge Injection	25°C		12		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5pF V_S = 6V, f = 100kHz Refer to Off Isolation	25°C		–70		dB
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5pF V_S = 6V, f = 1MHz Refer to Off Isolation	25°C		–50		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5pF V_S = 6V, f = 100kHz Refer to Crosstalk	25°C		–112		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5pF V_S = 6V, f = 1MHz Refer to Crosstalk	25°C		–93		dB
BW	–3dB Bandwidth	R_L = 50 Ω , C_L = 5pF V_S = 6V Refer to Bandwidth	25°C		125		MHz
I_L	Insertion loss	R_L = 50 Ω , C_L = 5pF V_S = 6V, f = 1MHz	25°C		–0.25		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50 Ω , C_L = 5pF, f = 1MHz Refer to ACPSRR	25°C		–70		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 6V, V_{BIAS} = 6V R_L = 10kΩ , C_L = 5pF, f = 20Hz to 20kHz Refer to THD + Noise	25°C		0.001		%
$C_{S(OFF)}$	Source off capacitance	V_S = 6V, f = 1MHz	25°C		35		pF
$C_{D(OFF)}$	Drain off capacitance	V_S = 6V, f = 1MHz	25°C		50		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance	V_S = 6V, f = 1MHz	25°C		145		pF

6.6 Typical Characteristics

at T_A = 25°C (unless otherwise noted)

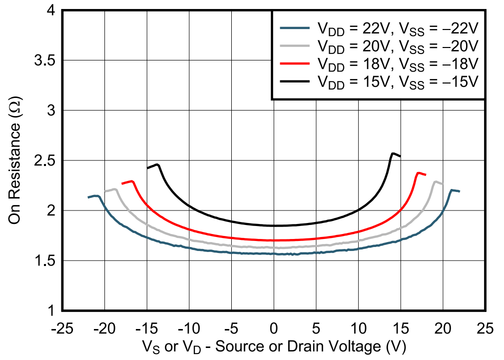


図 6-1. On-Resistance vs. Source or Drain Voltage – Dual Supply

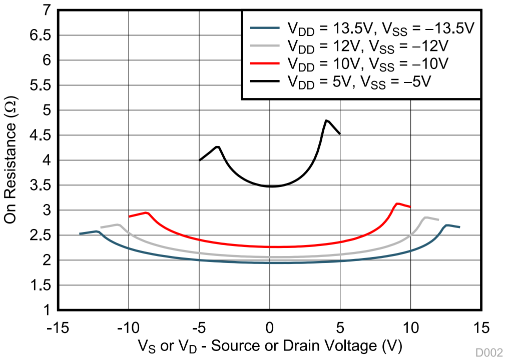


図 6-2. On-Resistance vs. Source or Drain Voltage – Dual Supply

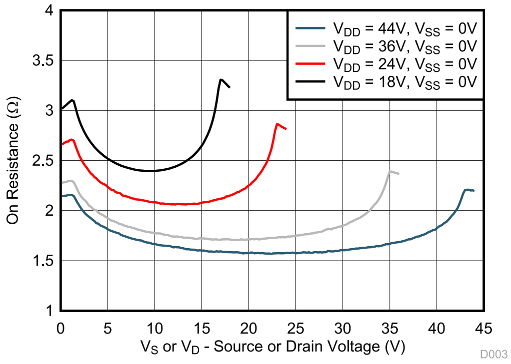


図 6-3. On-Resistance vs. Source or Drain Voltage – Single Supply

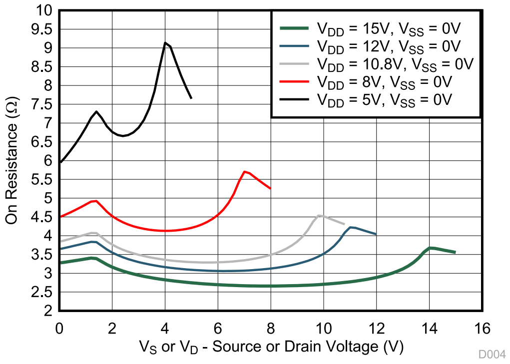
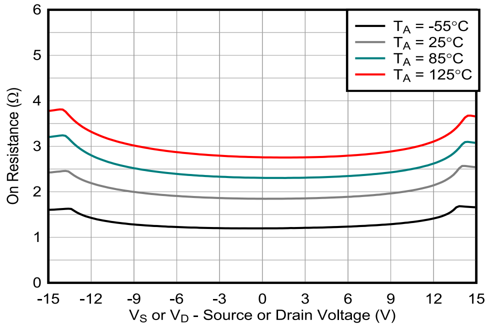
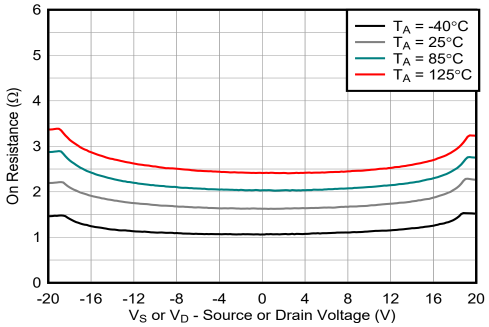


図 6-4. On-Resistance vs. Source or Drain Voltage – Single Supply



V_{DD} = 15 V, V_{SS} = -15 V

図 6-5. On-Resistance vs Temperature

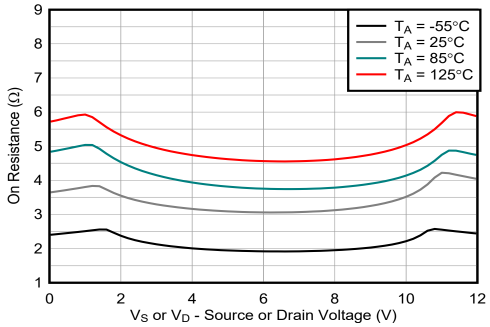


V_{DD} = 20 V, V_{SS} = -20 V

図 6-6. On-Resistance vs Temperature

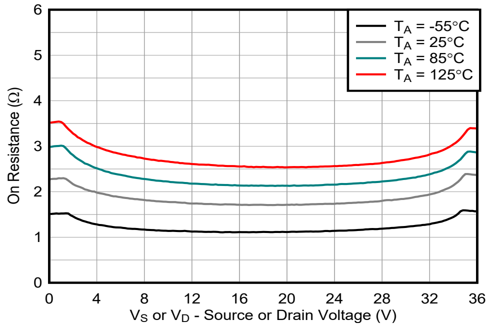
6.6 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)



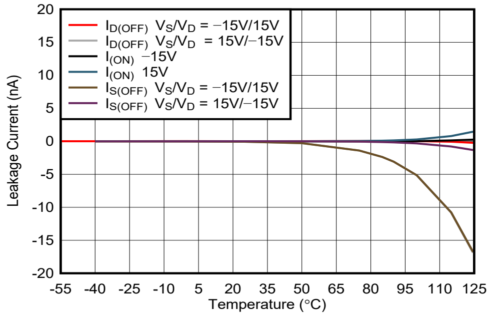
V_{DD} = 12 V, V_{SS} = 0V

図 6-7. On-Resistance vs Temperature



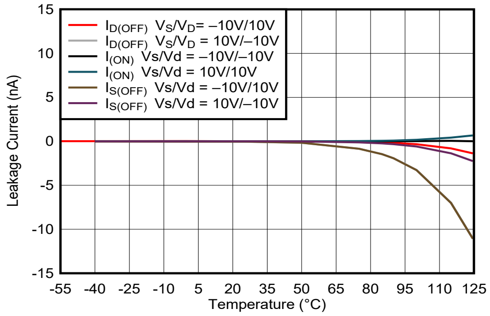
V_{DD} = 36 V, V_{SS} = 0V

図 6-8. On-Resistance vs Temperature



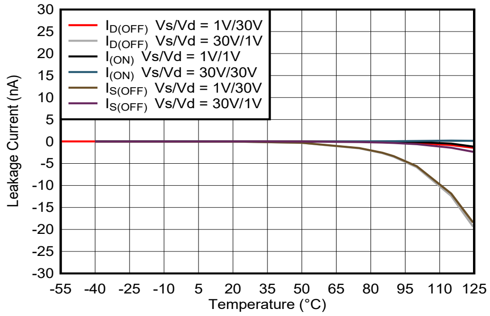
V_{DD} = 20 V, V_{SS} = -20 V

図 6-9. Leakage Current vs Temperature



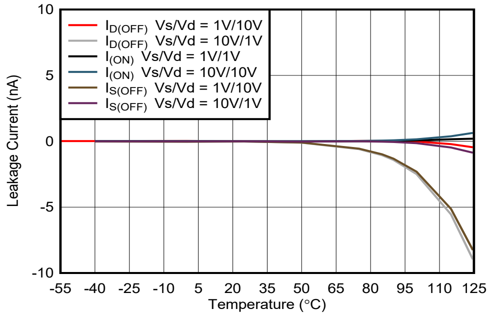
V_{DD} = 15 V, V_{SS} = -15 V

図 6-10. Leakage Current vs Temperature



V_{DD} = 36 V, V_{SS} = 0V

図 6-11. Leakage Current vs Temperature



V_{DD} = 12 V, V_{SS} = 0V

図 6-12. Leakage Current vs Temperature

6.6 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)

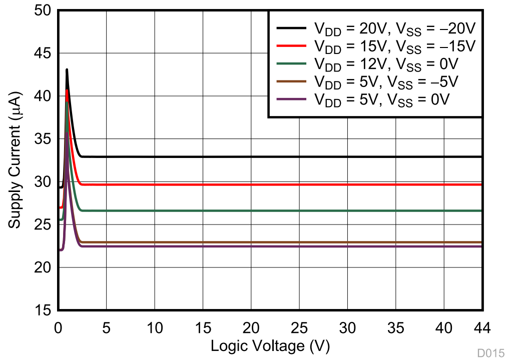


図 6-13. Supply Current vs. Logic Voltage

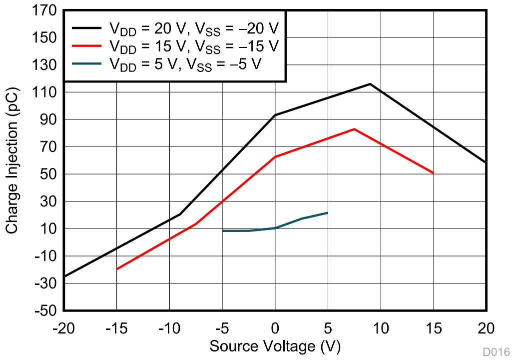


図 6-14. Charge Injection vs. Source Voltage – Dual Supply

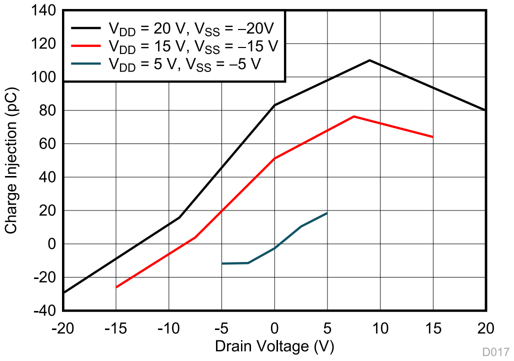


図 6-15. Charge Injection vs. Drain Voltage – Dual Supply

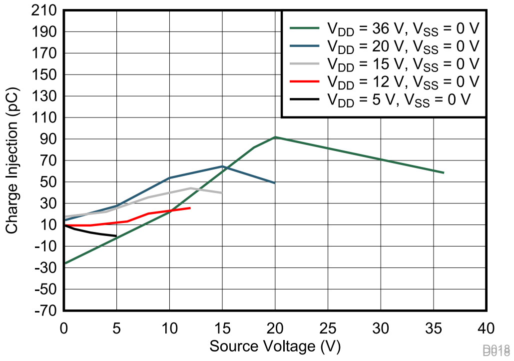


図 6-16. Charge Injection vs. Source Voltage – Single Supply

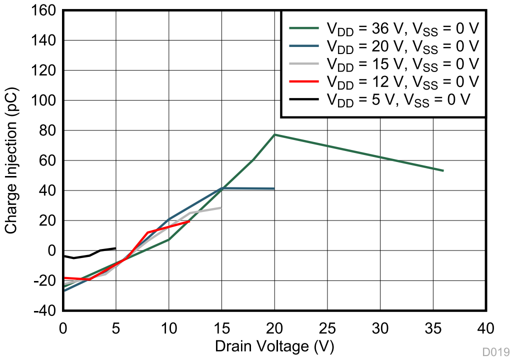
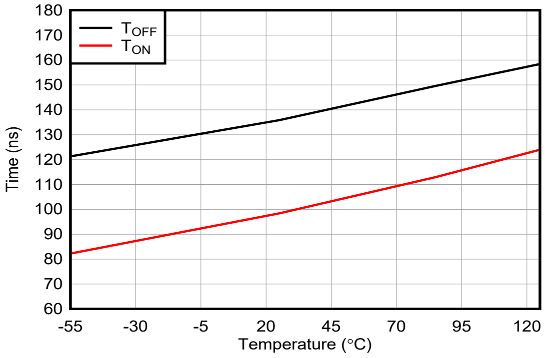


図 6-17. Charge Injection vs. Drain Voltage – Single Supply

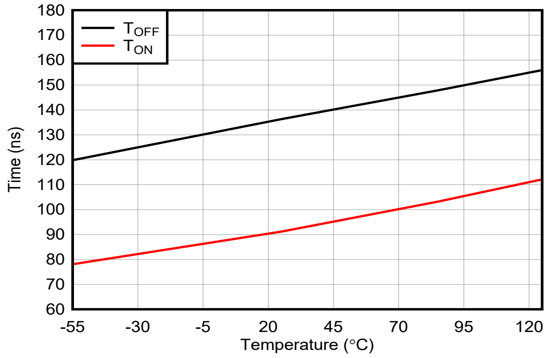


V_{DD} = 15 V, V_{SS} = -15 V

図 6-18. T_{ON} and T_{OFF} vs. Temperature

6.6 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)



V_{DD} = 36 V, V_{SS} = 0V

図 6-19. T_{ON} and T_{OFF} vs. Temperature

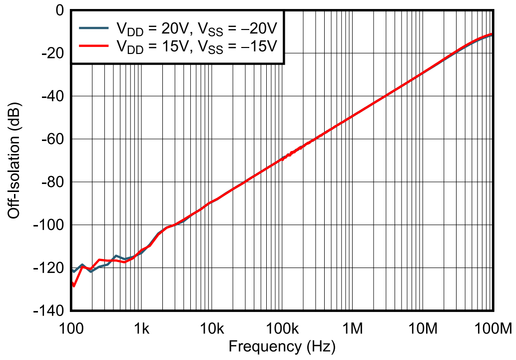


図 6-20. Off-Isolation vs Frequency

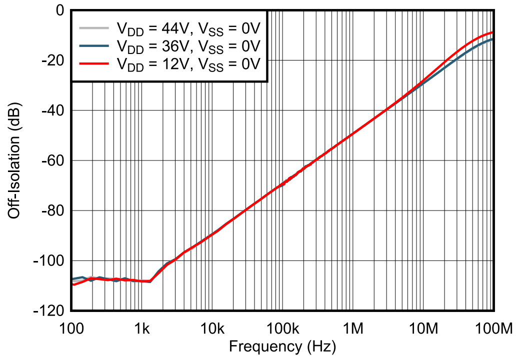
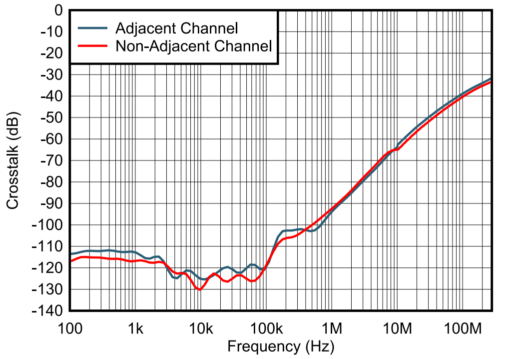


図 6-21. Off-Isolation vs Frequency



V_{DD} = +15 V, V_{SS} = -15 V

図 6-22. Crosstalk vs Frequency

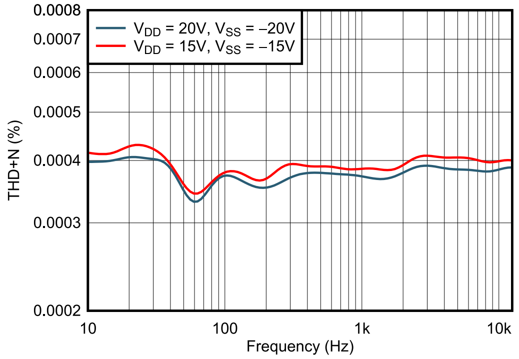


図 6-23. THD+N vs. Frequency (Dual Supplies)

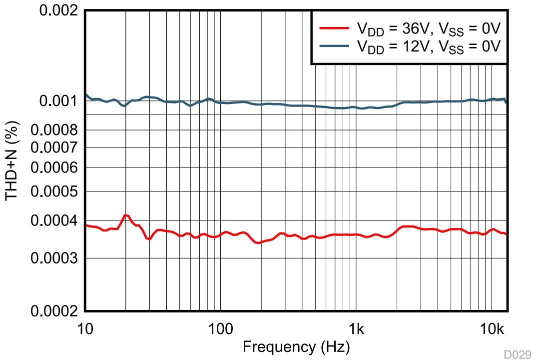
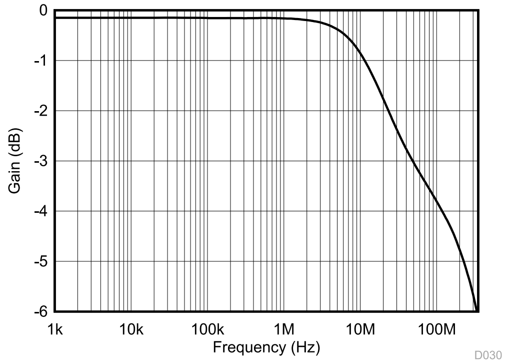


図 6-24. THD+N vs. Frequency (Single Supplies)

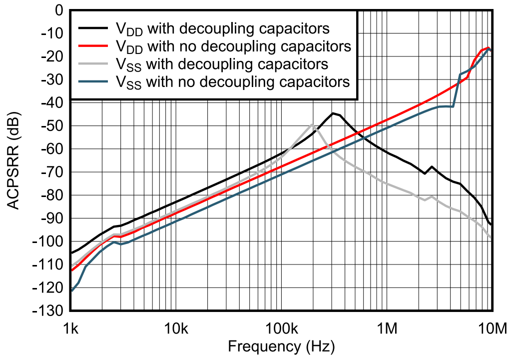
6.6 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)



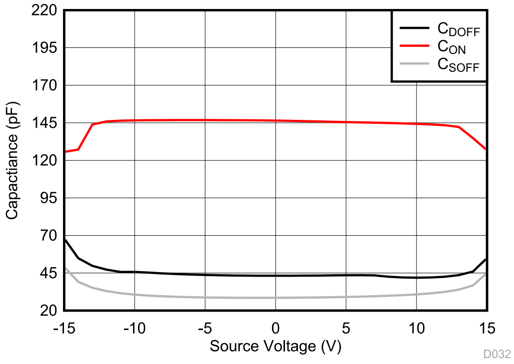
V_{DD} = +15 V, V_{SS} = -15 V

図 6-25. On Response vs Frequency



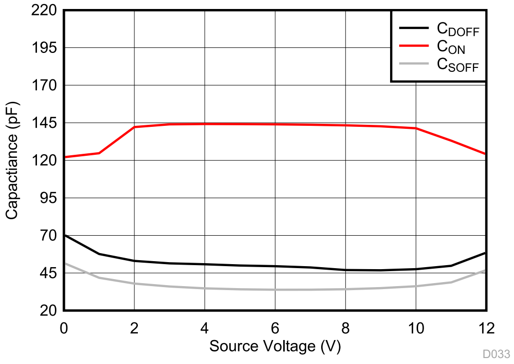
V_{DD} = +15 V, V_{SS} = -15 V

図 6-26. ACPSRR vs. Frequency



V_{DD} = +15 V, V_{SS} = -15 V

図 6-27. Capacitance vs. Source Voltage or Drain Voltage



V_{DD} = 12 V, V_{SS} = 0V

図 6-28. Capacitance vs. Source Voltage or Drain Voltage

7 Parameter Measurement Information

7.1 On-Resistance

The on-resistance of a device is the ohmic resistance between the source (Sx) and drain (Dx) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. 図 7-1 shows the measurement setup used to measure R_{ON}. Voltage (V) and current (I_{SD}) are measured using this setup, and R_{ON} is computed with $R_{ON} = V / I_{SD}$:

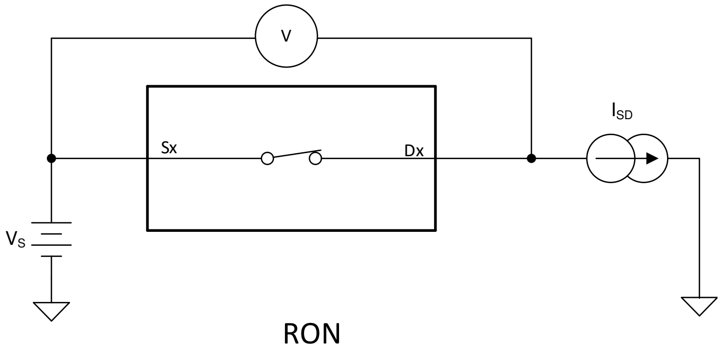


図 7-1. On-Resistance Measurement Setup

7.2 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

1. Source off-leakage current.
2. Drain off-leakage current.

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

Drain leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol $I_{D(OFF)}$.

図 7-2 shows the setup used to measure both off-leakage currents.

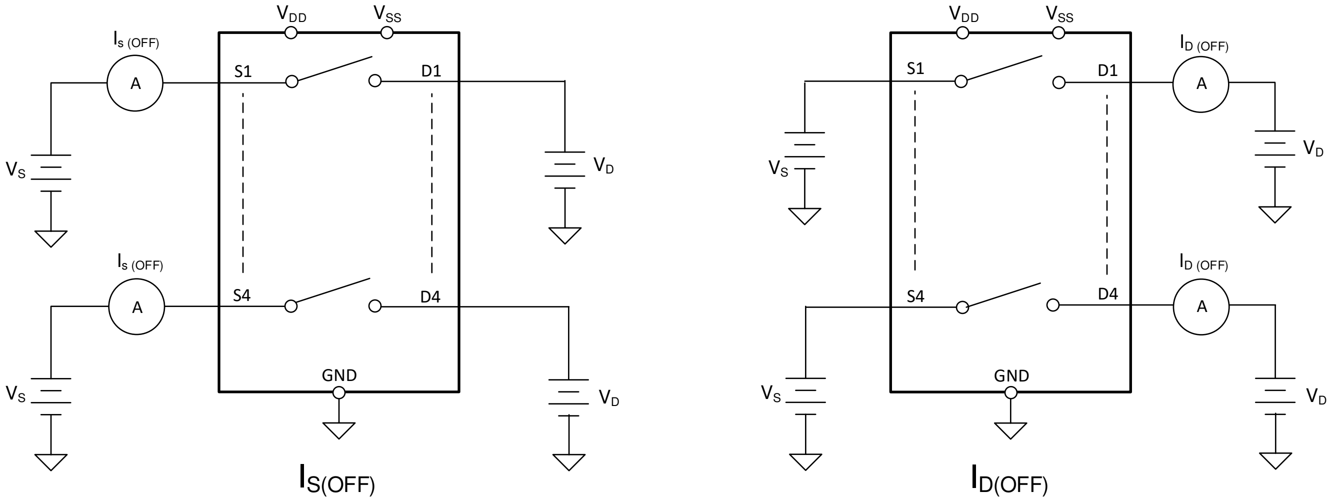


図 7-2. Off-Leakage Measurement Setup

7.3 On-Leakage Current

Source on-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is on. This current is denoted by the symbol $I_{S(ON)}$.

Drain on-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is on. This current is denoted by the symbol $I_{D(ON)}$.

Either the source pin or drain pin is left floating during the measurement. 図 7-3 shows the circuit used for measuring the on-leakage current, denoted by $I_{S(ON)}$ or $I_{D(ON)}$.

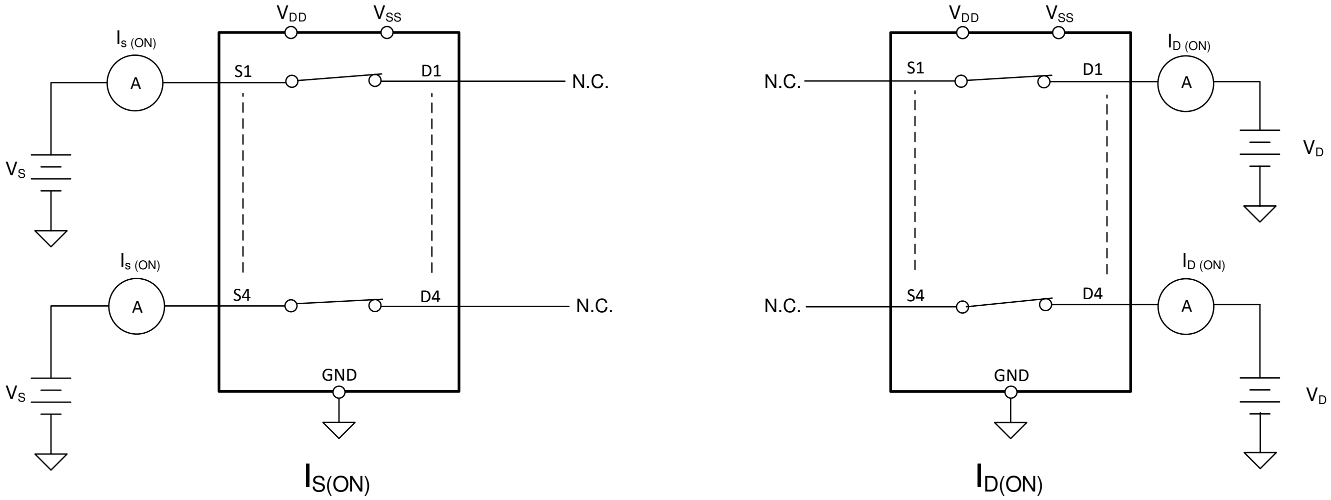


図 7-3. On-Leakage Measurement Setup

7.4 t_{ON} and t_{OFF} Time

Turn-on time is defined as the time taken by the output of the device to rise to 90% after the enable has risen past the logic threshold. The 90% measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. 図 7-4 shows the setup used to measure turn-on time, denoted by the symbol t_{ON}.

Turn-off time is defined as the time taken by the output of the device to fall to 10% after the enable has fallen past the logic threshold. The 10% measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. 図 7-4 shows the setup used to measure turn-off time, denoted by the symbol t_{OFF}.

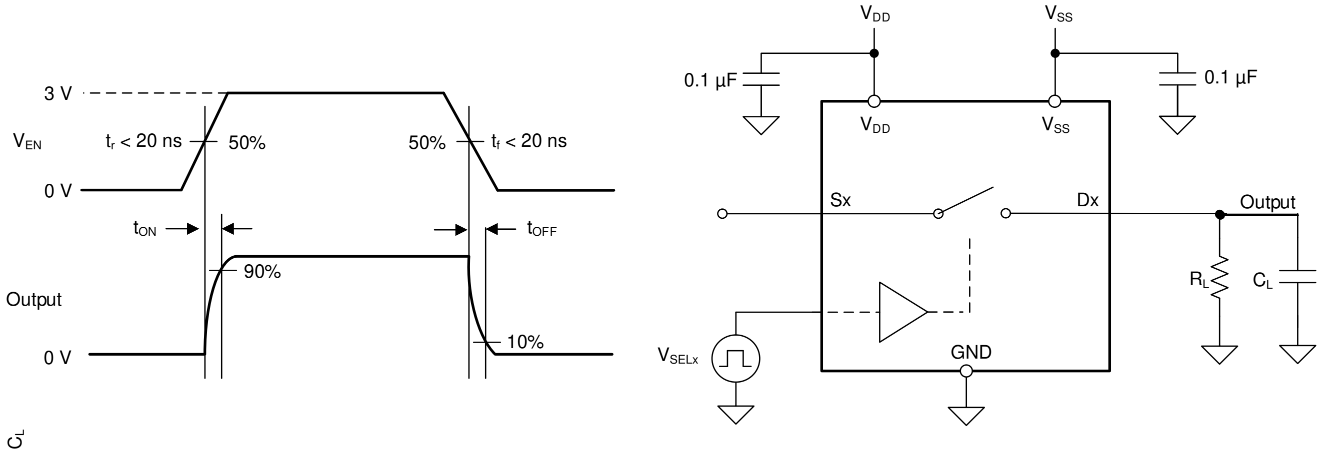


図 7-4. Turn-On and Turn-Off Time Measurement Setup

7.5 $t_{ON\ (VDD)}$ Time

The $t_{ON\ (VDD)}$ time is defined as the time taken by the output of the device to rise to 90% after the supply has risen past the supply threshold. The 90% measurement is used to provide the timing of the device turning on in the system. 図 7-5 shows the setup used to measure turn on time, denoted by the symbol $t_{ON\ (VDD)}$.

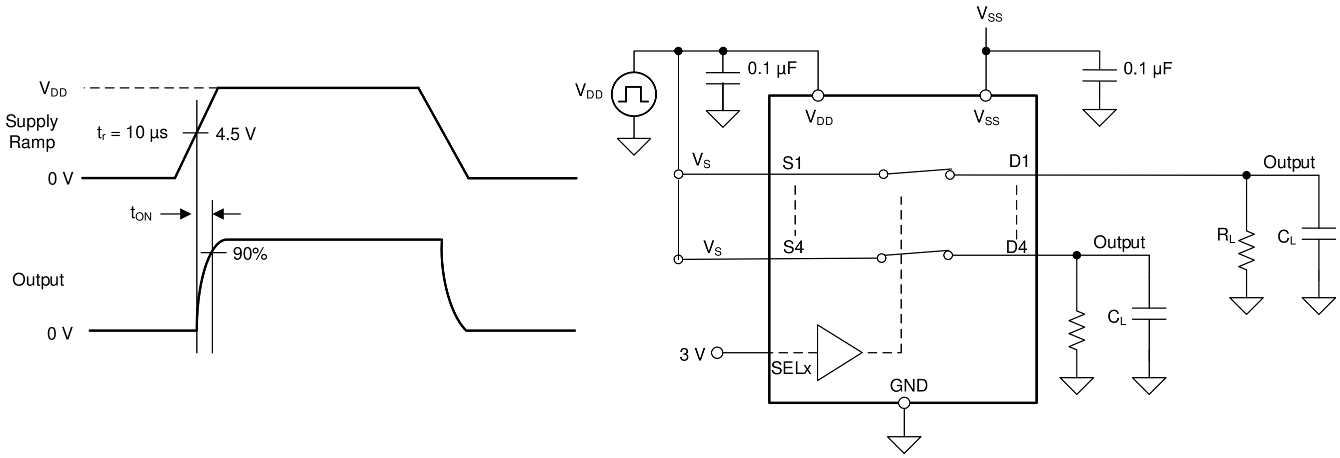


図 7-5. $t_{ON\ (VDD)}$ Time Measurement Setup

7.6 Propagation Delay

Propagation delay is defined as the time taken by the output of the device to rise or fall 50% after the input signal has risen or fallen past the 50% threshold. 図 7-6 shows the setup used to measure propagation delay, denoted by the symbol t_{PD}.

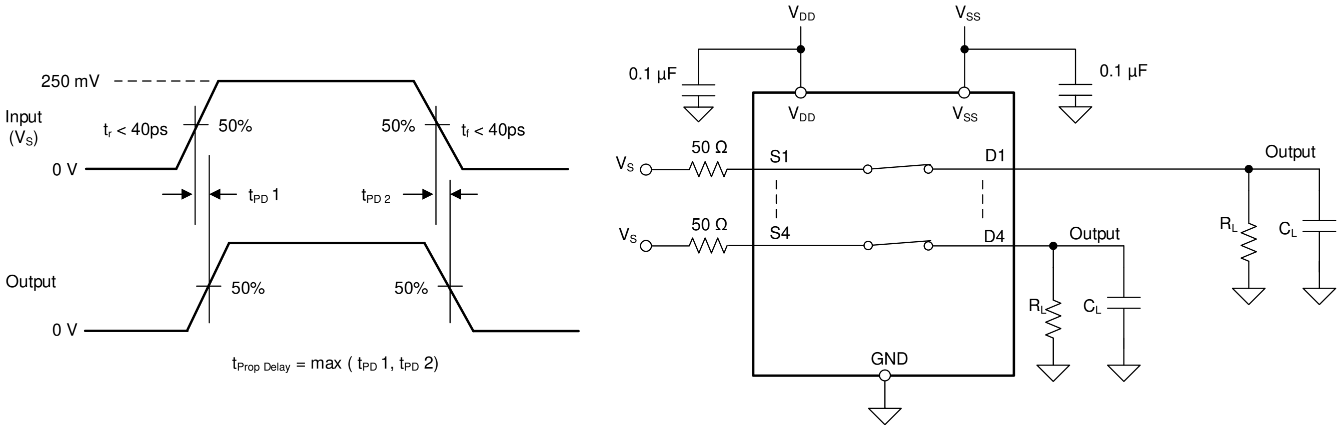


図 7-6. Propagation Delay Measurement Setup

7.7 Charge Injection

The TMUX7212M devices have a transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_C. 図 7-7 shows the setup used to measure charge injection from source (Sx) to drain (Dx).

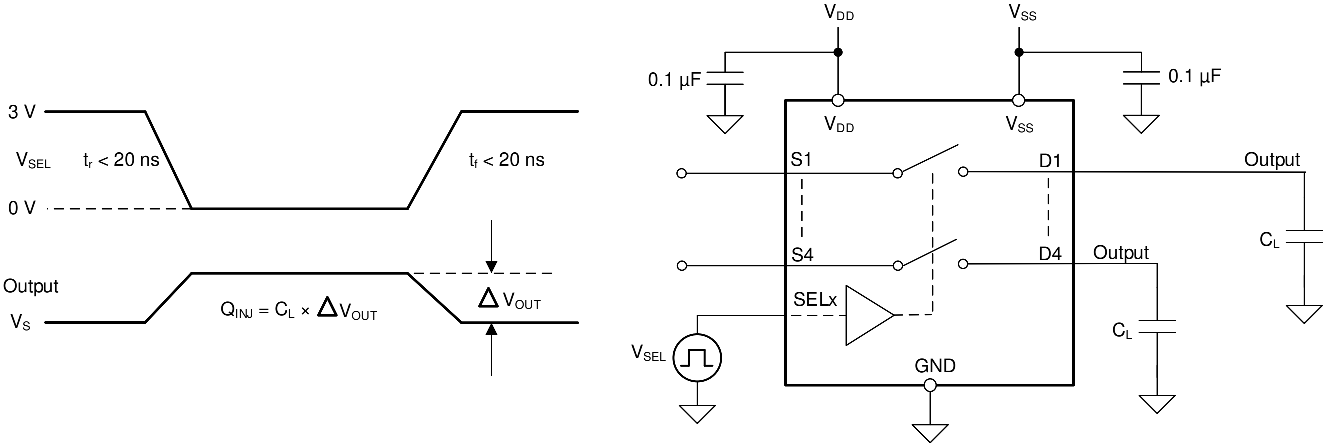
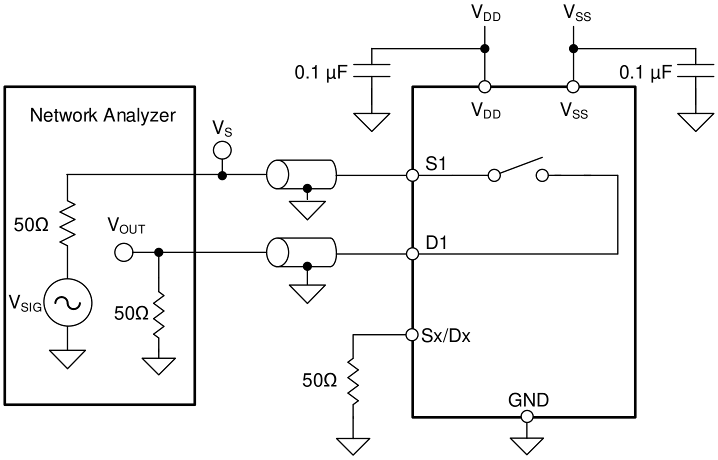


図 7-7. Charge-Injection Measurement Setup

7.8 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (Dx) of the device when a signal is applied to the source pin (Sx) of an off-channel. The characteristic impedance, Z_0, for the measurement is 50 Ω. 図 7-8 shows the setup used to measure off isolation. Use off isolation equation to compute off isolation.

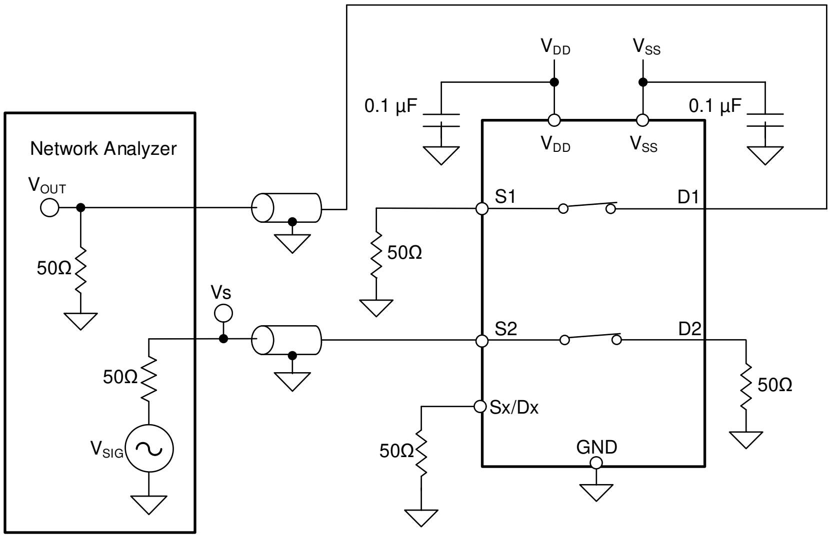


$$Off\ Isolation = 20 \times Log \frac{V_{OUT}}{V_S}$$

図 7-8. Off Isolation Measurement Setup

7.9 Channel-to-Channel Crosstalk

Crosstalk is defined as the ratio of the signal at the drain pin (Dx) of a different channel, when a signal is applied at the source pin (Sx) of an on-channel. The characteristic impedance, Z_0, for the measurement is 50 Ω. 図 7-9 shows the setup used to measure, and the equation used to compute crosstalk.

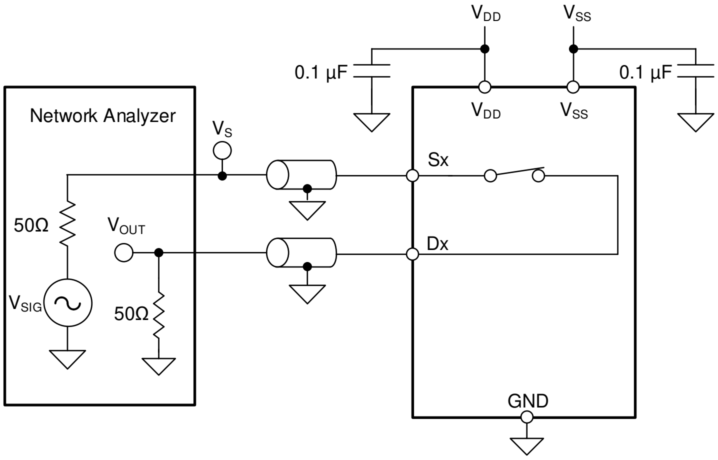


$$Crosstalk = 20 \times Log \frac{V_{OUT}}{V_S}$$

図 7-9. Channel-to-Channel Crosstalk Measurement Setup

7.10 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (Dx) of the device. The characteristic impedance, Z_0, for the measurement is 50 Ω. 図 7-10 shows the setup used to measure bandwidth.



$$Bandwidth = 20 \times Log \frac{V_{OUT}}{V_S}$$

図 7-10. Bandwidth Measurement Setup

7.11 THD + Noise

The total harmonic distortion (THD) of a signal is a measurement of the harmonic distortion, and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency at the mux output. The on-resistance of the device varies with the amplitude of the input signal and results in distortion when the drain pin is connected to a low-impedance load. Total harmonic distortion plus noise is denoted as THD + N.

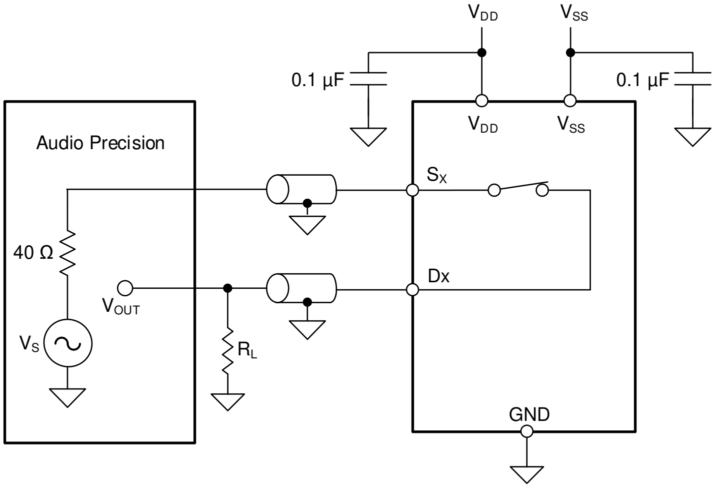
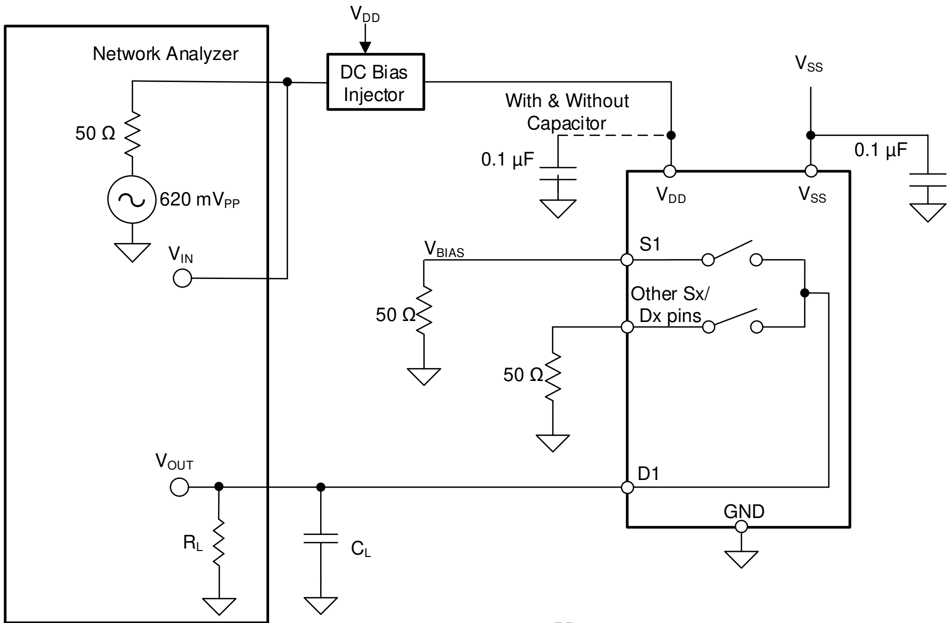


図 7-11. THD + N Measurement Setup

7.12 Power Supply Rejection Ratio (PSRR)

PSRR measures the ability of a device to prevent noise and spurious signals that appear on the supply voltage pin from coupling to the output of the switch. The DC voltage on the device supply is modulated by a sine wave of 100 mV_{PP}. The ratio of the amplitude of signal on the output to the amplitude of the modulated signal is the AC PSRR.



$$PSRR = 20 \times Log \frac{V_{OUT}}{V_{IN}}$$

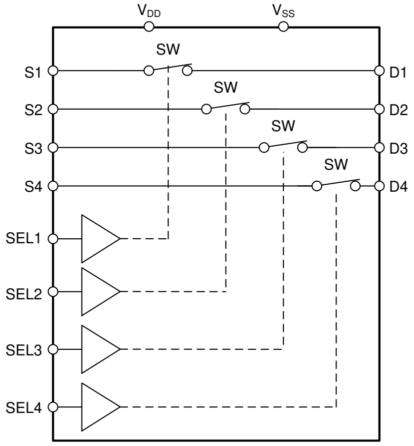
図 7-12. AC PSRR Measurement Setup

8 Detailed Description

8.1 Overview

The TMUX7212M is a 1:1 (SPST), 4-channel switch. The device has four independently selectable single-pole, single-throw switches that are turned-on or turned-off based on the state of the corresponding select pin.

8.2 Functional Block Diagram



TMUX7212M
(SELx = Logic 1)

8.3 Feature Description

8.3.1 Bidirectional Operation

The TMUX7212M conducts equally well from source (Sx) to drain (Dx) or from drain (Dx) to source (Sx). Each channel has similar characteristics in both directions and supports both analog and digital signals.

8.3.2 Rail-to-Rail Operation

The valid signal path input and output voltage for TMUX7212M ranges from V_{SS} to V_{DD}.

8.3.3 1.8V Logic Compatible Inputs

The TMUX7212M device has 1.8V logic compatible control for all logic control inputs. 1.8V logic level inputs allows the TMUX7212M to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and bill of material cost. For more information on 1.8V logic implementations refer to *Simplifying Design with 1.8V logic Muxes and Switches*.

8.3.4 Integrated Pull-Down Resistor on Logic Pins

The TMUX7212M has internal weak pull-down resistors to GND to ensure the logic pins are not left floating. The value of this pull-down resistor is approximately 4MΩ, but is clamped to about 1 µA at higher voltages. This feature integrates up to four external components and reduces system size and cost.

8.3.5 Fail-Safe Logic

The TMUX7212M supports Fail-Safe Logic on the control input pins (SEL1, SEL2, SEL3, and SEL4) allowing for operation up to 44 V, regardless of the state of the supply pin. This feature allows voltages on the control pins to be applied before the supply pin, protecting the device from potential damage. Fail-Safe Logic minimizes system complexity by removing the need for power supply sequencing on the logic control pins. For example, the Fail-Safe Logic feature allows the select pins of the TMUX7212M to be ramped to 44 V while V_{DD} and V_{SS} = 0V. The logic control inputs are protected against positive faults of up to 44 V in powered-off condition, but do not offer protection against negative overvoltage conditions.

8.3.6 Latch-Up Immune

Latch-up is a condition where a low impedance path is created between a supply pin and ground. This condition is caused by a trigger (current injection or overvoltage), but once activated, the low impedance path remains even after the trigger is no longer present. This low impedance path may cause system upset or catastrophic damage due to excessive current levels. The latch-up condition typically requires a power cycle to eliminate the low impedance path.

The TMUX7212M family of devices are constructed on silicon on insulator (SOI) based process where an oxide layer is added between the PMOS and NMOS transistor of each CMOS switch to prevent parasitic structures from forming. The oxide layer is also known as an insulating trench and prevents triggering of latch up events due to overvoltage or current injections. The latch-up immunity feature allows the TMUX7212M family of switches and multiplexers to be used in harsh environments. For more information on latch-up immunity refer to *Using Latch Up Immune Multiplexers to Help Improve System Reliability*.

8.3.7 Ultra-Low Charge Injection

図 8-1 shows how the TMUX7212M devices have a transmission gate topology. Any mismatch in the stray capacitance associated with the NMOS and PMOS causes an output level change whenever the switch is opened or closed.

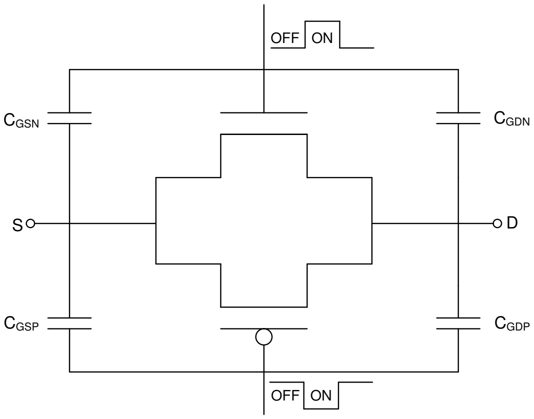


図 8-1. Transmission Gate Topology

The TMUX7212M contains specialized architecture to reduce charge injection on the Drain (Dx). To further reduce charge injection in a sensitive application, a compensation capacitor (Cp) can be added on the Source (Sx). This will ensure that excess charge from the switch transition will be pushed into the compensation capacitor on the Source (Sx) instead of the Drain (Dx). As a general rule, Cp should be 20x larger than the equivalent load capacitance on the Drain (Dx). 図 8-2 shows charge injection variation with different compensation capacitors on the Source side. This plot was captured on the TMUX7219M as part of the TMUX72xx family with a 100 pF load capacitance.

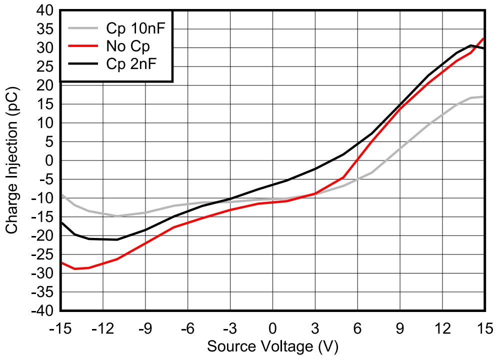


図 8-2. Charge Injection Compensation

8.4 Device Functional Modes

The TMUX7212M device has four independently selectable single-pole, single-throw switches that are turned-on or turned-off based on the state of the corresponding select pin. The control pins can be as high as 44 V.

The TMUX7212M devices can operate without any external components except for the supply decoupling capacitors. The SELx pins have internal pull-down resistors of 4MΩ. If unused, then the SELx pin must be tied to GND for the device to not consume additional current as highlighted in *Implications of Slow or Floating CMOS Inputs*. Unused signal path inputs (Sx or Dx) should be connected to GND.

8.5 Truth Tables

表 8-1 shows the truth tables for the TMUX7212M.

表 8-1. TMUX7212M Truth Table

SEL x (1)	CHANNEL x
0	Channel x OFF
1	Channel x ON

(1) x denotes 1, 2, 3, or 4 for the corresponding channel.

9 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

The TMUX7212M is part of the precision switches and multiplexers family of devices. These devices operate with dual supplies (±4.5V to ±22 V), a single supply (4.5V to 44 V), or asymmetric supplies (such as V_{DD} = 12 V, V_{SS} = –30 V), and offer true rail-to-rail input and output. The TMUX7212M offers low R_{ON}, low on and off leakage currents and ultra-low charge injection performance. These features makes the TMUX7212M a family of precision, robust, high-performance analog multiplexer for high-voltage, automotive applications.

9.2 Typical Application – Switched Gain Amplifier

Switches and multiplexers are commonly used in the feedback path of amplifier circuits to provide configurable gain control. By using various resistor values on each switch path the TMUX7212M allows the system to have multiple gain settings. An external resistor, or utilizing 1 channel always being closed, ensures the amplifier is not operating in an open loop configuration. The leakage current, On-Resistance, and charge injection performance of the TMUX7212M are key specifications to evaluate when selecting a device for gain control.

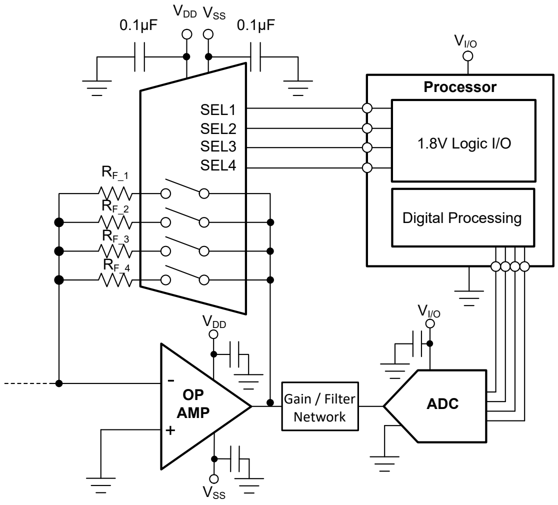


図 9-1. Switching Gain Settings

9.3 Design Requirements

For this design example, use the parameters listed in 表 9-1.

表 9-1. Design Parameters

PARAMETERS	VALUES
Supply (V_{DD})	15 V
Supply (V_{SS})	- 15 V
Input / Output signal range	-15 V to 15 V (Rail-to-Rail)
Control logic thresholds	1.8V compatible

9.4 Detailed Design Procedure

The TMUX7212M device can be operated without any external components except for the supply decoupling capacitors. All inputs signals passing through the switch must fall within the recommended operating conditions of the TMUX7212M including signal range and continuous current. For this design example, with a supply of +15 V and -15V, the signals can range from +15 V to -15V when the device is powered. The maximum continuous current can be 220mA.

The application shown in *Switching Gain Settings* demonstrates how to use the TMUX7212M to control the feedback gain of a precision op-amp. This feedback design can very sensitive to induced voltage and current offsets. The TMUX7212M has a typical On-leakage current of 100 pA which would lead to an accuracy well within 1% of a full scale 1 µA signal, thus minimizing errors from current offsets. The low On-Resistance of the TMUX7212M leads to a low error in the feedback resistance and resulting gain. This additionally minimizes any voltage offsets.

9.5 Power Supply Recommendations

The TMUX7212M device operates across a wide supply range of ±4.5V to ±22 V (4.5V to 44 V in single-supply mode). The device also perform well with asymmetrical supplies such as V_{DD} = 12 V and V_{SS} = –5 V.

Power-supply bypassing improves noise margin and prevents switching noise propagation from the supply rails to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1µF to 10µF at both the V_{DD} and V_{SS} pins to ground. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground and power planes. Always ensure the ground (GND) connection is established before supplies are ramped.

9.6 Layout

9.6.1 Layout Guidelines

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. 図 9-2 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

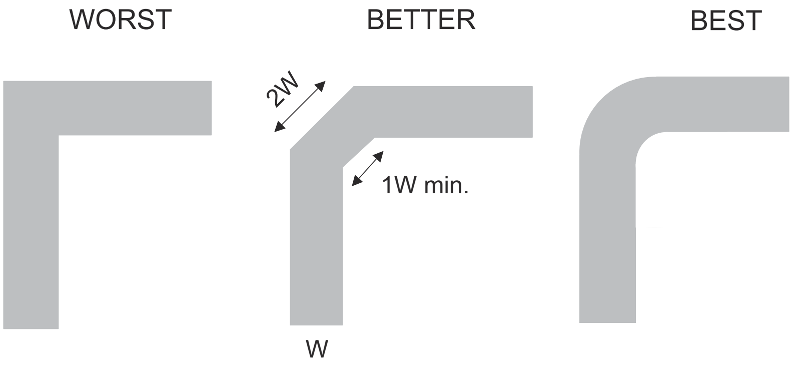


図 9-2. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

Some key considerations are:

- For reliable operation, connect a decoupling capacitor ranging from 0.1µF to 10µF between VDD/VSS and GND. We recommend a 0.1µF and 1µF capacitor, placing the lowest value capacitor as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the supply voltage.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.
- Using multiple vias in parallel will lower the overall inductance and is beneficial for connection to ground planes.

9.6.2 Layout Example

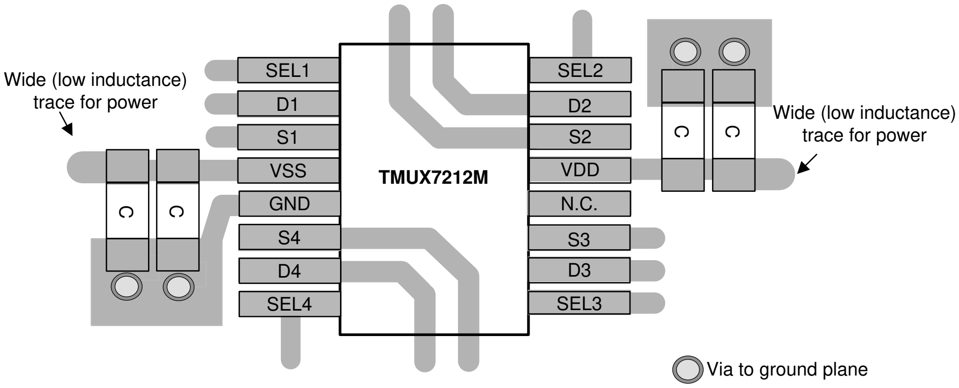


図 9-3. TMUX7212M Layout Example

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

- Texas Instruments, *Using Latch Up Immune Multiplexers to Help Improve System Reliability* application note
- Texas Instruments, *Improve Stability Issues with Low CON Multiplexers* application brief
- Texas Instruments, *Improving Signal Measurement Accuracy in Automated Test Equipment* application brief
- Texas Instruments, *Sample & Hold Glitch Reduction for Precision Outputs Reference Design* reference guide
- Texas Instruments, *Simplifying Design with 1.8V logic Muxes and Switches* application brief
- Texas Instruments, *System-Level Protection for High-Voltage Analog Multiplexers* application note
- Texas Instruments, *True Differential, 4 x 2 MUX, Analog Front End, Simultaneous-Sampling ADC Circuit* application note
- Texas Instruments, *Quad Flatpack No-Lead Logic Packages* application note

10.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

10.3 サポート・リソース

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10.6 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

11 Revision History

DATE	REVISION	NOTES
January 2024	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMUX7212MPWR	Active	Production	TSSOP (PW) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	X212
TMUX7212MPWR.B	Active	Production	TSSOP (PW) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	X212

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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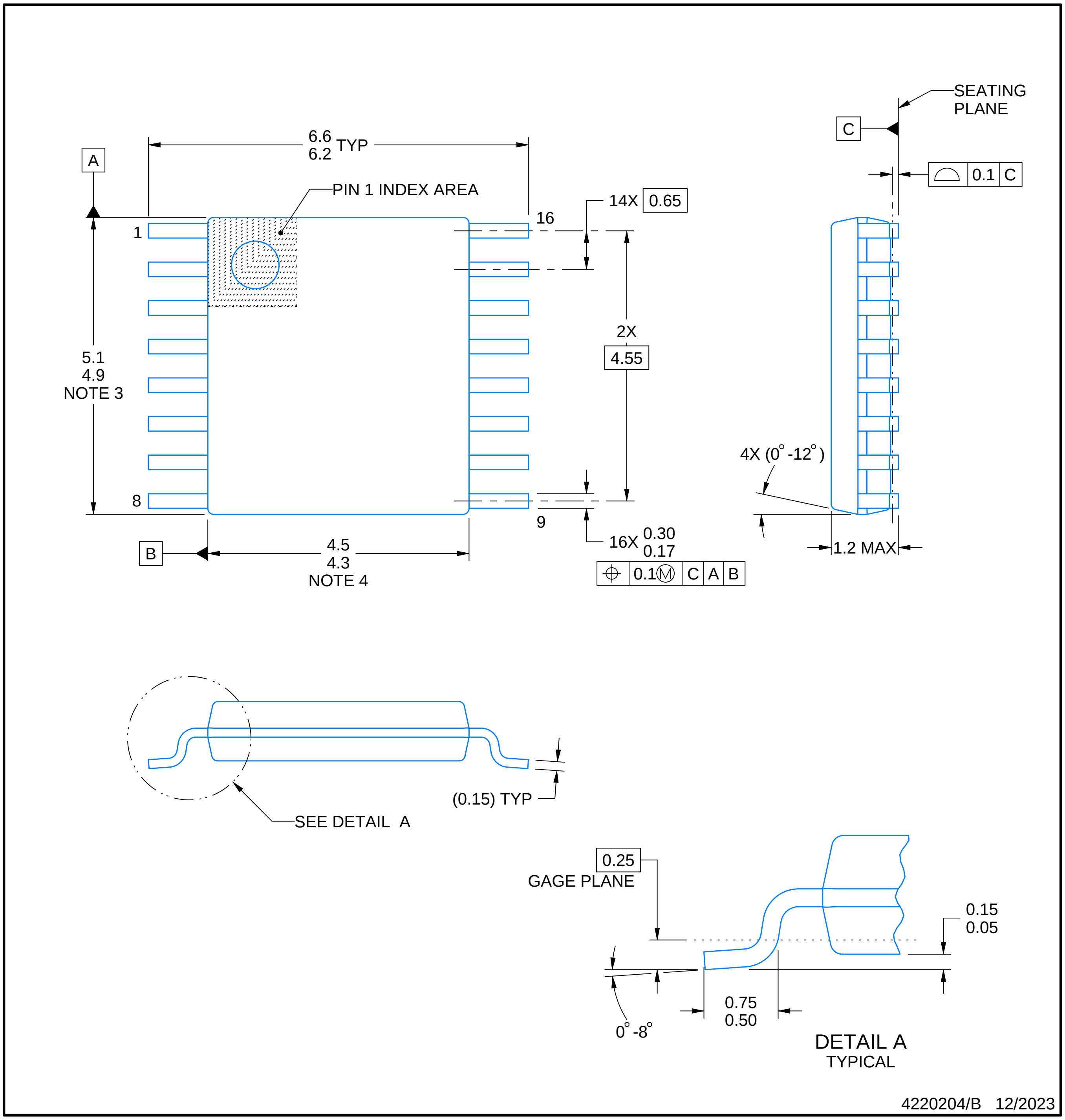

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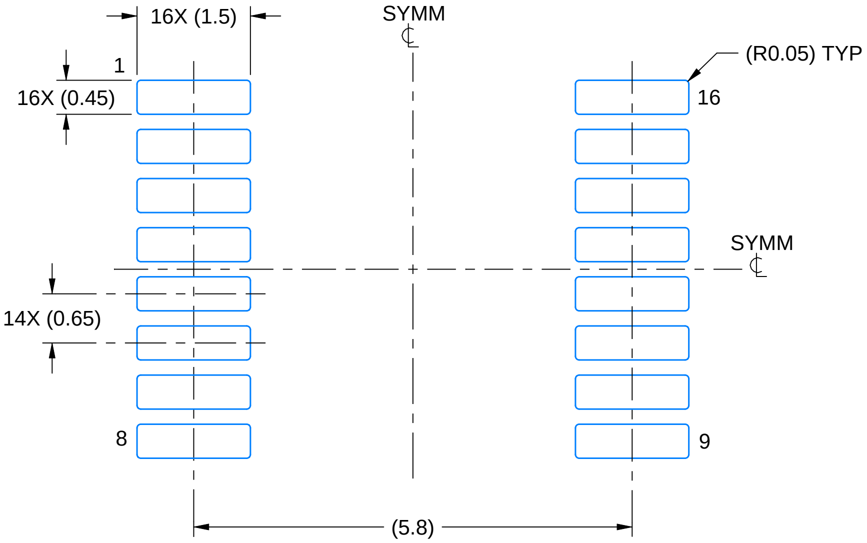
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

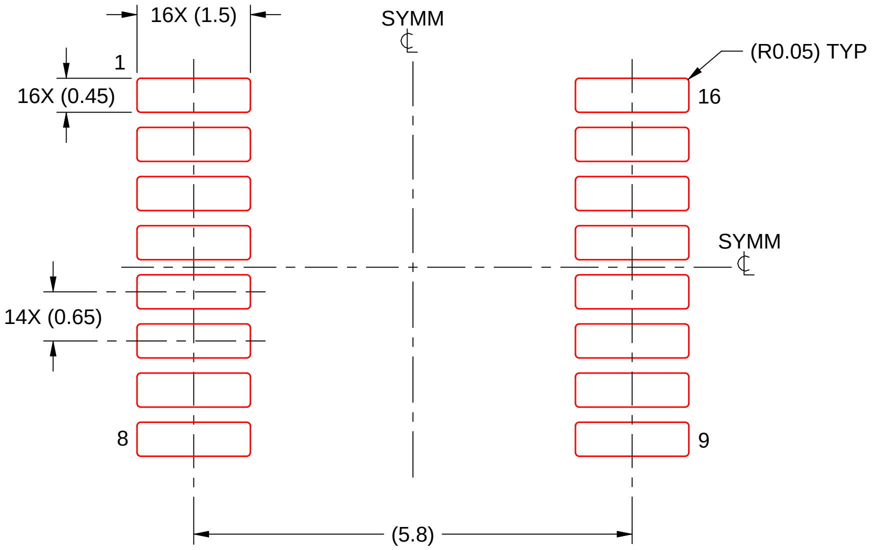
NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月