# TMUX646 1.8V ロジック対応、6GHz、5V、2:1 (SPDT)、10 チャネル MIPI スイッチ

## 1 特長

- 電源電圧範囲：1.5V ~ 5.5V
- 10 チャネル、2：1 双方向スイッチ
- MIPI CSI/DSI、SATA、LVDS、RGMII、DDR、イーサネット・インターフェイスをサポート
- 電源オフ保護：
  $V_{DD}$ = 0V のとき I/O は Hi-Z
- 低 $R_{ON}$：6Ω (標準値)
- 高帯域：6GHz
- 超低クロストーク：-40dB
- 低消費電力のディセーブル・モード
- 1.2V ロジック互換
- 双方向の信号パス
- ESD 保護：
  - 人体モデル (HBM) で 6kV
  - 人体モデル (CDM) で 2kV

## 2 アプリケーション

- 携帯電話 / スマートフォン
- タブレット
- PC とノート PC
- 仮想現実および拡張現実
- ドローン
- カメラ・ベースのカーコード・スキャナ
- 医療用
- IP ネットカム

## 3 概要

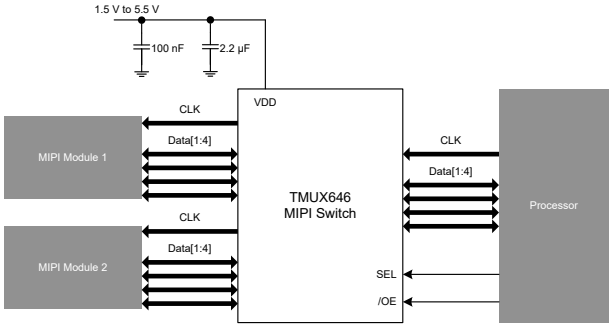
TMUX646 は、高速アプリケーション用に最適化された 10 チャネル (5 差動) の単極双投双方向スイッチです。TMUX646 は、複数の MIPI 準拠デバイスを単一の CSI/DSI、C-PHY/D-PHY モジュールに接続しやすくするよう設計されています。本デバイスは SATA、SAS、MIPI DSI/CSI、LVDS、RGMII、DDR、イーサネット・インターフェイスもサポートしています。

このデバイスは帯域幅が 6GHz で、チャネル間のスキューが低く、信号の劣化が少なく、レイアウト損失を補償するため広いマージンがあります。消費電流が小さいため、携帯電話や他の個人用電子機器など、低消費電力のアプリケーションの要求を満たすことができます。

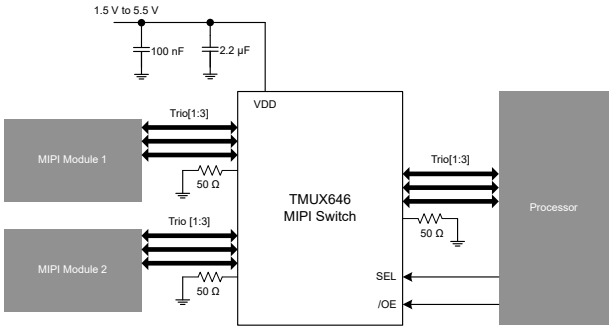
**製品情報**(1)

| 部品番号 | パッケージ | 本体サイズ (公称) |
|---|---|---|
| TMUX646 | nFBGA (ZEC) | 2.45mm × 2.45mm |

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。




**D-PHY の概略回路図**




**C-PHY の概略回路図**

# Table of Contents



## 4 Revision History

| DATE | REVISION | NOTES |
|---|---|---|
| June 2021 | * | Initial Release |

# 5 Pin Configuration and Functions

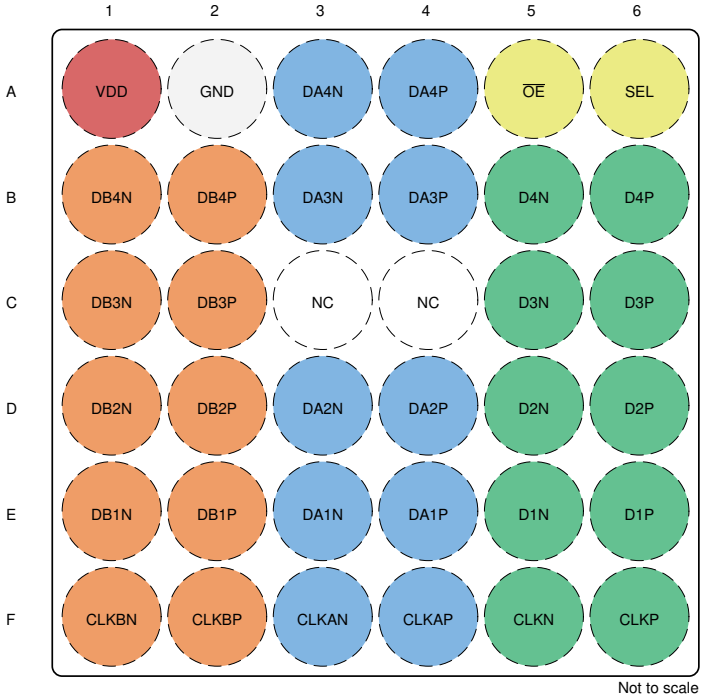



**図 5-1. nFBGA Package 36 Pin (ZEC) Top View**

**表 5-1. Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| CLKAN | F3 | I/O | Differential I/O |
| CLKAP | F4 | I/O | Differential I/O |
| CLKBN | F1 | I/O | Differential I/O |
| CLKBP | F2 | I/O | Differential I/O |
| CLKN | F5 | I/O | Differential I/O |
| CLKP | F6 | I/O | Differential I/O |
| D1N | E5 | I/O | Differential I/O |
| D1P | E6 | I/O | Differential I/O |
| D2N | D5 | I/O | Differential I/O |
| D2P | D6 | I/O | Differential I/O |
| D3N | C5 | I/O | Differential I/O |
| D3P | C6 | I/O | Differential I/O |
| D4N | B5 | I/O | Differential I/O |
| D4P | B6 | I/O | Differential I/O |
| DA1N | E3 | I/O | Differential I/O |
| DA1P | E4 | I/O | Differential I/O |
| DA2N | D3 | I/O | Differential I/O |
| DA2P | D4 | I/O | Differential I/O |
| DA3N | B3 | I/O | Differential I/O |
| DA3P | B4 | I/O | Differential I/O |
| DA4N | A3 | I/O | Differential I/O |
| DA4P | A4 | I/O | Differential I/O |

**表 5-1. Pin Functions (continued)**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| DB1N | E1 | I/O | Differential I/O |
| DB1P | E2 | I/O | Differential I/O |
| DB2N | D1 | I/O | Differential I/O |
| DB2P | D2 | I/O | Differential I/O |
| DB3N | C1 | I/O | Differential I/O |
| DB3P | C2 | I/O | Differential I/O |
| DB4N | B1 | I/O | Differential I/O |
| DB4P | B2 | I/O | Differential I/O |
| GND | A2 | P | Device Ground |
| NC | C3 | — | No internal connection |
| NC | C4 | — | No internal connection |
| $\overline{OE}$ | A5 | I | Output enable (active low), has internal pull-down resistor |
| SEL | A6 | I | Channel select, has internal pull-down resistor |
| VDD | A1 | P | Power supply input |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | –0.5 | 6 | V |
| $V_{SW}$ | Switch signal voltage (CLKP/N, CLKAP/N, CLKBP/N, DxP/N, DAxP/N, DBxP/N) | –0.5 | 4 | V |
| $V_{SEL}$, $V_{\overline{OE}}$ | Logic control input pin voltage (SEL, $\overline{OE}$) | –0.5 | 6 | V |
| $T_J$ | Junction temperature | –65 | 125 | °C |
| $T_{stg}$ | Storage temperature | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±6000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | ±2000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | 1.5 | | 5.5 | V |
| $V_{SW}$ | Switch signal voltage (CLKP/N, CLKAP/N, CLKBP/N, DxP/N, DAxP/N, DBxP/N) | 0 | | 3.6 | V |
| $V_{(SEL)}$ $V_{(\overline{OE})}$ | Logic control input pin voltage | 0 | | 5.5 | V |
| $I_S$ or $I_D$ (CONT) | Continuous current through switch | –35(1) | | 35(1) | mA |
| $T_A$ | Operating ambient temperature | –40 | | 85 | °C |

(1) At $T_J$ = 85°C

## 6.4 Thermal Information

| THERMAL METRIC(1) | | TMUX646 ZEC (nFBGA) 36 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 111.7 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 49.2 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 54.9 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 2.0 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 54.7 | °C/W |

## 6.4 Thermal Information (continued)

| THERMAL METRIC(1) | | TMUX646 ZEC (nFBGA) 36 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | |
| $I_{DD}$ | VDD active supply current | $V_{DD}$ = 1.5 V to 5.5 V<br>$\overline{OE}$ = 0 V<br>SEL = 0 V or 5.5 V<br>Dn, CLKn = 0 V | | 30 | 55 | µA |
| $I_{DD\_PD}$ | Power-down supply current | $V_{DD}$ = 1.5 V to 5.5 V<br>$\overline{OE}$ = $V_{DD}$<br>SEL = 0 V or 5.5 V<br>Dn, CLKn = 0 V | | 0.1 | 1 | µA |
| $\Delta I_{DD}$ | Increase in supply current per logic pin at 1.8 V | $V_{DD}$ = 2.5 V<br>$\overline{OE}$ = 1.8 V<br>SEL = 0 V or $V_{DD}$<br>Dn, CLKn = 0 V | | 1.3 | | µA |
| | | $V_{DD}$ = 5 V<br>$\overline{OE}$ = 1.8 V<br>SEL = 0 V or $V_{DD}$<br>Dn, CLKn = 0 V | | 2.5 | | µA |
| **DC CHARACTERISTICS** | | | | | | |
| $R_{ON\_HS}$ | On-state resistance | $V_{DD}$ = 1.5 V to 5.5 V<br>$\overline{OE}$ = 0 V, SEL = 0 V or $V_{DD}$ ,<br>Dn, CLKn = –8 mA, 0.2 V<br>DAn, DBn, CLKAn, CLKBn = 0.2 V, –8 mA | | 6 | 9 | Ω |
| $R_{ON\_LP}$ | On-state resistance | $V_{DD}$ = 1.5 V to 5.5 V<br>$\overline{OE}$ = 0 V, SEL = 0 V or $V_{DD}$ ,<br>Dn, CLKn = –8 mA, 1.2 V<br>DAn, DBn, CLKAn, CLKBn = 1.2 V, –8 mA | | 6 | 10 | Ω |
| $R_{ON\_flat\_HS}$ | On-state resistance flatness | $V_{DD}$ = 1.5 V to 5.5 V<br>$\overline{OE}$ = 0 V, SEL = 0 V or $V_{DD}$,<br>Dn, CLKn = –8 mA, 0 V to 0.3 V<br>DAn, DBn, CLKAn, CLKBn = 0 V to 0.3 V, –8 mA | | 0.1 | | Ω |
| $R_{ON\_flat\_LP}$ | On-state resistance flatness | $V_{DD}$ = 1.5 V to 5.5 V<br>$\overline{OE}$ = 0 V, SEL = 0 V or $V_{DD}$ ,<br>Dn, CLKn = –8 mA, 0 V to 1.3 V<br>DAn, DBn, CLKAn, CLKBn = 0 V to 1.3 V, –8 mA | | 0.9 | | Ω |
| $D_{RON\_HS}$ | On-state resistance match between + and – paths | $V_{DD}$ = 1.5 V to 5.5 V<br>$\overline{OE}$ = 0 V, SEL = 0 V or $V_{DD}$,<br>Dn, CLKn = –8 mA, 0.2 V<br>DAn, DBn, CLKAn, CLKBn = 0.2 V, –8 mA | | 0.1 | | Ω |
| $D_{RON\_LP}$ | On-state resistance match between + and – paths | $V_{DD}$ = 1.5 V to 5.5 V<br>$\overline{OE}$ = 0 V, SEL = 0 V or $V_{DD}$ ,<br>Dn, CLKn = –8 mA, 1.3 V<br>DAn, DBn, CLKAn, CLKBn = 1.3 V, –8 mA | | 0.1 | | Ω |

## 6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{OFF}$ | Switch off leakage current | $V_{DD}$ = 1.5 V to 5.5 V<br>$\overline{OE}$ = 0 V or 5.5 V<br>SEL = 0 V or 5.5 V<br>Dn, CLKn = 0 V to 1.3 V<br>DAn, DBn, CLKAn, CLKBn = 0 V to 1.3 V | –0.5 | | 0.5 | µA |
| $I_{OFF\_3\_6}$ | Switch off leakage current | VDD = 0 V, 1.5 V, 1.65 V, 3.3 V, 5.5 V<br>$\overline{OE}$ = 0 V or 5.5 V<br>SEL= 0 V or 5.5 V<br>DX,CLKX = 3.6 V<br>DAX,DBx,CLKAX,CLKBX = 3.6 V | –10 | | 10 | µA |
| $I_{ON}$ | Switch on leakage current | $V_{DD}$ = 1.5 V to 5.5 V<br>$\overline{OE}$ = 0 V<br>SEL = 0 V or 5.5 V<br>Dn, CLKn = 0 V to 1.3 V<br>DAn, DBn, CLKAn, CLKBn = 0 V to 1.3 V | –0.5 | | 0.5 | µA |
| $I_{ON\_3\_6}$ | Switch on leakage current | VDD = 1.5 V to 5.5 V<br>$\overline{OE}$ = 0 V<br>SEL= 0 V or 5.5 V<br>DX, CLKX = 3.6 V<br>DAX ,DBx, CLKAX, CLKBX = 3.6 V | –50 | | 50 | µA |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| $t_{SWITCH}$ | Switching time SEL to output | $V_{DD}$ = 1.5 V to 5.5 V<br>$\overline{OE}$ = 0 V<br>Dn, CLKn = 1.2 V<br>DAn, DBn, CLKAn, CLKBn:<br>$R_L$ = 50 Ω, $C_L$ = 15pF | | | 1.5 | µs |
| $t_{ON\_\overline{OE}}$ | Turnon time from $\overline{OE}$ to output | $V_{DD}$ = 1.5 V to 5.5 V<br>Dn, CLKn = 1.2 V<br>DAn, DBn, CLKAn, CLKBn:<br>$R_L$ = 50 Ω, $C_L$ = 15 pF | | 50 | 300 | µs |
| $t_{OFF\_\overline{OE}}$ | Turnoff time from $\overline{OE}$ to output | $V_{DD}$ = 1.5 V to 5.5 V<br>Dn, CLKn = 1.2 V<br>DAn, DBn, CLKAn, CLKBn:<br>$R_L$ = 50 Ω, $C_L$ = 15 pF | | 0.5 | 1 | µs |
| $f_{SEL\_MAX}$ | Maximum toggling frequency for the SEL line | $V_{DD}$ = 1.5 V to 5.5 V<br>Dn, CLKn = 1.2 V<br>DAn, DBn, CLKAn, CLKBn:<br>$R_L$ = 50 Ω, $C_L$ = 2 pF | | | 100 | kHz |
| $t_{ON\_VDD}$ | Turnon time from VDD to output | $V_{DD}$ = 0 V to 5.5 V<br>$V_{DD}$ ramp rate = 1 µs<br>Dn, CLKn = 1.2 V<br>DAn, DBn, CLKAn, CLKBn:<br>$R_L$ = 50 Ω, $C_L$ = 15 pF | | 50 | 300 | µs |
| $t_{OFF\_VDD}$ | Turnoff time from VDD to output | $V_{DD}$ = 5 V to 0 V<br>Dn, CLKn = 1.2 V<br>DAn, DBn, CLKAn, CLKBn:<br>$R_L$ = 50 Ω, $C_L$ = 15 pF | | 0.5 | 1 | ms |
| $t_{MIN\_\overline{OE}}$ | Minimum pulse width for $\overline{OE}$ | $V_{DD}$ = 1.5 V to 5.5 V<br>Dn, CLKn = 1.2 V<br>DAn, DBn, CLKAn, CLKBn:<br>$R_L$ = 50 Ω, $C_L$ = 2 pF | 500 | | | ns |
| $t_{BBM}$ | Break before make time | $V_{DD}$ = 1.5 V to 5.5 V<br>$\overline{OE}$ = 0 V<br>Dn, CLKn = $R_L$ = 50 Ω, $C_L$ = 15 pF<br>DAn, DBn, CLKAn, CLKBn: 1.2 V | 50 | | | ns |

## 6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{SKEW}$ | Intrapair skew (opposite transitions of same output) | $V_{DD}$ = 1.5 V to 5.5 V<br>$\overline{OE}$ = 0 V<br>Dn, CLKn =0.3 V<br>DnX, DBn, CLKAn, CLKBn:<br>$R_L$ = 50 Ω, $C_L$ = 5 pF | | 1 | | ps |
| $t_{SKEW}$ | Interpair Skew (Channel−to−Channel Skew) | $V_{DD}$ = 1.5 V to 5.5 V<br>$\overline{OE}$ = 0 V<br>Dn, CLKn = 0.3 V<br>DAn, DBn, CLKAn, CLKBn: $R_L$ = 50 Ω, $C_L$ = 5 pF | | 4 | | ps |
| $t_{PD}$ | Propagation delay with 100 ps rise time | $V_{DD}$ = 1.5 V to 5.5 V<br>$\overline{OE}$ = 0 V<br>Dn, CLKn = 1.2 V<br>DAn, DBn, CLKAn, CLKBn:<br>$R_L$ = 50 Ω, $C_L$ = 5 pF<br>$t_{RISE}$ = 100 ps | | 40 | | ps |
| $O_{ISO}$ | Differential off isolation | $V_{DD}$ = 1.5 V to 5.5 V<br>$\overline{OE}$ = 0 V, $V_{DD}$<br>SEL = 0 V, $V_{DD}$<br>Dn, CLKn, DAn, DBn, CLKAn, CLKBn:<br>$R_S$ = 50 Ω, $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_{SW}$ = 200 mVpp (differential)<br>f = 1250 MHz | | –20 | | dB |
| $X_{TALK}$ | Differential channel to channel crosstalk | $V_{DD}$ = 1.5 V to 5.5 V<br>$\overline{OE}$ = 0 V, $V_{DD}$<br>SEL = 0 V, $V_{DD}$<br>Dn, CLKn, DAn, DBn, CLKAn, CLKBn:<br>$R_S$ = 50 Ω, $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_{SW}$ = 200 mVpp (differential)<br>f = 1250 MHz | | –40 | | dB |
| BW | Differential Bandwidth | $V_{DD}$ = 1.5 V to 5.5 V<br>$\overline{OE}$ = 0 V<br>SEL = 0 V, $V_{DD}$<br>Dn, CLKn, DAn, DBn, CLKAn, CLKBn:<br>$V_{SW}$ = 200 mVpp (differential)<br>f = 1250 MHz | | 6 | | GHz |
| $I_{LOSS}$ | Insertion Loss | $V_{DD}$ = 1.5 V to 5.5 V<br>$\overline{OE}$ = 0 V<br>SEL = 0 V, $V_{DD}$<br>Dn, CLKn, DAn, DBn, CLKAn, CLKBn:<br>$R_S$ = 50 Ω, $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_{SW}$ = 200 mVpp (differential)<br>f = 100 kHz | | –0.65 | | dB |
| $C_{OFF}$ | Off capacitance | $V_{DD}$ = 1.5 V to 5.5 V<br>$\overline{OE}$ = 0 V, $V_{DD}$<br>SEL = 0 V, $V_{DD}$<br>Dn, CLKn, DAn, DBn, CLKAn, CLKBn = 0 V, 0.2 V<br>f = 1250 MHz | | 1.5 | | pF |
| $C_{ON}$ | On capacitance | $V_{DD}$ = 1.5 V to 5.5 V<br>$\overline{OE}$ = 0 V<br>SEL = 0 V, $V_{DD}$<br>Dn, CLKn, DAn, DBn, CLKAn, CLKBn = 0 V, 0.2 V<br>f = 1250 MHz | | 1.5 | | pF |
| **DIGITAL CHARACTERISTICS** | | | | | | |
| $V_{IH}$ | Input logic high | SEL, $\overline{OE}$ | 1 | | 5.5 | V |
| $V_{IL}$ | Input logic low | SEL, $\overline{OE}$ | 0 | | 0.4 | V |
| $I_{IH}$ | Input high leakage current | SEL, $\overline{OE}$ | –5 | | 5 | µA |

## 6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{IL}$ | Input low leakage current | SEL, $\overline{OE}$ | –5 | | 5 | µA |
| $R_{PD}$ | Internal pull-down resistance on digital input pins | SEL, $\overline{OE}$ | | 6 | | MΩ |
| $C_I$ | Digital Input capacitance | $V_{SEL}$ = 0 V, 1.8 V or $V_{DD}$<br>f = 1 MHz | | 5 | | pF |

## 6.6 Typical Characteristics

At $T_A$ = 25°C (unless otherwise noted).

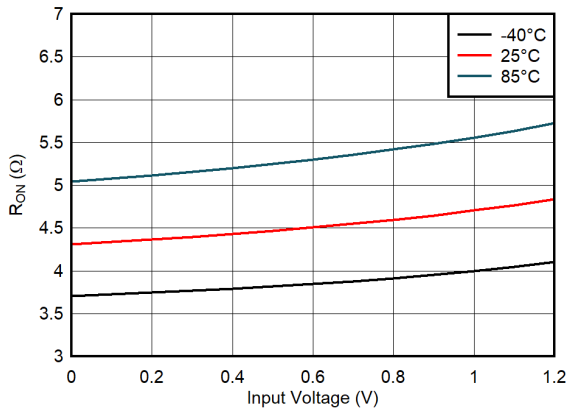



**図 6-1. $R_{ON}$ vs Input Voltage. $V_{DD}$ = 1.5 V**

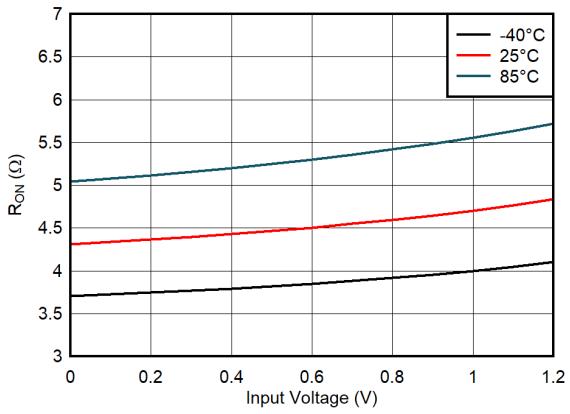



**図 6-2. $R_{ON}$ vs Input Voltage. $V_{DD}$ = 3.3 V**

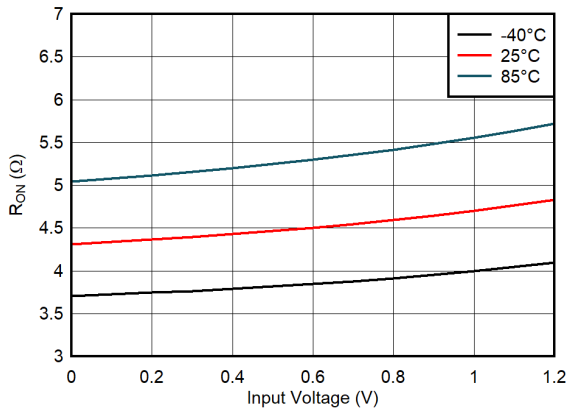



**図 6-3. $R_{ON}$ vs Input Voltage. $V_{DD}$ = 5.5 V**

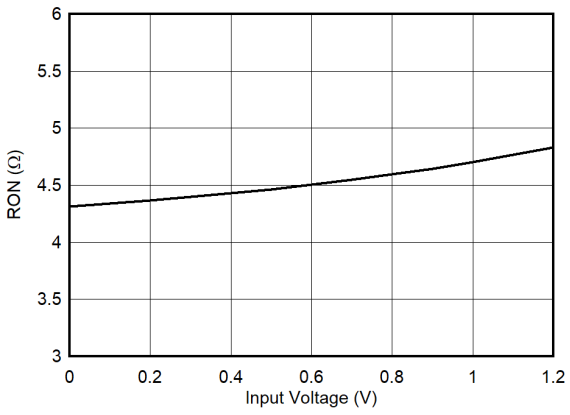



**図 6-4. $R_{ON}$ vs Input Voltage, $V_{DD}$ = 1.5 V to 5.5 V**

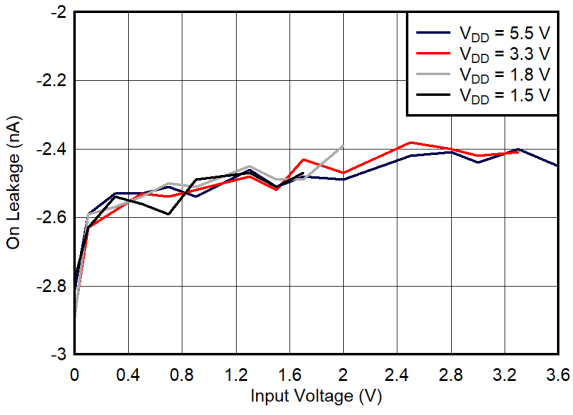



**図 6-5. On-Leakage vs Input Voltage**

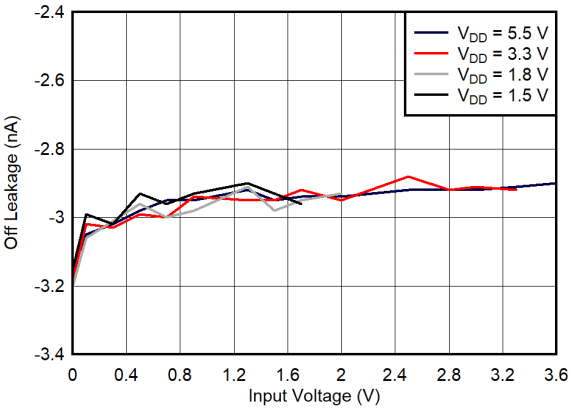



**図 6-6. Off-Leakage vs Input Voltage**

## 6.6 Typical Characteristics (continued)

At $T_A$ = 25°C (unless otherwise noted).

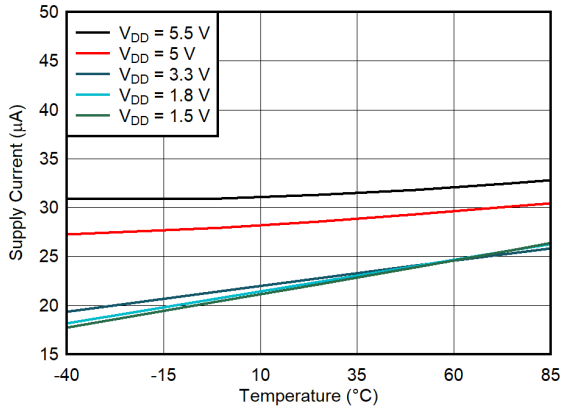



図 6-7. Supply Current vs Temperature

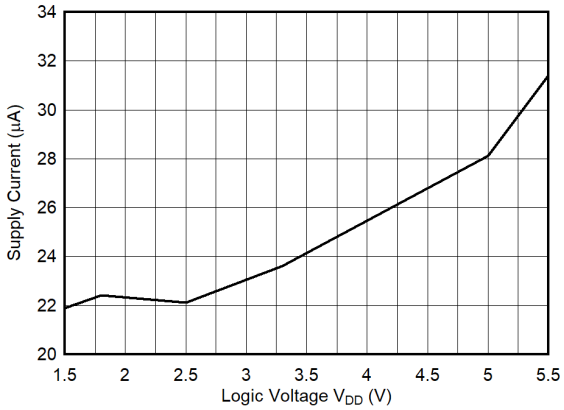



図 6-8. Supply Current vs Logic Voltage

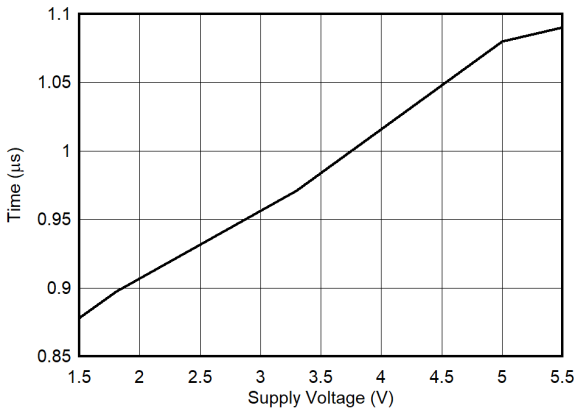



図 6-9. Switching Time ($t_{SWITCH}$) vs Supply Voltage

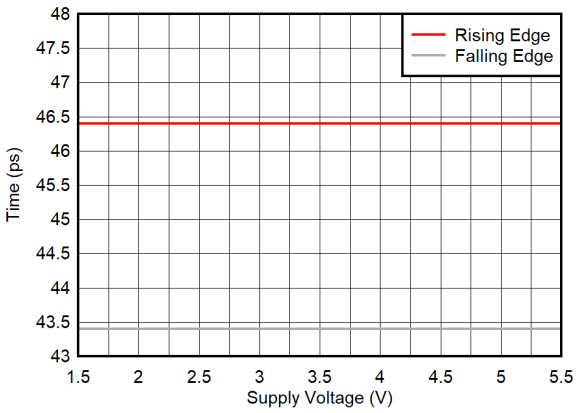



図 6-10. Propagation Delay ($t_{PD}$) vs Supply Voltage

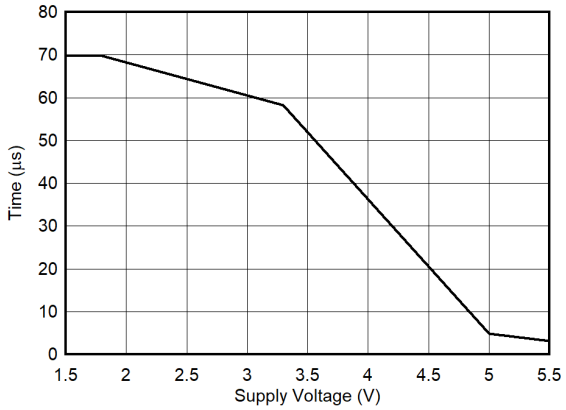



図 6-11. $t_{ON\_VDD}$ vs Supply Voltage

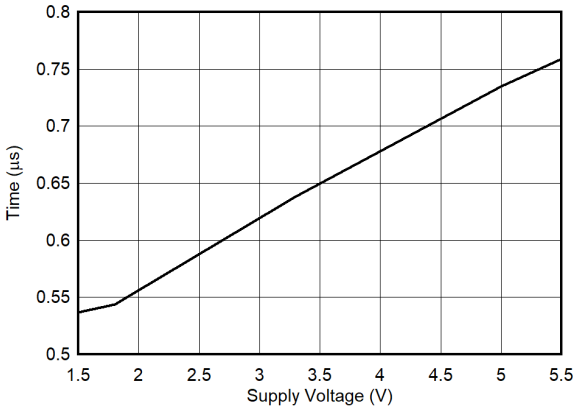



図 6-12. $t_{OFF\_VDD}$ vs Supply Voltage

## 6.6 Typical Characteristics (continued)

At $T_A$ = 25°C (unless otherwise noted).

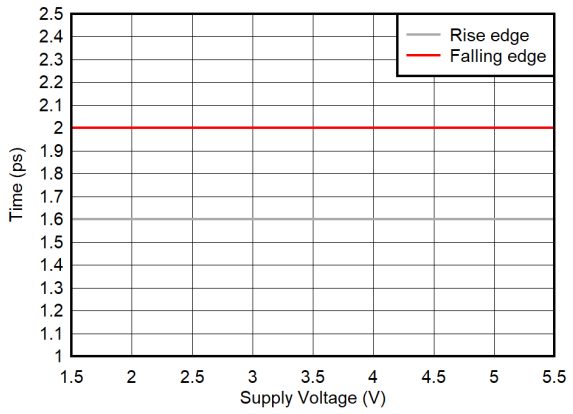



図 6-13. Interpair Skew vs Supply Voltage

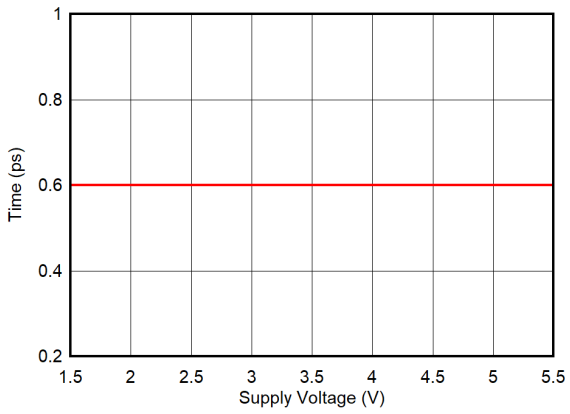



図 6-14. Intrapair Skew vs Supply Voltage

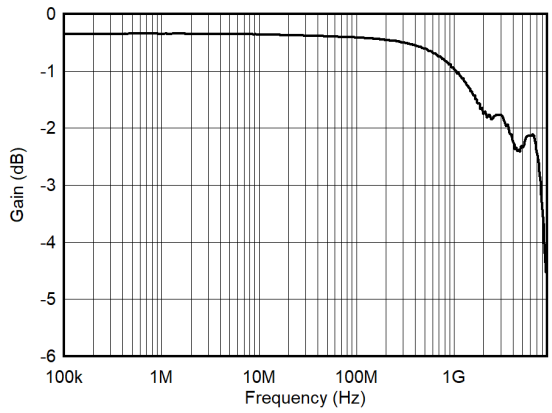



図 6-15. Differential Bandwidth

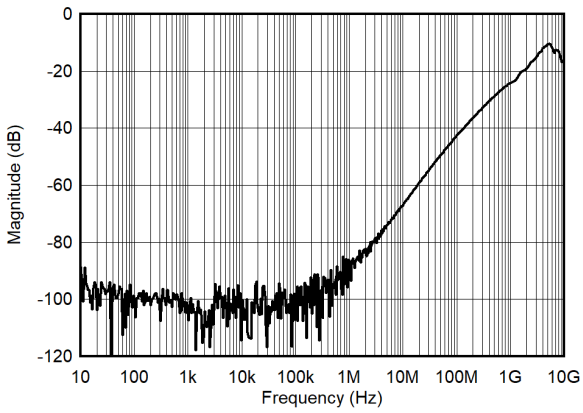



図 6-16. Off Isolation

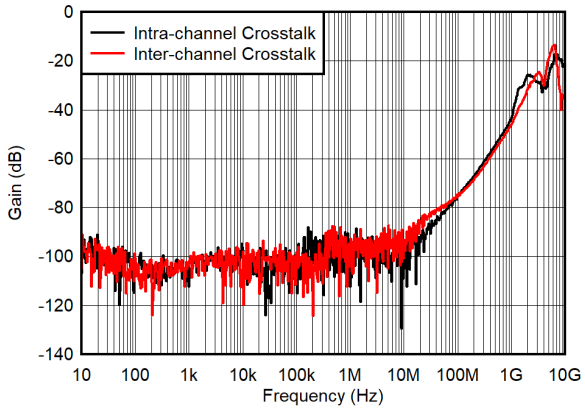



図 6-17. Differential Crosstalk

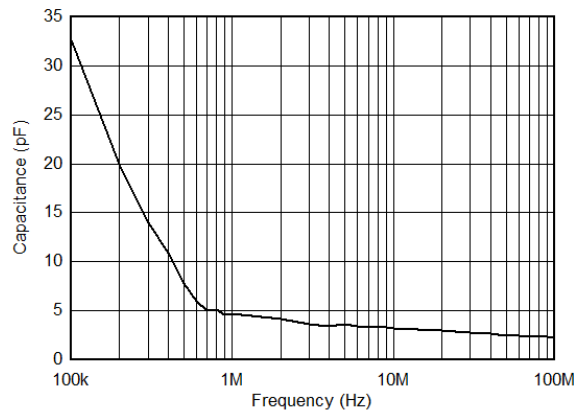



図 6-18. Capacitance vs Frequency

# 7 Parameter Measurement Information

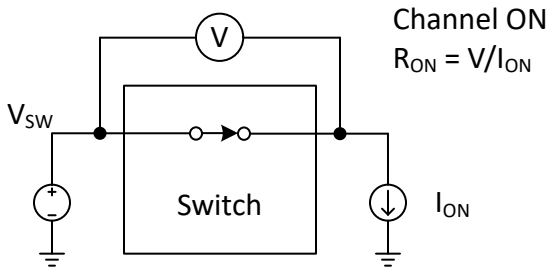



**図 7-1. On Resistance**

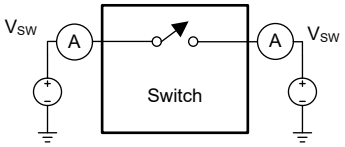



**図 7-2. Off Leakage**

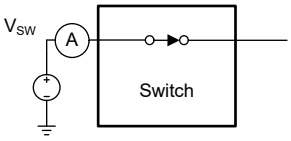
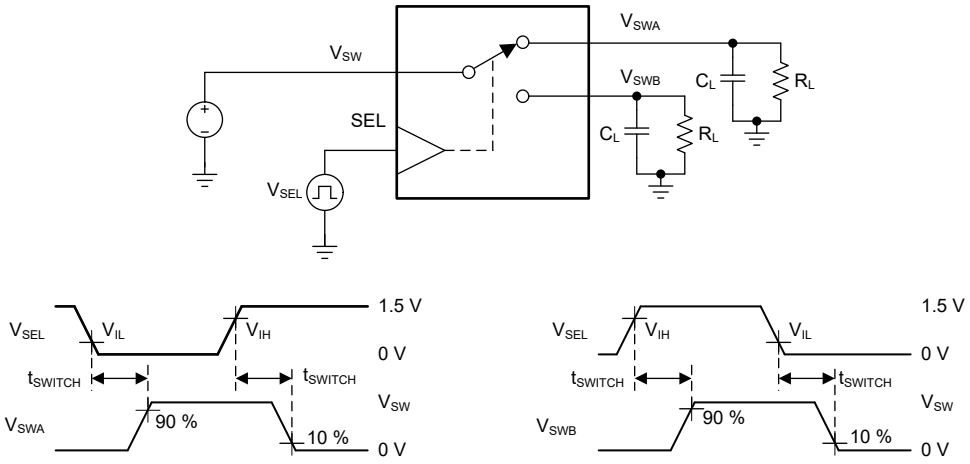
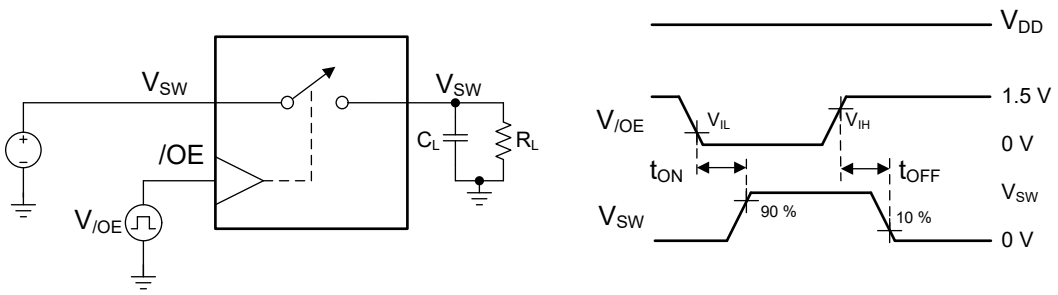



**図 7-3. On Leakage**




A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω , $t_r$ = 3 ns, $t_f$ = 3 ns.
B. $C_L$ includes probe and jig capacitance.

**図 7-4. $t_{SWITCH}$ Timing**




A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω , $t_r$ = 3 ns, $t_f$ = 3 ns.
B. $C_L$ includes probe and jig capacitance.

**図 7-5. $t_{ON}$ and $t_{OFF}$ Timing for $\overline{OE}$**

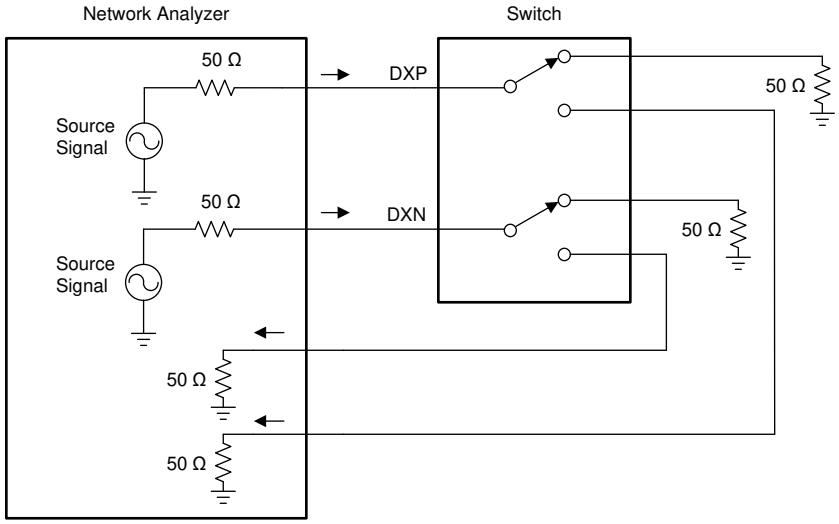





**図 7-6. Off Isolation**

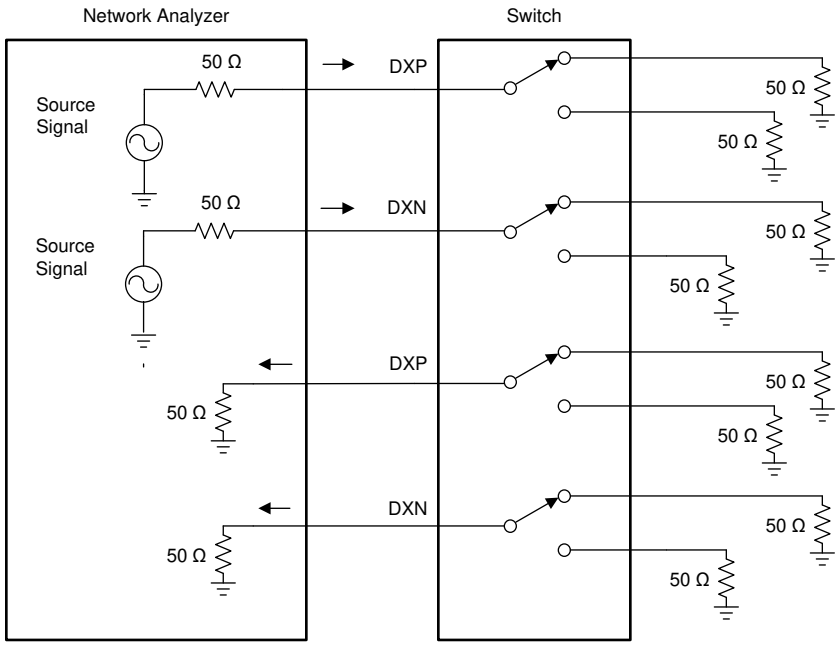





**図 7-7. Crosstalk**

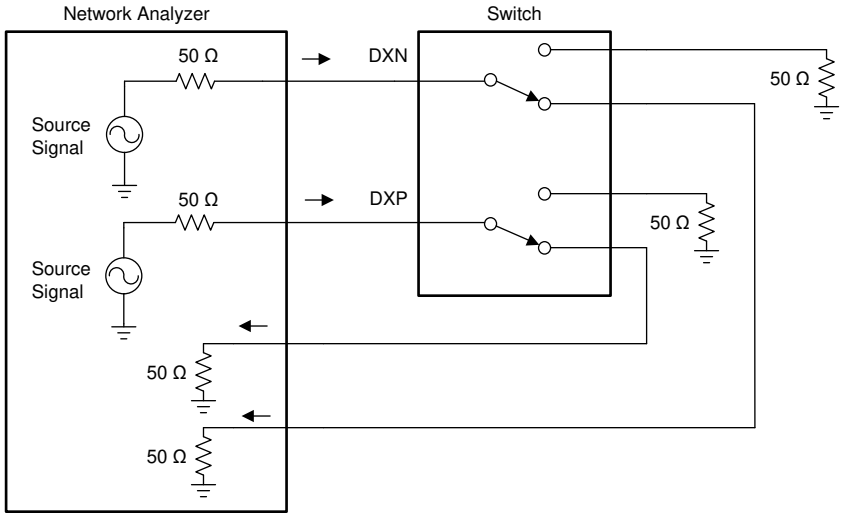





**図 7-8. Bandwidth and Insertion Loss**

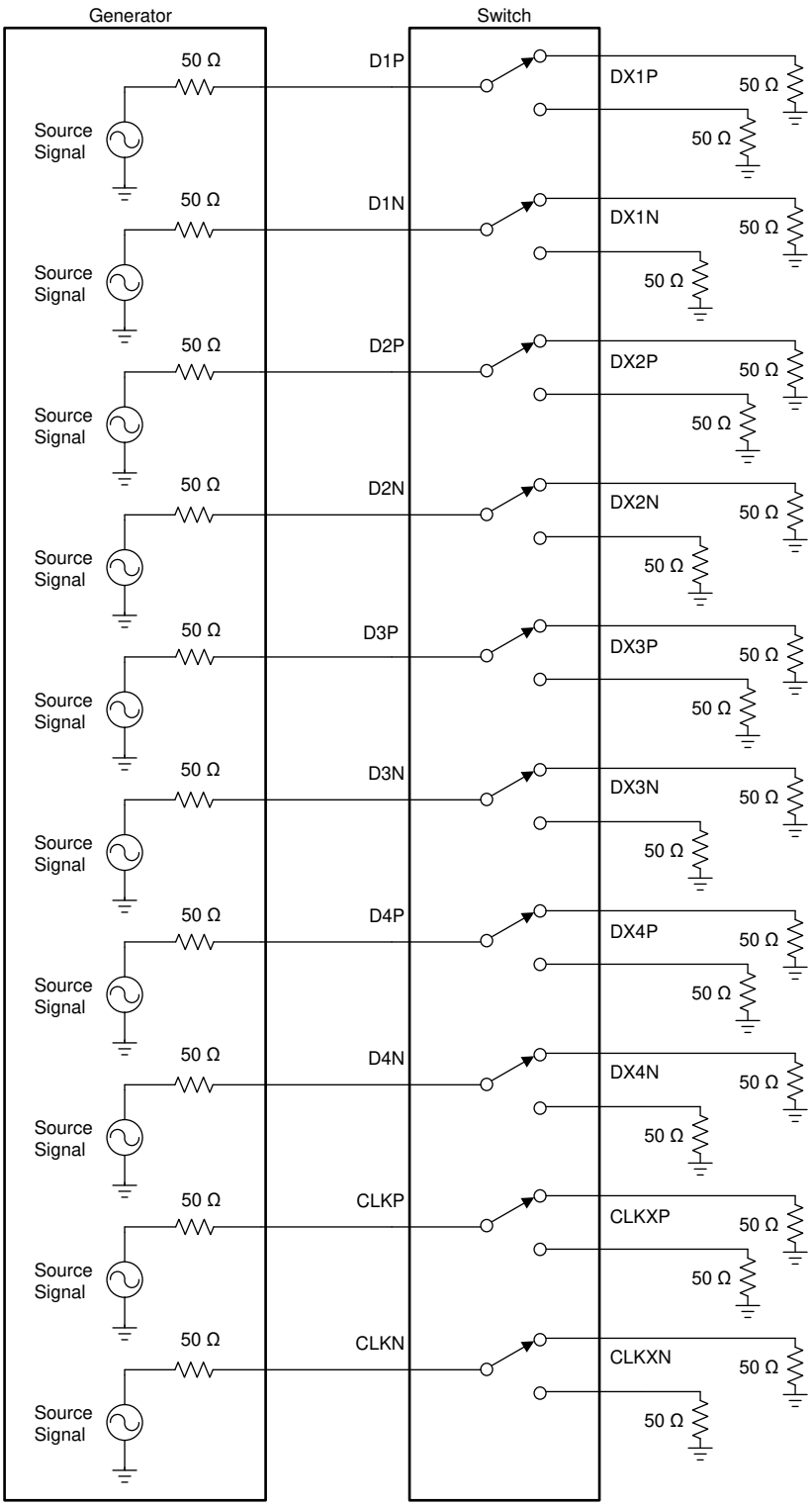
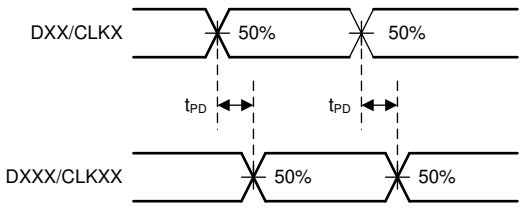


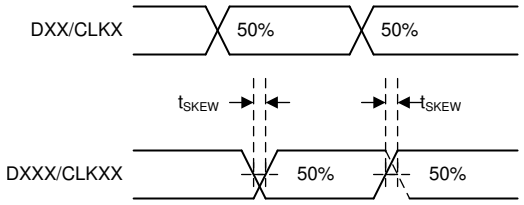



**図 7-9. $t_{PD}$, $t_{SKEW(INTRA)}$ and $t_{SKEW(INTER)}$ Setup**



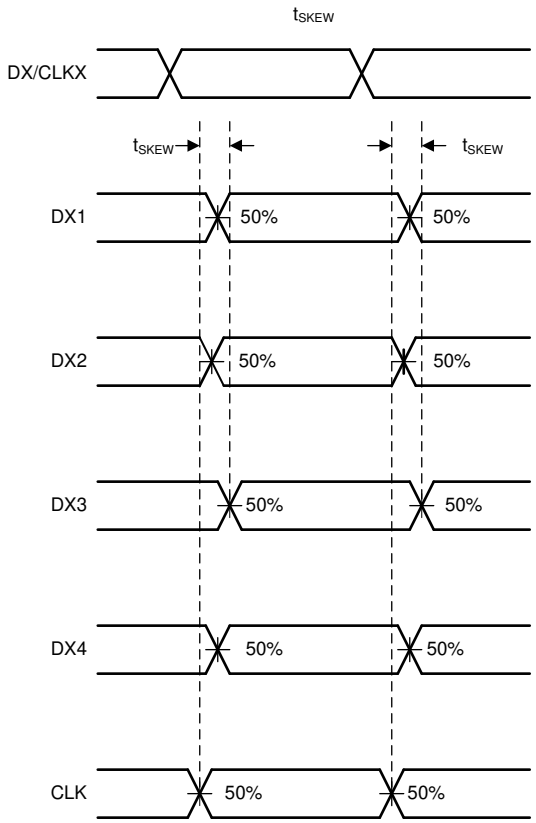

A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω , $t_r$ = 100 ps, $t_f$ = 100 ps.
B. $C_L$ includes probe and jig capacitance.

**図 7-10. $t_{PD}$**



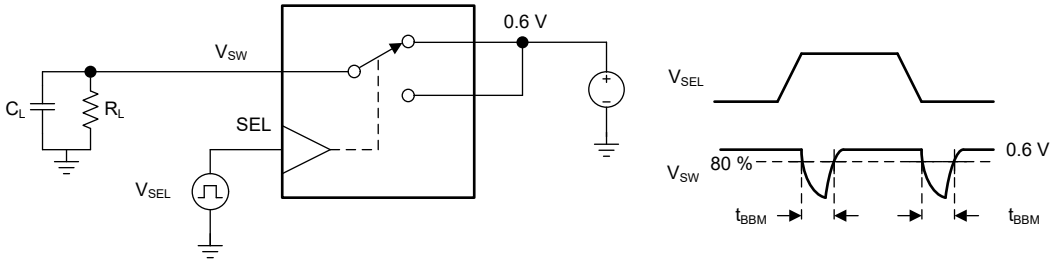

A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω , $t_r$ = 100 ps, $t_f$ = 100 ps.
B. $C_L$ includes probe and jig capacitance.

**図 7-11. $t_{SKEW(INTRA)}$**




A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω , $t_r$ = 100 ps, $t_f$ = 100 ps.
B. $C_L$ includes probe and jig capacitance.
C. $t_{SKEW}$ is the maximum skew between all channels. The diagram exaggerates $t_{SKEW}$ to show the measurement technique.

**図 7-12. $t_{SKEW(INTER)}$**




A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω , $t_r$ = 3 ns, $t_f$ = 3 ns.
B. $C_L$ includes probe and jig capacitance.

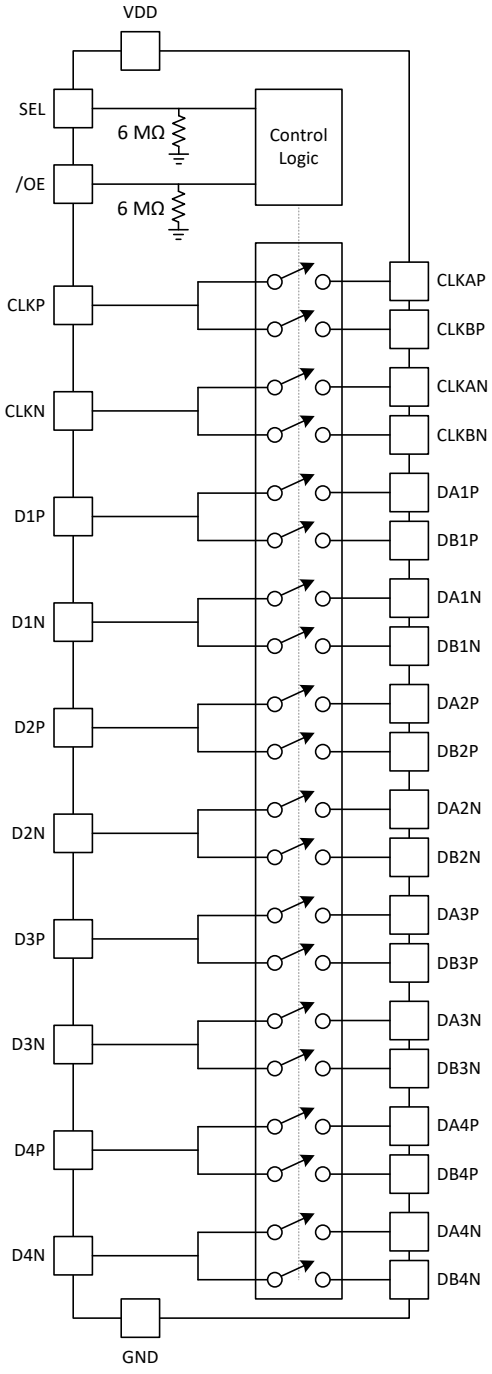
**図 7-13. $t_{BBM}$**

# 8 Detailed Description

## 8.1 Overview

The TMUX646 is a high-speed 4 data lane 2:1 MIPI Switch. The device includes 10 channels (5 differential) with 4 differential data lanes and 1 differential clock lane for D-PHY, CSI or DSI. The clock and data lanes can be interchanged as necessary to facilitate the best layout possible for the application. The switch allows a single MIPI port to interface between two MIPI modules, expanding the number of potential MIPI devices that can be used within a system that is MIPI port limited.

## 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 1.2-V Logic Compatible Inputs

The TMUX646 has 1.2-V logic compatible control inputs. Regardless of the $V_{DD}$ voltage, the 1.2-V logic level inputs allow the TMUX646 to interface with processors that have lower logic I/O rails and eliminates the need for an external voltage translator, which saves both space and BOM cost. For more information on 1.2 V and 1.8 V logic implementations, refer to *Simplifying Design with 1.8 V logic Muxes and Switches.*

### 8.3.2 Bidirectional Operation

The TMUX646 conducts equally well from A to COM, B to COM, COM to A, or COM to B. Each channel has very similar characteristics in both directions and supports analog and digital signals.

### 8.3.3 Powered-Off Protection

When the TMUX646 is powered off ($V_{DD}$ = 0 V) the I/Os and digital logic pins of the device remains in a high impedance state. The crosstalk, off-isolation, and leakage will remain within the electrical specifications. This prevents errant voltages from reaching the rest of the system and maintains isolation when the system is powering up:

図 8-1 shows an example system containing a switch without powered-off protection with the following system level scenario.

1. Subsystem A powers up and starts sending information to Subsystem B that remains unpowered.
2. The I/O voltage back powers the supply rail in Subsystem B.
3. The digital logic is back powered and turns on the switch. The signal is transmitted to Subsystem B before it is powered and damages it.

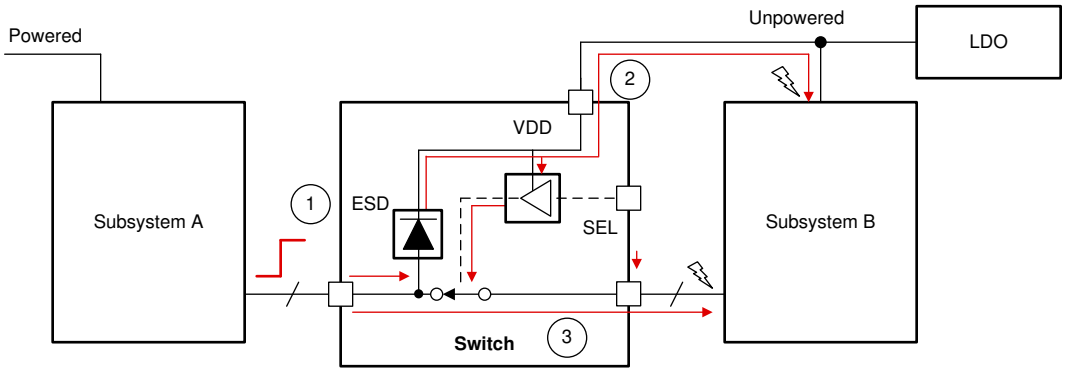



**図 8-1. System Without Powered-Off Protection**

With powered-off protection, the switch prevents back powering the supply and the switch remains high-impedance. Subsystem B remains protected.

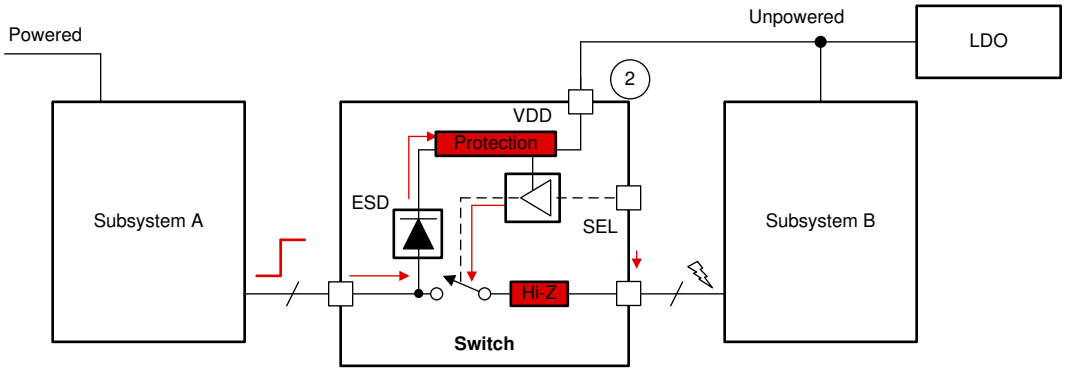



**図 8-2. System With Powered-Off Protection**

This features has the following system level benefits:

- Protects the system from damage.
- Prevents data from being transmitted unintentionally.
- Eliminates the need for power sequencing solutions, reducing BOM count and cost, simplifying system design, and improving reliability.

### 8.3.4 Low Power Disable Mode

The TMUX646 has a low power mode that places all the signal paths in a high impedance state and lowers the current consumption while the device is not in use. To put the device in low power mode and disable the switch, the output enable pin $\overline{OE}$ must be supplied with a logic high signal.

## 8.4 Device Functional Modes

### 8.4.1 Pin Functions

The SEL and $\overline{OE}$ pins have a weak 6-MΩ pull-down to prevent floating input logic.

**表 8-1. Function Table**

| $\overline{OE}$ | SEL | Function |
|---|---|---|
| H | X | I/O pins High-Impedance |
| L | L | CLK(P/N) = CLKA(P/N) |
| | | Dn(P/N) = DAn(P/N) |
| L | H | CLK(P/N) = CLKB(P/N) |
| | | Dn(P/N) = DBn(P/N) |

### 8.4.2 Low Power Disable Mode

While the output enable pin $\overline{OE}$ is supplied with a logic high, the device remains in the low power disabled state. This reduces the current consumption substantially and the switches are high impedance. The SEL pin is ignored while the $\overline{OE}$ remains high. Upon exiting low power mode, the switch status reflects the SEL pin as seen in 表 8-1.

### 8.4.3 Switch Enabled Mode

While the output enable pin $\overline{OE}$ is supplied with a logic low, the device remains in switch enabled mode.

# 9 Application and Implementation

**Note**

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

## 9.1 Application Information

The TMUX646 is a 2:1, 10 channel MIPI switch designed to facilitate multiple MIPI compliant devices to connect to a single CSI/DSI, C-PHY/D-PHY module.

## 9.2 Typical Application

図 9-1 represents a typical application of the TMUX646 MIPI switch. The TMUX646 is used to switch signals between multiple MIPI modules and a single MIPI port on a processor. This expands the capabilities of a single port to handle multiple MIPI modules.

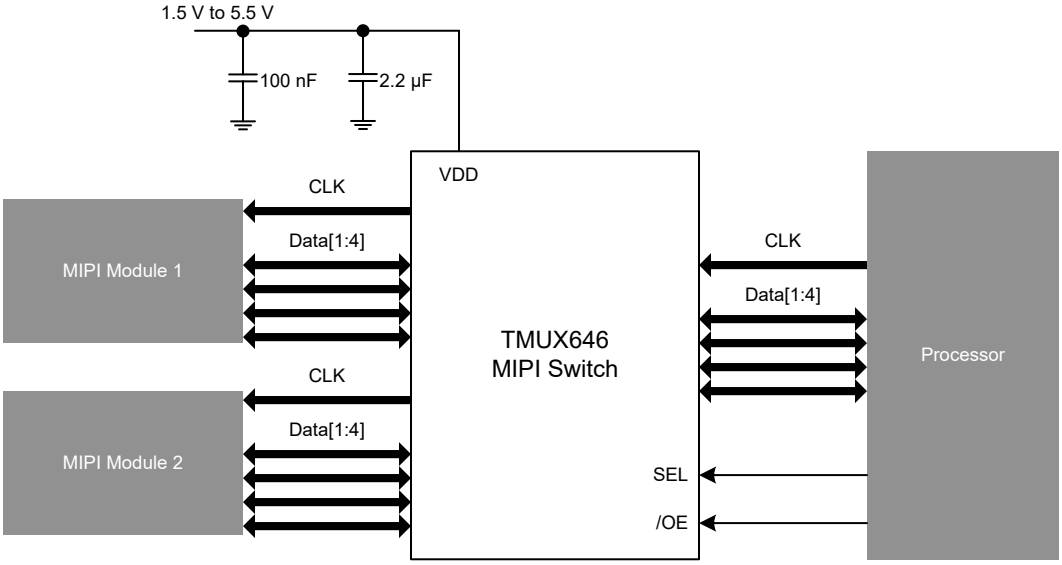



**図 9-1. Typical D-PHY Application**

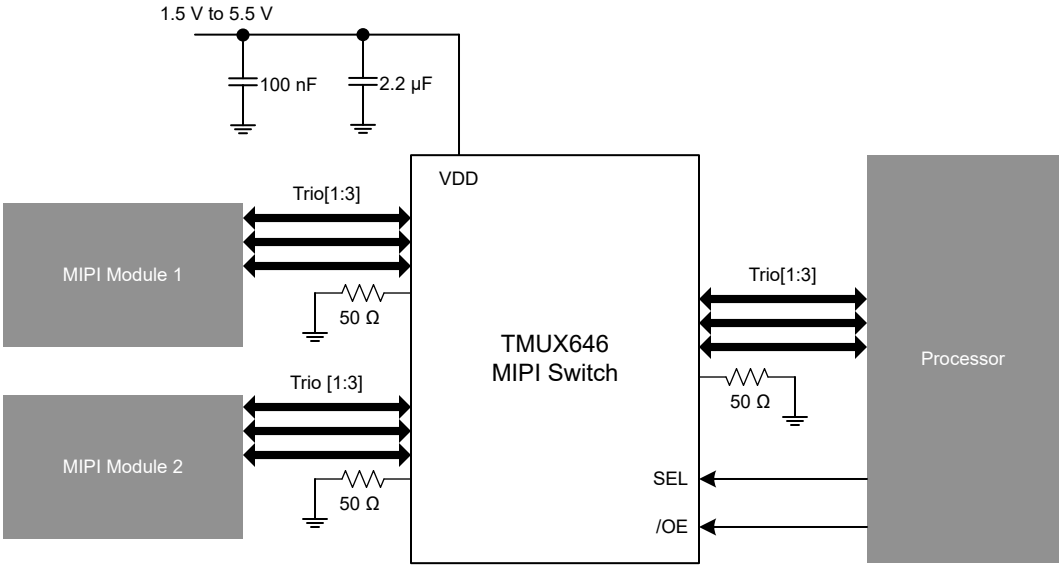



**図 9-2. Typical C-PHY Application**

### 9.2.1 Design Requirements

Design requirements of the MIPI standard must be followed. Supply pin decoupling capacitors of 2.2 µF and 100 nF are recommended for best performance. The TMUX646 has internal 6-MΩ pulldown resistors on SEL and $\overline{OE}$. The pulldown on these pins ensure that the digital remains in a non-floating state during system power-up to prevent shoot through current spikes and an unknown switch status. By default the switch will power up enabled and with the A path selected until driven externally by the processor.

### 9.2.2 Detailed Design Procedure

The TMUX646 can be properly operated without any external components. However, TI recommends that unused I/O signal pins be connected to ground through a 50 Ω resistor to prevent signal reflections and maintain device performance. The NC pins of the device do not require any external connections or terminations and have no connection to the rest of the device internally.

The clock and data lanes can be interchanged as necessary to facilitate the best layout possible for the application. For example, the clock can be placed on the D1 channel and a data lane can be used on the CLK channel if this improves the layout. In addition, the signal lines of the TMUX646 are routed single ended on the chip die. This makes the device suitable for differential and single-ended high-speed systems.

#### *9.2.2.1 MIPI D-PHY Application*

The clock and data lanes can be interchanged as necessary to facilitate the best layout possible for the application. In addition, the signal lines of the TMUX646 are routed single ended on the chip die. This makes the device suitable for differential and single-ended high-speed systems. This also allows the positive and negative lines to be interchanged as necessary to facilitate the best layout possible for the application.

D-PHY application includes a differential clock and 4 differential data lanes. All the channels of the device perform similar and the clock or data signals can be interchanged as necessary to facilitate the best layout possible for the application.

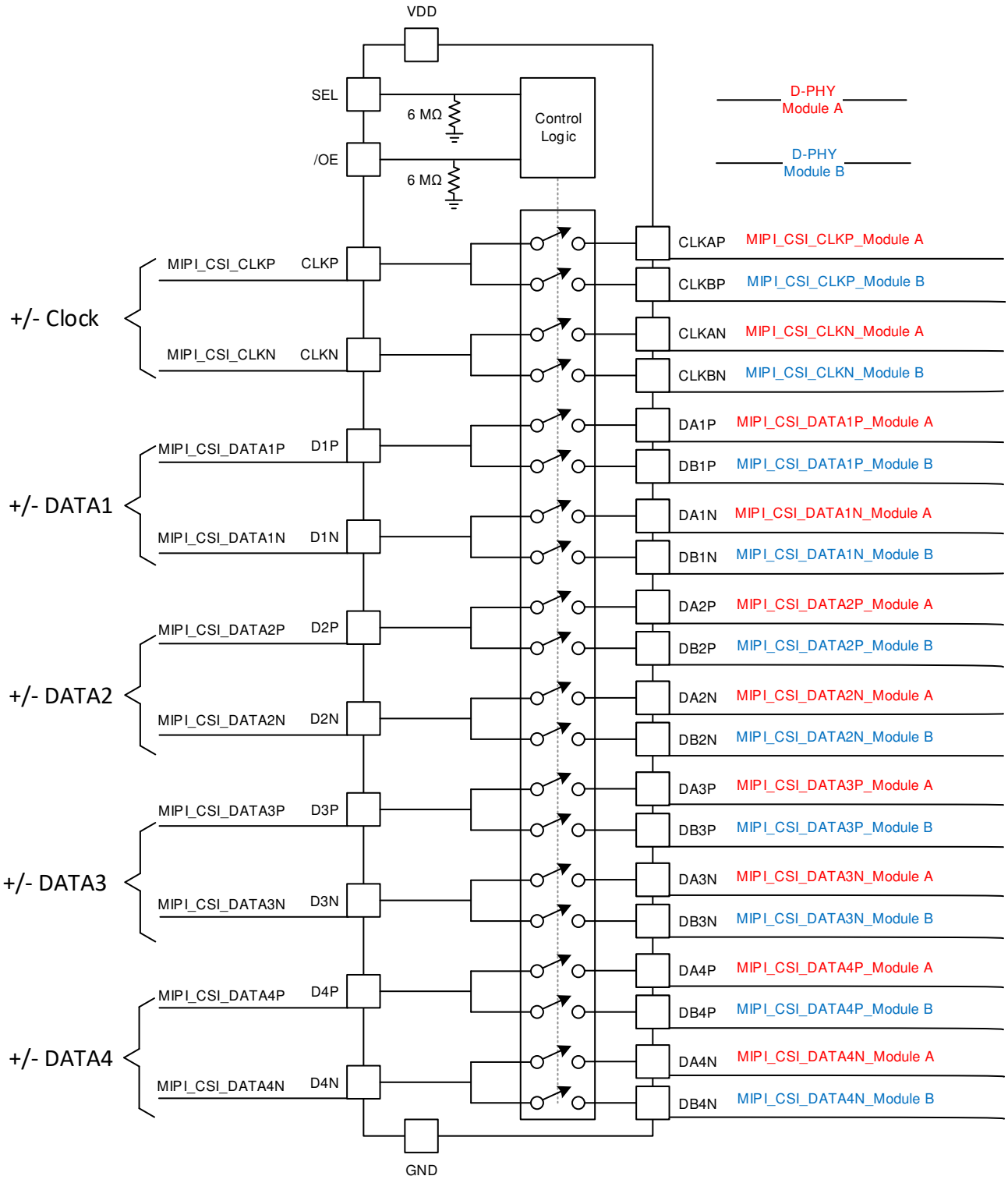



**図 9-3. MIPI D-PHY Example Pinout**

#### 9.2.2.2 MIPI C-PHY Application

The clock and data lanes can be interchanged as necessary to facilitate the best layout possible for the application. In addition, the signal lines of the TMUX646 are routed single ended on the chip die. This makes the device suitable for differential and single-ended high-speed systems. This also allows the positive and negative lines to be interchanged as necessary to facilitate the best layout possible for the application.

C-PHY application includes 3 trios of signals, which may be routed on any channel, which means there will be one unused channel on the TMUX646. TI recommends that the unused I/O signal pin be connected to ground through a 50 Ω resistor to prevent signal reflections and maintain device performance.

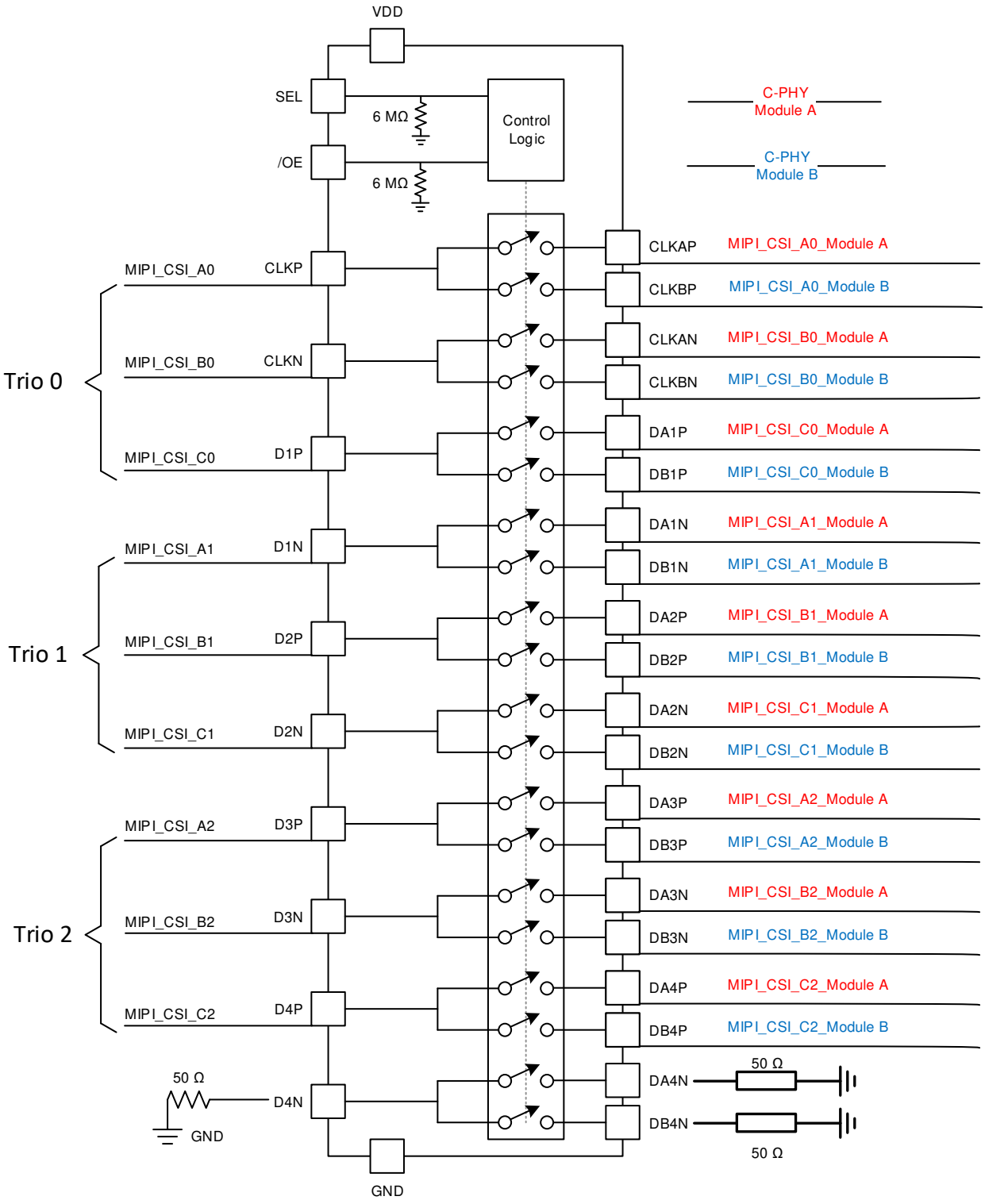



**図 9-4. MIPI C-PHY Example Pinout**

### 9.2.3 Application Curves

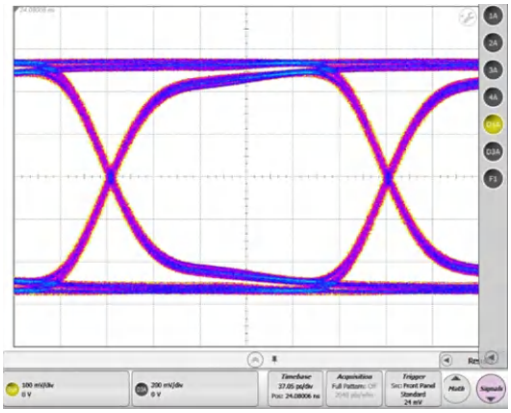


図 9-5. 4.5 Gbps Through Path (500-$mV_{pp}$)

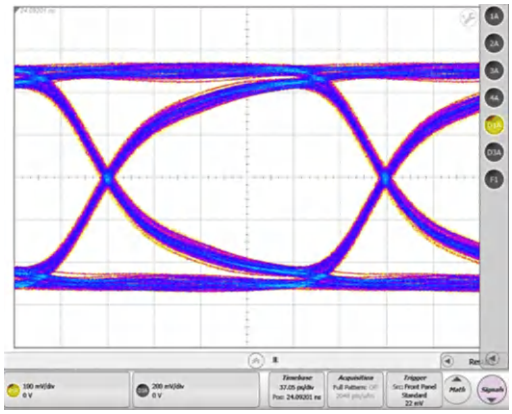


図 9-6. 4.5 Gbps with TMUX646 (500-$mV_{pp}$)

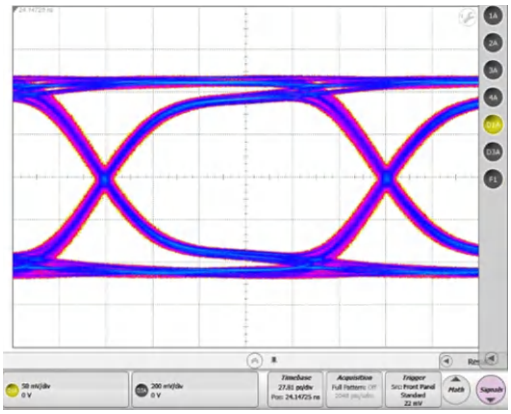


図 9-7. 6 Gbps Through Path (200-$mV_{pp}$)

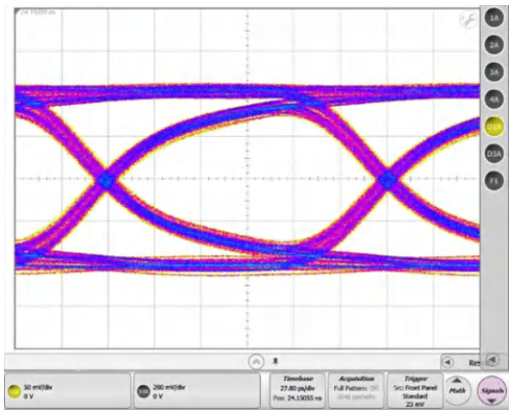


図 9-8. 6 Gbps with TMUX646 (200-$mV_{pp}$)

## 10 Power Supply Recommendations

When the TMUX646 is powered off ($V_{DD}$ = 0 V), the I/Os of the device remains in a high-Z state. The crosstalk, off-isolation, and leakage remain within the electrical characteristics セクション 6. Power to the device is supplied through the VDD pin. Decoupling capacitors of 100 nF and 2.2 µF are recommended on the supply.

# 11 Layout

## 11.1 Layout Guidelines

Place the supply de-coupling capacitors as close to the VDD and GND pin as possible. The spacing between the power traces, supply and ground, and the signal I/O lines, clock and data, should be a minimum of three times the race width of the signal I/O lines to maintain signal integrity.

The characteristic impedance of one or more traces must match that of the receiver and transmitter to maintain signal integrity. Route the high-speed traces using a minimum amount of vias and corners. This will reduce the amount of impedance changes.

When it becomes necessary to make the traces turn 90°, use two 45° turns or an arc instead of making a single 90° turn.

Do not route high-speed traces near crystals, oscillators, external clock signals, switching regulators, mounting holes or magnetic devices.

Avoid stubs on the signal lines.

All I/O signal traces should be routed over a continuous ground plane with no interruptions. The minimum width from the edge of the trace to any break in the ground plane must be 3 times the trace width. When routing on PCB inner signal layers, the high speed traces should be between two ground planes and maintain characteristic impedance.

High speed signal traces must be length matched as much as possible to minimize skew between data and clock lines.

## 11.2 Layout Example

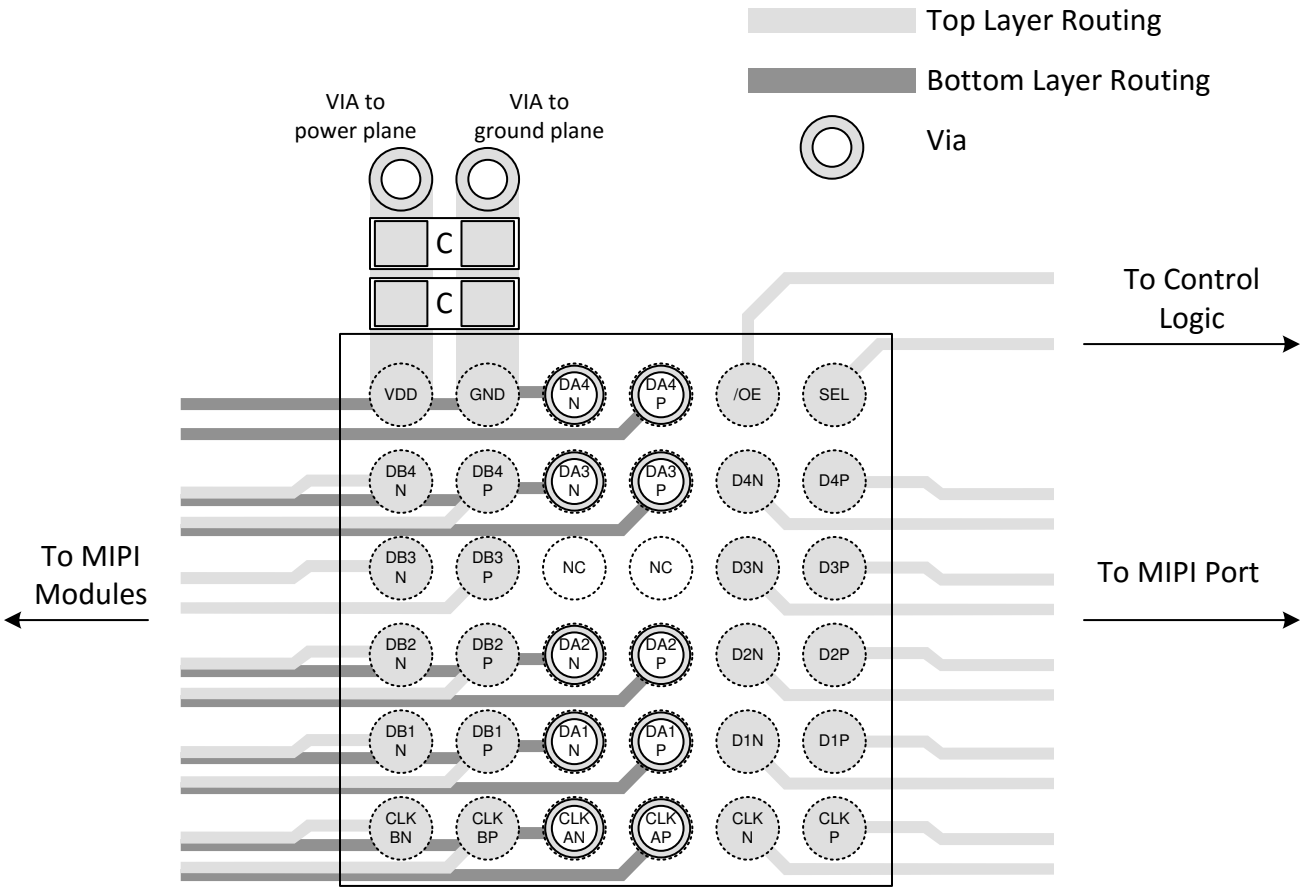



**図 11-1. Layout Example**

# 12 Device and Documentation Support

## 12.1 Documentation Support

### 12.1.1 Related Documentation

See the following for related documenation:

- Texas Instruments, *1.8 V Logic for Muxes and Signal Switches* application brief
- Texas Instruments, *High-Speed Interface Layout Guidelines* application report
- Texas Instruments, *High-Speed Layout Guidelines* application report
- Texas Instruments, *Multiplexers and Signal Switches Glossary* application report
- Texas Instruments, *nFBGA Packaging* application report
- Texas Instruments, *Small Body nFBGA Packages* application report

## 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 12.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

## 12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

## 12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 12.6 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TMUX646NZECR | Active | Production | NFBGA (ZEC) \| 36 | 2500 \| LARGE T&R | Yes | SNAGCU | Level-2-260C-1 YEAR | -40 to 85 | T646 |
| TMUX646NZECR.A | Active | Production | NFBGA (ZEC) \| 36 | 2500 \| LARGE T&R | Yes | SNAGCU | Level-2-260C-1 YEAR | -40 to 85 | T646 |
| TMUX646ZECR | Active | Production | NFBGA (ZEC) \| 36 | 2500 \| LARGE T&R | Yes | SNAGCU | Level-2-260C-1 YEAR | -40 to 85 | T646 |
| TMUX646ZECR.A | Active | Production | NFBGA (ZEC) \| 36 | 2500 \| LARGE T&R | Yes | SNAGCU | Level-2-260C-1 YEAR | -40 to 85 | T646 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

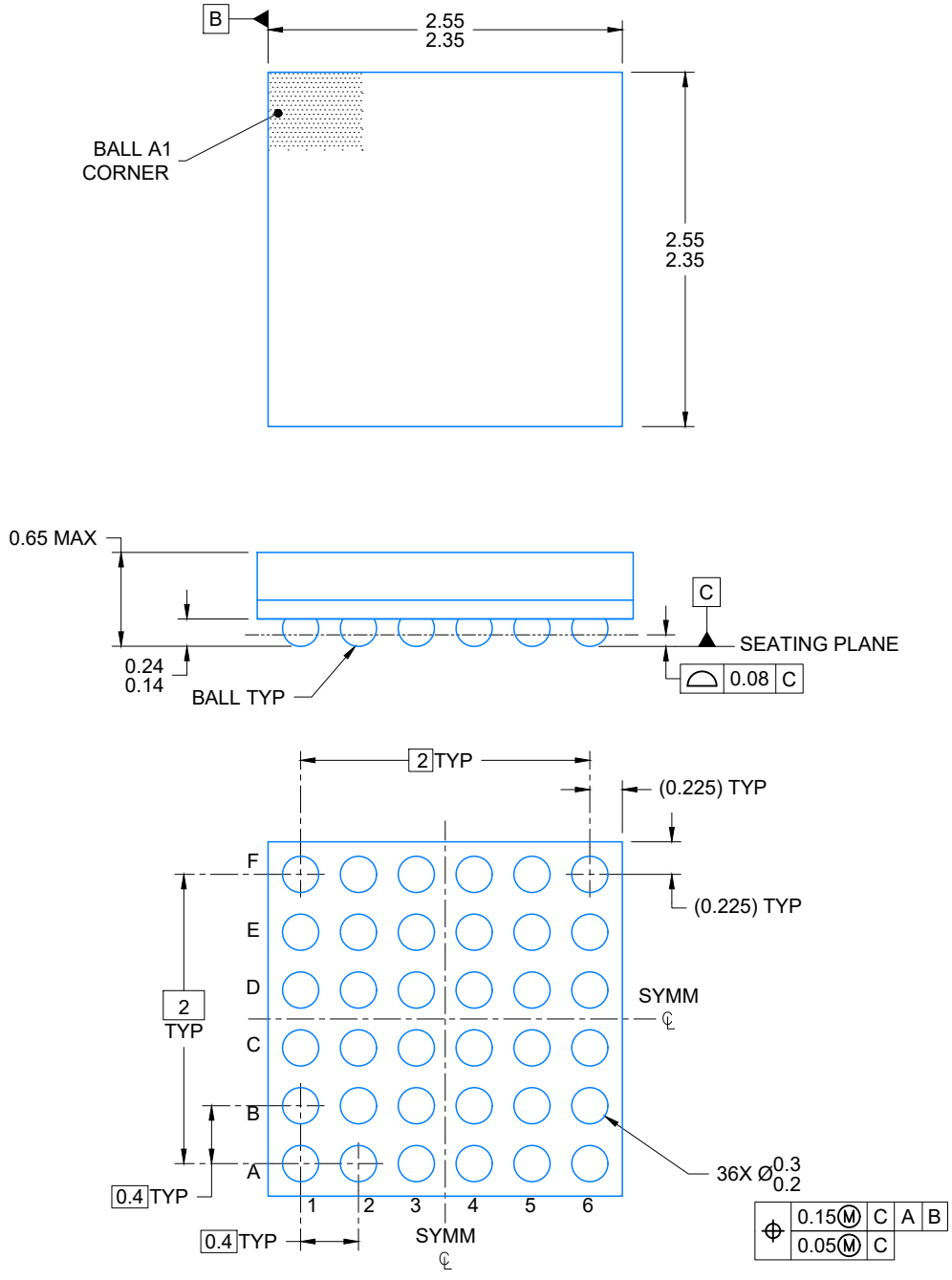
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

# PACKAGE OUTLINE

## ZEC0036A

## NFBGA - 0.65 mm max height

PLASTIC BALL GRID ARRAY

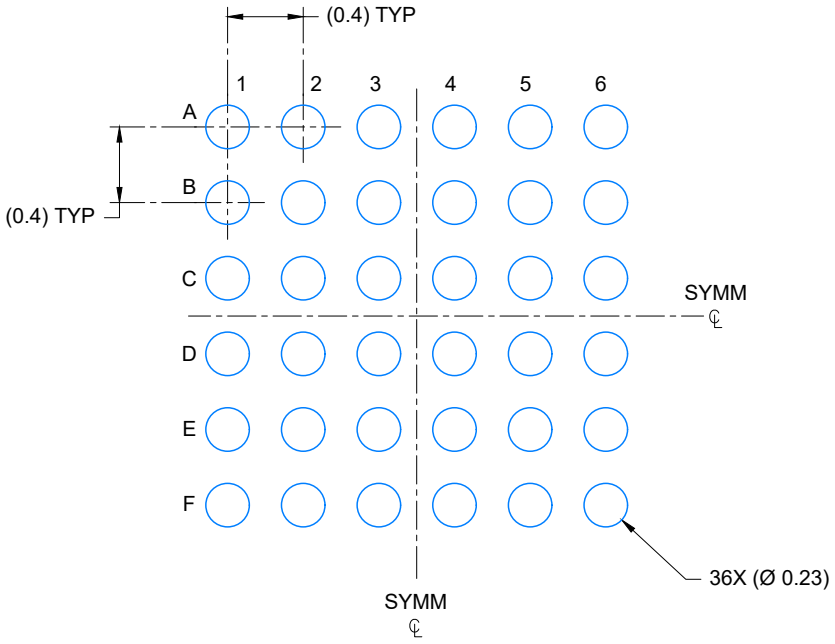



4226214/A 09/2020

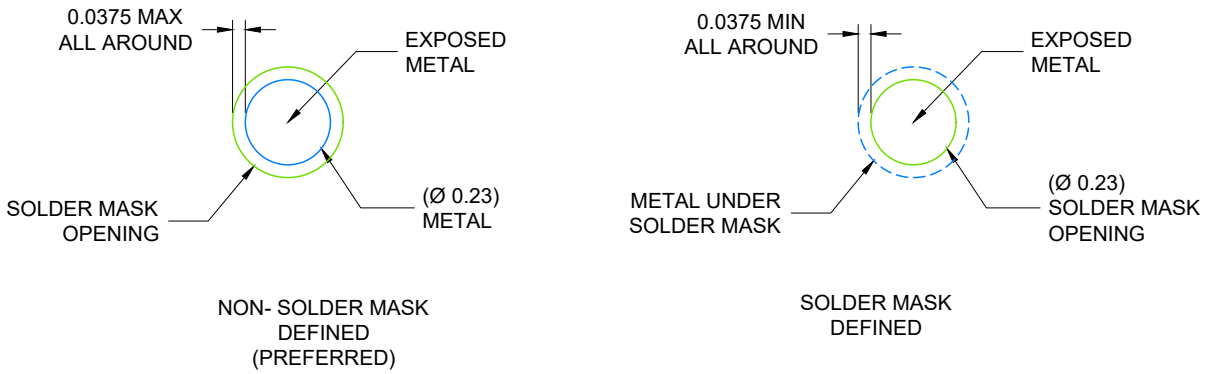
NOTES:

NanoFree is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

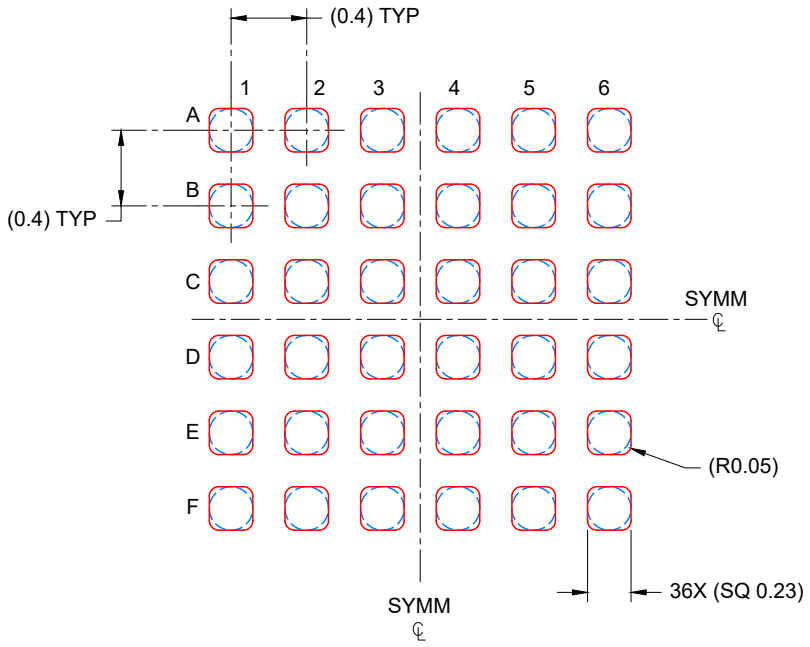



SOLDER MASK DETAILS
NOT TO SCALE

4226214/A 09/2020

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature number SNVA009 (www.ti.com/lit/snva009).




SOLDER PASTE EXAMPLE
BASED ON 0.100 mm THICK STENCIL
SCALE: 25X

4226214/A 09/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

# 重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件 、 TI の総合的な品質ガイドライン 、 ti.com または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。 TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。



最終更新日：2025 年 10 月