TMUX6136 ±16.5V、低静電容量、低リーク電流の高精度デュアル SPDT スイッチ

1 特長

- 広い電源電圧範囲:±5V～±16.5V (デュアル)、10V～16.5V (シングル)
- すべてのピンで、JESD78 Class II Level A 準拠の 100mA を満たすラッチアップ性能
- 小さいオン容量:5.5pF
- 低い入力リーク:0.5pA
- 少ない電荷注入:-0.4pC
- レール・ツー・レール動作
- 低オン抵抗:120Ω
- 高速な遷移時間:66ns
- ブレイク・ビフォー・メイクの切り替え動作
- SELx ピンを内蔵プルダウンにより V_{DD} に接続可能
- ロジック・レベル:2V～V_{DD}
- 低消費電流:17µA
- 人体モデル (HBM) ESD 保護:すべてのピンで ±2kV
- 業界標準の TSSOP パッケージ

2 アプリケーション

- ファクトリ・オートメーションと産業プロセス制御
- プログラマブル・ロジック・コントローラ (PLC)
- アナログ入力モジュール
- ATE 試験装置
- デジタル・マルチメータ
- バッテリ・モニタリング・システム

3 概要

TMUX6136 は、独立して選択可能な 2 つの SPDT スイッチを備えた相補型金属酸化膜半導体 (CMOS) アナログ・スイッチです。このデバイスは、デュアル電源 (±5V～±16.5V)、シングル電源 (10V～16.5V)、非対称電源のいずれでも正常に動作します。デジタル選択ピン (SELx) は、スレッショルドが TTL (Transistor-Transistor Logic) 互換で、TTL/CMOS ロジックの互換性が保証されます。

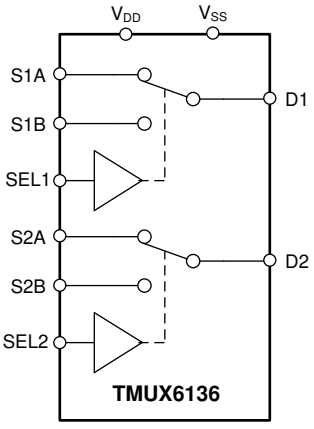
TMUX6136 は 2 つの入力 (Sx) の 1 つを、SELx ピンのステータスに応じて、共通の出力 (D) に切り替えます。各スイッチはオン位置において、どちらの方向にも同程度に導電性が高く、電源電圧までの入力信号範囲をサポートします。オフ状態では、電源電圧までの信号レベルがブロックされます。すべてのスイッチは、Break-Before-Make (BBM) スイッチング動作を行います。

TMUX6136 は、テキサス・インスツルメンツの高精度スイッチおよびマルチプレクサ・ファミリの製品です。このデバイスはリーク電流と電荷注入が非常に小さいため、高精度の測定アプリケーションに使用可能です。また、このデバイスはスイッチがオフ位置のとき、電源電圧までの信号レベルをブロックすることで、絶縁性能も非常に優れています。消費電流が 17µA と小さいため、携帯用アプリケーションで使用できます。

パッケージ情報 (1)

部品番号	パッケージ	本体サイズ (公称)
TMUX6136	PW (TSSOP、16)	5.00mm × 4.40mm

(1) 利用可能なパッケージについては、データシートの末尾にあるパッケージ・オプションについての付録を参照してください。



概略回路図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (November 2018) to Revision A (October 2022)	Page
• 文書全体にわたって表、図、相互参照の採番方法を更新	1
• Updated the *Transition-Time Measurement Setup* figure	13

5 Pin Configuration and Functions

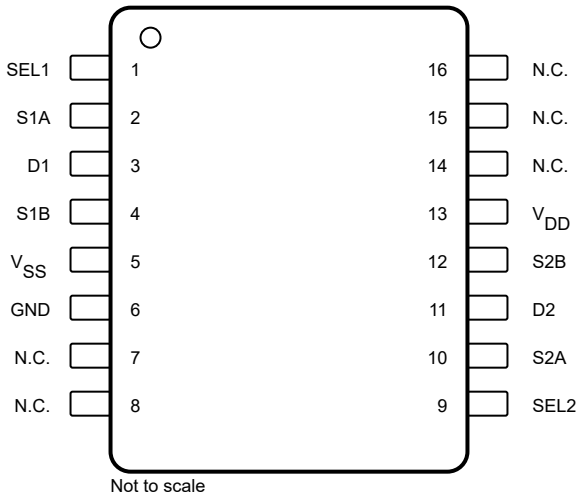


図 5-1. PW Package, 16-Pin TSSOP (Top View)

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
SEL1	1	I	Select line 0
S1A	2	I/O	Source pin 1A. Can be an input or output.
D1	3	I/O	Drain pin D1. Can be an input or output.
S1B	4	I/O	Source pin 1B. Can be an input or output.
V_{SS}	5	P	Negative power supply. This pin is the most negative power-supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{SS} and GND.
GND	6		Ground (0 V) reference
N.C.	7, 8, 14, 15, 16	No Connect	No internal connection
SEL2	9	I	Select line 1
S2A	10	I/O	Source pin 2A. Can be an input or output.
D2	11	I/O	Drain pin D2. Can be an input or output.
S2B	12	I/O	Source pin 2B. Can be an input or output.
V_{DD}	13	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{DD} and GND.

(1) I = input, O = output, P = power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD} to V_{SS}	Supply voltage		36	V
V_{DD} to GND		–0.3	18	V
V_{SS} to GND		–18	0.3	V
V_{DIG}	Digital input pin (SEL1, SEL2) voltage	GND –0.3	V_{DD}+0.3	V
I_{DIG}	Digital input pin (SEL1, SEL2) current	–30	30	mA
V_{ANA_IN}	Analog input pin (Sx) voltage	V_{SS}–0.3	V_{DD}+0.3	V
I_{ANA_IN}	Analog input pin (Sx) current	–30	30	mA
V_{ANA_OUT}	Analog output pin (D) voltage	V_{SS}–0.3	V_{DD}+0.3	V
I_{ANA_OUT}	Analog output pin (D) current	–30	30	mA
T_A	Ambient temperature	–55	140	°C
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Thermal Information

THERMAL METRIC(1)		TMUX6136 PW (TSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	111.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	41.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	57.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	56.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD} to V_{SS} (1)	Power supply voltage differential	10		33	V
V_{DD} to GND	Positive power supply voltage (singlle supply, V_{SS} = 0 V)	10		16.5	V
V_{DD} to GND	Positive power supply voltage (dual supply)	5		16.5	V
V_{SS} to GND	Negative power supply voltage (dual supply)	–16.5		–5	V
V_S (1)	Source pins voltage	V_{SS}		V_{DD}	V
V_D	Drain pin voltage	V_{SS}		V_{DD}	V
V_{DIG}	Digital input pin (SEL1, SEL2) voltage	0		V_{DD}	V
I_{CH}	Channel current (T_A = 25°C)	–25		25	mA
T_A	Ambient temperature	–40		125	°C

(1) V_{DD} and V_{SS} can be any value as long as 10 V ≤ (V_{DD} – V_{SS}) ≤ 33 V.

6.5 Electrical Characteristics (Dual Supplies: ±15 V)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = -15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
V_A	Analog signal range		T_A = –40°C to +125°C	V_{SS}		V_{DD}	V
R_{ON}	On-resistance	V_S = 0 V, I_S = 1 mA			120	135	Ω
		V_S = ±10 V, I_S = 1 mA			140	160	Ω
			T_A = –40°C to +85°C			210	Ω
			T_A = –40°C to +125°C			245	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = ±10 V, I_S = 1 mA			2.5	6	Ω
			T_A = –40°C to +85°C			9	Ω
			T_A = –40°C to +125°C			11	Ω
R_{ON_FLAT}	On-resistance flatness	V_S = –10 V, 0 V, +10 V, I_S = 1 mA			23	33	Ω
			T_A = –40°C to +85°C			35	Ω
			T_A = –40°C to +125°C			37	Ω
R_{ON_DRIFT}	On-resistance drift	V_S = 0 V			0.42		%/°C
$I_{S(OFF)}$	Source off leakage current(1)	Switch state is off, V_S = +10 V/ –10 V, V_D = –10 V/ + 10 V		–0.05	0.005	0.05	nA
		Switch state is off, V_S = +10 V/ –10 V, V_D = –10 V/ + 10 V	T_A = –40°C to +85°C	–0.17		0.1	nA
		Switch state is off, V_S = +10 V/ –10 V, V_D = –10 V/ + 10 V	T_A = –40°C to +125°C	–1		0.25	nA
$I_{D(ON)}$	Drain on leakage current	Switch state is on, V_S = +10 V/ –10 V, V_D = –10 V/ +10 V		–0.06	0.008	0.06	nA
			T_A = –40°C to +85°C	–0.25		0.15	nA
			T_A = –40°C to +125°C	–1.6		0.4	nA
DIGITAL INPUT (SELx pins)							
V_{IH}	Logic voltage high			2			V
V_{IL}	Logic voltage low					0.8	V

6.5 Electrical Characteristics (Dual Supplies: ±15 V) (continued)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = -15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{PD(SELx)}$	Pull-down resistance on SELx pins				6		MΩ
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_A = 0 V or 3.3 V, V_S = 0 V			17	21	µA
			T_A = –40°C to +85°C			22	µA
			T_A = –40°C to +125°C			23	µA
I_{SS}	V_{SS} supply current	V_A = 0 V or 3.3 V, V_S = 0 V			8	10	µA
			T_A = –40°C to +85°C			11	µA
			T_A = –40°C to +125°C			12	µA

(1) When V_S is positive, V_D is negative, and vice versa.

6.6 Switching Characteristics (Dual Supplies: ±15 V)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = -15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{TRAN}	Transition time	V_S = 10 V, R_L = 300 Ω , C_L = 35 pF		66	78	ns
		V_S = 10 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +85°C			107	ns
		V_S = 10 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +125°C			117	ns
tBBM	Break-before-make time delay	V_S = 10 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +125°C	20	40		ns
Q_J	Charge injection	V_S = 0 V, R_S = 0 Ω , C_L = 1 nF		–0.4		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF, f = 1 MHz		–85		dB
X_{TALK}	Channel-to-channel crosstalk	R_L = 50 Ω , C_L = 5 pF, f = 1 MHz (Inter-channel: S1x and S2x)		–105		dB
		R_L = 50 Ω , C_L = 5 pF, f = 1 MHz (Intra-channel: SxA and SxB)		–92		dB
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF, f = 1 MHz		–7		dB
ACPSRR	AC Power Supply Rejection Ratio	R_L = 10 kΩ , C_L = 5 pF, V_{PP}= 0.62 V on V_{DD}, f= 1 MHz		–59		dB
		R_L = 10 kΩ , C_L = 5 pF, V_{PP}= 0.62 V on V_{SS}, f= 1 MHz		–59		dB
BW	-3dB Bandwidth	R_L = 50 Ω , C_L = 5 pF		670		MHz
THD	Total harmonic distortion + noise	R_L = 10 kΩ , C_L = 5 pF, f= 20 Hz to 20 kHz		0.08		%
C_{IN}	Digital input capacitance	V_{IN} = 0 V or V_{DD}		1.5		pF
$C_{S(OFF)}$	Source off-capacitance	V_S = 0 V, f = 1 MHz		2.4	3.3	pF
$C_{S(ON)}$, $C_{D(ON)}$	Source and drain on-capacitance	V_S = 0 V, f = 1 MHz		5.5	7.5	pF

6.7 Electrical Characteristics (Single Supply: 12 V)

at T_A = 25°C, V_{DD} = 12 V, and V_{SS} = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG SWITCH							
V_A	Analog signal range			V_{SS}		V_{DD}	V
R_{ON}	On-resistance	V_S = 10 V, I_S = 1 mA			235	345	Ω
			T_A = –40°C to +85°C			400	Ω
			T_A = –40°C to +125°C			440	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = 10 V, I_S = 1 mA			4	12	Ω
			T_A = –40°C to +85°C			19	Ω
			T_A = –40°C to +125°C			23	Ω
R_{ON_DRIFT}	On-resistance drift	V_S = 0 V			0.47		%/°C
$I_{S(OFF)}$	Source off leakage current(1)	Switch state is off, V_S = 10 V/ 1 V, V_D = 1 V/ 10 V		–0.03	0.005	0.03	nA
			T_A = –40°C to +85°C	–0.1		0.07	nA
			T_A = –40°C to +125°C	–0.8		0.2	nA
$I_{D(ON)}$	Drain on leakage current	Switch state is on, V_S = floating, V_D = 1 V/ 10 V		–0.04	0.01	0.04	nA
			T_A = –40°C to +85°C	–0.16		0.09	nA
			T_A = –40°C to +125°C	–1.2		0.3	nA
DIGITAL INPUT (SELx pins)							
V_{IH}	Logic voltage high			2			V
V_{IL}	Logic voltage low					0.8	V
$R_{PD(SELx)}$	Pull-down resistance on SELx pins				6		MΩ
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_A = 0 V or 3.3 V, V_S = 0 V			13	16	µA
			T_A = –40°C to +85°C			17	µA
			T_A = –40°C to +125°C			18	µA

(1) When V_S is positive, V_D is negative, and vice versa.

6.8 Switching Characteristics (Single Supply: 12 V)

at T_A = 25°C, V_{DD} = 12 V, and V_{SS} = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{TRAN}	Transition time	V_S = 8 V, R_L = 300 Ω , C_L = 35 pF		72	84	ns
		V_S = 8 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +85°C			117	ns
		V_S = 8 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +125°C			128	ns
t_{BBM}	Break-before-make time delay	V_S = 8 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +125°C	20	40		ns
Q_J	Charge injection	V_S = 6 V, R_S = 0 Ω , C_L = 1 nF		–0.7		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF, f = 1 MHz		-85		dB
X_{TALK}	Channel-to-channel crosstalk	R_L = 50 Ω , C_L = 5 pF, f = 1 MHz (Inter-channel: S1x and S2x)		–110		dB
		R_L = 50 Ω , C_L = 5 pF, f = 1 MHz (Intra-channel: SxA and SxB)		–95		dB
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF, f = 1 MHz		–13		dB
ACPSRR	AC Power Supply Rejection Ratio	R_L= 10 kΩ , C_L = 5 pF, V_{PP}= 0.62 V, f= 1 MHz		–58		dB
BW	-3dB Bandwidth	R_L = 50 Ω , C_L = 5 pF		650		MHz

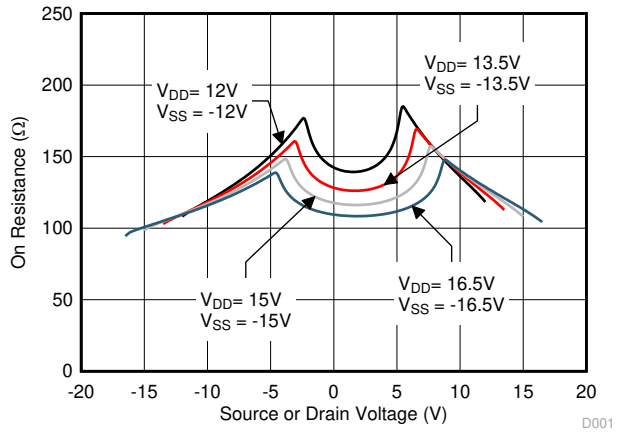
6.8 Switching Characteristics (Single Supply: 12 V) (continued)

at T_A = 25°C, V_{DD} = 12 V, and V_{SS} = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{IN}	Digital input capacitance	V_{IN} = 0 V or V_{DD}		1.7		pF
$C_{S(OFF)}$	Source off-capacitance	V_S = 6 V, f = 1 MHz		2.6	3.7	pF
$C_{S(ON)}$, $C_{D(ON)}$	Source and drain on-capacitance	V_S = 6 V, f = 1 MHz		6.3	8.5	pF

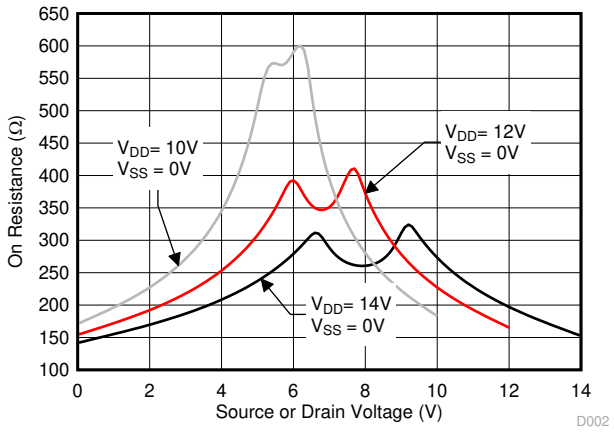
Typical Characteristics

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)



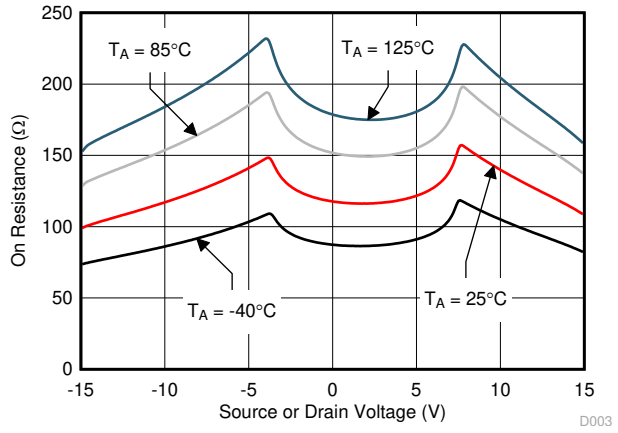
Dual Supply Operation (T_A = 25°C)

図 6-1. On-Resistance vs Source or Drain Voltage



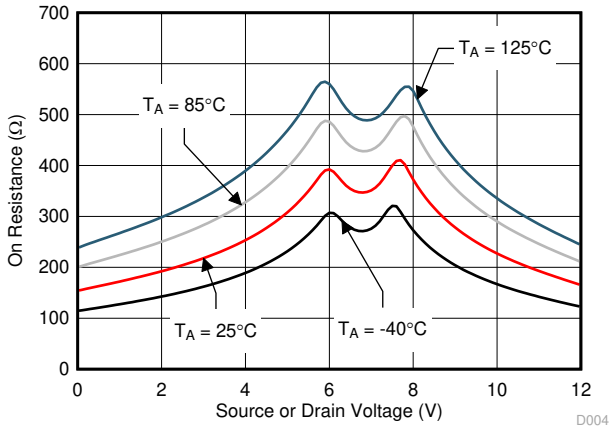
Single Supply Operation (T_A = 25°C)

図 6-2. On-Resistance vs Source or Drain Voltage



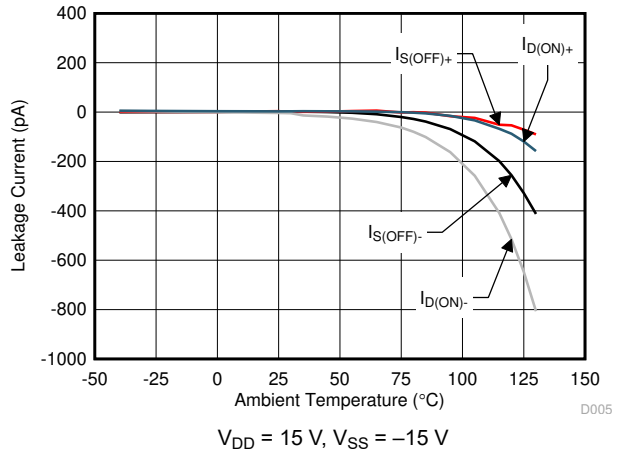
V_{DD} = 15 V, V_{SS} = –15 V

図 6-3. On-Resistance vs Source or Drain Voltage



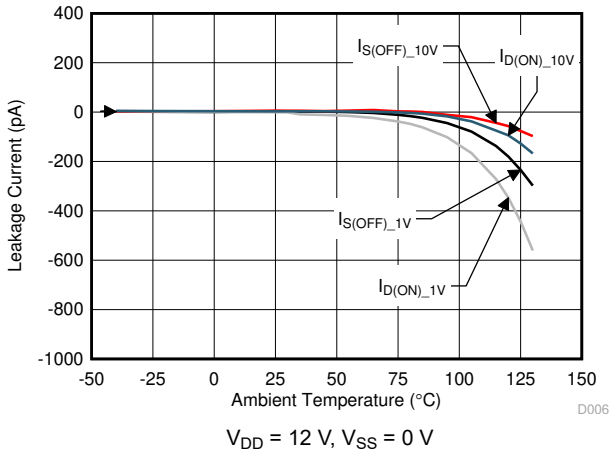
V_{DD} = 12 V, V_{SS} = 0 V

図 6-4. On-Resistance vs Source or Drain Voltage



V_{DD} = 15 V, V_{SS} = –15 V

図 6-5. Leakage Current vs Temperature

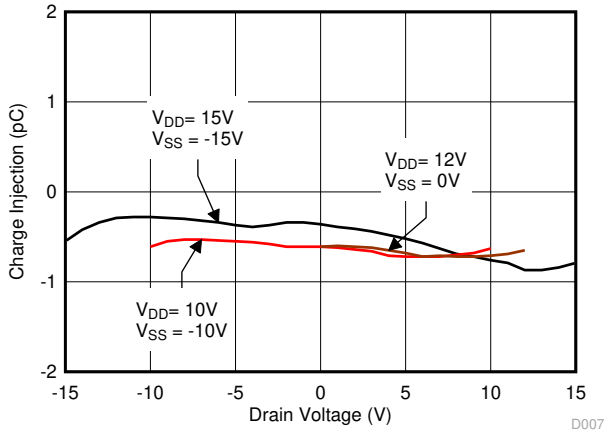


V_{DD} = 12 V, V_{SS} = 0 V

図 6-6. Leakage Current vs Temperature

Typical Characteristics

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)



T_A = 25°C

図 6-7. Charge Injection vs Source Voltage

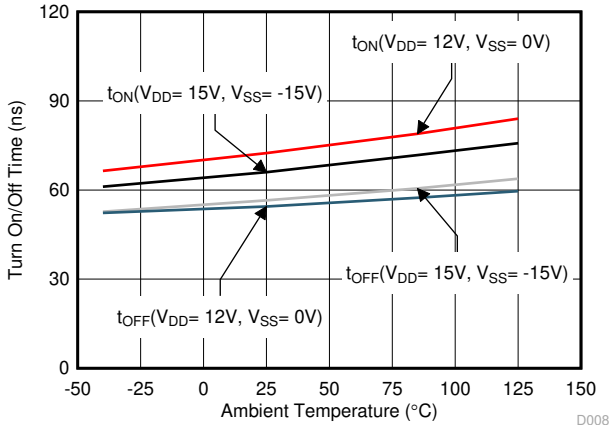
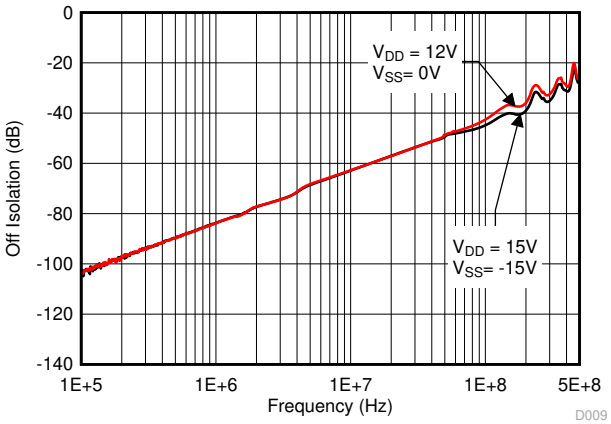
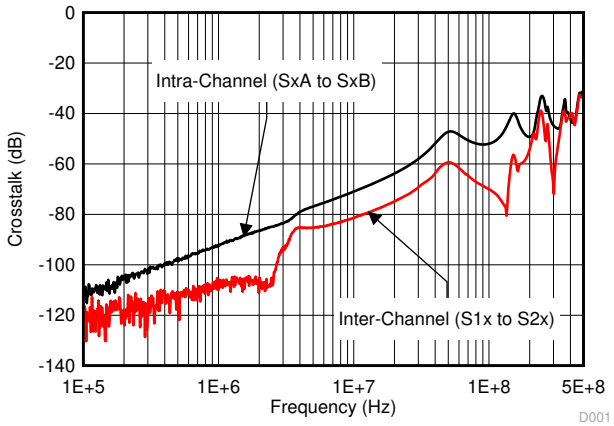


図 6-8. Transition Times vs Temperature



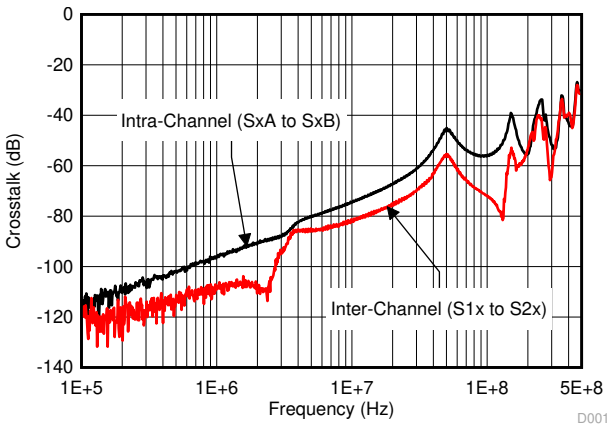
T_A = 25°C

図 6-9. Off Isolation vs Frequency



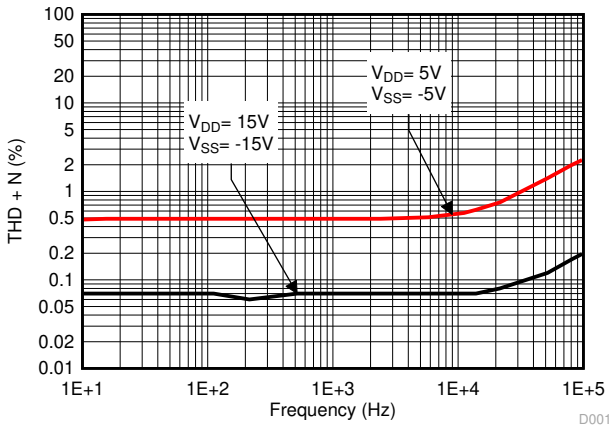
V_{DD} = 15 V, V_{SS} = –15 V, T_A = 25°C

図 6-10. Crosstalk vs Frequency



V_{DD} = 12 V, V_{SS} = 0 V, T_A = 25°C

図 6-11. Crosstalk vs Frequency

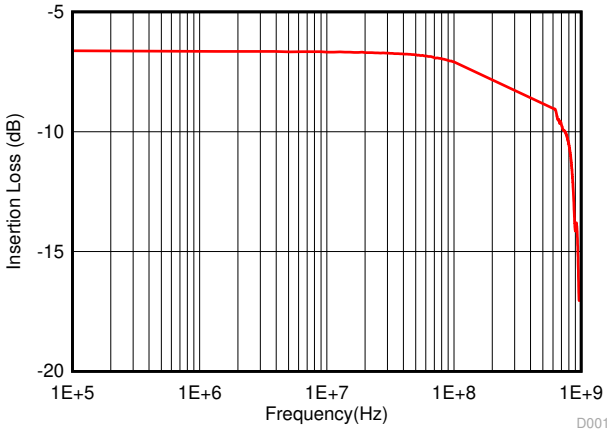


T_A = 25°C

図 6-12. THD+N vs Frequency

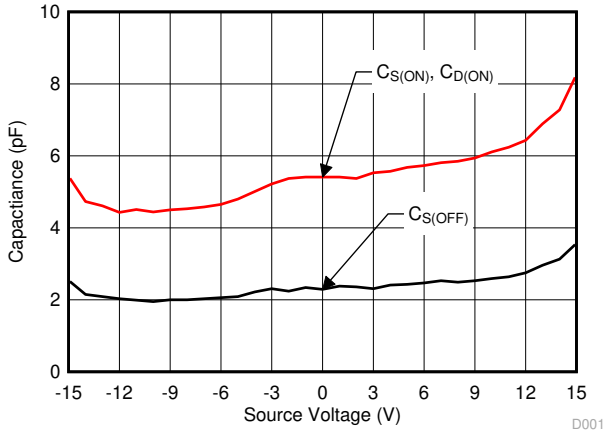
Typical Characteristics

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)



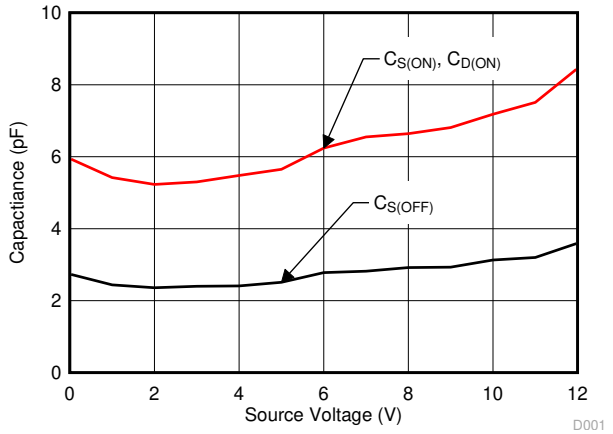
V_{DD} = 15 V, V_{SS} = –15 V, T_A = 25°C

図 6-13. On Response vs Frequency



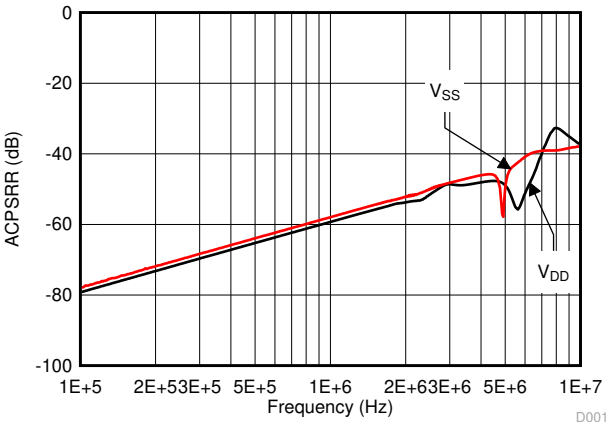
V_{DD} = 15 V, V_{SS} = –15 V, T_A = 25°C

図 6-14. Capacitance vs Source Voltage



V_{DD} = 12 V, V_{SS} = 0 V, T_A = 25°C

図 6-15. Capacitance vs Source Voltage



V_{DD} = 15 V, V_{SS} = –15 V, T_A = 25°C

図 6-16. ACPSRR vs Frequency

7 Detailed Description

7.1 Overview

7.1.1 On-Resistance

The on-resistance of the TMUX6136 is the ohmic resistance across the source (Sx) and drain (D) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. The measurement setup used to measure R_{ON} is shown in 図 7-1. Voltage (V) and current (I_{CH}) are measured using this setup, and R_{ON} is computed as shown in 式 1.

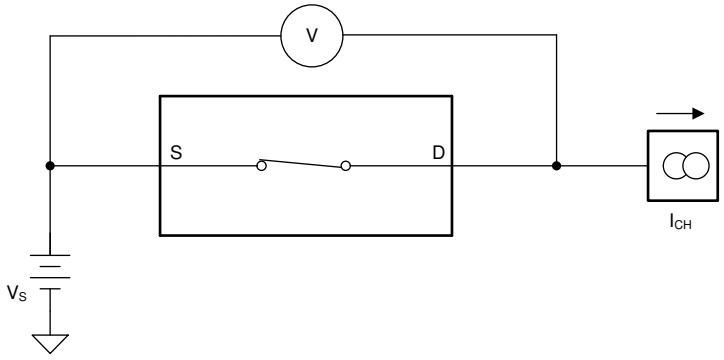


図 7-1. On-Resistance Measurement Setup

$$R_{ON} = V / I_{CH} \quad (1)$$

7.1.2 Off-Leakage Current

Source off-leakage current is defined as the leakage current that flows into or out of the source pin when the switch is in the off state. This current is denoted by the symbol $I_{S(OFF)}$. Drain off-leakage measurement is not characterization since the drain pin is always connected to one of the two source pins.

The setup used to measure both off-leakage currents is shown in 図 7-2.

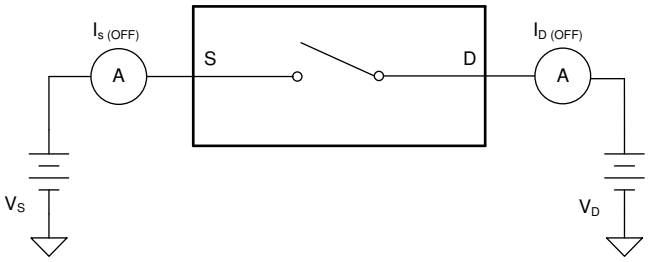


図 7-2. Off-Leakage Measurement Setup

7.1.3 On-Leakage Current

On-leakage current is defined as the leakage current that flows into or out of the drain pin when the switch is in the on state. The source pin is left floating during the measurement. 図 7-3 shows the circuit used for measuring the on-leakage current, denoted by $I_{D(ON)}$.

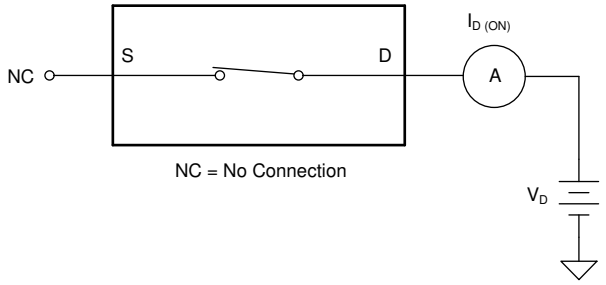


図 7-3. On-Leakage Measurement Setup

7.1.4 Transition Time

Transition time is defined as the time taken by the output of the TMUX6136 to rise or fall to 90% of the transition after the digital address signal has fallen or risen to 50% of the transition. 図 7-4 shows the setup used to measure transition time, denoted by the symbol t_{TRAN}.

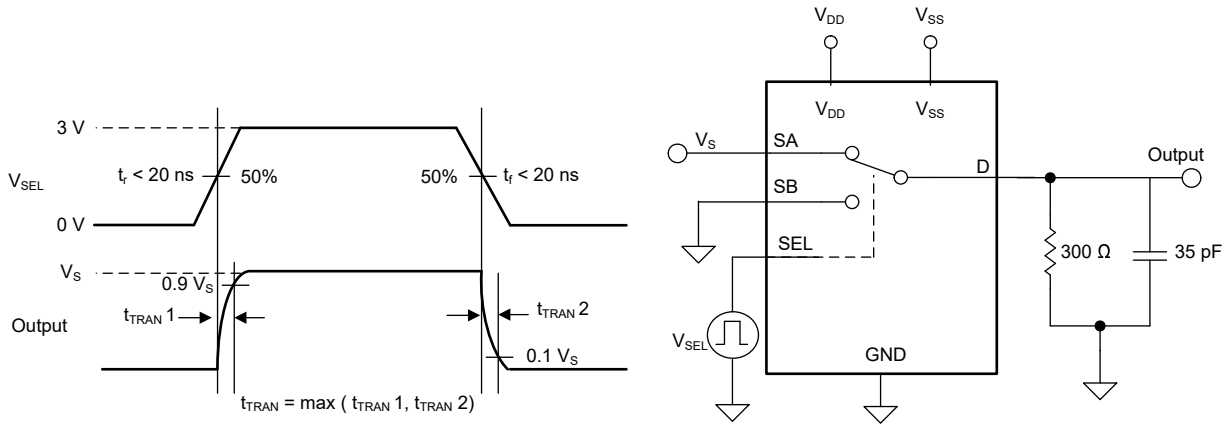


図 7-4. Transition-Time Measurement Setup

7.1.5 Break-Before-Make Delay

Break-before-make delay is a safety feature that prevents two inputs from connecting when the TMUX6136 is switching. The TMUX6136 output first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the *break* and the *make* is known as break-before-make delay. 図 7-5 shows the setup used to measure break-before-make delay, denoted by the symbol t_{BBM}.

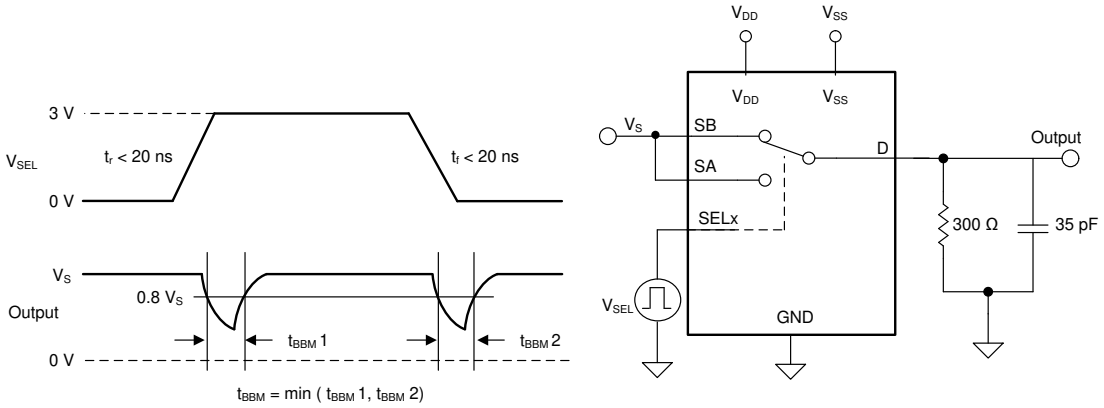


図 7-5. Break-Before-Make Delay Measurement Setup

7.1.6 Charge Injection

The TMUX6136 have a simple transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source of the device is known as charge injection, and is denoted by the symbol Q_{INJ}. 図 7-6 shows the setup used to measure charge injection from drain (D) to source (Sx).

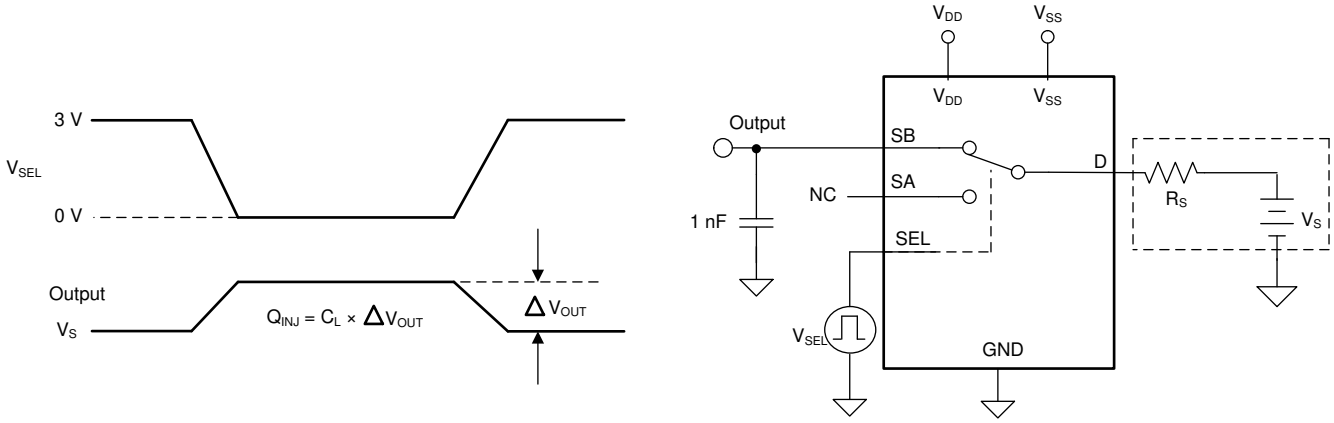


図 7-6. Charge-Injection Measurement Setup

7.1.7 Off Isolation

Off isolation is defined as the voltage at the drain pin (D) of the TMUX6136 when a 1-V_{RMS} signal is applied to the source pin (Sx) of an off-channel. 図 7-7 shows the setup used to measure off isolation. Use 式 2 to compute off isolation.

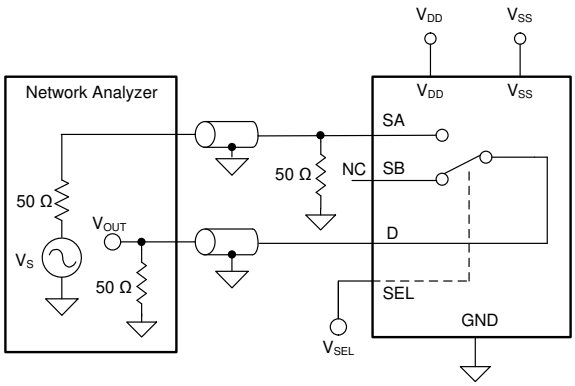


図 7-7. Off Isolation Measurement Setup

$$\text{Off Isolation} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right) \quad (2)$$

7.1.8 Channel-to-Channel Crosstalk

There are two types of crosstalk that can be defined for the TMUX6136:

1. Intra-channel crosstalk: the voltage at the source pin (Sx) of an off-switch input, when a 1-VRMS signal is applied at the source pin of an on-switch input in the same channel, as shown in 図 7-8.
2. Inter-channel crosstalk: the voltage at the source pin (Sx) of an on-switch input, when a 1-VRMS signal is applied at the source pin of an on-switch input in a different channel, as shown in 図 7-9.

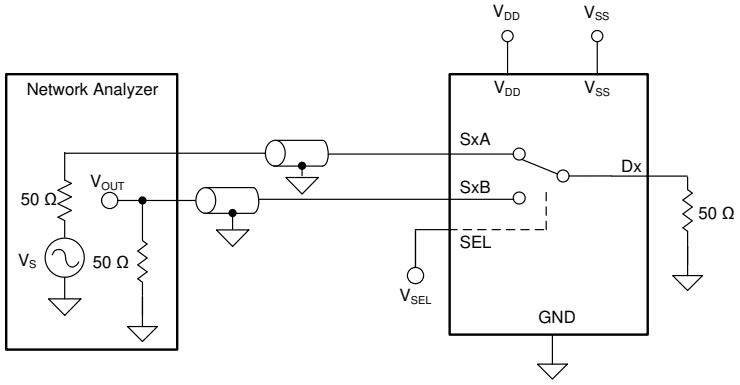


図 7-8. Intra-Channel Crosstalk Measurement Setup

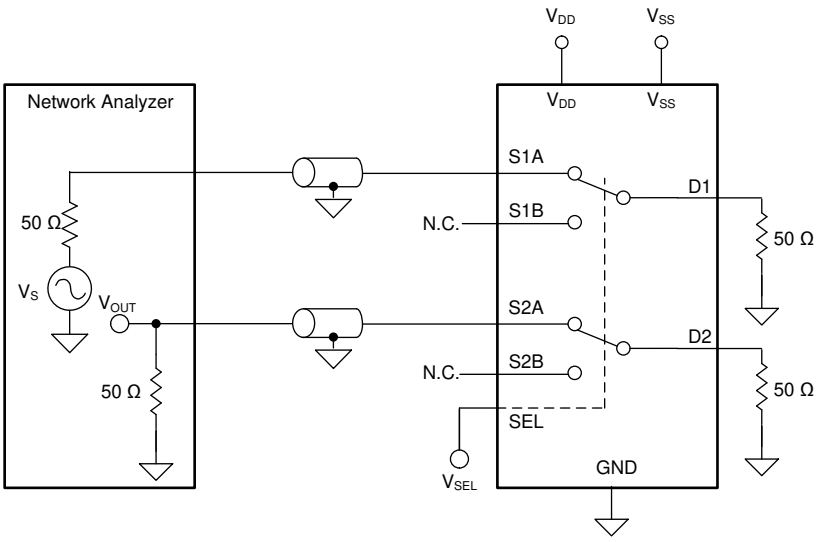


図 7-9. Inter-Channel Crosstalk Measurement Setup

$$\text{Channel-to-Channel Crosstalk} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right) \quad (3)$$

7.1.9 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by < 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (D) of the TMUX6136. 図 7-10 shows the setup used to measure bandwidth of the mux. Use 式 4 to compute the attenuation.

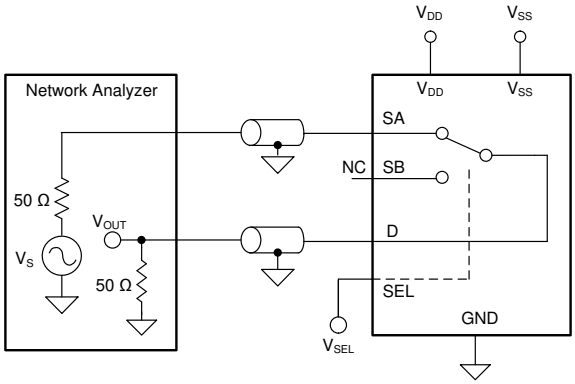


図 7-10. Bandwidth Measurement Setup

$$\text{Attenuation} = 20 \cdot \text{Log}\left(\frac{V_2}{V_1}\right) \quad (4)$$

7.1.10 THD + Noise

The total harmonic distortion (THD) of a signal is a measurement of the harmonic distortion, and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency at the mux output. The on-resistance of the TMUX6136 varies with the amplitude of the input signal and results in distortion when the drain pin is connected to a low-impedance load. Total harmonic distortion plus noise is denoted as THD+N.

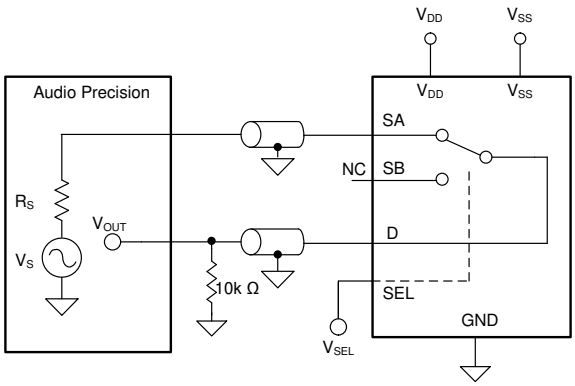


図 7-11. THD+N Measurement Setup

7.1.11 AC Power Supply Rejection Ratio (AC PSRR)

AC PSRR measures the ability of a device to prevent noise and spurious signals that appear on the supply voltage pin from coupling to the output of the switch. The DC voltage on the device supply is modulated by a sine wave of 620 mV_{PP}. The ratio of the amplitude of signal on the output to the amplitude of the modulated signal is the AC PSRR.

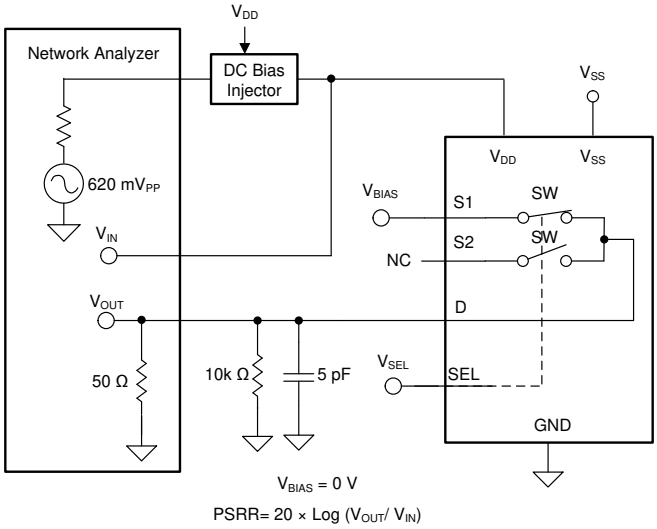
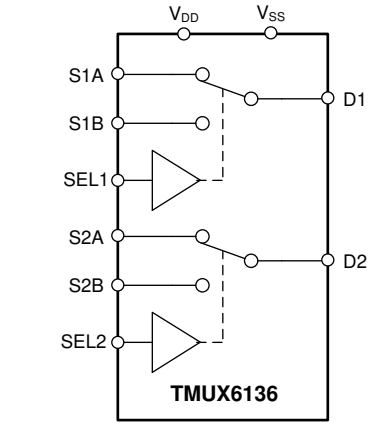


図 7-12. AC PSRR Measurement Setup

For a top-level block diagram of the TMUX6136, see セクション 7.2. The TMUX6136 is a 4-channel, single-ended, analog multiplexer. Each channel is turned on or turned off based on the state of the address lines and enable pin.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Ultralow Leakage Current

The TMUX6136 provides extremely low on- and off-leakage currents. The TMUX6136 is capable of switching signals from high source-impedance inputs into a high input-impedance op amp with minimal offset error because of the ultralow leakage currents. 図 7-13 shows typical leakage currents of the TMUX6136 versus temperature.

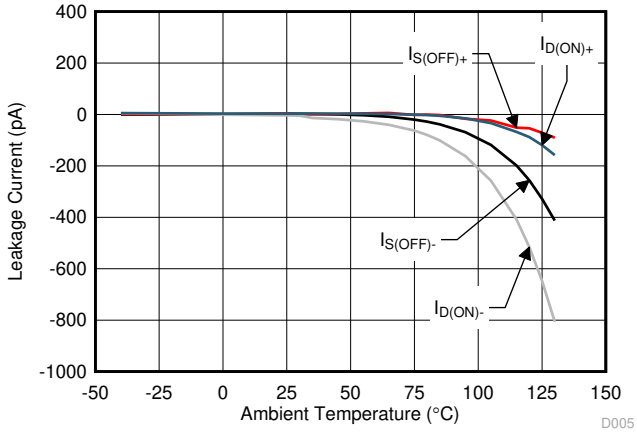


図 7-13. Leakage Current vs Temperature

7.3.2 Ultralow Charge Injection

The TMUX6136 is implemented with simple transmission gate topology, as shown in 図 7-14. Any mismatch in the stray capacitance associated with the NMOS and PMOS causes an output level change whenever the switch is opened or closed.

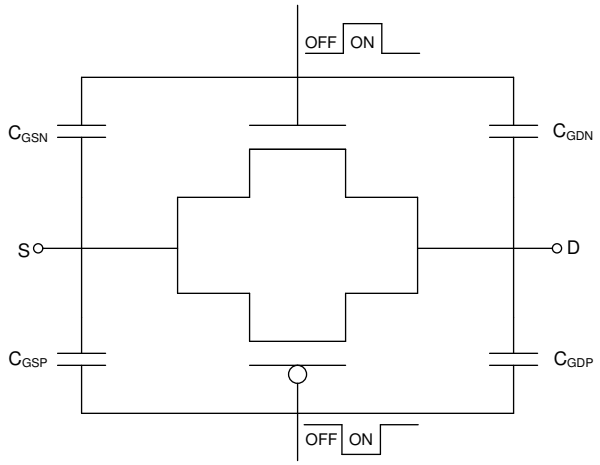


図 7-14. Transmission Gate Topology

The TMUX6136 utilizes special charge-injection cancellation circuitry that reduces the drain (D)-to-source (Sx) charge injection to as low as –0.4 pC at V_S = 0 V, as shown in 図 7-15.

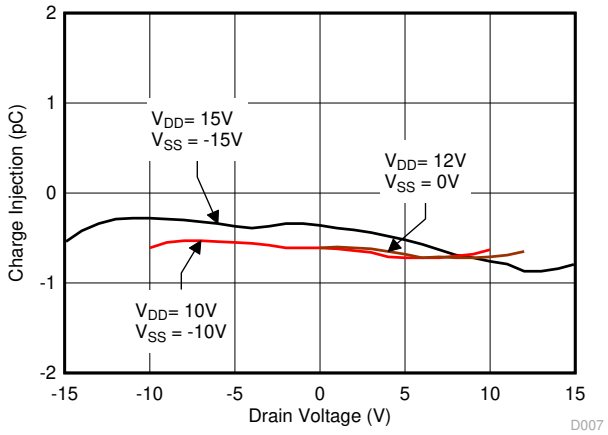


図 7-15. Charge Injection vs Drain Voltage

7.3.3 Bidirectional and Rail-to-Rail Operation

The TMUX6136 conducts equally well from source (Sx) to drain (D) or from drain (D) to source (Sx). Each TMUX6136 channel has very similar characteristics in both directions. The valid analog signal for TMUX6136 ranges from V_{SS} to V_{DD}. The input signal to the TMUX6136 swings from V_{SS} to V_{DD} without any significant degradation in performance.

7.4 Device Functional Modes

7.4.1 Truth Table

表 7-1. TMUX6136 Truth Table

SELx	Switch A (S1A to D1 or S2A to D2)	Switch B (S1B to D1 or S2B to D2)
0	OFF	ON
1	ON	OFF

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The TMUX6136 offers outstanding input and output leakage currents and ultralow charge injection. The device operates up to 33 V (V_{DD} to V_{SS} dual supply) or 16.5 V (V_{DD} single supply), and offers true rail-to-rail input and output. The on-capacitance of the TMUX6136 is low. These features make the TMUX6136 a precision, robust, high-performance analog multiplexer for high-voltage, industrial applications.

8.2 Typical Application

One example of the TMUX6136 precision performance to take advantage of is the implementation of parametric measurement unit (PMU) in the semiconductor automatic test equipment (ATE) application. The PMU is frequently used to characterize and measure the digital pin's DC characteristics of a device under test (DUT). Among all the PMU's capabilities, force voltage measure current (FVMC) and force current measure voltage (FCMV) are the two most typical configurations in DC characterizations.

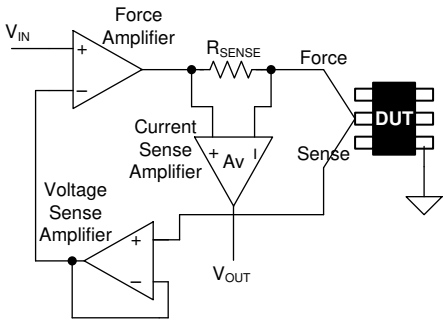


図 8-1. FVMC Measurement in PMU

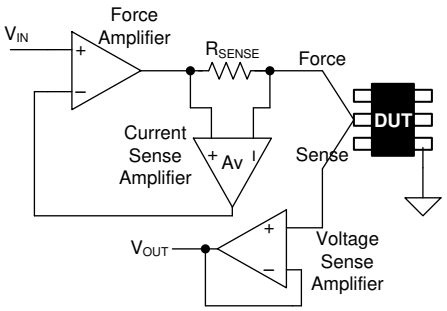


図 8-2. FCMV Measurement in PMU

図 8-1 shows a simplified diagram of the PMU in FVMC configuration. The control loop consists of the force amplifier with the voltage sense amplifier (unity gain in this example) making up the feedback path. Current flowing through the DUT is measured by sensing the current flowing through a sense resistor (R_{SENSE}) in series with the DUT. The current sense amplifier with a gain of Av generates a voltage (V_{OUT}) at its output and the voltage can then be measured by an ADC. The voltage produced at the DUT pin stays at the input voltage level (IN) as long as the force amplifier does not rail out (for example, I_{DUT} × R_{SENSE} x Av stays within the input voltage range of the force amplifier). Depending on the level of the DUT current to be measured, different gain settings need to be configured for the current sense amplifier.

図 8-2 shows a simplified diagram of the PMU in FCMV mode. The voltage V_{IN} is now converted to a current through the following relationship:

$$\text{Force Current} = V_{IN} / (R_{SENSE} \text{ x Av}) \quad (5)$$

The control loop consists of the force amplifier with the current sense amplifier making up the feedback path. The voltage at the DUT is sensed across the voltage sense amplifier (unity gain in this example) and presented at the output for sample.

8.2.1 Design Requirements

The goal of this design example is to simplify the FVMC and FCMV functions of a PMU design using a SPDT switch. The FVMC configuration is useful to test a device being used as a power supply, or in continuity or

leakage testing. In this configuration, the input voltage is directly applied to the DUT pin, and the current into or out of the DUT pin is converted to a voltage by a sense resistor and measured by an analog to digital converter (ADC). In the FCMV mode, an input current is forced to the DUT and the produced voltage on the DUT pin is directly measured. In this example, the PMU design is required to meet the following specifications:

- Force voltage range: –15 volts to +15 volts
- Force current range: ±5 µA to ±50 mA
- Measure voltage range: –15 volts to +15 volts
- Measure current range: ±5 µA to ±50 mA

In addition to the voltage and current requirements, fast throughput is also a key requirement in ATE because it relates directly to the cost of manufacturing the DUT.

8.2.2 Detailed Design Procedure

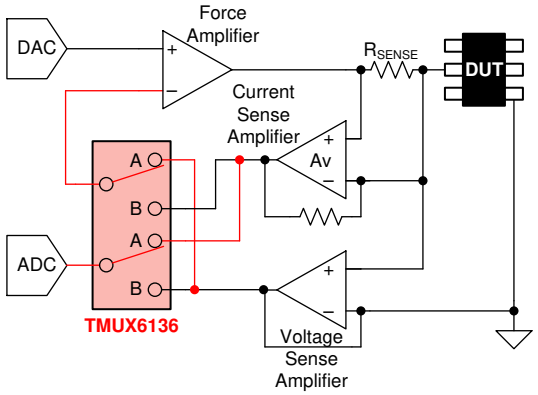


図 8-3. FVMC Implementation in PMU Using the TMUX6136

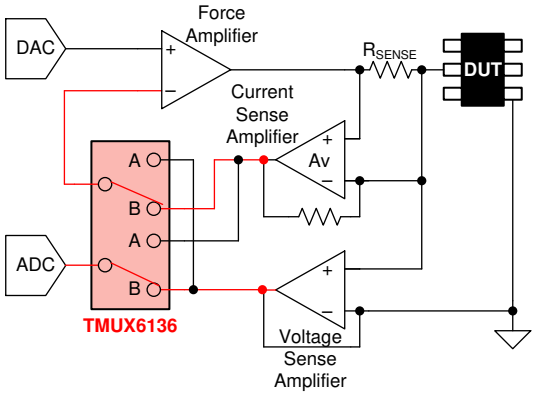


図 8-4. FCMV Implementation in PMU Using the TMUX6136

The implementation of the FVMC and FCMV modes can be combined with the use of a dual SPDT switch such as the TMUX6136. 図 8-3 and 図 8-4 shows simplified diagrams of such implementations. In the FVMC mode, the switch is toggled to position A and this allows the voltage sense amplifier to become part of the feedback loop and the voltage output of the current sense amplifier to be sampled by the ADC. In the FCMV mode, the switch is toggled to position B, and this allows the current sense amplifier to become part of the feedback loop and the voltage output of the voltage sense amplifier to be sampled by the ADC.

8.2.3 Application Curve

The fast transition time of the TMUX6136 and low input or output parasitic capacitance help minimize the settling time, making the TMUX6136 an excellent candidate to implement the FVMC and FCMV functions of the PMU. 図 8-5 shows the plot for the transition time versus temperature for the TMUX6136.

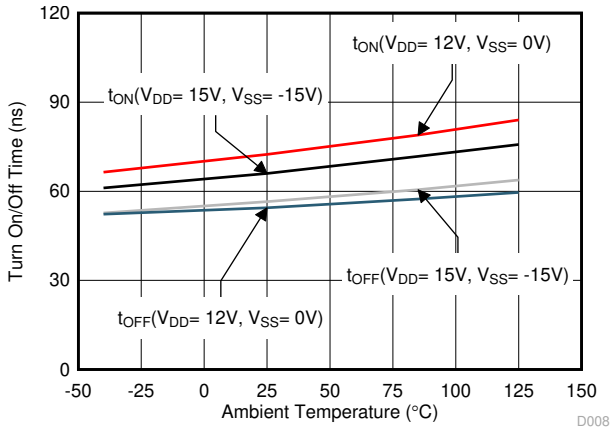


図 8-5. Transition Time vs Temperature for TMUX6136

9 Power Supply Recommendations

The TMUX6136 operates across a wide supply range of ±5 V to ±16.5 V (10 V to 16.5 V in single-supply mode). The device also performs well with unsymmetric supplies such as V_{DD} = 12 V and V_{SS}= –5 V. For reliable operation, use a supply decoupling capacitor ranging between 0.1 µF to 10 µF at both the V_{DD} and V_{SS} pins to ground.

10 Layout

10.1 Layout Guidelines

図 10-1 shows an example of a PCB layout with the TMUX6136.

Some key considerations are as follows:

1. Decouple the V_{DD} and V_{SS} pins with a 0.1-µF capacitor, placed as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the V_{DD} and V_{SS} supplies.
2. Keep the input lines as short as possible.
3. Use a solid ground plane to help distribute heat and reduce electromagnetic interference (EMI) noise pickup.
4. Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

10.2 Layout Example

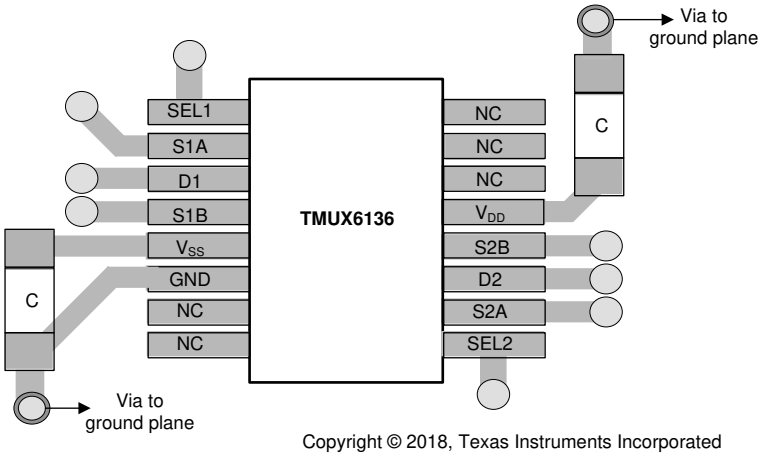


図 10-1. TMUX6136 Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *ADS8664 12-Bit, 500-kSPS, 4- and 8-Channel, Single-Supply, SAR ADCs with Bipolar Input Ranges*
- Texas Instruments, *OPA192 36-V, Precision, Rail-to-Rail Input/Output, Low Offset Voltage, Low Input Bias Current Op Amp with e-Trim™*

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 サポート・リソース

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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMUX6136PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MUX6136
TMUX6136PWR.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MUX6136
TMUX6136PWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MUX6136
TMUX6136PWRG4.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MUX6136

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

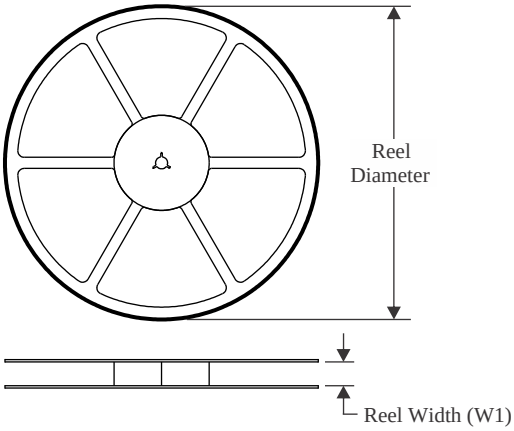
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

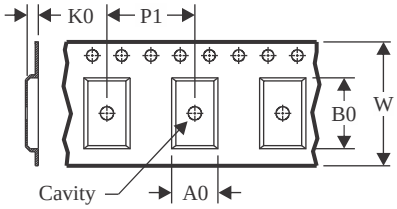
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

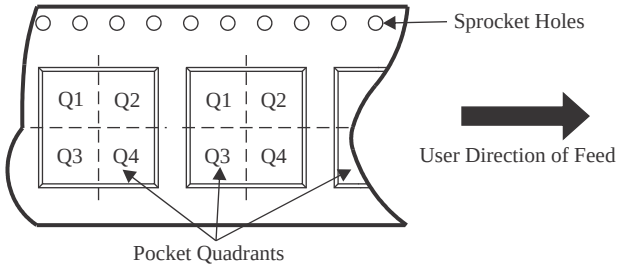


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

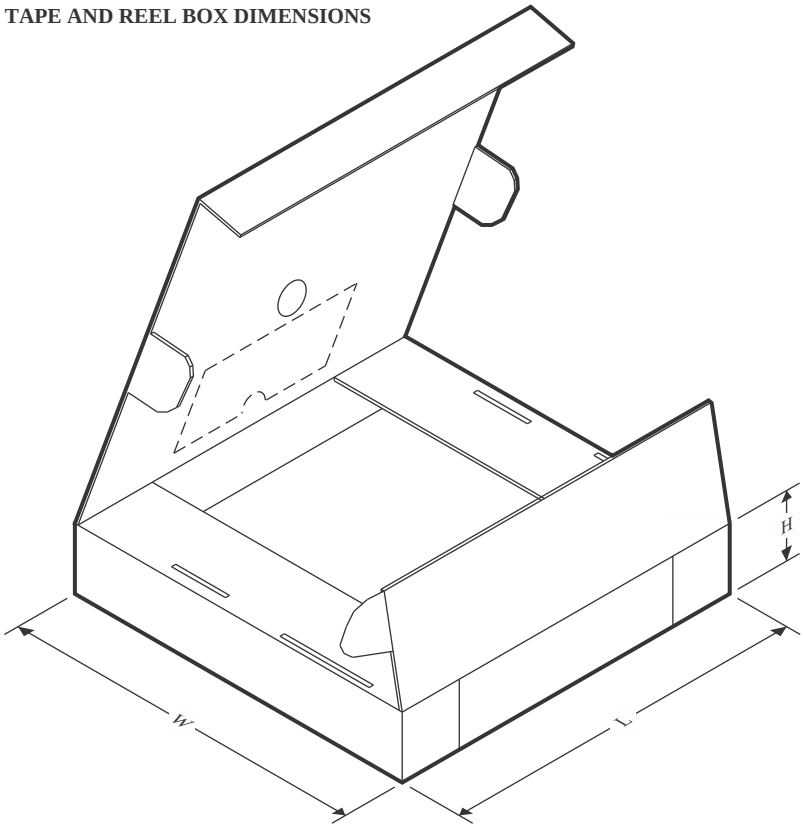
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUX6136PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TMUX6136PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

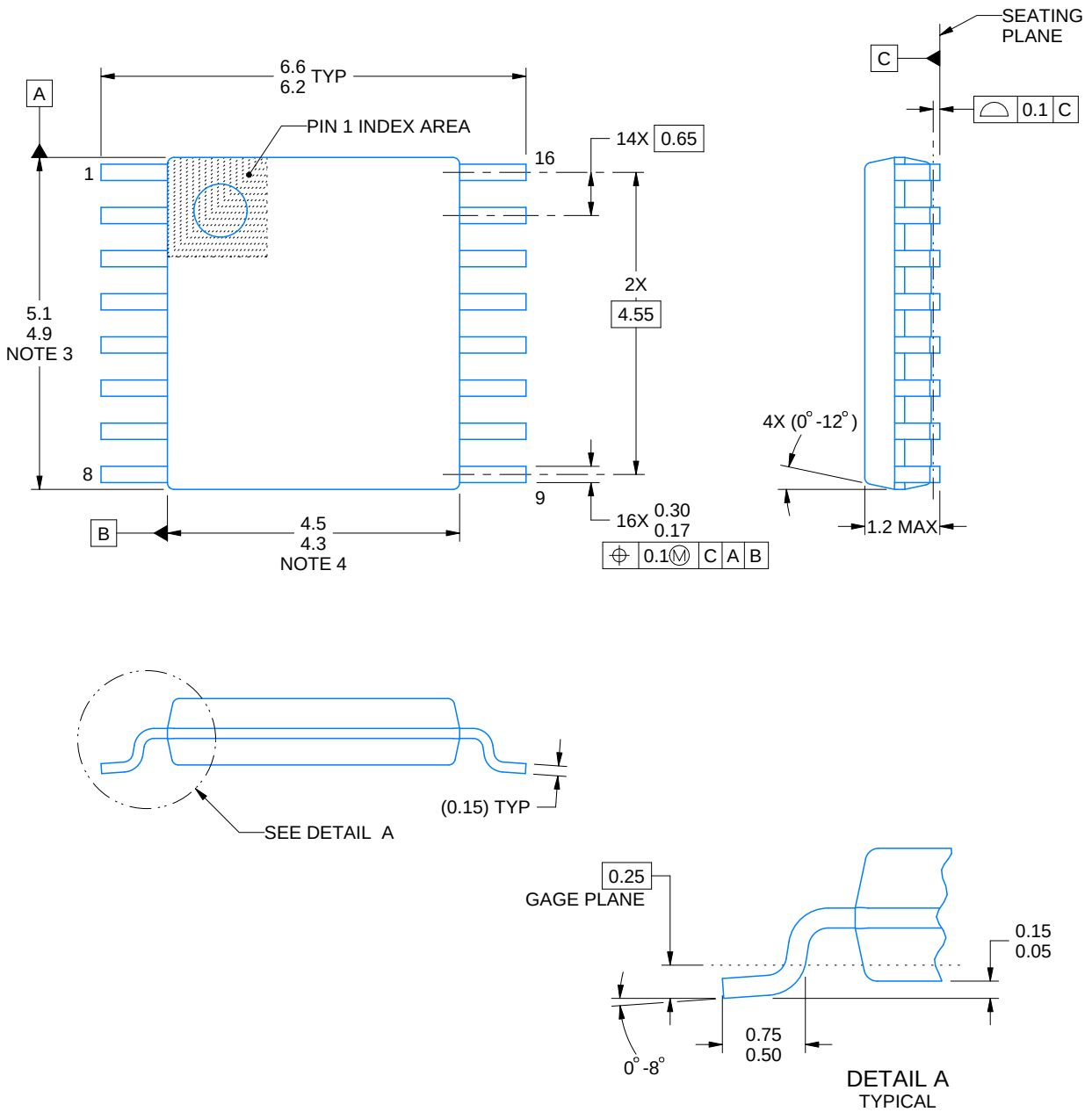
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUX6136PWR	TSSOP	PW	16	2000	353.0	353.0	32.0
TMUX6136PWRG4	TSSOP	PW	16	2000	353.0	353.0	32.0

PACKAGE OUTLINE

PW0016A

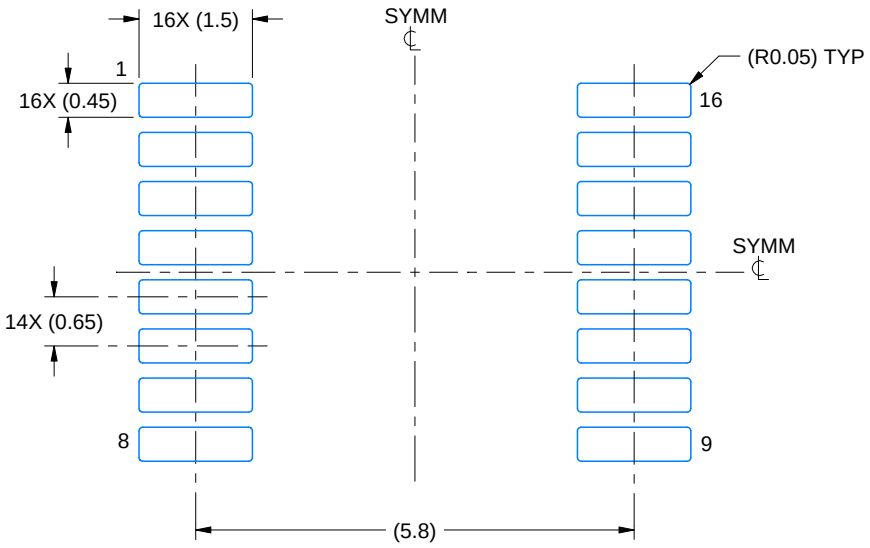
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

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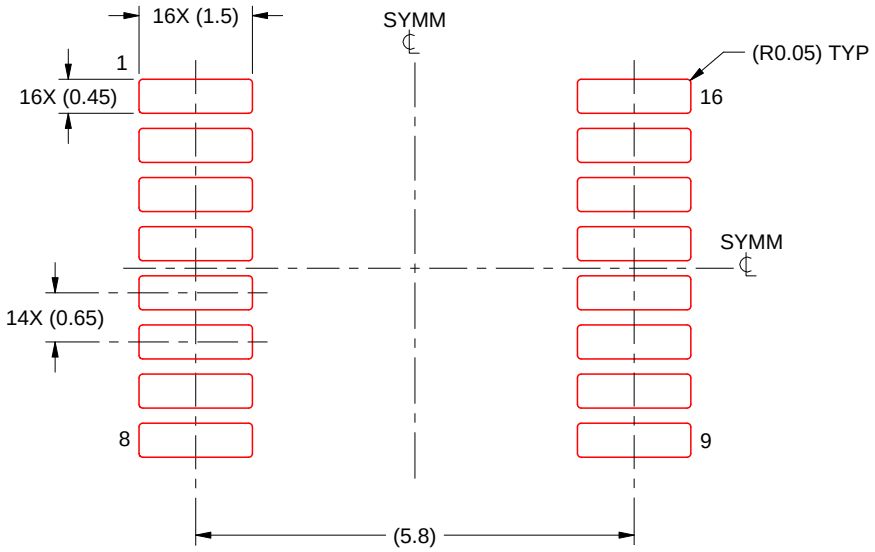
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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