

TMUX4157N -12V、低 RON、2:1 (SPDT)、 1.8V ロジック制御対応、負電圧スイッチ

1 特長

- 負の電圧に対応可能: -4V ~ -12V
- レール・ツー・レール動作
- 双方向の信号パス
- 1.8V ロジック互換
- フェイルセーフ・ロジック
- 大連続電流に対応可能: 150mA
- 低オン抵抗: 1.8Ω
- 55°C ~ +125°C の動作温度
- Break-Before-Make スイッチング
- ESD 保護 (HBM): 2000V

2 アプリケーション

- アナログおよびデジタル・スイッチング
- GaN パワー・アンプのゲート・スイッチング
- リモート無線ユニット (RRU)
- アクティブ・アンテナ・システム (AAS) の mMIMO
- ベースバンド・ユニット (BBU)
- ワイヤレス通信テスト

3 説明

TMUX4157N は汎用の 2:1 単極双投 (SPDT) スイッチで、負の電源レールのみをサポートします。電源電圧の範囲は -4V ~ -12V で、このデバイスはソース (Sx) ピンとドレイン (D) ピンで、GND から V_{SS} までの範囲の双方向アナログおよびデジタル信号をサポートします。選択ピンの状態 (SEL) は、ドレイン・ピンに接続される 2 つのソース・ピンのうちどちらかを制御します。

TMUX4157N は電源ピンと信号パスで負電圧をサポートしていますが、ロジック入力ピンは正電圧で制御されるため、GPIO 信号などの一般的な制御ロジック回路とのインターフェイスが可能です。ロジック入力ピンには 1.8V ロジック互換のスレッシュホールドがあり、最大 5.5 で動作できるため、システムの柔軟性が向上します。フェイルセーフ・ロジック回路により、電源ピンよりも先に制御ピンに電圧が印加されるため、デバイスへの損傷の可能性が避けられます。

TMUX4157N は、遷移時間が速く、スイッチを流れる連続電流が大きいいため、システムが 2 つの異なる電圧入力を迅速に切り替える必要があるアプリケーションに最適です。

製品情報

部品番号 ⁽¹⁾	パッケージ	本体サイズ (公称)
TMUX4157N	SC70 (6)	2.00mm × 1.25mm

- (1) 利用可能なすべてのパッケージについては、データシートの末尾にあるパッケージ・オプションについての付録を参照してください。

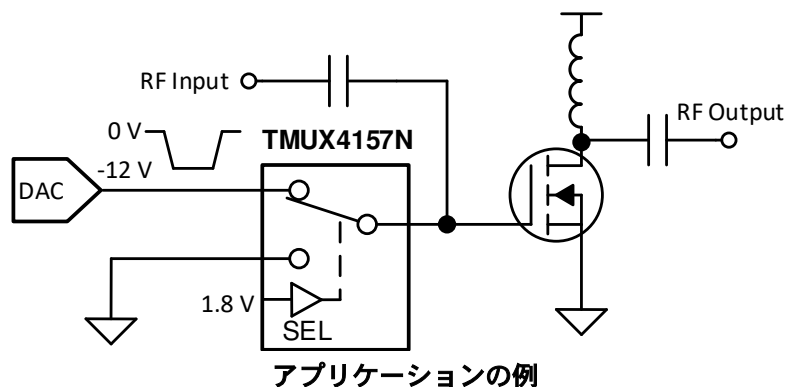
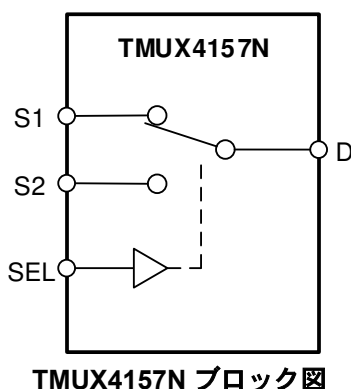


Table of Contents

1 特長	1	7.10 Crosstalk.....	14
2 アプリケーション	1	7.11 Bandwidth.....	16
3 説明	1	8 Detailed Description	16
4 Revision History	2	8.1 Overview.....	16
5 Pin Configuration and Functions	3	8.2 Functional Block Diagram.....	16
6 Specifications	4	8.3 Feature Description.....	16
6.1 Absolute Maximum Ratings	4	8.4 Device Functional Modes.....	17
6.2 ESD Ratings	4	8.5 Truth Tables.....	17
6.3 Recommended Operating Conditions	4	9 Application and Implementation	18
6.4 Thermal Information	5	9.1 Application Information.....	18
6.5 Electrical Characteristics	5	9.2 Typical Application.....	18
6.6 Dynamic Characteristics	6	10 Power Supply Recommendations	19
6.7 Timing Characteristics	7	11 Layout	20
6.8 Typical Characteristics.....	8	11.1 Layout Guidelines.....	20
7 Parameter Measurement Information	10	11.2 Layout Example.....	20
7.1 On-Resistance.....	10	12 Device and Documentation Support	21
7.2 Off-Leakage Current.....	10	12.1 Documentation Support.....	21
7.3 On-Leakage Current.....	11	12.2 Receiving Notification of Documentation Updates..	21
7.4 Transition Time.....	11	12.3 サポート・リソース.....	21
7.5 Break-Before-Make.....	12	12.4 Trademarks.....	21
7.6 Prop Delay.....	12	12.5 静電気放電に関する注意事項.....	21
7.7 Device Turn on Time.....	13	12.6 用語集.....	21
7.8 Charge Injection.....	13	13 Mechanical, Packaging, and Orderable Information	21
7.9 Off Isolation.....	14		

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (March 2020) to Revision A (March 2021)	Page
• ドキュメントのステータスを「事前情報」から:「量産データ」に変更	1

5 Pin Configuration and Functions

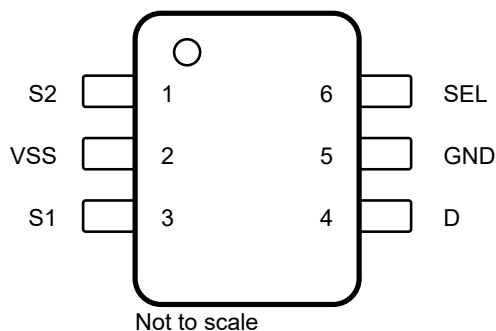


図 5-1. DCK Package 6-Pin SC70 Top View

表 5-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION ⁽²⁾
NAME	NO.		
S2	1	I/O	Source pin 2. Can be an input or output.
V _{SS}	2	P	Negative power supply. This pin is the most negative power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 μ F to 10 μ F between V _{SS} and GND.
S1	3	I/O	Source pin 1. Can be an input or output.
D	4	I/O	Drain pin. Can be an input or output.
GND	5	P	Ground (0 V) reference
SEL	6	I	Select pin: controls state of the switch according to 表 8-1. (Logic Low = S1 to D, Logic High = S2 to D)

(1) I = input, O = output, I/O = input and output, P = power.

(2) Refer to セクション 8.4 for what to do with unused pins.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)^{(1) (2) (3)}

		MIN	MAX	UNIT
V _{SS}	Supply voltage	–13	0.5	V
V _{SEL}	Logic control input pin voltage (SEL)	–0.5	6	
V _S or V _D	Source or drain voltage (Sx, D)	V _{SS} –0.5	0.5	
I _{SEL}	Logic control input pin diode current (SEL)	–50		mA
I _{IOK}	Switch source or drain pin diode current (Sx, D)	–50	50	
I _S or I _{D (CONT)}	Continuous current through switch (Sx, D pins) –40°C to +125°C	–100	100	
I _S or I _{D (CONT)}	Continuous current through switch (Sx, D pins) –40°C to +85°C	–150	150	
I _S or I _{D (PEAK)}	Source and drain peak current: (1 ms period max, 10% duty cycle maximum) (Sx, D)	–150	150	mA
P _D	Power dissipation		80	mW
T _{stg}	Storage temperature	–65	150	°C
T _J	Junction temperature		150	

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
- (3) All voltages are with respect to ground, unless otherwise specified.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±750	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{SS}	Supply voltage	–12		–4	V
V _S or V _D	Signal path input/output voltage (source or drain pin) (Sx, D)	V _{SS}		GND	V
V _{SEL}	Logic control input pin voltage (SEL)	0		5.5	V
I _S or I _{D (CONT)}	Continuous current through switch (Sx, D pins) –40°C to +125°C	–100		100	mA
I _S or I _{D (CONT)}	Continuous current through switch (Sx, D pins) –40°C to +85°C	–150		150	mA
T _A	Ambient temperature	–55		125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TMUX4157N	UNIT
		SC70 (DCK)	
		6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	181.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	132.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	73.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	56.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	72.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

Typical values measured at nominal V_{SS} and $T_A = 25^\circ\text{C}$.

PARAMETER		TEST CONDITIONS	V _{SS}	–55°C to 125°C			UNIT
				MIN	TYP	MAX	
ANALOG SWITCH							
R _{ON}	On-state switch resistance	V _S = V _{SS} to GND I _{SD} = 50 mA	–12 V	1.8	6.5	Ω	
			–10 V	1.8	6.5		
			–8 V	1.9	6.5		
			–6 V	2	6.5		
			–4 V	2.6	8		
R _{ON FLAT}	On-state switch resistance flatness	V _S = V _{SS} to GND I _{SD} = 50 mA	–12 V	1.8		Ω	
			–10 V	1.8			
			–8 V	1.8			
			–6 V	1.6			
			–4 V	1.4			
Δ _{RON}	On-state switch resistance matching between inputs	V _S = V _{SS} to GND I _{SD} = 50 mA	–12 V	0.2		Ω	
			–10 V	0.2			
			–8 V	0.25			
			–6 V	0.25			
			–4 V	0.3			
I _{S(OFF)}	Source off-state leakage current	Switch Off V _D = V _{SS} / GND V _S = GND / V _{SS}	–10 V	±1	±15	μA	
I _{D(ON)} I _{S(ON)}	Channel on-state leakage current	Switch On V _S = V _D = GND to V _{SS}	–10 V	±1	±15	μA	
C _{SOFF}	Source off capacitance	V _S = V _{SS} / 2 f = 1 MHz	–10 V	10		pF	
C _{SON} C _{DON}	On capacitance	V _S = V _{SS} / 2 f = 1 MHz	–10 V	20		pF	
POWER SUPPLY							
I _{SS}	V _{SS} supply current	Logic inputs = GND or 3.3 V V _S = V _{SS} or GND	–12 V to –4 V	20	70	μA	

6.5 Electrical Characteristics (continued)

Typical values measured at nominal V_{SS} and $T_A = 25^\circ\text{C}$.

PARAMETER		TEST CONDITIONS	V _{SS}	–55°C to 125°C			UNIT
				MIN	TYP	MAX	
LOGIC INPUT (SEL)							
V _{IH}	Input logic high		–12 V	1.35	5	V	
			–10 V	1.35	5		
			–8 V	1.35	5		
			–6 V	1.35	5		
			–4 V	1.35	5		
V _{IL}	Input logic low		–12 V	0	0.8	V	
			–10 V	0	0.8		
			–8 V	0	0.8		
			–6 V	0	0.8		
			–4 V	0	0.8		
I _{IH} I _{IL}	Logic input leakage current		–12 V to –4 V	±1	±30	μA	
C _{IN}	Logic input capacitance		–12 V to –4 V	3		pF	

6.6 Dynamic Characteristics

Typical values measured at nominal V_{SS} and $T_A = 25^\circ\text{C}$.

PARAMETER		TEST CONDITIONS	V_{SS}	–55°C to 125°C			UNIT
				MIN	TYP	MAX	
Q_{INJ}	Charge Injection	$V_S = V_{SS} / 2$ $R_S = 0 \Omega$, $C_L = 100 \text{ pF}$	–12 V		–80		pC
			–10 V		–70		
			–8 V		–55		
			–6 V		–40		
			–4 V		–25		
O_{ISO}	Off Isolation	$V_{BIAS} = V_{SS} / 2$ $V_S = 200 \text{ mVpp}$ $R_L = 50 \Omega$, $C_L = 5 \text{ pF}$ $f = 1 \text{ MHz}$	–12 V to –4 V		–65		dB
O_{ISO}	Off Isolation	$V_{BIAS} = V_{SS} / 2$ $V_S = 200 \text{ mVpp}$ $R_L = 50 \Omega$, $C_L = 5 \text{ pF}$ $f = 10 \text{ MHz}$	–12 V to –4 V		–40		dB
X_{TALK}	Crosstalk	$V_{BIAS} = V_{SS} / 2$ $V_S = 200 \text{ mVpp}$ $R_L = 50 \Omega$, $C_L = 5 \text{ pF}$ $f = 1 \text{ MHz}$	–12 V to –4 V		–65		dB
X_{TALK}	Crosstalk	$V_{BIAS} = V_{SS} / 2$ $V_S = 200 \text{ mVpp}$ $R_L = 50 \Omega$, $C_L = 5 \text{ pF}$ $f = 10 \text{ MHz}$	–12 V to –4 V		–42		dB
BW	Bandwidth	$V_{BIAS} = V_{SS} / 2$ $V_S = 200 \text{ mVpp}$ $R_L = 50 \Omega$, $C_L = 5 \text{ pF}$	–12 V to –4 V		340		MHz

6.7 Timing Characteristics

Typical values measured at nominal V_{SS} and $T_A = 25^\circ\text{C}$.

PARAMETER		TEST CONDITIONS	V_{SS}	–55°C to 125°C			UNIT
				MIN	TYP	MAX	
t_{PD}	Propagation delay Sx to D, D to Sx	$C_L = 100\text{ pF}$	–12 V		0.4	2	ns
			–10 V		0.4	2	
			–8 V		0.4	2	
			–6 V		0.4	2	
			–4 V		0.5	2.5	
$t_{TRAN\ HIGH}$	Transition-time between inputs turning on (high) SEL to D, SEL to Sx	$R_L = 250\ \Omega$, $C_L = 100\text{ pF}$ $V_S = V_{SS}$	–12 V			210	ns
			–10 V			200	
			–8 V			205	
			–6 V			215	
			–4 V			280	
$t_{TRAN\ LOW}$	Transition-time between inputs turning off (low) SEL to D, SEL to Sx	$R_L = 250\ \Omega$, $C_L = 100\text{ pF}$ $V_S = V_{SS}$	–12 V			210	ns
			–10 V			210	
			–8 V			215	
			–6 V			225	
			–4 V			260	
t_{BBM}	Break before make time	$R_L = 50\ \Omega$, $C_L = 100\text{ pF}$ $V_S = -2.5\text{ V}$	–12 V	5			ns
			–10 V	5			
			–8 V	10			
			–6 V	10			
			–4 V	40			
$T_{ON(VSS)}$	Device turn on time (V_{SS} to output)	$R_L = 250\ \Omega$, $C_L = 100\text{ pF}$ $V_S = V_{SS}$	–12 V to –4 V			20	μs

6.8 Typical Characteristics

At $T_A = 25^\circ\text{C}$, $V_{SS} = -10\text{ V}$ (unless otherwise noted).

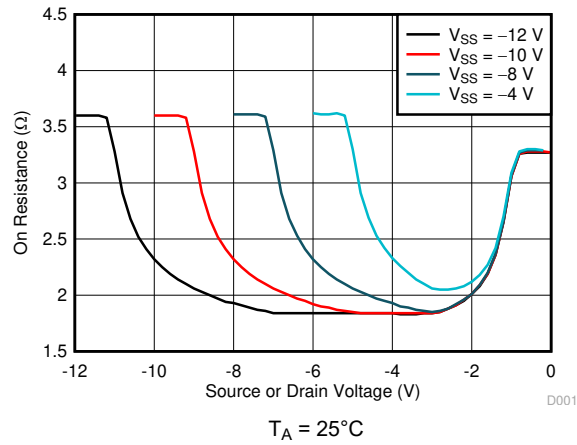


Figure 6-1. On-Resistance vs Signal Voltage

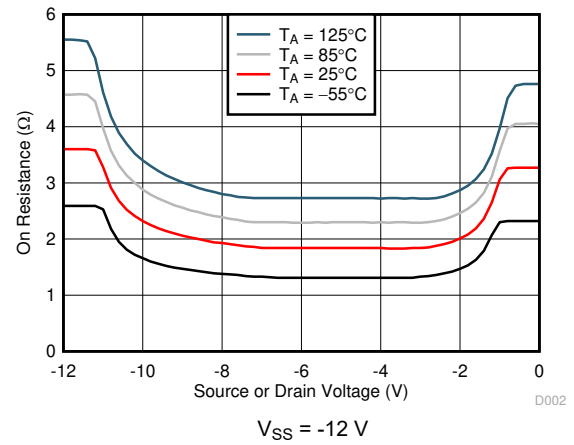


Figure 6-2. On-Resistance vs Signal Voltage

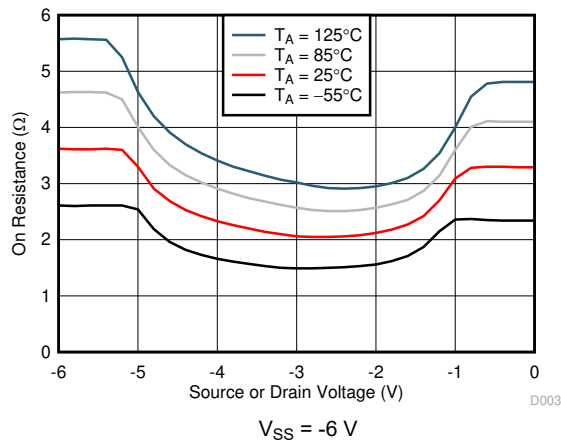


Figure 6-3. On-Resistance vs Signal Voltage

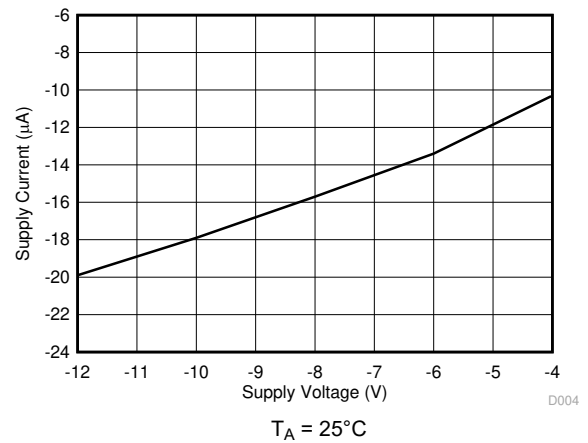


Figure 6-4. Supply Current vs Supply Voltage

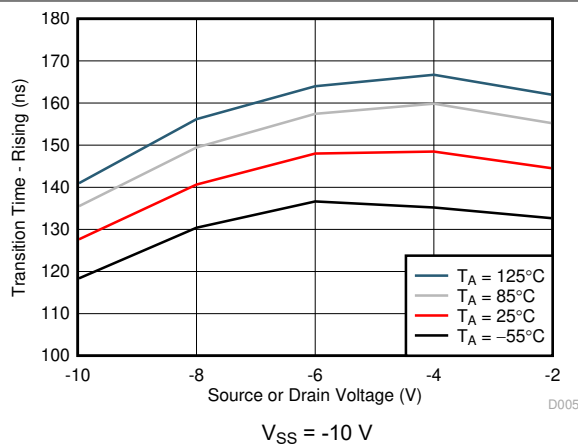


Figure 6-5. Transition Time vs Signal Voltage

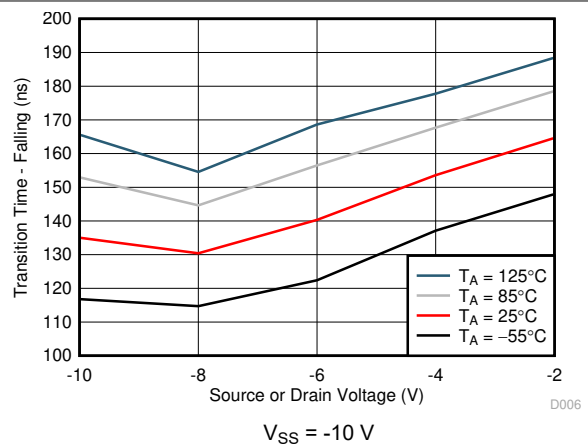
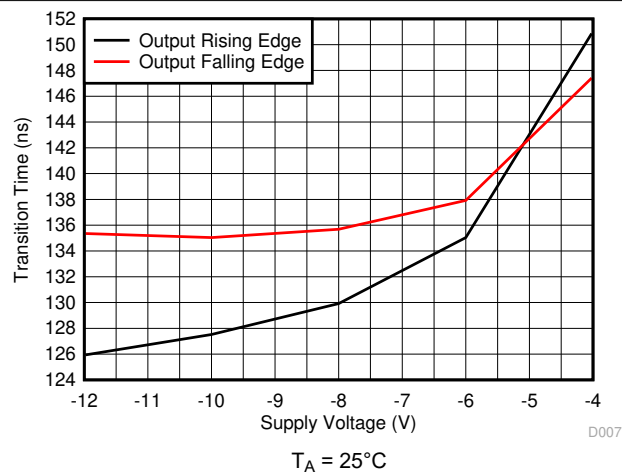


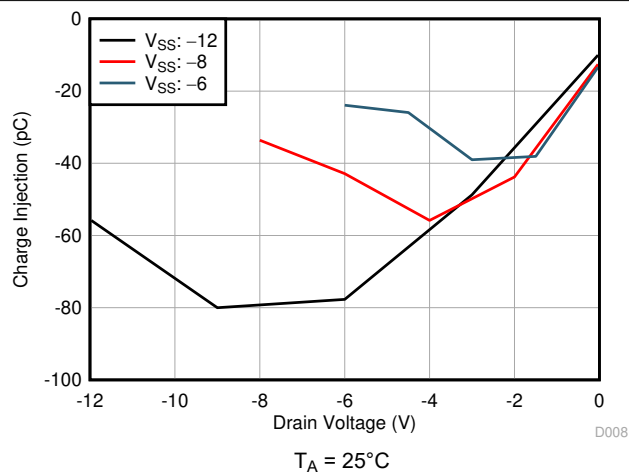
Figure 6-6. Transition Time vs Signal Voltage

6.8 Typical Characteristics (continued)

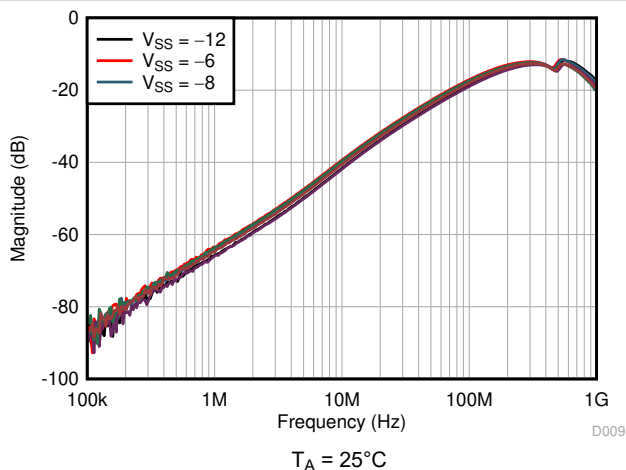
At $T_A = 25^\circ\text{C}$, $V_{SS} = -10\text{ V}$ (unless otherwise noted).



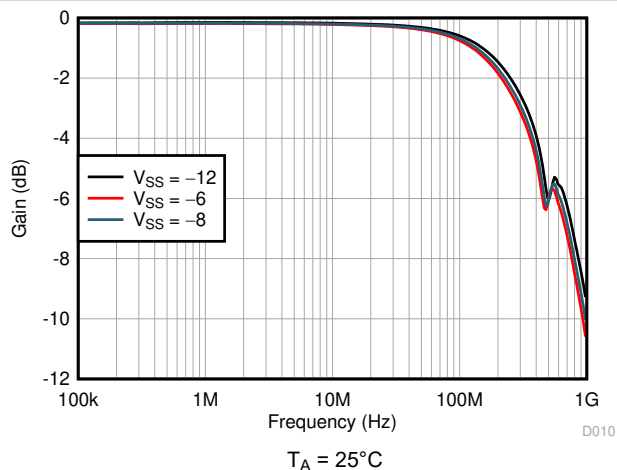
6-7. Transition Time vs Supply Voltage



6-8. Charge Injection vs Drain Voltage



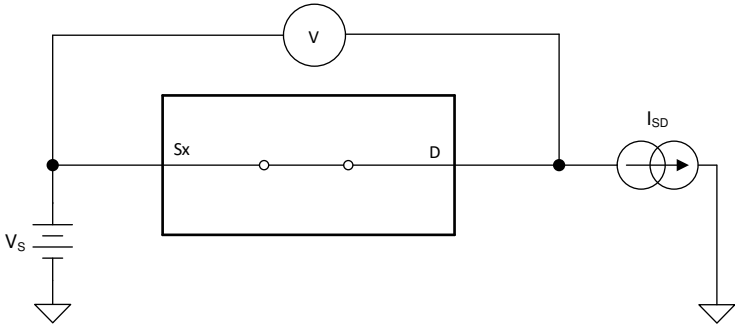
6-9. Crosstalk and Off-Isolation vs Frequency

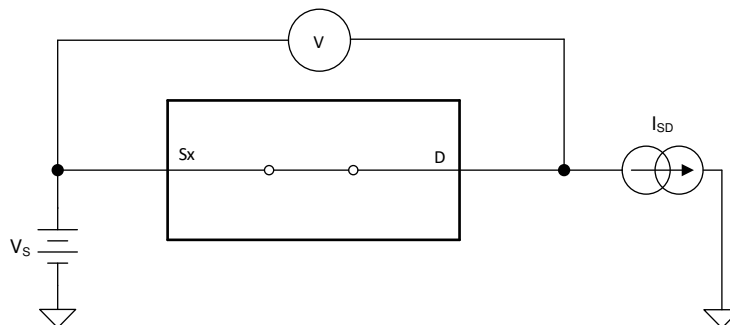


6-10. Frequency Response

7 Parameter Measurement Information

7.1 On-Resistance


The on-resistance of a device is the ohmic resistance between the source (Sx) and drain (D) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance.  shows the measurement setup used to measure R_{ON} . Voltage (V) and current (I_{SD}) are measured using this setup, and R_{ON} is computed with $R_{ON} = V / I_{SD}$:

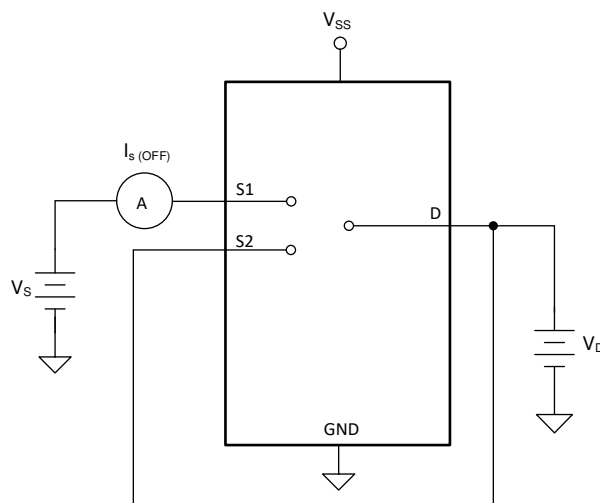


 **7-1. On-Resistance Measurement Setup**

7.2 Off-Leakage Current

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

 7-2 shows the setup used to measure off-leakage current.



 **7-2. Off-Leakage Measurement Setup**

7.3 On-Leakage Current

Source on-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is on. This current is denoted by the symbol $I_{S(ON)}$.

Drain on-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is on. This current is denoted by the symbol $I_{D(ON)}$.

Either the source pin or drain pin is left floating during the measurement. Figure 7-3 shows the circuit used for measuring the on-leakage current, denoted by $I_{S(ON)}$ or $I_{D(ON)}$.

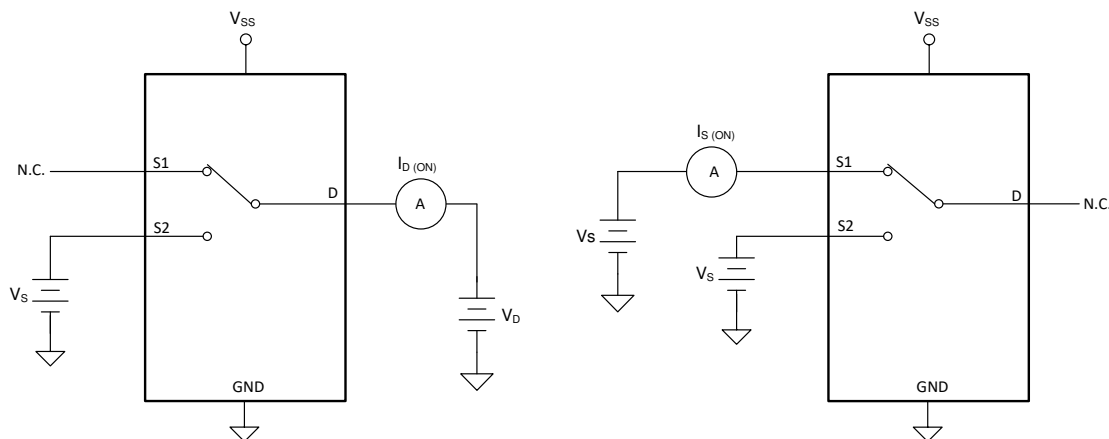


Figure 7-3. On-Leakage Measurement Setup

7.4 Transition Time

Transition time is defined as the time taken by the output of the device to rise or fall 50% after the logic control signal has risen or fallen past the 50% threshold. System level timing can then account for the time constant added from the load resistance and load capacitance. Figure 7-4 shows the setup used to measure transition time, denoted by the symbol $t_{TRANSITION}$.

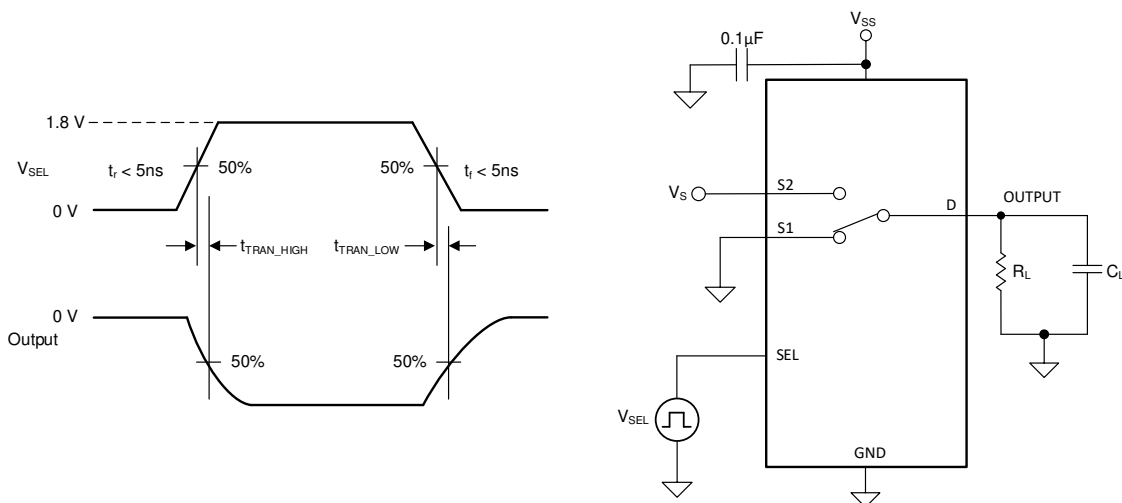

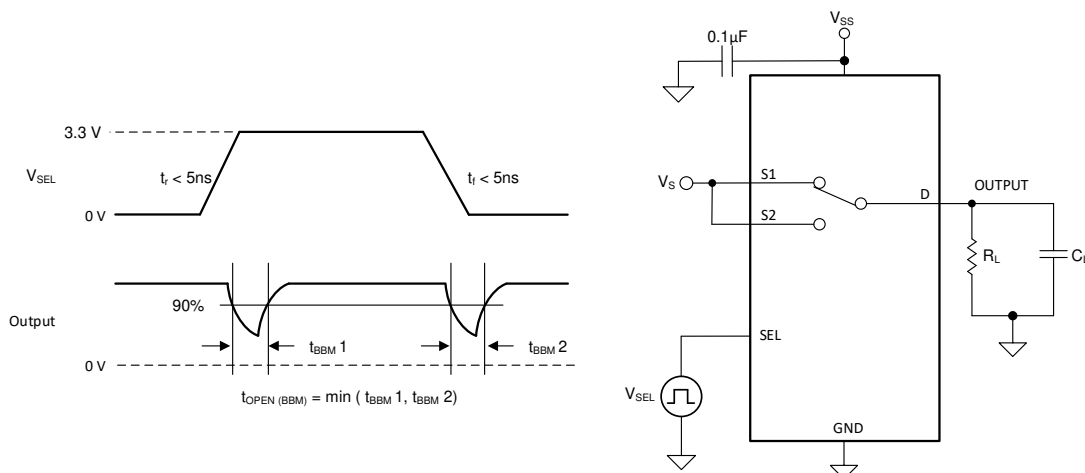


Figure 7-4. Transition-Time Measurement Setup


7.5 Break-Before-Make

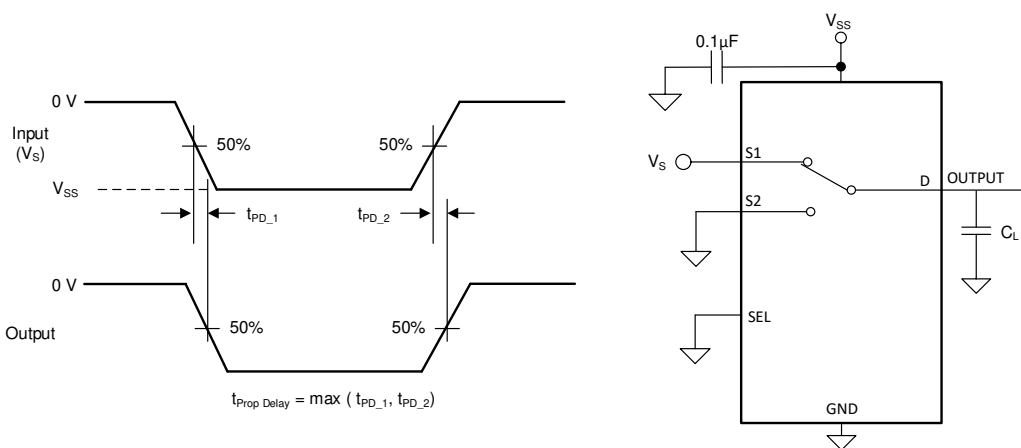
Break-before-make delay is a safety feature that prevents two inputs from connecting when the device is switching. The output first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the *break* and the *make* is known as break-before-make delay.  7-5 shows the setup used to measure break-before-make delay, denoted by the symbol $t_{\text{OPEN(BBM)}}$.



 7-5. Break-Before-Make Delay Measurement Setup

7.6 Prop Delay

Propagation delay is defined as the time taken by the output of the device to rise or fall 50% after the input signal has risen or fallen past the 50% threshold.  7-6 shows the setup used to measure propagation delay, denoted by the symbol t_{PD} .



 7-6. Prop Delay Measurement Setup

7.7 Device Turn on Time

The $T_{ON(VSS)}$ time is defined as the time taken by the output of the device to rise to 90% after the supply has risen past the supply threshold. The 90% measurement is used to provide the timing of the device turning on in the system. Figure 7-7 shows the setup used to measure turn on time, denoted by the symbol $T_{ON(VSS)}$.

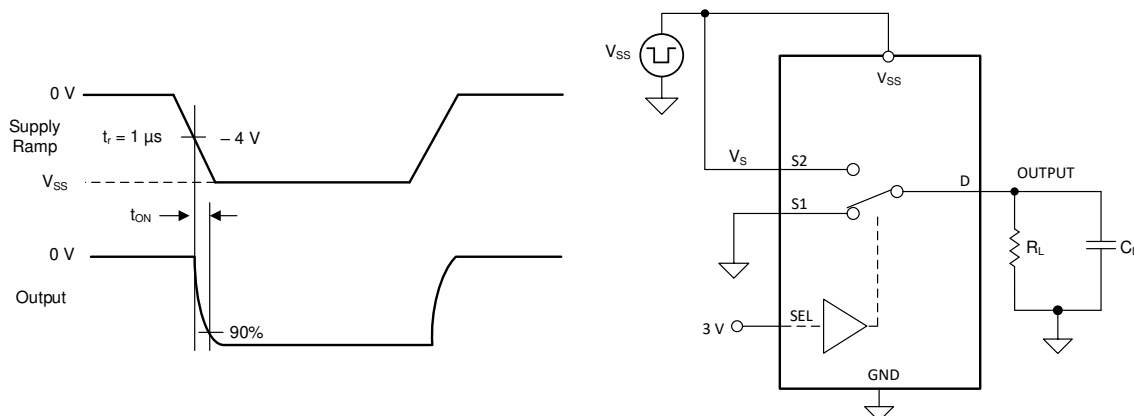


Figure 7-7. Device Turn on Time Measurement Setup

7.8 Charge Injection

The TMUX4157N has a transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_C . Figure 7-8 shows the setup used to measure charge injection from Drain (D) to Source (S_x).

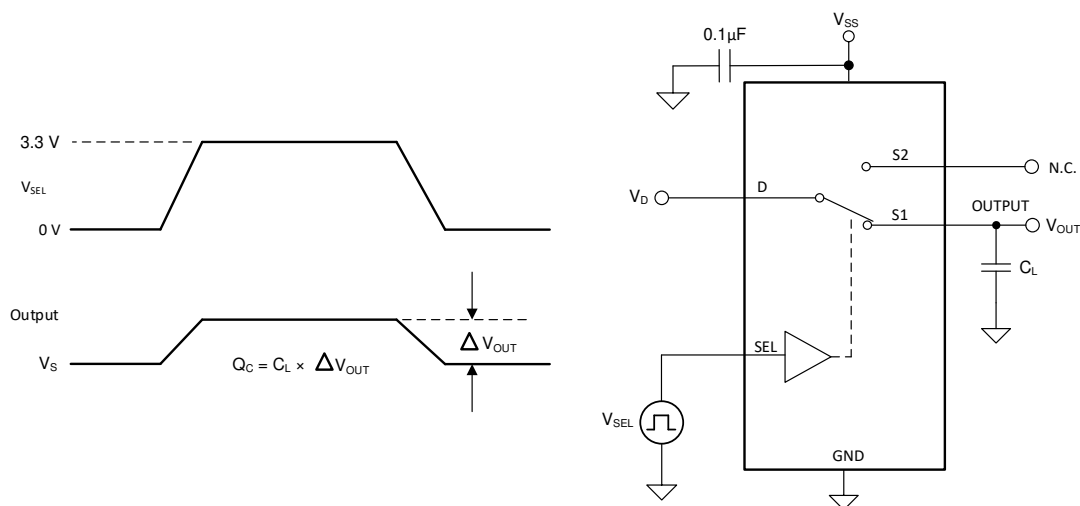

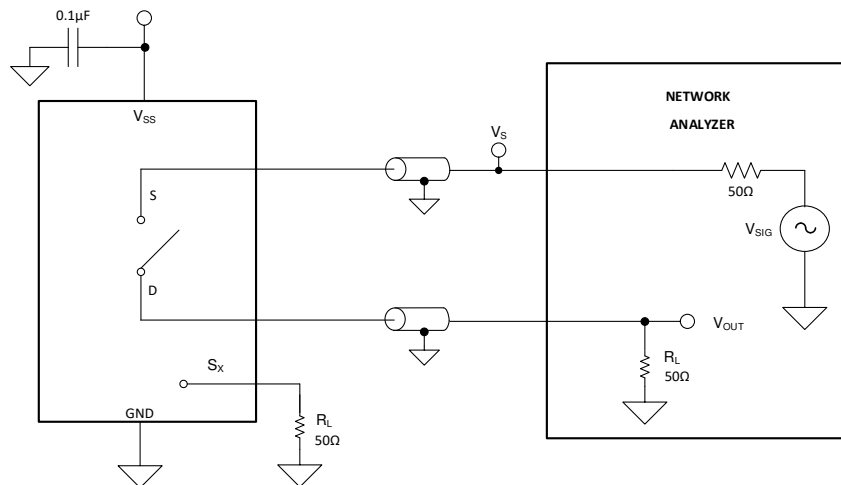


Figure 7-8. Charge-Injection Measurement Setup

7.9 Off Isolation


Off isolation is defined as the ratio of the signal at the drain pin (D) of the device when a signal is applied to the source pin (S_x) of an off-channel.  7-9 shows the setup used to measure, and the equation used to calculate off isolation.

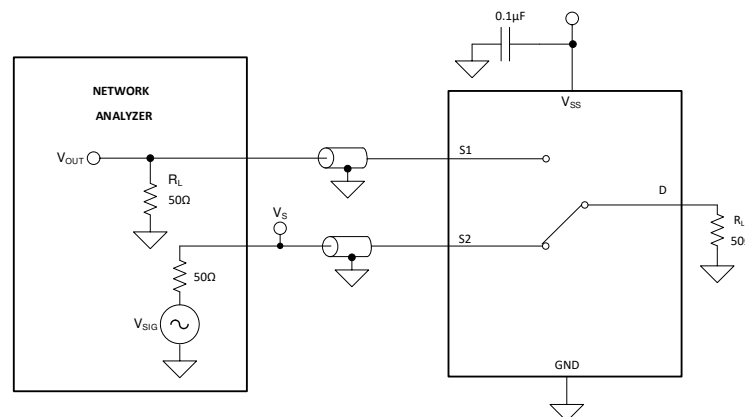


 7-9. Off Isolation Measurement Setup

$$\text{Off Isolation} = 20 \cdot \text{Log} \left(\frac{V_{\text{OUT}}}{V_S} \right) \quad (1)$$

7.10 Crosstalk

Crosstalk is defined as the ratio of the signal at the drain pin (D) of a different channel, when a signal is applied at the source pin (S_x) of an on-channel.  7-10 shows the setup used to measure, and the equation used to calculate crosstalk.



 7-10. Crosstalk Measurement Setup

$$\text{Channel-to-Channel Crosstalk} = 20 \cdot \text{Log} \left(\frac{V_{\text{OUT}}}{V_{\text{S}}} \right) \quad (2)$$

7.11 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (D) of the device. [Figure 7-11](#) shows the setup used to measure bandwidth.

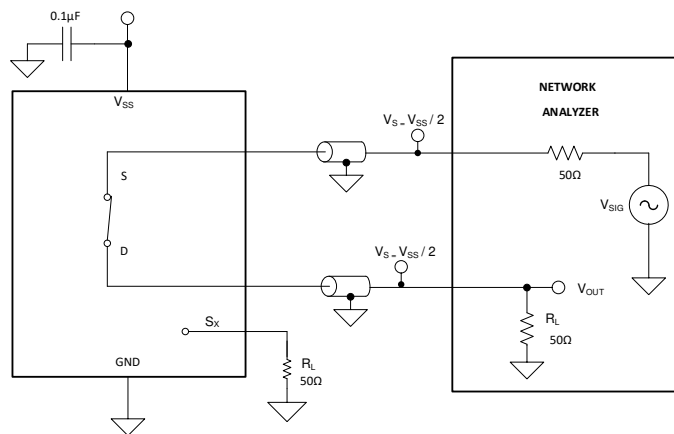


Figure 7-11. Bandwidth Measurement Setup

8 Detailed Description

8.1 Overview

The TMUX4157N is an 2:1 (SPDT), 1-channel switch where the input is controlled with a single select (SEL) control pin.

8.2 Functional Block Diagram

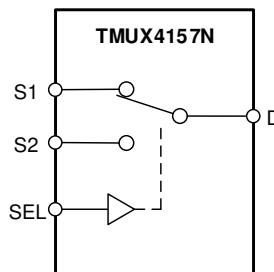


Figure 8-1. TMUX4157N Functional Block Diagram

8.3 Feature Description

8.3.1 Bidirectional Operation

The TMUX4157N conducts equally well from source (Sx) to drain (D) or from drain (D) to source (Sx). The device has very similar characteristics in both directions and supports both analog and digital signals.

8.3.2 Rail-to-Rail Operation

The valid signal path input or output voltage for TMUX4157N ranges from GND to VSS.

8.3.3 1.8 V Logic Compatible Inputs

The TMUX4157N has 1.8 V logic compatible control for the logic control input (SEL). The logic input threshold scales with supply but still provides 1.8 V logic control when operating at 5.5 V supply voltage. 1.8 V logic level inputs allow the TMUX4157N to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and BOM cost. Refer to [Simplifying Design with 1.8 V logic Muxes and Switches](#) for more information on 1.8 V logic implementations.

8.3.4 Fail-Safe Logic

The TMUX4157N supports Fail-Safe Logic on the control input pin (SEL) allowing for operation up to 5.5 V, regardless of the state of the supply pin. This feature allows voltages on the control pin to be applied before the supply pin, protecting the device from potential damage. Fail-Safe Logic minimizes system complexity by removing the need for power supply sequencing on the logic control pins. For example, the Fail-Safe Logic feature allows the select pin of the TMUX4157N to be ramped to 5.5 V while $V_{SS} = 0$ V. Additionally, the feature enables operation of the TMUX4157N with $V_{SS} = 1.2$ V while allowing the select pin to interface with a logic level of another device up to 5.5 V.

8.4 Device Functional Modes

The select (SEL) pin of the TMUX4157N controls which switch is connected to the drain of the device. When a given input is not selected, that source pin is in high impedance mode (HI-Z). The control pins can be as high as 5.5 V.

The TMUX4157N can be operated without any external components except for the supply decoupling capacitors. [Implications of Slow or Floating CMOS Inputs](#) highlights how the unused logic control pins should be tied to GND or logic high in order to ensure the device does not consume additional current. Unused signal path inputs (Sx or D) should be connected to GND.

8.5 Truth Tables

表 8-1. TMUX4157N Truth Table

CONTROL LOGIC (SEL)	Selected Source (Sx) Connected To Drain (D) Pin
0	S1
1	S2

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TMUX4157N system flexibility in GaN power amplifier biasing by supporting negative voltages across a wide operating supply (-4 V to -12 V). This device includes a 1.8 V logic compatible control input pin that enables operation in systems with 1.8 V I/O rails. These features allow the switch to reduce system complexity, board size, and overall system cost.

9.2 Typical Application

9.2.1 Negative Voltage Input Control for Power Amplifier

One application of the TMUX4157N is for input control of a power amplifier. Utilizing a switch allows a system to control when the DAC is connected to the power amplifier, and can stop biasing the power amplifier by switching the gate voltage. The ability to dynamically control the power amplifier is beneficial in multiple applications within communication equipment. [Figure 9-1](#) shows the TMUX4157N configured for control of the power amplifier.

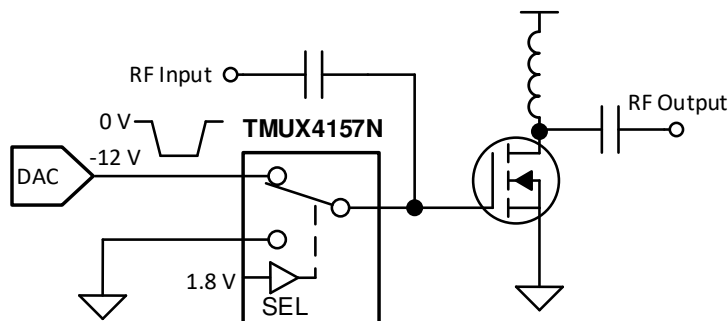


Figure 9-1. Input Control of Power Amplifier

9.2.1.1 Design Requirements

[Table 9-1](#) lists the parameters that are used in this design example.

Table 9-1. Design Parameters

PARAMETERS	VALUES
Supply (V_{SS})	-12 V
Switch I/O signal range	0 V to V_{SS} (Rail-to-Rail)
Control logic thresholds (SEL)	1.8 V compatible (up to 5.5 V)

9.2.1.2 Detailed Design Procedure

The application shown in [Figure 9-1](#) demonstrates how to toggle between the DAC output and GND for control of a GaN power amplifier using a single control input. The DAC output is utilized to bias the gate of the power amplifier and can be disconnected from the circuit using the select pin of the switch. The TMUX4157N can support 1.8-V logic signals on the control input, allowing the device to interface with low logic controls of an FPGA or MCU. The TMUX4157N can be operated without any external components except for the supply decoupling capacitors. The select pin is recommended to have a pull-down or pull-up resistor to ensure the input is in a known state if the control signal becomes disconnected. All inputs to the switch must fall within the recommended operating conditions of the TMUX4157N including signal range and continuous current.

9.2.1.3 Application Curve

A key parameter for this application is the transition time of the device. Faster transition time allows the system to toggle between input sources at a faster rate and allows the output to settle to the final value. [Figure 9-2](#) shows how the transition times varies with supply voltage.

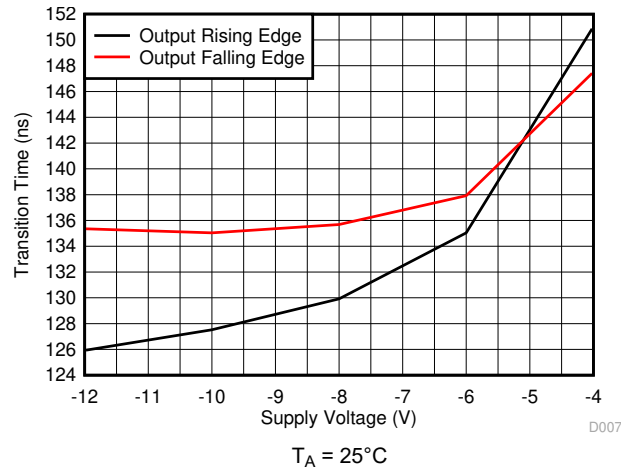


Figure 9-2. No Overshoot When Switching Between Inputs

10 Power Supply Recommendations

The TMUX4157N operates across a wide supply range of -4 V to -12 V. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the devices.

Power-supply bypassing improves noise margin and prevents switching noise propagation from the V_{SS} supply to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1 μ F to 10 μ F from V_{SS} to ground. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes.

11 Layout

11.1 Layout Guidelines

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection primarily occurs because the width of the trace changes. At the apex of the turn, the trace width increases to 1.414 times its width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. [Figure 11-1](#) shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

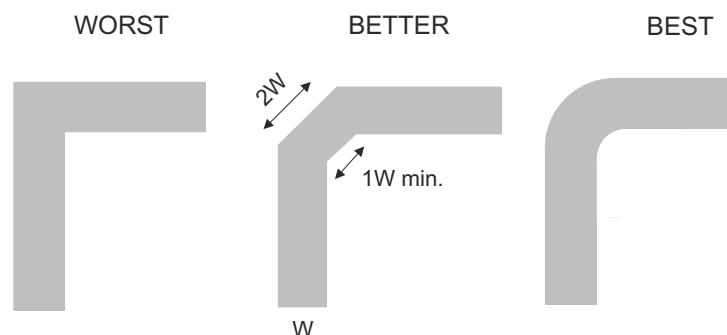


Figure 11-1. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

[Figure 11-2](#) illustrates an example of a PCB layout with the TMUX4157N. Some key considerations are:

- Decouple the V_{SS} pin with a 0.1- μ F capacitor, placed as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the V_{SS} supply.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

11.2 Layout Example

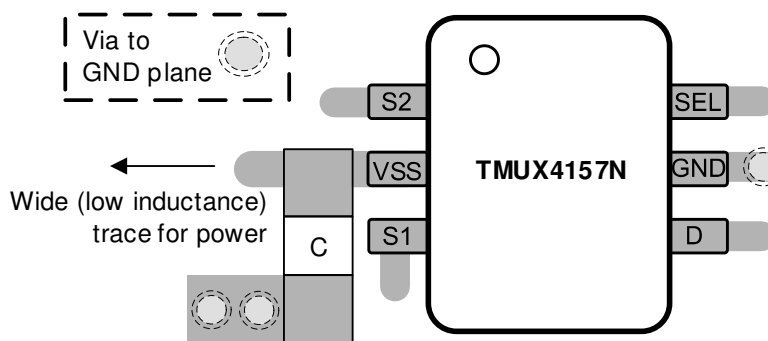


Figure 11-2. TMUX4157N Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

- Texas Instruments, [Eliminate Power Sequencing with Powered-off Protection Signal Switches application brief](#).
- Texas Instruments, [Improve Stability Issues with Low CON Multiplexers application brief](#).
- Texas Instruments, [Simplifying Design with 1.8 V logic Muxes and Switches application brief](#).
- Texas Instruments, [System-Level Protection for High-Voltage Analog Multiplexers application report](#).

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の[使用条件](#)を参照してください。

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

12.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい ESD 対策をとらないと、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

12.6 用語集

TI 用語集 この用語集には、用語や略語の一覧および定義が記載されています。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMUX4157NDCKR	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1
TMUX4157NDCKR.A	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1
TMUX4157NDCKRG4	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1
TMUX4157NDCKRG4.A	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUX4157NDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TMUX4157NDCKRG4	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUX4157NDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
TMUX4157NDCKRG4	SC70	DCK	6	3000	180.0	180.0	18.0



SOT - 1.1 max height

Technical drawing of a connector housing, showing three views: front, side, and cross-section.

Front View:

- Overall width: 2.4
- Pin pitch: 1.8
- Pin width: 1.4
- Pin 1 INDEX AREA (textured area)
- Pin 1 location: 1.3
- Pin 2 location: 4X 0.65
- Pin 3 location: 6X 0.30
- Pin 4 location: 0.15
- Pin 5 location: 0.15
- Pin 6 location: 0.15
- Pin 1 location: 1.3
- Pin 2 location: 4X 0.65
- Pin 3 location: 6X 0.30
- Pin 4 location: 0.15
- Pin 5 location: 0.15
- Pin 6 location: 0.15

Side View:

- Overall height: 2.15
- Pin width: 1.1
- Pin pitch: 0.8

Cross-section View:

- GAGE PLANE: 0.15
- SEATING PLANE: 0.08
- Base width: 0.46 TYP
- Top width: 0.22 TYP
- Bottom width: 0.08 TYP
- Angle: 4X 0°-12°
- Angle: 4X 4°-15°
- Angle: 8° TYP

Surface Texture Symbols:

- Symbol 1: $\sqrt{0.1}$ C A B
- Symbol 2: $\sqrt{0.1}$ C

NOTE 5

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

2. This drawing is subject to change without notice.

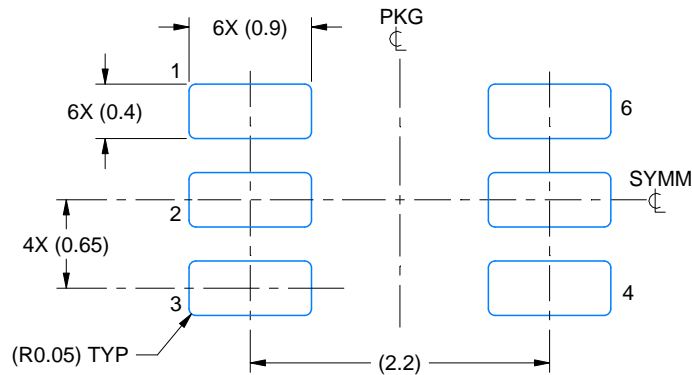
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.

4. Falls within JEDEC MO-203 variation AB.

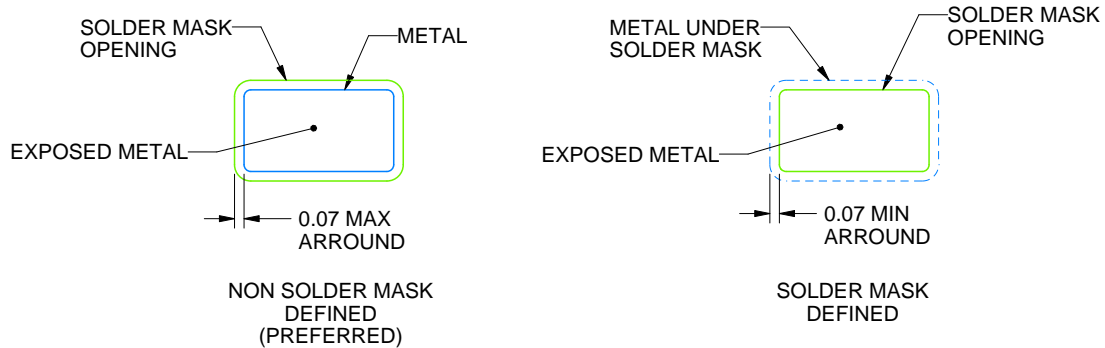
DCK0006A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4214835/D 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214835/D 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、TI は一切の責任を拒否します。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、[TI の総合的な品質ガイドライン](#)、[ti.com](#) または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

Copyright © 2025, Texas Instruments Incorporated

最終更新日：2025 年 10 月