TMUX1072 過電圧検出および保護機能付きの2チャネル、2:1アナログ・マルチプレクサ

1 特長

- 2.3V～5.5V の電源電圧範囲
- 電源オフ保護：
  V_{CC} = 0V のとき、I/O ピンは Hi-Z
- フォルト表示ピンによる 6V 過電圧および過熱検出
- COMピンで 18V の過電圧保護 (OVP)
- V_{CC} を超えて最高 5.5V までの信号に対応
- 低い R_{ON}：6Ω
- BW：1.2GHz (標準値)
- C_{ON}：4.5pF (標準値)
- 低消費電力のディセーブル・モード
- 1.8V 互換のロジック入力
- JESD 22 を超える ESD 保護
  - 人体モデル (HBM) 2000V
- 2.00mm × 1.70mm の小型 QFN パッケージで供給

2 アプリケーション

- データ・アクイジション (DAQ)
- 現場用計測機器
- ビデオ監視
- HVAC システム
- リア・カメラ

3 概要

TMUX1072は高速、2チャネル、2:1のアナログ・スイッチで、過電圧検出と電源オフ保護が内蔵されています。このデバイスは双方向で、2:1または1:2のスイッチとして使用でき、V_{CC}を超えて最高5.5Vまでの信号に対応できます。

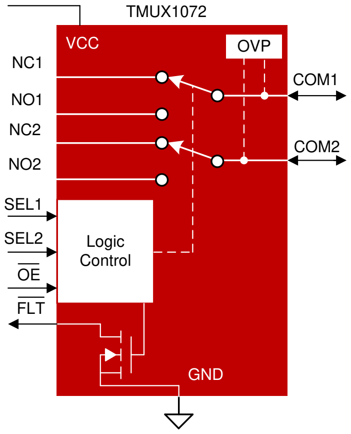
TMUX1072のI/Oピン上の保護機能は最高18Vまで耐えられ、自動シャットオフ回路により、スイッチより後にあるシステムの部品を損傷から保護できます。この保護機能は電源シーケンスに使用されます。システム内の一部の基板は、他の基板で信号の受信準備が整う前に電源オンにすることができます。このデバイスは過電圧および過熱イベントを検出し、$\overline{\text{FLT}}$ ピン経由でオープン・ドレイン信号を出力します。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TMUX1072	UQFN (12)	2.00mm×1.70mm
	VSSOP (10)	3.00mm×5.00mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

概略回路図



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

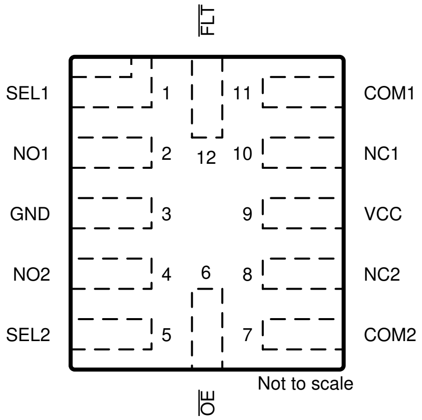
Revision B (June 2019) から Revision C に変更	**Page**
• 追加 Typical Characteristics curves for AC parameters	9
• Added the *Application Curves* section	18

Revision A (August 2018) から Revision B に変更	**Page**
• 「特長」を「COMピンで 0V～18V の過電圧保護 (OVP)」から「COMピンで 0V～6V の過電圧保護 (OVP)」に変更	1

2018年4月発行のものから更新	**Page**
• デバイスのステータスを「事前情報」から「量産データ」に変更	1

5 Pin Configuration and Functions

RUT Package
12-Pin UQFN
Top View



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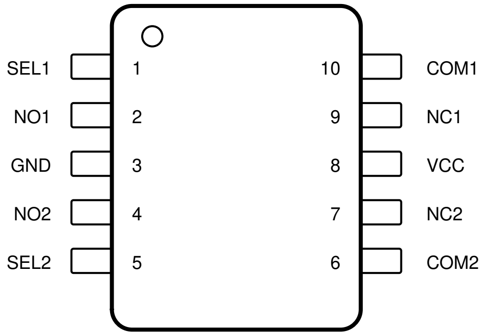
DGS Package
10-Pin VSSOP
Top View



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Pin Functions

PIN			I/O	DESCRIPTION
NAME	RUT	DGS		
SEL1	1	1	I	Switch select 1
NO1	2	2	I/O	Signal path NO1
GND	3	3	GND	Ground
NO2	4	4	I/O	Signal path NO2
SEL2	5	5	I	Switch select 2
$\overline{\text{OE}}$	6	-	I	Output enable (Active low)
COM2	7	6	I/O	Common signal path 2
NC2	8	7	I/O	Signal path NC2
VCC	9	8	PWR	Supply Voltage
NC1	10	9	I/O	Signal path NC1
COM1	11	10	I/O	Common signal path 1
$\overline{\text{FLT}}$	12	-	O	Fault indicator output pin (Active low) - open drain. If feature is unused, pin may be left floating or connected to ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(3)		–0.5	6	V
$V_{I/O}$	Input/Output DC voltage (COM1, COM2)(3)		–0.5	20	V
	Input/Output DC voltage (NC1, NO1, NC2, NO2) (3)		–0.5	6	V
V_I	Digital input voltage (SEL1, SEL2, $\overline{\text{OE}}$)		–0.5	6	V
V_O	Digital output voltage ($\overline{\text{FLT}}$)		–0.5	6	V
I_K	Input-output port diode current (COM1, COM2,NC1, NO1, NC2, NO2)	$V_{IN} < 0$	–50		mA
I_{IK}	Digital logic input clamp current (SEL1, SEL2, $\overline{\text{OE}}$) (3)	$V_I < 0$	–50		mA
I_{CC}	Continuous current through VCC			100	mA
I_{GND}	Continuous current through GND		–100		mA
T_{stg}	Storage temperature		–65	150	°C
T_J	Operating Junction Temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwise specified.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	5.5	V
$V_{I/O}$	Analog input/output	COM1, COM2	0	18	V
$V_{I/O}$		(NC1, NO1, NC2, NO2)	0	5.5	V
$I_{I/O}$		COM1, COM2	-50	50	mA
$I_{I/O}$		(NC1, NO1, NC2, NO2)	-50	50	mA
V_I	Digital input voltage	SEL1, SEL2, $\overline{\text{OE}}$	0	5.5	V
V_O	Digital output voltage	$\overline{\text{FLT}}$	0	5.5	V
$I_{I/O}$	Analog input/output port continuous current	(COM1, COM2, NC1, NO1, NC2, NO2)	-50	50	mA
I_{OL}	Digital output current			3	mA
T_A	Operating free-air temperature		–40	125	ºC
T_J	Junction temperature		–40	125	ºC

6.4 Thermal Information

THERMAL METRIC [1]		TMUX1072		UNIT
		RUT (UQFN)	DGS (VSSOP)	
		12 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	127	175	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	55.5	61.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	67.7	96.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.6	8.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	67.3	95.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

T_A = –40°C to +125°C , V_{CC} = 2.3 V to 5.5 V, GND = 0V, Typical values are at V_{CC} = 3.3 V, T_A = 25°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{CC}	Power supply voltage		2.3		5.5	V
I_{CC}	Active supply current	$\overline{OE}$ = 0 V SEL1, SEL2 = 0 V, 1.8 V or V_{CC} 0 V < $V_{I/O}$ < 3.6 V		75	110	µA
	Supply current during OVP condition	$\overline{OE}$ = 0 V SEL1, SEL2 = 0 V, 1.8 V or V_{CC} $V_{I/O}$ > V_{POS_THLD}		65	98	µA
I_{CC_PD} [1]	Standby powered down supply current	$\overline{OE}$ = 1.8 V or V_{CC} SEL1 = 0 V, 1.8 V, or VCC SEL2 = 0 V, 1.8 V, or VCC		3	10	µA
UVLO	Under Voltage Lock Out	V_{CC} = rising and falling	1.65			V
DC Characteristics						
R_{ON}	ON-state resistance	$V_{I/O}$ = 0 V to V_{CC} I_{SINK} = 8 mA Refer to ON-State Resistance Figure		6	18	Ω
ΔR_{ON}	ON-state resistance match between channels	$V_{I/O}$ = 0 V to V_{CC} I_{SINK} = 8 mA Refer to ON-State Resistance Figure		0.07	0.5	Ω
$R_{ON\ (FLAT)}$	ON-state resistance flatness	$V_{I/O}$ = 0 V to V_{CC} I_{SINK} = 8 mA Refer to ON-State Resistance Figure		2.5	7	Ω

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(1) Not tested for DGS package due to absence of FLT and OE pin.

Electrical Characteristics (continued)

T_A = –40°C to +125°C , V_{CC} = 2.3 V to 5.5 V, GND = 0V, Typical values are at V_{CC} = 3.3 V, T_A = 25°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OFF}	I/O pin OFF leakage current	$V_{COM1/2}$ = 0 V to 5.5 V (2) V_{CC} = 2.3 V to 5.5 V $V_{NC1/2}$ or $V_{NO1/2}$ = 5.5 V or 0 V Refer to Off Leakage Figure		3.6	10	µA
		$V_{COM1/2}$ = 5.5 V (2) V_{CC} = 5.5 V $V_{NC1/2}$ or $V_{NO1/2}$ = 5.5 V Refer to Off Leakage Figure			3	µA
		$V_{COM1/2}$ = 3.6 V (2) V_{CC} = 3.3 V $V_{NC1/2}$ or $V_{NO1/2}$ = 3.6 V Refer to Off Leakage Figure			2	µA
		$V_{COM1/2}$ = 5.5 V V_{CC} = 0 V $V_{NC1/2}$ or $V_{NO1/2}$ = 5.5 V Refer to Off Leakage Figure			15	µA
		$V_{COM1/2}$ = 3.6 V V_{CC} = 0 V $V_{NC1/2}$ or $V_{NO1/2}$ = 3.6 V Refer to Off Leakage Figure			10	uA
		$V_{COM1/2}$ = 1 V V_{CC} = 0 V $V_{NC1/2}$ or $V_{NO1/2}$ = 1 V Refer to Off Leakage Figure			2	uA
		$V_{COM1/2}$ = 18 V V_{CC} = 0 V, 5.5 V $V_{NC1/2}$ or $V_{NO1/2}$ = 0 V Refer to Off Leakage Figure		165	185	µA
I_{ON}	ON leakage current	$V_{COM1/2}$ = 5.5 V V_{CC} = 5.5 V $V_{NC1/2}$ and $V_{NO1/2}$ = high-Z Refer to On Leakage Figure		1.2	3.5	µA
		$V_{COM1/2}$ = 0 V to 5.5 V V_{CC} = 2.3-5.5 V $V_{NC1/2}$ and $V_{NO1/2}$ = high-Z Refer to On Leakage Figure			11.5	µA
Digital Characteristics						
V_{IH}	Input logic high	SEL1, SEL2, $\overline{OE}$	1.45			V
V_{IL}	Input logic low	SEL1, SEL2, $\overline{OE}$			0.5	V
V_{OL}	Output logic low	$\overline{FLT}$ I_{OL} = 3 mA			0.3	V
I_{IH}	Input high leakage current	SEL1, SEL2, $\overline{OE}$ = 1.8 V, V_{CC}	-1	2	5	µA
I_{IL}	Input low leakage current	SEL1, SEL2, $\overline{OE}$ = 0 V	-1	±0.2	1	µA
R_{PD}	Internal pull-down resistor on digital input pins	SEL1, SEL2		6	12	MΩ
		$\overline{OE}$		3	6	MΩ
C_I (3)	Digital input capacitance	SEL1, SEL2 = 0 V, 1.8 V or VCC f = 1 MHz		8		pF
Protection and Detection						
V_{OVP_TH}	OVP positive threshold		5.55	5.8	6.0	V
V_{OVP_HYST} (3)	OVP threshold hysteresis		40	100	300	mV

(2) Not tested on COM1/2 pins for DGS package due to the absence of OE pin
(3) Specified by design, not tested in production.

Electrical Characteristics (continued)

T_A = –40°C to +125°C , V_{CC} = 2.3 V to 5.5 V, GND = 0V, Typical values are at V_{CC} = 3.3 V, T_A = 25°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{SD_HYST} (3)	Thermal Shutdown Hysteresis		3		8	°C
T_{OTD_TH} (3)	Overtemperature detection threshold		135		165	°C
V_{CLAMP_V} (3)	Maximum voltage to appear on NC1/2 and NO1/2 pins during OVP scenario	$V_{COM1/2}$ = 0 to 18 V t_{RISE} and t_{FALL}(10% to 90 %) = 100 ns R_L = Open Switch on or off $\overline{OE}$ = 0 V	0		9.6	V
		$V_{COM1/2}$ = 0 to 18 V t_{RISE} and t_{FALL}(10% to 90 %) = 100 ns R_L = 50Ω Switch on or off $\overline{OE}$ = 0 V	0		9.0	V
t_{EN_OVP} (3)	OVP enable time	R_{PU} = 10 kΩ to VCC ($\overline{FLT}$) C_L = 35 pF Refer to OVP Timing Diagram Figure		0.6	3	µs
t_{REC_OVP} (3)	OVP recovery time	R_{PU} = 10 kΩ to VCC ($\overline{FLT}$) C_L = 35 pF Refer to OVP Timing Diagram Figure		1.5	5	µs

6.6 Dynamic Characteristics

T_A = –40°C to +125°C , V_{CC} = 2.3 V to 5.5V, GND = 0V, Typical values are at V_{CC} = 3.3 V, T_A = 25°C, (unless otherwise noted)

PARAMETER[1]		TEST CONDITIONS		MIN	TYP	MAX	UNIT
C_{OFF}	COM1, COM2 off capacitance	$V_{COM1/2}$ = 0 or 3.3 V, $\overline{\text{OE}}$ = V_{CC} f = 240 MHz	Switch OFF	1.2	4.0	6.2	pF
	NC1, NO1, NC2, NO2 off capacitance	$V_{COM1/2}$ = 0 or 3.3 V, $\overline{\text{OE}}$ = V_{CC} or $\overline{\text{OE}}$ = 0V with SEL1, SEL2 (switch not selected) f = 240 MHz	Switch OFF or not selected	1.2	4.0	6.2	pF
C_{ON}	COM1, COM2, NC1, NO1, NC2, NO2 on capacitance	$V_{COM1/2}$ = 0 or 3.3 V, f = 240 MHz	Switch ON	1.4	4.0	6.2	pF
O_{ISO}	Differential off isolation	RL = 50 Ω CL = 5 pF f = 100 kHz Refer to Off Isolation Figure	Switch OFF		-80		dB
		RL = 50 Ω CL = 5 pF f = 240 MHz Refer to Off Isolation Figure	Switch OFF		-22		dB
X_{TALK}	Channel to Channel crosstalk	RL = 50 Ω CL = 5 pF f = 100 kHz Refer to Crosstalk Figure	Switch ON		-90		dB
BW	Bandwidth	RL = 50 Ω; Refer to BW and Insertion Loss Figure	Switch ON		1.2		GHz
I_{LOSS}	Insertion loss	RL = 50 Ω f = TBD MHz; Refer to BW and Insertion Loss Figure	Switch ON		-0.8		dB

(1) Specified by design, not tested in production.

6.7 Timing Requirements

T_A = –40°C to +125°C , V_{CC} = 2.3 V to 5.5V, GND = 0V, Typical values are at V_{CC} = 3.3 V, T_A = 25°C, (unless otherwise noted)

PARAMETER[1]		TEST CONDITIONS		MIN	NOM	MAX	UNIT
t_{switch}	Switching time between channels (SEL1, SEL2 to output)	V_{NC} = 0.8 V Refer to Tswitch Timing Figure	R_L = 50 Ω, C_L = 5 pF, V_{CC} = 2.3 V to 5.5 V		0.9	1	µs
t_{on}	Device turn on time ($\overline{\text{OE}}$ to output)	V_{NC} = 0.8 V Refer to Ton and Toff Figure			200	250	µs
t_{off}	Device turn off time ($\overline{\text{OE}}$ to output)	V_{NC} = 0.8 V Refer to Ton and Toff Figure			1	10	µs
t_{off_Vcc}	Device turn off time V_{CC} to Switch off	V_{NC} = 0.8 V Refer to Ton and Toff Figure Ramp rate V_{CC} = 2.3 V to 0 V 250µs				250	µs
$t_{SK(P)}$	Skew of opposite transitions of same output (between COM1 and COM2)[1]	$V_{COM1/2}$ = V_{CC} Refer to Tsk Figure	R_L = 50 Ω, C_L = 1 pF, V_{CC} = 2.3 V to 5.5 V		9	50	ps
t_{pd}	Propagation delay[1]	$V_{COM1/2}$ = V_{CC} Refer to Tpd Figure	R_L = 50 Ω, C_L = 5 pF, V_{CC} = 2.3 V to 5.5 V		130	200	ps

(1) Specified by design, not tested in production.

6.8 Typical Characteristics

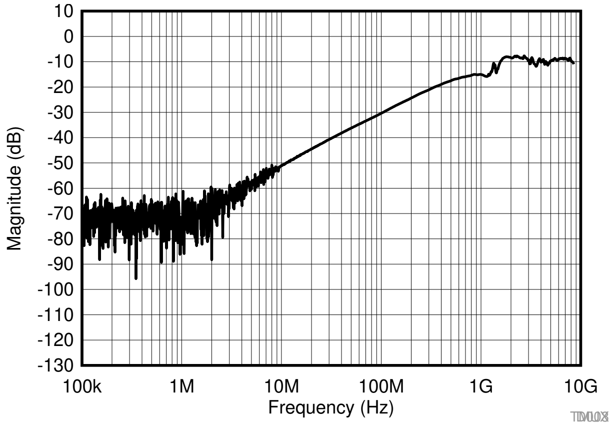


図 1. Off-Isolation vs Frequency

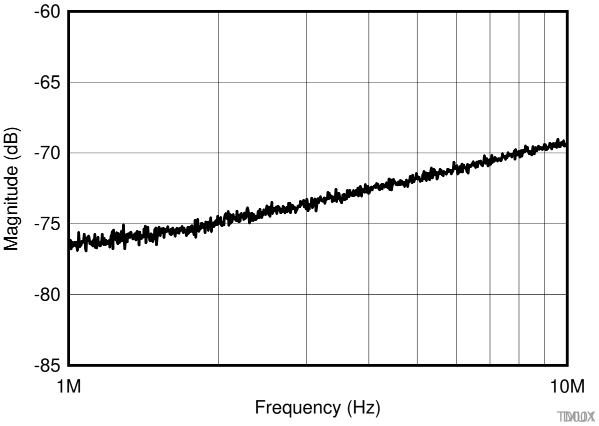


図 2. Xtalk vs Frequency

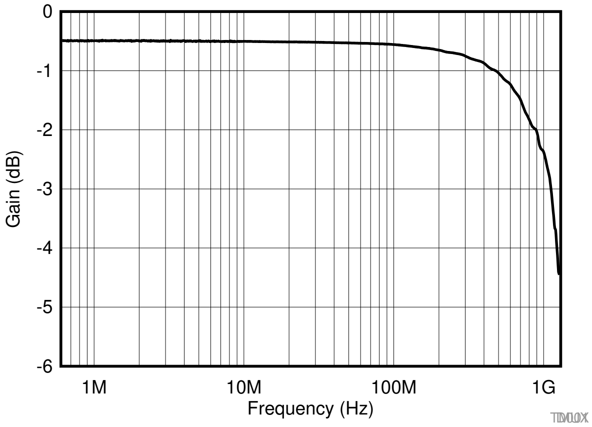
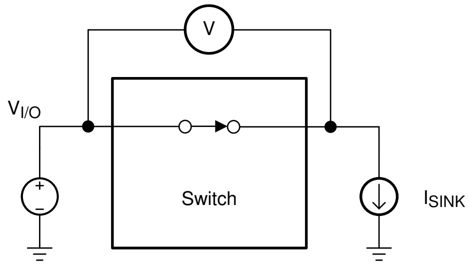


図 3. Bandwidth and Insertion Loss vs Frequency

7 Parameter Measurement Information



Channel ON, $R_{ON} = V/I_{SINK}$

図 4. ON-State Resistance (R_{ON})

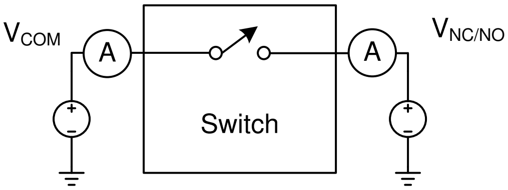


図 5. Off Leakage

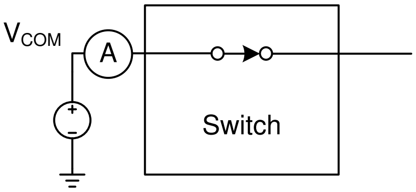
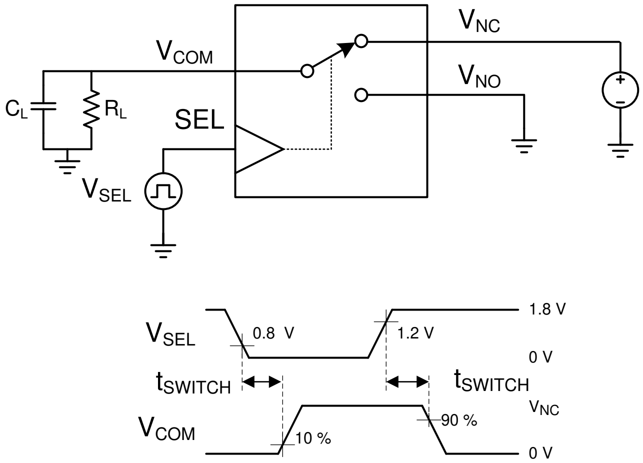


図 6. On Leakage

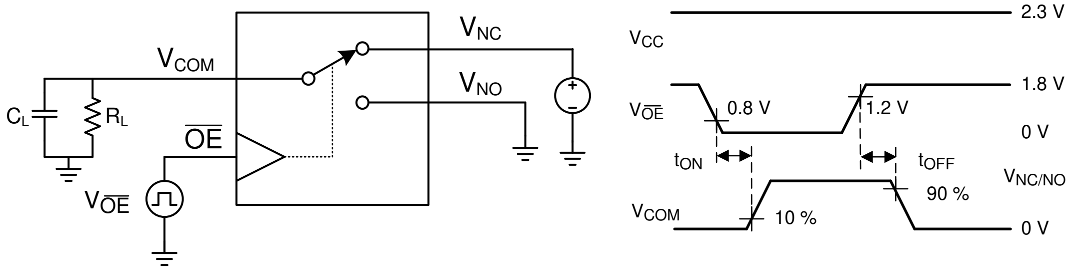


(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 500 ps, t_f < 500 ps.

(2) C_L includes probe and jig capacitance.

図 7. t_{SWITCH} Timing

Parameter Measurement Information (continued)



(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 500 ps, t_f < 500 ps.

(2) C_L includes probe and jig capacitance.

図 8. t_{ON}, t_{OFF} for $\overline{OE}$

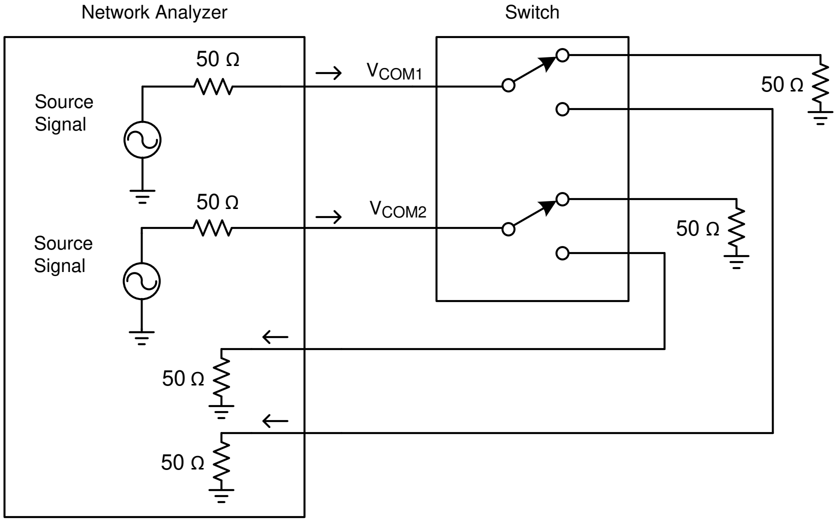


図 9. Off Isolation

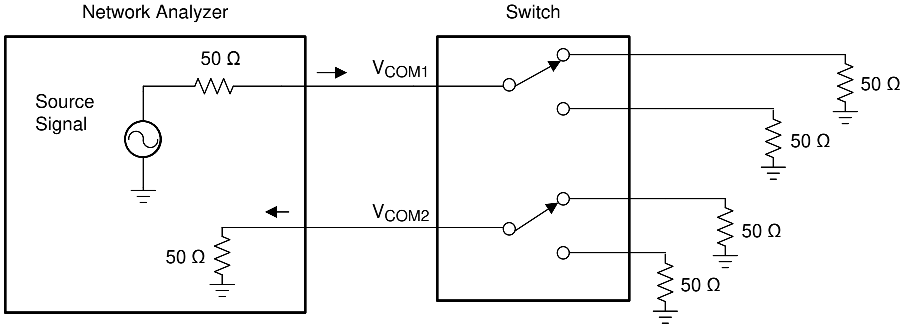


図 10. Cross Talk

Parameter Measurement Information (continued)

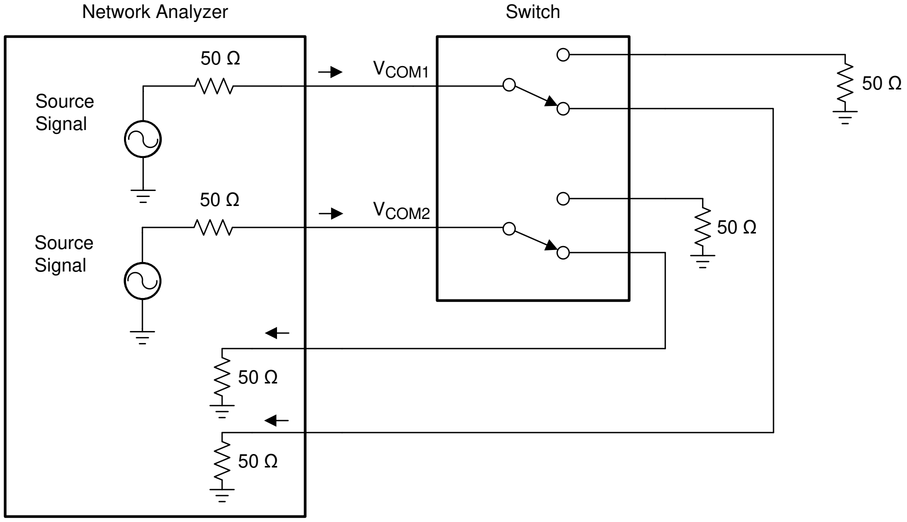


図 11. BW and Insertion Loss

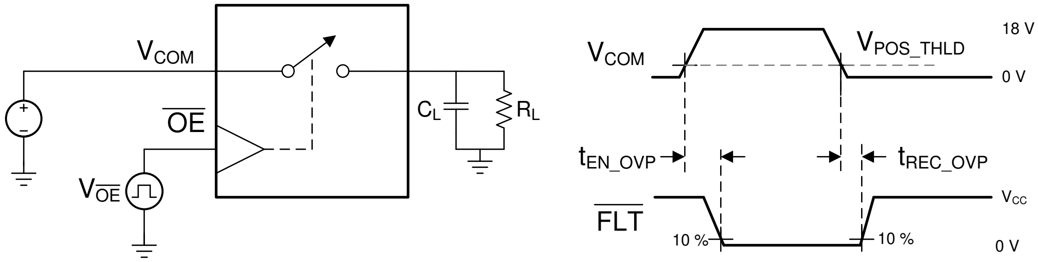
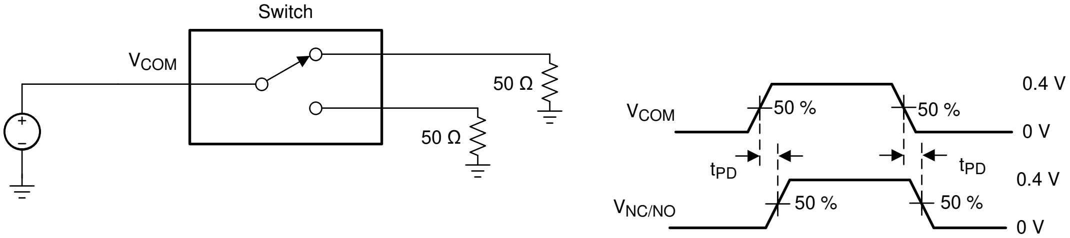


図 12. t_{EN_OVP} and t_{DIS_OVP} Timing Diagram

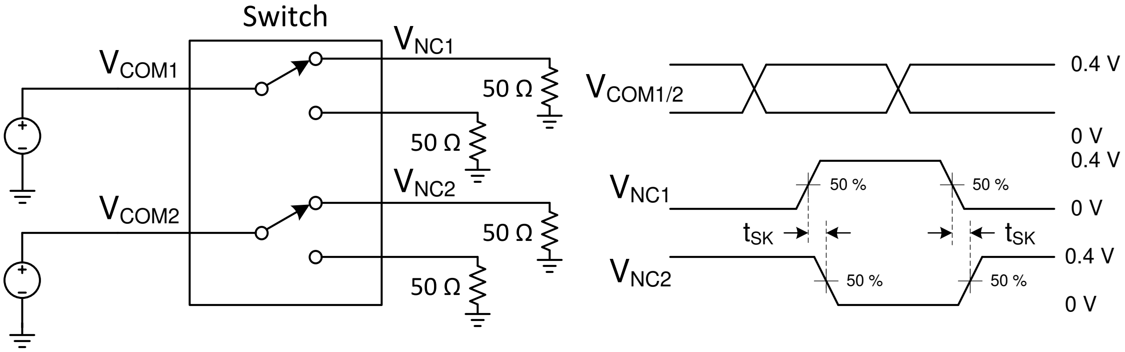


(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 500 ps, t_f < 500 ps.

(2) C_L includes probe and jig capacitance.

図 13. t_{PD}

Parameter Measurement Information (continued)



(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 500 ps, t_f < 500 ps.

(2) C_L includes probe and jig capacitance.

図 14. t_{SK}

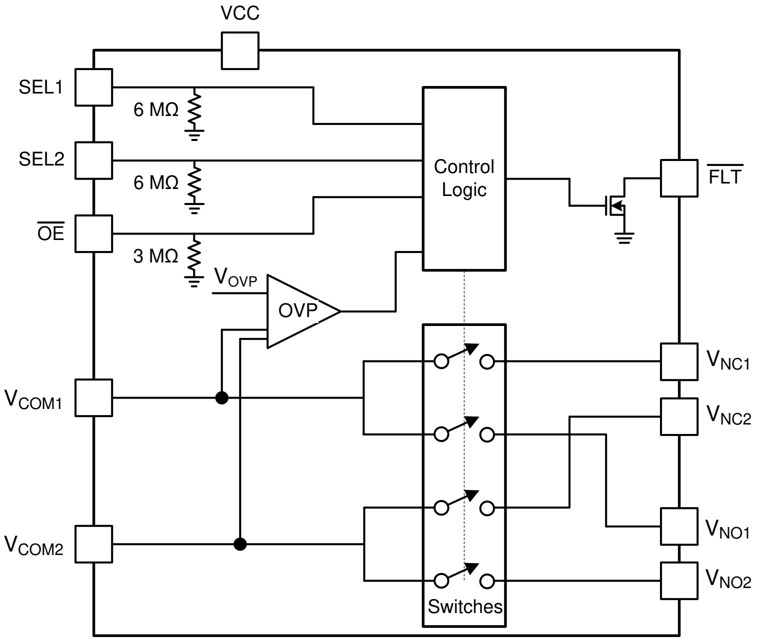
8 Detailed Description

8.1 Overview

The TMUX1072 is a high speed, 2-channel 2:1 analog switch with overvoltage protection. The device is bidirectional and can be used as a dual 2:1 or 1:2 switch, but OVP only applies to the COM pins. The device also contains a fault indicator pin which can signal to the system of either an over voltage or over temperature event.

The device maintains excellent signal integrity through the optimization of both R_{ON} and BW while protecting the system with up to 18 V OVP protection. The OVP implementation is designed to protect sensitive system components behind the switch that cannot survive fault conditions.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Powered-off Protection

When the TMUX1072 is powered off the I/Os of the device remain in a high-Z state. The crosstalk, off-isolation, and leakage remain within the *Electrical Specifications*

This prevents errant voltages from reaching the rest of the system and maintains isolation when the system is powering up.

8.3.2 Overvoltage Detection

When a voltage on the COM pin exceeds the V_{OVP_TH}, the open drain output $\overline{\text{FLT}}$pin pulls the pin low to indicate an overvoltage event has been detected. The open drain output will release the $\overline{\text{FLT}}$ pin when the voltage on the COM pin returns below the V_{OVP_TH}.

8.3.3 Overtemperature Detection

When the junction temperature of the device exceeds the overtemperature detection threshold T_{OTD_TH}, the open drain output $\overline{\text{FLT}}$ pin pulls the pin low to indicate an overtemperature event has been detected. The open drain output releases the $\overline{\text{FLT}}$ pin when the junction temperature returns below the T_{OTD_TH}.

8.3.4 Overvoltage Protection

The OVP of the TMUX1072 is designed to protect the system from overvoltage conditions up to 18 V on the COM1 and COM2 pins. This protection is valid even if Vcc = 0V. 図 15 depicts an event where up to 18 V could appear on COM1 and COM2 that could pass through the device and damage components behind the device.

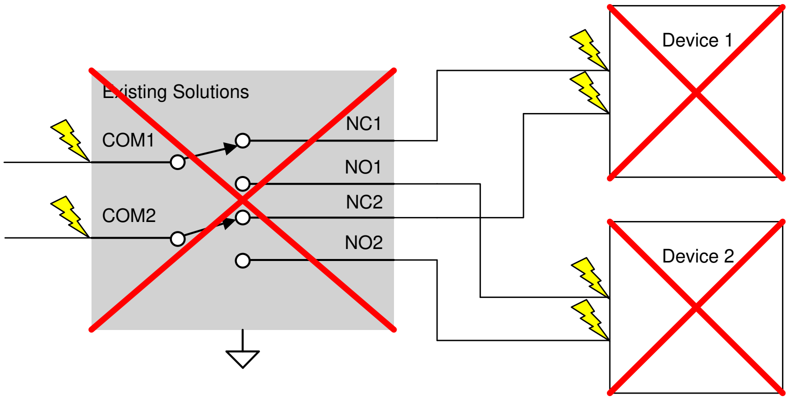


図 15. Existing Solution Being Damaged by a Short, 18 V

The TMUX1072 opens the switches and protect the rest of the system by blocking the 18 V as depicted in 図 16.

Feature Description (continued)

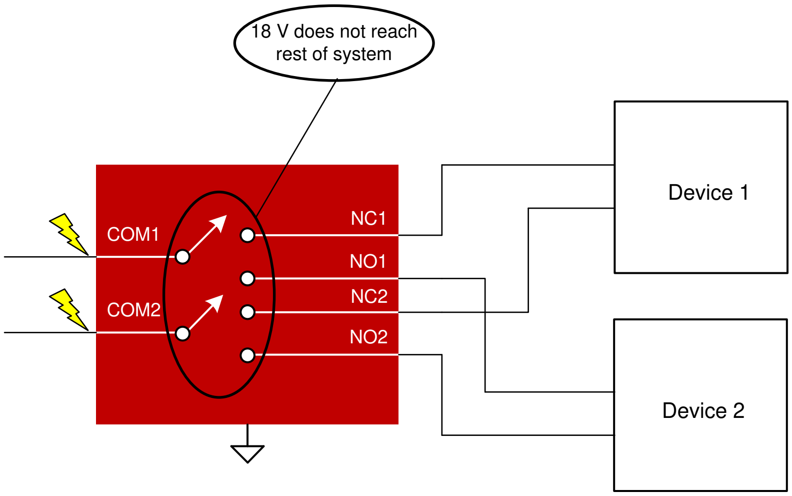


図 16. Protecting During a 18-V Short

図 17 is a waveform showing the voltage on the pins during an overvoltage scenario.

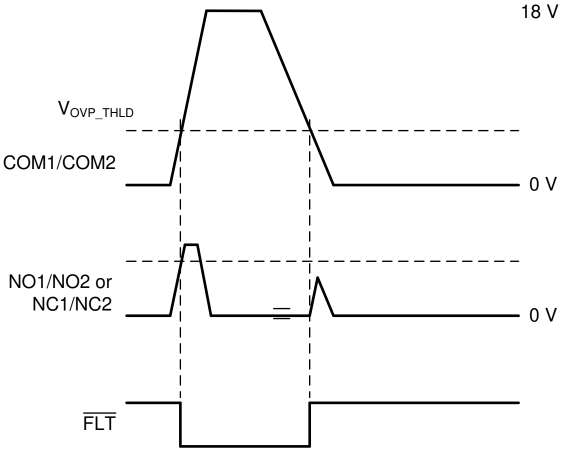


図 17. Overvoltage Protection Waveform, 18 V

8.4 Device Functional Modes

8.4.1 Pin Functions

表 1. Function Table

$\overline{OE}$	SEL1	SEL2	COM1 Connection	COM2 Connection
H	X	X	High-Z	High-Z
L	L	L	COM1 to NC1	COM2 to NC2
L	L	H	COM1 to NC1	COM2 to NO2
L	H	L	COM1 to NO1	COM2 to NC2
L	H	H	COM1 to NO1	COM2 to NO2

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

There are many applications in which processors and microcontrollers have a limited number of I/Os. This IC can effectively expand the limited number of I/Os by switching between multiple signal paths in order to interface them to a single processor or microcontroller. The device can also be used to connect a single microcontroller to two signal paths. With independent control of the two switches using SEL1 and SEL2, TMUX1072 can be used to cross switch single ended signals.

9.2 Typical Application

The TMUX1072 is used to switch signals between the high speed signal paths that may be exposed to a connector or near a bus which could experience an overvoltage condition. The TMUX1072 has internal pull-down resistors on SEL1, SEL2, and $\overline{\text{OE}}$. The pull-down on SEL1 and SEL2 pins ensure the NC1/NC2 channel is selected by default. The pull-down on $\overline{\text{OE}}$ enables the switch when power is applied.

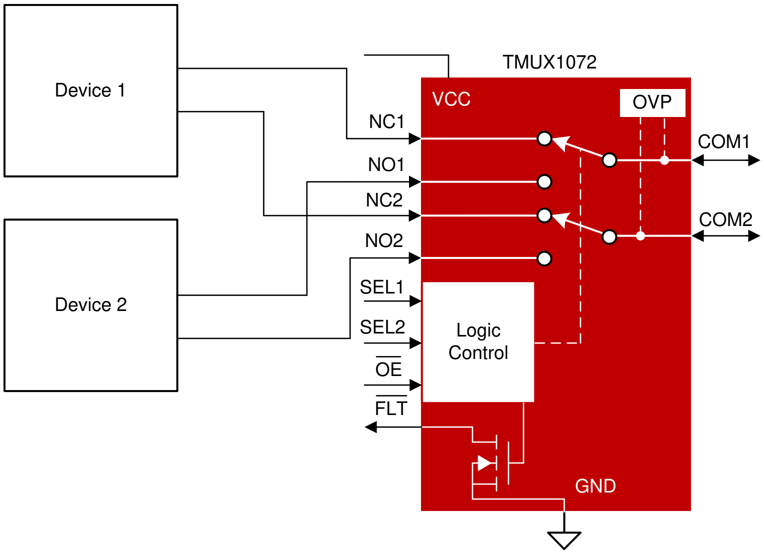


図 18. Typical TMUX1072 Application

9.2.1 Design Requirements

The TMUX1072 has internal pull-down resistors on SEL1, SEL2, and $\overline{\text{OE}}$, so no external resistors are required on the logic pins. The internal pull-down resistor on SEL1 and SEL2 pins ensures the NC1 and NC2 channels are selected by default. The internal pull-down resistor on $\overline{\text{OE}}$ enables the switch when power is applied to VCC.

The $\overline{\text{FLT}}$ indicator output pin is an open drain output that will require an external pull-up resistor for the overvoltage and overtemperature condition to be detected. If feature is unused, $\overline{\text{FLT}}$ pin may be left floating or connected to ground

9.2.2 Detailed Design Procedure

The TMUX1072 can be properly operated without any external components. However, TI recommends that unused signal pins must be connected to ground through a 50-Ω resistor to prevent signal reflections back into the device. TI does recommend a 100-nF bypass capacitor placed close to TMUX1072 VCC pin.

Typical Application (continued)

9.2.3 Application Curves

Bandwidth is defined as the range of frequencies that are attenuated by less than 3 dB when the input is applied to the source pin of an on-channel, and the output is measured at the drain pin of the TMUX1072. 図 19 shows the bandwidth of TMUX1072.

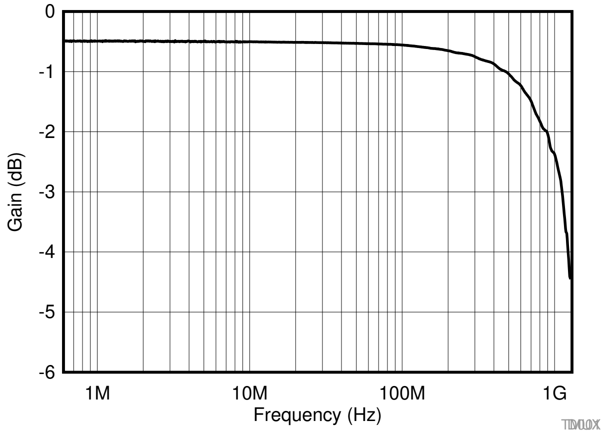


図 19. Bandwidth and Insertion Loss vs Frequency

10 Power Supply Recommendations

Power to the device is supplied through the VCC pin. TI recommends placing a 100-nF bypass capacitor as close to the supply pin VCC as possible to help smooth out lower frequency noise to provide better load regulation across the frequency spectrum.

11 Layout

11.1 Layout Guidelines

1. Place supply bypass capacitors as close to VCC pin as possible and avoid placing the bypass caps near the signal traces.
2. The high-speed traces should always be of equal length and must be no more than 4 inches; otherwise, the eye diagram performance may be degraded.
3. Route the high-speed signals using a minimum of vias and corners which will reduce signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the transmission line of the signal and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.
4. When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.
5. Do not route signal traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices, or IC’s that use or duplicate clock signals.
6. Avoid stubs on the high-speed signals because they cause signal reflections.
7. Route all high-speed signal traces over continuous planes (VCC or GND), with no interruptions.
8. Avoid crossing over anti-etch, commonly found with plane splits.
9. For high frequency systems, a printed circuit board with at least four layers is recommended: two signal layers separated by a ground layer and a power layer. The majority of signal traces should run on a single layer, preferably Signal 1. Immediately next to this layer should be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies. For more information on layout guidelines, see High Speed Layout Guidelines (SCAA082)

11.2 Layout Example

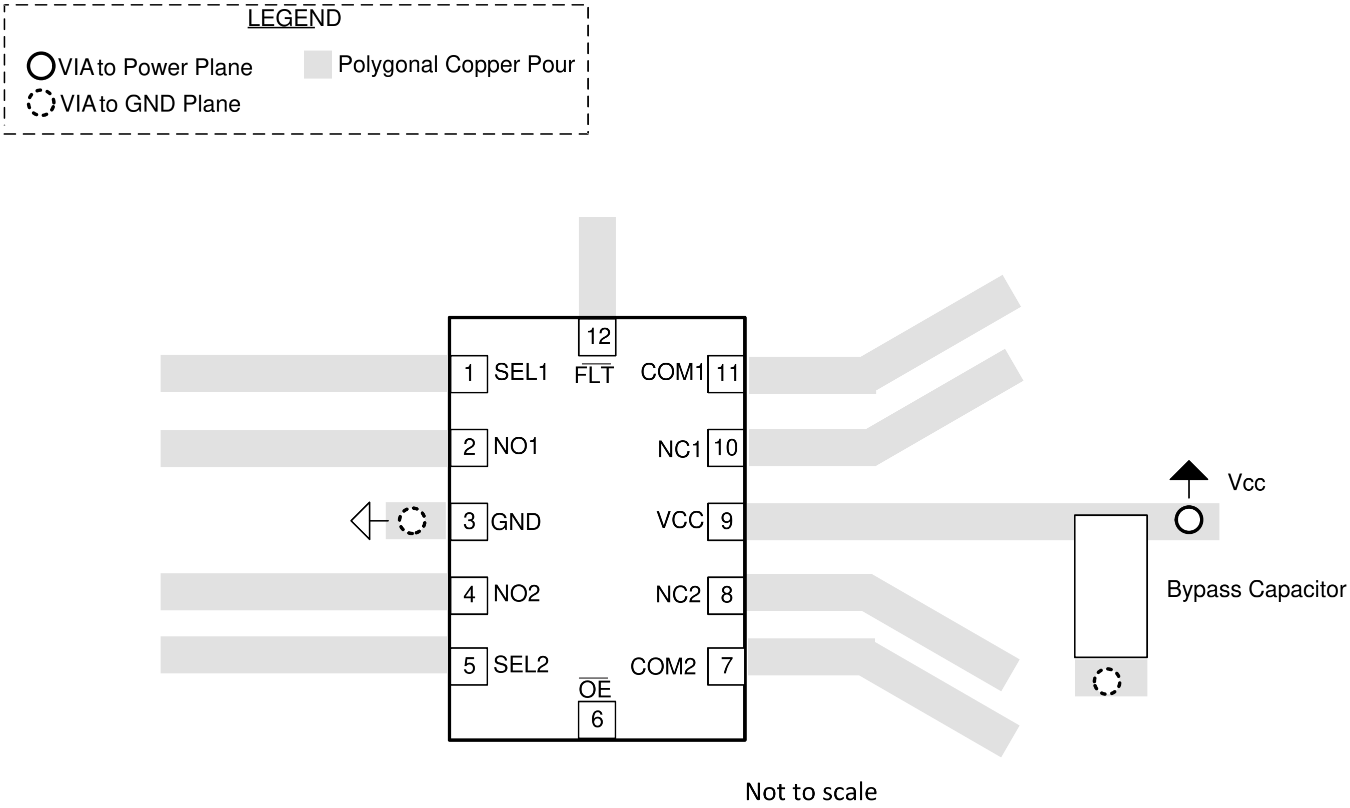


図 20. Layout Example

12 デバイスおよびドキュメントのサポート

12.1 ドキュメントのサポート

12.1.1 関連資料

関連資料については、以下を参照してください。

- *『高速レイアウト・ガイドライン』アプリケーション・レポート*
- *『高速インターフェイスのレイアウト・ガイドライン』*

12.2 ドキュメントの更新通知を受け取る方法

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12.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 商標

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12.5 静電気放電に関する注意事項

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静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMUX1072DGSR	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAUAG | SN	Level-1-260C-UNLIM	-40 to 125	1A9
TMUX1072DGSR.A	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1A9
TMUX1072RUTR	Active	Production	UQFN (RUT) | 12	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1BU
TMUX1072RUTR.A	Active	Production	UQFN (RUT) | 12	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1BU

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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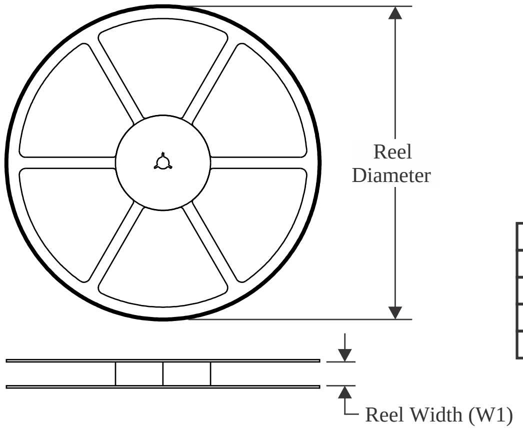
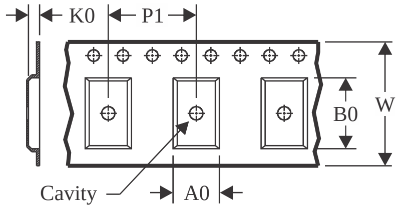
TAPE AND REEL INFORMATION

REEL DIMENSIONS

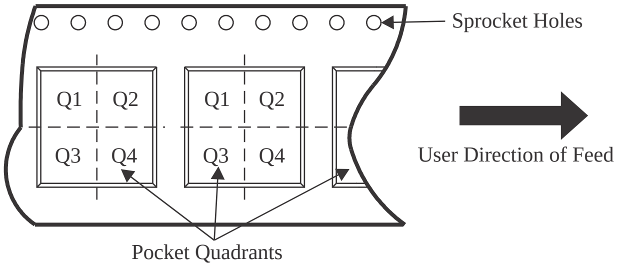


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

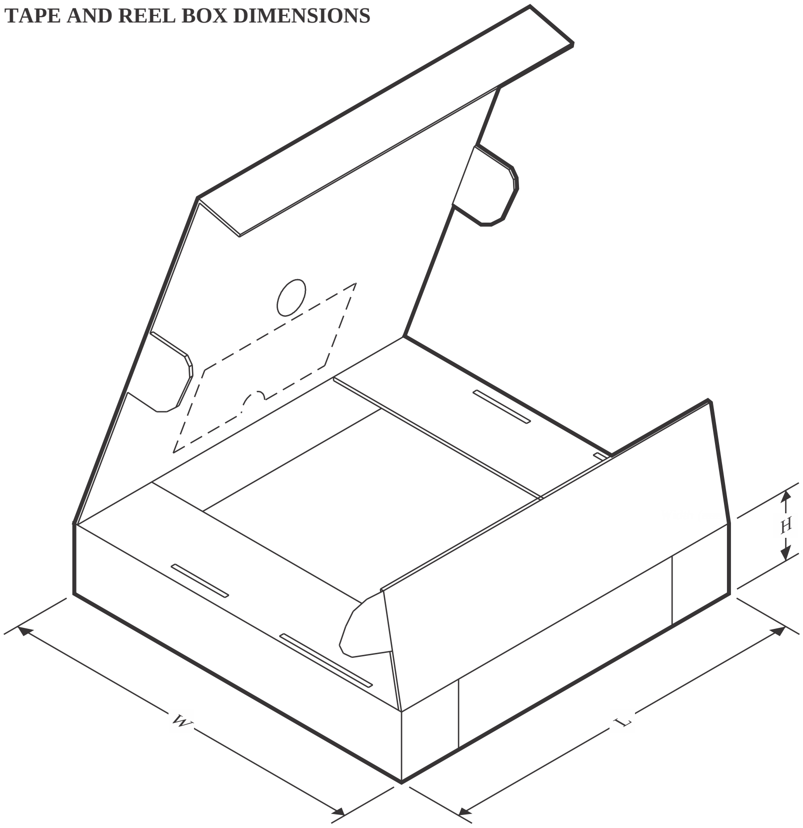
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUX1072DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
TMUX1072RUTR	UQFN	RUT	12	3000	180.0	9.5	1.9	2.2	0.7	4.0	8.0	Q1

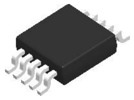
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUX1072DGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
TMUX1072RUTR	UQFN	RUT	12	3000	189.0	185.0	36.0

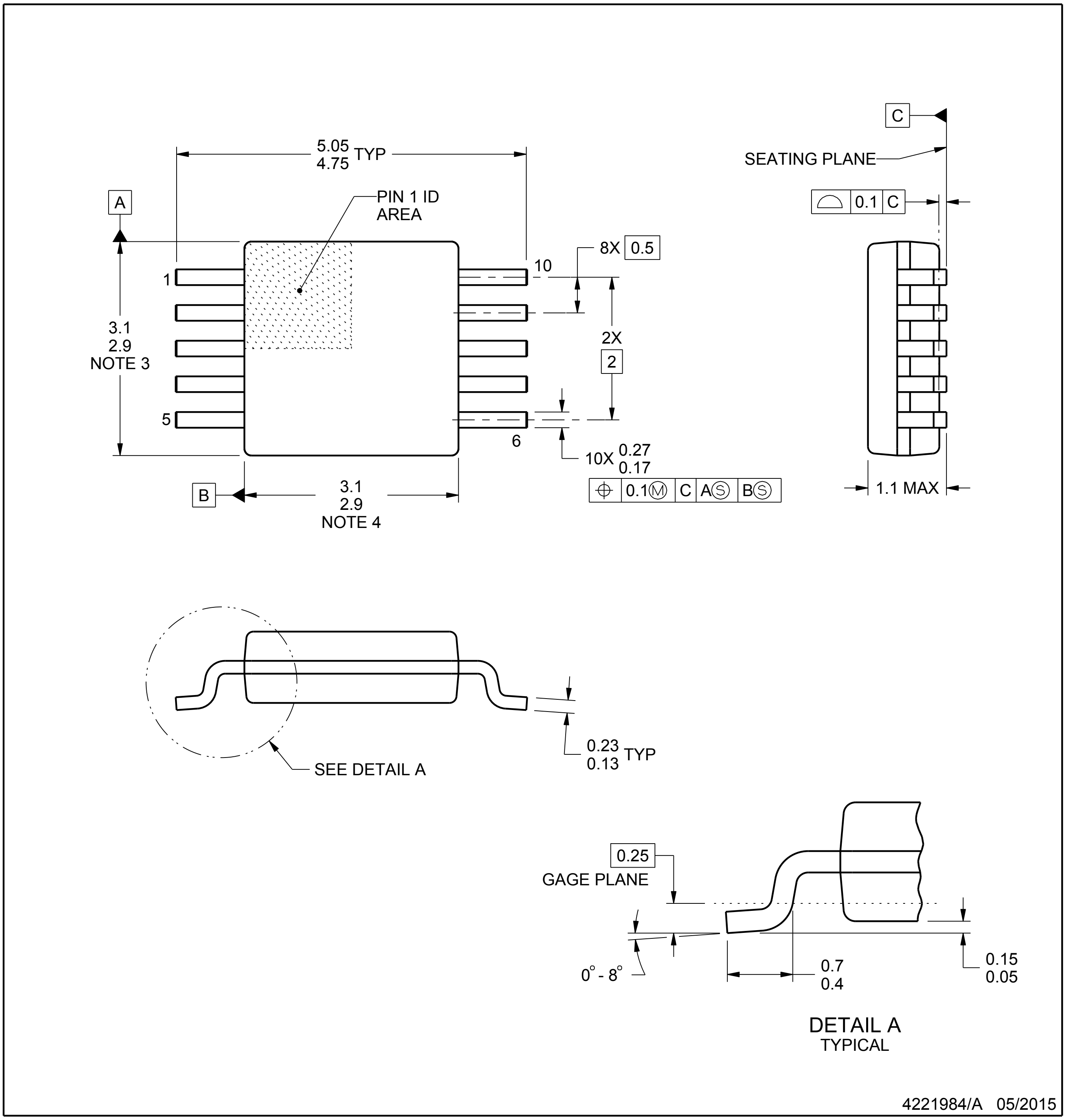
PACKAGE OUTLINE



DGS0010A

VSSOP - 1.1 mm max height

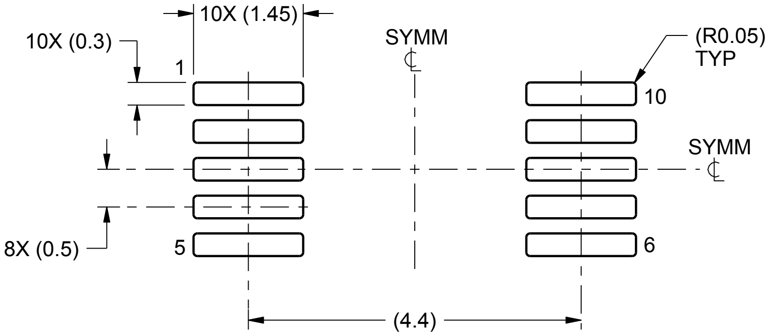
SMALL OUTLINE PACKAGE



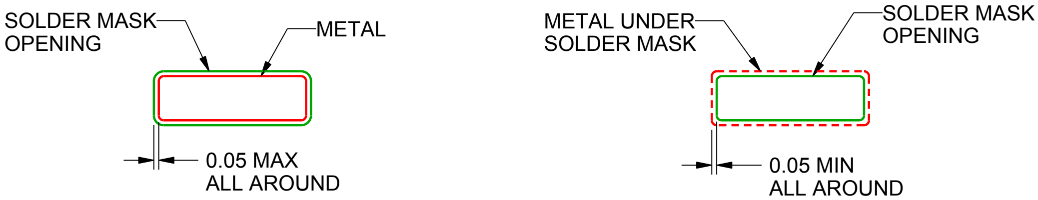
4221984/A 05/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X



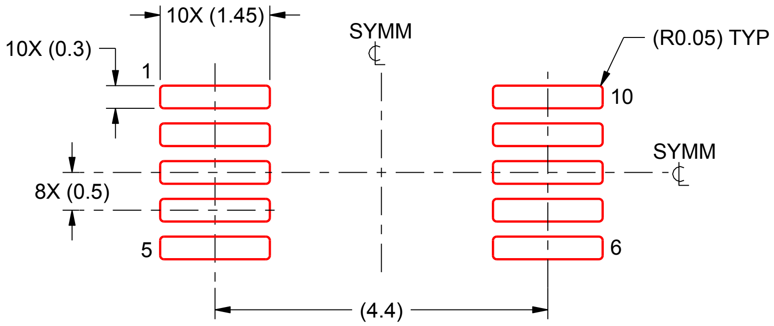
NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

NOTES: (continued)

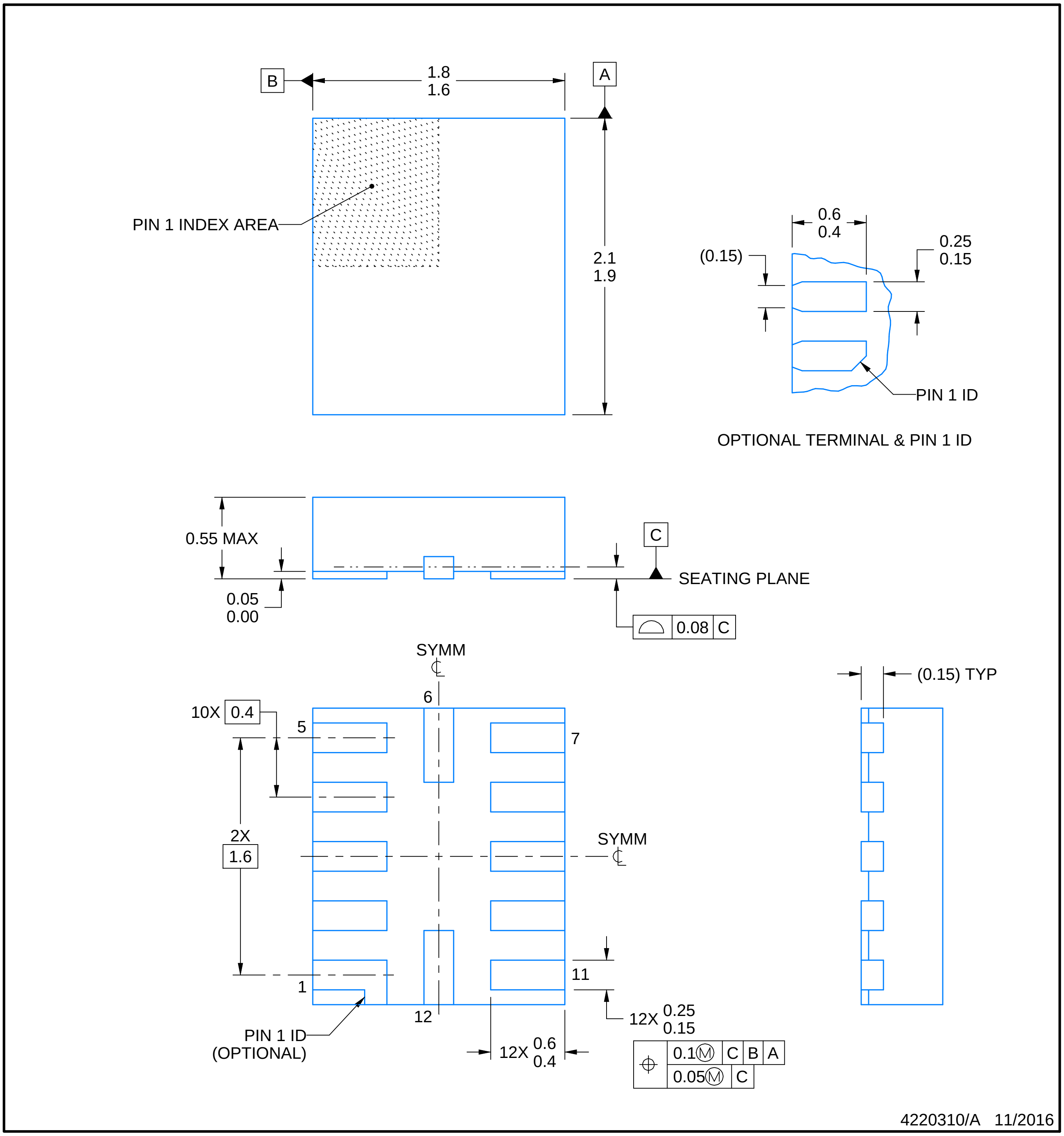
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

RUT0012A

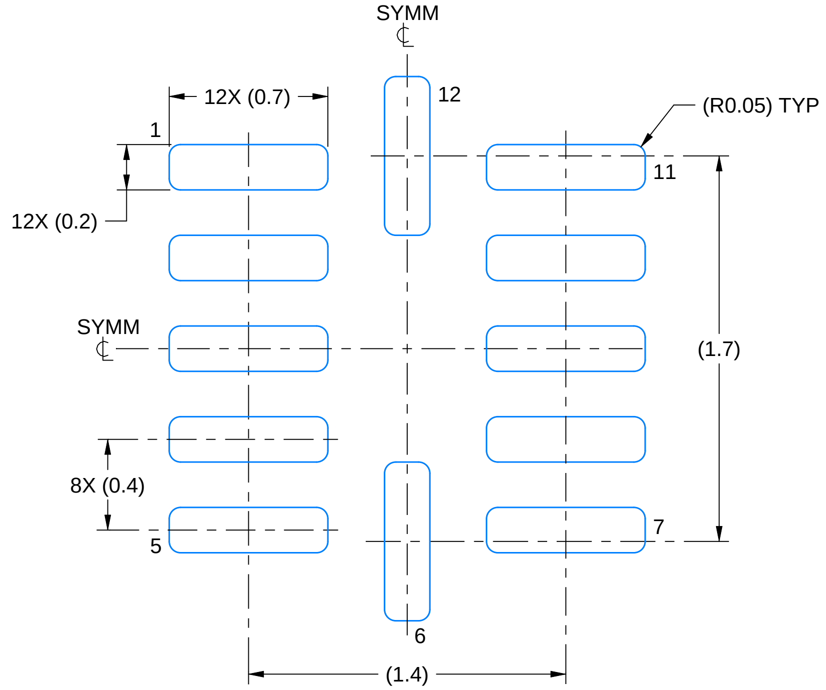
UQFN - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

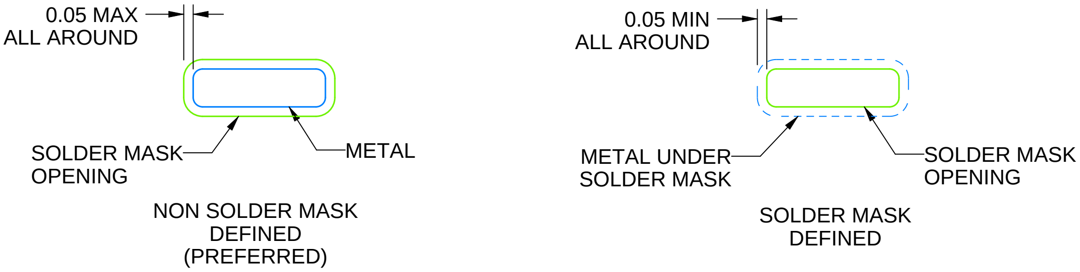


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



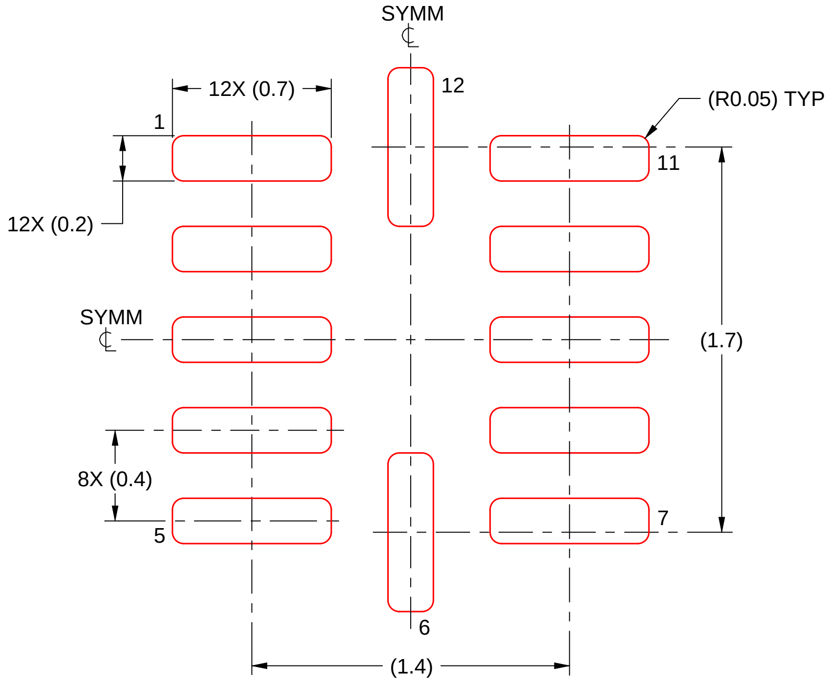
LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 30X

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

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