# TMS570LS3137 16- and 32-Bit RISC Flash Microcontroller

## 1 Device Overview

### 1.1 Features

- High-Performance Automotive-Grade Microcontroller for Safety-Critical Applications
  - Dual CPUs Running in Lockstep
  - ECC on Flash and RAM Interfaces
  - Built-In Self-Test (BIST) for CPU and On-chip RAMs
  - Error Signaling Module With Error Pin
  - Voltage and Clock Monitoring
- ARM® Cortex®-R4F 32-Bit RISC CPU
  - Efficient 1.66 DMIPS/MHz With 8-Stage Pipeline
  - FPU With Single- and Double-Precision
  - 12-Region Memory Protection Unit (MPU)
  - Open Architecture With Third-Party Support
- Operating Conditions
  - System Clock up to 180 MHz
  - Core Supply Voltage (VCC): 1.2 V Nominal
  - I/O Supply Voltage (VCCIO): 3.3 V Nominal
  - ADC Supply Voltage ($V_{CCAD}$): 3.0 to 5.25 V
- Integrated Memory
  - 3MB of Program Flash With ECC
  - 256KB of RAM With ECC
  - 64KB of Flash With ECC for Emulated EEPROM
- 16-Bit External Memory Interface
- Common Platform Architecture
  - Consistent Memory Map Across Family
  - Real-Time Interrupt (RTI) Timer OS Timer
  - 96-Channel Vectored Interrupt Module (VIM)
  - 2-Channel Cyclic Redundancy Checker (CRC)
- Direct Memory Access (DMA) Controller
  - 16 Channels and 32 Control Packets
  - Parity Protection for Control Packet RAM
  - DMA Accesses Protected by Dedicated MPU
- Frequency-Modulated Phase-Locked Loop (FMPLL) With Built-In Slip Detector
- Separate Nonmodulating PLL for FlexRay™
- Trace and Calibration Capabilities
  - Embedded Trace Macrocell (ETM-R4)
  - Data Modification Module (DMM)
  - RAM Trace Port (RTP)
  - Parameter Overlay Module (POM)
- Multiple Communication Interfaces
  - 10/100 Mbps Ethernet MAC (EMAC)
    - IEEE 802.3 Compliant (3.3-V I/O Only)
    - Supports MII, RMII, and MDIO
  - FlexRay Controller With Two Channels
    - 8KB of Message RAM With Parity Protection
    - Dedicated Transfer Unit (FTU)
  - Three CAN Controllers (DCANs)
    - 64 Mailboxes, Each With Parity Protection
    - Compliant to CAN Protocol Version 2.0B
  - Standard Serial Communication Interface (SCI)
  - Local Interconnect Network (LIN) Interface Controller
    - Compliant to LIN Protocol Version 2.1
    - Can be Configured as a Second SCI
  - Inter-Integrated Circuit ($I^2C$)
  - Three Multibuffered Serial Peripheral Interfaces (MibSPIs)
    - 128 Words With Parity Protection Each
  - Two Standard Serial Peripheral Interfaces (SPIs)
- Two Next Generation High-End Timer (N2HET) Modules
  - N2HET1: 32 Programmable Channels
  - N2HET2: 18 Programmable Channels
  - 160-Word Instruction RAM Each With Parity Protection
  - Each N2HET Includes Hardware Angle Generator
  - Dedicated High-End Transfer Unit (HTU) With MPU for Each N2HET
- Two 12-Bit Multibuffered ADC Modules
  - ADC1: 24 Channels
  - ADC2: 16 Channels Shared With ADC1
  - 64 Result Buffers With Parity Protection Each
- General-Purpose Input/Output (GPIO) Pins Capable of Generating Interrupts
  - Sixteen Pins on the ZWT Package
  - Four Pins on the PGE Package
- IEEE 1149.1 JTAG, Boundary Scan and ARM CoreSight™ Components
- JTAG Security Module
- Packages
  - 144-Pin Quad Flatpack (PGE) [Green]
  - 337-Ball Grid Array (ZWT) [Green]

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

## 1.2 Applications

- Braking Systems (Antilock Brake Systems and Electronic Stability Control)
- Electric Power Steering
- HEV and EV Inverter Systems
- Battery Management Systems
- Active Driver Assistance Systems
- Aerospace and Avionics
- Railway Communications
- Off-road Vehicles


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## 1.3 Description

The TMS570LS3137 device is a high-performance automotive-grade microcontroller family for safety systems. The safety architecture includes dual CPUs in lockstep, CPU and memory BIST logic, ECC on both the flash and the data SRAM, parity on peripheral memories, and loopback capability on peripheral I/Os.

The TMS570LS3137 device integrates the ARM Cortex-R4F Floating-Point CPU. The CPU offers an efficient 1.66 DMIPS/MHz, and has configurations that can run up to 180 MHz, providing up to 298 DMIPS. The device supports the word-invariant big-endian [BE32] format.

The TMS570LS3137 device has 3MB of integrated flash and 256KB of data RAM. Both the flash and RAM have single-bit error correction and double-bit error detection. The flash memory on this device is a nonvolatile, electrically erasable, and programmable memory implemented with a 64-bit-wide data bus interface. The flash operates on a 3.3-V supply input (same level as I/O supply) for all read, program, and erase operations. When in pipeline mode, the flash operates with a system clock frequency of up to 180 MHz. The SRAM supports single-cycle read and write accesses in byte, halfword, word, and double-word modes.

The TMS570LS3137 device features peripherals for real-time control-based applications, including two Next Generation High-End Timer (N2HET) timing coprocessors and two 12-bit Analog-to-Digital Converters (ADCs) supporting up to 24 inputs.

The N2HET is an advanced intelligent timer that provides sophisticated timing functions for real-time applications. The timer is software-controlled, using a reduced instruction set, with a specialized timer micromachine and an attached I/O port. The N2HET can be used for pulse-width-modulated outputs, capture or compare inputs, or GPIO. The N2HET is especially well suited for applications requiring multiple sensor information and drive actuators with complex and accurate time pulses. A High-End Timer Transfer Unit (HTU) can perform DMA-type transactions to transfer N2HET data to or from main memory. A Memory Protection Unit (MPU) is built into the HTU.

The device has two 12-bit-resolution MibADCs with 24 channels and 64 words of parity-protected buffer RAM each. The MibADC channels can be converted individually or can be grouped by software for sequential conversion sequences. Sixteen channels are shared between the two MibADCs. There are three separate groupings. Each sequence can be converted once when triggered or configured for continuous conversion mode. The MibADC has a 10-bit mode for use when compatibility with older devices or faster conversion time is desired.

The device has multiple communication interfaces: three MibSPIs, two SPIs, one LIN, one SCI, three DCANs, one I2C module, one Ethernet, and one FlexRay controller. The SPIs provide a convenient method of serial high-speed communication between similar shift-register type devices. The LIN supports the Local Interconnect standard 2.0 and can be used as a UART in full-duplex mode using the standard Non-Return-to-Zero (NRZ) format.

The DCAN supports the CAN 2.0 (A and B) protocol standard and uses a serial, multimaster communication protocol that efficiently supports distributed real-time control with robust communication rates of up to 1 Mbps. The DCAN is ideal for systems operating in noisy and harsh environments (for example, automotive vehicle networking and industrial fieldbus) that require reliable serial communication or multiplexed wiring.

The FlexRay controller uses a dual-channel serial, fixed time base multimaster communication protocol with communication rates of 10 Mbps per channel. A FlexRay Transfer Unit (FTU) enables autonomous transfers of FlexRay data to and from the CPU main memory. Transfers are protected by a dedicated, built-in MPU. The Ethernet module supports MII, RMII, and MDIO interfaces.

The I2C module is a multimaster communication module providing an interface between the microcontroller and an $I^2C$-compatible device through the $I^2C$ serial bus. The $I^2C$ supports speeds of 100 and 400 Kbps.

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The Frequency-Modulated Phase-Locked Loop (FMPLL) clock module is used to multiply the external frequency reference to a higher frequency for internal use. There are two FMPLL modules on this device. These modules, when enabled, provide two of the seven possible clock source inputs to the Global Clock Module (GCM). The GCM manages the mapping between the available clock sources and the device clock domains.

The device also has an External Clock Prescaler (ECP) module that when enabled, outputs a continuous external clock on the ECLK pin (or ball). The ECLK frequency is a user-programmable ratio of the peripheral interface clock (VCLK) frequency. This low-frequency output can be monitored externally as an indicator of the device operating frequency.

The DMA controller has 16 channels, 32 control packets, and parity protection on its memory. An MPU is built into the DMA to limit the DMA to prescribed areas of memory and to protect the rest of the memory system from any malfunction of the DMA.

The Error Signaling Module (ESM) monitors all device errors and determines whether an interrupt is generated or the external $\overline{\text{ERROR}}$ pin is toggled when a fault is detected. The $\overline{\text{ERROR}}$ pin can be monitored externally as an indicator of a fault condition in the microcontroller.

The External Memory Interface (EMIF) provides off-chip expansion capability with the ability to interface to synchronous DRAM (SDRAM) devices, asynchronous memories, peripherals or FPGA devices.

Several interfaces are implemented to enhance the debugging capabilities of application code. In addition to the built-in ARM Cortex-R4F CoreSight debug features, an External Trace Macrocell (ETM) provides instruction and data trace of program execution. For instrumentation purposes, a RAM Trace Port (RTP) module is implemented to support high-speed tracing of RAM and peripheral accesses by the CPU or any other master. A Data Modification Module (DMM) gives the ability to write external data into the device memory. Both the RTP and DMM have no or only minimum impact on the program execution time of the application code. A Parameter Overlay Module (POM) can reroute flash accesses to internal memory or to the EMIF. This rerouting allows the dynamic calibration against production code of parameters and tables without rebuilding the code to explicitly access RAM or halting the processor to reprogram the data flash.

With integrated safety features and a wide choice of communication and control peripherals, the TMS570LS3137 device is an ideal solution for high-performance real-time control applications with safety-critical requirements.

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE |
|---|---|---|
| TMS570LS3137ZWT | NFBGA (337) | 16.0 mm × 16.0 mm |
| TMS570LS3137PGE | LQFP (144) | 20.0 mm × 20.0 mm |

(1) For more information, see Section 9, *Mechanical Packaging and Orderable Information*.


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## 1.4 Functional Block Diagram

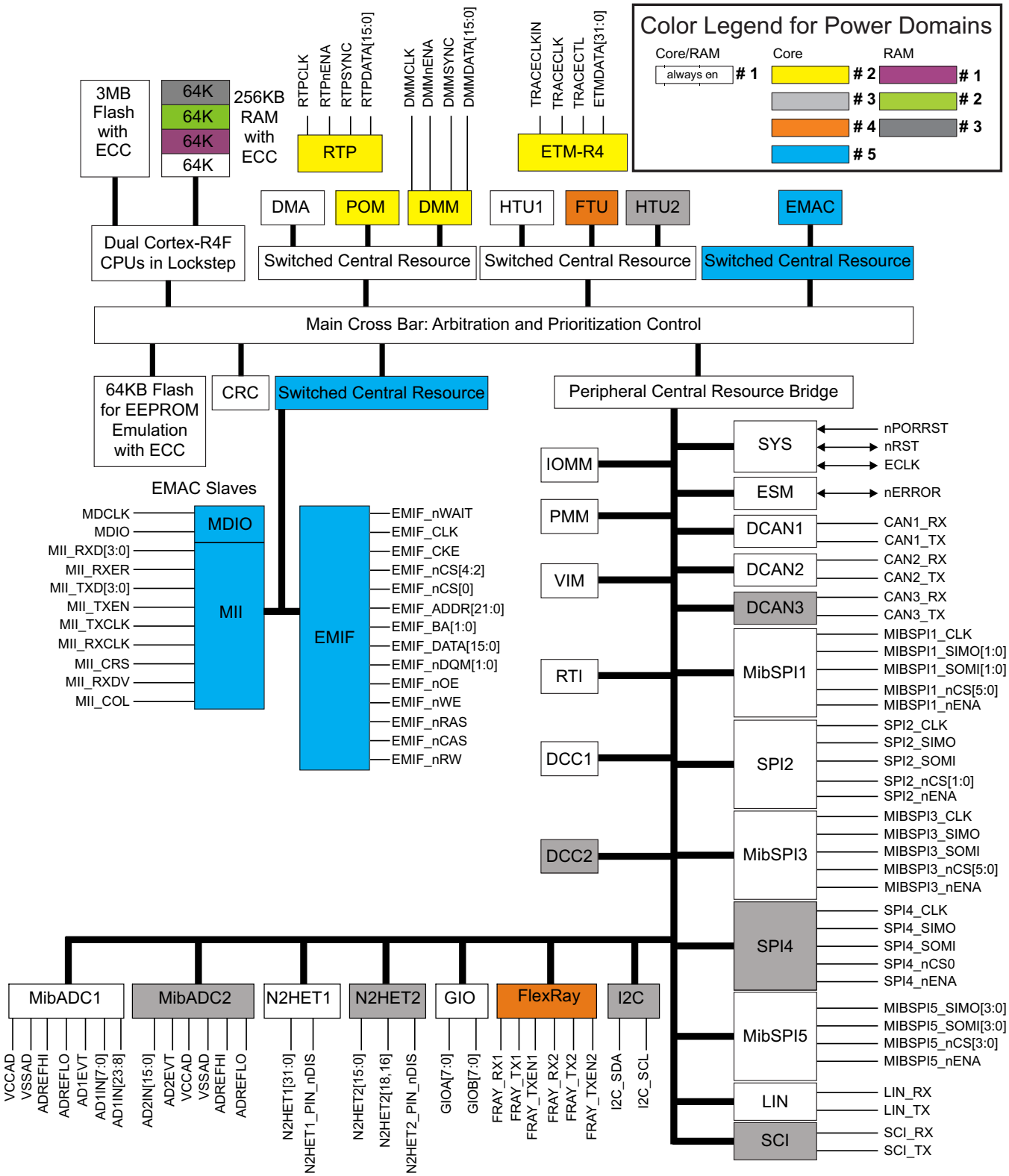


**Figure 1-1. Functional Block Diagram**

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## 2 Revision History

This data manual revision history highlights the technical changes made to the SPNS162B device-specific data manual to make it an SPNS162C revision.

**Scope:** Applicable updates to the Hercules™ TMS570 MCU device family, specifically relating to the TMS570LS3137 devices, which are now in the production data (PD) stage of development have been incorporated.

**Changes from August 1, 2013 to April 30, 2015 (from B Revision (July 2013) to C Revision)** **Page**

- Section 1 (Device Overview): Updated/Changed section title ..... 1
- Updated/Changed the N2HET feature ..... 1
- (Device Information): Added table ..... 4
- Added Section 3, Device Comparison ..... 9
- Section 4 (Terminal Configuration and Functions): Updated/Changed section title ..... 10
- Table 4-2 (PGE Enhanced High-End Timer Modules (N2HET1, N2HET2)): Updated/Changed N2HET1 time input capture or output compare pin description ..... 14
- Table 4-2: Added N2HET1_PIN_nDIS signal DESCRIPTION ..... 14
- Table 4-2: Updated/Changed N2HET2 time input capture or output compare pin description ..... 15
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- Table 4-3 Updated description about using GIOB[2] on pin 55 ..... 15
- Table 4-16 (PGE Test and Debug Modules Interface): Updated/Changed TEST pin description ..... 19
- Table 4-22 (ZWT Enhanced High-End Timer (N2HET) Modules): Updated/Changed N2HET1 time input capture or output compare pin description ..... 23
- Table 4-22 Added alternate terminals for N2HET1 pins 17, 19, 21, 23, 25, 27, 29 and 31 ..... 23
- Table 4-22: Added N2HET1_PIN_nDIS signal DESCRIPTION ..... 23
- Table 4-22: Updated/Changed N2HET2 time input capture or output compare pin description ..... 24
- Table 4-22: Added N2HET2_PIN_nDIS signal DESCRIPTION ..... 24
- Table 4-23 Updated description about using GIOB[2] on ball V10 ..... 25
- Table 4-32: Added "receive" to the RMII_CRS_DV pin Description ..... 29
- Table 4-32: Added "receive" to the MII_CRS pin Description ..... 29
- Table 4-34 (External Memory Interface (EMIF)): Global: Deleted EMIF_RNW pin function ..... 30
- Table 4-40 (ZWT Test and Debug Modules Interface): Updated/Changed TEST pin description ..... 36
- Table 4-42 (No Connects): Deleted NC pins A8, B8, and B9; supported on FlexRay Interface Controller ..... 37
- Section 5 (Specifications): Updated/Changed section title ..... 41
- Section 5.1 (Absolute Maximum Ratings): Reformatted table ..... 41
- Section 5.1 (Absolute Maximum Ratings): Updated/Changed $V_{CCAD}$ supply voltage range MAX value from "5.5" to "6.25" V ..... 41
- Section 5.1: Updated/Changed ADC input pins input voltage range MAX value from "5.5" to "6.25" V ..... 41
- Section 5.2 (ESD Ratings): Added table (new) ..... 41
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- Section 5.8 (Input/Output Electrical Characteristics): Updated/Changed Input Clamp Current from $I_{IC}$ to $I_{IK}$ ..... 45
- Section 5.9 (Thermal Resistance Characteristics): Moved section and updated/changed subsection title. ..... 46
- Table 5-2 (Thermal Resistance Characteristics (PGE Package)): Added test conditions and added $\Psi_{JT}$ row for PGE package ..... 46
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- Figure 6-10 (TCRAM Block Diagram): Updated/Changed figure, deleted A TCM ..... 80
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- Table 6-25 Added RAM power domain information in the table notes ..... 82
- Table 6-26(Memory Initialization): Updated/Changed N2HET2 RAM ending address from "0xFF**57**FFFF" to

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"0xFF**45**FFFF" ..... 83
- Table 6-38 Corrected base JTAG ID Base Value From 0xn**D**8A002F to 0xn**B**8A002F ..... 106
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- Controller Area Network (DCAN) Section 7.6.1 (Features): Updated/Changed TRM references to the correct document titles ..... 135
- Table 7-24 (SPI Master Mode External Timing Parameters (CLOCK PHASE = 0, SPICLK = output, SPISIMO = output, and SPISOMI = input)): Updated/Changed table footnote to "... CLOCK PHASE bit (SPIFMTx.16) is cleared" ..... 145
- Section 7.11.1 (Ethernet MII Electrical and Timing Specifications): Updated/Changed the MII parameter names and parametric descriptions for this section ..... 153
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- Section 7.11.3 (Management Data Input/Output (MDIO) Electrical and Timing Specifications): Updated/Changed section title for clarification ..... 156
- Table 7-32 (Timing Requirements for MDIO Input): Updated/Changed table title and formatting for clarification ..... 156
- Section 8 (Device and Documentation Support): Updated/Changed section to meet new requirements, including addition of several subsections ..... 157
- Section 8.7 (Device Identification Code Register): Added Device ID code value for silicon Rev D ..... 160
- Section 8.8 (Die Identification Registers): Updated/Changed the address of the two die identification registers (DIEIDL and DIEIDH) to point to the original registers at location 0xFFFFFF7C and 0xFFFFFF80 for this section. 161
- Table 8-2 (Die-ID Registers): Updated/Changed the BIT LOCATION column for all ITEM rows ..... 161
- Section 9 (Mechanical Packaging and Orderable Information): Updated/Changed section title ..... 168
- Section 9.1 (Packaging Information): Updated/Changed the paragraph ..... 168


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# 3 Device Comparison

lists the features of the devices.

**Table 3-1. TMS570LS3137 Device Comparison(1)(2)**

| FEATURES | DEVICES | | | | | |
|---|---|---|---|---|---|---|
| Generic Part Number | TMS570LC4357ZWT(3) | TMS570LS3137ZWT(3) | TMS570LS3137PGE(3) | TMS570LS3135ZWT | TMS570LS3135PGE | TMS570LS1227ZWT(3) |
| Package | 337 BGA | 337 BGA | 144 QFP | 337 BGA | 144 QFP | 337 BGA |
| CPU | ARM Cortex-R5F | ARM Cortex-R4F | ARM Cortex-R4F | ARM Cortex-R4F | ARM Cortex-R4F | ARM Cortex-R4F |
| Frequency (MHz) | 300 | 180 | 160 | 180 | 160 | 180 |
| Cache (KB) | 32 I<br>32 D | – | – | – | – | – |
| Flash (KB) | 4096 | 3072 | 3072 | 3072 | 3072 | 1280 |
| RAM (KB) | 512 | 256 | 256 | 256 | 256 | 192 |
| Data Flash [EEPROM] (KB) | 128 | 64 | 64 | 64 | 64 | 64 |
| EMAC | 10/100 | 10/100 | 10/100 | – | – | 10/100 |
| FlexRay | 2-ch | 2-ch | 2-ch | 2-ch | 2-ch | 2-ch |
| CAN | 4 | 3 | 3 | 3 | 3 | 3 |
| MibADC 12-bit (Ch) | 2 (41ch) | 2 (24ch) | 2 (24ch) | 2 (24ch) | 2 (24ch) | 2 (24ch) |
| N2HET (Ch) | 2 (64) | 2 (44) | 2 (40) | 2 (50) | 2 (50) | 2 (44) |
| ePWM Channels | 14 | – | – | – | – | 14 |
| eCAP Channels | 6 | – | – | – | – | 6 |
| eQEP Channels | 2 | – | – | – | – | 2 |
| MibSPI (CS) | 5 (4 x 6 + 2) | 3 (6 + 6 + 4) | 3 (5 + 6 + 1) | 3 (6 + 6 + 4) | 3 (5 + 6 + 1) | 3 (6 + 6 + 4) |
| SPI (CS) | – | 2 (2 + 1) | 1 (1) | 2 (2 + 1) | 1 (1) | 2 (2 + 1) |
| SCI (LIN) | 4 (2 with LIN) | 2 (1 with LIN) | 2 (1 with LIN) | 2 (1 with LIN) | 2 (1 with LIN) | 2 (1 with LIN) |
| $i^2C$ | 2 | 1 | 1 | 1 | 1 | 1 |
| GPIO (INT)(4) | 168 (with 16 interrupt capable) | 144 (with 16 interrupt capable) | 58 (with 4 interrupt capable) | 144 (with 16 interrupt capable) | 58 (with 4 interrupt capable) | 101 (with 16 interrupt capable) |
| EMIF | 16-bit data | 16-bit data | – | 16-bit data | – | 16-bit data |
| ETM (Trace) | 32-bit | 32-bit | – | 32-bit | – | – |
| RTP/DMM | 16/16 | 16/16 | – | 16/16 | – | – |
| Operating Temperature | -40ºC to 125ºC | -40ºC to 125ºC | -40ºC to 125ºC | -40ºC to 125ºC | -40ºC to 125ºC | -40ºC to 125ºC |
| Core Supply (V) | 1.14 V – 1.32 V | 1.14 V – 1.32 V | 1.14 V – 1.32 V | 1.14 V – 1.32 V | 1.14 V – 1.32 V | 1.14 V – 1.32 V |
| I/O Supply (V) | 3.0 V – 3.6 V | 3.0 V – 3.6 V | 3.0 V – 3.6 V | 3.0 V – 3.6 V | 3.0 V – 3.6 V | 3.0 V – 3.6 V |

(1) For additional device variants, see www.ti.com/tms570
(2) This table reflects the maximum configuration for each peripheral. Some functions are multiplexed and not all pins are available at the same time.
(3) Superset device
(4) Total number of pins that can be used as general-purpose input or output when not used as part of a peripheral

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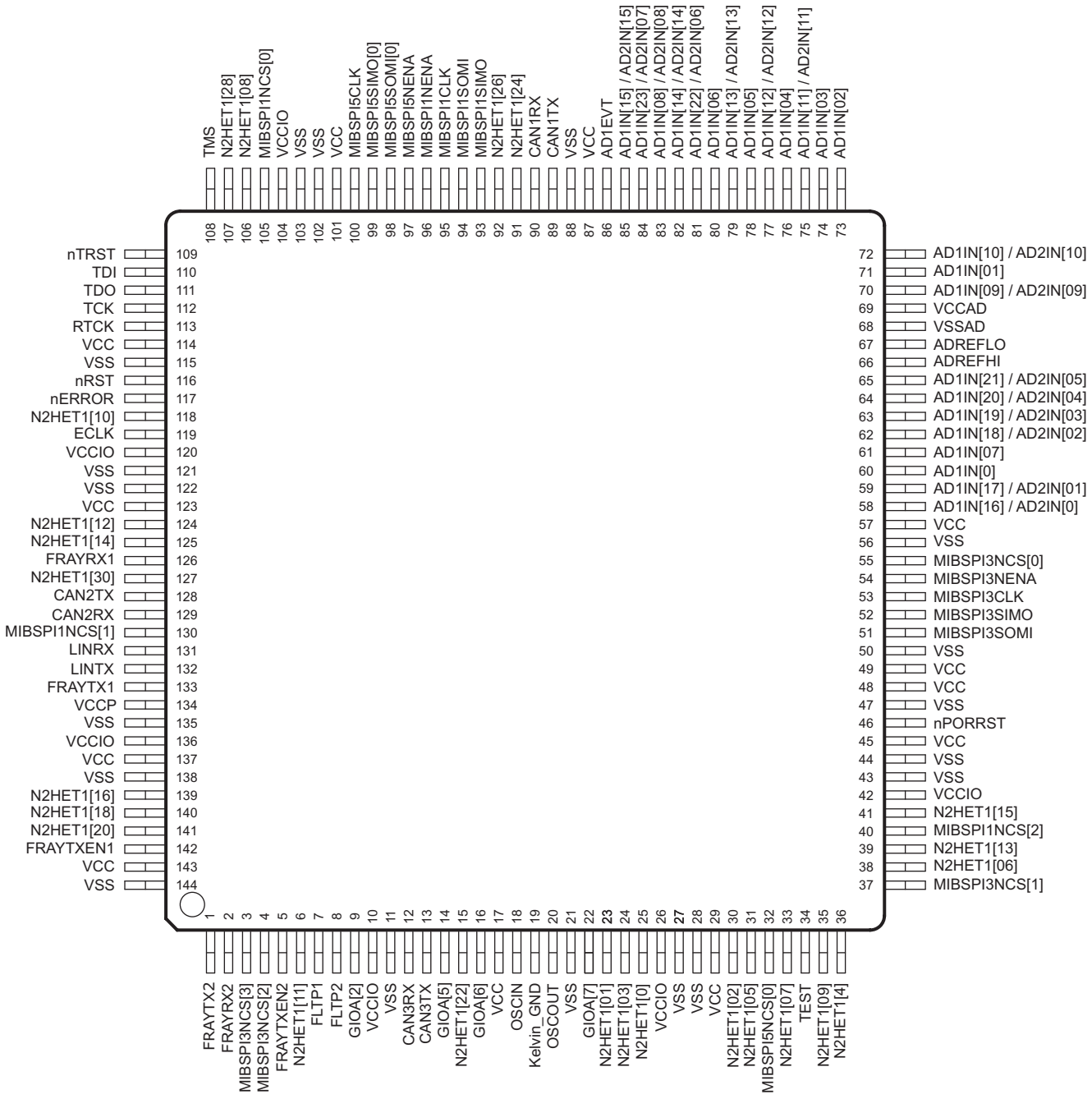
# 4 Terminal Configuration and Functions

## 4.1 PGE QFP Package Pinout (144-Pin)




A. Pins can have multiplexed functions. Only the default function is depicted in the figure.

**Figure 4-1. PGE QFP Package Pinout (144-Pin)(A)**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## 4.2 ZWT BGA Package Ball-Map (337-Ball Grid Array)

| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | R | T | U | V | W | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 19 | VSS | VSS | TMS | N2HET1 [10] | MIBSPI5 NCS[0] | MIBSPI1 SIMO | MIBSPI1 NENA | MIBSPI5 CLK | MIBSPI5 SIMO[0] | N2HET1 [28] | DMM_ DATA[0] | CAN3RX | AD1EVT | AD1IN[15] / AD2IN[15] | AD1IN[22] / AD2IN[06] | AD1IN [06] | AD1IN[11] / AD2IN[11] | VSSAD | VSSAD | 19 |
| 18 | VSS | TCK | TDO | nTRST | N2HET1 [08] | MIBSPI1 CLK | MIBSPI1 SOMI | MIBSPI5 NENA | MIBSPI5 SOMI[0] | N2HET1 [0] | DMM_ DATA[1] | CAN3TX | NC | AD1IN[08] / AD2IN[08] | AD1IN[14] / AD2IN[14] | AD1IN[13] / AD2IN[13] | AD1IN [04] | AD1IN [02] | VSSAD | 18 |
| 17 | TDI | $\overline{RST}$ | EMIF_ ADDR[21] | EMIF_ nWE | MIBSPI5 SOMI[1] | DMM_ CLK | MIBSPI5 SIMO[3] | MIBSPI5 SIMO[2] | N2HET1 [31] | EMIF_ nCS[3] | EMIF_ nCS[2] | EMIF_ nCS[4] | EMIF_ nCS[0] | NC | AD1IN [05] | AD1IN [03] | AD1IN[10] / AD2IN[10] | AD1IN [01] | AD1IN[09] / AD2IN[09] | 17 |
| 16 | RTCK | FRAY TXEN1 | EMIF_ ADDR[20] | EMIF_ BA[1] | MIBSPI5 SIMO[1] | DMM_ NENA | MIBSPI5 SOMI[3] | MIBSPI5 SOMI[2] | DMM_ SYNC | NC | NC | NC | NC | NC | AD1IN[23] / AD2IN[07] | AD1IN[12] / AD2IN[12] | AD1IN[19] / AD2IN[03] | ADREFLO | VSSAD | 16 |
| 15 | FRAY RX1 | FRAY TX1 | EMIF_ ADDR[19] | EMIF_ ADDR[18] | ETM DATA[06] | ETM DATA[05] | ETM DATA[04] | ETM DATA[03] | ETM DATA[02] | ETM DATA[16] / EMIF_ DATA[0] | ETM DATA[17] / EMIF_ DATA[1] | ETM DATA[18] / EMIF_ DATA[2] | ETM DATA[19] / EMIF_ DATA[3] | NC | NC | AD1IN[21] / AD2IN[05] | AD1IN[20] / AD2IN[04] | ADREFHI | VCCAD | 15 |
| 14 | N2HET1 [26] | nERROR | EMIF_ ADDR[17] | EMIF_ ADDR[16] | ETM DATA[07] | VCCIO | VCCIO | VCCIO | VCC | VCC | VCCIO | VCCIO | VCCIO | VCCIO | NC | NC | AD1IN[18] / AD2IN[02] | AD1IN [07] | AD1IN [0] | 14 |
| 13 | N2HET1 [17] | N2HET1 [19] | EMIF_ ADDR[15] | NC | ETM DATA[12] / EMIF_BA[0] | VCCIO | | | | | | | | VCCIO | ETM DATA[01] | NC | AD1IN[17] / AD2IN[01] | AD1IN[16] / AD2IN[0] | NC | 13 |
| 12 | ECLK | N2HET1 [04] | EMIF_ ADDR[14] | NC | ETM DATA[13] / EMIF_nOE | VCCIO | | VSS | VSS | VCC | VSS | VSS | | VCCIO | ETM DATA[0] | MIBSPI5 NCS[3] | NC | NC | NC | 12 |
| 11 | N2HET1 [14] | N2HET1 [30] | EMIF_ ADDR[13] | NC | ETM DATA[14] / EMIF_ nDQM[1] | VCCIO | | VSS | VSS | VSS | VSS | VSS | | VCCPLL | ETME TRACE CTL | NC | NC | NC | NC | 11 |
| 10 | CAN1TX | CAN1RX | EMIF_ ADDR[12] | NC | ETM DATA[15] / EMIF_ nDQM[0] | VCC | | VCC | VSS | VSS | VSS | VCC | | VCC | ETM TRACE CLKOUT | NC | NC | MIBSPI3 NCS[0] | GIOB[3] | 10 |
| 9 | N2HET1 [27] | FRAY TXEN2 | EMIF_ ADDR[11] | NC | ETM DATA[08] / EMIF_ ADDR[5] | VCC | | VSS | VSS | VSS | VSS | VSS | | VCCIO | ETM TRACE CLKIN | NC | NC | MIBSPI3 CLK | MIBSPI3 NENA | 9 |
| 8 | FRAY RX2 | FRAY TX2 | EMIF_ ADDR[10] | NC | ETM DATA[09] / EMIF_ ADDR[4] | VCCP | | VSS | VSS | VCC | VSS | VSS | | VCCIO | ETM DATA[31] / EMIF_ DATA[15] | NC | NC | MIBSPI3 SOMI | MIBSPI3 SIMO | 8 |
| 7 | LINRX | LINTX | EMIF_ ADDR[9] | NC | ETM DATA[10] / EMIF_ ADDR[3] | VCCIO | | | | | | | | VCCIO | ETM DATA[30] / EMIF_ DATA[14] | NC | NC | N2HET1 [09] | nPORRST | 7 |
| 6 | GIOA[4] | MIBSPI5 NCS[1] | EMIF_ ADDR[8] | NC | ETM DATA[11] / EMIF_ ADDR[2] | VCCIO | VCCIO | VCCIO | VCCIO | VCC | VCC | VCCIO | VCCIO | VCCIO | ETM DATA[29] / EMIF_ DATA[13] | NC | NC | N2HET1 [05] | MIBSPI5 NCS[2] | 6 |
| 5 | GIOA[0] | GIOA[5] | EMIF_ ADDR[7] | EMIF_ ADDR[1] | ETM DATA[20] / EMIF_ DATA[4] | ETM DATA[21] / EMIF_ DATA[5] | ETM DATA[22] / EMIF_ DATA[6] | FLTP2 | FLTP1 | ETM DATA[23] / EMIF_ DATA[7] | ETM DATA[24] / EMIF_ DATA[8] | ETM DATA[25] / EMIF_ DATA[9] | ETM DATA[26] / EMIF_ DATA[10] | ETM DATA[27] / EMIF_ DATA[11] | ETM DATA[28] / EMIF_ DATA[12] | NC | NC | MIBSPI3 NCS[1] | N2HET1 [02] | 5 |
| 4 | N2HET1 [16] | N2HET1 [12] | EMIF_ ADDR[6] | EMIF_ ADDR[0] | NC | NC | NC | N2HET1 [21] | N2HET1 [23] | NC | NC | NC | NC | NC | EMIF_ nCAS | NC | NC | NC | NC | 4 |
| 3 | N2HET1 [29] | N2HET1 [22] | MIBSPI3 NCS[3] | SPI2 NENA | N2HET1 [11] | MIBSPI1 NCS[1] | MIBSPI1 NCS[2] | GIOA[6] | MIBSPI1 NCS[3] | EMIF_ CLK | EMIF_ CKE | N2HET1 [25] | SPI2 NCS[0] | EMIF_ nWAIT | EMIF_ nRAS | NC | NC | NC | N2HET1 [06] | 3 |
| 2 | VSS | MIBSPI3 NCS[2] | GIOA[1] | SPI2 SOMI | SPI2 CLK | GIOB[2] | GIOB[5] | CAN2TX | GIOB[6] | GIOB[1] | KELVIN_ GND | GIOB[0] | N2HET1 [13] | N2HET1 [20] | MIBSPI1 NCS[0] | NC | TEST | N2HET1 [01] | VSS | 2 |
| 1 | VSS | VSS | GIOA[2] | SPI2 SIMO | GIOA[3] | GIOB[7] | GIOB[4] | CAN2RX | N2HET1 [18] | OSCIN | OSCOUT | GIOA[7] | N2HET1 [15] | N2HET1 [24] | NC | N2HET1 [07] | N2HET1 [03] | VSS | VSS | 1 |
| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | R | T | U | V | W | |

A. Balls can have multiplexed functions. Only the default function, except for the EMIF signals that are multiplexed with ETM signals, is depicted in the figure.

**Figure 4-2. ZWT Package Pinout. Top View(A)**

## 4.3 Terminal Functions

Section 4.3.1 and Section 4.3.2 identify the external signal names, the associated pin or ball numbers along with the mechanical package designator, the pin or ball type (Input, Output, I/O, Power, or Ground), whether the pin or ball has any internal pullup or pulldown, whether the pin or ball can be configured as a GPIO, and a functional pin or ball description. The first signal name listed is the primary function for that terminal. The signal name in **bold** is the function being described. For information on how to select between different multiplexed functions, see the *TMS570LS31x/21x 16/32-Bit RISC Flash Microcontroller* Technical Reference Manual (SPNU499) .

**NOTE**

In the Terminal Functions table below, the "Reset Pull State" is the state of the pull applied to the terminal while nPORRST is low and immediately after nPORRST goes High. The default pull direction may change when software configures the pin for an alternate function. The "Pull Type" is the type of pull asserted when the signal name in bold is enabled for the given terminal by the IOMM control registers.

All I/O signals except nRST are configured as inputs while nPORRST is low and immediately after nPORRST goes High. While nPORRST is low, the input buffers are disabled, and the output buffers are disabled with the default pulls enabled.

All output-only signals have the output buffer disabled and the default pull enabled while nPORRST is low, and are configured as outputs with the pulls disabled immediately after nPORRST goes High.

### *4.3.1 PGE Package*

#### 4.3.1.1 Multibuffered Analog-to-Digital Converters (MibADCs)

**Table 4-1. PGE Multibuffered Analog-to-Digital Converters (MibADC1, MibADC2)**

| TERMINAL | | SIGNAL TYPE | RESET PULL STATE | PULL TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| SIGNAL NAME | 144 PGE | | | | |
| **ADREFHI**(1) | 66 | Input | N/A | None | ADC high reference supply |
| **ADREFLO**(1) | 67 | Input | | | ADC low reference supply |
| **VCCAD**(1) | 69 | Power | | | Operating supply for ADC |
| **VSSAD**(1) | 68 | Ground | | | |
| **AD1EVT**/MII_RX_ER/RMII_RX_ER | 86 | I/O | Pulldown | Programmable, 20 µA | ADC1 event trigger input, or GPIO |
| MIBSPI3NCS[0]/**AD2EVT**/GIOB[2]/N2HET2_PIN_nDIS | 55 | I/O | Pullup | Programmable, 20 µA | ADC2 event trigger input, or GPIO |
| **AD1IN[0]** | 60 | Input | N/A | None | ADC1 analog input |
| **AD1IN[1]** | 71 | | | | |
| **AD1IN[2]** | 73 | | | | |
| **AD1IN[3]** | 74 | | | | |
| **AD1IN[4]** | 76 | | | | |
| **AD1IN[5]** | 78 | | | | |
| **AD1IN[6]** | 80 | | | | |
| **AD1IN[7]** | 61 | | | | |

(1) The ADREFHI, ADREFLO, VCCAD and VSSAD connections are common for both ADC cores.


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### Table 4-1. PGE Multibuffered Analog-to-Digital Converters (MibADC1, MibADC2) (continued)

| TERMINAL | | SIGNAL TYPE | RESET PULL STATE | PULL TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| SIGNAL NAME | 144 PGE | | | | |
| AD1IN[8] / AD2IN[8] | 83 | Input | N/A | None | ADC1/ADC2 shared analog inputs |
| AD1IN[9] / AD2IN[9] | 70 | | | | |
| AD1IN[10] / AD2IN[10] | 72 | | | | |
| AD1IN[11] / AD2IN[11] | 75 | | | | |
| AD1IN[12] / AD2IN[12] | 77 | | | | |
| AD1IN[13] / AD2IN[13] | 79 | | | | |
| AD1IN[14] / AD2IN[14] | 82 | | | | |
| AD1IN[15] / AD2IN[15] | 85 | | | | |
| AD1IN[16] / AD2IN[0] | 58 | | | | |
| AD1IN[17] / AD2IN[1] | 59 | | | | |
| AD1IN[18] / AD2IN[2] | 62 | | | | |
| AD1IN[19] / AD2IN[3] | 63 | | | | |
| AD1IN[20] / AD2IN[4] | 64 | | | | |
| AD1IN[21] / AD2IN[5] | 65 | | | | |
| AD1IN[22] / AD2IN[6] | 81 | | | | |
| AD1IN[23] / AD2IN[7] | 84 | | | | |

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### 4.3.1.2 Enhanced High-End Timer (N2HET) Modules

**Table 4-2. PGE Enhanced High-End Timer Modules (N2HET1, N2HET2)**

| TERMINAL | | SIGNAL TYPE | RESET PULL STATE | PULL TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| SIGNAL NAME | 144 PGE | | | | |
| **N2HET1[0]**/SPI4CLK | 25 | I/O | Pulldown | Programmable, 20 µA | N2HET1 timer input capture or output compare, or GIO.<br>Each terminal has a suppression filter with a programmable duration. |
| **N2HET1[1]**/SPI4NENA/N2HET2[8] | 23 | | | | |
| **N2HET1[2]**/SPI4SIMO[0] | 30 | | | | |
| **N2HET1[3]**/SPI4NCS[0]/N2HET2[10] | 24 | | | | |
| **N2HET1[4]** | 36 | | | | |
| **N2HET1[5]**/SPI4SOMI[0]/N2HET2[12] | 31 | | | | |
| **N2HET1[6]**/SCIRX | 38 | | | | |
| **N2HET1[7]**/N2HET2[14] | 33 | | | | |
| **N2HET1[8]**/MIBSPI1SIMO[1]/MII_TXD[3] | 106 | | | | |
| **N2HET1[9]**/N2HET2[16] | 35 | | | | |
| **N2HET1[10]**/MII_TX_CLK/MII_TX_AVCLK4 | 118 | | | | |
| **N2HET1[11]**/MIBSPI3NCS[4]/N2HET2[18] | 6 | | | | |
| **N2HET1[12]**/MII_CRS/RMII_CRS_DV | 124 | | | | |
| **N2HET1[13]**/SCITX | 39 | | | | |
| **N2HET1[14]** | 125 | | | | |
| **N2HET1[15]**/MIBSPI1NCS[4] | 41 | | | | |
| **N2HET1[16]** | 139 | | | | |
| MIBSPI1NCS[1]/**N2HET1[17]**/MII_COL | 130 | I/O | Pullup | Programmable, 20 µA | |
| **N2HET1[18]** | 140 | I/O | Pulldown | Programmable, 20 µA | |
| MIBSPI1NCS[2]/**N2HET1[19]**/MDIO | 40 | I/O | Pullup | Programmable, 20 µA | |
| **N2HET1[20]** | 141 | I/O | Pulldown | Programmable, 20 µA | |
| **N2HET1[22]** | 15 | I/O | Pulldown | Programmable, 20 µA | |
| MIBSPI1NENA/**N2HET1[23]**/MII_RXD[2] | 96 | I/O | Pullup | Programmable, 20 µA | |
| **N2HET1[24]**/MIBSPI1NCS[5]/MII_RXD[0]/RMII_RXD[0] | 91 | I/O | Pulldown | Programmable, 20 µA | |
| MIBSPI3NCS[1]/**N2HET1[25]**/MDCLK | 37 | I/O | Pullup | Programmable, 20 µA | |
| **N2HET1[26]**/MII_RXD[1]/RMII_RXD[1] | 92 | I/O | Pulldown | Programmable, 20 µA | |
| MIBSPI3NCS[2]/I2C_SDA/**N2HET1[27]** | 4 | I/O | Pullup | Programmable, 20 µA | |
| **N2HET1[28]**/MII_RX_CLK/RMII_REFCLK/MII_RX_AVCLK4 | 107 | I/O | Pulldown | Programmable, 20 µA | |
| MIBSPI3NCS[3]/I2C_SCL/**N2HET1[29]** | 3 | I/O | Pullup | Programmable, 20 µA | |
| **N2HET1[30]**/MII_RX_DV | 127 | I/O | Pulldown | Programmable, 20 µA | |
| MIBSPI3NENA/MIBSPI3NCS[5]/**N2HET1[31]** | 54 | I/O | Pullup | Programmable, 20 µA | |
| GIOA[5]/EXTCLKIN/**N2HET1_PIN_nDIS** | 14 | I/O | Pulldown | Programmable, 20 µA | Disable selected PWM outputs |


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**Table 4-2. PGE Enhanced High-End Timer Modules (N2HET1, N2HET2) (continued)**

| TERMINAL | | SIGNAL TYPE | RESET PULL STATE | PULL TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| SIGNAL NAME | 144 PGE | | | | |
| GIOA[2]/**N2HET2[0]** | 9 | I/O | Pulldown | Programmable, 20 µA | N2HET2 time input capture or output compare, or GPIO<br>Each terminal has a suppression filter with a programmable duration. |
| GIOA[6]/**N2HET2[4]** | 16 | | | | |
| GIOA[7]/**N2HET2[6]** | 22 | | | | |
| N2HET1[1]/SPI4NENA/**N2HET2[8]** | 23 | | | | |
| N2HET1[3]/SPI4NCS[0]/**N2HET2[10]** | 24 | | | | |
| N2HET1[5]/SPI4SOMI[0]/**N2HET2[12]** | 31 | | | | |
| N2HET1[7]/**N2HET2[14]** | 33 | | | | |
| N2HET1[9]/**N2HET2[16]** | 35 | | | | |
| N2HET1[11]/MIBSPI3NCS[4]/**N2HET2[18]** | 6 | | | | |
| MIBSPI3NCS[0]/AD2EVT/GIOB[2]/**N2HET2_PIN_nDIS** | 55 | I/O | Pullup | Programmable, 20 µA | Disable selected PWM outputs |

### 4.3.1.3 General-Purpose Input/Output (GPIO)

**Table 4-3. PGE General-Purpose Input/Output (GPIO)**

| TERMINAL | | SIGNAL TYPE | RESET PULL STATE | PULL TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| SIGNAL NAME | 144 PGE | | | | |
| **GIOA[2]**/N2HET2[0] | 9 | I/O | Pulldown | Programmable, 20 µA | General-purpose I/O.<br>All GPIO terminals are capable of generating interrupts to the CPU on rising / falling / both edges. |
| **GIOA[5]**/EXTCLKIN/N2HET1_PIN_nDIS | 14 | | | | |
| **GIOA[6]**/N2HET2[4] | 16 | | | | |
| **GIOA[7]**/N2HET2[6] | 22 | | | | |
| MIBSPI3NCS[0]/AD2EVT/**GIOB[2]**/N2HET2_PIN_nDIS | 55 | I/O | Pullup | Programmable, 20 µA | The application cannot output a level onto this terminal when it is configured as GIOB[2]. A pull-up is enabled on this input. This pull cannot be disabled, and is not programmable using the GIO module pull control registers. |

### 4.3.1.4 FlexRay Interface Controller (FlexRay)

**Table 4-4. FlexRay Interface Controller (FlexRay)**

| TERMINAL | | SIGNAL TYPE | RESET PULL STATE | PULL TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| SIGNAL NAME | 144 PGE | | | | |
| **FRAYRX1** | 126 | Input | Pullup | Fixed 100 µA Pullup | FlexRay data receive (channel 1) |
| **FRAYTX1** | 133 | Output | N/A | None | FlexRay data transmit (channel 1) |
| **FRAYTXEN1** | 142 | Output | | | FlexRay transmit enable (channel 1) |
| **FRAYRX2** | 2 | Input | Pullup | Fixed 100 µA Pullup | FlexRay data receive (channel 2) |
| **FRAYTX2** | 1 | Output | N/A | None | FlexRay data transmit (channel 2) |
| **FRAYTXEN2** | 5 | Output | | | FlexRay transmit enable (channel 2) |

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#### 4.3.1.5 Controller Area Network Controllers (DCANs)

**Table 4-5. PGE Controller Area Network Controllers (DCAN)**

| TERMINAL | | SIGNAL TYPE | RESET PULL STATE | PULL TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| SIGNAL NAME | 144 PGE | | | | |
| **CAN1RX** | 90 | I/O | Pullup | Programmable, 20 µA | CAN1 receive, or GPIO |
| **CAN1TX** | 89 | | | | CAN1 transmit, or GPIO |
| **CAN2RX** | 129 | | | | CAN2 receive, or GPIO |
| **CAN2TX** | 128 | | | | CAN2 transmit, or GPIO |
| **CAN3RX** | 12 | | | | CAN3 receive, or GPIO |
| **CAN3TX** | 13 | | | | CAN3 transmit, or GPIO |

#### 4.3.1.6 Local Interconnect Network Interface Module (LIN)

**Table 4-6. PGE Local Interconnect Network Interface Module (LIN)**

| TERMINAL | | SIGNAL TYPE | RESET PULL STATE | PULL TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| SIGNAL NAME | 144 PGE | | | | |
| **LINRX** | 131 | I/O | Pullup | Programmable, 20 µA | LIN receive, or GPIO |
| **LINTX** | 132 | | | | LIN transmit, or GPIO |

#### 4.3.1.7 Standard Serial Communication Interface (SCI)

**Table 4-7. PGE Standard Serial Communication Interface (SCI)**

| TERMINAL | | SIGNAL TYPE | RESET PULL STATE | PULL TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| SIGNAL NAME | 144 PGE | | | | |
| N2HET1[6]/**SCIRX** | 38 | I/O | Pulldown | Programmable, 20 µA | SCI receive, or GPIO |
| N2HET1[13]/**SCITX** | 39 | | | | SCI transmit, or GPIO |

#### 4.3.1.8 Inter-Integrated Circuit Interface Module (I2C)

**Table 4-8. PGE Inter-Integrated Circuit Interface Module (I2C)**

| TERMINAL | | SIGNAL TYPE | RESET PULL STATE | PULL TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| SIGNAL NAME | 144 PGE | | | | |
| MIBSPI3NCS[2]/**I2C_SDA**/N2HET1[27] | 4 | I/O | Pullup | Programmable, 20 µA | I2C serial data, or GPIO |
| MIBSPI3NCS[3]/**I2C_SCL**/N2HET1[29] | 3 | | | | I2C serial clock, or GPIO |

#### 4.3.1.9 Standard Serial Peripheral Interface (SPI)

**Table 4-9. PGE Standard Serial Peripheral Interface (SPI)**

| TERMINAL | | SIGNAL TYPE | RESET PULL STATE | PULL TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| SIGNAL NAME | 144 PGE | | | | |
| N2HET1[0]/**SPI4CLK** | 25 | I/O | Pulldown | Programmable, 20 µA | SPI4 clock, or GPIO |
| N2HET1[3]/**SPI4NCS[0]**/N2HET2[10] | 24 | | | | SPI4 chip select, or GPIO |
| N2HET1[1]/**SPI4NENA**/N2HET2[8] | 23 | | | | SPI4 enable, or GPIO |
| N2HET1[2]/**SPI4SIMO[0]** | 30 | | | | SPI4 slave-input master-output, or GPIO |
| N2HET1[5]/**SPI4SOMI[0]**/N2HET2[12] | 31 | | | | SPI4 slave-output master-input, or GPIO |


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### 4.3.1.10 Multibuffered Serial Peripheral Interface Modules (MibSPI)

**Table 4-10. PGE Multibuffered Serial Peripheral Interface Modules (MibSPI)**

| TERMINAL | | SIGNAL TYPE | RESET PULL STATE | PULL TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| SIGNAL NAME | 144 PGE | | | | |
| **MIBSPI1CLK** | 95 | I/O | Pullup | Programmable, 20 µA | MibSPI1 clock, or GPIO |
| **MIBSPI1NCS[0]**/MIBSPI1SOMI[1]/MII_TXD[2] | 105 | | | | MibSPI1 chip select, or GPIO |
| **MIBSPI1NCS[1]**/N2HET1[17]/MII_COL | 130 | | | | |
| **MIBSPI1NCS[2]**/N2HET1[19]/MDIO | 40 | | | | |
| N2HET1[15]/**MIBSPI1NCS[4]** | 41 | | Pulldown | Programmable, 20 µA | MibSPI1 chip select, or GPIO |
| N2HET1[24]/**MIBSPI1NCS[5]**/MII_RXD[0]/RMII_RXD[0] | 91 | | | | |
| **MIBSPI1NENA**/N2HET1[23]/MII_RXD[2] | 96 | | Pullup | Programmable, 20 µA | MibSPI1 enable, or GPIO |
| **MIBSPI1SIMO[0]** | 93 | | | | MibSPI1 slave-in master-out, or GPIO |
| N2HET1[8]/**MIBSPI1SIMO[1]**/MII_TXD[3] | 106 | | Pulldown | Programmable, 20 µA | MibSPI1 slave-in master-out, or GPIO |
| **MIBSPI1SOMI[0]** | 94 | | Pullup | Programmable, 20 µA | MibSPI1 slave-out master-in, or GPIO |
| MIBSPI1NCS[0]/**MIBSPI1SOMI[1]**/MII_TXD[2] | 105 | | | | |
| **MIBSPI3CLK** | 53 | I/O | Pullup | Programmable, 20 µA | MibSPI3 clock, or GPIO |
| **MIBSPI3NCS[0]**/AD2EVT/GIOB[2]/N2HET2_PIN_nDIS | 55 | | | | MibSPI3 chip select, or GPIO |
| **MIBSPI3NCS[1]**/N2HET1[25]/MDCLK | 37 | | | | |
| **MIBSPI3NCS[2]**/I2C_SDA/N2HET1[27] | 4 | | | | |
| **MIBSPI3NCS[3]**/I2C_SCL/N2HET1[29] | 3 | | | | |
| N2HET1[11]/**MIBSPI3NCS[4]**/N2HET2[18] | 6 | | Pulldown | Programmable, 20 µA | MibSPI3 chip select, or GPIO |
| MIBSPI3NENA /**MIBSPI3NCS[5]**/N2HET1[31] | 54 | | Pullup | Programmable, 20 µA | MibSPI3 chip select, or GPIO |
| **MIBSPI3NENA**/MIBSPI3NCS[5]/N2HET1[31] | 54 | | | | MibSPI3 enable, or GPIO |
| **MIBSPI3SIMO[0]** | 52 | | | | MibSPI3 slave-in master-out, or GPIO |
| **MIBSPI3SOMI[0]** | 51 | | | | MibSPI3 slave-out master-in, or GPIO |
| **MIBSPI5CLK**/MII_TXEN/RMII_TXEN | 100 | I/O | Pullup | Programmable, 20 µA | MibSPI5 clock, or GPIO |
| **MIBSPI5NCS[0]** | 32 | | | | MibSPI5 chip select, or GPIO |
| **MIBSPI5NENA**/MII_RXD[3] | 97 | | | | MibSPI5 enable, or GPIO |
| **MIBSPI5SIMO[0]**/MII_TXD[1]/RMII_TXD[1] | 99 | | | | MibSPI5 slave-in master-out, or GPIO |
| **MIBSPI5SOMI[0]**/MII_TXD[0]/RMII_TXD[0] | 98 | | | | MibSPI5 slave-out master-in, or GPIO |

### 4.3.1.11 Ethernet Controller

**Table 4-11. PGE Ethernet Controller: MDIO Interface**

| TERMINAL | | SIGNAL TYPE | RESET PULL STATE | PULL TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| SIGNAL NAME | 144 PGE | | | | |
| MIBSPI3NCS[1]/N2HET1[25]/**MDCLK** | 37 | Output | Pullup | Programmable, 20 µA | Serial clock output |
| MIBSPI1NCS[2]/N2HET1[19]/**MDIO** | 40 | I/O | Pullup | Fixed 20 µA Pullup | Serial data input/output |

### Table 4-12. PGE Ethernet Controller: Reduced Media Independent Interface (RMII)

| TERMINAL | | SIGNAL TYPE | RESET PULL STATE | PULL TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| SIGNAL NAME | 144 PGE | | | | |
| N2HET1[12]/MII_CRS/**RMII_CRS_DV** | 124 | Input | Pulldown | Fixed 20 µA Pulldown | RMII carrier sense and data valid |
| N2HET1[28]/MII_RX_CLK/**RMII_REFCLK**/MII_RX_AVCLK4 | 107 | | | | RMII synchronous reference clock for receive, transmit and control interface |
| AD1EVT/MII_RX_ER/**RMII_RX_ER** | 86 | | | | RMII receive error |
| N2HET1[24]/MIBSPI1NCS[5]/MII_RXD[0]/**RMII_RXD[0]** | 91 | | | | RMII receive data |
| N2HET1[26]/MII_RXD[1]/**RMII_RXD[1]** | 92 | | | | |
| MIBSPI5SOMI[0]/MII_TXD[0]/**RMII_TXD[0]** | 98 | Output | Pullup | None | RMII transmit data |
| MIBSPI5SIMO[0]/MII_TXD[1]/**RMII_TXD[1]** | 99 | | | | |
| MIBSPI5CLK/MII_TXEN/**RMII_TXEN** | 100 | | | | RMII transmit enable |

### Table 4-13. PGE Ethernet Controller: Media Independent Interface (MII)

| TERMINAL | | SIGNAL TYPE | RESET PULL STATE | PULL TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| SIGNAL NAME | 144 PGE | | | | |
| MIBSPI1NCS[1]/N2HET1[17]/**MII_COL** | 130 | Input | Pullup | None | Collision detect |
| N2HET1[12]/**MII_CRS**/RMII_CRS_DV | 124 | | Pulldown | Fixed 20 µA Pulldown | Carrier sense and receive valid |
| N2HET1[28]/MII_RX_CLK/RMII_REFCLK/**MII_RX_AVCLK4** | 107 | I/O | Pulldown | None | MII output receive clock |
| N2HET1[30]/**MII_RX_DV** | 127 | Input | Pulldown | Fixed 20 µA Pulldown | Received data valid |
| AD1EVT/**MII_RX_ER**/RMII_RX_ER | 86 | | | | Receive error |
| N2HET1[28]/**MII_RX_CLK**/RMII_REFCLK/MII_RX_AVCLK4 | 107 | I/O | | | Receive clock |
| N2HET1[24]/MIBSPI1NCS[5]/**MII_RXD[0]**/RMII_RXD[0] | 91 | Input | | | Receive data |
| N2HET1[26]/**MII_RXD[1]**/RMII_RXD[1] | 92 | | | | |
| MIBSPI1NENA/N2HET1[23]/**MII_RXD[2]** | 96 | | Pullup | Fixed 20 µA Pulldown | |
| MIBSPI5NENA/**MII_RXD[3]** | 97 | | | | |
| N2HET1[10]/MII_TX_CLK/**MII_TX_AVCLK4** | 118 | I/O | Pulldown | None | MII output transmit clock |
| N2HET1[10]/**MII_TX_CLK**/MII_TX_AVCLK4 | 118 | | | | Transmit clock |
| MIBSPI5SOMI[0]/**MII_TXD[0]**/RMII_TXD[0] | 98 | Output | Pullup | None | Transmit data |
| MIBSPI5SIMO[0]/**MII_TXD[1]**/RMII_TXD[1] | 99 | | | | |
| MIBSPI1NCS[0]/MIBSPI1SOMI[1]/**MII_TXD[2]** | 105 | | | | |
| N2HET1[8]/MIBSPI1SIMO[1]/**MII_TXD[3]** | 106 | | Pulldown | None | |
| MIBSPI5CLK/**MII_TXEN**/RMII_TXEN | 100 | | Pullup | None | Transmit enable |

#### 4.3.1.12 System Module Interface

### Table 4-14. PGE System Module Interface

| TERMINAL | | SIGNAL TYPE | RESET PULL STATE | PULL TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| SIGNAL NAME | 144 PGE | | | | |
| **nPORRST** | 46 | Input | Pulldown | Fixed 100 µA Pulldown | Power-on reset, cold reset External power supply monitor circuitry must drive nPORRST low when any of the supplies to the microcontroller fall out of the specified range. This terminal has a glitch filter. See Section 6.8. |


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**Table 4-14. PGE System Module Interface (continued)**

| TERMINAL | | SIGNAL TYPE | RESET PULL STATE | PULL TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| SIGNAL NAME | 144 PGE | | | | |
| **nRST** | 116 | I/O | Pullup | Fixed 100 µA Pullup | System reset, warm reset, bidirectional.<br>The internal circuitry indicates any reset condition by driving nRST low.<br>The external circuitry can assert a system reset by driving nRST low. To ensure that an external reset is not arbitrarily generated, TI recommends that an external pullup resistor is connected to this terminal.<br>This terminal has a glitch filter. See Section 6.8. |
| **nERROR** | 117 | I/O | Pulldown | Fixed 20 µA Pulldown | ESM Error Signal<br>Indicates error of high severity. See Section 6.18. |

### 4.3.1.13 Clock Inputs and Outputs

**Table 4-15. PGE Clock Inputs and Outputs**

| TERMINAL | | SIGNAL TYPE | RESET PULL STATE | PULL TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| SIGNAL NAME | 144 PGE | | | | |
| **OSCIN** | 18 | Input | N/A | None | From external crystal/resonator, or external clock input |
| **KELVIN_GND** | 19 | Input | | | Kelvin ground for oscillator |
| **OSCOUT** | 20 | Output | | | To external crystal/resonator |
| **ECLK** | 119 | I/O | Pulldown | Programmable, 20 µA | External prescaled clock output, or GIO. |
| GIOA[5]/**EXTCLKIN**/N2HET1_PIN_nDIS | 14 | Input | Pulldown | 20 µA | External clock input #1 |

### 4.3.1.14 Test and Debug Modules Interface

**Table 4-16. PGE Test and Debug Modules Interface**

| TERMINAL | | SIGNAL TYPE | RESET PULL STATE | PULL TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| SIGNAL NAME | 144 PGE | | | | |
| **TEST** | 34 | I/O | Pulldown | Fixed 100 µA Pulldown | Test enable. This terminal must be connected to ground directly or via a pulldown resistor. |
| **nTRST** | 109 | Input | | | JTAG test hardware reset |
| **RTCK** | 113 | Output | N/A | None | JTAG return test clock |
| **TCK** | 112 | Input | Pulldown | Fixed 100 µA Pulldown | JTAG test clock |
| **TDI** | 110 | I/O | Pullup | Fixed 100 µA Pullup | JTAG test data in |
| **TDO** | 111 | Output | 100 µA Pulldown | None | JTAG test data out |
| **TMS** | 108 | I/O | Pullup | Fixed 100 µA Pullup | JTAG test select |

#### 4.3.1.15 Flash Supply and Test Pads

**Table 4-17. PGE Flash Supply and Test Pads**

| TERMINAL | | SIGNAL TYPE | RESET PULL STATE | PULL TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| SIGNAL NAME | 144 PGE | | | | |
| VCCP | 134 | 3.3-V Power | N/A | None | Flash pump supply |
| FLTP1 | 7 | | N/A | None | Flash test pads. These terminals are reserved for TI use only. For proper operation these terminals must connect only to a test pad or not be connected at all [no connect (NC)]. |
| FLTP2 | 8 | | | | |

#### 4.3.1.16 Supply for Core Logic: 1.2-V Nominal

**Table 4-18. PGE Supply for Core Logic: 1.2-V Nominal**

| TERMINAL | | SIGNAL TYPE | RESET PULL STATE | PULL TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| SIGNAL NAME | 144 PGE | | | | |
| VCC | 17 | 1.2-V Power | N/A | None | 1.2-V Core supply |
| VCC | 29 | | | | |
| VCC | 45 | | | | |
| VCC | 48 | | | | |
| VCC | 49 | | | | |
| VCC | 57 | | | | |
| VCC | 87 | | | | |
| VCC | 101 | | | | |
| VCC | 114 | | | | |
| VCC | 123 | | | | |
| VCC | 137 | | | | |
| VCC | 143 | | | | |

#### 4.3.1.17 Supply for I/O Cells: 3.3-V Nominal

**Table 4-19. PGE Supply for I/O Cells: 3.3-V Nominal**

| TERMINAL | | SIGNAL TYPE | RESET PULL STATE | PULL TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| SIGNAL NAME | 144 PGE | | | | |
| VCCIO | 10 | 3.3-V Power | N/A | None | 3.3-V Operating supply for I/Os |
| VCCIO | 26 | | | | |
| VCCIO | 42 | | | | |
| VCCIO | 104 | | | | |
| VCCIO | 120 | | | | |
| VCCIO | 136 | | | | |


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#### 4.3.1.18 Ground Reference for All Supplies Except VCCAD

**Table 4-20. PGE Ground Reference for All Supplies Except VCCAD**

| TERMINAL | | SIGNAL TYPE | RESET PULL STATE | PULL TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| SIGNAL NAME | 144 PGE | | | | |
| **VSS** | 11 | Ground | N/A | None | Ground reference |
| **VSS** | 21 | | | | |
| **VSS** | 27 | | | | |
| **VSS** | 28 | | | | |
| **VSS** | 43 | | | | |
| **VSS** | 44 | | | | |
| **VSS** | 47 | | | | |
| **VSS** | 50 | | | | |
| **VSS** | 56 | | | | |
| **VSS** | 88 | | | | |
| **VSS** | 102 | | | | |
| **VSS** | 103 | | | | |
| **VSS** | 115 | | | | |
| **VSS** | 121 | | | | |
| **VSS** | 122 | | | | |
| **VSS** | 135 | | | | |
| **VSS** | 138 | | | | |
| **VSS** | 144 | | | | |

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## 4.3.2 ZWT Package

### 4.3.2.1 Multibuffered Analog-to-Digital Converters (MibADCs)

**Table 4-21. ZWT Multibuffered Analog-to-Digital Converters (MibADC1, MibADC2)**

| TERMINAL | | SIGNAL TYPE | RESET PULL STATE | PULL TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| SIGNAL NAME | 337 ZWT | | | | |
| **ADREFHI**(1) | V15 | Input | N/A | None | ADC high reference supply |
| **ADREFLO**(1) | V16 | Input | | | ADC low reference supply |
| **VCCAD**(1) | W15 | Power | | | Operating supply for ADC |
| **VSSAD** | V19 | Ground | N/A | None | ADC supply power |
| **VSSAD** | W16 | | | | |
| **VSSAD** | W18 | | | | |
| **VSSAD** | W19 | | | | |
| **AD1EVT**/MII_RX_ER/RMII_RX_ER | N19 | I/O | Pulldown | Programmable, 20 µA | ADC1 event trigger input, or GPIO |
| MIBSPI3NCS[0]/**AD2EVT**/GIOB[2]/N2HET2_PIN_nDIS | V10 | I/O | Pullup | Programmable, 20 µA | ADC2 event trigger input, or GPIO |
| **AD1IN[0]** | W14 | Input | N/A | None | ADC1 analog input |
| **AD1IN[1]** | V17 | | | | |
| **AD1IN[2]** | V18 | | | | |
| **AD1IN[3]** | T17 | | | | |
| **AD1IN[4]** | U18 | | | | |
| **AD1IN[5]** | R17 | | | | |
| **AD1IN[6]** | T19 | | | | |
| **AD1IN[7]** | V14 | | | | |
| **AD1IN[8] / AD2IN[8]** | P18 | Input | N/A | None | ADC1/ADC2 shared analog inputs |
| **AD1IN[9] / AD2IN[9]** | W17 | | | | |
| **AD1IN[10] / AD2IN[10]** | U17 | | | | |
| **AD1IN[11] / AD2IN[11]** | U19 | | | | |
| **AD1IN[12] / AD2IN[12]** | T16 | | | | |
| **AD1IN[13] / AD2IN[13]** | T18 | | | | |
| **AD1IN[14] / AD2IN[14]** | R18 | | | | |
| **AD1IN[15] / AD2IN[15]** | P19 | | | | |
| **AD1IN[16] / AD2IN[0]** | V13 | | | | |
| **AD1IN[17] / AD2IN[1]** | U13 | | | | |
| **AD1IN[18] / AD2IN[2]** | U14 | | | | |
| **AD1IN[19] / AD2IN[3]** | U16 | | | | |
| **AD1IN[20] / AD2IN[4]** | U15 | | | | |
| **AD1IN[21] / AD2IN[5]** | T15 | | | | |
| **AD1IN[22] / AD2IN[6]** | R19 | | | | |
| **AD1IN[23] / AD2IN[7]** | R16 | | | | |

(1) The ADREFHI, ADREFLO, VCCAD and VSSAD connections are common for both ADC cores.


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#### 4.3.2.2 Enhanced High-End Timer (N2HET) Modules

**Table 4-22. ZWT Enhanced High-End Timer (N2HET) Modules**

| TERMINAL | | SIGNAL TYPE | RESET PULL STATE | PULL TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| SIGNAL NAME | 337 ZWT | | | | |
| **N2HET1[0]**/SPI4CLK | K18 | I/O | Pulldown | Programmable, 20 µA | N2HET1 time input capture or output compare, or GIO.<br>Each terminal has a suppression filter with a programmable duration. |
| **N2HET1[1]**/SPI4NENA/N2HET2[8] | V2 | | | | |
| **N2HET1[2]**/SPI4SIMO[0] | W5 | | | | |
| **N2HET1[3]**/SPI4NCS[0]/N2HET2[10] | U1 | | | | |
| **N2HET1[4]** | B12 | | | | |
| **N2HET1[5]**/SPI4SOMI[0]/N2HET2[12] | V6 | | | | |
| **N2HET1[6]**/SCIRX | W3 | | | | |
| **N2HET1[7]**/N2HET2[14] | T1 | | | | |
| **N2HET1[8]**/MIBSPI1SIMO[1]/MII_TXD[3] | E18 | | | | |
| **N2HET1[9]**/N2HET2[16] | V7 | | | | |
| **N2HET1[10]**/MII_TX_CLK/MII_TX_AVCLK4 | D19 | | | | |
| **N2HET1[11]**/MIBSPI3NCS[4]/N2HET2[18] | E3 | | | | |
| **N2HET1[12]**/MII_CRS/RMII_CRS_DV | B4 | | | | |
| **N2HET1[13]**/SCITX | N2 | | | | |
| **N2HET1[14]** | A11 | | | | |
| **N2HET1[15]**/MIBSPI1NCS[4] | N1 | | | | |
| **N2HET1[16]** | A4 | | | | |
| **N2HET1[17]** | A13 | | | | |
| MIBSPI1NCS[1]/**N2HET1[17]**/MII_COL | F3 | | | | |
| **N2HET1[18]** | J1 | | | | |
| **N2HET1[19]** | B13 | | | | |
| MIBSPI1NCS[2]/**N2HET1[19]**/MDIO | G3 | | | | |
| **N2HET1[20]** | P2 | | | | |
| **N2HET1[21]** | H4 | | | | |
| MIBSPI1NCS[3]/**N2HET1[21]** | J3 | | | | |
| **N2HET1[22]** | B3 | | | | |
| **N2HET1[23]** | J4 | | | | |
| MIBSPI1NENA/**N2HET1[23]**/MII_RXD[2] | G19 | | | | |
| **N2HET1[24]**/MIBSPI1NCS[5]/MII_RXD[0]/RMII_RXD[0] | P1 | | | | |
| **N2HET1[25]** | M3 | | | | |
| MIBSPI3NCS[1]/**N2HET1[25]**/MDCLK | V5 | | | | |
| **N2HET1[26]**/MII_RXD[1]/RMII_RXD[1] | A14 | | | | |
| **N2HET1[27]** | A9 | | | | |
| MIBSPI3NCS[2]/I2C_SDA/**N2HET1[27]** | B2 | | | | |
| **N2HET1[28]**/MII_RX_CLK/RMII_REFCLK/MII_RX_AVCLK4 | K19 | | | | |
| **N2HET1[29]** | A3 | | | | |
| MIBSPI3NCS[3]/I2C_SCL/**N2HET1[29]** | C3 | | | | |
| **N2HET1[30]**/MII_RX_DV | B11 | | | | |
| **N2HET1[31]** | J17 | | | | |
| MIBSPI3NENA/MIBSPI3NCS[5]/**N2HET1[31]** | W9 | | | | |
| GIOA[5]/EXTCLKIN/**N2HET1_PIN_nDIS** | B5 | I/O | Pulldown | Programmable, 20 µA | Disable selected PWM outputs |

### Table 4-22. ZWT Enhanced High-End Timer (N2HET) Modules (continued)

| TERMINAL | | SIGNAL TYPE | RESET PULL STATE | PULL TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| SIGNAL NAME | 337 ZWT | | | | |
| GIOA[2]/**N2HET2[0]** | C1 | I/O | Pulldown | Programmable, 20 µA | N2HET2 time input capture or output compare, or GIO.<br>Each terminal has a suppression filter with a programmable duration. |
| EMIF_ADDR[0]/**N2HET2[1]** | D4 | | | | |
| GIOA[3]/**N2HET2[2]** | E1 | | | | |
| EMIF_ADDR[1]/**N2HET2[3]** | D5 | | | | |
| GIOA[6]/**N2HET2[4]** | H3 | | | | |
| EMIF_BA[1]/**N2HET2[5]** | D16 | | | | |
| GIOA[7]/**N2HET2[6]** | M1 | | | | |
| EMIF_nCS[0]/RTP_DATA[15]/**N2HET2[7]** | N17 | | | | |
| N2HET1[1]/SPI4NENA/**N2HET2[8]** | V2 | | | | |
| EMIF_nCS[3]/RTP_DATA[14]/**N2HET2[9]** | K17 | | | | |
| N2HET1[3]/SPI4NCS[0]/**N2HET2[10]** | U1 | | | | |
| EMIF_ADDR[6]/RTP_DATA[13]/**N2HET2[11]** | C4 | | | | |
| N2HET1[5]/SPI4SOMI[0]/**N2HET2[12]** | V6 | | | | |
| EMIF_ADDR[7]/RTP_DATA[12]/**N2HET2[13]** | C5 | | | | |
| N2HET1[7]/**N2HET2[14]** | T1 | | | | |
| EMIF_ADDR[8]/RTP_DATA[11]/**N2HET2[15]** | C6 | | | | |
| N2HET1[9]/**N2HET2[16]** | V7 | | | | |
| N2HET1[11]/MIBSPI3NCS[4]/**N2HET2[18]** | E3 | | | | |
| MIBSPI3NCS[0]/AD2EVT/GIOB[2]/**N2HET2_PIN_nDIS** | V10 | I/O | Pullup | Programmable, 20 µA | Disable selected PWM outputs |


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#### 4.3.2.3 General-Purpose Input/Output (GPIO)

**Table 4-23. ZWT General-Purpose Input/Output (GPIO)**

| TERMINAL | | SIGNAL TYPE | RESET PULL STATE | PULL TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| SIGNAL NAME | 337 ZWT | | | | |
| **GIOA[0]** | A5 | I/O | Pulldown | Programmable, 20 µA | General-purpose I/O. All GPIO terminals are capable of generating interrupts to the CPU on rising / falling / both edges. |
| **GIOA[1]** | C2 | | | | |
| **GIOA[2]**/N2HET2[0] | C1 | | | | |
| **GIOA[3]**/N2HET2[2] | E1 | | | | |
| **GIOA[4]** | A6 | | | | |
| **GIOA[5]**/EXTCLKIN/N2HET1_PIN_nDIS | B5 | | | | |
| **GIOA[6]**/N2HET2[4] | H3 | | | | |
| **GIOA[7]**/N2HET2[6] | M1 | | | | |
| **GIOB[0]** | M2 | | | | |
| **GIOB[1]** | K2 | | | | |
| **GIOB[2]** | F2 | | | | |
| **GIOB[3]** | W10 | | | | |
| **GIOB[4]** | G1 | | | | |
| **GIOB[5]** | G2 | | | | |
| **GIOB[6]** | J2 | | | | |
| **GIOB[7]** | F1 | | | | |
| MIBSPI3NCS[0]/AD2EVT/**GIOB[2]**/N2HET2_PIN_nDIS | V10 | | Pullup | Fixed 20 µA Pulldown | The application cannot output a level onto this terminal when it is configured as GIOB[2]. A pull-up is enabled on this input. This pull cannot be disabled, and is not programmable using the GIO module pull control registers |

#### 4.3.2.4 FlexRay Interface Controller (FlexRay)

**Table 4-24. FlexRay Interface Controller (FlexRay)**

| TERMINAL | | SIGNAL TYPE | RESET PULL STATE | PULL TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| SIGNAL NAME | 337 ZWT | | | | |
| **FRAYRX1** | A15 | Input | Pullup | Fixed 100 µA Pullup | FlexRay data receive (channel 1) |
| **FRAYTX1** | B15 | Output | None | None | FlexRay data transmit (channel 1) |
| **FRAYTXEN1** | B16 | Output | | | FlexRay transmit enable (channel 1) |
| **FRAYRX2** | A8 | Input | Pullup | Fixed 100 µA Pullup | FlexRay data receive (channel 2) |
| **FRAYTX2** | B8 | Output | None | None | FlexRay data transmit (channel 2) |
| **FRAYTXEN2** | B9 | Output | | | FlexRay transmit enable (channel 2) |

#### 4.3.2.5 Controller Area Network Controllers (DCANs)

**Table 4-25. ZWT Controller Area Network Controllers (DCANs)**

| TERMINAL | | SIGNAL TYPE | RESET PULL STATE | PULL TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| SIGNAL NAME | 337 ZWT | | | | |
| **CAN1RX** | B10 | I/O | Pullup | Programmable, 20 µA | CAN1 receive, or GPIO |
| **CAN1TX** | A10 | | | | CAN1 transmit, or GPIO |
| **CAN2RX** | H1 | | | | CAN2 receive, or GPIO |
| **CAN2TX** | H2 | | | | CAN2 transmit, or GPIO |
| **CAN3RX** | M19 | | | | CAN3 receive, or GPIO |
| **CAN3TX** | M18 | | | | CAN3 transmit, or GPIO |

#### 4.3.2.6 Local Interconnect Network Interface Module (LIN)

**Table 4-26. ZWT Local Interconnect Network Interface Module (LIN)**

| TERMINAL | | SIGNAL TYPE | RESET PULL STATE | PULL TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| SIGNAL NAME | 337 ZWT | | | | |
| **LINRX** | A7 | I/O | Pullup | Programmable, 20 µA | LIN receive, or GPIO |
| **LINTX** | B7 | | | | LIN transmit, or GPIO |

#### 4.3.2.7 Standard Serial Communication Interface (SCI)

**Table 4-27. ZWT Standard Serial Communication Interface (SCI)**

| TERMINAL | | SIGNAL TYPE | RESET PULL STATE | PULL TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| SIGNAL NAME | 337 ZWT | | | | |
| N2HET1[6]/**SCIRX** | W3 | I/O | Pulldown | Programmable, 20 µA | SCI receive, or GPIO |
| N2HET1[13]/**SCITX** | N2 | | | | SCI transmit, or GPIO |


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#### 4.3.2.8 Inter-Integrated Circuit Interface Module (I2C)

**Table 4-28. ZWT Inter-Integrated Circuit Interface Module (I2C)**

| TERMINAL | | SIGNAL TYPE | RESET PULL STATE | PULL TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| SIGNAL NAME | 337 ZWT | | | | |
| MIBSPI3NCS[2]/**I2C_SDA**/N2HET1[27] | B2 | I/O | Pullup | Programmable, 20 µA | I2C serial data, or GPIO |
| MIBSPI3NCS[3]/**I2C_SCL**/N2HET1[29] | C3 | | | | I2C serial clock, or GPIO |

#### 4.3.2.9 Standard Serial Peripheral Interface (SPI)

**Table 4-29. ZWT Standard Serial Peripheral Interface (SPI)**

| TERMINAL | | SIGNAL TYPE | RESET PULL STATE | PULL TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| SIGNAL NAME | 337 ZWT | | | | |
| **SPI2CLK** | E2 | I/O | Pullup | Programmable, 20 µA | SPI2 clock, or GPIO |
| **SPI2NCS[0]** | N3 | | | | SPI2 chip select, or GPIO |
| SPI2NENA/**SPI2NCS[1]** | D3 | | | | SPI2 chip select, or GPIO |
| **SPI2NENA**/SPI2NCS[1] | D3 | | | | SPI2 enable, or GPIO |
| **SPI2SIMO[0]** | D1 | | | | SPI2 slave-input master-output, or GPIO |
| **SPI2SOMI[0]** | D2 | | | | SPI2 slave-output master-input, or GPIO |
| N2HET1[0]/**SPI4CLK** | K18 | I/O | Pulldown | Programmable, 20 µA | SPI4 clock, or GPIO |
| N2HET1[3]/**SPI4NCS[0]**/N2HET2[10] | U1 | | | | SPI4 chip select, or GPIO |
| N2HET1[1]/**SPI4NENA**/N2HET2[8] | V2 | | | | SPI4 enable, or GPIO |
| N2HET1[2]/**SPI4SIMO[0]** | W5 | | | | SPI4 slave-input master-output, or GPIO |
| N2HET1[5]/**SPI4SOMI[0]**/N2HET2[12] | V6 | | | | SPI4 slave-output master-input, or GPIO |

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### 4.3.2.10 Multibuffered Serial Peripheral Interface Modules (MibSPI)

**Table 4-30. ZWT Multibuffered Serial Peripheral Interface Modules (MibSPI)**

| TERMINAL | | SIGNAL TYPE | RESET PULL STATE | PULL TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| SIGNAL NAME | 337 ZWT | | | | |
| **MIBSPI1CLK** | F18 | I/O | Pullup | Programmable, 20 µA | MibSPI1 clock, or GPIO |
| **MIBSPI1NCS[0]**/MIBSPI1SOMI[1]/MII_TXD[2] | R2 | | | | MibSPI1 chip select, or GPIO |
| **MIBSPI1NCS[1]**/N2HET1[17]/MII_COL | F3 | | | | |
| **MIBSPI1NCS[2]**/N2HET1[19]/MDIO | G3 | | | | |
| **MIBSPI1NCS[3]**/N2HET1[21] | J3 | | | | |
| N2HET1[15]/**MIBSPI1NCS[4]** | N1 | | Pulldown | Programmable, 20 µA | MibSPI1 chip select, or GPIO |
| N2HET1[24]/**MIBSPI1NCS[5]**/MII_RXD[0]/RMII_RXD[0] | P1 | | | | |
| **MIBSPI1NENA**/N2HET1[23]/MII_RXD[2] | G19 | | Pullup | Programmable, 20 µA | MibSPI1 enable, or GPIO |
| **MIBSPI1SIMO[0]** | F19 | | | | MibSPI1 slave-in master-out, or GPIO |
| N2HET1[8]/**MIBSPI1SIMO[1]**/MII_TXD[3] | E18 | | Pulldown | Programmable, 20 µA | MibSPI1 slave-in master-out, or GPIO |
| **MIBSPI1SOMI[0]** | G18 | | Pullup | Programmable, 20 µA | MibSPI1 slave-out master-in, or GPIO |
| MIBSPI1NCS[0]/**MIBSPI1SOMI[1]**/MII_TXD[2] | R2 | | | | |
| **MIBSPI3CLK** | V9 | I/O | Pullup | Programmable, 20 µA | MibSPI3 clock, or GPIO |
| **MIBSPI3NCS[0]**/AD2EVT/GIOB[2]/N2HET2_PIN_nDIS | V10 | | | | MibSPI3 chip select, or GPIO |
| **MIBSPI3NCS[1]**/N2HET1[25]/MDCLK | V5 | | | | |
| **MIBSPI3NCS[2]**/I2C_SDA/N2HET1[27] | B2 | | | | |
| **MIBSPI3NCS[3]**/I2C_SCL/N2HET1[29] | C3 | | | | |
| N2HET1[11]/**MIBSPI3NCS[4]**/N2HET2[18] | E3 | | Pulldown | Programmable, 20 µA | MibSPI3 chip select, or GPIO |
| MIBSPI3NENA/**MIBSPI3NCS[5]**/N2HET1[31] | W9 | | Pullup | Programmable, 20 µA | MibSPI3 chip select, or GPIO |
| **MIBSPI3NENA**/MIBSPI3NCS[5]/N2HET1[31] | W9 | | | | MibSPI3 enable, or GPIO |
| **MIBSPI3SIMO[0]** | W8 | | | | MibSPI3 slave-in master-out, or GPIO |
| **MIBSPI3SOMI[0]** | V8 | | | | MibSPI3 slave-out master-in, or GPIO |
| **MIBSPI5CLK**/DMM_DATA[4]/MII_TXEN/RMII_TXEN | H19 | I/O | Pullup | Programmable, 20 µA | MibSPI5 clock, or GPIO |
| **MIBSPI5NCS[0]**/DMM_DATA[5] | E19 | | | | MibSPI5 chip select, or GPIO |
| **MIBSPI5NCS[1]**/DMM_DATA[6] | B6 | | | | |
| **MIBSPI5NCS[2]**/DMM_DATA[2] | W6 | | | | |
| **MIBSPI5NCS[3]**/DMM_DATA[3] | T12 | | | | |
| **MIBSPI5NENA**/DMM_DATA[7]/MII_RXD[3] | H18 | | | | MibSPI5 enable, or GPIO |
| **MIBSPI5SIMO[0]**/DMM_DATA[8]/MII_TXD[1]/RMII_TXD[1] | J19 | | | | MibSPI5 slave-in master-out, or GPIO |
| **MIBSPI5SIMO[1]**/DMM_DATA[9] | E16 | | | | |
| **MIBSPI5SIMO[2]**/DMM_DATA[10] | H17 | | | | |
| **MIBSPI5SIMO[3]**/DMM_DATA[11] | G17 | | | | |
| **MIBSPI5SOMI[0]**/DMM_DATA[12]/MII_TXD[0]/RMII_TXD[0] | J18 | | | | |
| **MIBSPI5SOMI[1]**/DMM_DATA[13] | E17 | | | | |
| **MIBSPI5SOMI[2]**/DMM_DATA[14] | H16 | | | | |
| **MIBSPI5SOMI[3]**/DMM_DATA[15] | G16 | | | | |


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#### 4.3.2.11 Ethernet Controller

**Table 4-31. ZWT Ethernet Controller: MDIO Interface**

| TERMINAL | | SIGNAL TYPE | RESET PULL STATE | PULL TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| SIGNAL NAME | 337 ZWT | | | | |
| MIBSPI3NCS[1]/N2HET1[25]/**MDCLK** | V5 | Output | Pullup | None | Serial clock output |
| MIBSPI1NCS[2]/N2HET1[19]/**MDIO** | G3 | I/O | Pullup | Fixed, 20 µA | Serial data input/output |

**Table 4-32. ZWT Ethernet Controller: Reduced Media Independent Interface (RMII)**

| TERMINAL | | SIGNAL TYPE | RESET PULL STATE | PULL TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| SIGNAL NAME | 337 ZWT | | | | |
| N2HET1[12]/MII_CRS/**RMII_CRS_DV** | B4 | Input | Pulldown | Fixed 12 µA Pulldown | RMII carrier sense and receive data valid |
| N2HET1[28]/MII_RX_CLK/**RMII_REFCLK**/MII_RX_AVCLK4 | K19 | | | | RMII synchronous reference clock for receive, transmit and control interface |
| AD1EVT/MII_RX_ER/**RMII_RX_ER** | N19 | | | | RMII receive error |
| N2HET1[24]/MIBSPI1NCS[5]/MII_RXD[0]/**RMII_RXD[0]** | P1 | | | | RMII receive data |
| N2HET1[26]/MII_RXD[1]/**RMII_RXD[1]** | A14 | | | | |
| MIBSPI5SOMI[0]/DMM_DATA[12]/MII_TXD[0]/**RMII_TXD[0]** | J18 | Output | Pullup | None | RMII transmit data |
| MIBSPI5SIMO[0]/DMM_DATA[8]/MII_TXD[1]/**RMII_TXD[1]** | J19 | | | | |
| MIBSPI5CLK/DMM_DATA[4]/MII_TXEN/**RMII_TXEN** | H19 | | | | RMII transmit enable |

**Table 4-33. ZWT Ethernet Controller: Media Independent Interface (MII)**

| TERMINAL | | SIGNAL TYPE | RESET PULL STATE | PULL TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| SIGNAL NAME | 337 ZWT | | | | |
| MIBSPI1NCS[1]/N2HET1[17]/**MII_COL** | F3 | Input | Pullup | None | Collision detect |
| N2HET1[12]/**MII_CRS**/RMII_CRS_DV | B4 | | Pulldown | Fixed 20 µA Pulldown | Carrier sense and receive data valid |
| N2HET1[28]/MII_RX_CLK/RMII_REFCLK/**MII_RX_AVCLK4** | K19 | I/O | Pulldown | None | MII output receive clock |
| N2HET1[30]/**MII_RX_DV** | B11 | Input | Pulldown | Fixed 20 µA Pulldown | Received data valid |
| AD1EVT/**MII_RX_ER**/RMII_RX_ER | N19 | | | | Receive error |
| N2HET1[28]/**MII_RX_CLK**/RMII_REFCLK/MII_RX_AVCLK4 | K19 | I/O | | | Receive clock |
| N2HET1[24]/MIBSPI1NCS[5]/**MII_RXD[0]**/RMII_RXD[0] | P1 | Input | | | Receive data |
| N2HET1[26]/**MII_RXD[1]**/RMII_RXD[1] | A14 | | | | |
| MIBSPI1NENA/N2HET1[23]/**MII_RXD[2]** | G19 | | Pullup | Fixed 20 µA Pulldown | |
| MIBSPI5NENA/DMM_DATA[7]/**MII_RXD[3]** | H18 | | | | |
| N2HET1[10]/MII_TX_CLK/**MII_TX_AVCLK4** | D19 | I/O | Pulldown | None | MII output transmit clock |
| N2HET1[10]/**MII_TX_CLK**/MII_TX_AVCLK4 | D19 | | | | Transmit clock |
| MIBSPI5SOMI[0]/DMM_DATA[12]/**MII_TXD[0]**/RMII_TXD[0] | J18 | Output | Pullup | None | Transmit data |
| MIBSPI5SIMO[0]/DMM_DATA[8]/**MII_TXD[1]**/RMII_TXD[1] | J19 | | | | |
| MIBSPI1NCS[0]/MIBSPI1SOMI[1]/**MII_TXD[2]** | R2 | | | | |
| N2HET1[8]/MIBSPI1SIMO[1]/**MII_TXD[3]** | E18 | | Pulldown | None | |
| MIBSPI5CLK/DMM_DATA[4]/**MII_TXEN**/RMII_TXEN | H19 | | Pullup | None | Transmit enable |

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### 4.3.2.12 External Memory Interface (EMIF)

**Table 4-34. External Memory Interface (EMIF)**

| TERMINAL | | SIGNAL TYPE | RESET PULL STATE | PULL TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| SIGNAL NAME | 337 ZWT | | | | |
| **EMIF_CKE** | L3 | Output | Pulldown | None | EMIF Clock Enable |
| **EMIF_CLK** | K3 | I/O | | None | EMIF clock. This is an output signal in functional mode. It is gated off by default, so that the signal is tri-stated. PINMUX29[8] must be cleared to enable this output. |
| ETMDATA[13]/**EMIF_nOE** | E12 | | Pulldown | None | EMIF Output Enable |
| **EMIF_nWAIT** | P3 | I/O | Pullup | Fixed 20 µA Pullup | EMIF Extended Wait Signal |
| **EMIF_nWE** | D17 | Output | Pullup | None | EMIF Write Enable. |
| **EMIF_nCAS** | R4 | Output | | | EMIF column address strobe |
| **EMIF_nRAS** | R3 | Output | | | EMIF row address strobe |
| **EMIF_nCS[0]**/RTP_DATA[15]/N2HET2[7] | N17 | Output | Pulldown | | EMIF chip select, SDRAM |
| **EMIF_nCS[2]** | L17 | Output | Pullup | | EMIF chip selects, asynchronous<br>This applies to chip selects 2, 3, and 4 |
| **EMIF_nCS[3]**/RTP_DATA[14]/N2HET2[9] | K17 | Output | Pulldown | | |
| **EMIF_nCS[4]**/RTP_DATA[7] | M17 | Output | Pullup | | |
| ETMDATA[15]/**EMIF_nDQM[0]** | E10 | Output | Pulldown | | EMIF Data Mask or Write Strobe.<br>Data mask for SDRAM devices, write strobe for connected asynchronous devices. |
| ETMDATA[14]/**EMIF_nDQM[1]** | E11 | Output | | | |
| ETMDATA[12]/**EMIF_BA[0]** | E13 | Output | | | EMIF bank address or address line |
| **EMIF_BA[1]**/N2HET2[5] | D16 | Output | | | EMIF bank address or address line |
| **EMIF_ADDR[0]**/N2HET2[1] | D4 | Output | | | EMIF address |
| **EMIF_ADDR[1]**/N2HET2[3] | D5 | Output | | | |
| ETMDATA[11]/**EMIF_ADDR[2]** | E6 | Output | | | |
| ETMDATA[10]/**EMIF_ADDR[3]** | E7 | Output | | | |
| ETMDATA[9]/**EMIF_ADDR[4]** | E8 | Output | | | |
| ETMDATA[8]/**EMIF_ADDR[5]** | E9 | Output | | | |
| **EMIF_ADDR[6]**/RTP_DATA[13]/N2HET2[11] | C4 | Output | | | |
| **EMIF_ADDR[7]**/RTP_DATA[12]/N2HET2[13] | C5 | Output | | | |
| **EMIF_ADDR[8]**/RTP_DATA[11]/N2HET2[15] | C6 | Output | | | |
| **EMIF_ADDR[9]**/RTP_DATA[10] | C7 | Output | | | |
| **EMIF_ADDR[10]**/RTP_DATA[9] | C8 | Output | | | |
| **EMIF_ADDR[11]**/RTP_DATA[8] | C9 | Output | | | |
| **EMIF_ADDR[12]**/RTP_DATA[6] | C10 | Output | | | |
| **EMIF_ADDR[13]**/RTP_DATA[5] | C11 | Output | | | |
| **EMIF_ADDR[14]**/RTP_DATA[4] | C12 | Output | | | |
| **EMIF_ADDR[15]**/RTP_DATA[3] | C13 | Output | | | |
| **EMIF_ADDR[16]**/RTP_DATA[2] | D14 | Output | | | |
| **EMIF_ADDR[17]**/RTP_DATA[1] | C14 | Output | Pulldown | | |
| **EMIF_ADDR[18]**/RTP_DATA[0] | D15 | Output | | | |
| **EMIF_ADDR[19]**/RTP_nENA | C15 | Output | | | |
| **EMIF_ADDR[20]**/RTP_nSYNC | C16 | Output | | | |
| **EMIF_ADDR[21]**/RTP_CLK | C17 | Output | | | |


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### Table 4-34. External Memory Interface (EMIF) (continued)

| TERMINAL | | SIGNAL TYPE | RESET PULL STATE | PULL TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| SIGNAL NAME | 337 ZWT | | | | |
| ETMDATA[16]/**EMIF_DATA[0]** | K15 | I/O | Pulldown | Fixed 20 µA Pullup | EMIF Data |
| ETMDATA[17]/**EMIF_DATA[1]** | L15 | I/O | | | |
| ETMDATA[18]/**EMIF_DATA[2]** | M15 | I/O | | | |
| ETMDATA[19]/**EMIF_DATA[3]** | N15 | I/O | | | |
| ETMDATA[20]/**EMIF_DATA[4]** | E5 | I/O | | | |
| ETMDATA[21]/**EMIF_DATA[5]** | F5 | I/O | | | |
| ETMDATA[22]/**EMIF_DATA[6]** | G5 | I/O | | | |
| ETMDATA[23]/**EMIF_DATA[7]** | K5 | I/O | | | |
| ETMDATA[24]/**EMIF_DATA[8]** | L5 | I/O | | | |
| ETMDATA[25]/**EMIF_DATA[9]** | M5 | I/O | | | |
| ETMDATA[26]/**EMIF_DATA[10]** | N5 | I/O | | | |
| ETMDATA[27]/**EMIF_DATA[11]** | P5 | I/O | | | |
| ETMDATA[28]/**EMIF_DATA[12]** | R5 | I/O | | | |
| ETMDATA[29]/**EMIF_DATA[13]** | R6 | I/O | | | |
| ETMDATA[30]/**EMIF_DATA[14]** | R7 | I/O | | | |
| ETMDATA[31]/**EMIF_DATA[15]** | R8 | I/O | | | |

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### 4.3.2.13 Embedded Trace Macrocell for Cortex-R4F CPU (ETM-R4F)

**Table 4-35. Embedded Trace Macrocell for Cortex-R4F CPU (ETM-R4F)**

| TERMINAL | | SIGNAL TYPE | RESET PULL STATE | PULL TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| SIGNAL NAME | 337 ZWT | | | | |
| **ETMTRACECLKIN**/EXTCLKIN2 | R9 | Input | Pulldown | Fixed 20 µA Pullup | ETM Trace Clock Input |
| **ETMTRACECLKOUT** | R10 | Output | Pulldown | None | ETM Trace Clock Output |
| **ETMTRACECTL** | R11 | | | | ETM trace control |
| **ETMDATA[0]** | R12 | | | | ETM data |
| **ETMDATA[1]** | R13 | | | | |
| **ETMDATA[2]** | J15 | | | | |
| **ETMDATA[3]** | H15 | | | | |
| **ETMDATA[4]** | G15 | | | | |
| **ETMDATA[5]** | F15 | | | | |
| **ETMDATA[6]** | E15 | | | | |
| **ETMDATA[7]** | E14 | | | | |
| **ETMDATA[8]**/EMIF_ADDR[5] | E9 | | | | |
| **ETMDATA[9]**/EMIF_ADDR[4] | E8 | | | | |
| **ETMDATA[10]**/EMIF_ADDR[3] | E7 | | | | |
| **ETMDATA[11]**/EMIF_ADDR[2] | E6 | | | | |
| **ETMDATA[12]**/EMIF_BA[0] | E13 | | | | |
| **ETMDATA[13]**/EMIF_nOE | E12 | | | | |
| **ETMDATA[14]**/EMIF_nDQM[1] | E11 | | | | |
| **ETMDATA[15]**/EMIF_nDQM[0] | E10 | | | | |
| **ETMDATA[16]**/EMIF_DATA[0] | K15 | | | | |
| **ETMDATA[17]**/EMIF_DATA[1] | L15 | | | | |
| **ETMDATA[18]**/EMIF_DATA[2] | M15 | | | | |
| **ETMDATA[19]**/EMIF_DATA[3] | N15 | | | | |
| **ETMDATA[20]**/EMIF_DATA[4] | E5 | | | | |
| **ETMDATA[21]**/EMIF_DATA[5] | F5 | | | | |
| **ETMDATA[22]**/EMIF_DATA[6] | G5 | | | | |
| **ETMDATA[23]**/EMIF_DATA[7] | K5 | | | | |
| **ETMDATA[24]**/EMIF_DATA[8] | L5 | | | | |
| **ETMDATA[25]**/EMIF_DATA[9] | M5 | | | | |
| **ETMDATA[26]**/EMIF_DATA[10] | N5 | | | | |
| **ETMDATA[27]**/EMIF_DATA[11] | P5 | | | | |
| **ETMDATA[28]**/EMIF_DATA[12] | R5 | | | | |
| **ETMDATA[29]**/EMIF_DATA[13] | R6 | | | | |
| **ETMDATA[30]**/EMIF_DATA[14] | R7 | | | | |
| **ETMDATA[31]**/EMIF_DATA[15] | R8 | | | | |


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### 4.3.2.14 RAM Trace Port (RTP)

**Table 4-36. RAM Trace Port (RTP)**

| TERMINAL | | SIGNAL TYPE | RESET PULL STATE | PULL TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| SIGNAL NAME | 337 ZWT | | | | |
| EMIF_ADDR[21]/**RTP_CLK** | C17 | I/O | Pulldown | Programmable, 20 µA | RTP packet clock, or GPIO |
| EMIF_ADDR[19]/**RTP_nENA** | C15 | I/O | | | RTP packet handshake, or GPIO |
| EMIF_ADDR[20]/**RTP_nSYNC** | C16 | I/O | | | RTP synchronization, or GPIO |
| EMIF_ADDR[18]/**RTP_DATA[0]** | D15 | I/O | | | RTP packet data, or GPIO |
| EMIF_ADDR[17]/**RTP_DATA[1]** | C14 | | | | |
| EMIF_ADDR[16]/**RTP_DATA[2]** | D14 | | | | |
| EMIF_ADDR[15]/**RTP_DATA[3]** | C13 | | | | |
| EMIF_ADDR[14]/**RTP_DATA[4]** | C12 | | | | |
| EMIF_ADDR[13]/**RTP_DATA[5]** | C11 | | | | |
| EMIF_ADDR[12]/**RTP_DATA[6]** | C10 | | | | |
| EMIF_nCS[4]/**RTP_DATA[7]** | M17 | | Pullup | Programmable, 20 µA | |
| EMIF_ADDR[11]/**RTP_DATA[8]** | C9 | | Pulldown | Programmable, 20 µA | |
| EMIF_ADDR[10]/**RTP_DATA[9]** | C8 | | | | |
| EMIF_ADDR[9]/**RTP_DATA[10]** | C7 | | | | |
| EMIF_ADDR[8]/**RTP_DATA[11]**/N2HET2[15] | C6 | | | | |
| EMIF_ADDR[7]/**RTP_DATA[12]**/N2HET2[13] | C5 | | | | |
| EMIF_ADDR[6]/**RTP_DATA[13]**/N2HET2[11] | C4 | | | | |
| EMIF_nCS[0]/**RTP_DATA[15]**/N2HET2[7] | N17 | | | | |
| EMIF_nCS[3]/**RTP_DATA[14]**/N2HET2[9] | K17 | | | | |

### 4.3.2.15 Data Modification Module (DMM)

**Table 4-37. Data Modification Module (DMM)**

| TERMINAL | | SIGNAL TYPE | RESET PULL STATE | PULL TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| SIGNAL NAME | 337 ZWT | | | | |
| **DMM_CLK** | F17 | I/O | Pullup | Programmable, 20 µA | DMM clock, or GPIO |
| **DMM_nENA** | F16 | | | | DMM handshake, or GPIO |
| **DMM_SYNC** | J16 | | | | DMM synchronization, or GPIO |
| **DMM_DATA[0]** | L19 | | | | DMM data, or GPIO |
| **DMM_DATA[1]** | L18 | | | | |
| MIBSPI5NCS[2]/**DMM_DATA[2]** | W6 | | | | |
| MIBSPI5NCS[3]/**DMM_DATA[3]** | T12 | | | | |
| MIBSPI5CLK/**DMM_DATA[4]**/MII_TXEN/RMII_TXEN | H19 | | | | |
| MIBSPI5NCS[0]/**DMM_DATA[5]** | E19 | | | | |
| MIBSPI5NCS[1]/**DMM_DATA[6]** | B6 | | | | |
| MIBSPI5NENA/**DMM_DATA[7]**/MII_RXD[3] | H18 | | | | |
| MIBSPI5SIMO[0]/**DMM_DATA[8]**/MII_TXD[1]/RMII_TXD[1] | J19 | | | | |
| MIBSPI5SIMO[1]/**DMM_DATA[9]** | E16 | | | | |
| MIBSPI5SIMO[2]/**DMM_DATA[10]** | H17 | | | | |
| MIBSPI5SIMO[3]/**DMM_DATA[11]** | G17 | | | | |
| MIBSPI5SOMI[0]/**DMM_DATA[12]**/MII_TXD[0]/RMII_TXD[0] | J18 | | | | |
| MIBSPI5SOMI[1]/**DMM_DATA[13]** | E17 | | | | |
| MIBSPI5SOMI[2]/**DMM_DATA[14]** | H16 | | | | |
| MIBSPI5SOMI[3]/**DMM_DATA[15]** | G16 | | | | |


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### 4.3.2.16 System Module Interface

**Table 4-38. ZWT System Module Interface**

| TERMINAL | | SIGNAL TYPE | RESET PULL STATE | PULL TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| SIGNAL NAME | 337 ZWT | | | | |
| **nPORRST** | W7 | Input | Pulldown | Fixed 100 µA Pulldown | Power-on reset, cold reset External power supply monitor circuitry must drive nPORRST low when any of the supplies to the microcontroller fall out of the specified range. This terminal has a glitch filter. See Section 6.8. |
| **nRST** | B17 | I/O | Pullup | Fixed 100 µA Pullup | System reset, warm reset, bidirectional. The internal circuitry indicates any reset condition by driving nRST low. The external circuitry can assert a system reset by driving nRST low. To ensure that an external reset is not arbitrarily generated, TI recommends that an external pullup resistor is connected to this terminal. This terminal has a glitch filter. See Section 6.8. |
| **nERROR** | B14 | I/O | Pulldown | Fixed 20 µA Pulldown | ESM Error Signal Indicates error of high severity. See Section 6.18. |

### 4.3.2.17 Clock Inputs and Outputs

**Table 4-39. ZWT Clock Inputs and Outputs**

| TERMINAL | | SIGNAL TYPE | RESET PULL STATE | PULL TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| SIGNAL NAME | 337 ZWT | | | | |
| **OSCIN** | K1 | Input | N/A | None | From external crystal/resonator, or external clock input |
| **KELVIN_GND** | L2 | Input | | | Kelvin ground for oscillator |
| **OSCOUT** | L1 | Output | | | To external crystal/resonator |
| **ECLK** | A12 | I/O | Pulldown | Programmable, 20 µA | External prescaled clock output, or GIO. |
| GIOA[5]/**EXTCLKIN**/N2HET1_PIN_nDIS | B5 | Input | Pulldown | Fixed 20 µA Pulldown | External clock input #1 |
| ETMTRACECLKIN/**EXTCLKIN2** | R9 | Input | | | External clock input #2 |
| **VCCPLL** | P11 | 1.2-V Power | N/A | None | Dedicated core supply for PLLs |

### 4.3.2.18 Test and Debug Modules Interface

**Table 4-40. ZWT Test and Debug Modules Interface**

| TERMINAL | | SIGNAL TYPE | RESET PULL STATE | PULL TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| SIGNAL NAME | 337 ZWT | | | | |
| **TEST** | U2 | I/O | Pulldown | Fixed 100 µA Pulldown | Test enable. This terminal must be connected to ground directly or via a pulldown resistor. |
| **nTRST** | D18 | Input | | | JTAG test hardware reset |
| **RTCK** | A16 | Output | N/A | None | JTAG return test clock |
| **TCK** | B18 | Input | Pulldown | Fixed 100 µA Pulldown | JTAG test clock |
| **TDI** | A17 | I/O | Pullup | Fixed 100 µA Pullup | JTAG test data in |
| **TDO** | C18 | Output | 100 µA Pulldown | None | JTAG test data out |
| **TMS** | C19 | I/O | Pullup | Fixed 100 µA Pullup | JTAG test select |

### 4.3.2.19 Flash Supply and Test Pads

**Table 4-41. ZWT Flash Supply and Test Pads**

| TERMINAL | | SIGNAL TYPE | RESET PULL STATE | PULL TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| SIGNAL NAME | 337 ZWT | | | | |
| **VCCP** | F8 | 3.3-V Power | N/A | None | Flash pump supply |
| **FLTP1** | J5 | – | N/A | None | Flash test pads. These terminals are reserved for TI use only. For proper operation these terminals must connect only to a test pad or not be connected at all [no connect (NC)]. |
| **FLTP2** | H5 | | | | |


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### 4.3.2.20 No Connects

**Table 4-42. No Connects**

| TERMINAL | | SIGNAL TYPE | RESET PULL STATE | PULL TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| SIGNAL NAME | 337 ZWT | | | | |
| NC | D6 | – | N/A | None | No Connects. These balls are not connected to any internal logic and can be connected to the PCB ground without affecting the functionality of the device. |
| NC | D7 | – | N/A | None | |
| NC | D8 | – | N/A | None | |
| NC | D9 | – | N/A | None | |
| NC | D10 | – | N/A | None | |
| NC | D11 | – | N/A | None | |
| NC | D12 | – | N/A | None | |
| NC | D13 | – | N/A | None | |
| NC | E4 | – | N/A | None | |
| NC | F4 | – | N/A | None | |
| NC | G4 | – | N/A | None | |
| NC | K4 | – | N/A | None | |
| NC | K16 | – | N/A | None | |
| NC | L4 | – | N/A | None | |
| NC | L16 | – | N/A | None | |
| NC | M4 | – | N/A | None | |
| NC | M16 | – | N/A | None | |
| NC | N4 | – | N/A | None | |
| NC | N16 | – | N/A | None | |
| NC | N18 | – | N/A | None | |
| NC | P4 | – | N/A | None | |
| NC | P15 | – | N/A | None | |
| NC | P16 | – | N/A | None | |
| NC | P17 | – | N/A | None | |
| NC | R1 | – | N/A | None | |
| NC | R14 | – | N/A | None | |
| NC | R15 | – | N/A | None | |
| NC | T2 | – | N/A | None | |
| NC | T3 | – | N/A | None | |
| NC | T4 | – | N/A | None | |
| NC | T5 | – | N/A | None | |
| NC | T6 | – | N/A | None | |
| NC | T7 | – | N/A | None | |
| NC | T8 | – | N/A | None | |
| NC | T9 | – | N/A | None | |
| NC | T10 | – | N/A | None | |
| NC | T11 | – | N/A | None | |
| NC | T13 | – | N/A | None | |
| NC | T14 | – | N/A | None | |
| NC | U3 | – | N/A | None | |
| NC | U4 | – | N/A | None | |

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### Table 4-42. No Connects (continued)

| TERMINAL | | SIGNAL TYPE | RESET PULL STATE | PULL TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| SIGNAL NAME | 337 ZWT | | | | |
| NC | U5 | – | N/A | None | No Connects. These balls are not connected to any internal logic and can be connected to the PCB ground without affecting the functionality of the device. |
| NC | U6 | – | N/A | None | |
| NC | U7 | – | N/A | None | |
| NC | U8 | – | N/A | None | |
| NC | U9 | – | N/A | None | |
| NC | U10 | – | N/A | None | |
| NC | U11 | – | N/A | None | |
| NC | U12 | – | N/A | None | |
| NC | V3 | – | N/A | None | |
| NC | V4 | – | N/A | None | |
| NC | V11 | – | N/A | None | |
| NC | V12 | – | N/A | None | |
| NC | W4 | – | N/A | None | |
| NC | W11 | – | N/A | None | |
| NC | W12 | – | N/A | None | |
| NC | W13 | – | N/A | None | |

#### 4.3.2.21 Supply for Core Logic: 1.2-V Nominal

### Table 4-43. ZWT Supply for Core Logic: 1.2-V Nominal

| TERMINAL | | SIGNAL TYPE | RESET PULL STATE | PULL TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| SIGNAL NAME | 337 ZWT | | | | |
| **VCC** | F9 | 1.2-V Power | N/A | None | Core supply |
| **VCC** | F10 | | | | |
| **VCC** | H10 | | | | |
| **VCC** | J14 | | | | |
| **VCC** | K6 | | | | |
| **VCC** | K8 | | | | |
| **VCC** | K12 | | | | |
| **VCC** | K14 | | | | |
| **VCC** | L6 | | | | |
| **VCC** | M10 | | | | |
| **VCC** | P10 | | | | |


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#### 4.3.2.22 Supply for I/O Cells: 3.3-V Nominal

**Table 4-44. ZWT Supply for I/O Cells: 3.3-V Nominal**

| TERMINAL | | SIGNAL TYPE | RESET PULL STATE | PULL TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| SIGNAL NAME | 337 ZWT | | | | |
| VCCIO | F6 | 3.3-V Power | N/A | None | Operating supply for I/Os |
| VCCIO | F7 | | | | |
| VCCIO | F11 | | | | |
| VCCIO | F12 | | | | |
| VCCIO | F13 | | | | |
| VCCIO | F14 | | | | |
| VCCIO | G6 | | | | |
| VCCIO | G14 | | | | |
| VCCIO | H6 | | | | |
| VCCIO | H14 | | | | |
| VCCIO | J6 | | | | |
| VCCIO | L14 | | | | |
| VCCIO | M6 | | | | |
| VCCIO | M14 | | | | |
| VCCIO | N6 | | | | |
| VCCIO | N14 | | | | |
| VCCIO | P6 | | | | |
| VCCIO | P7 | | | | |
| VCCIO | P8 | | | | |
| VCCIO | P9 | | | | |
| VCCIO | P12 | | | | |
| VCCIO | P13 | | | | |
| VCCIO | P14 | | | | |

#### 4.3.2.23 Ground Reference for All Supplies Except VCCAD

**Table 4-45. ZWT Ground Reference for All Supplies Except VCCAD**

| TERMINAL | | SIGNAL TYPE | RESET PULL STATE | PULL TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| SIGNAL NAME | 337 ZWT | | | | |
| VSS | A1 | Ground | N/A | None | Ground reference |
| VSS | A2 | | | | |
| VSS | A18 | | | | |
| VSS | A19 | | | | |
| VSS | B1 | | | | |
| VSS | B19 | | | | |
| VSS | H8 | | | | |
| VSS | H9 | | | | |
| VSS | H11 | | | | |
| VSS | H12 | | | | |
| VSS | J8 | | | | |
| VSS | J9 | | | | |
| VSS | J10 | | | | |
| VSS | J11 | | | | |
| VSS | J12 | | | | |
| VSS | K9 | | | | |
| VSS | K10 | | | | |
| VSS | K11 | | | | |
| VSS | L8 | | | | |
| VSS | L9 | | | | |
| VSS | L10 | | | | |
| VSS | L11 | | | | |
| VSS | L12 | | | | |
| VSS | M8 | | | | |
| VSS | M9 | | | | |
| VSS | M11 | | | | |
| VSS | M12 | | | | |
| VSS | V1 | | | | |
| VSS | W1 | | | | |
| VSS | W2 | | | | |


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# 5 Specifications

## 5.1 Absolute Maximum Ratings (1)

Over Operating Free-Air Temperature Range

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage | $V_{CC}$ (2) | –0.3 | 1.43 | V |
| | $V_{CCIO}$, $V_{CCP}$ (2) | –0.3 | 4.6 | |
| | $V_{CCAD}$ | –0.3 | 6.25 | |
| Input voltage | All input pins | –0.3 | 4.6 | V |
| | ADC input pins | –0.3 | 6.25 | |
| Input clamp current | $I_{IK}$ ($V_I$ < 0 or $V_I$ > $V_{CCIO}$)<br>All pins, except AD1IN[23:0] and AD2IN[15:0] | –20 | 20 | mA |
| | $I_{IK}$ ($V_I$ < 0 or $V_I$ > $V_{CCAD}$)<br>AD1IN[23:0] and AD2IN[15:0] | –10 | 10 | |
| | Total | –40 | 40 | mA |
| Operating free-air temperature, $T_A$: | | –40 | 125 | °C |
| Operating junction temperature, $T_J$: | | –40 | 150 | °C |
| Storage temperature, $T_{stg}$ | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to their associated grounds.

## 5.2 ESD Ratings

| | | | | VALUE | UNIT |
|---|---|---|---|---|---|
| $V_{ESD}$ | Electrostatic discharge (ESD) performance: | Human body model (HBM), per AEC Q100-002 (1) | | ±2 | kV |
| | | Charged device model (CDM), per AEC Q100-011 | All pins | ±500 | V |
| | | | Corner pins on 144-pin PGE (1, 36, 37, 72, 73, 108, 109, 144) | ±750 | |
| | | | Corner balls on 337-ball ZWT (A1, A19, W1, W19) | ±750 | |

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 5.3 Power-On Hours (POH) (1) (2)

| NOMINAL CORE VOLTAGE ($V_{CC}$) | JUNCTION TEMPERATURE (Tj) | LIFETIME POH |
|---|---|---|
| 1.2 | 105ºC | 100K |

(1) This information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.
(2) To avoid significant degradation, the device power-on hours (POH) must be limited to those specified in this table. To convert to equivalent POH for a specific temperature profile, see the *Calculating Equivalent Power-on-Hours for Hercules Safety MCUs* Application Report (SPNA207).

## 5.4 Recommended Operating Conditions[(1)]

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Digital logic supply voltage (Core) | 1.14 | 1.2 | 1.32 | V |
| $V_{CCPLL}$ | PLL Supply Voltage | 1.14 | 1.2 | 1.32 | V |
| $V_{CCIO}$ | Digital logic supply voltage (I/O) | 3 | 3.3 | 3.6 | V |
| $V_{CCAD}$ | MibADC supply voltage | 3 | 3.3/5.0 | 5.25 | V |
| $V_{CCP}$ | Flash pump supply voltage | 3 | 3.3 | 3.6 | V |
| $V_{SS}$ | Digital logic supply ground | | 0 | | V |
| $V_{SSAD}$ | MibADC supply ground | –0.1 | | 0.1 | V |
| $V_{ADREFHI}$ | A-to-D high-voltage reference source | $V_{SSAD}$ | | $V_{CCAD}$ | V |
| $V_{ADREFLO}$ | A-to-D low-voltage reference source | $V_{SSAD}$ | | $V_{CCAD}$ | V |
| $V_{SLEW}$ | Maximum positive slew rate for $V_{CCIO}$, $V_{CCAD}$ and $V_{CCP}$ supplies | | | 1 | V/µs |
| $T_A$ | Operating free-air temperature | -40 | | 125 | °C |
| $T_J$ | Operating junction temperature[(2)] | -40 | | 150 | °C |

(1) All voltages are with respect to $V_{SS}$, except $V_{CCAD}$, which is with respect to $V_{SSAD}$
(2) Reliability data is based upon a temperature profile that is equivalent to 100,000 power-on hours at 105°C junction temperature.


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## 5.5 Switching Characteristics for Clock Domains

Over Recommended Operating Conditions

**Table 5-1. Clock Domain Timing Specifications**

| PARAMETER | DESCRIPTION | CONDITIONS | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{HCLK}$ | HCLK - System clock frequency | PGE | Pipeline mode enabled | | 160 | MHz |
| | | | Pipeline mode disabled | | 50 | |
| | | ZWT | Pipeline mode enabled | | 180 | |
| | | | Pipeline mode disabled | | 50 | |
| $f_{GCLK}$ | GCLK - CPU clock frequency | | | | $f_{HCLK}$ | MHz |
| $f_{VCLK}$ | VCLK - Primary peripheral clock frequency | | | | 100 | MHz |
| $f_{VCLK2}$ | VCLK2 - Secondary peripheral clock frequency | | | | 100 | MHz |
| $f_{VCLK3}$ | VCLK3 - Secondary peripheral clock frequency | | | | 100 | MHz |
| $f_{VCLKA1}$ | VCLKA1 - Primary asynchronous peripheral clock frequency | | | | 100 | MHz |
| $f_{VCLKA2}$ | VCLKA2 - Secondary asynchronous peripheral clock frequency | | | | 100 | MHz |
| $f_{VCLKA4}$ | VCLKA4 - Secondary asynchronous peripheral clock frequency | | | | 50 | MHz |
| $f_{RTICLK}$ | RTICLK - clock frequency | | | | $f_{VCLK}$ | MHz |

## 5.6 Wait States Required

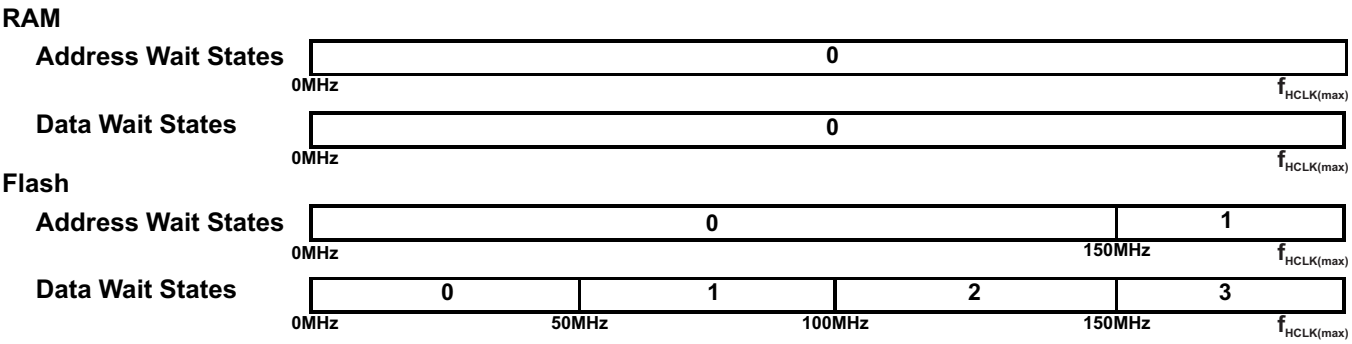


**Figure 5-1. Wait States Scheme**

As shown in Figure 5-1, the TCM RAM can support program and data fetches at full CPU speed without any address or data wait states required.

The TCM flash can support zero address and data wait states up to a CPU speed of 50 MHz in nonpipelined mode. The flash supports a maximum CPU clock speed of 160 MHz in pipelined mode for the PGE Package and 180 MHz for the ZWT package, with one address wait state and three data wait states.

The flash wrapper defaults to nonpipelined mode with zero address wait state and one random-read data wait state.

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## 5.7 Power Consumption

Over Recommended Operating Conditions

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{CC}$, $I_{CCPLL}$ | $V_{CC}$ Digital supply current (operating mode) | $f_{HCLK}$ = 180 MHz (ZWT Package only)<br>$f_{VCLK}$ = 90 MHz, Flash in pipelined mode, $V_{CCmax}$ | | 220 (1) | 440 (2) | mA |
| | $V_{CC}$ Digital supply current (LBIST mode) | LBIST clock rate = 90 MHz (ZWT Package only) | | | 700 (3)(4) | |
| | $V_{CC}$ Digital supply current (PBIST mode) | PBIST ROM clock frequency = 90 MHz (ZWT Package only) | | | 700 (3)(4) | |
| | $V_{CC}$ Digital supply current (operating mode) | $f_{HCLK}$ = 160 MHz<br>$f_{VCLK}$ = 80 MHz, Flash in pipelined mode, $V_{CCmax}$ | | 200 (1) | 420 (2) | |
| | $V_{CC}$ Digital supply current (LBIST mode) | LBIST clock rate = 80 MHz | | | 665 (3)(4) | |
| | $V_{CC}$ Digital supply current (PBIST mode) | PBIST ROM clock frequency = 80 MHz | | | 665 (3)(4) | |
| $I_{CCIO}$ | $V_{CCIO}$ supply current (operating mode) | No DC load, $V_{CCmax}$ | | | 10 | mA |
| $I_{CCAD}$ | $V_{CCAD}$ supply current (operating mode) | Single ADC operational, $V_{CCADmax}$ | | | 15 | mA |
| | | Both ADCs operational, $V_{CCADmax}$ | | | 30 | |
| $I_{ADREFHI}$ | $AD_{REFHI}$ supply current (operating mode) | Single ADC operational, $AD_{REFHImax}$ | | | 3 | mA |
| | | Both ADCs operational, $AD_{REFHImax}$ | | | 6 | |
| $I_{CCP}$ | $V_{CCP}$ pump supply current | Read from 1 bank and program or erase another bank, $V_{CCPmax}$ | | | 60 | mA |

(1) The typical value is the average current for the nominal process corner and junction temperature of 25ºC.
(2) The maximum $I_{CC,}$ value can be derated
- linearly with voltage
- by 1 ma/MHz for lower operating frequency when $f_{HCLK}$= 2 * $f_{VCLK}$
- for lower junction temperature by the equation below where $T_{JK}$ is the junction temperature in Kelvin and the result is in milliamperes. **$235 - 0.15\ e^{0.0174\ T_{JK}}$**

(3) The maximum $I_{CC,}$ value can be derated
- linearly with voltage
- by 1.7 ma/MHz for lower operating frequency when $f_{HCLK}$= 2 * $f_{VCLK}$
- for lower junction temperature by the equation below where $T_{JK}$ is the junction temperature in Kelvin and the result is in milliamperes. **$235 - 0.15\ e^{0.0174\ T_{JK}}$**

(4) LBIST and PBIST currents are for a short duration, typically less than 10 ms. They are usually ignored for thermal calculations for the device and the voltage regulator


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## 5.8 Input/Output Electrical Characteristics[1]

Over Recommended Operating Conditions

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{hys}$ | Input hysteresis | All inputs except FRAYRX1, FRAYRX2 | | 180 | | | mV |
| | | FRAYRX1, FRAYRX2 | | 100 | | | |
| $V_{IL}$ | Low-level input voltage | All inputs[2] (except FRAYRX1, FRAYRX2) | | –0.3 | | 0.8 | V |
| | | FRAYRX1, FRAYRX2 | | | | 0.4 $V_{CCIO}$ | |
| $V_{IH}$ | High-level input voltage | All inputs[2] (except FRAYRX1, FRAYRX2) | | 2 | | $V_{CCIO}$ + 0.3 | V |
| | | FRAYRX1, FRAYRX2 | | 0.6 $V_{CCIO}$ | | | |
| $V_{OL}$ | Low-level output voltage | | $I_{OL}$ = $I_{OLmax}$ | | | 0.2 $V_{CCIO}$ | V |
| | | | $I_{OL}$ = 50 µA, standard output mode | | | 0.2 | |
| | | | $I_{OL}$ = 50 µA, low-EMI output mode (see Section 5.13) | | | 0.2 $V_{CCIO}$ | |
| $V_{OH}$ | High-level output voltage | | $I_{OH}$ = $I_{OHmax}$ | 0.8 $V_{CCIO}$ | | | V |
| | | | $I_{OH}$ = 50 µA, standard output mode | $V_{CCIO}$ – 0.3 | | | |
| | | | $I_{OH}$ = 50 µA, low-EMI output mode (see Section 5.13) | 0.8 $V_{CCIO}$ | | | |
| $I_{IK}$ | Input clamp current (I/O pins) | | $V_I$ < $V_{SSIO}$ - 0.3 or $V_I$ > $V_{CCIO}$ + 0.3 | –3.5 | | 3.5 | mA |
| $I_I$ | Input current (I/O pins) | $I_{IH}$ Pulldown 20 µA | $V_I$ = $V_{CCIO}$ | 5 | | 40 | µA |
| | | $I_{IH}$ Pulldown 100 µA | $V_I$ = $V_{CCIO}$ | 40 | | 195 | |
| | | $I_{IL}$ Pullup 20 µA | $V_I$ = $V_{SS}$ | –40 | | –5 | |
| | | $I_{IL}$ Pullup 100 µA | $V_I$ = $V_{SS}$ | –195 | | –40 | |
| | | All other pins | No pullup or pulldown | –1 | | 1 | |
| $C_I$ | Input capacitance | | | | | 2 | pF |
| $C_O$ | Output capacitance | | | | | 3 | pF |

(1) Source currents (out of the device) are negative while sink currents (into the device) are positive.
(2) This does not apply to the nPORRST pin.

## 5.9 Thermal Resistance Characteristics

Table 5-2 shows the thermal resistance characteristics for the QFP - PGE mechanical package.

Table 5-3 shows the thermal resistance characteristics for the BGA - ZWT mechanical package.

**Table 5-2. Thermal Resistance Characteristics (PGE Package)**

| | | °C / W |
|---|---|---|
| $R\Theta_{JA}$ | Junction-to-free air thermal resistance, Still air using JEDEC 2S2P test board | 39 |
| $R\Theta_{JB}$ | Junction-to-board thermal resistance | 26.3 |
| $R\Theta_{JC}$ | Junction-to-case thermal resistance | 6.7 |
| $\Psi_{JT}$ | Junction-to-package top, Still air | 0.10 |

**Table 5-3. Thermal Resistance Characteristics (ZWT Package)**

| | | °C / W |
|---|---|---|
| $R\Theta_{JA}$ | Junction-to-free air thermal resistance, Still air (includes 5x5 thermal via cluster in 2s2p PCB connected to 1st ground plane) | 18.8 |
| $R\Theta_{JB}$ | Junction-to-board thermal resistance | 14.1 |
| $R\Theta_{JC}$ | Junction-to-case thermal resistance | 7.1 |
| $\Psi_{JT}$ | Junction-to-package top, Still air (includes 5x5 thermal via cluster in 2s2p PCB connected to 1st ground plane) | 0.33 |


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## 5.10 Output Buffer Drive Strengths

### Table 5-4. Output Buffer Drive Strengths

| LOW-LEVEL OUTPUT CURRENT, $I_{OL}$ for $V_I=V_{OLmax}$ or HIGH-LEVEL OUTPUT CURRENT, $I_{OH}$ for $V_I=V_{OHmin}$ | SIGNALS |
|---|---|
| 8 mA | FRAYTX2, FRAYTX1, FRAYTXEN1, FRAYTXEN2,<br>MIBSPI5CLK, MIBSPI5SOMI[0], MIBSPI5SOMI[1], MIBSPI5SOMI[2], MIBSPI5SOMI[3], MIBSPI5SIMO[0], MIBSPI5SIMO[1], MIBSPI5SIMO[2], MIBSPI5SIMO[3],<br>TMS, TDI, TDO, RTCK,<br>SPI4CLK, SPI4SIMO, SPI4SOMI, nERROR,<br>N2HET2[1], N2HET2[3],<br>All EMIF Outputs and I/Os, All ETM Outputs |
| 4 mA | MIBSPI3SOMI, MIBSPI3SIMO, MIBSPI3CLK, MIBSPI1SIMO, MIBSPI1SOMI, MIBSPI1CLK,<br>nRST |
| 2 mA zero-dominant | AD1EVT,<br>CAN1RX, CAN1TX, CAN2RX, CAN2TX, CAN3RX, CAN3TX,<br>DMM_CLK, DMM_DATA[0], DMM_DATA[1], DMM_nENA, DMM_SYNC,<br>GIOA[0-7], GIOB[0-7],<br>LINRX, LINTX,<br>MIBSPI1NCS[0], MIBSPI1NCS[1-3], MIBSPI1NENA, MIBSPI3NCS[0-3], MIBSPI3NENA, MIBSPI5NCS[0-3], MIBSPI5NENA,<br>N2HET1[0-31], N2HET2[0], N2HET2[2], N2HET2[4], N2HET2[5], N2HET2[6], N2HET2[7], N2HET2[8], N2HET2[9], N2HET2[10], N2HET2[11], N2HET2[12], N2HET2[13], N2HET2[14], N2HET2[15], N2HET2[16], N2HET2[18],<br>SPI2NCS[0], SPI2NENA, SPI4NCS[0], SPI4NENA |
| selectable 8 mA/2 mA | ECLK,<br>SPI2CLK, SPI2SIMO, SPI2SOMI<br>The default output buffer drive strength is 8mA for these signals. |

### Table 5-5. Selectable 8 mA/2 mA Control

| SIGNAL | CONTROL BIT | ADDRESS | 8 mA | 2 mA |
|---|---|---|---|---|
| ECLK | SYSPC10[0] | 0xFFFF FF78 | 0 | 1 |
| SPI2CLK | SPI2PC9[9] (1) | 0xFFF7 F668 | 0 | 1 |
| SPI2SIMO | SPI2PC9[10] (1) | 0xFFF7 F668 | 0 | 1 |
| SPI2SOMI | SPI2PC9[11] (1) | 0xFFF7 F668 | 0 | 1 |

(1) Either SPI2PC9[11] or SPI2PC9[24] can change the output strength of the SPI2SOMI pin. In case of a 32-bit write where these two bits differ, SPI2PC9[11] determines the drive strength.

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## 5.11 Input Timings

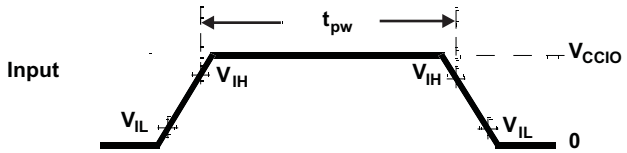


**Figure 5-2. TTL-Level Inputs**

**Table 5-6. Timing Requirements for Inputs (1)**

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{pw}$ | Input minimum pulse width | $t_{c(VCLK)}$ + 10 (2) | | ns |

(1) $t_{c(VCLK)}$ = peripheral VBUS clock cycle time = 1 / $f_{(VCLK)}$
(2) The timing shown in Figure 5-2 is only valid for pins used in GPIO mode.

## 5.12 Output Timings

**Table 5-7. Switching Characteristics for Output Timings versus Load Capacitance ($C_L$)**

| PARAMETER | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| Rise time, $t_r$ | 8 mA low EMI pins (see Table 5-4) | CL = 15 pF | | 2.5 | ns |
| | | CL = 50 pF | | 4 | |
| | | CL = 100 pF | | 7.2 | |
| | | CL = 150 pF | | 12.5 | |
| Fall time, $t_f$ | | CL = 15 pF | | 2.5 | ns |
| | | CL = 50 pF | | 4 | |
| | | CL = 100 pF | | 7.2 | |
| | | CL = 150 pF | | 12.5 | |
| Rise time, $t_r$ | 4 mA low EMI pins (see Table 5-4) | CL = 15 pF | | 5.6 | ns |
| | | CL = 50 pF | | 10.4 | |
| | | CL = 100 pF | | 16.8 | |
| | | CL = 150 pF | | 23.2 | |
| Fall time, $t_f$ | | CL = 15 pF | | 5.6 | ns |
| | | CL= 50 pF | | 10.4 | |
| | | CL = 100 pF | | 16.8 | |
| | | CL = 150 pF | | 23.2 | |
| Rise time, $t_r$ | 2 mA-z low EMI pins (see Table 5-4) | CL = 15 pF | | 8 | ns |
| | | CL = 50 pF | | 15 | |
| | | CL = 100 pF | | 23 | |
| | | CL = 150 pF | | 33 | |
| Fall time, $t_f$ | | CL = 15 pF | | 8 | ns |
| | | CL = 50 pF | | 15 | |
| | | CL = 100 pF | | 23 | |
| | | CL = 150 pF | | 33 | |


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### Table 5-7. Switching Characteristics for Output Timings versus Load Capacitance ($C_L$) (continued)

| PARAMETER | | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| Rise time, $t_r$ | Selectable 8 mA/2 mA-z pins (see Table 5-4) | 8 mA mode | CL = 15 pF | | 2.5 | ns |
| | | | CL = 50 pF | | 4 | |
| | | | CL = 100 pF | | 7.2 | |
| | | | CL = 150 pF | | 12.5 | |
| Fall time, $t_f$ | | | CL = 15 pF | | 2.5 | ns |
| | | | CL = 50 pF | | 4 | |
| | | | CL = 100 pF | | 7.2 | |
| | | | CL = 150 pF | | 12.5 | |
| Rise time, $t_r$ | | 2 mA-z mode | CL = 15 pF | | 8 | ns |
| | | | CL = 50 pF | | 15 | |
| | | | CL = 100 pF | | 23 | |
| | | | CL = 150 pF | | 33 | |
| Fall time, $t_f$ | | | CL = 15 pF | | 8 | ns |
| | | | CL = 50 pF | | 15 | |
| | | | CL = 100 pF | | 23 | |
| | | | CL = 150 pF | | 33 | |

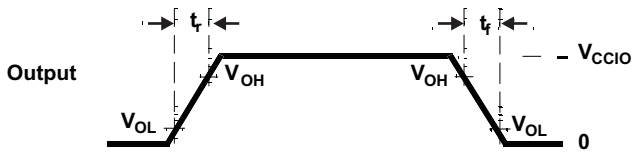


**Figure 5-3. CMOS-Level Outputs**

### Table 5-8. Timing Requirements for Outputs(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{d(parallel_out)}$ | Delay between low to high, or high to low transition of general-purpose output signals that can be configured by an application in parallel, for example, all signals in a GIOA port, or all N2HET1 signals, and so forth. | | 5 | ns |

(1) This specification does not account for any output buffer drive strength differences or any external capacitive loading differences. Check Table 5-4 for output buffer drive strength information on each signal.

## 5.13 Low-EMI Output Buffers

The low-EMI output buffer has been designed explicitly to address the issue of decoupling sources of emissions from the pins which they drive. This is accomplished by adaptively controlling the impedance of the output buffer, and is particularly effective with capacitive loads.

This is not the default mode of operation of the low-EMI output buffers and must be enabled by setting the system module GPCR1 register for the desired module or signal, as shown in Table 5-9. The adaptive impedance control circuit monitors the DC bias point of the output signal. The buffer internally generates two reference levels, VREFLOW and VREFHIGH, which are set to approximately 10% and 90% of VCCIO, respectively.

Once the output buffer has driven the output to a low level, if the output voltage is below VREFLOW, then the impedance of the output buffer will increase to Hi-Z. A high degree of decoupling between the internal ground bus and the output pin will occur with capacitive loads, or any load in which no current is flowing, for example, the buffer is driving low on a resistive path to ground. Current loads on the buffer which attempt to pull the output voltage above VREFLOW will be opposed by the impedance of the output buffer so as to maintain the output voltage at or below VREFLOW.

Conversely, once the output buffer has driven the output to a high level, if the output voltage is above VREFHIGH then the output buffer's impedance will again increase to Hi-Z. A high degree of decoupling between internal power bus ad output pin will occur with capacitive loads or any loads in which no current is flowing, for example, buffer is driving high on a resistive path to VCCIO. Current loads on the buffer which attempt to pull the output voltage below VREFHIGH will be opposed by the buffer's output impedance so as to maintain the output voltage at or above VREFHIGH.

The bandwidth of the control circuitry is relatively low, so that the output buffer in adaptive impedance control mode cannot respond to high-frequency noise coupling into the power buses of the buffer. In this manner, internal bus noise approaching 20% peak-to-peak of VCCIO can be rejected.

Unlike standard output buffers which clamp to the rails, an output buffer in impedance control mode will allow a positive current load to pull the output voltage up to VCCIO + 0.6 V without opposition. Also, a negative current load will pull the output voltage down to VSSIO – 0.6 V without opposition. This is not an issue because the actual clamp current capability is always greater than the IOH / IOL specifications.

The low-EMI output buffers are automatically configured to be in the standard buffer mode when the device enters a low-power mode.


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**Table 5-9. Low-EMI Output Buffer Hookup**

| MODULE OR SIGNAL NAME | CONTROL REGISTER TO ENABLE LOW-EMI MODE |
|---|---|
| Module: MibSPI1 | GPREG1.0 |
| Module: SPI2 | GPREG1.1 |
| Module: MibSPI3 | GPREG1.2 |
| Reserved | GPREG1.3 |
| Module: MibSPI5 | GPREG1.4 |
| Module: FlexRay | GPREG1.5 |
| Module: EMIF | GPREG1.6 |
| Module: ETM | GPREG1.7 |
| Signal: TMS | GPREG1.8 |
| Signal: TDI | GPREG1.9 |
| Signal: TDO | GPREG1.10 |
| Signal: RTCK | GPREG1.11 |
| Signal: TEST | GPREG1.12 |
| Signal: nERROR | GPREG1.13 |
| Reserved | GPREG1.14 |
| Module: RTP | GPREG1.15 |

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# 6 System Information and Electrical Specifications

## 6.1 Device Power Domains

The device core logic is split up into multiple power domains in order to optimize the power for a given application use case. There are 8 core power domains in total: PD1, PD2, PD3, PD4, PD5, RAM_PD1, RAM_PD2 and RAM_PD3.

The actual contents of these power domains are indicated in Section 1.4.

PD1 is an "always-ON" power domain, which cannot be turned off. Each of the other core power domains can be turned ON/OFF one time during device initialization as per the application requirement. Refer to the Power Management Module (PMM) chapter of TMS570LS31X/21X Technical Reference Manual (SPNU499) for more details.

**NOTE**

The clocks to a module must be turned off before powering down the core domain that contains the module.

**NOTE**

The logic in the modules that are powered down lose power completely. Any access to modules that are powered down results in an abort being generated. When power is restored, the modules power-up to their default states (after normal power-up). No register or memory contents are preserved in the core domains that are turned off.


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## 6.2 Voltage Monitor Characteristics

A voltage monitor is implemented on this device. The purpose of this voltage monitor is to eliminate the requirement for a specific sequence when powering up the core and I/O voltage supplies.

### *6.2.1 Important Considerations*

- The voltage monitor does not eliminate the need of a voltage supervisor circuit to guarantee that the device is held in reset when the voltage supplies are out of range.
- The voltage monitor only monitors the core supply (VCC) and the I/O supply (VCCIO). The other supplies are not monitored by the VMON. For example, if the VCCAD or VCCP are supplied from a source different from that for VCCIO, then there is no internal voltage monitor for the VCCAD and VCCP supplies.

### *6.2.2 Voltage Monitor Operation*

The voltage monitor generates the Power Good MCU signal (PGMCU) as well as the I/Os Power Good IO signal (PGIO) on the device. During power-up or power-down, the PGMCU and PGIO are driven low when the core or I/O supplies are lower than the specified minimum monitoring thresholds. The PGIO and PGMCU being low isolates the core logic as well as the I/O controls during the power-up or power-down of the supplies. This allows the core and I/O supplies to be powered up or down in any order.

When the voltage monitor detects a low voltage on the I/O supply, it will assert a power-on reset. When the voltage monitor detects an out-of-range voltage on the core supply, it asynchronously makes all output pins high impedance, and asserts a power-on reset. The voltage monitor is disabled when the device enters a low power mode.

The VMON also incorporates a glitch filter for the nPORRST input. Refer to Section 6.3.3.1 for the timing information on this glitch filter.

**Table 6-1. Voltage Monitoring Specifications**

| PARAMETER | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{MON}$ | Voltage monitoring thresholds | VCC low - VCC level below this threshold is detected as too low. | 0.75 | 0.9 | 1.13 | V |
| | | VCC high - VCC level above this threshold is detected as too high. | 1.40 | 1.7 | 2.1 | |
| | | VCCIO low - VCCIO level below this threshold is detected as too low. | 1.85 | 2.4 | 2.9 | |

### *6.2.3 Supply Filtering*

The VMON has the capability to filter glitches on the VCC and VCCIO supplies.

Table 6-2 shows the characteristics of the supply filtering. Glitches in the supply larger than the maximum specification cannot be filtered.

**Table 6-2. VMON Supply Glitch Filtering Capability**

| PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|
| Width of glitch on VCC that can be filtered | 250 | 1000 | ns |
| Width of glitch on VCCIO that can be filtered | 250 | 1000 | ns |

## 6.3 Power Sequencing and Power On Reset

### *6.3.1 Power-Up Sequence*

There is no timing dependency between the ramp of the VCCIO and the VCC supply voltage. The power-up sequence starts with the I/O voltage rising above the minimum I/O supply threshold, (see Table 6-4 for more details), core voltage rising above the minimum core supply threshold and the release of power-on reset. The high frequency oscillator will start up first and its amplitude will grow to an acceptable level. The oscillator start up time is dependent on the type of oscillator and is provided by the oscillator vendor. The different supplies to the device can be powered up in any order.

The device goes through the following sequential phases during power up.

**Table 6-3. Power-Up Phases**

| | |
|---|---|
| Oscillator startup and validity check | 1032 oscillator cycles |
| eFuse autoload | 1180 oscillator cycles |
| Flash pump power-up | 688 oscillator cycles |
| Flash bank power-up | 617 oscillator cycles |
| **Total** | **3517 oscillator cycles** |

The CPU reset is released at the end of the sequence in Table 6-3 and fetches the first instruction from address 0x00000000.


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### 6.3.2 Power-Down Sequence

The different supplies to the device can be powered down in any order.

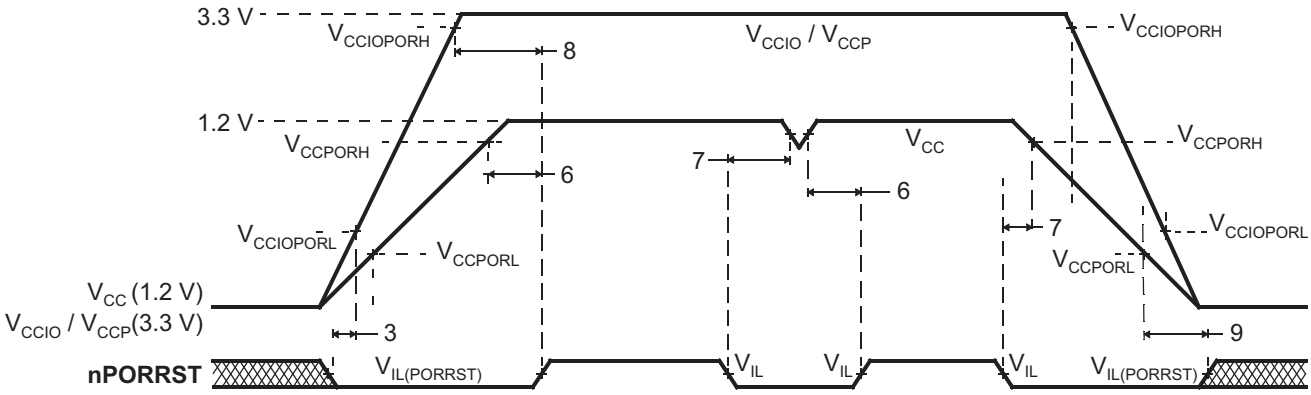
### 6.3.3 Power-On Reset: nPORRST

This is the power-on reset. This reset must be asserted by an external circuitry whenever the I/O or core supplies are outside the specified recommended range. This signal has a glitch filter on it. It also has an internal pulldown.

#### 6.3.3.1 nPORRST Electrical and Timing Requirements

**Table 6-4. Electrical Requirements for nPORRST**

| NO. | PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| | $V_{CCPORL}$ | $V_{CC}$ low supply level when nPORRST must be active during power-up | | 0.5 | V |
| | $V_{CCPORH}$ | $V_{CC}$ high supply level when nPORRST must remain active during power-up and become active during power down | 1.14 | | V |
| | $V_{CCIOPORL}$ | $V_{CCIO}$ / $V_{CCP}$ low supply level when nPORRST must be active during power-up | | 1.1 | V |
| | $V_{CCIOPORH}$ | $V_{CCIO}$ / $V_{CCP}$ high supply level when nPORRST must remain active during power-up and become active during power down | 3.0 | | V |
| | $V_{IL(PORRST)}$ | Low-level input voltage of nPORRST $V_{CCIO}$ > 2.5V | | 0.2 * $V_{CCIO}$ | V |
| | | Low-level input voltage of nPORRST $V_{CCIO}$ < 2.5V | | 0.5 | V |
| 3 | $t_{su(PORRST)}$ | Setup time, nPORRST active before $V_{CCIO}$ and $V_{CCP}$ > $V_{CCIOPORL}$ during power-up | 0 | | ms |
| 6 | $t_{h(PORRST)}$ | Hold time, nPORRST active after $V_{CC}$ > $V_{CCPORH}$ | 1 | | ms |
| 7 | $t_{su(PORRST)}$ | Setup time, nPORRST active before $V_{CC}$ < $V_{CCPORH}$ during power down | 2 | | µs |
| 8 | $t_{h(PORRST)}$ | Hold time, nPORRST active after $V_{CCIO}$ and $V_{CCP}$ > $V_{CCIOPORH}$ | 1 | | ms |
| 9 | $t_{h(PORRST)}$ | Hold time, nPORRST active after $V_{CC}$ < $V_{CCPORL}$ | 0 | | ms |
| | $t_{f(nPORRST)}$ | Filter time nPORRST pin;<br>pulses less than MIN will be filtered out, pulses greater than MAX will generate a reset. | 500 | 2000 | ns |




NOTE: There is no timing dependency between the ramp of the VCCIO and the VCC supply voltage; this is just an exemplary drawing.

**Figure 6-1. nPORRST Timing Diagram**

## 6.4 Warm Reset (nRST)

This is a bidirectional reset signal. The internal circuitry drives the signal low on detecting any device reset condition. An external circuit can assert a device reset by forcing the signal low. On this terminal, the output buffer is implemented as an open drain (drives low only). To ensure an external reset is not arbitrarily generated, TI recommends that an external pullup resistor is connected to this terminal.

This terminal has a glitch filter. It also has an internal pullup

### *6.4.1 Causes of Warm Reset*

**Table 6-5. Causes of Warm Reset**

| DEVICE EVENT | SYSTEM STATUS FLAG |
|---|---|
| Power-Up Reset | Exception Status Register, bit 15 |
| Oscillator fail | Global Status Register, bit 0 |
| PLL slip | Global Status Register, bits 8 and 9 |
| Watchdog exception / Debugger reset | Exception Status Register, bit 13 |
| CPU Reset (driven by the CPU STC) | Exception Status Register, bit 5 |
| Software Reset | Exception Status Register, bit 4 |
| External Reset | Exception Status Register, bit 3 |

### *6.4.2 nRST Timing Requirements*

**Table 6-6. nRST Timing Requirements**

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{v(RST)}$ | Valid time, nRST active after nPORRST inactive | $2256t_{c(OSC)}$ (1) | | ns |
| | Valid time, nRST active (all other System reset conditions) | $32t_{c(VCLK)}$ | | |
| $t_{f(nRST)}$ | Filter time nRST pin; pulses less than MIN will be filtered out; pulses greater than MAX will generate a reset. See Section 6.8. | 475 | 2000 | ns |

(1) Assumes the oscillator has started up and stabilized before nPORRST is released .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## 6.5 ARM-R4F CPU Information

### 6.5.1 Summary of ARM Cortex-R4F CPU Features

The features of the ARM Cortex-R4F CPU include:

- An integer unit with integral EmbeddedICE-RT logic.
- High-speed Advanced Microprocessor Bus Architecture (AMBA) Advanced eXtensible Interfaces (AXI) for Level two (L2) master and slave interfaces.
- Floating Point Coprocessor
- Dynamic branch prediction with a global history buffer, and a 4-entry return stack
- Low interrupt latency.
- Nonmaskable interrupt.
- A Harvard Level one (L1) memory system with:
  - Tightly-Coupled Memory (TCM) interfaces with support for error correction or parity checking memories
  - ARMv7-R architecture Memory Protection Unit (MPU) with 12 regions
- Dual core logic for fault detection in safety-critical applications.
- An L2 memory interface:
  - Single 64-bit master AXI interface
  - 64-bit slave AXI interface to TCM RAM blocks
- A debug interface to a CoreSight Debug Access Port (DAP).
- A trace interface to a CoreSight ETM-R4.
- A Performance Monitoring Unit (PMU).
- A Vectored Interrupt Controller (VIC) port.

For more information on the ARM Cortex-R4F CPU see www.arm.com.

### 6.5.2 ARM Cortex-R4F CPU Features Enabled by Software

The following CPU features are disabled on reset and must be enabled by the application if required.

- ECC On Tightly-Coupled Memory (TCM) Accesses
- Hardware Vectored Interrupt (VIC) Port
- Floating Point Coprocessor
- Memory Protection Unit (MPU)

### 6.5.3 Dual Core Implementation

The device has two Cortex-R4F cores, where the output signals of both CPUs are compared in the CCM-R4 unit. To avoid common mode impacts the signals of the CPUs to be compared are delayed by two clock cycles as shown in Figure 6-3.

The CPUs have a diverse CPU placement given by following requirements:

- different orientation; for example, CPU1 = "north" orientation, CPU2 = "flip west" orientation
- dedicated guard ring for each CPU

**Figure 6-2. Dual-CPU Orientation**

### 6.5.4 Duplicate Clock Tree After GCLK

The CPU clock domain is split into two clock trees, one for each CPU, with the clock of the second CPU running at the same frequency and in phase to the clock of CPU1. See Figure 6-3.

### 6.5.5 ARM Cortex-R4F CPU Compare Module (CCM-R4) for Safety

This device has two ARM Cortex-R4F CPU cores, where the output signals of both CPUs are compared in the CCM-R4 unit. To avoid common mode impacts the signals of the CPUs to be compared are delayed in a different way as shown in Figure 6-3.

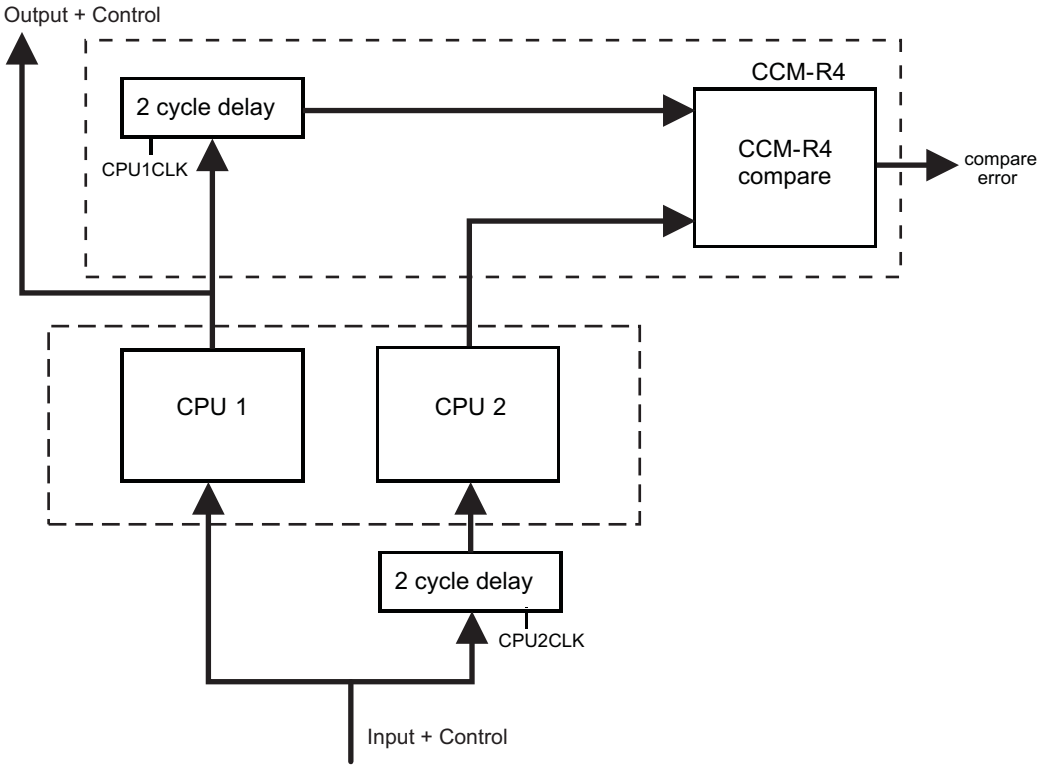


**Figure 6-3. Dual Core Implementation**

To avoid an erroneous CCM-R4 compare error, the application software must initialize the registers of both CPUs before the registers are used, including function calls where the register values are pushed onto the stack.

### 6.5.6 CPU Self-Test

The CPU STC (Self-Test Controller) is used to test the two Cortex-R4F CPU Cores using the Deterministic Logic BIST Controller as the test engine.

The main features of the self-test controller are:

- Ability to divide the complete test run into independent test intervals
- Capable of running the complete test as well as running few intervals at a time
- Ability to continue from the last executed interval (test set) as well as ability to restart from the beginning (First test set)
- Complete isolation of the self-tested CPU core from rest of the system during the self-test run
- Ability to capture the Failure interval number
- Time-out counter for the CPU self-test run as a fail-safe feature


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#### 6.5.6.1 Application Sequence for CPU Self-Test

1. Configure clock domain frequencies.
2. Select number of test intervals to be run.
3. Configure the time-out period for the self-test run.
4. Enable self-test.
5. Wait for CPU reset.
6. In the reset handler, read CPU self-test status to identify any failures.
7. Retrieve CPU state if required.

For more information see the device specific technical reference manual.

#### 6.5.6.2 CPU Self-Test Clock Configuration

The maximum clock rate for the self-test is 90MHz. The STCCLK is divided down from the CPU clock. This divider is configured by the STCCLKDIV register at address 0xFFFFE108.

For more information see the device specific technical reference manual.

#### 6.5.6.3 CPU Self-Test Coverage

Table 6-7 shows CPU test coverage achieved for each self-test interval. It also lists the cumulative test cycles. The test time can be calculated by multiplying the number of test cycles with the STC clock period.

**Table 6-7. CPU Self-Test Coverage**

| INTERVALS | TEST COVERAGE, % | TEST CYCLES |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 62.13 | 1365 |
| 2 | 70.09 | 2730 |
| 3 | 74.49 | 4095 |
| 4 | 77.28 | 5460 |
| 5 | 79.28 | 6825 |
| 6 | 80.90 | 8190 |
| 7 | 82.02 | 9555 |
| 8 | 83.10 | 10920 |
| 9 | 84.08 | 12285 |
| 10 | 84.87 | 13650 |
| 11 | 85.59 | 15015 |
| 12 | 86.11 | 16380 |
| 13 | 86.67 | 17745 |
| 14 | 87.16 | 19110 |
| 15 | 87.61 | 20475 |
| 16 | 87.98 | 21840 |
| 17 | 88.38 | 23205 |
| 18 | 88.69 | 24570 |
| 19 | 88.98 | 25935 |
| 20 | 89.28 | 27300 |
| 21 | 89.50 | 28665 |
| 22 | 89.76 | 30030 |
| 23 | 90.01 | 31395 |
| 24 | 90.21 | 32760 |

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## 6.6 Clocks

### 6.6.1 Clock Sources

Table 6-8 lists the available clock sources on the device. Each of the clock sources can be enabled or disabled using the CSDISx registers in the system module. The clock source number in the table corresponds to the control bit in the CSDISx register for that clock source.

Table 6-8 also shows the default state of each clock source.

**Table 6-8. Available Clock Sources**

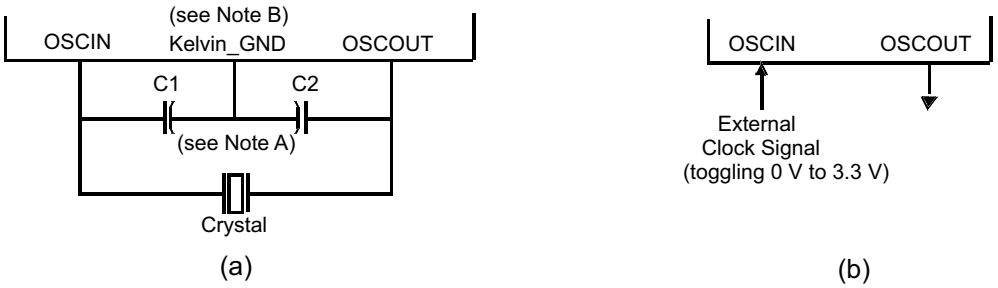
| CLOCK SOURCE # | NAME | DESCRIPTION | DEFAULT STATE |
|---|---|---|---|
| 0 | OSCIN | Main Oscillator | Enabled |
| 1 | PLL1 | Output From PLL1 | Disabled |
| 2 | Reserved | Reserved | Disabled |
| 3 | EXTCLKIN1 | External Clock Input #1 | Disabled |
| 4 | CLK80K | Low Frequency Output of Internal Reference Oscillator | Enabled |
| 5 | CLK10M | High Frequency Output of Internal Reference Oscillator | Enabled |
| 6 | PLL2 | Output From PLL2 | Disabled |
| 7 | EXTCLKIN2 | External Clock Input #2 | Disabled |

#### 6.6.1.1 Main Oscillator

The oscillator is enabled by connecting the appropriate fundamental resonator/crystal and load capacitors across the external OSCIN and OSCOUT pins as shown in Figure 6-4. The oscillator is a single stage inverter held in bias by an integrated bias resistor. This resistor is disabled during leakage test measurement and low power modes.

**TI strongly encourages each customer to submit samples of the device to the resonator/crystal vendors for validation. The vendors are equipped to determine what load capacitors will best tune their resonator/crystal to the microcontroller device for optimum startup and operation over temperature/voltage extremes.**

An external oscillator source can be used by connecting a 3.3-V clock signal to the OSCIN pin and leaving the OSCOUT pin unconnected (open) as shown in Figure 6-4.




Note A: The values of C1 and C2 should be provided by the resonator/crystal vendor.
Note B: Kelvin_GND should not be connected to any other GND.

**Figure 6-4. Recommended Crystal/Clock Connection**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#### 6.6.1.1.1 Timing Requirements for Main Oscillator

**Table 6-9. Timing Requirements for Main Oscillator**

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{c(OSC)}$ | Cycle time, OSCIN (when using a sine-wave input) | 50 | 200 | ns |
| $t_{c(OSC_SQR)}$ | Cycle time, OSCIN, (when input to the OSCIN is a square wave ) | 50 | 200 | ns |
| $t_{w(OSCIL)}$ | Pulse duration, OSCIN low (when input to the OSCIN is a square wave) | 6 | | ns |
| $t_{w(OSCIH)}$ | Pulse duration, OSCIN high (when input to the OSCIN is a square wave) | 6 | | ns |

#### 6.6.1.2 Low Power Oscillator

The Low Power Oscillator (LPO) is comprised of two oscillators — HF LPO and LF LPO, in a single macro.

##### *6.6.1.2.1 Features*

The main features of the LPO are:

- Supplies a clock at extremely low power for power-saving modes. This is connected as clock source # 4 of the Global Clock Module.
- Supplies a high-frequency clock for nontiming-critical systems. This is connected as clock source # 5 of the Global Clock Module.
- Provides a comparison clock for the crystal oscillator failure detection circuit.

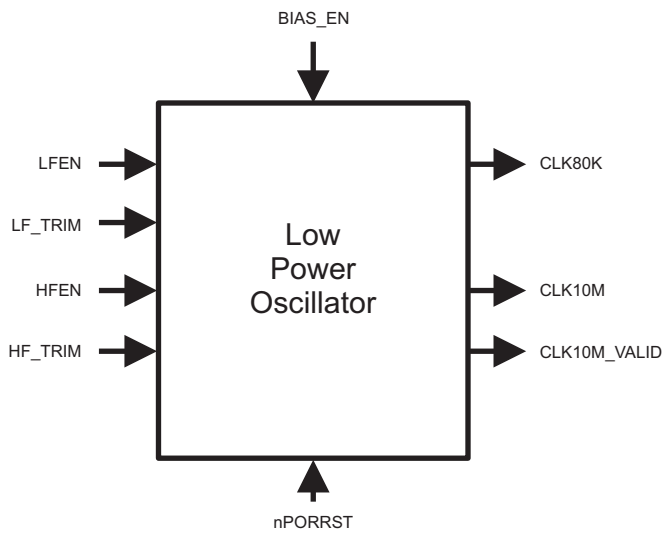


**Figure 6-5. LPO Block Diagram**

Figure 6-5 shows a block diagram of the internal reference oscillator. This is a low power oscillator (LPO) and provides two clock sources: one nominally 80 kHz and one nominally 10 MHz.

##### *6.6.1.2.2 LPO Electrical and Timing Specifications*

**Table 6-10. LPO Specifications**

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Clock Detection | Oscillator fail frequency - lower threshold, using untrimmed LPO output | 1.375 | 2.4 | 4.875 | MHz |
| | Oscillator fail frequency - higher threshold, using untrimmed LPO output | 22 | 38.4 | 78 | MHz |
| LPO - HF oscillator ($f_{HFLPO}$) | Untrimmed frequency | 5.5 | 9 | 19.5 | MHz |
| | Trimmed frequency | 8 | 9.6 | 11 | MHz |
| | Startup time from STANDBY (LPO BIAS_EN High for at least 900µs) | | | 10 | µs |
| | Cold startup time | | | 900 | µs |
| LPO - LF oscillator ($f_{LFLPO}$) | Untrimmed frequency | 36 | 85 | 180 | kHz |
| | Startup time from STANDBY (LPO BIAS_EN High for at least 900µs) | | | 100 | µs |
| | cold startup time | | | 2000 | µs |


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#### 6.6.1.3 Phase Locked Loop (PLL) Clock Modules

The PLL is used to multiply the input frequency to some higher frequency.

The main features of the PLL are:

- Frequency modulation can be optionally superimposed on the synthesized frequency of PLL1. The frequency modulation capability of PLL2 is permanently disabled.
- Configurable frequency multipliers and dividers.
- Built-in PLL Slip monitoring circuit.
- Option to reset the device on a PLL slip detection.

##### *6.6.1.3.1 Block Diagram*

Figure 6-6 shows a high-level block diagram of the two PLL macros on this microcontroller. PLLCTL1 and PLLCTL2 are used to configure the multiplier and dividers for the PLL1. PLLCTL3 is used to configure the multiplier and dividers for PLL2.

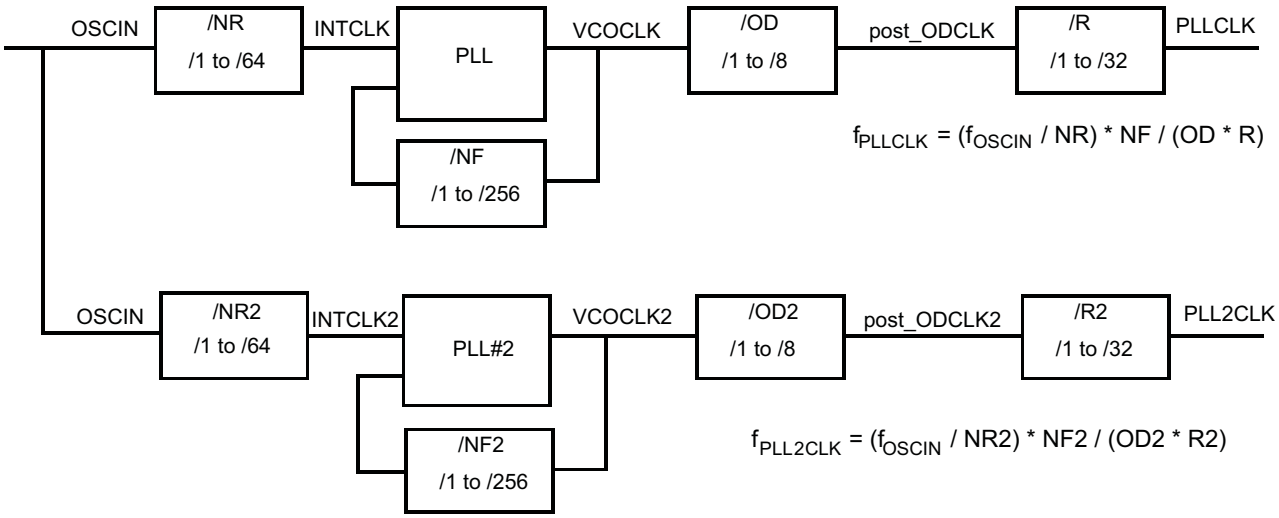


**Figure 6-6. ZWT PLLx Block Diagram**

##### *6.6.1.3.2 PLL Timing Specifications*

**Table 6-11. PLL Timing Specifications**

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $f_{INTCLK}$ | PLL1 Reference Clock frequency | 1 | 20 | MHz |
| $f_{post_ODCLK}$ | Post-ODCLK – PLL1 Post-divider input clock frequency | | 400 | MHz |
| $f_{VCOCLK}$ | VCOCLK – PLL1 Output Divider (OD) input clock frequency | 150 | 550 | MHz |
| $f_{INTCLK2}$ | PLL2 Reference Clock frequency | 1 | 20 | MHz |
| $f_{post_ODCLK2}$ | Post-ODCLK – PLL2 Post-divider input clock frequency | | 400 | MHz |
| $f_{VCOCLK2}$ | VCOCLK – PLL2 Output Divider (OD) input clock frequency | 150 | 550 | MHz |

#### 6.6.1.4 External Clock Inputs

The device supports up to two external clock inputs. This clock input must be a square wave input. The electrical and timing requirements for these clock inputs are specified in Table 6-12. The external clock sources are not checked for validity. They are assumed valid when enabled.

**Table 6-12. External Clock Timing and Electrical Specifications**

| PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|
| $f_{EXTCLKx}$ | External clock input frequency | | 80 | MHz |
| $t_{w(EXTCLKIN)H}$ | EXTCLK high-pulse duration | 6 | | ns |
| $t_{w(EXTCLKIN)L}$ | EXTCLK low-pulse duration | 6 | | ns |
| $v_{iL(EXTCLKIN)}$ | Low-level input voltage | -0.3 | 0.8 | V |
| $v_{iH(EXTCLKIN)}$ | High-level input voltage | 2 | VCCIO + 0.3 | V |

### *6.6.2 Clock Domains*

#### 6.6.2.1 Clock Domain Descriptions

Table 6-13 lists the device clock domains and their default clock sources. The table also shows the system module control register that is used to select an available clock source for each clock domain.

**Table 6-13. Clock Domain Descriptions**

| CLOCK DOMAIN NAME | DEFAULT CLOCK SOURCE | CLOCK SOURCE SELECTION REGISTER | DESCRIPTION |
|---|---|---|---|
| HCLK | OSCIN | GHVSRC | • Is disabled via the CDDISx registers bit 1<br>• Used for all system modules including DMA, ESM |
| GCLK | OSCIN | GHVSRC | • Always the same frequency as HCLK<br>• In phase with HCLK<br>• Is disabled separately from HCLK via the CDDISx registers bit 0<br>• Can be divided by 1up to 8 when running CPU self-test (LBIST) using the CLKDIV field of the STCCLKDIV register at address 0xFFFFE108 |
| GCLK2 | OSCIN | GHVSRC | • Always the same frequency as GCLK<br>• 2 cycles delayed from GCLK<br>• Is disabled along with GCLK<br>• Gets divided by the same divider setting as that for GCLK when running CPU self-test (LBIST) |
| VCLK | OSCIN | GHVSRC | • Divided down from HCLK<br>• Can be HCLK/1, HCLK/2, ... or HCLK/16<br>• Is disabled separately from HCLK via the CDDISx registers bit 2 |
| VCLK2 | OSCIN | GHVSRC | • Divided down from HCLK<br>• Can be HCLK/1, HCLK/2, ... or HCLK/16<br>• Frequency must be an integer multiple of VCLK frequency<br>• Is disabled separately from HCLK via the CDDISx registers bit 3 |
| VCLK3 | OSCIN | GHVSRC | • Divided down from HCLK<br>• Can be HCLK/1, HCLK/2, ... or HCLK/16<br>• Is disabled separately from HCLK via the CDDISx registers bit 8 |
| VCLKA1 | VCLK | VCLKASRC | • Defaults to VCLK as the source<br>• Is disabled via the CDDISx registers bit 4 |
| VCLKA2 | VCLK | VCLKASRC | • Defaults to VCLK as the source<br>• Is disabled via the CDDISx registers bit 5 |


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**Table 6-13. Clock Domain Descriptions (continued)**

| CLOCK DOMAIN NAME | DEFAULT CLOCK SOURCE | CLOCK SOURCE SELECTION REGISTER | DESCRIPTION |
|---|---|---|---|
| VCLKA3 | VCLK | VCLKACON1 | • Defaults to VCLK as the source<br>• Frequency can be as fast as HCLK frequency.<br>• Is disabled via the CDDISx registers bit 10 |
| VCLKA3_DIVR | VCLK | VCLKACON1 | • Divided down from the VCLKA3 using the VCLKA3R field of the VCLKACON1 register at address 0xFFFFE140<br>• Frequency can be VCLKA3/1, VCLKA3/2, ..., or VCLKA3/8<br>• Default frequency is VCLKA3/2<br>• Is disabled separately via the VCLKACON1 register VCLKA3_DIV_CDDIS bit only if the VCLKA3 clock is not disabled |
| VCLKA4 | VCLK | VCLKACON1 | • Defaults to VCLK as the source<br>• Is disabled via the CDDISx registers bit 11 |
| RTICLK | VCLK | RCLKSRC | • Defaults to VCLK as the source<br>• If a clock source other than VCLK is selected for RTICLK, then the RTICLK frequency must be less than or equal to VCLK/3<br>– Application can ensure this by programming the RTI1DIV field of the RCLKSRC register, if necessary<br>• Is disabled via the CDDISx registers bit 6 |

### 6.6.2.2 Mapping of Clock Domains to Device Modules

Each clock domain has a dedicated functionality as shown in Figure 6-7.

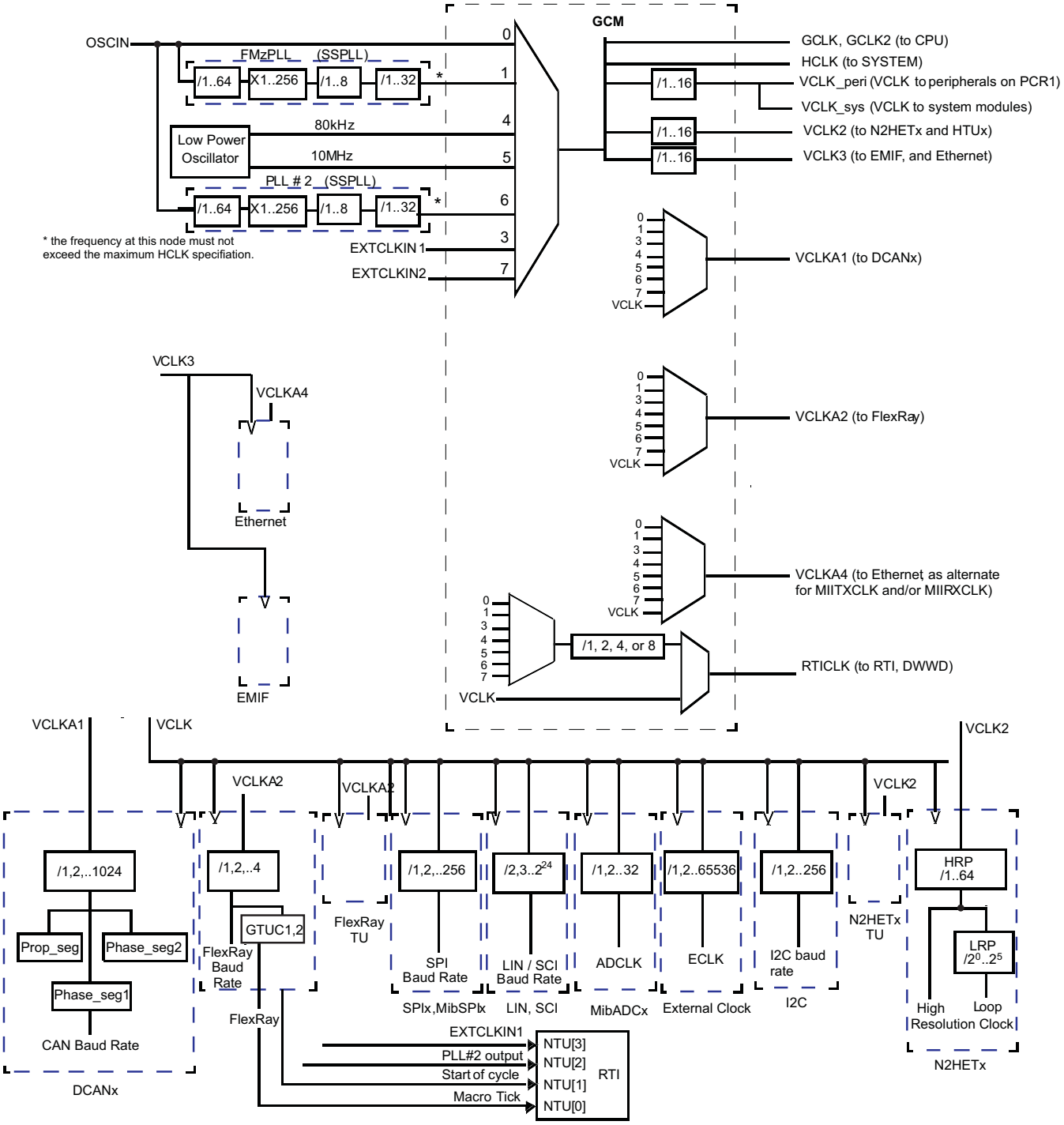


**Figure 6-7. Device Clock Domains**


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### 6.6.3 Clock Test Mode

The TMS570 platform architecture defines a special mode that allows various clock signals to be brought out on to the ECLK pin and N2HET1[12] device outputs. This mode is called the Clock Test mode. It is very useful for debugging purposes and can be configured via the CLKTEST register in the system module.

**Table 6-14. Clock Test Mode Options**

| SEL_ECP_PIN = CLKTEST[3-0] | SIGNAL ON ECLK | | SEL_GIO_PIN = CLKTEST[11-8] | SIGNAL ON N2HET1[12] |
|---|---|---|---|---|
| 0000 | Oscillator | | 0000 | Oscillator Valid Status |
| 0001 | Main PLL free-running clock output | | 0001 | Main PLL Valid status |
| 0010 | Reserved | | 0010 | Reserved |
| 0011 | EXTCLKIN1 | | 0011 | Reserved |
| 0100 | CLK80K | | 0100 | Reserved |
| 0101 | CLK10M | | 0101 | CLK10M Valid status |
| 0110 | Secondary PLL free-running clock output | | 0110 | Secondary PLL Valid Status |
| 0111 | EXTCLKIN2 | | 0111 | Reserved |
| 1000 | GCLK | | 1000 | CLK80K |
| 1001 | RTI Base | | 1001 | Reserved |
| 1010 | Reserved | | 1010 | Reserved |
| 1011 | VCLKA1 | | 1011 | Reserved |
| 1100 | VCLKA2 | | 1100 | Reserved |
| 1101 | Reserved | | 1101 | Reserved |
| 1110 | VCLKA4 | | 1110 | Reserved |
| 1111 | Reserved | | 1111 | Reserved |

## 6.7 Clock Monitoring

The LPO Clock Detect (LPOCLKDET) module consists of a clock monitor (CLKDET) and an internal low power oscillator (LPO).

The LPO provides two different clock sources – a low frequency (LFLPO) and a high frequency (HFLPO).

The CLKDET is a supervisor circuit for an externally supplied clock signal (OSCIN). In case the OSCIN frequency falls out of a frequency window, the CLKDET flags this condition in the global status register (GLBSTAT bit 0: OSC FAIL) and switches all clock domains sourced by OSCIN to the HFLPO clock (limp mode clock).

The valid OSCIN frequency range is defined as: $f_{HFLPO} / 4 < f_{OSCIN} < f_{HFLPO} * 4$.

### 6.7.1 Clock Monitor Timings

For more information on LPO and Clock detection, refer to Table 6-10.

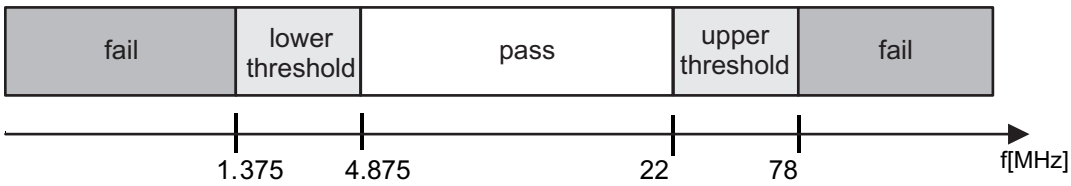


**Figure 6-8. LPO and Clock Detection, Untrimmed HFLPO**

### 6.7.2 External Clock (ECLK) Output Functionality

The ECLK pin can be configured to output a prescaled clock signal indicative of an internal device clock. This output can be externally monitored as a safety diagnostic.

### 6.7.3 Dual Clock Comparators

The Dual Clock Comparator (DCC) module determines the accuracy of selectable clock sources by counting the pulses of two independent clock sources (counter 0 and counter 1). If one clock is out of spec, an error signal is generated. For example, the DCC1 can be configured to use CLK10M as the reference clock (for counter 0) and VCLK as the "clock under test" (for counter 1). This configuration allows the DCC1 to monitor the PLL output clock when VCLK is using the PLL output as its source.

An additional use of this module is to measure the frequency of a selectable clock source, using the input clock as a reference, by counting the pulses of two independent clock sources. Counter 0 generates a fixed-width counting window after a preprogrammed number of pulses. Counter 1 generates a fixed-width pulse (1 cycle) after a preprogrammed number of pulses. This pulse sets as an error signal if counter 1 does not reach 0 within the counting window generated by counter 0.

#### 6.7.3.1 Features

- Takes two different clock sources as input to two independent counter blocks.
- One of the clock sources is the known-good, or reference clock; the second clock source is the "clock under test."
- Each counter block is programmable with initial, or seed values.
- The counter blocks start counting down from their seed values at the same time; a mismatch from the expected frequency for the clock under test generates an error signal which is used to interrupt the CPU.


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#### 6.7.3.2 Mapping of DCC Clock Source Inputs

**Table 6-15. DCC1 Counter 0 Clock Sources**

| CLOCK SOURCE [3:0] | CLOCK NAME |
|---|---|
| others | oscillator (OSCIN) |
| 0x5 | high frequency LPO |
| 0xA | test clock (TCK) |

**Table 6-16. DCC1 Counter 1 Clock Sources**

| KEY [3:0] | CLOCK SOURCE [3:0] | CLOCK NAME |
|---|---|---|
| others | - | N2HET1[31] |
| 0xA | 0x0 | Main PLL free-running clock output |
| | 0x1 | PLL #2 free-running clock output |
| | 0x2 | low frequency LPO |
| | 0x3 | high frequency LPO |
| | 0x4 | flash HD pump oscillator |
| | 0x5 | EXTCLKIN1 |
| | 0x6 | EXTCLKIN2 |
| | 0x7 | ring oscillator |
| | 0x8 - 0xF | VCLK |

**Table 6-17. DCC2 Counter 0 Clock Sources**

| CLOCK SOURCE [3:0] | CLOCK NAME |
|---|---|
| others | oscillator (OSCIN) |
| 0xA | test clock (TCK) |

**Table 6-18. DCC2 Counter 1 Clock Sources**

| KEY [3:0] | CLOCK SOURCE [3:0] | CLOCK NAME |
|---|---|---|
| others | - | N2HET2[0] |
| 0xA | 00x0 - 0x7 | Reserved |
| | 0x8 - 0xF | VCLK |

## 6.8 Glitch Filters

A glitch filter is present on the following signals.

**Table 6-19. Glitch Filter Timing Specifications**

| PIN | PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| nPORRST | $t_{f(nPORRST)}$ | Filter time nPORRST pin;<br>pulses less than MIN will be filtered out, pulses greater than MAX will generate a reset[(1)] | 475 | 2000 | ns |
| nRST | $t_{f(nRST)}$ | Filter time nRST pin;<br>pulses less than MIN will be filtered out, pulses greater than MAX will generate a reset | 475 | 2000 | ns |
| TEST | $t_{f(TEST)}$ | Filter time TEST pin;<br>pulses less than MIN will be filtered out, pulses greater than MAX will pass through | 475 | 2000 | ns |

(1) The glitch filter design on the nPORRST signal is designed such that no size pulse will reset any part of the microcontroller (flash pump, I/O pins, and so forth) without also generating a valid reset signal to the CPU.


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## 6.9 Device Memory Map

### *6.9.1 Memory Map Diagram*

Figure 6-9 shows the device memory map.

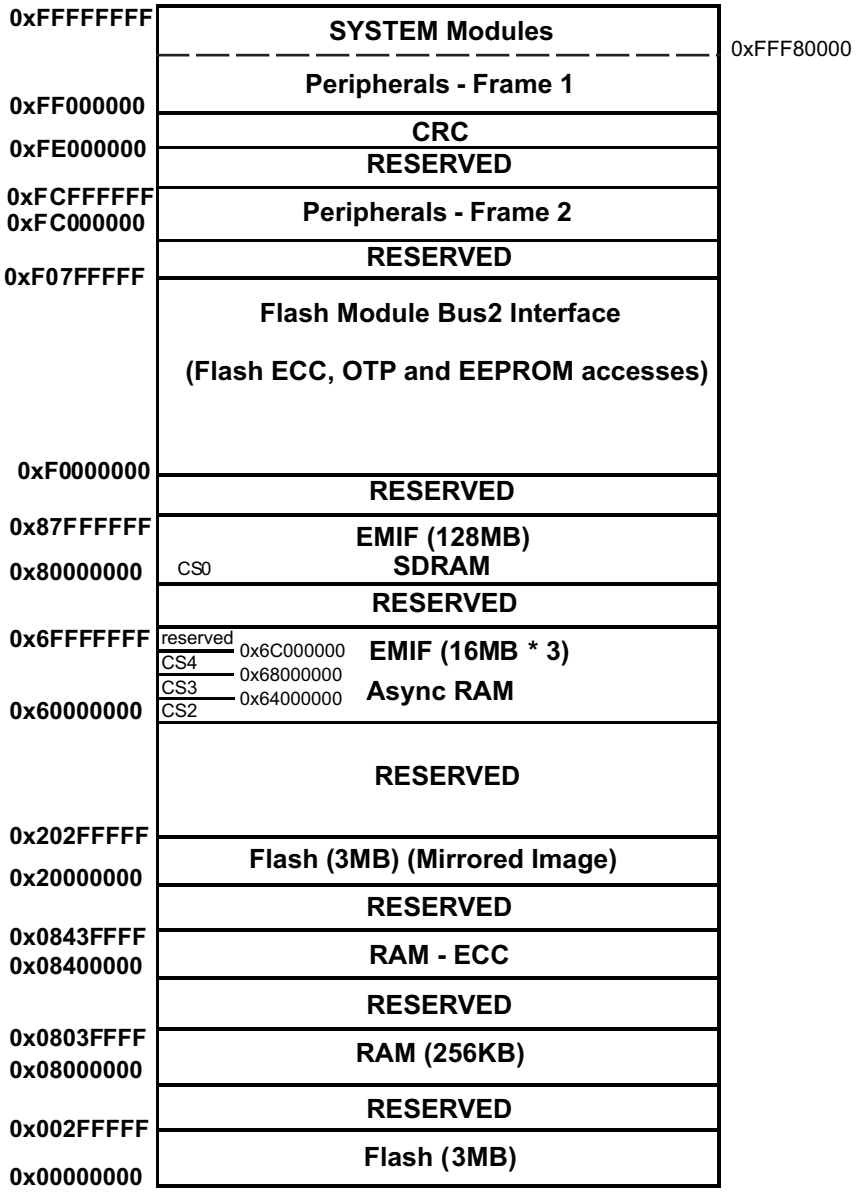


**Figure 6-9. TMS570LS3137 Memory Map**

The Flash memory is mirrored to support ECC logic testing. The base address of the mirrored Flash image is 0x2000 0000.

### 6.9.2 Memory Map Table

**Table 6-20. Device Memory Map**

| MODULE NAME | FRAME CHIP SELECT | FRAME ADDRESS RANGE | | FRAME SIZE | ACTUAL SIZE | RESPONSE FOR ACCESS TO UNIMPLEMENTED LOCATIONS IN FRAME |
|---|---|---|---|---|---|---|
| | | START | END | | | |
| **MEMORIES TIGHTLY COUPLED TO THE ARM CORTEX-R4F CPU** | | | | | | |
| TCM Flash | CS0 | 0x00000000 | 0x00FFFFFF | 16MB | 3MB | Abort |
| TCM RAM + RAM ECC | CSRAM0 | 0x08000000 | 0x0BFFFFFF | 64MB | 256KB | |
| Mirrored Flash | Flash mirror frame | 0x20000000 | 0x20FFFFFF | 16MB | 3MB | |
| **EXTERNAL MEMORY ACCESSES** | | | | | | |
| EMIF Chip Select 2 (asynchronous) | EMIF select 2 | 0x60000000 | 0x63FFFFFF | 64MB | 16MB | Access to "Reserved" space will generate Abort |
| EMIF Chip Select 3 (asynchronous) | EMIF select 3 | 0x64000000 | 0x67FFFFFF | 64MB | 16MB | |
| EMIF Chip Select 4 (asynchronous) | EMIF select 4 | 0x68000000 | 0x6BFFFFFF | 64MB | 16MB | |
| EMIF Chip Select 0 (synchronous) | EMIF select 0 | 0x80000000 | 0x87FFFFFF | 128MB | 128MB | |
| **FLASH MODULE BUS2 INTERFACE** | | | | | | |
| Customer OTP, TCM Flash Bank 0 | | 0xF0000000 | 0xF0001FFF | 8KB | 4KB | Abort |
| Customer OTP, TCM Flash Bank 1 | | 0xF0002000 | 0xF0003FFF | 8KB | 4KB | |
| Customer OTP, EEPROM Bank 7 | | 0xF000E000 | 0xF000FFFF | 8KB | 2KB | |
| Customer OTP–ECC, TCM Flash Bank 0 | | 0xF0040000 | 0xF00403FF | 1KB | 512B | |
| Customer OTP–ECC, TCM Flash Bank 1 | | 0xF0040400 | 0xF00407FF | 1KB | 512B | |
| Customer OTP–ECC, EEPROM Bank 7 | | 0xF0041C00 | 0xF0041FFF | 1KB | 256B | |
| TI OTP, TCM Flash Bank 0 | | 0xF0080000 | 0xF0081FFF | 8KB | 4KB | |
| TI OTP, TCM Flash Bank 1 | | 0xF0082000 | 0xF0083FFF | 8KB | 4KB | |
| TI OTP, EEPROM Bank 7 | | 0xF008E000 | 0xF008FFFF | 8KB | 2KB | |
| TI OTP–ECC, TCM Flash Bank 0 | | 0xF00C0000 | 0xF00C03FF | 1KB | 512B | |
| TI OTP–ECC, TCM Flash Bank 1 | | 0xF00C0400 | 0xF00C07FF | 1KB | 512B | |
| TI OTP–ECC, EEPROM Bank 7 | | 0xF00C1C00 | 0xF00C1FFF | 1KB | 256B | |
| EEPROM Bank–ECC | | 0xF0100000 | 0xF013FFFF | 256KB | 8KB | |
| EEPROM Bank | | 0xF0200000 | 0xF03FFFFF | 2MB | 64KB | |
| Flash Data Space ECC | | 0xF0400000 | 0xF04FFFFF | 1MB | 384KB | |
| **ETHERNET AND EMIF SLAVE INTERFACES** | | | | | | |
| CPPI Memory Slave (Ethernet RAM) | | 0xFC520000 | 0xFC521FFF | 8KB | 8KB | Abort |
| EMAC Slave (Ethernet Slave) | | 0xFCF78000 | 0xFCF787FF | 2KB | 2KB | No error |
| EMACSS Wrapper (Ethernet Wrapper) | | 0xFCF78800 | 0xFCF788FF | 256B | 256B | No error |
| Ethernet MDIO Interface | | 0xFCF78900 | 0xFCF789FF | 256B | 256B | No error |
| EMIF Registers | | 0xFCFFE800 | 0xFCFFE8FF | 256B | 256B | Abort |


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## Table 6-20. Device Memory Map (continued)

| MODULE NAME | FRAME CHIP SELECT | FRAME ADDRESS RANGE | | FRAME SIZE | ACTUAL SIZE | RESPONSE FOR ACCESS TO UNIMPLEMENTED LOCATIONS IN FRAME |
|---|---|---|---|---|---|---|
| | | START | END | | | |
| **CYCLIC REDUNDANCY CHECKER (CRC) MODULE REGISTERS** | | | | | | |
| CRC | CRC frame | 0xFE000000 | 0xFEFFFFFF | 16MB | 512B | Accesses above 0x200 generate abort. |
| **PERIPHERAL MEMORIES** | | | | | | |
| MIBSPI5 RAM | PCS[5] | 0xFF0A0000 | 0xFF0BFFFF | 128KB | 2KB | Abort for accesses above 2KB |
| MIBSPI3 RAM | PCS[6] | 0xFF0C0000 | 0xFF0DFFFF | 128KB | 2KB | Abort for accesses above 2KB |
| MIBSPI1 RAM | PCS[7] | 0xFF0E0000 | 0xFF0FFFFF | 128KB | 2KB | Abort for accesses above 2KB |
| DCAN3 RAM | PCS[13] | 0xFF1A0000 | 0xFF1BFFFF | 128KB | 2KB | Wrap around for accesses to unimplemented address offsets lower than 0x7FF. Abort generated for accesses beyond offset 0x800. |
| DCAN2 RAM | PCS[14] | 0xFF1C0000 | 0xFF1DFFFF | 128KB | 2KB | Wrap around for accesses to unimplemented address offsets lower than 0x7FF. Abort generated for accesses beyond offset 0x800. |
| DCAN1 RAM | PCS[15] | 0xFF1E0000 | 0xFF1FFFFF | 128KB | 2KB | Wrap around for accesses to unimplemented address offsets lower than 0x7FF. Abort generated for accesses beyond offset 0x800. |
| MIBADC2 RAM | PCS[29] | 0xFF3A0000 | 0xFF3BFFFF | 128KB | 8KB | Wrap around for accesses to unimplemented address offsets lower than 0x1FFF. Abort generated for accesses beyond 0x1FFF. |
| MIBADC1 RAM | PCS[31] | 0xFF3E0000 | 0xFF3FFFFF | 128KB | 8KB | Wrap around for accesses to unimplemented address offsets lower than 0x1FFF. Abort generated for accesses beyond 0x1FFF. |
| N2HET2 RAM | PCS[34] | 0xFF440000 | 0xFF45FFFF | 128KB | 16KB | Wrap around for accesses to unimplemented address offsets lower than 0x3FFF. Abort generated for accesses beyond 0x3FFF. |
| N2HET1 RAM | PCS[35] | 0xFF460000 | 0xFF47FFFF | 128KB | 16KB | Wrap around for accesses to unimplemented address offsets lower than 0x3FFF. Abort generated for accesses beyond 0x3FFF. |
| HTU2 RAM | PCS[38] | 0xFF4C0000 | 0xFF4DFFFF | 128KB | 1KB | Abort |
| HTU1 RAM | PCS[39] | 0xFF4E0000 | 0xFF4FFFFF | 128KB | 1KB | Abort |
| FTU RAM | PCS[40] | 0xFF500000 | 0xFF51FFFF | 128KB | 1KB | Abort |
| **DEBUG COMPONENTS** | | | | | | |
| CoreSight Debug ROM | CSCS0 | 0xFFA00000 | 0xFFA00FFF | 4KB | 4KB | Reads: 0, writes: no effect |
| Cortex-R4F Debug | CSCS1 | 0xFFA01000 | 0xFFA01FFF | 4KB | 4KB | Reads: 0, writes: no effect |
| ETM-R4 | CSCS2 | 0xFFA02000 | 0xFFA02FFF | 4KB | 4KB | Reads: 0, writes: no effect |
| CoreSight TPIU | CSCS3 | 0xFFA03000 | 0xFFA03FFF | 4KB | 4KB | Reads: 0, writes: no effect |
| POM | CSCS4 | 0xFFA04000 | 0xFFA04FFF | 4KB | 4KB | Abort |
| **PERIPHERAL CONTROL REGISTERS** | | | | | | |
| FTU | PS[23] | 0xFFF7A000 | 0xFFF7A1FF | 512B | 512B | Reads: 0, writes: no effect |
| HTU1 | PS[22] | 0xFFF7A400 | 0xFFF7A4FF | 256B | 256B | Reads: 0, writes: no effect |
| HTU2 | PS[22] | 0xFFF7A500 | 0xFFF7A5FF | 256B | 256B | Reads: 0, writes: no effect |
| N2HET1 | PS[17] | 0xFFF7B800 | 0xFFF7B8FF | 256B | 256B | Reads: 0, writes: no effect |
| N2HET2 | PS[17] | 0xFFF7B900 | 0xFFF7B9FF | 256B | 256B | Reads: 0, writes: no effect |
| GPIO | PS[16] | 0xFFF7BC00 | 0xFFF7BCFF | 256B | 256B | Reads: 0, writes: no effect |
| MIBADC1 | PS[15] | 0xFFF7C000 | 0xFFF7C1FF | 512B | 512B | Reads: 0, writes: no effect |
| MIBADC2 | PS[15] | 0xFFF7C200 | 0xFFF7C3FF | 512B | 512B | Reads: 0, writes: no effect |
| FlexRay | PS[12]+PS[13] | 0xFFF7C800 | 0xFFF7CFFF | 2KB | 2KB | Reads: 0, writes: no effect |
| I2C | PS[10] | 0xFFF7D400 | 0xFFF7D4FF | 256B | 256B | Reads: 0, writes: no effect |
| DCAN1 | PS[8] | 0xFFF7DC00 | 0xFFF7DDFF | 512B | 512B | Reads: 0, writes: no effect |
| DCAN2 | PS[8] | 0xFFF7DE00 | 0xFFF7DFFF | 512B | 512B | Reads: 0, writes: no effect |

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## Table 6-20. Device Memory Map (continued)

| MODULE NAME | FRAME CHIP SELECT | FRAME ADDRESS RANGE | | FRAME SIZE | ACTUAL SIZE | RESPONSE FOR ACCESS TO UNIMPLEMENTED LOCATIONS IN FRAME |
|---|---|---|---|---|---|---|
| | | START | END | | | |
| DCAN3 | PS[7] | 0xFFF7E000 | 0xFFF7E1FF | 512B | 512B | Reads: 0, writes: no effect |
| LIN | PS[6] | 0xFFF7E400 | 0xFFF7E4FF | 256B | 256B | Reads: 0, writes: no effect |
| SCI | PS[6] | 0xFFF7E500 | 0xFFF7E5FF | 256B | 256B | Reads: 0, writes: no effect |
| MibSPI1 | PS[2] | 0xFFF7F400 | 0xFFF7F5FF | 512B | 512B | Reads: 0, writes: no effect |
| SPI2 | PS[2] | 0xFFF7F600 | 0xFFF7F7FF | 512B | 512B | Reads: 0, writes: no effect |
| MibSPI3 | PS[1] | 0xFFF7F800 | 0xFFF7F9FF | 512B | 512B | Reads: 0, writes: no effect |
| SPI4 | PS[1] | 0xFFF7FA00 | 0xFFF7FBFF | 512B | 512B | Reads: 0, writes: no effect |
| MibSPI5 | PS[0] | 0xFFF7FC00 | 0xFFF7FDFF | 512B | 512B | Reads: 0, writes: no effect |
| **SYSTEM MODULES CONTROL REGISTERS AND MEMORIES** | | | | | | |
| DMA RAM | PPCS0 | 0xFFF80000 | 0xFFF80FFF | 4KB | 4KB | Abort |
| VIM RAM | PPCS2 | 0xFFF82000 | 0xFFF82FFF | 4KB | 1KB | Wrap around for accesses to unimplemented address offsets between 1kB and 4kB. |
| RTP RAM | PPCS3 | 0xFFF83000 | 0xFFF83FFF | 4KB | 4KB | Abort |
| Flash Module | PPCS7 | 0xFFF87000 | 0xFFF87FFF | 4KB | 4KB | Abort |
| eFuse Controller | PPCS12 | 0xFFF8C000 | 0xFFF8CFFF | 4KB | 4KB | Abort |
| Power Management Module (PMM) | PPSE0 | 0xFFFF0000 | 0xFFFF01FF | 512B | 512B | Abort |
| Test Controller (FMTM) | PPSE1 | 0xFFFF0400 | 0xFFFF07FF | 1KB | 1KB | Reads: 0, writes: no effect |
| PCR registers | PPS0 | 0xFFFFE000 | 0xFFFFE0FF | 256B | 256B | Reads: 0, writes: no effect |
| System Module - Frame 2 (see device TRM) | PPS0 | 0xFFFFE100 | 0xFFFFE1FF | 256B | 256B | Reads: 0, writes: no effect |
| PBIST | PPS1 | 0xFFFFE400 | 0xFFFFE5FF | 512B | 512B | Reads: 0, writes: no effect |
| STC | PPS1 | 0xFFFFE600 | 0xFFFFE6FF | 256B | 256B | Generates address error interrupt, if enabled |
| IOMM Multiplexing Control Module | PPS2 | 0xFFFFEA00 | 0xFFFFEBFF | 512B | 512B | Reads: 0, writes: no effect |
| DCC1 | PPS3 | 0xFFFFEC00 | 0xFFFFECFF | 256B | 256B | Reads: 0, writes: no effect |
| DMA | PPS4 | 0xFFFFF000 | 0xFFFFF3FF | 1KB | 1KB | Reads: 0, writes: no effect |
| DCC2 | PPS5 | 0xFFFFF400 | 0xFFFFF4FF | 256B | 256B | Reads: 0, writes: no effect |
| ESM | PPS5 | 0xFFFFF500 | 0xFFFFF5FF | 256B | 256B | Reads: 0, writes: no effect |
| CCMR4 | PPS5 | 0xFFFFF600 | 0xFFFFF6FF | 256B | 256B | Reads: 0, writes: no effect |
| DMM | PPS5 | 0xFFFFF700 | 0xFFFFF7FF | 256B | 256B | Reads: 0, writes: no effect |
| RAM ECC even | PPS6 | 0xFFFFF800 | 0xFFFFF8FF | 256B | 256B | Reads: 0, writes: no effect |
| RAM ECC odd | PPS6 | 0xFFFFF900 | 0xFFFFF9FF | 256B | 256B | Reads: 0, writes: no effect |
| RTP | PPS6 | 0xFFFFFA00 | 0xFFFFFAFF | 256B | 256B | Reads: 0, writes: no effect |
| RTI + DWWD | PPS7 | 0xFFFFFC00 | 0xFFFFFCFF | 256B | 256B | Reads: 0, writes: no effect |
| VIM Parity | PPS7 | 0xFFFFFD00 | 0xFFFFFDFF | 256B | 256B | Reads: 0, writes: no effect |
| VIM | PPS7 | 0xFFFFFE00 | 0xFFFFFEFF | 256B | 256B | Reads: 0, writes: no effect |
| System Module - Frame 1 (see device TRM) | PPS7 | 0xFFFFFF00 | 0xFFFFFFFF | 256B | 256B | Reads: 0, writes: no effect |


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### 6.9.3 Master/Slave Access Privileges

Table 6-21 lists the access permissions for each bus master on the device. A bus master is a module that can initiate a read or a write transaction on the device.

Each slave module on the main interconnect is listed in the table. A "Yes" indicates that the module listed in the "MASTERS" column can access that slave module.

**Table 6-21. Master / Slave Access Matrix**

| MASTERS | ACCESS MODE | SLAVES ON MAIN SCR | | | | |
|---|---|---|---|---|---|---|
| | | Flash Module Bus2 Interface: OTP, ECC, EEPROM Bank | Non-CPU Accesses to Program Flash and CPU Data RAM | CRC | EMIF, Ethernet Slave Interfaces | Peripheral Control Registers, All Peripheral Memories, And All System Module Control Registers And Memories |
| CPU READ | User/Privilege | Yes | Yes | Yes | Yes | Yes |
| CPU WRITE | User/Privilege | No | Yes | Yes | Yes | Yes |
| DMA | User | Yes | Yes | Yes | Yes | Yes |
| POM | User | Yes | Yes | Yes | Yes | Yes |
| DMM | User | Yes | Yes | Yes | Yes | Yes |
| DAP | Privilege | Yes | Yes | Yes | Yes | Yes |
| HTU1 | Privilege | No | Yes | Yes | Yes | Yes |
| HTU2 | Privilege | No | Yes | Yes | Yes | Yes |
| FTU | User | No | Yes | Yes | Yes | Yes |
| EMAC DMA | User | No | Yes | No | Yes | No |

#### 6.9.3.1 Special Notes on Accesses to Certain Slaves

Write accesses to the Power Domain Management Module (PMM) control registers are limited to the CPU (master id = 1). The other masters can only read from these registers.

A debugger can also write to the PMM registers. The master-id check is disabled in debug mode.

The device contains dedicated logic to generate a bus error response on any access to a module that is in a power domain that has been turned OFF.

### 6.9.4 POM Overlay Considerations

- The POM overlay can map onto up to 8MB of the internal or external memory space. The starting address and the size of the memory overlay are configurable via the POM module control registers. Care must be taken to ensure that the overlay is mapped on to available memory.
- ECC must be disabled by software via CP15 in case POM overlay is enabled; otherwise ECC errors will be generated.
- POM overlay must not be enabled when the flash and internal RAM memories are swapped via the MEM SWAP field of the Bus Matrix Module Control Register 1 (BMMCR1).
- When POM is used to overlay the flash onto internal or external RAM, there is a bus contention possibility when another master accesses the TCM flash. This results in a system hang.
  - The POM module implements a time-out feature to detect this exact scenario. The time-out needs to be enabled whenever POM overlay is enabled.
  - The time-out can be enabled by writing 1010 to the Enable TimeOut (ETO) field of the POM Global Control register (POMGLBCTRL, address = 0xFFA04000).
  - In case a read request by the POM cannot be completed within 32 HCLK cycles, the time-out (TO) flag is set in the POM Flag register (POMFLG, address = 0xFFA0400C). Also, an abort is generated to the CPU. This can be a prefetch abort for an instruction fetch or a data abort for a data fetch.
  - The prefetch- and data-abort handlers must be modified to check if the TO flag in the POM module is set. If so, then the application can assume that the time-out is caused by a bus contention between the POM transaction and another master accessing the same memory region. The abort handlers need to clear the TO flag, so that any further aborts are not misinterpreted as having been caused due to a time-out from the POM.


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## 6.10 Flash Memory

### *6.10.1 Flash Memory Configuration*

**Flash Bank:** A separate block of logic consisting of 1 to 16 sectors. Each flash bank normally has a customer-OTP and a TI-OTP area. These flash sectors share input/output buffers, data paths, sense amplifiers, and control logic.

**Flash Sector:** A contiguous region of flash memory which must be erased simultaneously due to physical construction constraints.

**Flash Pump:** A charge pump which generates all the voltages required for reading, programming, or erasing the flash banks.

**Flash Module:** Interface circuitry required between the host CPU and the flash banks and pump module.

**Table 6-22. Flash Memory Banks and Sectors**

| MEMORY ARRAYS (OR BANKS)(1) | SECTOR NO. | SEGMENT (BYTES) | LOW ADDRESS | HIGH ADDRESS |
|---|---|---|---|---|
| BANK0 (1.5MB) | 0 | 32KB | 0x0000_0000 | 0x0000_7FFF |
| | 1 | 32KB | 0x0000_8000 | 0x0000_FFFF |
| | 2 | 32KB | 0x0001_0000 | 0x0001_7FFF |
| | 3 | 32KB | 0x0001_8000 | 0x0001_FFFF |
| | 4 | 128KB | 0x0002_0000 | 0x0003_FFFF |
| | 5 | 128KB | 0x0004_0000 | 0x0005_FFFF |
| | 6 | 128KB | 0x0006_0000 | 0x0007_FFFF |
| | 7 | 128KB | 0x0008_0000 | 0x0009_FFFF |
| | 8 | 128KB | 0x000A_0000 | 0x000B_FFFF |
| | 9 | 128KB | 0x000C_0000 | 0x000D_FFFF |
| | 10 | 128KB | 0x000E_0000 | 0x000F_FFFF |
| | 11 | 128KB | 0x0010_0000 | 0x0011_FFFF |
| | 12 | 128KB | 0x0012_0000 | 0x0013_FFFF |
| | 13 | 128KB | 0x0014_0000 | 0x0015_FFFF |
| | 14 | 128KB | 0x0016_0000 | 0x0017_FFFF |
| BANK1 (1.5MB) | 0 | 128KB | 0x0018_0000 | 0x0019_FFFF |
| | 1 | 128KB | 0x001A_0000 | 0x001B_FFFF |
| | 2 | 128KB | 0x001C_0000 | 0x001D_FFFF |
| | 3 | 128KB | 0x001E_0000 | 0x001F_FFFF |
| | 4 | 128KB | 0x0020_0000 | 0x0021_FFFF |
| | 5 | 128KB | 0x0022_0000 | 0x0023_FFFF |
| | 6 | 128KB | 0x0024_0000 | 0x0025_FFFF |
| | 7 | 128KB | 0x0026_0000 | 0x0027_FFFF |
| | 8 | 128KB | 0x0028_0000 | 0x0029_FFFF |
| | 9 | 128KB | 0x002A_0000 | 0x002B_FFFF |
| | 10 | 128KB | 0x002C_0000 | 0x002D_FFFF |
| | 11 | 128KB | 0x002E_0000 | 0x002F_FFFF |
| BANK7 (64KB) for EEPROM emulation(2)(3) | 0 | 16KB | 0xF020_0000 | 0xF020_3FFF |
| | 1 | 16KB | 0xF020_4000 | 0xF020_7FFF |
| | 2 | 16KB | 0xF020_8000 | 0xF020_BFFF |
| | 3 | 16KB | 0xF020_C000 | 0xF020_FFFF |

(1) The Flash banks are 144-bit-wide bank with ECC support.
(2) The flash bank7 can be programmed while executing code from flash bank0 or bank1.
(3) Code execution is not allowed from flash bank7.

### 6.10.2 Main Features of Flash Module

- Support for multiple flash banks for program and/or data storage
- Simultaneous read access on a bank while performing program or erase operation on any other bank
- Integrated state machines to automate flash erase and program operations
- Software interface for flash program and erase operations
- Pipelined mode operation to improve instruction access interface bandwidth
- Support for Single Error Correction Double Error Detection (SECDED) block inside Cortex-R4F CPU
  - Error address is captured for host system debugging
- Support for a rich set of diagnostic features

### 6.10.3 ECC Protection for Flash Accesses

All accesses to the program flash memory are protected by Single Error Correction Double Error Detection (SECDED) logic embedded inside the CPU. The flash module provides 8 bits of ECC code for 64 bits of instructions or data fetched from the flash memory. The CPU calculates the expected ECC code based on the 64 bits received and compares it with the ECC code returned by the flash module. A single-bit error is corrected and flagged by the CPU, while a multibit error is only flagged. The CPU signals an ECC error via its Event bus. This signaling mechanism is not enabled by default and must be enabled by setting the 'X' bit of the Performance Monitor Control Register, c9.

```
MRC p15,#0,r1,c9,c12,#0    ;Enabling Event monitor states
ORR r1, r1, #0x00000010
MCR p15,#0,r1,c9,c12,#0    ;Set 4th bit (‘X’) of PMNC register
MRC p15,#0,r1,c9,c12,#0
```

The application must also explicitly enable the CPU's ECC checking for accesses on the CPU's ATCM and BTCM interfaces. These are connected to the program flash and data RAM respectively. ECC checking for these interfaces can be done by setting the B1TCMPCEN, B0TCMPCEN and ATCMPCEN bits of the System Control coprocessor's Auxiliary Control Register, c1.

```
MRC p15, #0, r1, c1, c0, #1
ORR r1, r1, #0x0e000000        ;Enable ECC checking for ATCM and BTCMs
DMB
MCR p15, #0, r1, c1, c0, #1
```

### 6.10.4 Flash Access Speeds

For information on flash memory access speeds and the relevant wait states required, refer to Section 5.6.

### 6.10.5 Flash Program and Erase Timings for Program Flash

**Table 6-23. Timing Specifications for Program Flash**

| PARAMETER | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{prog}$ (144bit) | Wide Word (144bit) programming time | | | 40 | 300 | µs |
| $t_{prog}$ (Total) | 3-MB programming time (1) | -40°C to 125°C | | | 32 | s |
| | | 0°C to 60°C, for first 25 cycles | | 8 | 16 | s |
| $t_{erase}$ | Sector/Bank erase time (2) | -40°C to 125°C | | 0.03 | 4 | s |
| | | 0°C to 60°C, for first 25 cycles | | 16 | 100 | ms |
| $t_{wec}$ | Write/erase cycles with 15-year Data Retention requirement | -40°C to 125°C | | | 1000 | cycles |

(1) This programming time includes overhead of state machine, but does not include data transfer time. The programming time assumes programming 144 bits at a time at the maximum specified operating frequency.
(2) During bank erase, the selected sectors are erased simultaneously. The time to erase the bank is specified as equal to the time to erase a sector.


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### 6.10.6 Flash Program and Erase Timings for Data Flash

**Table 6-24. Timing Specifications for Data Flash**

| PARAMETER | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{prog}$ (144bit) | Wide Word (144bit) programming time | | | 40 | 300 | µs |
| $t_{prog}$ (Total) | 64-KB programming time(1) | -40°C to 125°C | | | 660 | ms |
| | | 0°C to 60°C, for first 25 cycles | | 165 | 330 | ms |
| $t_{erase}$ | Sector/Bank erase time(2) | -40°C to 125°C | | 0.2 | 8 | s |
| | | 0°C to 60°C, for first 25 cycles | | 14 | 100 | ms |
| $t_{wec}$ | Write/erase cycles with 15-year Data Retention requirement | -40°C to 125°C | | | 100000 | cycles |

(1) This programming time includes overhead of state machine, but does not include data transfer time. The programming time assumes programming 144 bits at a time at the maximum specified operating frequency.
(2) During bank erase, the selected sectors are erased simultaneously. The time to erase the bank is specified as equal to the time to erase a sector.

## 6.11 Tightly Coupled RAM (TCRAM) Interface Module

Figure 6-10 illustrates the connection of the Tightly Coupled RAM (TCRAM) to the Cortex-R4F CPU.

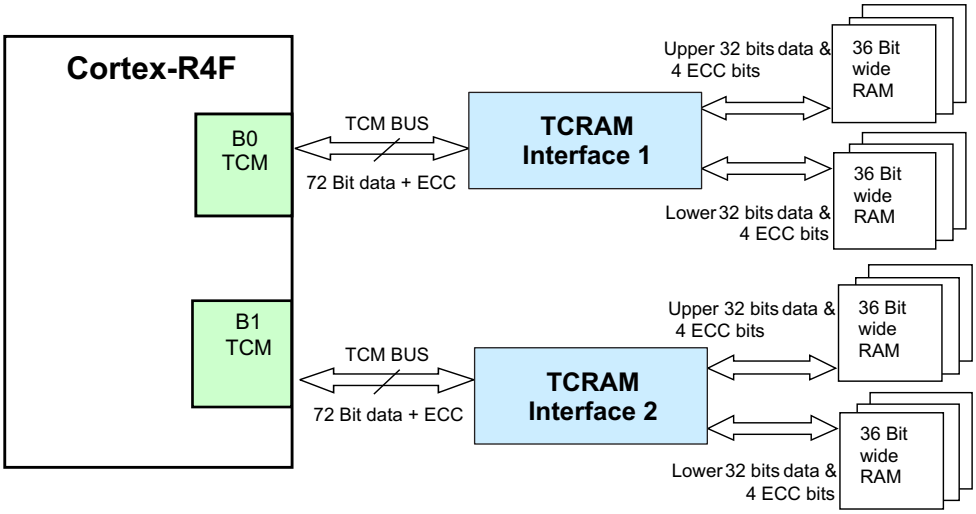


**Figure 6-10. TCRAM Block Diagram**

### *6.11.1 Features*

The features of the TCRAM Module are:

- Acts as slave to the Cortex-R4F CPU's BTCM interface
- Supports CPU's internal ECC scheme by providing 64-bit data and 8-bit ECC code
- Monitors CPU Event Bus and generates single or multibit error interrupts
- Stores addresses for single and multibit errors
- Supports RAM trace module
- Provides CPU address bus integrity checking by supporting parity checking on the address bus
- Performs redundant address decoding for the RAM bank chip select and ECC select generation logic
- Provides enhanced safety for the RAM addressing by implementing two 36-bit wide byte-interleaved RAM banks and generating independent RAM access control signals to the two banks
- Supports auto-initialization of the RAM banks along with the ECC bits
- No support for bit-wise RAM accesses

### *6.11.2 TCRAM Interface ECC Support*

The TCRAM interface passes on the ECC code for each data read by the Cortex-R4F CPU from the RAM. It also stores the CPU's ECC port contents in the ECC RAM when the CPU does a write to the RAM. The TCRAM interface monitors the CPU's event bus and provides registers for indicating singlebit or multibit errors and also for identifying the address that caused the single or multibit error. The event signaling and the ECC checking for the RAM accesses must be enabled inside the CPU.

For more information see the device specific technical reference manual.

## 6.12 Parity Protection for Peripheral RAMs

Most peripheral RAMs are protected by odd/even parity checking. During a read access the parity is calculated based on the data read from the peripheral RAM and compared with the good parity value stored in the parity RAM for that peripheral. If any word fails the parity check, the module generates a parity error signal that is mapped to the Error Signaling Module. The module also captures the peripheral RAM address that caused the parity error.


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The parity protection for peripheral RAMs is not enabled by default and must be enabled by the application. Each individual peripheral contains control registers to enable the parity protection for accesses to its RAM.

**NOTE**

The CPU read access gets the actual data from the peripheral. The application can choose to generate an interrupt whenever a peripheral RAM parity error is detected.

## 6.13 On-Chip SRAM Initialization and Testing

### *6.13.1 On-Chip SRAM Self-Test Using PBIST*

#### 6.13.1.1 Features

- Extensive instruction set to support various memory test algorithms
- ROM-based algorithms allow application to run TI production-level memory tests
- Independent testing of all on-chip SRAM

#### 6.13.1.2 PBIST RAM Groups

**Table 6-25. PBIST RAM Grouping**

| MEMORY | RAM GROUP | TEST CLOCK | MEM TYPE | TEST PATTERN (ALGORITHM) | | | |
|---|---|---|---|---|---|---|---|
| | | | | TRIPLE READ SLOW READ | TRIPLE READ FAST READ | MARCH 13N(1) TWO PORT (CYCLES) | MARCH 13N(1) SINGLE PORT (CYCLES) |
| | | | | ALGO MASK 0x1 | ALGO MASK 0x2 | ALGO MASK 0x4 | ALGO MASK 0x8 |
| PBIST_ROM | 1 | ROM CLK | ROM | 24578 | 8194 | | |
| STC_ROM | 2 | ROM CLK | ROM | 19586 | 6530 | | |
| DCAN1 | 3 | VCLK | Dual Port | | | 25200 | |
| DCAN2 | 4 | VCLK | Dual Port | | | 25200 | |
| DCAN3 | 5 | VCLK | Dual Port | | | 25200 | |
| ESRAM1(2) | 6 | HCLK | Single Port | | | | 266280 |
| MIBSPI1 | 7 | VCLK | Dual Port | | | 33440 | |
| MIBSPI3 | 8 | VCLK | Dual Port | | | 33440 | |
| MIBSPI5 | 9 | VCLK | Dual Port | | | 33440 | |
| VIM | 10 | VCLK | Dual Port | | | 12560 | |
| MIBADC1 | 11 | VCLK | Dual Port | | | 4200 | |
| DMA | 12 | HCLK | Dual Port | | | 18960 | |
| N2HET1 | 13 | VCLK | Dual Port | | | 31680 | |
| HTU1 | 14 | VCLK | Dual Port | | | 6480 | |
| RTP | 15 | HCLK | Dual Port | | | 37800 | |
| FLEXRAY | 16 | VCLK | Dual Port | | | 75400 | |
| | 17 | | Single Port | | | | 133160 |
| MIBADC2 | 18 | VCLK | Dual Port | | | 4200 | |
| N2HET2 | 19 | VCLK | Dual Port | | | 31680 | |
| HTU2 | 20 | VCLK | Dual Port | | | 6480 | |
| ESRAM5(3) | 21 | HCLK | Single Port | | | | 266280 |
| ESRAM6(4) | 22 | HCLK | Single Port | | | | 266280 |
| ETHERNET | 23 | VCLK3 | Dual Port | | | 8700 | |
| | 24 | | | | | 6360 | |
| | 25 | | Single Port | | | | 133160 |
| ESRAM8(5) | 28 | HCLK | Single Port | | | | 266280 |

(1) There are several memory testing algorithms stored in the PBIST ROM. However, TI recommends the March13N algorithm for application testing.
(2) ESRAM1: Address 0x08000000 - 0x0800FFFF (Always on power domain)
(3) ESRAM5: Address 0x08010000 - 0x0801FFFF (RAM power domain 1)
(4) ESRAM6: Address 0x08020000 - 0x0802FFFF (RAM power domain 2)
(5) ESRAM8: Address 0x08030000 - 0x0803FFFF (RAM power domain 3)


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The PBIST ROM clock frequency is limited to 90 MHz, if 90 MHz < HCLK <= HCLKmax, or HCLK, if HCLK <= 90 MHz.

The PBIST ROM clock is divided down from HCLK. The divider is selected by programming the ROM_DIV field of the Memory Self-Test Global Control Register (MSTGCR) at address 0xFFFFFF58.

### 6.13.2 On-Chip SRAM Auto Initialization

This microcontroller allows some of the on-chip memories to be initialized to zero via the Memory Hardware Initialization mechanism in the System module. This hardware mechanism allows an application to program the memory arrays with error detection capability to a known state based on their error detection scheme (odd/even parity or ECC).

The MINITGCR register enables the memory initialization sequence, and the MSINENA register selects the memories that are to be initialized.

For more information on these registers see the device specific technical reference manual.

The mapping of the different on-chip memories to the specific bits of the MSINENA registers is shown in Table 6-26.

**Table 6-26. Memory Initialization**

| CONNECTING MODULE | ADDRESS RANGE | | MSINENA REGISTER BIT # |
|---|---|---|---|
| | BASE ADDRESS | ENDING ADDRESS | |
| RAM (PD#1) | 0x08000000 | 0x0800FFFF | 0 (1) |
| RAM (RAM_PD#1) | 0x08010000 | 0x0801FFFF | 0 (1) |
| RAM (RAM_PD#2) | 0x08020000 | 0x0802FFFF | 0 (1) |
| RAM (RAM_PD#3) | 0x08030000 | 0x0803FFFF | 0 (1) |
| MIBSPI5 RAM | 0xFF0A0000 | 0xFF0BFFFF | 12 (2) |
| MIBSPI3 RAM | 0xFF0C0000 | 0xFF0DFFFF | 11 (2) |
| MIBSPI1 RAM | 0xFF0E0000 | 0xFF0FFFFF | 7 (2) |
| DCAN3 RAM | 0xFF1A0000 | 0xFF1BFFFF | 10 |
| DCAN2 RAM | 0xFF1C0000 | 0xFF1DFFFF | 6 |
| DCAN1 RAM | 0xFF1E0000 | 0xFF1FFFFF | 5 |
| FlexRay RAM | RAM is not CPU-Addressable | | n/a (3) |
| MIBADC2 RAM | 0xFF3A0000 | 0xFF3BFFFF | 14 |
| MIBADC1 RAM | 0xFF3E0000 | 0xFF3FFFFF | 8 |
| N2HET2 RAM | 0xFF440000 | 0xFF45FFFF | 15 |
| N2HET1 RAM | 0xFF460000 | 0xFF47FFFF | 3 |
| HTU2 RAM | 0xFF4C0000 | 0xFF4DFFFF | 16 |
| HTU1 RAM | 0xFF4E0000 | 0xFF4FFFFF | 4 |
| DMA RAM | 0xFFF80000 | 0xFFF80FFF | 1 |
| VIM RAM | 0xFFF82000 | 0xFFF82FFF | 2 |
| RTP RAM | 0xFFF83000 | 0xFFF83FFF | n/a |
| FTU RAM | 0xFF500000 | 0xFF51FFFF | 13 |
| Ethernet RAM (CPPI Memory Slave) | 0xFC520000 | 0xFC521FFF | n/a |

(1) The TCM RAM wrapper has separate control bits to select the RAM power domain that is to be auto-initialized.
(2) The MibSPIx modules perform an initialization of the transmit and receive RAMs as soon as the module is released from its local reset via the SPIGCR0 register. This is independent of whether the application chooses to initialize the MibSPIx RAMs using the system module auto-initialization method. Before the MibSPI RAM can be initialized using the system module auto-initialization method: (I) The module must be released from its local reset, AND (ii) The application must poll for the "BUF INIT ACTIVE" status flag in the SPIFLG register to become cleared (zero)
(3) Reserved only. The FlexRay RAM has its own initialization mechanism.

## 6.14 External Memory Interface (EMIF)

### *6.14.1 Features*

The EMIF includes many features to enhance the ease and flexibility of connecting to external asynchronous memories or SDRAM devices. The EMIF features includes support for:

- 3 addressable chip select for asynchronous memories of up to 16MB each
- 1 addressable chip select space for SDRAMs up to 128MB
- 8- or 16-bit data bus width
- Programmable cycle timings such as setup, strobe, and hold times as well as turnaround time
- Select strobe mode
- Extended Wait mode
- Data bus parking

### *6.14.2 Electrical and Timing Specifications*

#### 6.14.2.1 Asynchronous RAM

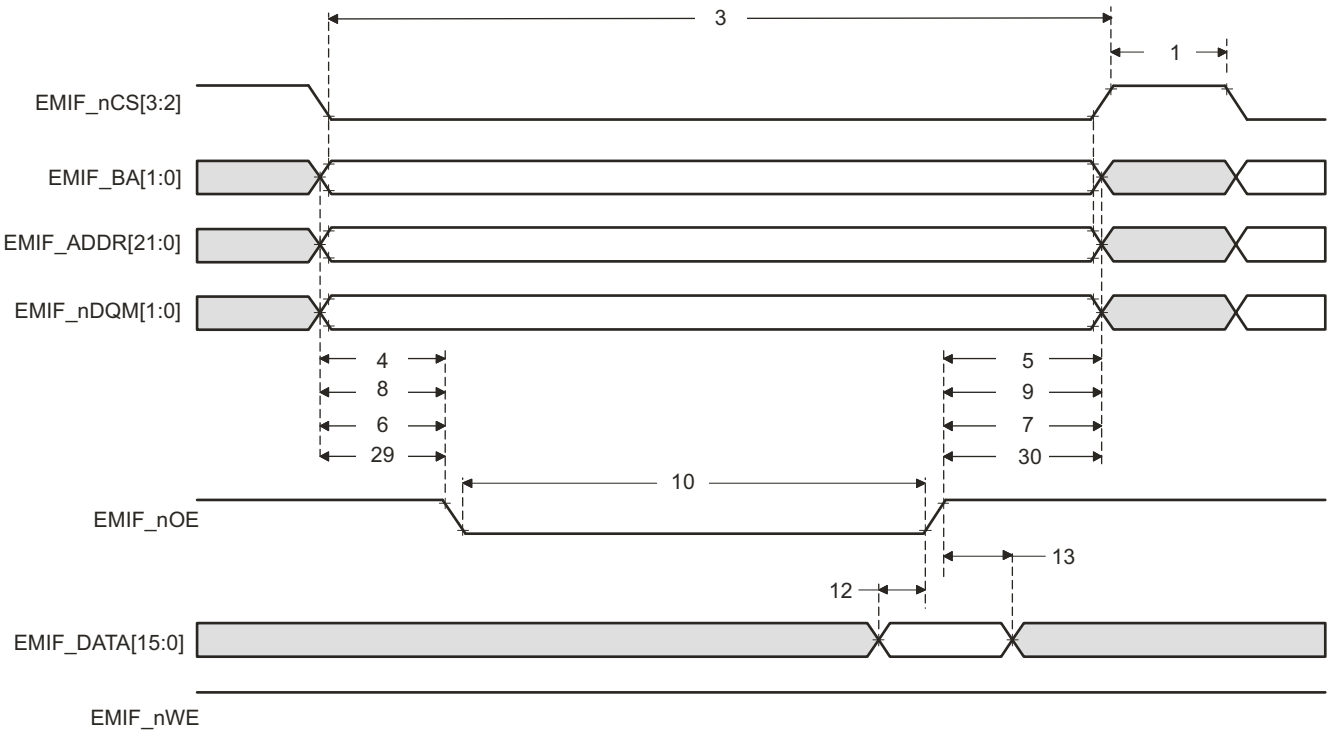


**Figure 6-11. Asynchronous Memory Read Timing**


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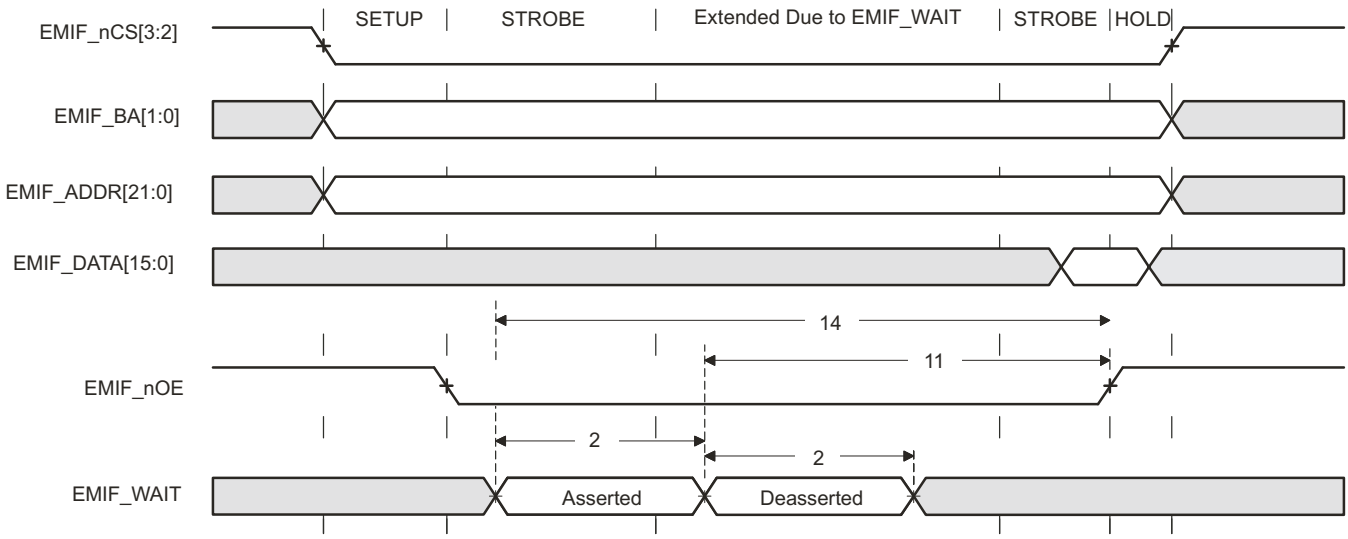


**Figure 6-12. EMIFnWAIT Read Timing Requirements**

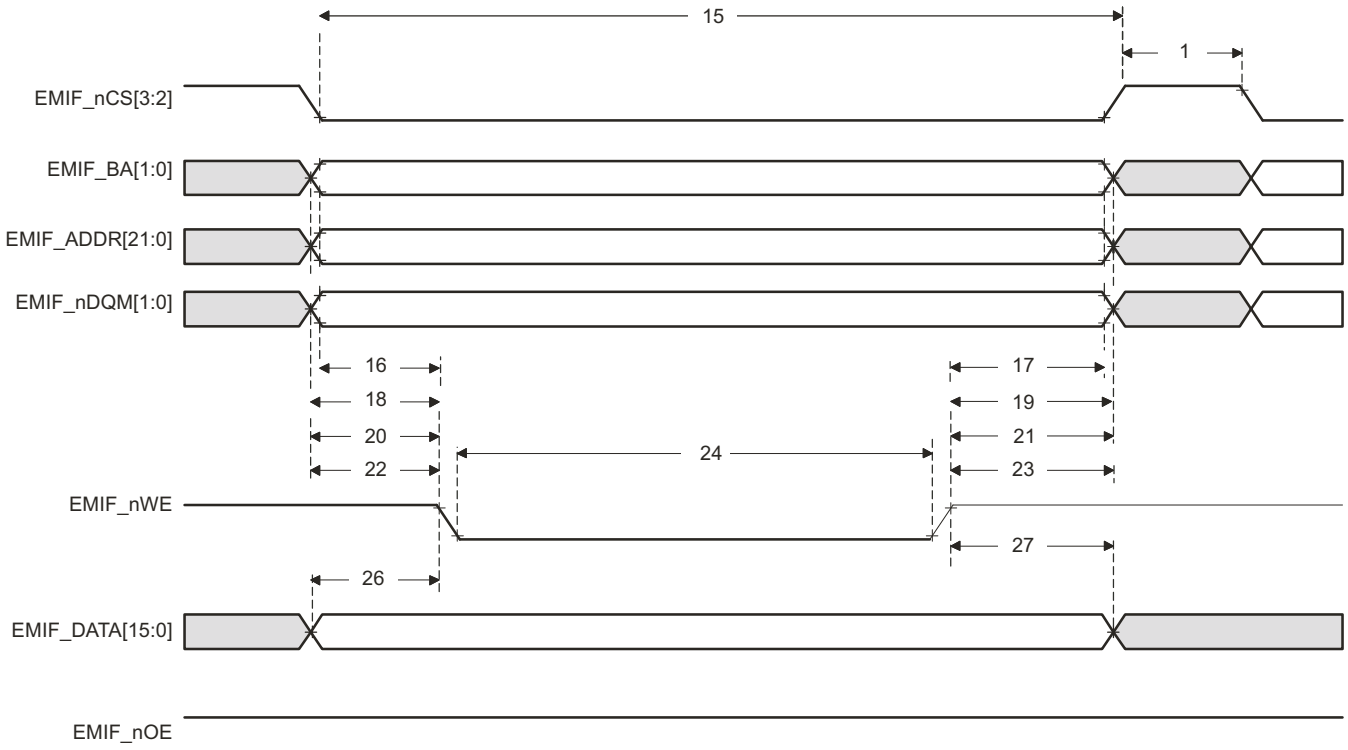


**Figure 6-13. Asynchronous Memory Write Timing**

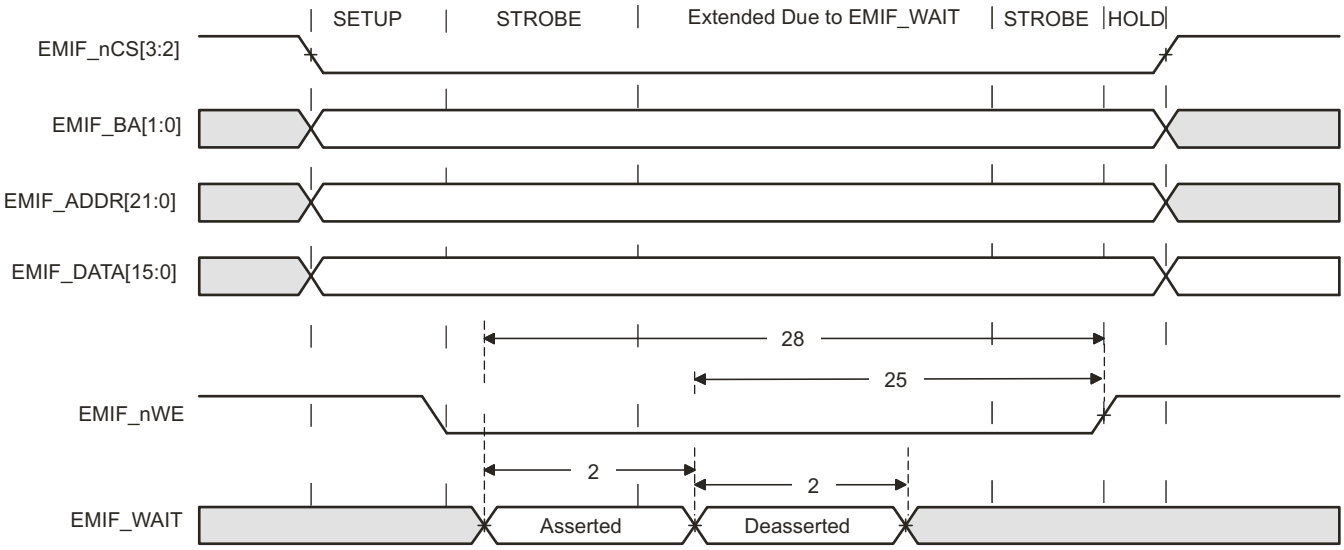


**Figure 6-14. EMIFnWAIT Write Timing Requirements**

**Table 6-27. EMIF Asynchronous Memory Timing Requirements**

| NO. | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Reads and Writes** | | | | | | |
| | E | EMIF clock period | 11 | | | ns |
| 2 | $t_{w(EM_WAIT)}$ | Pulse duration, EMIFnWAIT assertion and deassertion | 2E | | | ns |
| **Reads** | | | | | | |
| 12 | $t_{su(EMDV-EMOEH)}$ | Setup time, EMIFDATA[15:0] valid before EMIFnOE high | 30 | | | ns |
| 13 | $t_{h(EMOEH-EMDIV)}$ | Hold time, EMIFDATA[15:0] valid after EMIFnOE high | 0.5 | | | ns |
| 14 | $t_{su(EMOEL-EMWAIT)}$ | Setup Time, EMIFnWAIT asserted before end of Strobe Phase (1) | 4E+30 | | | ns |
| **Writes** | | | | | | |
| 28 | $t_{su(EMWEL-EMWAIT)}$ | Setup Time, EMIFnWAIT asserted before end of Strobe Phase (1) | 4E+30 | | | ns |

(1) Setup before end of STROBE phase (if no extended wait states are inserted) by which EMIFnWAIT must be asserted to add extended wait states. Figure Figure 6-12 and Figure Figure 6-14 describe EMIF transactions that include extended wait states inserted during the STROBE phase. However, cycles inserted as part of this extended wait period should not be counted; the 4E requirement is to the start of where the HOLD phase would begin if there were no extended wait cycles.

**Table 6-28. EMIF Asynchronous Memory Switching Characteristics (1) (2) (3)**

| NO. | PARAMETER | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Reads and Writes** | | | | | | |
| 1 | $t_{d(TURNAROUND)}$ | Turn around time | (TA)*E - 4 | (TA)*E | (TA)*E + 3 | ns |
| **Reads** | | | | | | |

(1) TA = Turn around, RS = Read setup, RST = Read strobe, RH = Read hold, WS = Write setup, WST = Write strobe, WH = Write hold, MEWC = Maximum external wait cycles. These parameters are programmed via the Asynchronous Bank and Asynchronous Wait Cycle Configuration Registers. These support the following ranges of values: TA[4–1], RS[16–1], RST[64–1], RH[8–1], WS[16–1], WST[64–1], WH[8–1], and MEWC[1–256]. See the TMS570LS31X/21X Technical Reference Manual (SPNU499) for more information.
(2) E = EMIF_CLK period in ns.
(3) EWC = external wait cycles determined by EMIFnWAIT input signal. EWC supports the following range of values. EWC[256–1]. Note that the maximum wait time before time-out is specified by bit field MEWC in the Asynchronous Wait Cycle Configuration Register. See the TMS570LS31X/21X Technical Reference Manual (SPNU499) for more information.


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### Table 6-28. EMIF Asynchronous Memory Switching Characteristics[(1)(2)(3)] (continued)

| NO. | PARAMETER | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| 3 | $t_{c(EMRCYCLE)}$ | EMIF read cycle time (EW = 0) | (RS+RST+RH)*E -3 | (RS+RST+RH)*E | (RS+RST+RH)*E + 3 | ns |
| | | EMIF read cycle time (EW = 1) | (RS+RST+RH+(EWC*16))*E -3 | (RS+RST+RH+(EWC*16))*E | (RS+RST+RH+(EWC*16))*E + 3 | ns |
| 4 | $t_{su(EMCEL-EMOEL)}$ | Output setup time, EMIFnCS[4:2] low to EMIFnOE low (SS = 0) | (RS)*E-4 | (RS)*E | (RS)*E+3 | ns |
| | | Output setup time, EMIFnCS[4:2] low to EMIFnOE low (SS = 1) | -3 | 0 | +3 | ns |
| 5 | $t_{h(EMOEH-EMCEH)}$ | Output hold time, EMIFnOE high to EMIFnCS[4:2] high (SS = 0) | (RH)*E -4 | (RH)*E | (RH)*E + 3 | ns |
| | | Output hold time, EMIFnOE high to EMIFnCS[4:2] high (SS = 1) | -3 | 0 | +3 | ns |
| 6 | $t_{su(EMBAV-EMOEL)}$ | Output setup time, EMIFBA[1:0] valid to EMIFnOE low | (RS)*E-4 | (RS)*E | (RS)*E+3 | ns |
| 7 | $t_{h(EMOEH-EMBAIV)}$ | Output hold time, EMIFnOE high to EMIFBA[1:0] invalid | (RH)*E-4 | (RH)*E | (RH)*E+3 | ns |
| 8 | $t_{su(EMAV-EMOEL)}$ | Output setup time, EMIFADDR[21:0] valid to EMIFnOE low | (RS)*E-4 | (RS)*E | (RS)*E+3 | ns |
| 9 | $t_{h(EMOEH-EMAIV)}$ | Output hold time, EMIFnOE high to EMIFADDR[21:0] invalid | (RH)*E-4 | (RH)*E | (RH)*E+3 | ns |
| 10 | $t_{w(EMOEL)}$ | EMIFnOE active low width (EW = 0) | (RST)*E-3 | (RST)*E | (RST)*E+3 | ns |
| | | EMIFnOE active low width (EW = 1) | (RST+(EWC*16)) *E-3 | (RST+(EWC*16))*E | (RST+(EWC*16)) *E+3 | ns |
| 11 | $t_{d(EMWAITH-EMOEH)}$ | Delay time from EMIFnWAIT deasserted to EMIFnOE high | 3E-3 | 4E | 4E+30 | ns |
| 29 | $t_{su(EMDQMV-EMOEL)}$ | Output setup time, EMIFnDQM[1:0] valid to EMIFnOE low | (RS)*E-4 | (RS)*E | (RS)*E+3 | ns |
| 30 | $t_{h(EMOEH-EMDQMIV)}$ | Output hold time, EMIFnOE high to EMIFnDQM[1:0] invalid | (RH)*E-4 | (RH)*E | (RH)*E+3 | ns |
| **Writes** | | | | | | |
| 15 | $t_{c(EMWCYCLE)}$ | EMIF write cycle time (EW = 0) | (WS+WST+WH) * E-3 | (WS+WST+WH) *E | (WS+WST+WH) * E+3 | ns |
| | | EMIF write cycle time (EW = 1) | (WS+WST+WH +( EWC*16))*E -3 | (WS+WST+WH +(E WC*16))*E | (WS+WST+WH +( EWC*16))*E + 3 | ns |
| 16 | $t_{su(EMCEL-EMWEL)}$ | Output setup time, EMIFnCS[4:2] low to EMIFnWE low (SS = 0) | (WS)*E -4 | (WS)*E | (WS)*E + 3 | ns |
| | | Output setup time, EMIFnCS[4:2] low to EMIFnWE low (SS = 1) | -4 | 0 | +3 | ns |
| 17 | $t_{h(EMWEH-EMCEH)}$ | Output hold time, EMIFnWE high to EMIFnCS[4:2] high (SS = 0) | (WH)*E-4 | (WH)*E | (WH)*E+3 | ns |
| | | Output hold time, EMIFnWE high to EMIFCS[4:2] high (SS = 1) | -4 | 0 | +3 | ns |
| 18 | $t_{su(EMDQMV-EMWEL)}$ | Output setup time, EMIFBA[1:0] valid to EMIFnWE low | (WS)*E-4 | (WS)*E | (WS)*E+3 | ns |
| 19 | $t_{h(EMWEH-EMDQMIV)}$ | Output hold time, EMIFnWE high to EMIFBA[1:0] invalid | (WH)*E-4 | (WH)*E | (WH)*E+3 | ns |
| 20 | $t_{su(EMBAV-EMWEL)}$ | Output setup time, EMIFBA[1:0] valid to EMIFnWE low | (WS)*E-4 | (WS)*E | (WS)*E+3 | ns |
| 21 | $t_{h(EMWEH-EMBAIV)}$ | Output hold time, EMIFnWE high to EMIFBA[1:0] invalid | (WH)*E-4 | (WH)*E | (WH)*E+3 | ns |
| 22 | $t_{su(EMAV-EMWEL)}$ | Output setup time, EMIFADDR[21:0] valid to EMIFnWE low | (WS)*E-4 | (WS)*E | (WS)*E+3 | ns |

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**Table 6-28. EMIF Asynchronous Memory Switching Characteristics[(1)(2)(3)] (continued)**

| NO. | PARAMETER | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| 23 | $t_{h(EMWEH-EMAIV)}$ | Output hold time, EMIFnWE high to EMIFADDR[21:0] invalid | (WH)*E-4 | (WH)*E | (WH)*E+3 | ns |
| 24 | $t_{w(EMWEL)}$ | EMIFnWE active low width (EW = 0) | (WST)*E-3 | (WST)*E | (WST)*E+3 | ns |
| | | EMIFnWE active low width (EW = 1) | (WST+(EWC*16 )) *E-3 | (WST+(EWC*16 ))*E | (WST+(EWC*16 )) *E+3 | ns |
| 25 | $t_{d(EMWAITH-EMWEH)}$ | Delay time from EMIFnWAIT deasserted to EMIFnWE high | 3E-4 | 4E | 4E+30 | ns |
| 26 | $t_{su(EMDV-EMWEL)}$ | Output setup time, EMIFDATA[15:0] valid to EMIFnWE low | (WS)*E-4 | (WS)*E | (WS)*E+3 | ns |
| 27 | $t_{h(EMWEH-EMDIV)}$ | Output hold time, EMIFnWE high to EMIFDATA[15:0] invalid | (WH)*E-4 | (WH)*E | (WH)*E+3 | ns |
| 31 | $t_{su(EMDQMV-EMWEL)}$ | Output setup time, EMIFnDQM[1:0] valid to EMIFnWE low | (WH)*E-4 | (WH)*E | (WH)*E+3 | ns |
| 32 | $t_{h(EMWEH-EMDQMIV)}$ | Output hold time, EMIFnWE high to EMIFnDQM[1:0] invalid | (WH)*E-4 | (WH)*E | (WH)*E+3 | ns |

### 6.14.2.2 Synchronous Timing

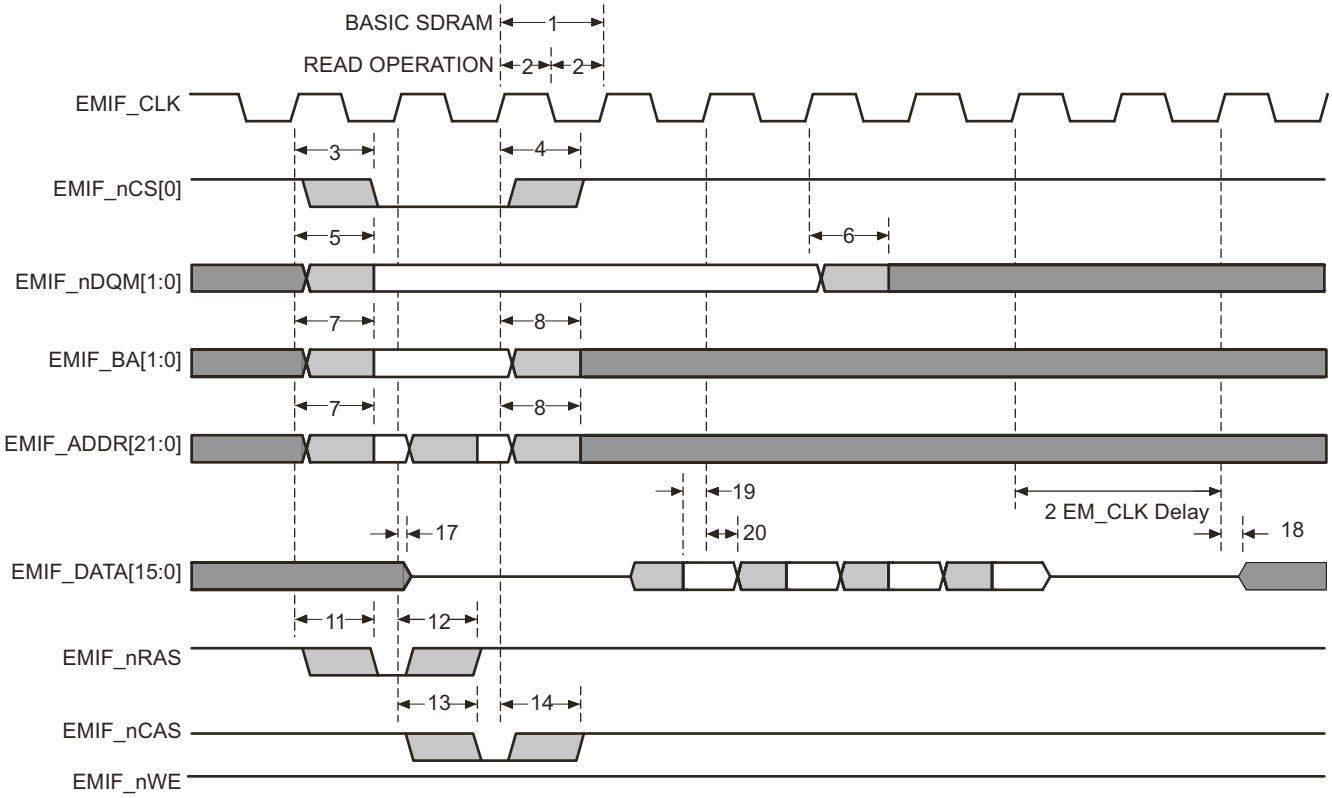


**Figure 6-15. Basic SDRAM Read Operation**


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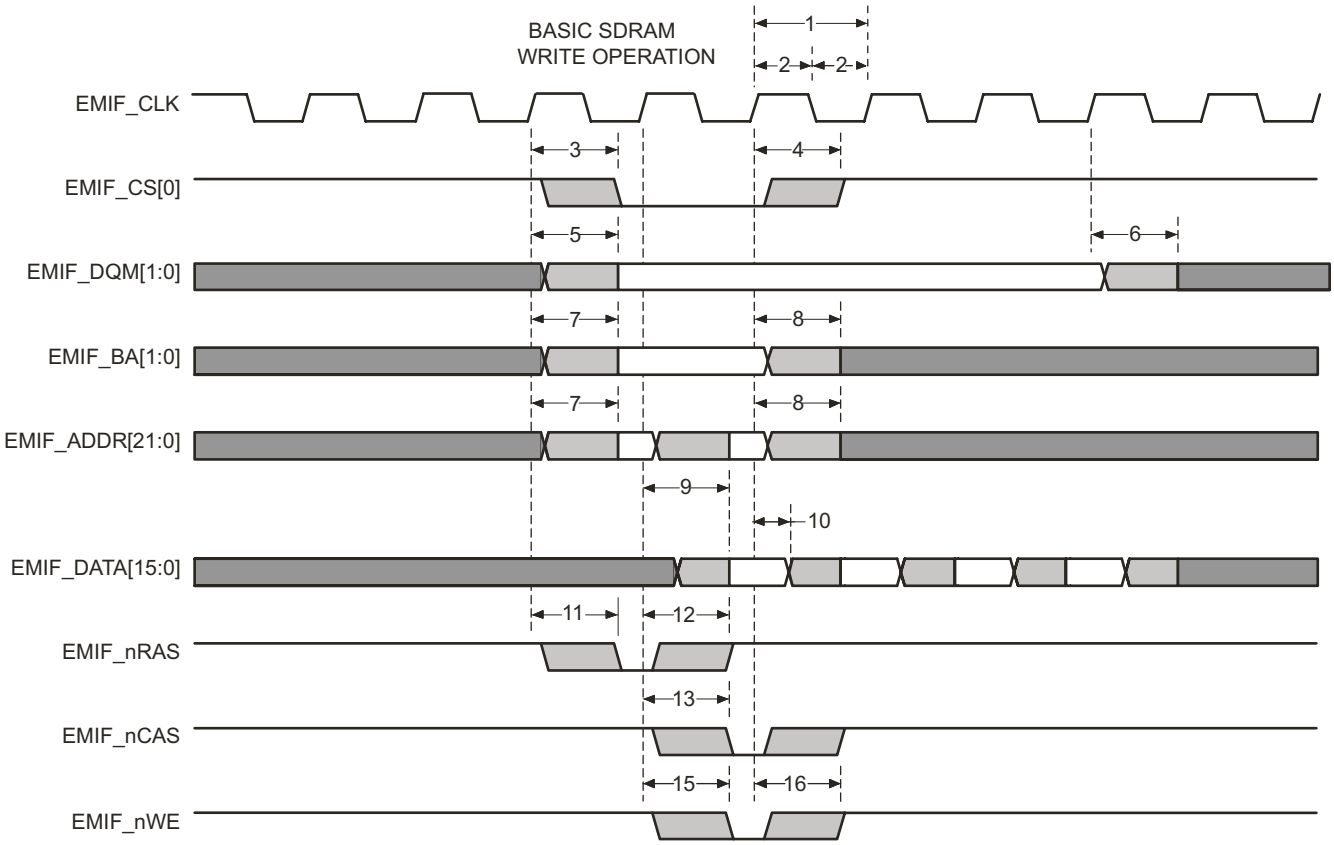


**Figure 6-16. Basic SDRAM Write Operation**

**Table 6-29. EMIF Synchronous Memory Timing Requirements**

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 19 | $t_{su(EMIFDV-EM_CLKH)}$ | Input setup time, read data valid on EMIFDATA[15:0] before EMIF_CLK rising | 2 | | ns |
| 20 | $t_{h(CLKH-DIV)}$ | Input hold time, read data valid on EMIFDATA[15:0] after EMIF_CLK rising | 1.5 | | ns |

**Table 6-30. EMIF Synchronous Memory Switching Characteristics**

| NO. | PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{c(CLK)}$ | Cycle time, EMIF clock EMIF_CLK | 20 | | ns |
| 2 | $t_{w(CLK)}$ | Pulse width, EMIF clock EMIF_CLK high or low | 5 | | ns |
| 3 | $t_{d(CLKH-CSV)}$ | Delay time, EMIF_CLK rising to EMIFnCS[0] valid | | 13 | ns |
| 4 | $t_{oh(CLKH-CSIV)}$ | Output hold time, EMIF_CLK rising to EMIFnCS[0] invalid | 1 | | ns |
| 5 | $t_{d(CLKH-DQMV)}$ | Delay time, EMIF_CLK rising to EMIFnDQM[1:0] valid | | 13 | ns |
| 6 | $t_{oh(CLKH-DQMIV)}$ | Output hold time, EMIF_CLK rising to EMIFnDQM[1:0] invalid | 1 | | ns |
| 7 | $t_{d(CLKH-AV)}$ | Delay time, EMIF_CLK rising to EMIFADDR[21:0] and EMIFBA[1:0] valid | | 13 | ns |
| 8 | $t_{oh(CLKH-AIV)}$ | Output hold time, EMIF_CLK rising to EMIFADDR[21:0] and EMIFBA[1:0] invalid | 1 | | ns |
| 9 | $t_{d(CLKH-DV)}$ | Delay time, EMIF_CLK rising to EMIFDATA[15:0] valid | | 13 | ns |

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**Table 6-30. EMIF Synchronous Memory Switching Characteristics (continued)**

| NO. | PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 10 | $t_{oh(CLKH-DIV)}$ | Output hold time, EMIF_CLK rising to EMIFDATA[15:0] invalid | 1 | | ns |
| 11 | $t_{d(CLKH-RASV)}$ | Delay time, EMIF_CLK rising to EMIFnRAS valid | | 13 | ns |
| 12 | $t_{oh(CLKH-RASIV)}$ | Output hold time, EMIF_CLK rising to EMIFnRAS invalid | 1 | | ns |
| 13 | $t_{d(CLKH-CASV)}$ | Delay time, EMIF_CLK rising to EMIFnCAS valid | | 13 | ns |
| 14 | $t_{oh(CLKH-CASIV)}$ | Output hold time, EMIF_CLK rising to EMIFnCAS invalid | 1 | | ns |
| 15 | $t_{d(CLKH-WEV)}$ | Delay time, EMIF_CLK rising to EMIFnWE valid | | 13 | ns |
| 16 | $t_{oh(CLKH-WEIV)}$ | Output hold time, EMIF_CLK rising to EMIFnWE invalid | 1 | | ns |
| 17 | $t_{dis(CLKH-DHZ)}$ | Delay time, EMIF_CLK rising to EMIFDATA[15:0] tri-stated | | 7 | ns |
| 18 | $t_{ena(CLKH-DLZ)}$ | Output hold time, EMIF_CLK rising to EMIFDATA[15:0] driving | 1 | | ns |


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## 6.15 Vectored Interrupt Manager

The vectored interrupt manager (VIM) provides hardware assistance for prioritizing and controlling the many interrupt sources present on this device. Interrupts are caused by events outside of the normal flow of program execution. Normally, these events require a timely response from the central processing unit (CPU); therefore, when an interrupt occurs, the CPU switches execution from the normal program flow to an interrupt service routine (ISR).

### *6.15.1 VIM Features*

The VIM module has the following features:

- Supports 96 interrupt channels.
  - Provides programmable priority and enable for interrupt request lines.
- Provides a direct hardware dispatch mechanism for fastest IRQ dispatch.
- Provides two software dispatch mechanisms when the CPU VIC port is not used.
  - Index interrupt
  - Register vectored interrupt
- Parity protected vector interrupt table

### *6.15.2 Interrupt Request Assignments*

**Table 6-31. Interrupt Request Assignments**

| MODULES | INTERRUPT SOURCES | DEFAULT VIM INTERRUPT CHANNEL |
|---|---|---|
| ESM | ESM High level interrupt (NMI) | 0 |
| Reserved | Reserved | 1 |
| RTI | RTI compare interrupt 0 | 2 |
| RTI | RTI compare interrupt 1 | 3 |
| RTI | RTI compare interrupt 2 | 4 |
| RTI | RTI compare interrupt 3 | 5 |
| RTI | RTI overflow interrupt 0 | 6 |
| RTI | RTI overflow interrupt 1 | 7 |
| RTI | RTI timebase interrupt | 8 |
| GPIO | GPIO interrupt A | 9 |
| N2HET1 | N2HET1 level 0 interrupt | 10 |
| HTU1 | HTU1 level 0 interrupt | 11 |
| MIBSPI1 | MIBSPI1 level 0 interrupt | 12 |
| LIN | LIN level 0 interrupt | 13 |
| MIBADC1 | MIBADC1 event group interrupt | 14 |
| MIBADC1 | MIBADC1 sw group 1 interrupt | 15 |
| DCAN1 | DCAN1 level 0 interrupt | 16 |
| SPI2 | SPI2 level 0 interrupt | 17 |
| FlexRay | FlexRay level 0 interrupt | 18 |
| CRC | CRC Interrupt | 19 |
| ESM | ESM Low level interrupt | 20 |
| SYSTEM | Software interrupt (SSI) | 21 |
| CPU | PMU Interrupt | 22 |
| GPIO | GPIO interrupt B | 23 |
| N2HET1 | N2HET1 level 1 interrupt | 24 |
| HTU1 | HTU1 level 1 interrupt | 25 |

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**Table 6-31. Interrupt Request Assignments (continued)**

| MODULES | INTERRUPT SOURCES | DEFAULT VIM INTERRUPT CHANNEL |
|---|---|---|
| MIBSPI1 | MIBSPI1 level 1 interrupt | 26 |
| LIN | LIN level 1 interrupt | 27 |
| MIBADC1 | MIBADC1 sw group 2 interrupt | 28 |
| DCAN1 | DCAN1 level 1 interrupt | 29 |
| SPI2 | SPI2 level 1 interrupt | 30 |
| MIBADC1 | MIBADC1 magnitude compare interrupt | 31 |
| FlexRay | FlexRay level 1 interrupt | 32 |
| DMA | FTCA interrupt | 33 |
| DMA | LFSA interrupt | 34 |
| DCAN2 | DCAN2 level 0 interrupt | 35 |
| DMM | DMM level 0 interrupt | 36 |
| MIBSPI3 | MIBSPI3 level 0 interrupt | 37 |
| MIBSPI3 | MIBSPI3 level 1 interrupt | 38 |
| DMA | HBCA interrupt | 39 |
| DMA | BTCA interrupt | 40 |
| EMIF | AEMIFINT3 | 41 |
| DCAN2 | DCAN2 level 1 interrupt | 42 |
| DMM | DMM level 1 interrupt | 43 |
| DCAN1 | DCAN1 IF3 interrupt | 44 |
| DCAN3 | DCAN3 level 0 interrupt | 45 |
| DCAN2 | DCAN2 IF3 interrupt | 46 |
| FPU | "OR" of the six Cortex R4F FPU Exceptions | 47 |
| FTU | FTU Transfer Status interrupt | 48 |
| SPI4 | SPI4 level 0 interrupt | 49 |
| MIBADC2 | MibADC2 event group interrupt | 50 |
| MIBADC2 | MibADC2 sw group1 interrupt | 51 |
| FlexRay | FlexRay T0C interrupt | 52 |
| MIBSPI5 | MIBSPI5 level 0 interrupt | 53 |
| SPI4 | SPI4 level 1 interrupt | 54 |
| DCAN3 | DCAN3 level 1 interrupt | 55 |
| MIBSPI5 | MIBSPI5 level 1 interrupt | 56 |
| MIBADC2 | MibADC2 sw group2 interrupt | 57 |
| FTU | FTU Error interrupt | 58 |
| MIBADC2 | MibADC2 magnitude compare interrupt | 59 |
| DCAN3 | DCAN3 IF3 interrupt | 60 |
| FMC | FSM_DONE interrupt | 61 |
| FlexRay | FlexRay T1C interrupt | 62 |
| N2HET2 | N2HET2 level 0 interrupt | 63 |
| SCI | SCI level 0 interrupt | 64 |
| HTU2 | HTU2 level 0 interrupt | 65 |
| I2C | I2C level 0 interrupt | 66 |
| Reserved | Reserved | 67-72 |
| N2HET2 | N2HET2 level 1 interrupt | 73 |
| SCI | SCI level 1 interrupt | 74 |
| HTU2 | HTU2 level 1 interrupt | 75 |
| Ethernet | C0_MISC_PULSE | 76 |
| Ethernet | C0_TX_PULSE | 77 |


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**Table 6-31. Interrupt Request Assignments (continued)**

| MODULES | INTERRUPT SOURCES | DEFAULT VIM INTERRUPT CHANNEL |
|---|---|---|
| Ethernet | C0_THRESH_PULSE | 78 |
| Ethernet | C0_RX_PULSE | 79 |
| HWAG1 | HWA_INT_REQ_H | 80 |
| HWAG2 | HWA_INT_REQ_H | 81 |
| DCC1 | DCC1 done interrupt | 82 |
| DCC2 | DCC2 done interrupt | 83 |
| Reserved | Reserved | 84 |
| PBIST | PBIST_DONE | 85 |
| Reserved | Reserved | 86 |
| Reserved | Reserved | 87 |
| HWAG1 | HWA_INT_REQ_L | 88 |
| HWAG2 | HWA_INT_REQ_L | 89 |
| Reserved | Reserved | 90-95 |

**NOTE**

Address location 0x00000000 in the VIM RAM is reserved for the phantom interrupt ISR entry; therefore only request channels 0..94 can be used and are offset by 1 address in the VIM RAM.

**NOTE**

The EMIF_nWAIT signal has a pullup on it. The EMIF module generates a "Wait Rise" interrupt whenever it detects a rising edge on the EMIF_nWAIT signal. This interrupt condition is indicated as soon as the device is powered up. This can be ignored if the EMIF_nWAIT signal is not used in the application. If the EMIF_nWAIT signal is actually used in the application, then the external slave memory must always drive the EMIF_nWAIT signal such that an interrupt is not caused due to the default pullup on this signal.

**NOTE**

The lower-order interrupt channels are higher priority channels than the higher-order interrupt channels.

**NOTE**

The application can change the mapping of interrupt sources to the interrupt channels via the interrupt channel control registers (CHANCTRLx) inside the VIM module.

## 6.16 DMA Controller

The DMA controller is used to transfer data between two locations in the memory map in the background of CPU operations. Typically, the DMA is used to:

- Transfer blocks of data between external and internal data memories
- Restructure portions of internal data memory
- Continually service a peripheral

### *6.16.1 DMA Features*

- CPU independent data transfer
- One master port - PortB (64 bits wide) that interfaces to the TMS570 Memory System.
- FIFO buffer(4 entries deep and each 64 bits wide)
- Channel control information is stored in RAM protected by parity
- 16 channels with individual enable
- Channel chaining capability
- 32 peripheral DMA requests
- Hardware and Software DMA requests
- 8-, 16-, 32-, or 64-bit transactions supported
- Multiple addressing modes for source/destination (fixed, increment, offset)
- Auto-initiation
- Power-management mode
- Memory Protection with four configurable memory regions


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### 6.16.2 Default DMA Request Map

The DMA module on this microcontroller has 16 channels and up to 32 hardware DMA requests. The module contains DREQASIx registers which are used to map the DMA requests to the DMA channels. By default, channel 0 is mapped to request 0, channel 1 to request 1, and so on.

Some DMA requests have multiple sources, as shown in Table 6-32. The application must ensure that only one of these DMA request sources is enabled at any time.

**Table 6-32. DMA Request Line Connection**

| Modules | DMA Request Sources | DMA Request |
|---|---|---|
| MIBSPI1 | MIBSPI1[1] (1) | DMAREQ[0] |
| MIBSPI1 | MIBSPI1[0] (2) | DMAREQ[1] |
| SPI2 | SPI2 receive | DMAREQ[2] |
| SPI2 | SPI2 transmit | DMAREQ[3] |
| MIBSPI1 / MIBSPI3 / DCAN2 | MIBSPI1[2] / MIBSPI3[2] / DCAN2 IF3 | DMAREQ[4] |
| MIBSPI1 / MIBSPI3 / DCAN2 | MIBSPI1[3] / MIBSPI3[3] / DCAN2 IF2 | DMAREQ[5] |
| DCAN1 / MIBSPI5 | DCAN1 IF2 / MIBSPI5[2] | DMAREQ[6] |
| MIBADC1 / MIBSPI5 | MIBADC1 event / MIBSPI5[3] | DMAREQ[7] |
| MIBSPI1 / MIBSPI3 / DCAN1 | MIBSPI1[4] / MIBSPI3[4] / DCAN1 IF1 | DMAREQ[8] |
| MIBSPI1 / MIBSPI3 / DCAN2 | MIBSPI1[5] / MIBSPI3[5] / DCAN2 IF1 | DMAREQ[9] |
| MIBADC1 / I2C / MIBSPI5 | MIBADC1 G1 / I2C receive / MIBSPI5[4] | DMAREQ[10] |
| MIBADC1 / I2C / MIBSPI5 | MIBADC1 G2 / I2C transmit / MIBSPI5[5] | DMAREQ[11] |
| RTI / MIBSPI1 / MIBSPI3 | RTI DMAREQ0 / MIBSPI1[6] / MIBSPI3[6] | DMAREQ[12] |
| RTI / MIBSPI1 / MIBSPI3 | RTI DMAREQ1 / MIBSPI1[7] / MIBSPI3[7] | DMAREQ[13] |
| MIBSPI3 / MibADC2 / MIBSPI5 | MIBSPI3[1] (1) / MibADC2 event / MIBSPI5[6] | DMAREQ[14] |
| MIBSPI3 / MIBSPI5 | MIBSPI3[0] (2) / MIBSPI5[7] | DMAREQ[15] |
| MIBSPI1 / MIBSPI3 / DCAN1 / MibADC2 | MIBSPI1[8] / MIBSPI3[8] / DCAN1 IF3 / MibADC2 G1 | DMAREQ[16] |
| MIBSPI1 / MIBSPI3 / DCAN3 / MibADC2 | MIBSPI1[9] / MIBSPI3[9] / DCAN3 IF1 / MibADC2 G2 | DMAREQ[17] |
| RTI / MIBSPI5 | RTI DMAREQ2 / MIBSPI5[8] | DMAREQ[18] |
| RTI / MIBSPI5 | RTI DMAREQ3 / MIBSPI5[9] | DMAREQ[19] |
| N2HET1 / N2HET2 / DCAN3 | N2HET1 DMAREQ[4] / N2HET2 DMAREQ[4] / DCAN3 IF2 | DMAREQ[20] |
| N2HET1 / N2HET2 / DCAN3 | N2HET1 DMAREQ[5] / N2HET2 DMAREQ[5] / DCAN3 IF3 | DMAREQ[21] |
| MIBSPI1 / MIBSPI3 / MIBSPI5 | MIBSPI1[10] / MIBSPI3[10] / MIBSPI5[10] | DMAREQ[22] |
| MIBSPI1 / MIBSPI3 / MIBSPI5 | MIBSPI1[11] / MIBSPI3[11] / MIBSPI5[11] | DMAREQ[23] |
| N2HET1 / N2HET2 / SPI4 / MIBSPI5 | N2HET1 DMAREQ[6] / N2HET2 DMAREQ[6] / SPI4 receive / MIBSPI5[12] | DMAREQ[24] |
| N2HET1 / N2HET2 / SPI4 / MIBSPI5 | N2HET1 DMAREQ[7] / N2HET2 DMAREQ[7] / SPI4 transmit / MIBSPI5[13] | DMAREQ[25] |
| CRC / MIBSPI1 / MIBSPI3 | CRC DMAREQ[0] / MIBSPI1[12] / MIBSPI3[12] | DMAREQ[26] |
| CRC / MIBSPI1 / MIBSPI3 | CRC DMAREQ[1] / MIBSPI1[13] / MIBSPI3[13] | DMAREQ[27] |
| LIN / MIBSPI5 | LIN receive / MIBSPI5[14] | DMAREQ[28] |
| LIN / MIBSPI5 | LIN transmit / MIBSPI5[15] | DMAREQ[29] |
| MIBSPI1 / MIBSPI3 / SCI / MIBSPI5 | MIBSPI1[14] / MIBSPI3[14] / SCI receive / MIBSPI5[1] (1) | DMAREQ[30] |
| MIBSPI1 / MIBSPI3 / SCI / MIBSPI5 | MIBSPI1[15] / MIBSPI3[15] / SCI transmit / MIBSPI5[0] (2) | DMAREQ[31] |

(1) SPI1, SPI3, SPI5 receive in standard SPI mode
(2) SPI1, SPI3, SPI5 transmit in standard SPI mode

## 6.17 Real Time Interrupt Module

The real-time interrupt (RTI) module provides timer functionality for operating systems and for benchmarking code. The RTI module can incorporate several counters that define the timebases needed for scheduling an operating system.

The timers also allow you to benchmark certain areas of code by reading the values of the counters at the beginning and the end of the desired code range and calculating the difference between the values.

In addition the RTI provides a mechanism to synchronize the operating system to the FlexRay communication cycle. Clock supervision can detect issues on the FlexRay bus with an automatic switch to an internally generated timebase.

### *6.17.1 Features*

The RTI module has the following features:

- Two independent 64 bit counter blocks
- Four configurable compares for generating operating system ticks or DMA requests. Each event can be driven by either counter block 0 or counter block 1.
- One counter block usable for application synchronization to FlexRay network including clock supervision
- Fast enabling/disabling of events
- Two time-stamp (capture) functions for system or peripheral interrupts, one for each counter block

### *6.17.2 Block Diagrams*

Figure 6-17 shows a high-level block diagram for one of the two 64-bit counter blocks inside the RTI module. Both the counter blocks are identical except the Network Time Unit (NTUx) inputs are only available as time base inputs for the counter block 0.

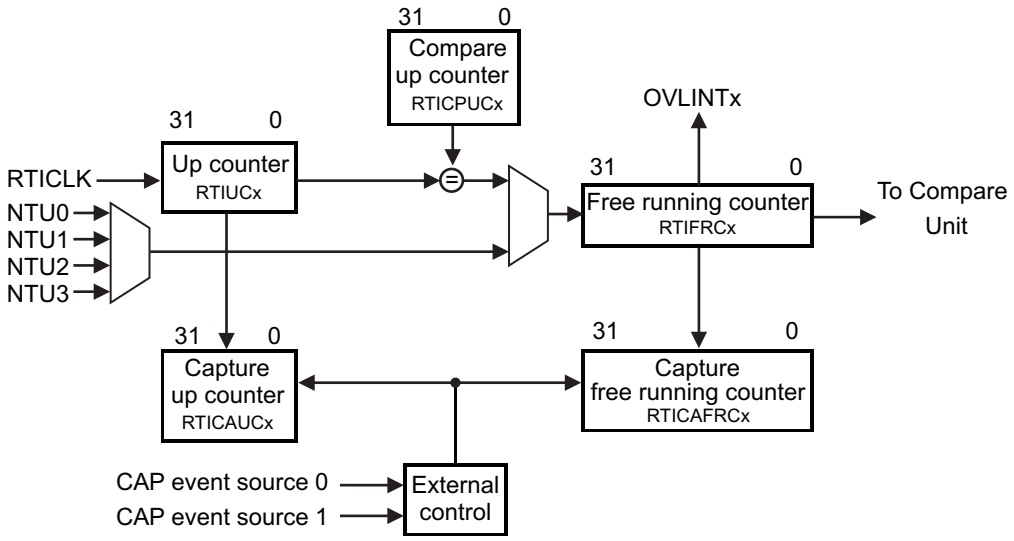


**Figure 6-17. Counter Block Diagram**


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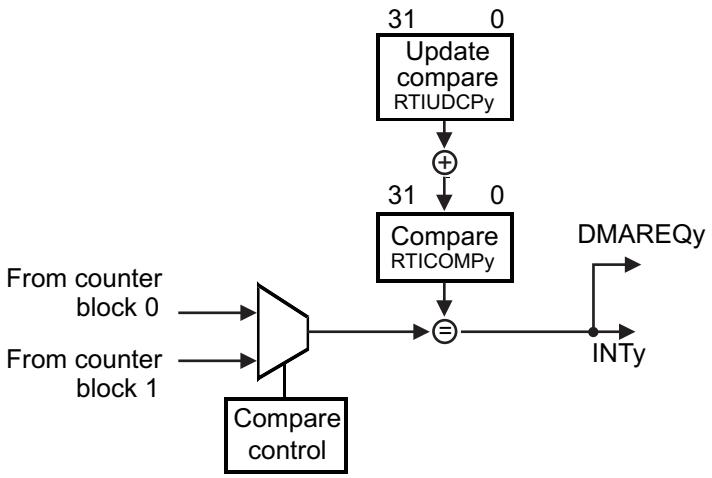


**Figure 6-18. Compare Block Diagram**

### 6.17.3 Clock Source Options

The RTI module uses the RTI1CLK clock domain for generating the RTI time bases.

The application can select the clock source for the RTI1CLK by configuring the RCLKSRC register in the System module at address 0xFFFFFF50. The default source for RTI1CLK is VCLK.

For more information on clock sources refer to Table 6-8 and Table 6-13.

### 6.17.4 Network Time Synchronization Inputs

The RTI module supports 4 Network Time Unit (NTU) inputs that signal internal system events, and which can be used to synchronize the time base used by the RTI module. On this device, these NTU inputs are connected as shown in Table 6-33.

**Table 6-33. Network Time Synchronization Inputs**

| NTU Input | Source |
|---|---|
| 0 | Macrotick |
| 1 | Start of Cycle |
| 2 | PLL2 Clock output |
| 3 | EXTCLKIN1 clock input |

## 6.18 Error Signaling Module

The Error Signaling Module (ESM) manages the various error conditions on the TMS570 microcontroller. The error condition is handled based on a fixed severity level assigned to it. Any severe error condition can be configured to drive a low level on a dedicated device terminal called nERROR. This can be used as an indicator to an external monitor circuit to put the system into a safe state.

### *6.18.1 Features*

The features of the Error Signaling Module are:

- 128 interrupt/error channels are supported, divided into 3 different groups
  - 64 channels with maskable interrupt and configurable error pin behavior
  - 32 error channels with nonmaskable interrupt and predefined error pin behavior
  - 32 channels with predefined error pin behavior only
- Error pin to signal severe device failure
- Configurable timebase for error signal
- Error forcing capability

### *6.18.2 ESM Channel Assignments*

The Error Signaling Module (ESM) integrates all the device error conditions and groups them in the order of severity. Group1 is used for errors of the lowest severity while Group3 is used for errors of the highest severity. The device response to each error is determined by the severity group it is connected to. Table 6-35 shows the channel assignment for each group.

**Table 6-34. ESM Groups**

| ERROR GROUP | INTERRUPT CHARACTERISTICS | INFLUENCE ON ERROR PIN |
|---|---|---|
| Group1 | maskable, low or high priority | configurable |
| Group2 | nonmaskable, high priority | fixed |
| Group3 | no interrupt generated | fixed |

**Table 6-35. ESM Channel Assignments**

| ERROR SOURCES | GROUP | CHANNELS |
|---|---|---|
| Reserved | Group1 | 0 |
| MibADC2 - parity | Group1 | 1 |
| DMA - MPU | Group1 | 2 |
| DMA - parity | Group1 | 3 |
| Reserved | Group1 | 4 |
| DMA/DMM - imprecise read error | Group1 | 5 |
| FMC - correctable error: bus1 and bus2 interfaces (does not include accesses to EEPROM bank) | Group1 | 6 |
| N2HET1/N2HET2 - parity | Group1 | 7 |
| HTU1/HTU2 - parity | Group1 | 8 |
| HTU1/HTU2 - MPU | Group1 | 9 |
| PLL - Slip | Group1 | 10 |
| Clock Monitor - interrupt | Group1 | 11 |
| FlexRay - parity | Group1 | 12 |
| DMA/DMM - imprecise write error | Group1 | 13 |
| FTU - parity | Group1 | 14 |
| VIM RAM - parity | Group1 | 15 |
| FTU - MPU | Group1 | 16 |
| MibSPI1 - parity | Group1 | 17 |
| MibSPI3 - parity | Group1 | 18 |


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**Table 6-35. ESM Channel Assignments (continued)**

| ERROR SOURCES | GROUP | CHANNELS |
|---|---|---|
| MibADC1 - parity | Group1 | 19 |
| Reserved | Group1 | 20 |
| DCAN1 - parity | Group1 | 21 |
| DCAN3 - parity | Group1 | 22 |
| DCAN2 - parity | Group1 | 23 |
| MibSPI5 - parity | Group1 | 24 |
| Reserved | Group1 | 25 |
| RAM even bank (B0TCM) - correctable error | Group1 | 26 |
| CPU - selftest | Group1 | 27 |
| RAM odd bank (B1TCM) - correctable error | Group1 | 28 |
| Reserved | Group1 | 29 |
| DCC1 - error | Group1 | 30 |
| CCM-R4 - selftest | Group1 | 31 |
| Reserved | Group1 | 32 |
| Reserved | Group1 | 33 |
| Reserved | Group1 | 34 |
| FMC - correctable error (EEPROM bank access) | Group1 | 35 |
| FMC - uncorrectable error (EEPROM bank access) | Group1 | 36 |
| IOMM - Mux configuration error | Group1 | 37 |
| Power domain controller compare error | Group1 | 38 |
| Power domain controller self-test error | Group1 | 39 |
| eFuse Controller Error – this error signal is generated when any bit in the eFuse controller error status register is set. The application can choose to generate an interrupt whenever this bit is set to service any eFuse controller error conditions. | Group1 | 40 |
| eFuse Controller - Self Test Error. This error signal is generated only when a self test on the eFuse controller generates an error condition. When an ECC self test error is detected, group 1 channel 40 error signal will also be set. | Group1 | 41 |
| PLL2 - Slip | Group1 | 42 |
| Ethernet Controller master interface | Group1 | 43 |
| Reserved | Group1 | 44 |
| Reserved | Group1 | 45 |
| Reserved | Group1 | 46 |
| Reserved | Group1 | 47 |
| Reserved | Group1 | 48 |
| Reserved | Group1 | 49 |
| Reserved | Group1 | 50 |
| Reserved | Group1 | 51 |
| Reserved | Group1 | 52 |
| Reserved | Group1 | 53 |
| Reserved | Group1 | 54 |
| Reserved | Group1 | 55 |
| Reserved | Group1 | 56 |
| Reserved | Group1 | 57 |
| Reserved | Group1 | 58 |
| Reserved | Group1 | 59 |
| Reserved | Group1 | 60 |
| Reserved | Group1 | 61 |
| DCC2 - error | Group1 | 62 |

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### Table 6-35. ESM Channel Assignments (continued)

| ERROR SOURCES | GROUP | CHANNELS |
|---|---|---|
| Reserved | Group1 | 63 |
| **GROUP 2** | | |
| Reserved | Group2 | 0 |
| Reserved | Group2 | 1 |
| CCMR4 - compare | Group2 | 2 |
| Reserved | Group2 | 3 |
| FMC - uncorrectable error (address parity on bus1 accesses) | Group2 | 4 |
| Reserved | Group2 | 5 |
| RAM even bank (B0TCM) - uncorrectable error | Group2 | 6 |
| Reserved | Group2 | 7 |
| RAM odd bank (B1TCM) - uncorrectable error | Group2 | 8 |
| Reserved | Group2 | 9 |
| RAM even bank (B0TCM) - address bus parity error | Group2 | 10 |
| Reserved | Group2 | 11 |
| RAM odd bank (B1TCM) - address bus parity error | Group2 | 12 |
| Reserved | Group2 | 13 |
| Reserved | Group2 | 14 |
| Reserved | Group2 | 15 |
| TCM - ECC live lock detect | Group2 | 16 |
| Reserved | Group2 | 17 |
| Reserved | Group2 | 18 |
| Reserved | Group2 | 19 |
| Reserved | Group2 | 20 |
| Reserved | Group2 | 21 |
| Reserved | Group2 | 22 |
| Reserved | Group2 | 23 |
| RTI_WWD_NMI | Group2 | 24 |
| Reserved | Group2 | 25 |
| Reserved | Group2 | 26 |
| Reserved | Group2 | 27 |
| Reserved | Group2 | 28 |
| Reserved | Group2 | 29 |
| Reserved | Group2 | 30 |
| Reserved | Group2 | 31 |
| **GROUP 3** | | |
| Reserved | Group3 | 0 |
| eFuse Controller - autoload error | Group3 | 1 |
| Reserved | Group3 | 2 |
| RAM even bank (B0TCM) - ECC uncorrectable error | Group3 | 3 |
| Reserved | Group3 | 4 |
| RAM odd bank (B1TCM) - ECC uncorrectable error | Group3 | 5 |
| Reserved | Group3 | 6 |
| FMC - uncorrectable error: bus1 and bus2 interfaces (does not include address parity error and errors on accesses to EEPROM bank) | Group3 | 7 |
| Reserved | Group3 | 8 |
| Reserved | Group3 | 9 |
| Reserved | Group3 | 10 |
| Reserved | Group3 | 11 |


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**Table 6-35. ESM Channel Assignments (continued)**

| ERROR SOURCES | GROUP | CHANNELS |
|---|---|---|
| Reserved | Group3 | 12 |
| Reserved | Group3 | 13 |
| Reserved | Group3 | 14 |
| Reserved | Group3 | 15 |
| Reserved | Group3 | 16 |
| Reserved | Group3 | 17 |
| Reserved | Group3 | 18 |
| Reserved | Group3 | 19 |
| Reserved | Group3 | 20 |
| Reserved | Group3 | 21 |
| Reserved | Group3 | 22 |
| Reserved | Group3 | 23 |
| Reserved | Group3 | 24 |
| Reserved | Group3 | 25 |
| Reserved | Group3 | 26 |
| Reserved | Group3 | 27 |
| Reserved | Group3 | 28 |
| Reserved | Group3 | 29 |
| Reserved | Group3 | 30 |
| Reserved | Group3 | 31 |

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## 6.19 Reset / Abort / Error Sources

**Table 6-36. Reset/Abort/Error Sources**

| ERROR SOURCE | SYSTEM MODE | ERROR RESPONSE | ESM HOOKUP group.channel |
|---|---|---|---|
| **CPU TRANSACTIONS** | | | |
| Precise write error (NCNB/Strongly Ordered) | User/Privilege | Precise Abort (CPU) | n/a |
| Precise read error (NCB/Device or Normal) | User/Privilege | Precise Abort (CPU) | n/a |
| Imprecise write error (NCB/Device or Normal) | User/Privilege | Imprecise Abort (CPU) | n/a |
| Illegal instruction | User/Privilege | Undefined Instruction Trap (CPU)(1) | n/a |
| MPU access violation | User/Privilege | Abort (CPU) | n/a |
| **SRAM** | | | |
| B0 TCM (even) ECC single error (correctable) | User/Privilege | ESM | 1.26 |
| B0 TCM (even) ECC double error (noncorrectable) | User/Privilege | Abort (CPU), ESM => nERROR | 3.3 |
| B0 TCM (even) uncorrectable error (for example, redundant address decode) | User/Privilege | ESM => NMI => nERROR | 2.6 |
| B0 TCM (even) address bus parity error | User/Privilege | ESM => NMI => nERROR | 2.10 |
| B1 TCM (odd) ECC single error (correctable) | User/Privilege | ESM | 1.28 |
| B1 TCM (odd) ECC double error (noncorrectable) | User/Privilege | Abort (CPU), ESM => nERROR | 3.5 |
| B1 TCM (odd) uncorrectable error (for example, redundant address decode) | User/Privilege | ESM => NMI => nERROR | 2.8 |
| B1 TCM (odd) address bus parity error | User/Privilege | ESM => NMI => nERROR | 2.12 |
| **FLASH** | | | |
| FMC correctable error - Bus1 and Bus2 interfaces (does not include accesses to EEPROM bank) | User/Privilege | ESM | 1.6 |
| FMC uncorrectable error - Bus1 accesses (does not include address parity error) | User/Privilege | Abort (CPU), ESM => nERROR | 3.7 |
| FMC uncorrectable error - Bus2 accesses (does not include address parity error and EEPROM bank accesses) | User/Privilege | ESM => nERROR | 3.7 |
| FMC uncorrectable error - address parity error on Bus1 accesses | User/Privilege | ESM => NMI => nERROR | 2.4 |
| FMC correctable error - Accesses to EEPROM bank | User/Privilege | ESM | 1.35 |
| FMC uncorrectable error - Accesses to EEPROM bank | User/Privilege | ESM | 1.36 |
| **DMA TRANSACTIONS** | | | |
| External imprecise error on read (Illegal transaction with ok response) | User/Privilege | ESM | 1.5 |
| External imprecise error on write (Illegal transaction with ok response) | User/Privilege | ESM | 1.13 |
| Memory access permission violation | User/Privilege | ESM | 1.2 |
| Memory parity error | User/Privilege | ESM | 1.3 |
| **DMM TRANSACTIONS** | | | |
| External imprecise error on read (Illegal transaction with ok response) | User/Privilege | ESM | 1.5 |
| External imprecise error on write (Illegal transaction with ok response) | User/Privilege | ESM | 1.13 |
| **HTU1** | | | |
| NCNB (Strongly Ordered) transaction with slave error response | User/Privilege | Interrupt => VIM | n/a |
| External imprecise error (Illegal transaction with ok response) | User/Privilege | Interrupt => VIM | n/a |
| Memory access permission violation | User/Privilege | ESM | 1.9 |

(1) The Undefined Instruction TRAP is NOT detectable outside the CPU. The trap is taken only if the instruction reaches the execute stage of the CPU.


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### Table 6-36. Reset/Abort/Error Sources (continued)

| ERROR SOURCE | SYSTEM MODE | ERROR RESPONSE | ESM HOOKUP group.channel |
|---|---|---|---|
| Memory parity error | User/Privilege | ESM | 1.8 |
| **HTU2** | | | |
| NCNB (Strongly Ordered) transaction with slave error response | User/Privilege | Interrupt => VIM | n/a |
| External imprecise error (Illegal transaction with ok response) | User/Privilege | Interrupt => VIM | n/a |
| Memory access permission violation | User/Privilege | ESM | 1.9 |
| Memory parity error | User/Privilege | ESM | 1.8 |
| **N2HET1** | | | |
| Memory parity error | User/Privilege | ESM | 1.7 |
| **N2HET2** | | | |
| Memory parity error | User/Privilege | ESM | 1.7 |
| **FLEXRAY** | | | |
| Memory parity error | User/Privilege | ESM | 1.12 |
| **FTU** | | | |
| NCNB (Strongly Ordered) transaction with slave error response | User/Privilege | Interrupt => VIM | n/a |
| External imprecise error (Illegal transaction with ok response) | User/Privilege | Interrupt => VIM | n/a |
| Memory access permission violation | User/Privilege | ESM | 1.16 |
| Memory parity error | User/Privilege | ESM | 1.14 |
| **ETHERNET MASTER INTERFACE** | | | |
| Any error reported by slave being accessed | User/Privilege | ESM | 1.43 |
| **MIBSPI** | | | |
| MibSPI1 memory parity error | User/Privilege | ESM | 1.17 |
| MibSPI3 memory parity error | User/Privilege | ESM | 1.18 |
| MibSPI5 memory parity error | User/Privilege | ESM | 1.24 |
| **MIBADC** | | | |
| MibADC1 Memory parity error | User/Privilege | ESM | 1.19 |
| MibADC2 Memory parity error | User/Privilege | ESM | 1.1 |
| **DCAN** | | | |
| DCAN1 memory parity error | User/Privilege | ESM | 1.21 |
| DCAN2 memory parity error | User/Privilege | ESM | 1.23 |
| DCAN3 memory parity error | User/Privilege | ESM | 1.22 |
| **PLL** | | | |
| PLL slip error | User/Privilege | ESM | 1.10 |
| PLL #2 slip error | User/Privilege | ESM | 1.42 |
| **CLOCK MONITOR** | | | |
| Clock monitor interrupt | User/Privilege | ESM | 1.11 |
| **DCC** | | | |
| DCC1 error | User/Privilege | ESM | 1.30 |
| DCC2 error | User/Privilege | ESM | 1.62 |
| **CCM-R4** | | | |
| Self test failure | User/Privilege | ESM | 1.31 |
| Compare failure | User/Privilege | ESM => NMI => nERROR | 2.2 |
| **VIM** | | | |
| Memory parity error | User/Privilege | ESM | 1.15 |
| **VOLTAGE MONITOR** | | | |
| VMON out of voltage range | n/a | Reset | n/a |
| **CPU SELFTEST (LBIST)** | | | |
| CPU Selftest (LBIST) error | User/Privilege | ESM | 1.27 |

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**Table 6-36. Reset/Abort/Error Sources (continued)**

| ERROR SOURCE | SYSTEM MODE | ERROR RESPONSE | ESM HOOKUP group.channel |
|---|---|---|---|
| **PIN MULTIPLEXING CONTROL** | | | |
| Mux configuration error | User/Privilege | ESM | 1.37 |
| **POWER DOMAIN CONTROL** | | | |
| PSCON compare error | User/Privilege | ESM | 1.38 |
| PSCON self-test error | User/Privilege | ESM | 1.39 |
| **eFuse CONTROLLER** | | | |
| eFuse Controller Autoload error | User/Privilege | ESM => nERROR | 3.1 |
| eFuse Controller - Any bit set in the error status register | User/Privilege | ESM | 1.40 |
| eFuse Controller self-test error | User/Privilege | ESM | 1.41 |
| **WINDOWED WATCHDOG** | | | |
| WWD Nonmaskable Interrupt exception | n/a | ESM => NMI => nERROR | 2.24 |
| **ERRORS REFLECTED IN THE SYSESR REGISTER** | | | |
| Power-Up Reset | n/a | Reset | n/a |
| Oscillator fail / PLL slip (2) | n/a | Reset | n/a |
| Watchdog exception | n/a | Reset | n/a |
| CPU Reset (driven by the CPU STC) | n/a | Reset | n/a |
| Software Reset | n/a | Reset | n/a |
| External Reset | n/a | Reset | n/a |

(2) Oscillator fail/PLL slip can be configured in the system register (SYS.PLLCTL1) to generate a reset.

## 6.20 Digital Windowed Watchdog

This device includes a digital windowed watchdog (DWWD) module that protects against runaway code execution.

The DWWD module allows the application to configure the time window within which the DWWD module expects the application to service the watchdog. A watchdog violation occurs if the application services the watchdog outside of this window, or fails to service the watchdog at all. The application can choose to generate a system reset or a nonmaskable interrupt to the CPU in case of a watchdog violation.

The watchdog is disabled by default and must be enabled by the application. Once enabled, the watchdog can only be disabled upon a system reset.


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## 6.21 Debug Subsystem

### 6.21.1 Block Diagram

The device contains an ICEPICK module to allow JTAG access to the scan chains.

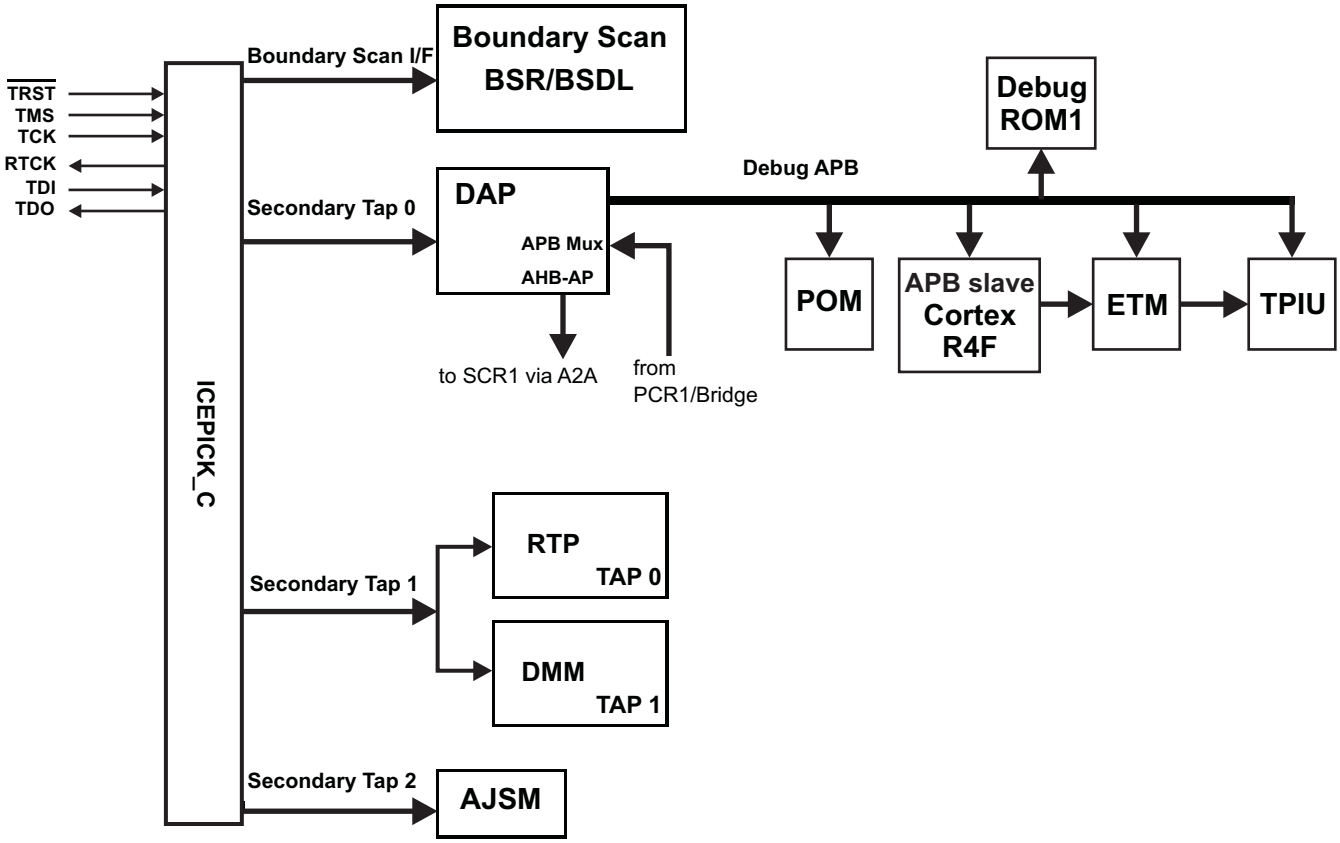


**Figure 6-19. Debug Subsystem Block Diagram**

**NOTE**

The ETM, RTP and DMM exist in silicon, but are not supported in the PGE package.

### 6.21.2 Debug Components Memory Map

**Table 6-37. Debug Components Memory Map**

| MODULE NAME | FRAME CHIP SELECT | FRAME ADDRESS RANGE | | FRAME SIZE | ACTUAL SIZE | RESPONSE FOR ACCESS TO UNIMPLEMENTED LOCATIONS IN FRAME |
|---|---|---|---|---|---|---|
| | | START | END | | | |
| CoreSight Debug ROM | CSCS0 | 0xFFA00000 | 0xFFA00FFF | 4KB | 4KB | Reads: 0, writes: no effect |
| Cortex-R4F Debug | CSCS1 | 0xFFA01000 | 0xFFA01FFF | 4KB | 4KB | Reads: 0, writes: no effect |
| ETM-R4 | CSCS2 | 0xFFA02000 | 0xFFA02FFF | 4KB | 4KB | Reads: 0, writes: no effect |
| CoreSight TPIU | CSCS3 | 0xFFA03000 | 0xFFA03FFF | 4KB | 4KB | Reads: 0, writes: no effect |

### 6.21.3 JTAG Identification Code

The JTAG ID code for this device is the same as the device ICEPick Identification Code.

**Table 6-38. JTAG ID Code**

| SILICON REVISION | ID |
|---|---|
| Rev A | 0x0B8A002F |
| Rev B | 0x2B8A002F |
| Rev C | 0x3B8A002F |
| Rev D | 0x4B8A002F |

### *6.21.4 Debug ROM*

The Debug ROM stores the location of the components on the Debug APB bus:

**Table 6-39. Debug ROM table**

| ADDRESS | DESCRIPTION | VALUE |
|---|---|---|
| 0x000 | pointer to Cortex-R4F | 0x00001003 |
| 0x001 | ETM-R4 | 0x00002003 |
| 0x002 | TPIU | 0x00003003 |
| 0x003 | POM | 0x00004003 |
| 0x004 | end of table | 0x00000000 |


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### 6.21.5 JTAG Scan Interface Timings

**Table 6-40. JTAG Scan Interface Timing (1)**

| NO. | PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| | fTCK | TCK frequency (at HCLKmax) | | 12 | MHz |
| | fRTCK | RTCK frequency (at TCKmax and HCLKmax) | 10 | | MHz |
| 1 | td(TCK -RTCK) | Delay time, TCK to RTCK | | 24 | ns |
| 2 | tsu(TDI/TMS - RTCKr) | Setup time, TDI, TMS before RTCK rise (RTCKr) | 26 | | ns |
| 3 | th(RTCKr -TDI/TMS) | Hold time, TDI, TMS after RTCKr | 0 | | ns |
| 4 | th(RTCKr -TDO) | Hold time, TDO after RTCKf | 0 | | ns |
| 5 | td(TCKf -TDO) | Delay time, TDO valid after RTCK fall (RTCKf) | | 12 | ns |

(1) Timings for TDO are specified for a maximum of 50pF load on TDO

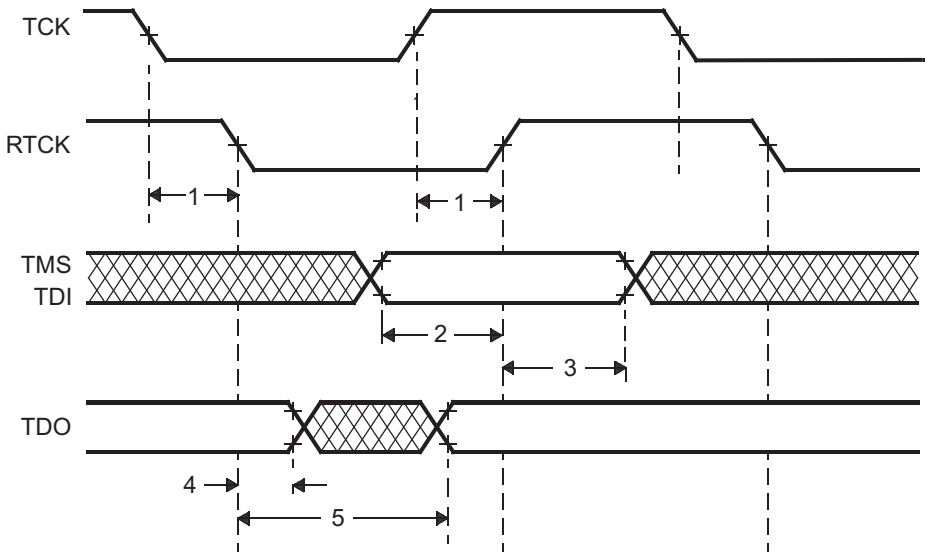


**Figure 6-20. JTAG Timing**

### 6.21.6 Advanced JTAG Security Module

This device includes an Advanced JTAG Security Module (AJSM) which provides maximum security to the memory content of the device by letting users secure the device after programming.

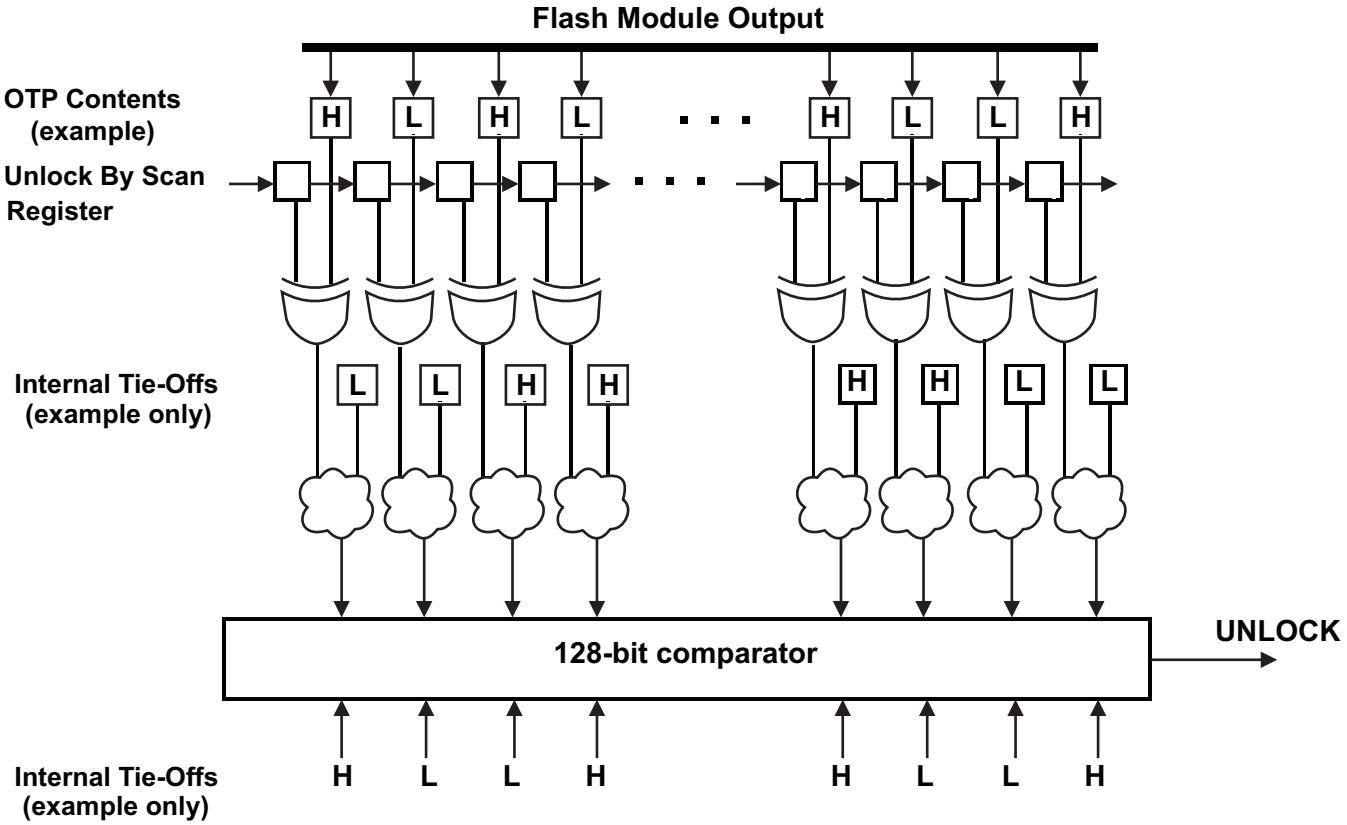


**Figure 6-21. AJSM Unlock**

The device is unsecure by default by virtue of a 128-bit visible unlock code programmed in the OTP address 0xF0000000.The OTP contents are XOR-ed with the "Unlock By Scan" register contents. The outputs of these XOR gates are again combined with a set of secret internal tie-offs. The output of this combinational logic is compared against a secret hard-wired 128-bit value. A match results in the UNLOCK signal being asserted, so that the device is now unsecure.

A user can secure the device by changing at least one bit in the visible unlock code from 1 to 0. Changing a 0 to 1 is not possible because the visible unlock code is stored in the One Time Programmable (OTP) flash region. Also, changing all the 128 bits to zeros is not a valid condition and will permanently secure the device.

Once secured, a user can unsecure the device by scanning an appropriate value into the "Unlock By Scan" register of the AJSM module. The value to be scanned is such that the XOR of the OTP contents and the Unlock-By-Scan register contents results in the original visible unlock code.

The Unlock-By-Scan register is reset only upon asserting power-on reset (nPORRST).

A secure device only permits JTAG accesses to the AJSM scan chain via the Secondary Tap # 2 of the ICEPick module. All other secondary taps, test taps and the boundary scan interface are not accessible in this state.


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### 6.21.7 Embedded Trace Macrocell (ETM-R4)

The device contains a ETM-R4 module with a 32-bit internal data port. The ETM-R4 module is connected to a TPIU with a 32-bit data bus; the TPIU provides a 35-bit (32-bit data, 3-bit control) external interface for trace. The ETM-R4 is CoreSight compliant and follows the ETM v3 specification; for more details see ARM CoreSight ETM-R4 TRM specification.

#### 6.21.7.1 ETM TRACECLKIN Selection

The ETM clock source can be selected as either VCLK or the external ETMTRACECLKIN pin. The selection is done by the EXTCTLOUT[1:0] control bits of the TPIU; the default is '00'. The address of this register is TPIU base address + 0x404.

Before you begin accessing TPIU registers, TPIU should be unlocked via coresight key and 1 or 2 should be written to this register.

**Table 6-41. TPIU / TRACECLKIN Selection**

| EXTCTLOUT[1:0] | TPIU/TRACECLKIN |
|---|---|
| 00 | tied-zero |
| 01 | VCLK |
| 10 | ETMTRACECLKIN |
| 11 | tied-zero |

#### 6.21.7.2 Timing Specifications

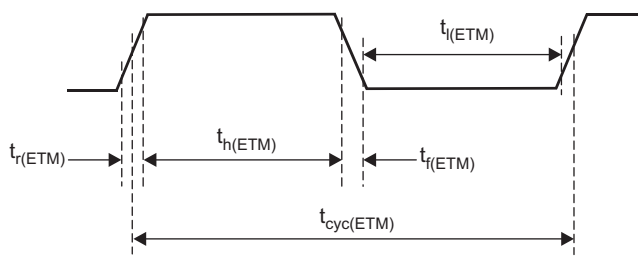


**Figure 6-22. ETMTRACECLKOUT Timing**

**Table 6-42. ETMTRACECLK Timing**

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{cyc(ETM)}$ | Clock period | $t_{(HCLK)}$ * 4 | | ns |
| $t_{l(ETM)}$ | Low pulse width | 20 | | ns |
| $t_{h(ETM)}$ | High pulse width | 20 | | ns |
| $t_{r(ETM)}$ | Clock and data rise time | | 3 | ns |
| $t_{f(ETM)}$ | Clock and data fall time | | 3 | ns |

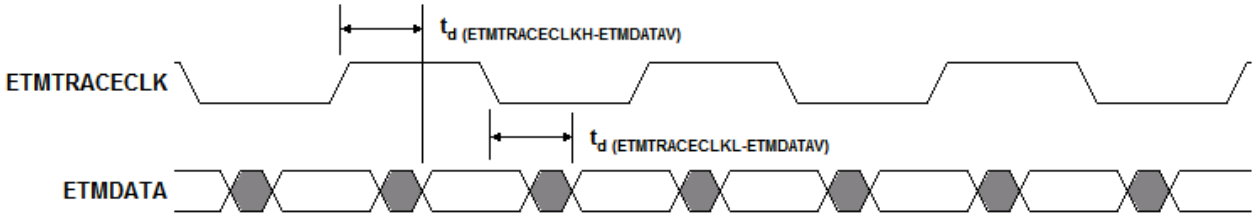


**Figure 6-23. ETMDATA Timing**

**Table 6-43. ETMDATA Timing**

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{d(ETMTRACECLKH-ETMDATAV)}$ | Delay time, ETM trace clock high to ETM data valid | 1.5 | 7 | ns |
| $t_{d(ETMTRACECLKl-ETMDATAV)}$ | Delay time, ETM trace clock low to ETM data valid | 1.5 | 7 | ns |

**NOTE**

The ETMTRACECLK and ETMDATA timing is based on a 15-pF load and for ambient temperature lower than 85°C.


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### 6.21.8 RAM Trace Port (RTP)

The RTP provides the ability to datalog the RAM contents of the TMS570 devices or accesses to peripherals without program intrusion. It can trace all data write or read accesses to internal RAM. In addition, it provides the capability to directly transfer data to a FIFO to support a CPU-controlled transmission of the data. The trace data is transmitted over a dedicated external interface.

#### 6.21.8.1 Features

The RTP offers the following features:

- Two modes of operation - Trace Mode and Direct Data Mode
  - Trace Mode
    - Nonintrusive data trace on write or read operation
    - Visibility of RAM content at any time on external capture hardware
    - Trace of peripheral accesses
    - 2 configurable trace regions for each RAM module to limit amount of data to be traced
    - FIFO to store data and address of data of multiple read/write operations
    - Trace of CPU and/or DMA accesses with indication of the master in the transmitted data packet
  - Direct Data Mode
    - Directly write data with the CPU or trace read operations to a FIFO, without transmitting header and address information
- Dedicated synchronous interface to transmit data to external devices
- Free-running clock generation or clock stop mode between transmissions
- Up to 100 Mbps/pin transfer rate for transmitting data
- Pins not used in functional mode can be used as GIOs

#### 6.21.8.2 Timing Specifications

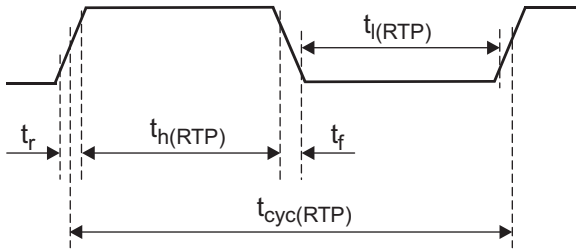


**Figure 6-24. RTPCLK Timing**

**Table 6-44. RTPCLK Timing**

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{cyc(RTP)}$ | Clock period, prescaled from HCLK; must not be faster than HCLK / 2 | 11 (= 90 MHz) | | ns |
| $t_{h(RTP)}$ | High pulse width | $((t_{cyc(RTP)})/2) - ((t_r+t_f)/2)$ | | ns |
| $t_{l(RTP)}$ | Low pulse width | $((t_{cyc(RTP)})/2) - ((t_r+t_f)/2)$ | | ns |

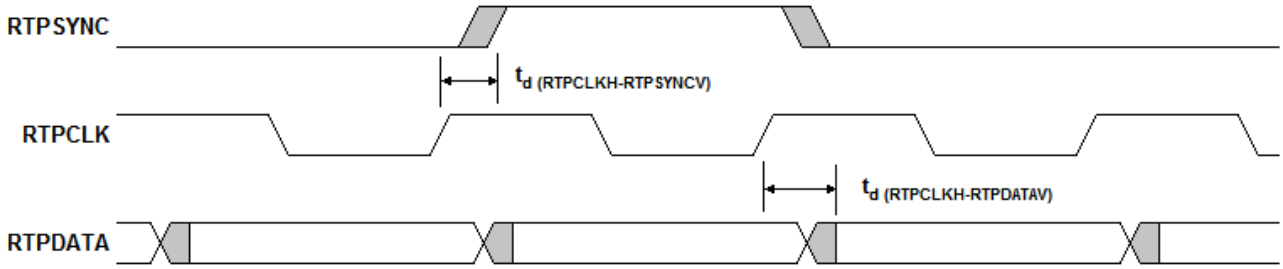


**Figure 6-25. RTPDATA Timing**

**Table 6-45. RTPDATA Timing**

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{d(RTPCLKH-RTPSYNCV)}$ | Delay time, RTPCLK high to RTPSYNC valid | –5 | 4 | ns |
| $t_{d(RTPCLKH-RTPDATAV)}$ | Delay time, RTPCLK high to RTPDATA valid | –5 | 4 | ns |

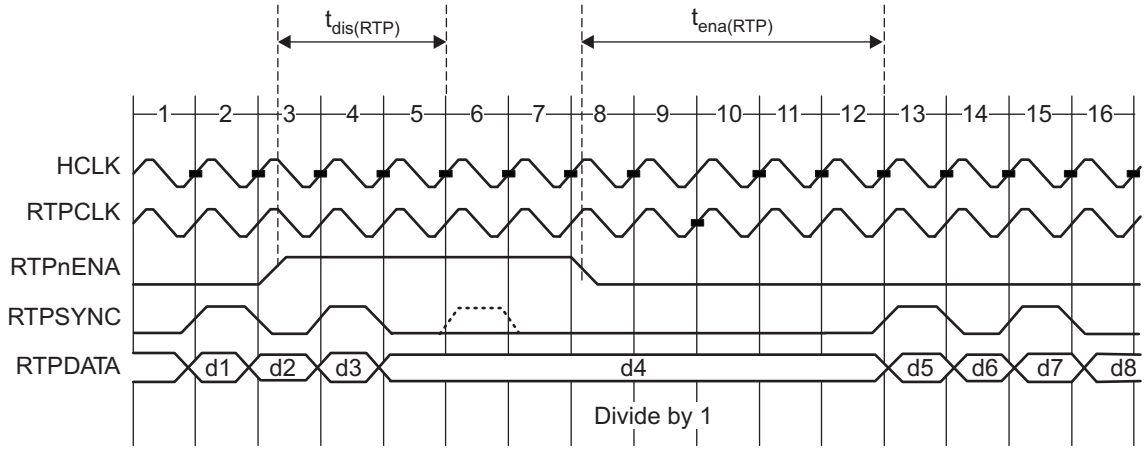


**Figure 6-26. RTPnENA Timing**

**Table 6-46. RTPnENA Timing**

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{dis(RTP)}$ | time RTPnENA must go high before what would be the next RTPSYNC, to ensure delaying the next packet | $3t_{c(HCLK)} + t_{r(RTPSYNC)} + 12$ | | ns |
| $t_{ena(RTP)}$ | time after RTPnENA goes low before a packet that has been halted, resumes | $4t_{c(HCLK)} + t_{r(RTPSYNC)}$ | $5t_{c(HCLK)} + t_{r(RTPSYNC)} + 12$ | ns |


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### 6.21.9 Data Modification Module (DMM)

The Data Modification Module (DMM) provides the capability to modify data in the entire 4-GB address space of the TMS570 devices from an external peripheral, with minimal interruption of the application.

#### 6.21.9.1 Features

The DMM module has the following features:

- Acts as a bus master, thus enabling direct writes to the 4-GB address space without CPU intervention
- Writes to memory locations specified in the received packet (leverages packets defined by trace mode of the RAM trace port (RTP) module
- Writes received data to consecutive addresses, which are specified by the DMM module (leverages packets defined by direct data mode of RTP module)
- Configurable port width (1, 2, 4, 8, 16 pins)
- Up to 100 Mbit/s pin data rate
- Unused pins configurable as GPIO pins

#### 6.21.9.2 Timing Specifications

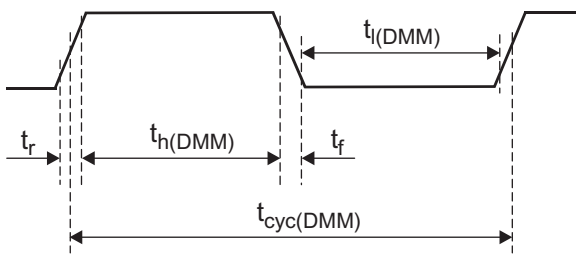


**Figure 6-27. DMMCLK Timing**

**Table 6-47. Timing Requirements for DMMCLK**

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{cyc(DMM)}$ | Cycle time, DMMCLK period | $t_{c(HCLK)}$ * 2 | | ns |
| $t_{h(DMM)}$ | Pulse duration, DMMCLK high | $((t_{cyc(DMM)})/2) - ((t_r+t_f)/2)$ | | ns |
| $t_{l(DMM)}$ | Pulse duration, DMMCLK low | $((t_{cyc(DMM)})/2) - ((t_r+t_f)/2)$ | | ns |

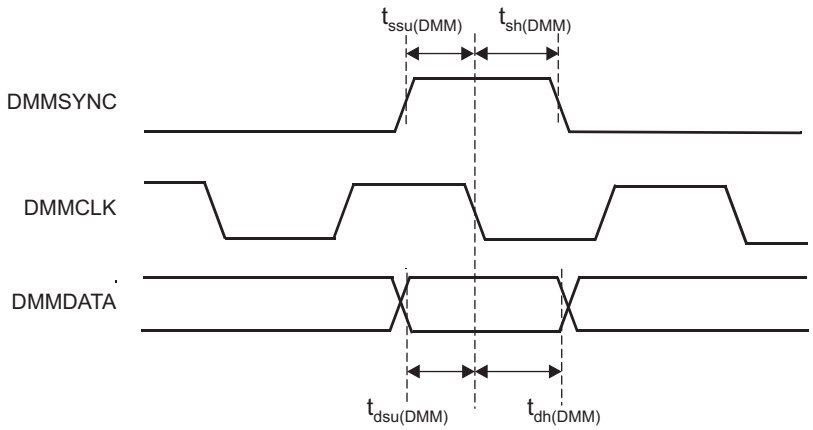


**Figure 6-28. DMMDATA Timing**

**Table 6-48. Timing Requirements for DMMDATA**

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{ssu(DMM)}$ | SYNC active to clk falling edge setup time | 2 | | ns |
| $t_{sh(DMM)}$ | clk falling edge to SYNC inactive hold time | 3 | | ns |
| $t_{dsu(DMM)}$ | DATA to clk falling edge setup time | 2 | | ns |
| $t_{dh(DMM)}$ | clk falling edge to DATA hold time | 3 | | ns |

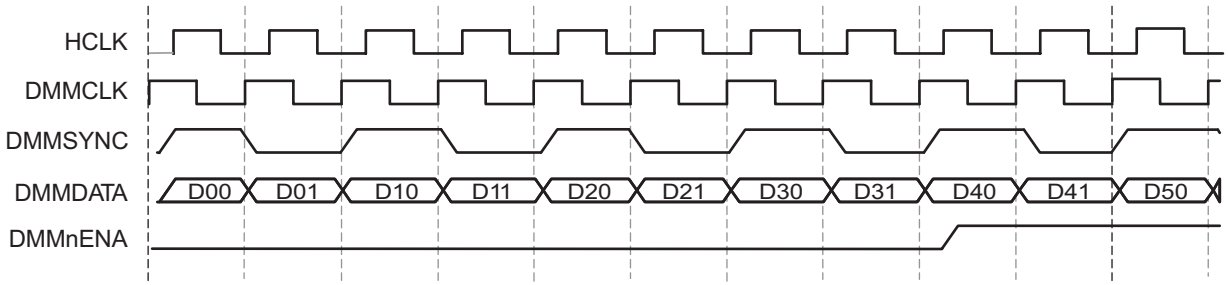


**Figure 6-29. DMMnENA Timing**

Figure 6-29 shows a case with 1 DMM packet per 2 DMMCLK cycles (Mode = Direct Data Mode, data width = 8, port width = 4) where none of the packets received by the DMM are sent out, leading to filling up of the internal buffers. The DMMnENA signal is shown asserted, after the first two packets have been received and synchronized to the HCLK domain. Here, the DMM has the capacity to accept packets D4x, D5x, D6x, D7x. Packet D8 would result in an overflow. Once DMMnENA is asserted, the DMM expects to stop receiving packets after 4 HCLK cycles; once DMMnENA is deasserted, the DMM can handle packets immediately (after 0 HCLK cycles).


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### 6.21.10 Boundary Scan Chain

The device supports IEEE1149.1-compliant boundary scan for testing pin-to-pin compatibility. The boundary scan chain is connected to the Boundary Scan Interface of the ICEPICK module.

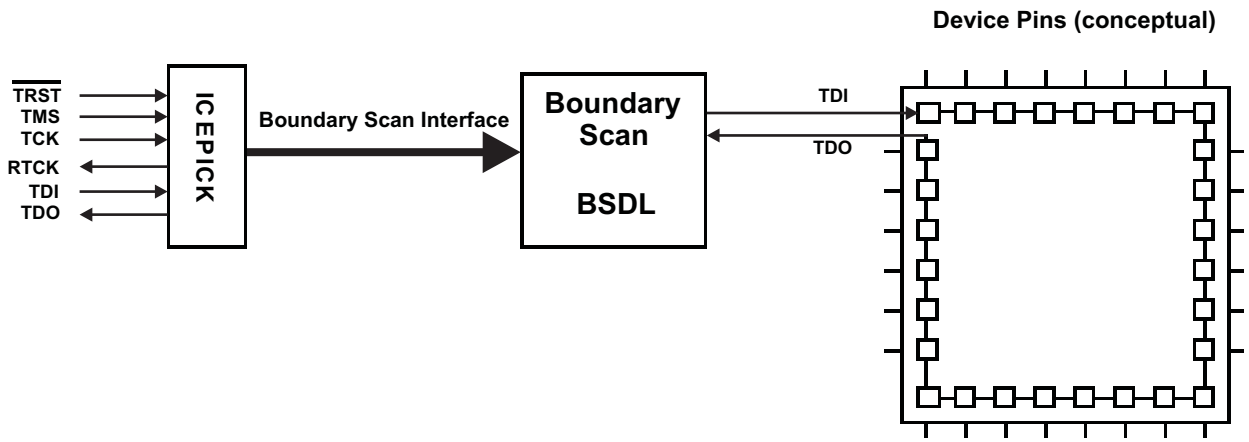


**Figure 6-30. Boundary Scan Implementation (Conceptual Diagram)**

Data is serially shifted into all boundary-scan buffers via TDI, and out via TDO.

# 7 Peripheral Information and Electrical Specifications

## 7.1 Peripheral Legend

**Table 7-1. Peripheral Legend**

| ABBREVIATION | FULL NAME |
|---|---|
| MibADC | Analog To Digital Converter |
| CCM-R4F | CPU Compare Module - CortexR4F |
| CRC | Cyclic Redundancy Check |
| DCAN | Controller Area Network |
| DCC | Dual Clock Comparator |
| DMA | Direct Memory Access |
| DMM | Data Modification Module |
| EMIF | External Memory Interface |
| ESM | Error Signaling Module |
| ETM-R4F | Embedded Trace Macrocell - CortexR4F |
| FTU | FlexRay Transfer Unit |
| GPIO | General-Purpose Input/Output |
| HTU | High End Timer Transfer Unit |
| I2C | Inter-Integrated Circuit |
| LIN | Local Interconnect Network |
| MIBSPI | Multibuffer Serial Peripheral Interface |
| N2HET | Platform High-End Timer |
| POM | Parameter Overlay Module |
| RTI | Real-Time Interrupt Module |
| RTP | RAM Trace Port |
| SCI | Serial Communications Interface |
| SPI | Serial Peripheral Interface |
| VIM | Vectored Interrupt Manager |

## 7.2 Multibuffered 12-Bit Analog-to-Digital Converter

The multibuffered A-to-D converter (MibADC) has a separate power bus for its analog circuitry that enhances the A-to-D performance by preventing digital switching noise on the logic circuitry which could be present on $V_{SS}$ and $V_{CC}$ from coupling into the A-to-D analog stage. All A-to-D specifications are given with respect to $AD_{REFLO}$ unless otherwise noted.

**Table 7-2. MibADC Overview**

| DESCRIPTION | VALUE |
|---|---|
| Resolution | 12 bits |
| Monotonic | Assured |
| Output conversion code | 00h to FFFh [00 for $V_{AI} \leq AD_{REFLO}$; FFF for $V_{AI} \geq AD_{REFHI}$] |


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### 7.2.1 Features

- 10-/12-bit resolution
- $AD_{REFHI}$ and $AD_{REFLO}$ pins (high and low reference voltages)
- Total Sample/Hold/Convert time: 600 ns Typical Minimum at 30 MHz ADCLK
- One memory region per conversion group is available (event, group 1, group 2)
- Allocation of channels to conversion groups is completely programmable
- Memory regions are serviced either by interrupt or by DMA
- Programmable interrupt threshold counter is available for each group
- Programmable magnitude threshold interrupt for each group for any one channel
- Option to read either 8-bit, 10-bit or 12-bit values from memory regions
- Single or continuous conversion modes
- Embedded self-test
- Embedded calibration logic
- Enhanced power-down mode
  - Optional feature to automatically power down ADC core when no conversion is in progress
- External event pin (ADEVT) programmable as general-purpose I/O

### 7.2.2 Event Trigger Options

The ADC module supports 3 conversion groups: Event Group, Group1 and Group2. Each of these 3 groups can be configured to be hardware event-triggered. In that case, the application can select from among 8 event sources to be the trigger for a group's conversions.

#### 7.2.2.1 Default MIBADC1 Event Trigger Hookup

**Table 7-3. MIBADC1 Event Trigger Hookup**

| Event # | Source Select Bits For G1, G2 Or Event (G1SRC[2:0], G2SRC[2:0] or EVSRC[2:0]) | Trigger |
|---|---|---|
| 1 | 000 | ADEVT |
| 2 | 001 | N2HET1[8] |
| 3 | 010 | N2HET1[10] |
| 4 | 011 | RTI compare 0 interrupt |
| 5 | 100 | N2HET1[12] |
| 6 | 101 | N2HET1[14] |
| 7 | 110 | GIOB[0] |
| 8 | 111 | GIOB[1] |

**NOTE**

For ADEVT, N2HET1 and GIOB trigger sources, the connection to the MibADC1 module trigger input is made from the output side of the input buffer. This way, a trigger condition can be generated either by configuring the function as output onto the pad (via the mux control), or by driving the function from an external trigger source as input. If the mux control module is used to select different functionality instead of the ADEVT, N2HET1[x] or GIOB[x] signals, then care must be taken to disable these signals from triggering conversions; there is no multiplexing on the input connections.

**NOTE**

For the RTI compare 0 interrupt source, the connection is made directly from the output of the RTI module. That is, the interrupt condition can be used as a trigger source even if the actual interrupt is not signaled to the CPU.

#### 7.2.2.2 Alternate MIBADC1 Event Trigger Hookup

**Table 7-4. Alternate MIBADC1 Event Trigger Hookup**

| EVENT # | SOURCE SELECT BITS FOR G1, G2 OR EVENT (G1SRC[2:0], G2SRC[2:0] or EVSRC[2:0]) | TRIGGER |
|---|---|---|
| 1 | 000 | ADEVT |
| 2 | 001 | N2HET2[5] |
| 3 | 010 | N2HET1[27] |
| 4 | 011 | RTI compare 0 interrupt |
| 5 | 100 | N2HET1[17] |
| 6 | 101 | N2HET1[19] |
| 7 | 110 | N2HET1[11] |
| 8 | 111 | N2HET2[13] |

The selection between the default MIBADC1 event trigger hook-up versus the alternate event trigger hook-up is done by multiplexing control module register 30 bits 0 and 1.

If 30[0] = 1, then the default MibADC1 event trigger hook-up is used.

If 30[0] = 0 and 30[1] = 1, then the alternate MibADC1 event trigger hook-up is used.

**NOTE**

For ADEVT trigger source, the connection to the MibADC1 module trigger input is made from the output side of the input buffer. This way, a trigger condition can be generated either by configuring ADEVT as an output function on to the pad (via the mux control), or by driving the ADEVT signal from an external trigger source as input. If the mux control module is used to select different functionality instead of the ADEVT signal, then care must be taken to disable ADEVT from triggering conversions; there is no multiplexing on the input connection.

**NOTE**

For N2HETx trigger sources, the connection to the MibADC1 module trigger input is made from the input side of the output buffer (at the N2HETx module boundary). This way, a trigger condition can be generated even if the N2HETx signal is not selected to be output on the pad.

**NOTE**

For the RTI compare 0 interrupt source, the connection is made directly from the output of the RTI module. That is, the interrupt condition can be used as a trigger source even if the actual interrupt is not signaled to the CPU.


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#### 7.2.2.3 Default MIBADC2 Event Trigger Hookup

**Table 7-5. MIBADC2 Event Trigger Hookup**

| EVENT # | SOURCE SELECT BITS FOR G1, G2 OR EVENT (G1SRC[2:0], G2SRC[2:0] or EVSRC[2:0]) | TRIGGER |
|---|---|---|
| 1 | 000 | AD2EVT |
| 2 | 001 | N2HET1[8] |
| 3 | 010 | N2HET1[10] |
| 4 | 011 | RTI compare 0 |
| 5 | 100 | N2HET1[12] |
| 6 | 101 | N2HET1[14] |
| 7 | 110 | GIOB[0] |
| 8 | 111 | GIOB[1] |

**NOTE**

For AD2EVT, N2HET1 and GIOB trigger sources, the connection to the MibADC2 module trigger input is made from the output side of the input buffer. This way, a trigger condition can be generated either by configuring the function as output onto the pad (via the mux control), or by driving the function from an external trigger source as input. If the mux control module is used to select different functionality instead of the AD2EVT, N2HET1[x] or GIOB[x] signals, then care must be taken to disable these signals from triggering conversions; there is no multiplexing on the input connections.

**NOTE**

For the RTI compare 0 interrupt source, the connection is made directly from the output of the RTI module. That is, the interrupt condition can be used as a trigger source even if the actual interrupt is not signaled to the CPU.

#### 7.2.2.4 Alternate MIBADC2 Event Trigger Hookup

**Table 7-6. Alternate MIBADC2 Event Trigger Hookup**

| EVENT # | SOURCE SELECT BITS FOR G1, G2 OR EVENT (G1SRC[2:0], G2SRC[2:0] or EVSRC[2:0]) | TRIGGER |
|---|---|---|
| 1 | 000 | AD2EVT |
| 2 | 001 | N2HET2[5] |
| 3 | 010 | N2HET1[27] |
| 4 | 011 | RTI compare 0 |
| 5 | 100 | N2HET1[17] |
| 6 | 101 | N2HET1[19] |
| 7 | 110 | N2HET1[11] |
| 8 | 111 | N2HET2[13] |

The selection between the default MIBADC2 event trigger hook-up versus the alternate event trigger hook-up is done by multiplexing control module register 30 bits 0 and 1.

If 30[0] = 1, then the default MibADC2 event trigger hook-up is used.

If 30[0] = 0 and 30[1] = 1, then the alternate MibADC2 event trigger hook-up is used.

**NOTE**

For AD2EVT trigger source, the connection to the MibADC2 module trigger input is made from the output side of the input buffer. This way, a trigger condition can be generated either by configuring AD2EVT as an output function on to the pad (via the mux control), or by driving the AD2EVT signal from an external trigger source as input. If the mux control module is used to select different functionality instead of the AD2EVT signal, then care must be taken to disable AD2EVT from triggering conversions; there is no multiplexing on the input connections.

**NOTE**

For N2HETx trigger sources, the connection to the MibADC2 module trigger input is made from the input side of the output buffer (at the N2HETx module boundary). This way, a trigger condition can be generated even if the N2HETx signal is not selected to be output on the pad.

**NOTE**

For the RTI compare 0 interrupt source, the connection is made directly from the output of the RTI module. That is, the interrupt condition can be used as a trigger source even if the actual interrupt is not signaled to the CPU.


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### 7.2.3 ADC Electrical and Timing Specifications

**Table 7-7. MibADC Recommended Operating Conditions**

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $AD_{REFHI}$ | A-to-D high-voltage reference source | $AD_{REFLO}$ | $V_{CCAD}$ (1) | V |
| $AD_{REFLO}$ | A-to-D low-voltage reference source | $V_{SSAD}$ (1) | $AD_{REFHI}$ | V |
| $V_{AI}$ | Analog input voltage | $AD_{REFLO}$ | $AD_{REFHI}$ | V |
| $I_{AIK}$ | Analog input clamp current (2)<br>(VAI < VSSAD – 0.3 or VAI > VCCAD + 0.3) | - 2 | 2 | mA |

(1) For $V_{CCAD}$ and $V_{SSAD}$ recommended operating conditions, see Section 5.4.
(2) Input currents into any ADC input channel outside the specified limits could affect conversion results of other channels.

**Table 7-8. MibADC Electrical Characteristics Over Full Ranges of Recommended Operating Conditions**

| PARAMETER | | DESCRIPTION/CONDITIONS | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $R_{mux}$ | Analog input mux on-resistance | See Figure 7-1 | | | 250 | Ω |
| $R_{samp}$ | ADC sample switch on-resistance | See Figure 7-1 | | | 250 | Ω |
| $C_{mux}$ | Input mux capacitance | See Figure 7-1 | | | 16 | pF |
| $C_{samp}$ | ADC sample capacitance | See Figure 7-1 | | | 13 | pF |
| $I_{AIL}$ | Analog off-state input leakage current | $V_{CCAD}$ = 3.6 V maximum | $V_{SSAD} \le V_{IN} < V_{SSAD}$ + 100 mV | –300 | 200 | nA |
| | | | $V_{SSAD}$ + 100 mV ≤ $V_{IN} \le V_{CCAD}$ - 200 mV | –200 | 200 | |
| | | | $V_{CCAD}$ - 200 mV < $V_{IN} \le V_{CCAD}$ | –200 | 500 | |
| $I_{AIL}$ | Analog off-state input leakage current | $V_{CCAD}$ = 5.5 V maximum | $V_{SSAD} \le V_{IN} < V_{SSAD}$ + 300 mV | –1000 | 250 | nA |
| | | | $V_{SSAD}$ + 300 mV ≤ $V_{IN} \le V_{CCAD}$ - 300 mV | –250 | 250 | |
| | | | $V_{CCAD}$ - 300 mV < $V_{IN} \le V_{CCAD}$ | –250 | 1000 | |
| $I_{AOSB1}$ (1) | ADC1 Analog on-state input bias current | $V_{CCAD}$ = 3.6 V maximum | $V_{SSAD} \le V_{IN} < V_{SSAD}$ + 100 mV | –8 | 2 | µA |
| | | | $V_{SSAD}$ + 100 mV < $V_{IN}$ < $V_{CCAD}$ - 200 mV | –4 | 2 | |
| | | | $V_{CCAD}$ - 200 mV < $V_{IN}$ < $V_{CCAD}$ | –4 | 12 | |
| $I_{AOSB2}$ (1) | ADC2 Analog on-state input bias current | $V_{CCAD}$ = 3.6 V maximum | $V_{SSAD} \le V_{IN} < V_{SSAD}$ + 100 mV | –7 | 2 | µA |
| | | | $V_{SSAD}$ + 100 mV ≤ $V_{IN} \le V_{CCAD}$ - 200 mV | –4 | 2 | |
| | | | $V_{CCAD}$ - 200 mV < $V_{IN} \le V_{CCAD}$ | –4 | 10 | |
| $I_{AOSB1}$ (1) | ADC1 Analog on-state input bias current | $V_{CCAD}$ = 5.5 V maximum | $V_{SSAD} \le V_{IN} < V_{SSAD}$ + 300 mV | –10 | 3 | µA |
| | | | $V_{SSAD}$ + 300 mV ≤ $V_{IN} \le V_{CCAD}$ - 300 mV | –5 | 3 | |
| | | | $V_{CCAD}$ - 300 mV < $V_{IN} \le V_{CCAD}$ | –5 | 14 | |
| $I_{AOSB2}$ (1) | ADC2 Analog on-state input bias current | $V_{CCAD}$ = 5.5 V maximum | $V_{SSAD} \le V_{IN} < V_{SSAD}$ + 300 mV | –8 | 3 | µA |
| | | | $V_{SSAD}$ + 300 mV ≤ $V_{IN} \le V_{CCAD}$ - 300 mV | –5 | 3 | |
| | | | $V_{CCAD}$ - 300 mV < $V_{IN} \le V_{CCAD}$ | –5 | 12 | |
| $I_{ADREFHI}$ | $AD_{REFHI}$ input current | $AD_{REFHI} = V_{CCAD}$, $AD_{REFLO} = V_{SSAD}$ | | | 3 | mA |
| $I_{CCAD}$ | Static supply current | Normal operating mode | | | 15 | mA |
| | | ADC core in power down mode | | | 5 | µA |

(1) If a shared channel is being converted by both ADC converters at the same time, the on-state leakage is equal to $I_{AOSL1} + I_{AOSL2}$

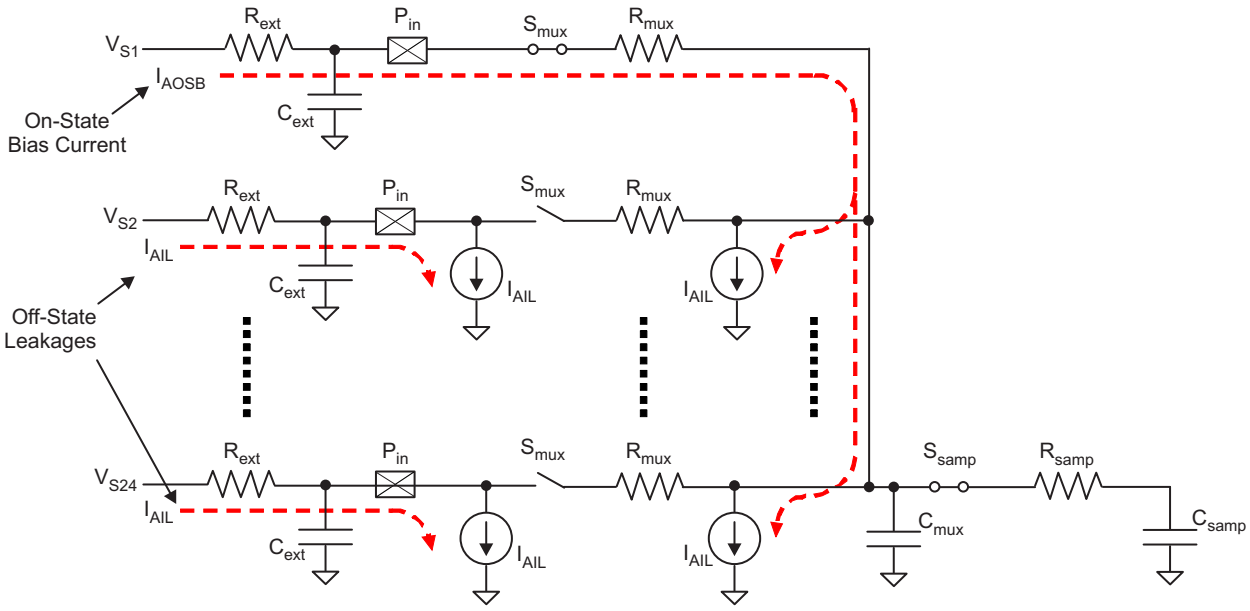


**Figure 7-1. MibADC Input Equivalent Circuit**

**Table 7-9. MibADC Timing Specifications**

| PARAMETER | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{c(ADCLK)}$ (1) | Cycle time, MibADC clock | 0.033 | | | µs |
| $t_{d(SH)}$ (2) | Delay time, sample and hold time | 0.2 | | | µs |
| $t_{d(PU-ADV)}$ | Delay time from ADC power on until first input can be sampled | 1 | | | µs |
| **12-BIT MODE** | | | | | |
| $t_{d(c)}$ | Delay time, conversion time | 0.4 | | | µs |
| $t_{d(SHC)}$ (3) | Delay time, total sample/hold and conversion time | 0.6 | | | µs |
| **10-BIT MODE** | | | | | |
| $t_{d(c)}$ | Delay time, conversion time | 0.33 | | | µs |
| $t_{d(SHC)}$ (3) | Delay time, total sample/hold and conversion time | 0.53 | | | µs |

(1) The MibADC clock is the ADCLK, generated by dividing down the VCLK by a prescale factor defined by the ADCLOCKCR register bits 4:0.
(2) The sample and hold time for the ADC conversions is defined by the ADCLK frequency and the AD<GP>SAMP register for each conversion group. The sample time needs to be determined by accounting for the external impedance connected to the input channel as well as the ADC's internal impedance.
(3) This is the minimum sample/hold and conversion time that can be achieved. These parameters are dependent on many factors, for example, the prescale settings.


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### Table 7-10. MibADC Operating Characteristics Over Full Ranges of Recommended Operating Conditions

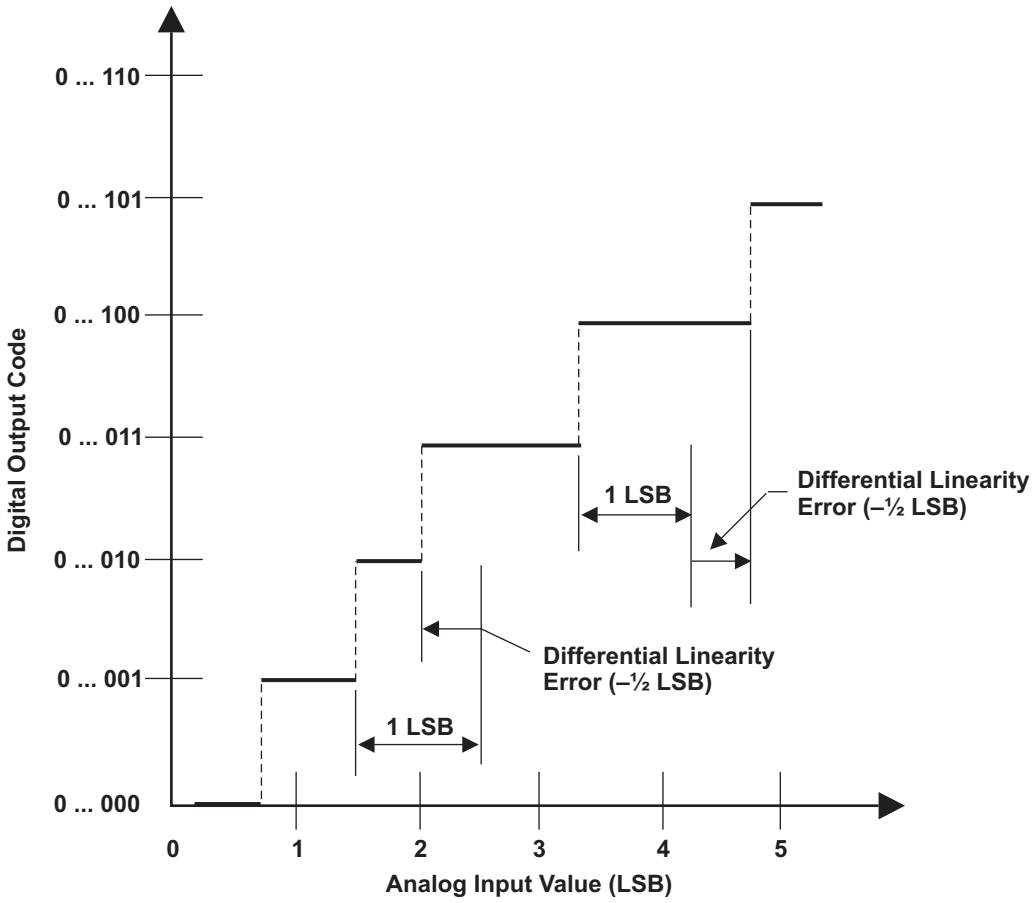
| PARAMETER | | DESCRIPTION/CONDITIONS | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| CR | Conversion range over which specified accuracy is maintained | $AD_{REFHI}$ - $AD_{REFLO}$ | | 3 | | 5.5 | V |
| $Z_{SET}$ | Zero Scale Offset | Difference between the first ideal transition (from code 000h to 001h) and the actual transition | 10-bit mode | | | 1 | LSB (1) |
| | | | 12-bit mode | | | 2 | LSB (2) |
| $F_{SET}$ | Full Scale Offset | Difference between the range of the measured code transitions (from first to last) and the range of the ideal code transitions | 10-bit mode | | | 2 | LSB |
| | | | 12-bit mode | | | 3 | LSB |
| $E_{DNL}$ | Differential nonlinearity error | Difference between the actual step width and the ideal value. (See Figure 76) | 10-bit mode | | | ± 1.5 | LSB |
| | | | 12-bit mode | | | ± 2 | LSB |
| $E_{INL}$ | Integral nonlinearity error | Maximum deviation from the best straight line through the MibADC. MibADC transfer characteristics, excluding the quantization error. | 10-bit mode | | | ± 2 | LSB |
| | | | 12-bit mode | | | ± 2 | LSB |
| $E_{TOT}$ | Total unadjusted error | Maximum value of the difference between an analog value and the ideal midstep value. | 10-bit mode | | | ± 2 | LSB |
| | | | 12-bit mode | | | ± 4 | LSB |

(1) 1 LSB = $(AD_{REFHI} – AD_{REFLO})/ 2^{10}$ for 10-bit mode
(2) 1 LSB = $(AD_{REFHI} – AD_{REFLO})/ 2^{12}$ for 12-bit mode

### 7.2.4 Performance (Accuracy) Specifications

#### 7.2.4.1 MibADC Nonlinearity Errors

The differential nonlinearity error shown in Figure 7-2 (sometimes referred to as differential linearity) is the difference between an actual step width and the ideal value of 1 LSB.




NOTE A: 1 LSB = $(AD_{REFHI} - AD_{REFLO})/2^{12}$

**Figure 7-2. Differential Nonlinearity (DNL) Error**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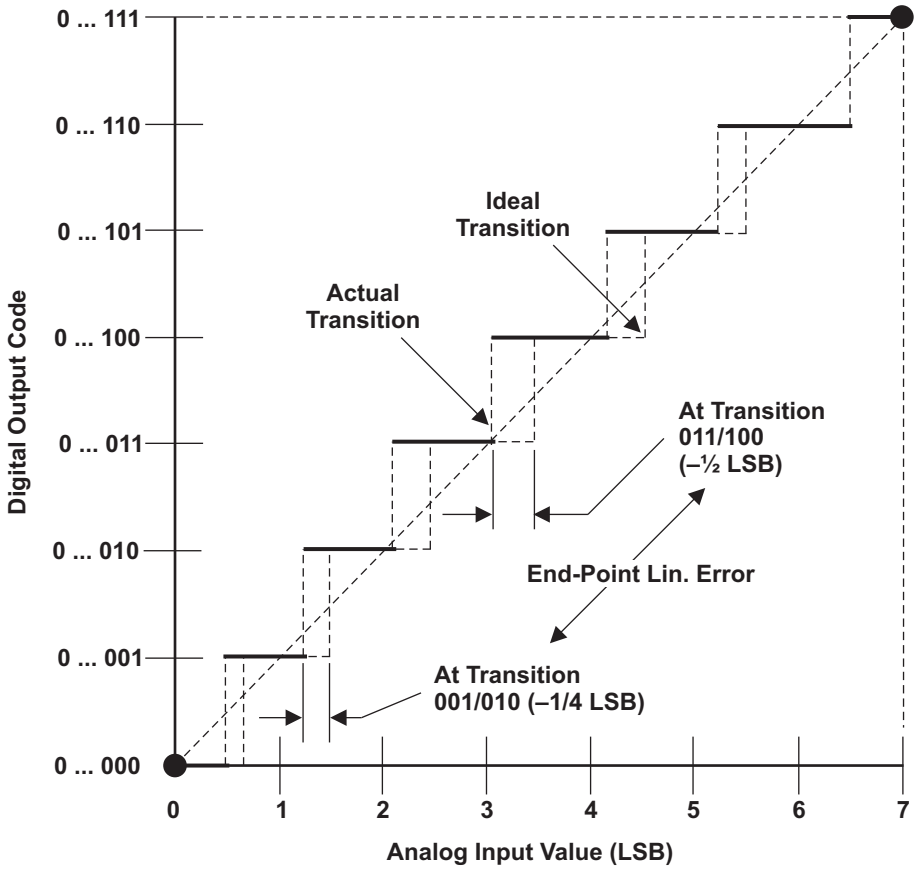
The integral nonlinearity error shown in Figure 7-3 (sometimes referred to as linearity error) is the deviation of the values on the actual transfer function from a straight line.

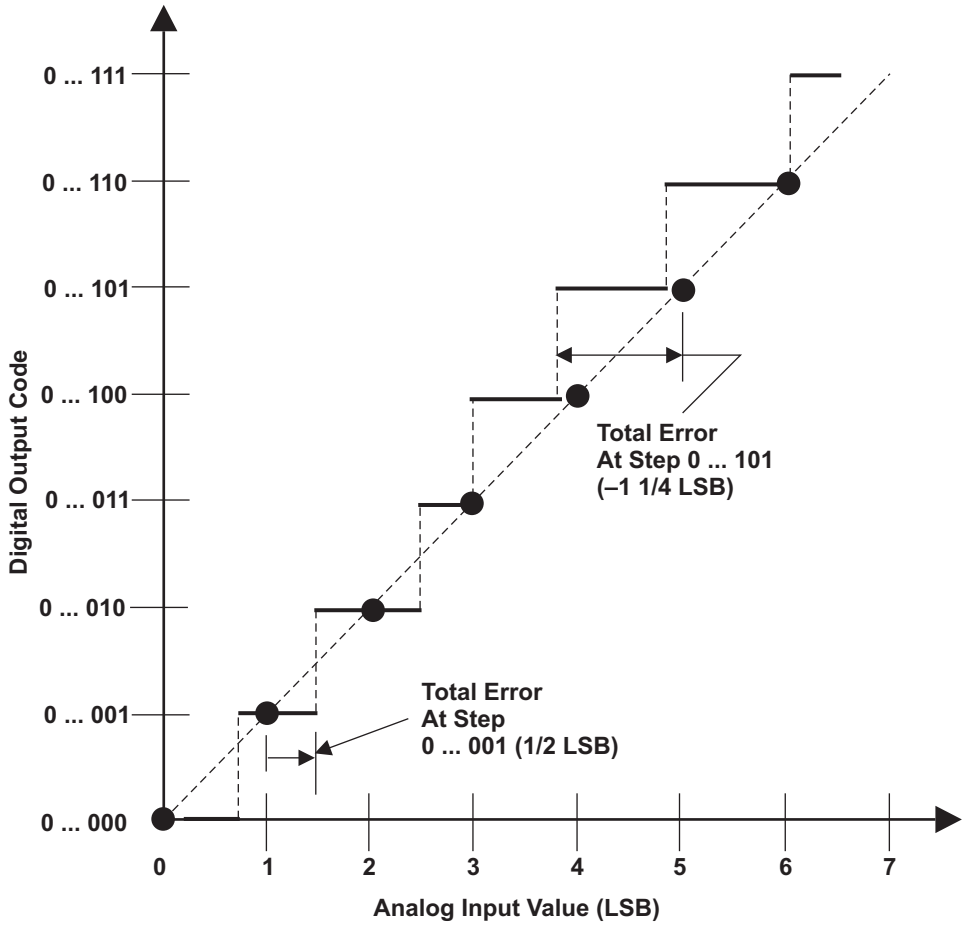



NOTE A: 1 LSB = $(AD_{REFHI} - AD_{REFLO})/2^{12}$

**Figure 7-3. Integral Nonlinearity (INL) Error**

#### 7.2.4.2 MibADC Total Error

The absolute accuracy or total error of an MibADC as shown in Figure 7-4 is the maximum value of the difference between an analog value and the ideal midstep value.




NOTE A: 1 LSB = $(AD_{REFHI} - AD_{REFLO})/2^{12}$

**Figure 7-4. Absolute Accuracy (Total) Error**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## 7.3 General-Purpose Input/Output

The GPIO module on this device supports two ports, GIOA and GIOB. The I/O pins are bidirectional and bit-programmable. Both GIOA and GIOB support external interrupt capability.

### *7.3.1 Features*

The GPIO module has the following features:

- Each IO pin can be configured as:
  - Input
  - Output
  - Open Drain
- The interrupts have the following characteristics:
  - Programmable interrupt detection either on both edges or on a single edge (set in GIOINTDET)
  - Programmable edge-detection polarity, either rising or falling edge (set in GIOPOL register)
  - Individual interrupt flags (set in GIOFLG register)
  - Individual interrupt enables, set and cleared through GIOENASET and GIOENACLR registers respectively
  - Programmable interrupt priority, set through GIOLVLSET and GIOLVLCLR registers
- Internal pullup/pulldown allows unused I/O pins to be left unconnected

For information on input and output timings see Section 5.11 and Section 5.12

## 7.4 Enhanced High-End Timer (N2HET)

The N2HET is an advanced intelligent timer that provides sophisticated timing functions for real-time applications. The timer is software-controlled, using a reduced instruction set, with a specialized timer micromachine and an attached I/O port. The N2HET can be used for pulse width modulated outputs, capture or compare inputs, or general-purpose I/O. It is especially well suited for applications requiring multiple sensor information and drive actuators with complex and accurate time pulses.

### *7.4.1 Features*

The N2HET module has the following features:

- Programmable timer for input and output timing functions
- Reduced instruction set (30 instructions) for dedicated time and angle functions
- 160 words of instruction RAM protected by parity
- User defined number of 25-bit virtual counters for timer, event counters and angle counters
- 7-bit hardware counters for some pins allow up to 32-bit resolution in conjunction with the 25-bit virtual counters
- Up to 32 pins usable for input signal measurements or output signal generation
- Programmable suppression filter for each input pin with adjustable limiting frequency
- Low CPU overhead and interrupt load
- Efficient data transfer to or from the CPU memory with dedicated High-End-Timer Transfer Unit (HTU) or DMA
- Diagnostic capabilities with different loopback mechanisms and pin status readback functionality

### *7.4.2 N2HET RAM Organization*

The timer RAM uses 4 RAM banks, where each bank has two port access capability. This means that one RAM address may be written while another address is read. The RAM words are 96 bits wide, which are split into three 32-bit fields (program, control, and data).

### *7.4.3 Input Timing Specifications*

The N2HET instructions PCNT and WCAP impose some timing constraints on the input signals.

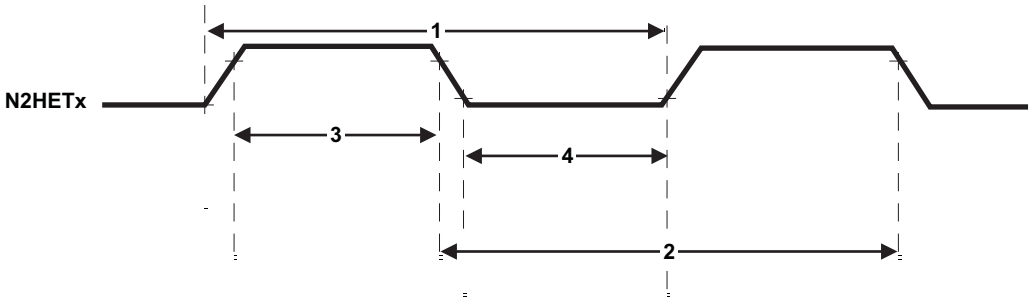


**Figure 7-5. N2HET Input Capture Timings**


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### Table 7-11. Input Timing Requirements for the N2HET Input Capture Functionality

| NO. | | MIN (1) (2) | MAX (1) (2) | UNIT |
|---|---|---|---|---|
| 1 | Input signal period, PCNT or WCAP for rising edge to rising edge | 2 (hr) (lr) $tc_{(VCLK2)}$ + 2 | $2^{25}$ (hr) (lr) $tc_{(VCLK2)}$ - 2 | ns |
| 2 | Input signal period, PCNT or WCAP for falling edge to falling edge | 2 (hr) (lr) $tc_{(VCLK2)}$ + 2 | $2^{25}$ (hr) (lr) $tc_{(VCLK2)}$ - 2 | ns |
| 3 | Input signal high phase, PCNT or WCAP for rising edge to falling edge | (hr) (lr) $tc_{(VCLK2)}$ + 2 | $2^{25}$ (hr) (lr) $tc_{(VCLK2)}$ - 2 | ns |
| 4 | Input signal low phase, PCNT or WCAP for falling edge to rising edge | (hr) (lr) $tc_{(VCLK2)}$ + 2 | $2^{25}$ (hr) (lr) $tc_{(VCLK2)}$ - 2 | ns |

(1) hr = High-resolution prescaler, configured using the HRPFC field of the Prescale Factor Register (HETPFR).
(2) lr = Loop-resolution prescaler, configured using the LFPRC field of the Prescale Factor Register (HETPFR).

Both N2HET1 and N2HET2 have channels that are enhanced to be able to capture inputs with smaller pulse widths than that specified in Table 7-11. See Table 7-13 for a list of which pins support small pulse capture.

The input capture capability for these channels is specified in Table 7-12.

### Table 7-12. Input Timing Requirements for N2HET Channels with Enhanced Pulse Capture

| NO. | | MIN | MAX | UNIT |
|---|---|---|---|---|
| 1 | Input signal period, PCNT or WCAP for rising edge to rising edge | (hr) (lr) $tc_{(VCLK2)}$ + 2 | $2^{25}$ (hr) (lr) $tc_{(VCLK2)}$ - 2 | ns |
| 2 | Input signal period, PCNT or WCAP for falling edge to falling edge | (hr) (lr) $tc_{(VCLK2)}$ + 2 | $2^{25}$ (hr) (lr) $tc_{(VCLK2)}$ - 2 | ns |
| 3 | Input signal high phase, PCNT or WCAP for rising edge to falling edge | 2 (hr) $tc_{(VCLK2)}$ + 2 | $2^{25}$ (hr) (lr) $tc_{(VCLK2)}$ - 2 | ns |
| 4 | Input signal low phase, PCNT or WCAP for falling edge to rising edge | 2 (hr) $tc_{(VCLK2)}$ + 2 | $2^{25}$ (hr) (lr) $tc_{(VCLK2)}$ - 2 | ns |

### Table 7-13. Input Capture Pin Capability

| CHANNEL | SUPPORTS 32-BIT CAPTURE | ENHANCED PULSE CAPTURE |
|---|---|---|
| N2HET1[00] | **Yes** | No |
| N2HET1[01] | **Yes** | No |
| N2HET1[02] | **Yes** | No |
| N2HET1[03] | **Yes** | No |
| N2HET1[04] | **Yes** | No |
| N2HET1[05] | **Yes** | No |
| N2HET1[06] | **Yes** | No |
| N2HET1[07] | **Yes** | No |
| N2HET1[08] | **Yes** | No |
| N2HET1[09] | **Yes** | No |
| N2HET1[10] | **Yes** | No |
| N2HET1[11] | **Yes** | No |
| N2HET1[12] | **Yes** | No |
| N2HET1[13] | **Yes** | No |
| N2HET1[14] | **Yes** | No |
| N2HET1[15] | **Yes** | **Yes** |
| N2HET1[16] | **Yes** | No |
| N2HET1[17] | **Yes** | No |
| N2HET1[18] | **Yes** | No |
| N2HET1[19] | **Yes** | No |
| N2HET1[20] | **Yes** | **Yes** |

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**Table 7-13. Input Capture Pin Capability (continued)**

| CHANNEL | SUPPORTS 32-BIT CAPTURE | ENHANCED PULSE CAPTURE |
|---|---|---|
| N2HET1[21] | **Yes** | No |
| N2HET1[22] | **Yes** | No |
| N2HET1[23] | **Yes** | No |
| N2HET1[24] | **Yes** | No |
| N2HET1[25] | **Yes** | No |
| N2HET1[26] | **Yes** | No |
| N2HET1[27] | **Yes** | No |
| N2HET1[28] | **Yes** | No |
| N2HET1[29] | **Yes** | No |
| N2HET1[30] | **Yes** | No |
| N2HET1[31] | **Yes** | **Yes** |
| N2HET2[00] | **Yes** | No |
| N2HET2[01] | No | No |
| N2HET2[02] | No | No |
| N2HET2[03] | No | No |
| N2HET2[04] | **Yes** | No |
| N2HET2[05] | No | No |
| N2HET2[06] | **Yes** | No |
| N2HET2[07] | No | No |
| N2HET2[08] | No | No |
| N2HET2[09] | No | No |
| N2HET2[10] | No | No |
| N2HET2[11] | No | No |
| N2HET2[12] | **Yes** | **Yes** |
| N2HET2[13] | No | No |
| N2HET2[14] | **Yes** | **Yes** |
| N2HET2[15] | No | No |
| N2HET2[16] | **Yes** | **Yes** |
| N2HET2[18] | No | No |

### *7.4.4 N2HET1-N2HET2 Interconnections*

In some applications the N2HET resolutions must be synchronized. Some other applications require a single time base to be used for all PWM outputs and input timing captures.

The N2HET provides such a synchronization mechanism. The Clk_master/slave (HETGCR.16) configures the N2HET in master or slave mode (default is slave mode). A N2HET in master mode provides a signal to synchronize the prescalers of the slave N2HET. The slave N2HET synchronizes its loop resolution to the loop resolution signal sent by the master. The slave does not require this signal after it receives the first synchronization signal. However, anytime the slave receives the resynchronization signal from the master, the slave must synchronize itself again..

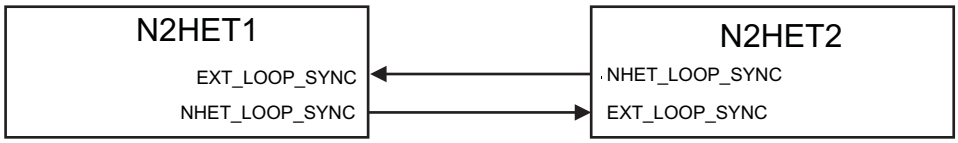


**Figure 7-6. N2HET1 – N2HET2 Synchronization Hookup**


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### 7.4.5 N2HET Checking

#### 7.4.5.1 Internal Monitoring

To assure correctness of the high-end timer operation and output signals, the two N2HET modules can be used to monitor each other's signals as shown in Figure 7-7. The direction of the monitoring is controlled by the I/O multiplexing control module.

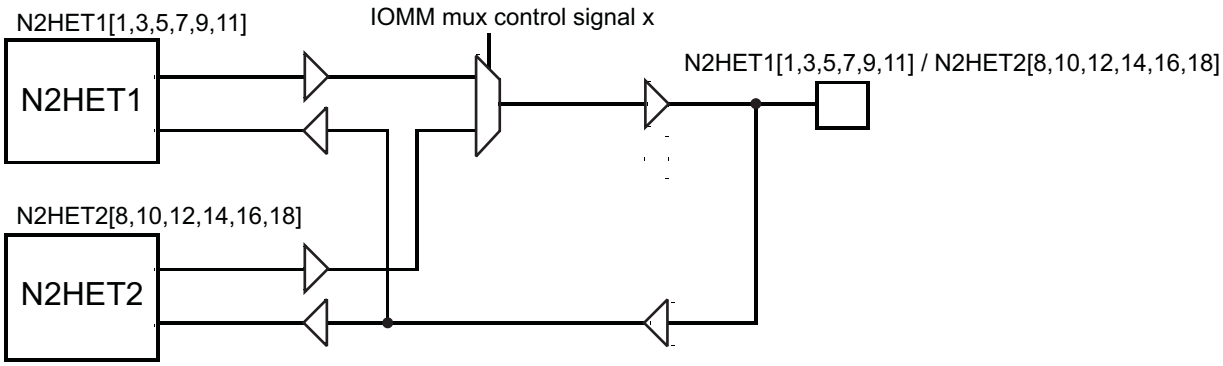


**Figure 7-7. N2HET Monitoring**

#### 7.4.5.2 Output Monitoring Using Dual Clock Comparator (DCC)

N2HET1[31] is connected as a clock source for counter 1 in DCC1. This allows the application to measure the frequency of the pulse-width modulated (PWM) signal on N2HET1[31].

Similarly, N2HET2[0] is connected as a clock source for counter 1 in DCC2. This allows the application to measure the frequency of the pulse-width modulated (PWM) signal on N2HET2[0].

Both N2HET1[31] and N2HET2[0] can be configured to be internal-only channels. That is, the connection to the DCC module is made directly from the output of the N2HETx module (from the input of the output buffer).

For more information on DCC see Section 6.7.3.

### 7.4.6 Disabling N2HET Outputs

Some applications require the N2HET outputs to be disabled under some fault condition. The N2HET module provides this capability via the "Pin Disable" input signal. This signal, when driven low, causes the N2HET outputs identified by a programmable register (HETPINDIS) to be tri-stated. See the device specific technical reference manual for more details on the "N2HET Pin Disable" feature.

GIOA[5] is connected to the "Pin Disable" input for N2HET1, and GIOB[2] is connected to the "Pin Disable" input for N2HET2.

### 7.4.7 High-End Timer Transfer Unit (HTU)

A High End Timer Transfer Unit (HTU) can perform DMA type transactions to transfer N2HET data to or from main memory. A Memory Protection Unit (MPU) is built into the HTU.

#### 7.4.7.1 Features

- CPU and DMA independent
- Master Port to access system memory
- 8 control packets supporting dual buffer configuration
- Control packet information is stored in RAM protected by parity
- Event synchronization (HET transfer requests)
- Supports 32- or 64-bit transactions
- Addressing modes for HET address (8 byte or 16 byte) and system memory address (fixed, 32 bit or 64 bit)
- One shot, circular and auto switch buffer transfer modes
- Request lost detection

#### 7.4.7.2 Trigger Connections

**Table 7-14. HTU1 Request Line Connection**

| MODULES | REQUEST SOURCE | HTU1 REQUEST |
|---|---|---|
| N2HET1 | HTUREQ[0] | HTU1 DCP[0] |
| N2HET1 | HTUREQ[1] | HTU1 DCP[1] |
| N2HET1 | HTUREQ[2] | HTU1 DCP[2] |
| N2HET1 | HTUREQ[3] | HTU1 DCP[3] |
| N2HET1 | HTUREQ[4] | HTU1 DCP[4] |
| N2HET1 | HTUREQ[5] | HTU1 DCP[5] |
| N2HET1 | HTUREQ[6] | HTU1 DCP[6] |
| N2HET1 | HTUREQ[7] | HTU1 DCP[7] |

**Table 7-15. HTU2 Request Line Connection**

| MODULES | REQUEST SOURCE | HTU2 REQUEST |
|---|---|---|
| N2HET2 | HTUREQ[0] | HTU2 DCP[0] |
| N2HET2 | HTUREQ[1] | HTU2 DCP[1] |
| N2HET2 | HTUREQ[2] | HTU2 DCP[2] |
| N2HET2 | HTUREQ[3] | HTU2 DCP[3] |
| N2HET2 | HTUREQ[4] | HTU2 DCP[4] |
| N2HET2 | HTUREQ[5] | HTU2 DCP[5] |
| N2HET2 | HTUREQ[6] | HTU2 DCP[6] |
| N2HET2 | HTUREQ[7] | HTU2 DCP[7] |


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## 7.5 FlexRay Interface

The FlexRay module performs communication according to the FlexRay protocol specification v2.1. The sample clock bit rate can be programmed to values up to 10 Mbps. Additional bus driver (BD) hardware is required for connection to the physical layer.

For communication on a FlexRay network, individual message buffers with up to 254 data bytes are configurable. The message storage consists of a single-ported message RAM that holds up to 128 message buffers. All functions concerning the handling of messages are implemented in the message handler. Those functions are the acceptance filtering, the transfer of messages between the two FlexRay Channel Protocol Controllers and the message RAM, maintaining the transmission schedule, as well as providing message status information.

The register set of the FlexRay module can be accessed directly by the CPU through the VBUS interface. These registers are used to control, configure, and monitor the FlexRay channel protocol controllers, message handler, global time unit, system universal control, frame/symbol processing, network management, interrupt control, and to access the message RAM through the I/O buffer.

### *7.5.1 Features*

The FlexRay module has the following features:

- Conformance with FlexRay protocol specification v2.1
- Data rates of up to 10 Mbps on each channel
- Up to 128 message buffers
- 8KB of message RAM for storage (for example, 128 message buffers with maximum of 48-byte data section or up to 30 message buffers with 254-byte data section)
- Configuration of message buffers with different payload lengths
- One configurable receive FIFO
- Each message buffer can be configured as receive buffer, as transmit buffer or as part of the receive FIFO.
- CPU access to message buffers through input and output buffer
- FlexRay Transfer Unit (FTU) for automatic data transfer between data memory and message buffers without CPU interaction
- Filtering for slot counter, cycle counter, and channel ID
- Maskable module interrupts
- Supports Network Management

### *7.5.2 Electrical and Timing Specifications*

**Table 7-16. Timing Requirements for FlexRay Inputs**

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{pw}$ | Input minimum pulse width to meet the FlexRay sampling requirement | $t_{c(AVCLK2)}$ + 2.5 (1) | | ns |

(1) $t_{RxAsymDelay}$ parameter

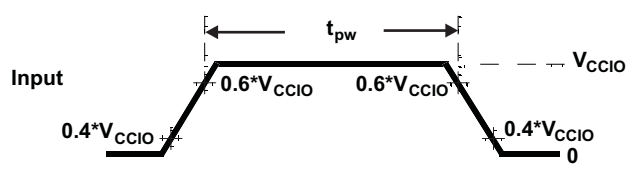


**Figure 7-8. FlexRay Inputs**

**Table 7-17. FlexRay Jitter Timing**

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{Tx1bit}$ | Clock jitter and signal symmetry | 98 | 102 | ns |
| $t_{Tx10bit}$ | FlexRay BSS (byte start sequence) to BSS | 999 | 1001 | ns |
| $t_{Tx10bitAvg}$ | Average over 10,000 samples | 999.5 | 1000.5 | ns |
| $t_{RxAsymDelay}$ | Delay difference between rise and fall from Rx pin to sample point in FlexRay core | – | 2.5 | ns |
| $t_{jit(SCLK)}$ | Jitter for the 80-MHz Sample Clock generated by the PLL | – | 0.5 | ns |

### *7.5.3 FlexRay Transfer Unit*

The FTU can transfer data between the input buffer (IBF) and output buffer (OBF) of the communication controller and the system memory without CPU interaction.

Because the FlexRay module is accessed through the FTU, the FTU must be powered up by setting bit 23 in the Peripheral Power Down Registers of the System Module before accessing any FlexRay module register.

For more information on the FTU, see the TMS570LS31x/TMS570LS21x 16/32-Bit RISC Flash Microcontroller Technical Reference Manual (SPNU499).


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## 7.6 Controller Area Network (DCAN)

The DCAN supports the CAN 2.0B protocol standard and uses a serial, multimaster communication protocol that efficiently supports distributed real-time control with robust communication rates of up to 1 Mbps. The DCAN is ideal for applications operating in noisy and harsh environments (for example, automotive and industrial fields) that require reliable serial communication or multiplexed wiring.

### *7.6.1 Features*

Features of the DCAN module include:

- Supports CAN protocol version 2.0 part A, B
- Bit rates up to 1 Mbps
- The CAN kernel can be clocked by the oscillator for baud-rate generation.
- 64 mailboxes on each DCAN
- Individual identifier mask for each message object
- Programmable FIFO mode for message objects
- Programmable loop-back modes for self-test operation
- Automatic bus on after Bus-Off state by a programmable 32-bit timer
- Message RAM protected by parity
- Direct access to Message RAM during test mode
- CAN Rx / Tx pins configurable as general purpose IO pins
- Message RAM Auto Initialization
- DMA support

For more information on the DCAN, see the TMS570LS31x/21x 16/32-Bit RISC Flash Microcontroller Technical Reference Manual (SPNU499).

### *7.6.2 Electrical and Timing Specifications*

**Table 7-18. Dynamic Characteristics for the DCANx TX and RX Pins**

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{d(CANnTX)}$ | Delay time, transmit shift register to CANnTX pin (1) | | 15 | ns |
| $t_{d(CANnRX)}$ | Delay time, CANnRX pin to receive shift register | | 5 | ns |

(1) These values do not include rise/fall times of the output buffer.

## 7.7 Local Interconnect Network Interface (LIN)

The SCI/LIN module can be programmed to work either as an SCI or as a LIN. The core of the module is an SCI. The hardware features of the SCI are augmented to achieve LIN compatibility.

The SCI module is a universal asynchronous receiver-transmitter that implements the standard nonreturn to zero format. The SCI can be used to communicate, for example, through an RS-232 port or over a K-line.

The LIN standard is based on the SCI (UART) serial data link format. The communication concept is single-master/multiple-slave with a message identification for multicast transmission between any network nodes.

### *7.7.1 LIN Features*

The following are features of the LIN module:

- Compatible to LIN 1.3, 2.0, and 2.1 protocols
- Multibuffered receive and transmit units DMA capability for minimal CPU intervention
- Identification masks for message filtering
- Automatic Master Header Generation
  - Programmable Synch Break Field
  - Synch Field
  - Identifier Field
- Slave Automatic Synchronization
  - Synch break detection
  - Optional baudrate update
  - Synchronization Validation
- $2^{31}$ programmable transmission rates with 7 fractional bits
- Error detection
- 2 Interrupt lines with priority encoding


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## 7.8 Serial Communication Interface (SCI)

### *7.8.1 Features*

- Standard universal asynchronous receiver-transmitter (UART) communication
- Supports full- or half-duplex operation
- Standard nonreturn to zero (NRZ) format
- Double-buffered receive and transmit functions
- Configurable frame format of 3 to 13 bits per character based on the following:
  - Data word length programmable from 1 to 8 bits
  - Additional address bit in address-bit mode
  - Parity programmable for zero or 1 parity bit, odd or even parity
  - Stop programmable for 1 or 2 stop bits
- Asynchronous or isosynchronous communication modes
- Two multiprocessor communication formats allow communication between more than two devices.
- Sleep mode is available to free CPU resources during multiprocessor communication.
- The 24-bit programmable baud rate supports $2^{24}$ different baud rates provide high accuracy baud rate selection.
- Four error flags and five status flags provide detailed information regarding SCI events.
- Capability to use DMA for transmit and receive data.

## 7.9 Inter-Integrated Circuit (I2C)

The inter-integrated circuit (I2C) module is a multimaster communication module providing an interface between the TMS570 microcontroller and devices compliant with Philips Semiconductor I2C-bus specification version 2.1 and connected by an $I^2C$-bus™. This module will support any slave or master I2C compatible device.

### *7.9.1 Features*

The I2C has the following features:

- Compliance to the Philips $I^2C$-bus specification, v2.1 (The I2C Specification, Philips document number 9398 393 40011)
  - Bit/Byte format transfer
  - 7-bit and 10-bit device addressing modes
  - General call
  - START byte
  - Multimaster transmitter/ slave receiver mode
  - Multimaster receiver/ slave transmitter mode
  - Combined master transmit/receive and receive/transmit mode
  - Transfer rates of 10 kbps up to 400 kbps (Phillips fast-mode rate)
- Free data format
- Two DMA events (transmit and receive)
- DMA event enable/disable capability
- Seven interrupts that can be used by the CPU
- Module enable/disable capability
- The SDA and SCL are optionally configurable as general-purpose I/O
- Slew rate control of the outputs
- Open-drain control of the outputs
- Programmable pullup/pulldown capability on the inputs
- Supports Ignore NACK mode

**NOTE**

This I2C module does not support:

- High-speed (HS) mode
- C-bus compatibility mode
- The combined format in 10-bit address mode (the I2C module sends the slave address second byte every time it sends the slave address first byte)


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### 7.9.2 I2C I/O Timing Specifications

**Table 7-19. I2C Signals (SDA and SCL) Switching Characteristics(1)**

| PARAMETER | | STANDARD MODE | | FAST MODE | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $t_{c(I2CCLK)}$ | Cycle time, Internal Module clock for I2C, prescaled from VCLK | 75.2 | 149 | 75.2 | 149 | ns |
| $f_{(SCL)}$ | SCL Clock frequency | 0 | 100 | 0 | 400 | kHz |
| $t_{c(SCL)}$ | Cycle time, SCL | 10 | | 2.5 | | µs |
| $t_{su(SCLH-SDAL)}$ | Setup time, SCL high before SDA low (for a repeated START condition) | 4.7 | | 0.6 | | µs |
| $t_{h(SCLL-SDAL)}$ | Hold time, SCL low after SDA low (for a repeated START condition) | 4 | | 0.6 | | µs |
| $t_{w(SCLL)}$ | Pulse duration, SCL low | 4.7 | | 1.3 | | µs |
| $t_{w(SCLH)}$ | Pulse duration, SCL high | 4 | | 0.6 | | µs |
| $t_{su(SDA-SCLH)}$ | Setup time, SDA valid before SCL high | 250 | | 100 | | ns |
| $t_{h(SDA-SCLL)}$ | Hold time, SDA valid after SCL low (for I2C bus devices) | 0 | 3.45(2) | 0 | 0.9 | µs |
| $t_{w(SDAH)}$ | Pulse duration, SDA high between STOP and START conditions | 4.7 | | 1.3 | | µs |
| $t_{su(SCLH-SDAH)}$ | Setup time, SCL high before SDA high (for STOP condition) | 4.0 | | 0.6 | | µs |
| $t_{w(SP)}$ | Pulse duration, spike (must be suppressed) | | | 0 | 50 | ns |
| $C_b$(3) | Capacitive load for each bus line | | 400 | | 400 | pF |

(1) The I2C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down.
(2) The maximum $t_{h(SDA-SCLL)}$ for I2C bus devices has only to be met if the device does not stretch the low period ($t_{w(SCLL)}$) of the SCL signal.
(3) $C_b$ = The total capacitance of one bus line in pF.

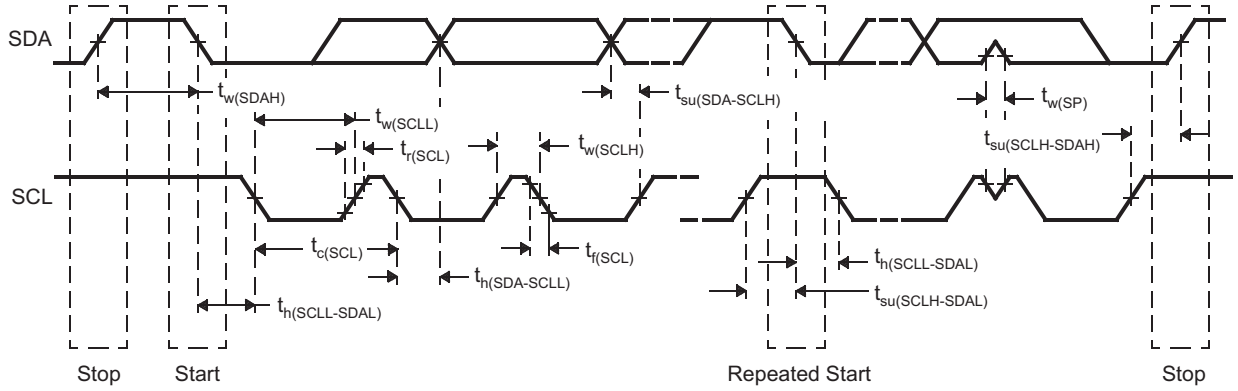


**Figure 7-9. I2C Timings**

**NOTE**

- A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the VIHmin of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- The maximum $t_{h(SDA-SCLL)}$ has only to be met if the device does not stretch the LOW period ($t_{w(SCLL)}$) of the SCL signal.
- A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement $t_{su(SDA-SCLH)} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line tr max + $t_{su(SDA-SCLH)}$.
- $C_b$ = total capacitance of one bus line in pF. If mixed with fast-mode devices, faster fall-times are allowed.


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## 7.10 Multibuffered / Standard Serial Peripheral Interface

The MibSPI is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length (2 to 16 bits) to be shifted in and out of the device at a programmed bit-transfer rate. Typical applications for the SPI include interfacing to external peripherals, such as I/Os, memories, display drivers, and analog-to-digital converters.

### *7.10.1 Features*

Both Standard and MibSPI modules have the following features:

- 16-bit shift register
- Receive buffer register
- 5-bit baud clock generator
- SPICLK can be internally-generated (master mode) or received from an external clock source (slave mode)
- Each word transferred can have a unique format
- SPI I/Os not used in the communication can be used as digital input/output signals

**Table 7-20. MibSPI/SPI Configurations**

| MibSPIx/SPIx | I/Os |
|---|---|
| MibSPI1 | MIBSPI1SIMO[1:0], MIBSPI1SOMI[1:0], MIBSPI1CLK, MIBSPI1nCS[5:0], MIBSPI1nENA |
| MibSPI3 | MIBSPI3SIMO, MIBSPI3SOMI, MIBSPI3CLK, MIBSPI3nCS[5:0], MIBSPI3nENA |
| MibSPI5 | MIBSPI5SIMO[3:0], MIBSPI5SOMI[3:0], MIBSPI5CLK, MIBSPI5nCS[3:0], MIBSPI5nENA |
| SPI2 | SPI2SIMO, SPI2SOMI, SPI2CLK, SPI2nCS[1:0], SPI2nENA |
| SPI4 | SPI4SIMO, SPI4SOMI, SPI4CLK, SPI4nCS[0], SPI4nENA |

### *7.10.2 MibSPI Transmit and Receive RAM Organization*

The Multibuffer RAM is comprised of 128 buffers. Each entry in the Multibuffer RAM consists of 4 parts: a 16-bit transmit field, a 16-bit receive field, a 16-bit control field and a 16-bit status field. The Multibuffer RAM can be partitioned into multiple transfer group with variable number of buffers each.

### *7.10.3 MibSPI Transmit Trigger Events*

Each of the transfer groups can be configured individually. For each of the transfer groups a trigger event and a trigger source can be chosen. A trigger event can be for example a rising edge or a permanent low level at a selectable trigger source. For example, up to 15 trigger sources are available which can be used by each transfer group. These trigger options are listed in Table 7-21 for MIBSPI1, Section 7.10.3.2 for MIBSPI3 and Section 7.10.3.3 for MibSPI5.

#### 7.10.3.1 MIBSPI1 Event Trigger Hookup

**Table 7-21. MIBSPI1 Event Trigger Hookup**

| EVENT # | TGxCTRL TRIGSRC[3:0] | TRIGGER |
|---|---|---|
| Disabled | 0000 | No trigger source |
| EVENT0 | 0001 | GIOA[0] |
| EVENT1 | 0010 | GIOA[1] |
| EVENT2 | 0011 | GIOA[2] |
| EVENT3 | 0100 | GIOA[3] |
| EVENT4 | 0101 | GIOA[4] |
| EVENT5 | 0110 | GIOA[5] |
| EVENT6 | 0111 | GIOA[6] |
| EVENT7 | 1000 | GIOA[7] |
| EVENT8 | 1001 | N2HET1[8] |
| EVENT9 | 1010 | N2HET1[10] |
| EVENT10 | 1011 | N2HET1[12] |
| EVENT11 | 1100 | N2HET1[14] |
| EVENT12 | 1101 | N2HET1[16] |
| EVENT13 | 1110 | N2HET1[18] |
| EVENT14 | 1111 | Internal Tick counter |

**NOTE**

For N2HET1 trigger sources, the connection to the MibSPI1 module trigger input is made from the input side of the output buffer (at the N2HET1 module boundary). This way, a trigger condition can be generated even if the N2HET1 signal is not selected to be output on the pad.

**NOTE**

For GIOx trigger sources, the connection to the MibSPI1 module trigger input is made from the output side of the input buffer. This way, a trigger condition can be generated either by selecting the GIOx pin as an output pin plus selecting the pin to be a GIOx pin, or by driving the GIOx pin from an external trigger source. If the mux control module is used to select different functionality instead of the GIOx signal, then care must be taken to disable GIOx from triggering MibSPI1 transfers; there is no multiplexing on the input connections.

#### 7.10.3.2 MIBSPI3 Event Trigger Hookup

**Table 7-22. MIBSPI3 Event Trigger Hookup**

| EVENT # | TGxCTRL TRIGSRC[3:0] | TRIGGER |
|---|---|---|
| Disabled | 0000 | No trigger source |
| EVENT0 | 0001 | GIOA[0] |
| EVENT1 | 0010 | GIOA[1] |
| EVENT2 | 0011 | GIOA[2] |
| EVENT3 | 0100 | GIOA[3] |
| EVENT4 | 0101 | GIOA[4] |
| EVENT5 | 0110 | GIOA[5] |
| EVENT6 | 0111 | GIOA[6] |
| EVENT7 | 1000 | GIOA[7] |
| EVENT8 | 1001 | HET[8] |
| EVENT9 | 1010 | N2HET1[10] |


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**Table 7-22. MIBSPI3 Event Trigger Hookup (continued)**

| EVENT # | TGxCTRL TRIGSRC[3:0] | TRIGGER |
|---|---|---|
| EVENT10 | 1011 | N2HET1[12] |
| EVENT11 | 1100 | N2HET1[14] |
| EVENT12 | 1101 | N2HET1[16] |
| EVENT13 | 1110 | N2HET1[18] |
| EVENT14 | 1111 | Internal Tick counter |

**NOTE**

For N2HET1 trigger sources, the connection to the MibSPI3 module trigger input is made from the input side of the output buffer (at the N2HET1 module boundary). This way, a trigger condition can be generated even if the N2HET1 signal is not selected to be output on the pad.

**NOTE**

For GIOx trigger sources, the connection to the MibSPI3 module trigger input is made from the output side of the input buffer. This way, a trigger condition can be generated either by selecting the GIOx pin as an output pin plus selecting the pin to be a GIOx pin, or by driving the GIOx pin from an external trigger source. If the mux control module is used to select different functionality instead of the GIOx signal, then care must be taken to disable GIOx from triggering MibSPI3 transfers; there is no multiplexing on the input connections.

### 7.10.3.3 MIBSPI5 Event Trigger Hookup

**Table 7-23. MIBSPI5 Event Trigger Hookup**

| EVENT # | TGxCTRL TRIGSRC[3:0] | TRIGGER |
|---|---|---|
| Disabled | 0000 | No trigger source |
| EVENT0 | 0001 | GIOA[0] |
| EVENT1 | 0010 | GIOA[1] |
| EVENT2 | 0011 | GIOA[2] |
| EVENT3 | 0100 | GIOA[3] |
| EVENT4 | 0101 | GIOA[4] |
| EVENT5 | 0110 | GIOA[5] |
| EVENT6 | 0111 | GIOA[6] |
| EVENT7 | 1000 | GIOA[7] |
| EVENT8 | 1001 | N2HET1[8] |
| EVENT9 | 1010 | N2HET1[10] |
| EVENT10 | 1011 | N2HET1[12] |
| EVENT11 | 1100 | N2HET1[14] |
| EVENT12 | 1101 | N2HET1[16] |
| EVENT13 | 1110 | N2HET1[18] |
| EVENT14 | 1111 | Internal Tick counter |

**NOTE**

For N2HET1 trigger sources, the connection to the MibSPI5 module trigger input is made from the input side of the output buffer (at the N2HET1 module boundary). This way, a trigger condition can be generated even if the N2HET1 signal is not selected to be output on the pad.

**NOTE**

For GIOx trigger sources, the connection to the MibSPI5 module trigger input is made from the output side of the input buffer. This way, a trigger condition can be generated either by selecting the GIOx pin as an output pin + selecting the pin to be a GIOx pin, or by driving the GIOx pin from an external trigger source. If the mux control module is used to select different functionality instead of the GIOx signal, then care must be taken to disable GIOx from triggering MibSPI5 transfers; there is no multiplexing on the input connections.


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### 7.10.4 MibSPI/SPI Master Mode I/O Timing Specifications

**Table 7-24. SPI Master Mode External Timing Parameters (CLOCK PHASE = 0, SPICLK = output, SPISIMO = output, and SPISOMI = input)(1)(2)(3)**

| NO. | PARAMETER | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| 1 | $t_{c(SPC)M}$ | Cycle time, SPICLK(4) | | 40 | $256t_{c(VCLK)}$ | ns |
| 2(5) | $t_{w(SPCH)M}$ | Pulse duration, SPICLK high (clock polarity = 0) | | $0.5t_{c(SPC)M} – t_{r(SPC)M} – 3$ | $0.5t_{c(SPC)M} + 3$ | ns |
| | $t_{w(SPCL)M}$ | Pulse duration, SPICLK low (clock polarity = 1) | | $0.5t_{c(SPC)M} – t_{f(SPC)M} – 3$ | $0.5t_{c(SPC)M} + 3$ | |
| 3(5) | $t_{w(SPCL)M}$ | Pulse duration, SPICLK low (clock polarity = 0) | | $0.5t_{c(SPC)M} – t_{f(SPC)M} – 3$ | $0.5t_{c(SPC)M} + 3$ | ns |
| | $t_{w(SPCH)M}$ | Pulse duration, SPICLK high (clock polarity = 1) | | $0.5t_{c(SPC)M} – t_{r(SPC)M} – 3$ | $0.5t_{c(SPC)M} + 3$ | |
| 4(5) | $t_{d(SPCH-SIMO)M}$ | Delay time, SPISIMO valid before SPICLK low (clock polarity = 0) | | $0.5t_{c(SPC)M} – 6$ | | ns |
| | $t_{d(SPCL-SIMO)M}$ | Delay time, SPISIMO valid before SPICLK high (clock polarity = 1) | | $0.5t_{c(SPC)M} – 6$ | | |
| 5(5) | $t_{v(SPCL-SIMO)M}$ | Valid time, SPISIMO data valid after SPICLK low (clock polarity = 0) | | $0.5t_{c(SPC)M} – t_{f(SPC)} – 4$ | | ns |
| | $t_{v(SPCH-SIMO)M}$ | Valid time, SPISIMO data valid after SPICLK high (clock polarity = 1) | | $0.5t_{c(SPC)M} – t_{r(SPC)} – 4$ | | |
| 6(5) | $t_{su(SOMI-SPCL)M}$ | Setup time, SPISOMI before SPICLK low (clock polarity = 0) | | $t_{f(SPC)} + 2.2$ | | ns |
| | $t_{su(SOMI-SPCH)M}$ | Setup time, SPISOMI before SPICLK high (clock polarity = 1) | | $t_{r(SPC)} + 2.2$ | | |
| 7(5) | $t_{h(SPCL-SOMI)M}$ | Hold time, SPISOMI data valid after SPICLK low (clock polarity = 0) | | 10 | | ns |
| | $t_{h(SPCH-SOMI)M}$ | Hold time, SPISOMI data valid after SPICLK high (clock polarity = 1) | | 10 | | |
| 8(6) | $t_{C2TDELAY}$ | Setup time CS active until SPICLK high (clock polarity = 0) | CSHOLD = 0 | $C2TDELAY*t_{c(VCLK)} + 2*t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} – 7$ | $(C2TDELAY+2) * t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} + 5.5$ | ns |
| | | | CSHOLD = 1 | $C2TDELAY*t_{c(VCLK)} + 3*t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} – 7$ | $(C2TDELAY+3) * t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} + 5.5$ | |
| | | Setup time CS active until SPICLK low (clock polarity = 1) | CSHOLD = 0 | $C2TDELAY*t_{c(VCLK)} + 2*t_{c(VCLK)} - t_{f(SPICS)} + t_{f(SPC)} – 7$ | $(C2TDELAY+2) * t_{c(VCLK)} - t_{f(SPICS)} + t_{f(SPC)} + 5.5$ | |
| | | | CSHOLD = 1 | $C2TDELAY*t_{c(VCLK)} + 3*t_{c(VCLK)} - t_{f(SPICS)} + t_{f(SPC)} – 7$ | $(C2TDELAY+3) * t_{c(VCLK)} - t_{f(SPICS)} + t_{f(SPC)} + 5.5$ | |
| 9(6) | $t_{T2CDELAY}$ | Hold time SPICLK low until CS inactive (clock polarity = 0) | | $0.5*t_{c(SPC)M} + T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{f(SPC)} + t_{r(SPICS)} - 7$ | $0.5*t_{c(SPC)M} + T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{f(SPC)} + t_{r(SPICS)} + 11$ | ns |
| | | Hold time SPICLK high until CS inactive (clock polarity = 1) | | $0.5*t_{c(SPC)M} + T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{r(SPC)} + tr(SPICS) - 7$ | $0.5*t_{c(SPC)M} + T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{r(SPC)} + t_{r(SPICS)} + 11$ | |
| 10 | $t_{SPIENA}$ | SPIENAn Sample point | | $(C2TDELAY+1) * t_{c(VCLK)} - t_{f(SPICS)} – 29$ | $(C2TDELAY+1)*t_{c(VCLK)}$ | ns |
| 11 | $t_{SPIENAW}$ | SPIENAn Sample point from write to buffer | | | $(C2TDELAY+2)*t_{c(VCLK)}$ | ns |

(1) The MASTER bit (SPIGCR1.0) is set and the CLOCK PHASE bit (SPIFMTx.16) is cleared.
(2) $t_{c(VCLK)}$ = interface clock cycle time = 1 / $f_{(VCLK)}$
(3) For rise and fall timings, see Table 5-7.
(4) When the SPI is in Master mode, the following must be true:
For PS values from 1 to 255: $t_{c(SPC)M} \geq (PS +1)t_{c(VCLK)} \geq 40ns$, where PS is the prescale value set in the SPIFMTx.[15:8] register bits.
For PS values of 0: $t_{c(SPC)M} = 2t_{c(VCLK)} \geq 40ns$.
The external load on the SPICLK pin must be less than 60pF.
(5) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).
(6) C2TDELAY and T2CDELAY is programmed in the SPIDELAY register

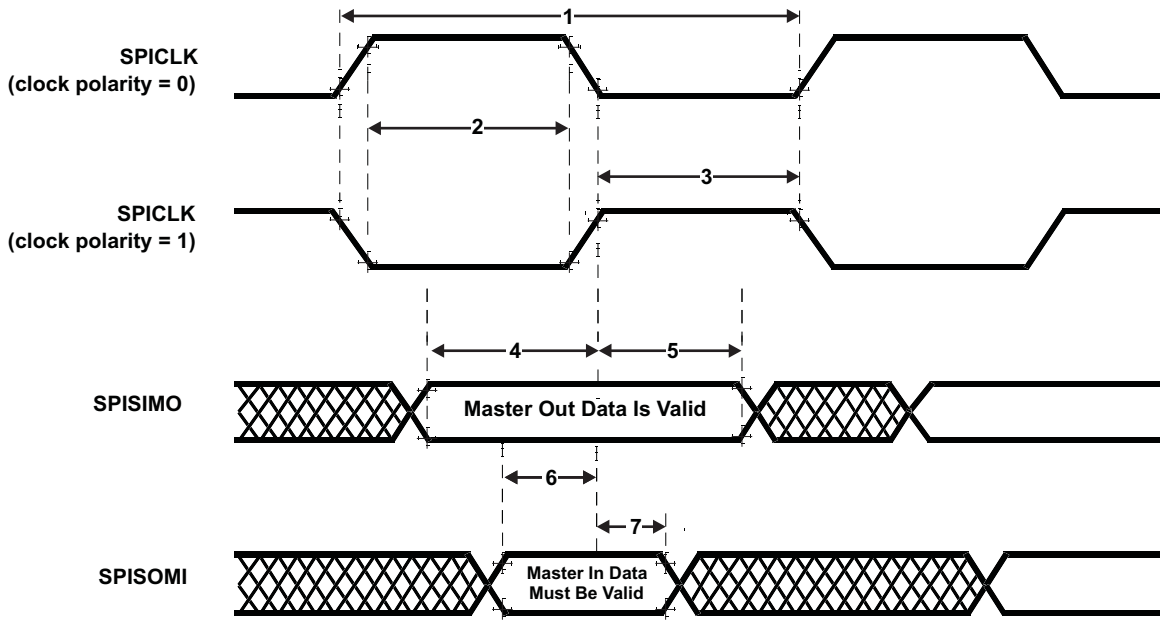


**Figure 7-10. SPI Master Mode External Timing (CLOCK PHASE = 0)**

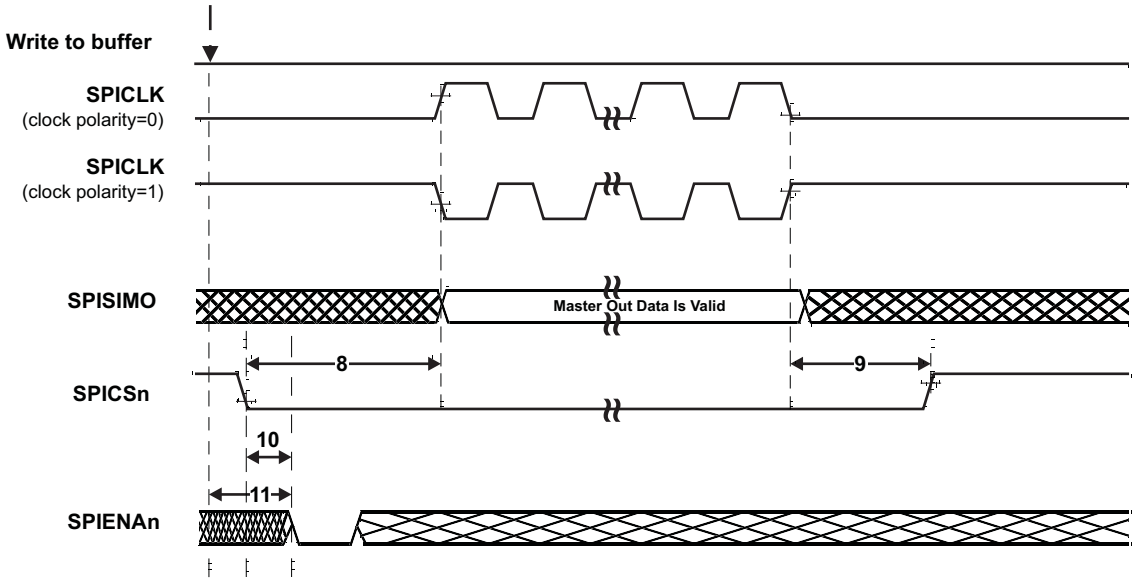


**Figure 7-11. SPI Master Mode Chip Select Timing (CLOCK PHASE = 0)**


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### Table 7-25. SPI Master Mode External Timing Parameters (CLOCK PHASE = 1, SPICLK = output, SPISIMO = output, and SPISOMI = input)(1)(2)(3)

| NO. | PARAMETER | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| 1 | $t_{c(SPC)M}$ | Cycle time, SPICLK (4) | | 40 | $256t_{c(VCLK)}$ | ns |
| 2(5) | $t_{w(SPCH)M}$ | Pulse duration, SPICLK high (clock polarity = 0) | | $0.5t_{c(SPC)M} – t_{r(SPC)M} – 3$ | $0.5t_{c(SPC)M} + 3$ | ns |
| | $t_{w(SPCL)M}$ | Pulse duration, SPICLK low (clock polarity = 1) | | $0.5t_{c(SPC)M} – t_{f(SPC)M} – 3$ | $0.5t_{c(SPC)M} + 3$ | |
| 3(5) | $t_{w(SPCL)M}$ | Pulse duration, SPICLK low (clock polarity = 0) | | $0.5t_{c(SPC)M} – t_{f(SPC)M} – 3$ | $0.5t_{c(SPC)M} + 3$ | ns |
| | $t_{w(SPCH)M}$ | Pulse duration, SPICLK high (clock polarity = 1) | | $0.5t_{c(SPC)M} – t_{r(SPC)M} – 3$ | $0.5t_{c(SPC)M} + 3$ | |
| 4(5) | $t_{v(SIMO-SPCH)M}$ | Valid time, SPICLK high after SPISIMO data valid (clock polarity = 0) | | $0.5t_{c(SPC)M} – 6$ | | ns |
| | $t_{v(SIMO-SPCL)M}$ | Valid time, SPICLK low after SPISIMO data valid (clock polarity = 1) | | $0.5t_{c(SPC)M} – 6$ | | |
| 5(5) | $t_{v(SPCH-SIMO)M}$ | Valid time, SPISIMO data valid after SPICLK high (clock polarity = 0) | | $0.5t_{c(SPC)M} – t_{r(SPC)} – 4$ | | ns |
| | $t_{v(SPCL-SIMO)M}$ | Valid time, SPISIMO data valid after SPICLK low (clock polarity = 1) | | $0.5t_{c(SPC)M} – t_{f(SPC)} – 4$ | | |
| 6(5) | $t_{su(SOMI-SPCH)M}$ | Setup time, SPISOMI before SPICLK high (clock polarity = 0) | | $t_{r(SPC)} + 2.2$ | | ns |
| | $t_{su(SOMI-SPCL)M}$ | Setup time, SPISOMI before SPICLK low (clock polarity = 1) | | $t_{f(SPC)} + 2.2$ | | |
| 7(5) | $t_{v(SPCH-SOMI)M}$ | Valid time, SPISOMI data valid after SPICLK high (clock polarity = 0) | | 10 | | ns |
| | $t_{v(SPCL-SOMI)M}$ | Valid time, SPISOMI data valid after SPICLK low (clock polarity = 1) | | 10 | | |
| 8(6) | $t_{C2TDELAY}$ | Setup time CS active until SPICLK high (clock polarity = 0) | CSHOLD = 0 | $0.5*t_{c(SPC)M} + (C2TDELAY+2) * t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} – 7$ | $0.5*t_{c(SPC)M} + (C2TDELAY+2) * t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} + 5.5$ | ns |
| | | | CSHOLD = 1 | $0.5*t_{c(SPC)M} + (C2TDELAY+3) * t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} – 7$ | $0.5*t_{c(SPC)M} + (C2TDELAY+3) * t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} + 5.5$ | |
| | | Setup time CS active until SPICLK low (clock polarity = 1) | CSHOLD = 0 | $0.5*t_{c(SPC)M} + (C2TDELAY+2) * t_{c(VCLK)} - t_{f(SPICS)} + t_{f(SPC)} – 7$ | $0.5*t_{c(SPC)M} + (C2TDELAY+2) * t_{c(VCLK)} - t_{f(SPICS)} + t_{f(SPC)} + 5.5$ | |
| | | | CSHOLD = 1 | $0.5*t_{c(SPC)M} + (C2TDELAY+3) * t_{c(VCLK)} - t_{f(SPICS)} + t_{f(SPC)} – 7$ | $0.5*t_{c(SPC)M} + (C2TDELAY+3) * t_{c(VCLK)} - t_{f(SPICS)} + t_{f(SPC)} + 5.5$ | |
| 9(6) | $t_{T2CDELAY}$ | Hold time SPICLK low until CS inactive (clock polarity = 0) | | $T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{f(SPC)} + t_{r(SPICS)} - 7$ | $T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{f(SPC)} + t_{r(SPICS)} + 11$ | ns |
| | | Hold time SPICLK high until CS inactive (clock polarity = 1) | | $T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{r(SPC)} + t_{r(SPICS)} - 7$ | $T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{r(SPC)} + t_{r(SPICS)} + 11$ | |
| 10 | $t_{SPIENA}$ | SPIENAn Sample Point | | $(C2TDELAY+1)* t_{c(VCLK)} - t_{f(SPICS)} – 29$ | $(C2TDELAY+1)*t_{c(VCLK)}$ | ns |
| 11 | $t_{SPIENAW}$ | SPIENAn Sample point from write to buffer | | | $(C2TDELAY+2)*t_{c(VCLK)}$ | ns |

(1) The MASTER bit (SPIGCR1.0) is set and the CLOCK PHASE bit (SPIFMTx.16) is set.
(2) $t_{c(VCLK)}$ = interface clock cycle time = 1 / $f_{(VCLK)}$
(3) For rise and fall timings, see the Table 5-7.
(4) When the SPI is in Master mode, the following must be true:
For PS values from 1 to 255: $t_{c(SPC)M} \geq (PS +1)t_{c(VCLK)} \geq 40ns$, where PS is the prescale value set in the SPIFMTx.[15:8] register bits.
For PS values of 0: $t_{c(SPC)M} = 2t_{c(VCLK)} \geq 40ns$.
The external load on the SPICLK pin must be less than 60pF.
(5) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).
(6) C2TDELAY and T2CDELAY is programmed in the SPIDELAY register

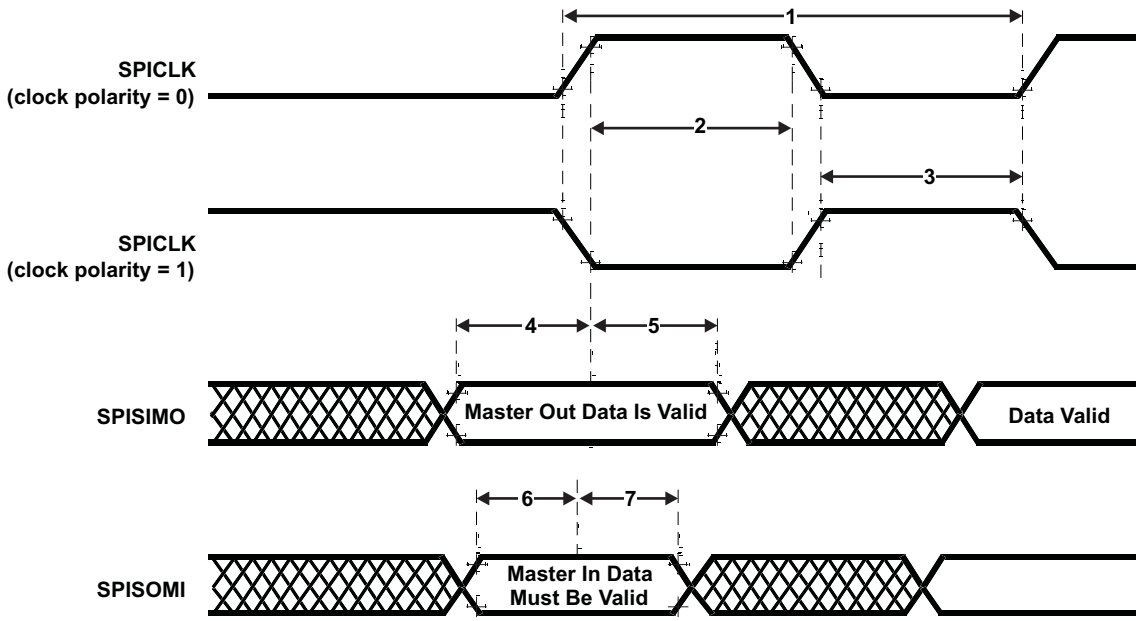


**Figure 7-12. SPI Master Mode External Timing (CLOCK PHASE = 1)**

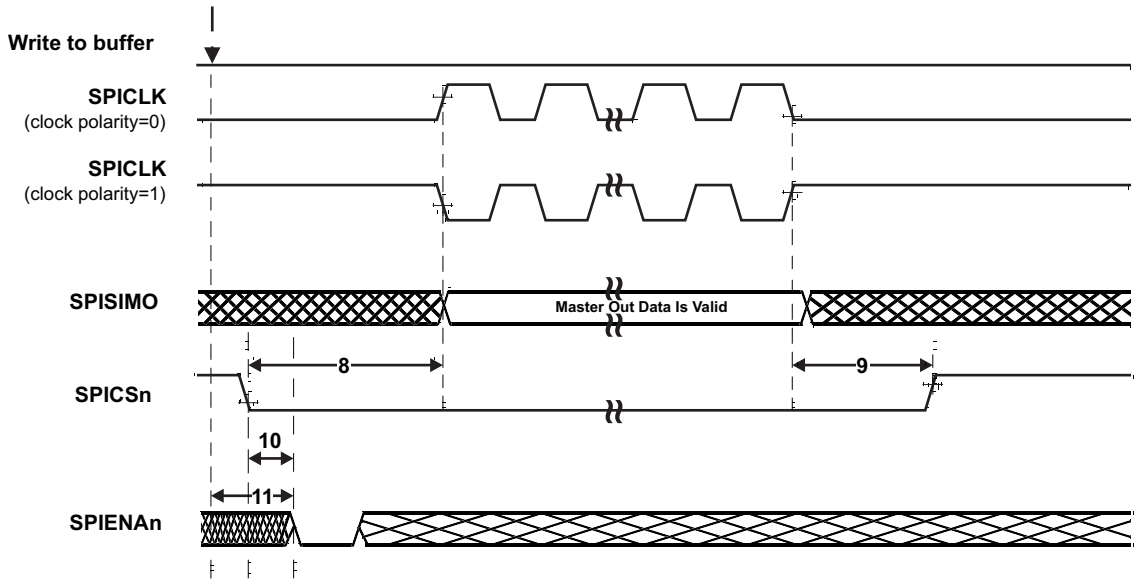


**Figure 7-13. SPI Master Mode Chip Select Timing (CLOCK PHASE = 1)**


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### 7.10.5 SPI Slave Mode I/O Timings

**Table 7-26. SPI Slave Mode External Timing Parameters (CLOCK PHASE = 0, SPICLK = input, SPISIMO = input, and SPISOMI = output)(1)(2)(3)(4)**

| NO. | PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{c(SPC)S}$ | Cycle time, SPICLK(5) | 40 | | ns |
| 2(6) | $t_{w(SPCH)S}$ | Pulse duration, SPICLK high (clock polarity = 0) | 14 | | ns |
| | $t_{w(SPCL)S}$ | Pulse duration, SPICLK low (clock polarity = 1) | 14 | | |
| 3(6) | $t_{w(SPCL)S}$ | Pulse duration, SPICLK low (clock polarity = 0) | 14 | | ns |
| | $t_{w(SPCH)S}$ | Pulse duration, SPICLK high (clock polarity = 1) | 14 | | |
| 4(6) | $t_{d(SPCH-SOMI)S}$ | Delay time, SPISOMI valid after SPICLK high (clock polarity = 0) | | $t_{rf(SOMI)}$ + 20 | ns |
| | $t_{d(SPCL-SOMI)S}$ | Delay time, SPISOMI valid after SPICLK low (clock polarity = 1) | | $t_{rf(SOMI)}$ + 20 | |
| 5(6) | $t_{h(SPCH-SOMI)S}$ | Hold time, SPISOMI data valid after SPICLK high (clock polarity =0) | 2 | | ns |
| | $t_{h(SPCL-SOMI)S}$ | Hold time, SPISOMI data valid after SPICLK low (clock polarity =1) | 2 | | |
| 6(6) | $t_{su(SIMO-SPCL)S}$ | Setup time, SPISIMO before SPICLK low (clock polarity = 0) | 4 | | ns |
| | $t_{su(SIMO-SPCH)S}$ | Setup time, SPISIMO before SPICLK high (clock polarity = 1) | 4 | | |
| 7(6) | $t_{h(SPCL-SIMO)S}$ | Hold time, SPISIMO data valid after SPICLK low (clock polarity = 0) | 2 | | ns |
| | $t_{h(SPCH-SIMO)S}$ | Hold time, SPISIMO data valid after S PICLK high (clock polarity = 1) | 2 | | |
| 8 | $t_{d(SPCL-SENAH)S}$ | Delay time, SPIENAn high after last SPICLK low (clock polarity = 0) | $1.5t_{c(VCLK)}$ | $2.5t_{c(VCLK)}+t_{r(ENAn)}+22$ | ns |
| | $t_{d(SPCH-SENAH)S}$ | Delay time, SPIENAn high after last SPICLK high (clock polarity = 1) | $1.5t_{c(VCLK)}$ | $2.5t_{c(VCLK)}+ t_{r(ENAn)} + 22$ | |
| 9 | $t_{d(SCSL-SENAL)S}$ | Delay time, SPIENAn low after SPICSn low (if new data has been written to the SPI buffer) | $t_{f(ENAn)}$ | $t_{c(VCLK)}+t_{f(ENAn)}+27$ | ns |

(1) The MASTER bit (SPIGCR1.0) is cleared and the CLOCK PHASE bit (SPIFMTx.16) is cleared.
(2) If the SPI is in slave mode, the following must be true: $t_{c(SPC)S} \geq (PS + 1)\ t_{c(VCLK)}$, where PS = prescale value set in SPIFMTx.[15:8].
(3) For rise and fall timings, see Table 5-7.
(4) $t_{c(VCLK)}$ = interface clock cycle time = 1 /$f_{(VCLK)}$
(5) When the SPI is in Slave mode, the following must be true:
For PS values from 1 to 255: $t_{c(SPC)S} \geq (PS +1)t_{c(VCLK)} \geq 40$ns, where PS is the prescale value set in the SPIFMTx.[15:8] register bits.
For PS values of 0: $t_{c(SPC)S} = 2t_{c(VCLK)} \geq 40$ns.
(6) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).

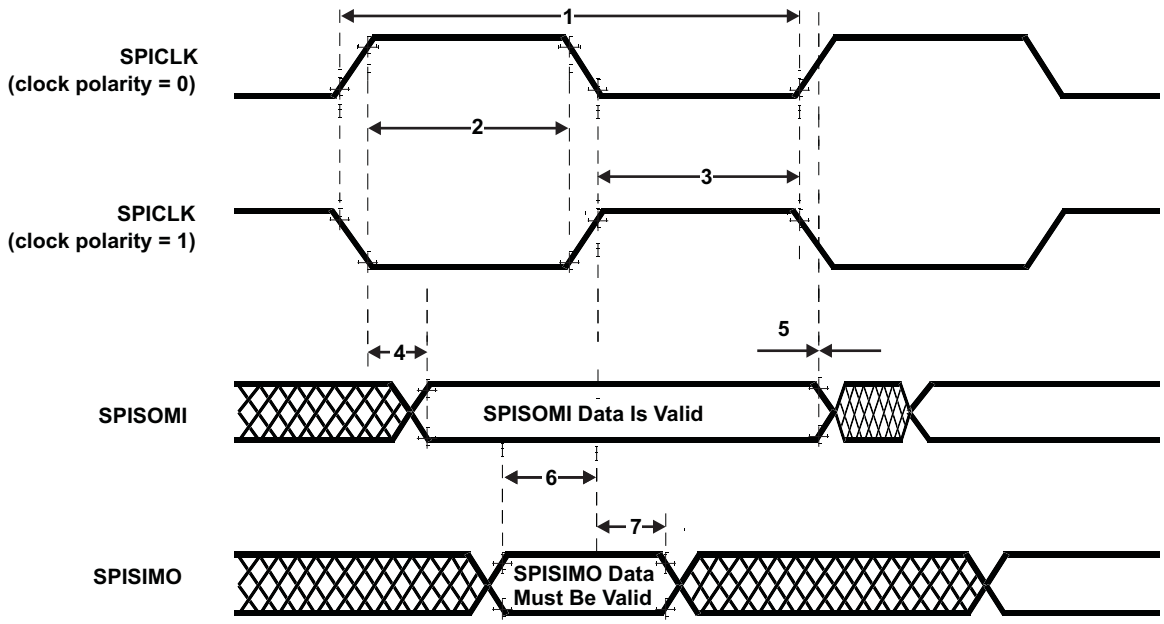


**Figure 7-14. SPI Slave Mode External Timing (CLOCK PHASE = 0)**

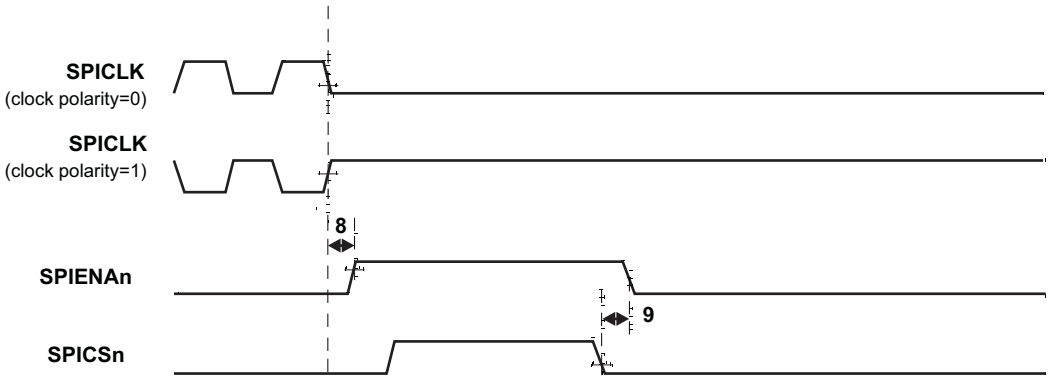


**Figure 7-15. SPI Slave Mode Enable Timing (CLOCK PHASE = 0)**


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### Table 7-27. SPI Slave Mode External Timing Parameters (CLOCK PHASE = 1, SPICLK = input, SPISIMO = input, and SPISOMI = output)(1)(2)(3)(4)

| NO. | PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{c(SPC)S}$ | Cycle time, SPICLK(5) | 40 | | ns |
| 2(6) | $t_{w(SPCH)S}$ | Pulse duration, SPICLK high (clock polarity = 0) | 14 | | ns |
| | $t_{w(SPCL)S}$ | Pulse duration, SPICLK low (clock polarity = 1) | 14 | | |
| 3(6) | $t_{w(SPCL)S}$ | Pulse duration, SPICLK low (clock polarity = 0) | 14 | | ns |
| | $t_{w(SPCH)S}$ | Pulse duration, SPICLK high (clock polarity = 1) | 14 | | |
| 4(6) | $t_{d(SOMI-SPCL)S}$ | Dealy time, SPISOMI data valid after SPICLK low (clock polarity = 0) | | $t_{rf(SOMI)}$ + 20 | ns |
| | $t_{d(SOMI-SPCH)S}$ | Delay time, SPISOMI data valid after SPICLK high (clock polarity = 1) | | $t_{rf(SOMI)}$ + 20 | |
| 5(6) | $t_{h(SPCL-SOMI)S}$ | Hold time, SPISOMI data valid after SPICLK high (clock polarity =0) | 2 | | ns |
| | $t_{h(SPCH-SOMI)S}$ | Hold time, SPISOMI data valid after SPICLK low (clock polarity =1) | 2 | | |
| 6(6) | $t_{su(SIMO-SPCH)S}$ | Setup time, SPISIMO before SPICLK high (clock polarity = 0) | 4 | | ns |
| | $t_{su(SIMO-SPCL)S}$ | Setup time, SPISIMO before SPICLK low (clock polarity = 1) | 4 | | |
| 7(6) | $t_{v(SPCH-SIMO)S}$ | High time, SPISIMO data valid after SPICLK high (clock polarity = 0) | 2 | | ns |
| | $t_{v(SPCL-SIMO)S}$ | High time, SPISIMO data valid after SPICLK low (clock polarity = 1) | 2 | | |
| 8 | $t_{d(SPCH-SENAH)S}$ | Delay time, SPIENAn high after last SPICLK high (clock polarity = 0) | $1.5t_{c(VCLK)}$ | $2.5t_{c(VCLK)}+t_{r(ENAn)}$ + 22 | ns |
| | $t_{d(SPCL-SENAH)S}$ | Delay time, SPIENAn high after last SPICLK low (clock polarity = 1) | $1.5t_{c(VCLK)}$ | $2.5t_{c(VCLK)}+t_{r(ENAn)}$ + 22 | |
| 9 | $t_{d(SCSL-SENAL)S}$ | Delay time, SPIENAn low after SPICSn low (if new data has been written to the SPI buffer) | $t_{f(ENAn)}$ | $t_{c(VCLK)}+t_{f(ENAn)}$+ 27 | ns |
| 10 | $t_{d(SCSL-SOMI)S}$ | Delay time, SOMI valid after SPICSn low (if new data has been written to the SPI buffer) | $t_{c(VCLK)}$ | $2t_{c(VCLK)}+t_{rf(SOMI)}$+ 28 | ns |

(1) The MASTER bit (SPIGCR1.0) is cleared and the CLOCK PHASE bit (SPIFMTx.16) is set.
(2) If the SPI is in slave mode, the following must be true: tc(SPC)S ≤ (PS + 1) tc(VCLK), where PS = prescale value set in SPIFMTx.[15:8].
(3) For rise and fall timings, see Table 5-7.
(4) $t_{c(VCLK)}$ = interface clock cycle time = 1 /$f_{(VCLK)}$
(5) When the SPI is in Slave mode, the following must be true:
For PS values from 1 to 255: $t_{c(SPC)S} \geq (PS + 1)t_{c(VCLK)} \geq 40ns$, where PS is the prescale value set in the SPIFMTx.[15:8] register bits.
For PS values of 0: $t_{c(SPC)S} = 2t_{c(VCLK)} \geq 40ns$.
(6) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).

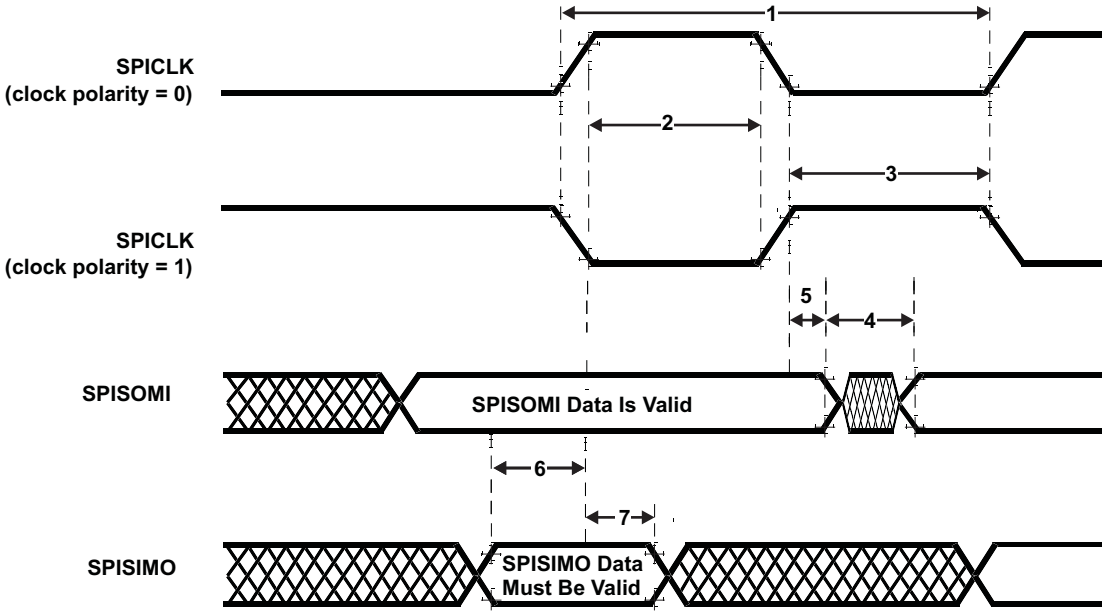


**Figure 7-16. SPI Slave Mode External Timing (CLOCK PHASE = 1)**

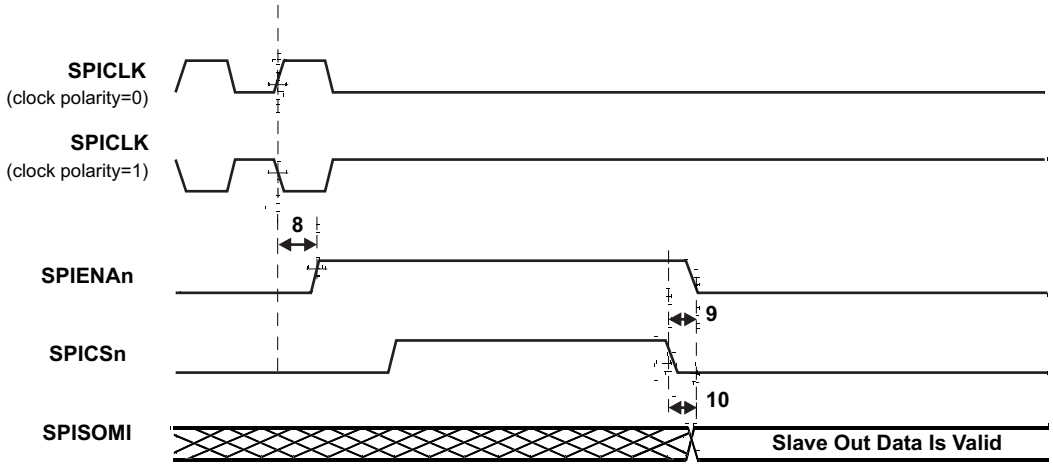


**Figure 7-17. SPI Slave Mode Enable Timing (CLOCK PHASE = 1)**


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## 7.11 Ethernet Media Access Controller

The Ethernet Media Access Controller (EMAC) provides an efficient interface between the CPU and the network. The EMAC supports both 10Base-T and 100Base-TX, or 10 Mbits/second (Mbps) and 100 Mbps in either half- or full-duplex mode, with hardware flow control and quality of service (QoS) support.

The EMAC controls the flow of packet data from the TMS570 device to the PHY. The MDIO module controls PHY configuration and status monitoring.

Both the EMAC and the MDIO modules interface to the TMS570 device through a custom interface that allows efficient data transmission and reception. This custom interface is referred to as the EMAC control module, and is considered integral to the EMAC/MDIO peripheral. The control module is also used to multiplex and control interrupts.

### *7.11.1 Ethernet MII Electrical and Timing Specifications*

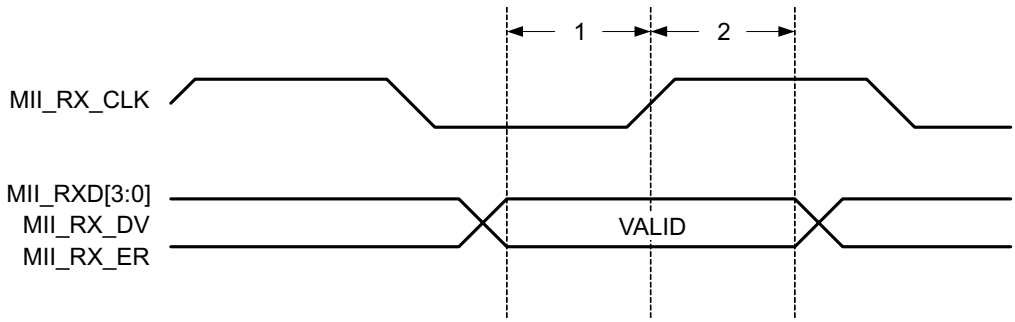


**Figure 7-18. MII Receive Timing**

**Table 7-28. Timing Requirements for EMAC MII Receive**

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{su(MIIRXD - MIIRXCLKH)}$ | Setup time, MII_RXD[3:0] before MII_RX_CLK rising edge | 8 | | ns |
| | $t_{su(MIIRXDV - MIIRXCLKH)}$ | Setup time, MII_RX_DV before MII_RX_CLK rising edge | 8 | | ns |
| | $t_{su(MIIRXER - MIIRXCLKH)}$ | Setup time, MII_RX_ER before MII_RX_CLK rising edge | 8 | | ns |
| 2 | $t_{h(MIIRXCLKH - MIIRXD)}$ | Hold time, MII_RXD[3:0] valid after MII_RX_CLK rising edge | 8 | | ns |
| | $t_{h(MIIRXCLKH - MIIRXDV)}$ | Hold time, MII_RX_DV valid after MII_RX_CLK rising edge | 8 | | ns |
| | $t_{h(MIIRXCLKH - MIIRXER)}$ | Hold time, MII_RX_ER valid after MII_RX_CLK rising edge | 8 | | ns |

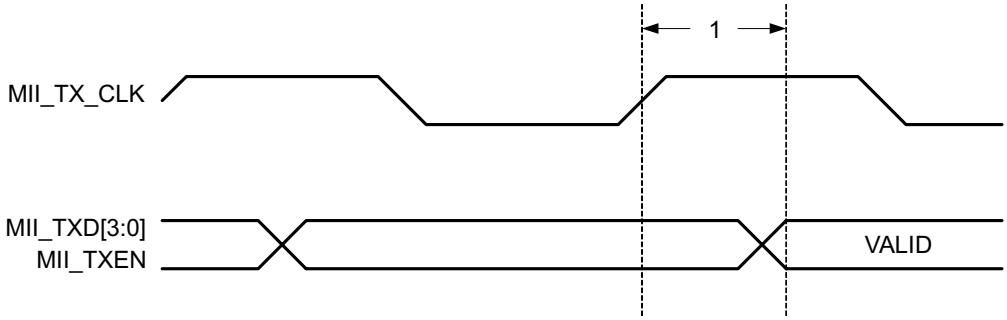


**Figure 7-19. MII Transmit Timing**

**Table 7-29. Switching Characteristics Over Recommended Operating Conditions for EMAC MII Transmit**

| NO. | PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{d(MIIRXCLKH - MIITXD)}$ | Delay time, MII_TX_CLK rising edge to MII_TXD[3:0] valid | 5 | 25 | ns |
| | $t_{d(MIIRXCLKH - MIITXEN)}$ | Delay time, MII_TX_CLK rising edge to MII_TXEN valid | 5 | 25 | ns |


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### 7.11.2 Ethernet RMII Electrical and Timing Specifications

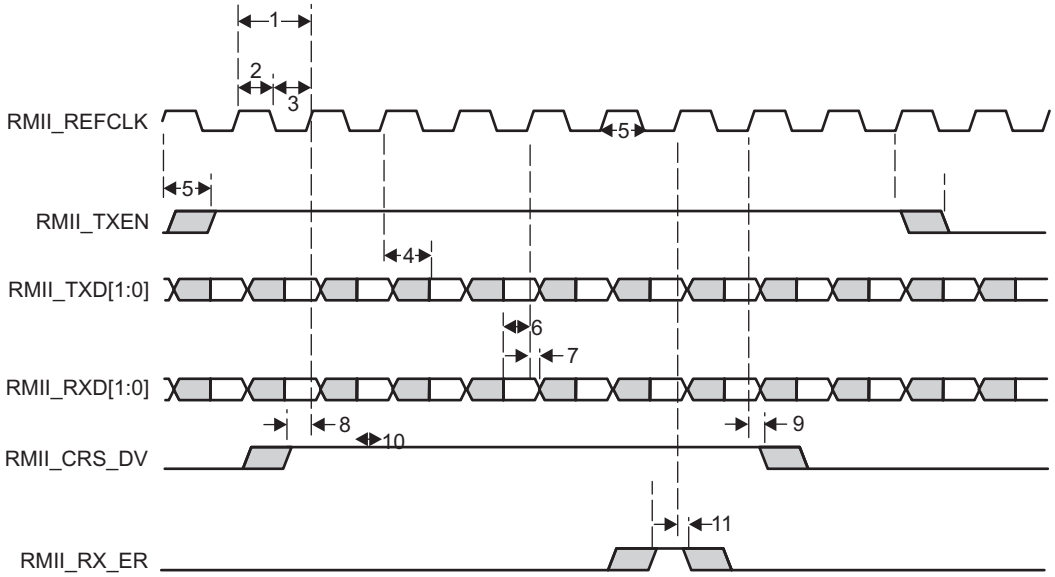


**Figure 7-20. RMII Timing Diagram**

**Table 7-30. Timing Requirements for EMAC RMII Receive and RMII_REFCLK**

| NO. | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| 1 | $t_{c(REFCLK)}$ | Cycle time, RMII_REFCLK | | 20 | | ns |
| 2 | $t_{w(REFCLKH)}$ | Pulse width, RMII_REFCLK high | 7 | | 13 | ns |
| 3 | $t_{w(REFCLKL)}$ | Pulse width, RMII_REFCLK low | 7 | | 13 | ns |
| 6 | $t_{su(RXD-REFCLK)}$ | Input setup time, RMII_RXD[1:0] valid before RMII_REFCLK high | 4 | | | ns |
| 7 | $t_{h(REFCLK-RXD)}$ | Input hold time, RMII_RXD[1:0] valid after RMII_REFCLK high | 2 | | | ns |
| 8 | $t_{su(CRSDV-REFCLK)}$ | Input setup time, RMII_CRS_DV valid before RMII_REFCLK high | 4 | | | ns |
| 9 | $t_{h(REFCLK-CRSDV)}$ | Input hold time, RMII_CRS_DV valid after RMII_REFCLK high | 2 | | | ns |
| 10 | $t_{su(RXER-REFCLK)}$ | Input setup time, RMII_RX_ER valid before RMII_REFCLK high | 4 | | | ns |
| 11 | $t_{h(REFCLK-RXER)}$ | Input hold time, RMII_RX_ER valid after RMII_REFCLK high | 2 | | | ns |

**Table 7-31. Switching Characteristics Over Recommended Operating Conditions for EMAC RMII Transmit**

| NO. | PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 4 | $t_{d(REFCLK-TXD)}$ | Output delay time, RMII_REFCLK high to RMII_TXD[1:0] valid | 2 | | ns |
| 5 | $t_{d(REFCLK-TXEN)}$ | Output delay time, RMII_REFCLK high to RMII_TXEN valid | 2 | | ns |

### 7.11.3 Management Data Input/Output (MDIO) Electrical and Timing Specifications

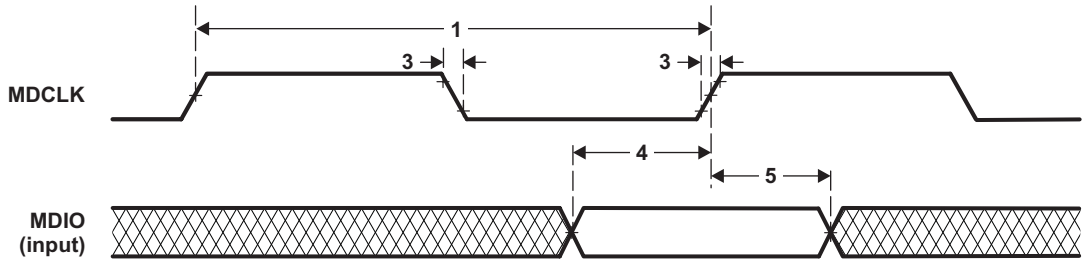


**Figure 7-21. MDIO Input Timing**

**Table 7-32. Timing Requirements for MDIO Input**

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{c(MDCLK)}$ | Cycle time, MDCLK | 400 | - | ns |
| 2 | $t_{w(MDCLK)}$ | Pulse duration, MDCLK high or low | 180 | - | ns |
| 3 | $t_{t(MDCLK)}$ | Transition time, MDCLK | - | 5 | ns |
| 4 | $t_{su(MDIO-MDCLKH)}$ | Setup time, MDIO data input valid before MDCLK High | 33 (1) | - | ns |
| 5 | $t_{h(MDCLKH-MDIO)}$ | Hold time, MDIO data input valid after MDCLK High | 10 | - | ns |

(1) This is a discrepancy to IEEE 802.3, but is compatible with many PHY devices.

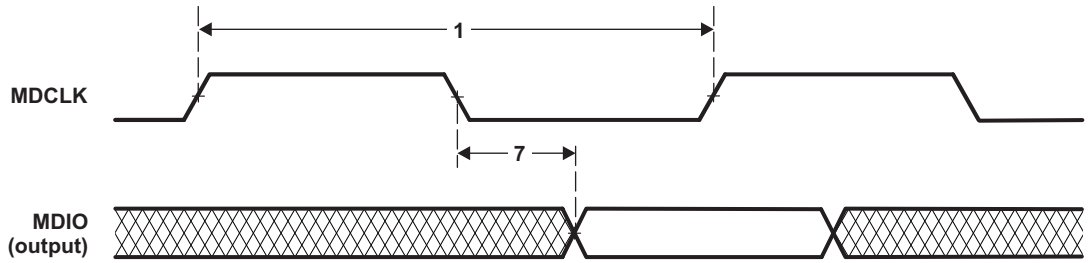


**Figure 7-22. MDIO Output Timing**

**Table 7-33. MDIO Output Timing Requirements**

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | tc(MDCLK) | Cycle time, MDCLK | 400 | – | ns |
| 7 | td(MDCLKL-MDIO) | Delay time, MDCLK low to MDIO data output valid | –7 | 100 | ns |


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# 8 Device and Documentation Support

## 8.1 Device Support

### *8.1.1 Development Support*

Texas Instruments (TI) offers an extensive line of development tools for the TMS570LSxRM48Lx family of MCUs, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules.

The following products support development:

**Software Development Tools**

- Code Composer Studio™ (CCS) Integrated Development Environment (IDE)–
  - C/C++ Compiler
  - Code generation tools
  - Assembler/Linker
  - FPU Optimized Libraries
- Application algorithms
- Sample applications code

**Hardware Development Tools**

- Development and evaluation boards
- JTAG-based emulators - XDS510™ class, XDS560™ emulator, XDS100v2, XDS110, XDS200
- Flash programming tools

For a complete listing of development-support tools, visit the Texas Instruments website at www.ti.com.

### *8.1.2 Device Nomenclature*

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all devices. Each commercial family member has one of three prefixes: TMX, TMP, or TMS (for example, **TMS**570LS3137). These prefixes represent evolutionary stages of product development from engineering prototypes (TMX) through fully qualified production devices (TMS).

Device development evolutionary flow:

**TMX** Experimental device that is not necessarily representative of the final device's electrical specifications.

**TMP** Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification.

**TMS** Fully-qualified production device.

TMX and TMP devices are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

TMS devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

Figure 8-1 shows the numbering and symbol nomenclature for the TMS570LS3137 .

For additional information on the device nomenclature markings, see the device-specific silicon errata document listed in Section 8.2.1, *Related Documentation from Texas Instruments*.

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Full Part # | TMS | 570 | LS | 31 | 3 | 7 | D | ZWT | Q | Q1 | R |
| Orderable Part # | TMS | 570 | | 31 | 3 | 7 | D | ZWT | Q | Q1 | R |

Prefix: TM
TMS = Fully Qualified
TMP = Prototype
TMX = Samples

Core Technology:
570 = Cortex-R4F

Architecture:
LS = Dual CPUs in Lockstep
(not included in orderable part #)

Flash Memory Size:
31 = 3MB

RAM MemorySize:
3 = 256KB

Peripheral Set:
7 = FlexRay, Ethernet

Die Revision:
Blank = Initial Die
A = 1st Die Revision
B = 2nd Die Revision
C = 3rd Die Revision
D = 4th Die Revision

Package Type:
ZWT = 337-BGA Package
PGE = 144-Pin Package

Temperature Range:
Q = –40°C to 125°C

Quality Designator:
Q1 = Automotive

Shipping Options:
R = Tape and Reel

**Figure 8-1. TMS570LS3137 Device Numbering Conventions**


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## 8.2 Documentation Support

### *8.2.1 Related Documentation from Texas Instruments*

The following documents describe the *TMS570LS3137* microcontroller..

**SPNU499** ***TMS570LS31x/21x 16/32-Bit RISC Flash Microcontroller Technical Reference Manual*** details the integration, the environment, the functional description, and the programming models for each peripheral and subsystem in the device.

**SPNZ195** ***TMS570LS31x/21x Microcontroller, Silicon Revision C, Silicon Errata*** describes the usage notes and known exceptions to the functional specifications for the device silicon revision C.

**SPNZ222** ***TMS570LS31x/21x Microcontroller, Silicon Revision D, Silicon Errata*** describes the usage notes and known exceptions to the functional specifications for the device silicon revision D.

**SPNA207** ***Calculating Equivalent Power-on-Hours for Hercules™ Safety MCUs*** details how to use the spreadsheet to calculate the aging effect of temperature on Texas Instruments Hercules Safety MCUs.

## 8.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**TI Embedded Processors Wiki** ***Texas Instruments Embedded Processors Wiki.*** Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

## 8.4 Trademarks

Code Composer Studio, XDS510, XDS560, E2E are trademarks of Texas Instruments.
CoreSight is a trademark of ARM Limited.
ARM, Cortex are registered trademarks of ARM Limited (or its subsidiaries) in the EU and/or elsewhere.
All rights reserved.
$I^2C$-bus is a trademark of NXP Semiconductors N. V.
All other trademarks are the property of their respective owners.

## 8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 8.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 8.7 Device Identification Code Register

The device identification code register identifies several aspects of the device including the silicon version. The details of the device identification code register are shown in Table 8-1. The device identification code register value for this device is:

- Rev A = 0x802AAD05
- Rev B = 0x802AAD15
- Rev C = 0x802AAD1D
- Rev D = 0x802AAD25

**Figure 8-2. Device ID Bit Allocation Register**

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CP-15 | UNIQUE ID | | | | | | | | | | | | | | TECH |
| R-1 | R-00000000010101 | | | | | | | | | | | | | | R-0 |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TECH | | | I/O VOLTAGE | PERIPH PARITY | FLASH ECC | | RAM ECC | VERSION | | | | | 1 | 0 | 1 |
| R-101 | | | R-0 | R-1 | R-10 | | R-1 | R-00000 | | | | | R-1 | R-0 | R-1 |

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

**Table 8-1. Device ID Bit Allocation Register Field Descriptions**

| BIT | FIELD | VALUE | DESCRIPTION |
|---|---|---|---|
| 31 | CP15 | | Indicates the presence of coprocessor 15 |
| | | 1 | CP15 present |
| 30-17 | UNIQUE ID | 10101 | Silicon version (revision) bits.<br>This bit field holds a unique number for a dedicated device configuration (die). |
| 16-13 | TECH | | Process technology on which the device is manufactured. |
| | | 0101 | F021 |
| 12 | I/O VOLTAGE | | I/O voltage of the device. |
| | | 0 | I/O are 3.3 V |
| 11 | PERIPHERAL PARITY | | Peripheral Parity |
| | | 1 | Parity on peripheral memories |
| 10-9 | FLASH ECC | | Flash ECC |
| | | 10 | Program memory with ECC |
| 8 | RAM ECC | | Indicates if RAM memory ECC is present. |
| | | 1 | ECC implemented |
| 7-3 | REVISION | | Revision of the device. |
| 2-0 | 101 | | The platform family ID is always 0b101 |


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## 8.8 Die Identification Registers

The two die ID registers at addresses 0xFFFFFF7C and 0xFFFFFF80 form a 64-bit die ID with the information as shown in Table 8-2.

**Table 8-2. Die-ID Registers**

| ITEM | NUMBER OF BITS | BIT LOCATION |
|---|---|---|
| X Coord. on Wafer | 12 | 0xFFFFFF7C[11:0] |
| Y Coord. on Wafer | 12 | 0xFFFFFF7C[23:12] |
| Wafer # | 8 | 0xFFFFFF7C[31:24] |
| Lot # | 24 | 0xFFFFFF80[23:0] |
| Reserved | 8 | 0xFFFFFF80[31:24] |

## 8.9 Module Certifications

The following communications modules have received certification of adherence to a standard.

### *8.9.1 FlexRay™ Certifications*

# FlexRay™ Protocol Conformance Certificate

**Device (IUT):**

Name: TMS570LS3137 Rev C , TMS570LS3136 Rev C
TMS570LS3135 Rev C , TMS570LS2135 Rev C
TMS570LS2125 Rev C

Package: ZWT (S-PBGA-N337) Plastic Ball Grid Array

Version: Core Release Register: 0x10390206 (CREL[31:0])
Device Identification Code: 0x802AAD1D (DEVID[31:0])

Vendor: Texas Instruments Incorporated
12500 TI Boulevard
Dallas, Texas 75243
USA

**Test basis:**

FlexRay™ protocol version: 2.1 / 2.1RevA
Test specification version: 2.1.2

**Test execution:**

Date: 27.04.2013
Hour of completion: 04:37

**Test results:**

Test cases executed: 275
Test cases passed: 275
Test cases failed: 0

**Test report:**

Execution ID:
TMP570LS3136ZWT1367030227819

Essen, 10.05.2013

Heiko Ehrich

TÜV NORD Mobilität GmbH & Co.KG
Institute for Vehicle Technology and Mobility

**IUT-Details – According to the vendor's data sheet, the IUT has the following peculiarities and optional features:**

| Peculiarity | Value |
|---|---|
| MTS transmission activation adjustment time-string | 0:x:x:0:0:0 |
| MTS transmission deactivation adjustment time-string | 0:x:x:0:0:0 |
| MTS transmission deactivation required | False |
| cIntDecoderDelay [ST] | 8 |
| cColdstartCollisionAbortDelay [µT] | 10 |
| Message ID filtering impl. Via valid message indicator | False |

| Optional feature | Supported/Unsupported |
|---|---|
| Message ID filtering | Unsupported |
| Relative timer | Supported |
| Network Management Vector | Supported |
| (Re)setting of the 'transmit buffer valid flag' | Supported |

This certificate is valid for the hardware and software configuration documented in the test report.

TÜV NORD Mobilität

**Figure 8-3. FlexRay Certification for ZWT Package**


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# FlexRay™ Protocol Conformance Certificate

**Device (IUT):**

Name: TMS570LS3137 Rev C , TMS570LS3135 Rev C
TMS570LS2125 Rev C , TMS570LS2135 Rev C

Package: PGE (S-PQFP-G144) Plastic Quat Flatpack

Version: Core Release Register: 0x10390206 (CREL[31:0])
Device Identification Code: 0x802AAD1D (DEVID[31:0])

Vendor: Texas Instruments Incorporated
12500 TI Boulevard
Dallas, Texas 75243
USA

**Test basis:**

FlexRay™ protocol version: 2.1 / 2.1RevA
Test specification version: 2.1.2

**Test execution:**

Date: 05.05.2013
Hour of completion: 12:45

**Test results:**

Test cases executed: 275
Test cases passed: 275
Test cases failed: 0

**Test report:**

Execution ID:
TMX570LS3137CPGE1367750722343

Essen, 10.05.2013

Heiko Ehrich

TÜV NORD Mobilität GmbH & Co.KG
Institute for Vehicle Technology and Mobility

**IUT-Details – According to the vendor's data sheet, the IUT has the following peculiarities and optional features:**

| Peculiarity | Value |
|---|---|
| MTS transmission activation adjustment time-string | 0:x:x:0:0:0 |
| MTS transmission deactivation adjustment time-string | 0:x:x:0:0:0 |
| MTS transmission deactivation required | False |
| cIntDecoderDelay [ST] | 8 |
| cColdstartCollisionAbortDelay [µT] | 10 |
| Message ID filtering impl. Via valid message indicator | False |

| Optional feature | Supported/Unsupported |
|---|---|
| Message ID filtering | Unsupported |
| Relative timer | Supported |
| Network Management Vector | Supported |
| (Re)setting of the 'transmit buffer valid flag' | Supported |

This certificate is valid for the hardware and software configuration documented in the test report.

TÜV NORD Mobilität

**Figure 8-4. FlexRay Certification for PGE Package**

### 8.9.2 DCAN Certification

**Testhouse**
C&S group GmbH
Am Exer 19b
D-38302 Wolfenbuettel
Phone: +49 5331/90 555-0
Fax: +49 5331/90 555-110

C&S
CAN

## Authentication
**on CAN Conformance**

## Texas Instruments
P10_0294_021_CAN_DL_Test_Authentication_r01.doc
Date of Approval: 2011-Feb-08

C&S is worldwide recognized as a neutral expert in testing of communication systems such as CAN Transceiver, CAN, CAN Software Drivers, (CAN) Network Management, FlexRay and LIN.

Herewith C&S group is proud to confirm that the followings tests on the subsequently specified device implementations have been performed by C&S resulting in the findings given below:

## C&S Conformance Test Results

| | |
|---|---|
| **Manufacturer** | Texas Instruments |
| **Component/Part Number** | TMSx70 x021 Microcontroller Family, DCAN Core Release 0xA3170504, 980 A2C0007940000 X470MUF C63C1 P80576 24 YFB-08A9X6W |
| **Date of Tests** | February 2011 |
| **Version of Test Specification** | CAN Conformance Test<br>1 ISO CAN Conformance Tests according to "ISO 16845:2004 Road vehicles - Controller area network (CAN) - Conformance test plan" and C&S enhancement/ corrections according to "CAN CONFORMANCE TESTING Test Specification C&S Version 2.0 RC"<br>2 C&S Register Functionality Tests according to "C&S Register Functionality Test Specification V2.0"<br>3 C&S Robustness Tests according to "C&S Robustness Test Specification V1.4" |
| **Corresponding Test Report** | P10_0294_020_CAN_DL_Test_report_r01 |
| 1 ISO CAN conformance tests | **Pass** |
| 2 C&S Register Functionality tests | **Pass** |
| 3 C&S Robustness tests | **Pass** |
| • Further Observations | **None** |

Frank Fischer, CTO

Lothar Kukla, Project Manager

Quote No. P10_0294 R01

**Figure 8-5. DCAN Certification**


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### 8.9.3 LIN Certification

#### 8.9.3.1 LIN Master Mode

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LOCAL INTERCONNECT NETWORK

DAkkS
Deutsche
Akkreditierungsstelle
D-PL-17201-01-01

Accredited test lab by DAkkS GmbH according DIN ISO/IEC 17025.
The accreditation is valid for all test methods stated in the certificate.

**Test Summary**
**for**
**LIN 2.1 Conformance Test - Master**

| | |
|---|---|
| *Client / Manufacturer:* | **Texas Instruments** |
| | Automotive Applications |
| | 12500 TI Boulevard |
| | 75243 DALLAS, TEXAS |
| | UNITED STATES OF AMERICA |
| *Implementation Under Test:* | **Microcontroller TMS570LS3137** |
| *Part Number:* | **LIN Master Mode** |
| *Revision:* | SW: : 2013-05-31_IHR_LIN |
| *Test Sample Marking:* | TMX570LS 3137 CZWTQQ1 YFC-2AAQ32W |
| *Test Board:* | Gladiator 337 SN# 58 rev. B |
| *Performed Tests:* | **LIN OSI Layer 2 – Data Link Layer** |
| | **Node Configuration / Network Management** |
| *Specification References:* | **LIN Conformance Test Specification, 10-Oct-2008** |
| | for the LIN Specification Package Revision 2.1 , 24-Nov-2006 |
| *Result / Status:* | **The device has *passed* the test.** |
| *Version / Date:* | 1.0 / 13-May-2013 |
| *Document Number:* | Test Summary_DLL21_Master_20121130_130513_TMS570LS_V1.0.doc |
| *ihr Reference:* | 20121130 |

**This test summary don't represent a complete test report according the LIN consortium**.
It contains 7 pages and shall not be reproduced except in full without written approval of the *ihr* Test Center. All performed test results concerns the above mentioned IUT revision only.

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**Figure 8-6. LIN Certification - Master Mode**

### 8.9.3.2 LIN Slave Mode - Fixed Baud Rate

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DAkkS
Deutsche
Akkreditierungsstelle
D-PL-17201-01-01

Accredited test lab by DAkkS GmbH according DIN ISO/IEC 17025.
The accreditation is valid for all test methods stated in the certificate.

# Test Summary
for
# LIN 2.1 Conformance Test - Slave

| | |
|---|---|
| *Client / Manufacturer:* | **Texas Instruments** |
| | Automotive Applications |
| | 12500 TI Boulevard |
| | 75243 DALLAS, TEXAS |
| | UNITED STATES OF AMERICA |
| *Implementation Under Test:* | **Microcontroller TMS570LS3137** |
| | **LIN Slave Mode - Fixed Baud Rate Mode** |
| *Revision:* | SW: 2013-05-31_IHR_LIN |
| *Test Sample Marking:* | TMX570LS 3137 CZWTQQ1 YFC-2AAQ32W |
| *Test Board:* | Gladiator 337 SN# 58 rev. B |
| *Performed Tests:* | **LIN OSI Layer 2 – Data Link Layer** |
| | **Node Configuration / Network Management** |
| *Specification References:* | **LIN Conformance Test Specification, 10-Oct-2008** |
| | for the LIN Specification Package Revision 2.1 , 24-Nov-2006 |
| *Result / Status:* | **The device has *passed* the test.** |
| *Version / Date:* | 1.0 / 13-May-2013 |
| *Document Number:* | Test Summary_DLL21_Slave_Fixed_20121130_130513_TMS570LS_V1.0.doc |
| ***ihr** Reference:* | 20121130 |

**This test summary don't represent a complete test report according the LIN consortium**.

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All performed test results concerns the above mentioned IUT revision only.

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**Figure 8-7. LIN Certification - Slave Mode - Fixed Baud Rate**


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### 8.9.3.3 LIN Slave Mode - Adaptive Baud Rate

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DAkkS
Deutsche
Akkreditierungsstelle
D-PL-17201-01-01

Accredited test lab by DAkkS GmbH according DIN ISO/IEC 17025.
The accreditation is valid for all test methods stated in the certificate.

# Test Summary
for
# LIN 2.1 Conformance Test - Slave

| | |
|---|---|
| *Client / Manufacturer:* | **Texas Instruments** |
| | Automotive Applications |
| | 12500 TI Boulevard |
| | 75243 DALLAS, TEXAS |
| | UNITED STATES OF AMERICA |
| *Implementation Under Test:* | **Microcontroller TMS570LS3137** |
| | **LIN Slave Mode - Adaptive Baud Rate Mode** |
| *Revision:* | SW: 2013-05-31_IHR_LIN |
| *Test Sample Marking:* | TMX570LS 3137 CZWTQQ1 YFC-2AAQ32W |
| *Test Board:* | Gladiator 337 SN# 58 rev. B |
| *Performed Tests:* | **LIN OSI Layer 2 – Data Link Layer** |
| | **Node Configuration / Network Management** |
| *Specification References:* | **LIN Conformance Test Specification, 10-Oct-2008** |
| | for the LIN Specification Package Revision 2.1 , 24-Nov-2006 |
| *Result / Status:* | **The device has *passed* the test.** |
| *Version / Date:* | 1.0 / 13-May-2013 |
| *Document Number:* | Test Summary_DLL21_Slave_Adapt_TI_TMS570LS_130513_V1.0.doc |
| ***ihr** Reference:* | 20121130 |

**This test summary don't represent a complete test report according the LIN consortium**.

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All performed test results concerns the above mentioned IUT revision only.

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Bank: Volksbank Bühl
Konto: 1376209
BLZ: 66291400
UST-Id-Nr. DE177221429

Geschäftsführer: Jörg Holzberg
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Handelsreg.:Baden-Baden HRB908BH
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**Figure 8-8. LIN Certification - Slave Mode - Adaptive Baud Rate**

# 9 Mechanical Packaging and Orderable Information

## 9.1 Packaging Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TMS5703137CGWTMEP | Active | Production | NFBGA (GWT) \| 337 | 90 \| JEDEC TRAY (5+1) | No | SNPB | Level-3-220C-168 HR | -55 to 125 | TMS570 LS3137CGWTMEP |
| TMS5703137CGWTQEP | Active | Production | NFBGA (GWT) \| 337 | 90 \| JEDEC TRAY (5+1) | No | SNPB | Level-3-220C-168 HR | -40 to 125 | TMS570 LS3137CGWTQEP |
| TMS5703137DPGEQQ1 | Active | Production | LQFP (PGE) \| 144 | 60 \| JEDEC TRAY (10+1) | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | TMS570LS 3137DPGEQQ1 |
| TMS5703137DPGEQQ1.B | Active | Production | LQFP (PGE) \| 144 | 60 \| JEDEC TRAY (10+1) | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | TMS570LS 3137DPGEQQ1 |
| TMS5703137DZWTQQ1 | Active | Production | NFBGA (ZWT) \| 337 | 90 \| JEDEC TRAY (10+1) | Yes | SNAGCU | Level-3-260C-168 HR | -40 to 125 | TMS570LS 3137DZWTQQ1 |
| TMS5703137DZWTQQ1.B | Active | Production | NFBGA (ZWT) \| 337 | 90 \| JEDEC TRAY (10+1) | Yes | SNAGCU | Level-3-260C-168 HR | -40 to 125 | TMS570LS 3137DZWTQQ1 |
| V62/13629-01XE | Active | Production | NFBGA (GWT) \| 337 | 90 \| JEDEC TRAY (5+1) | No | SNPB | Level-3-220C-168 HR | -40 to 125 | TMS570 LS3137CGWTQEP |
| V62/13629-02XE | Active | Production | NFBGA (GWT) \| 337 | 90 \| JEDEC TRAY (5+1) | No | SNPB | Level-3-220C-168 HR | -55 to 125 | TMS570 LS3137CGWTMEP |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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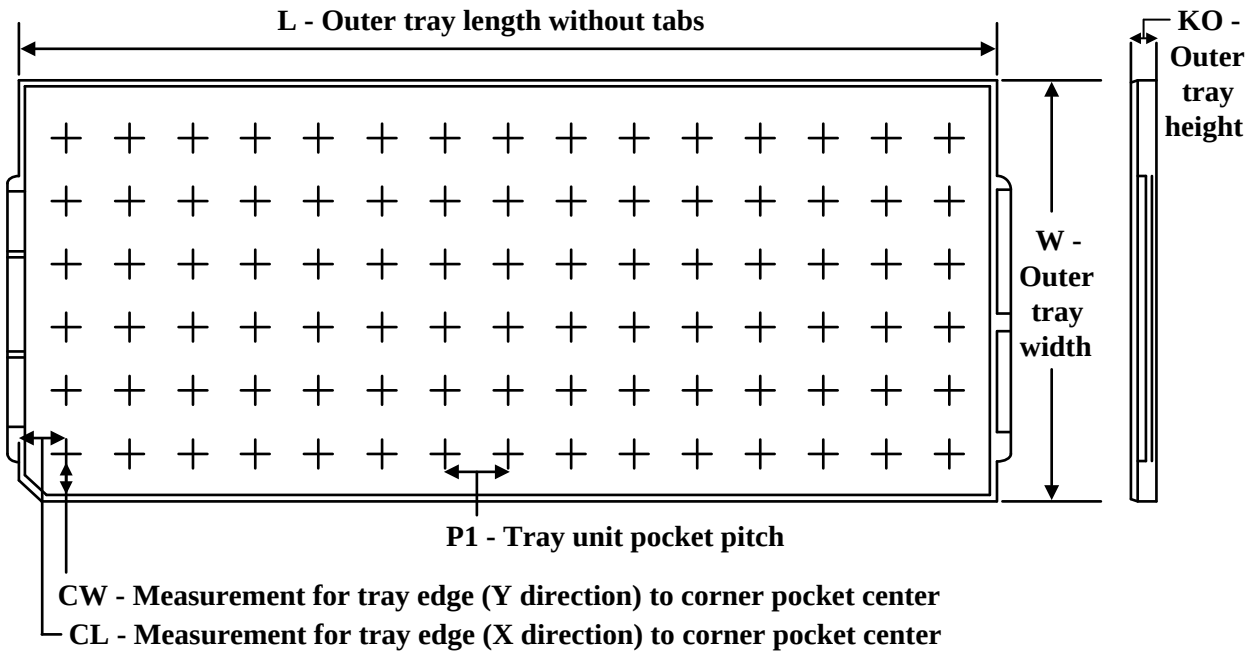
**OTHER QUALIFIED VERSIONS OF TMS570LS3137, TMS570LS3137-EP :**

- Catalog : TMS570LS3137
- Enhanced Product : TMS570LS3137-EP

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TRAY

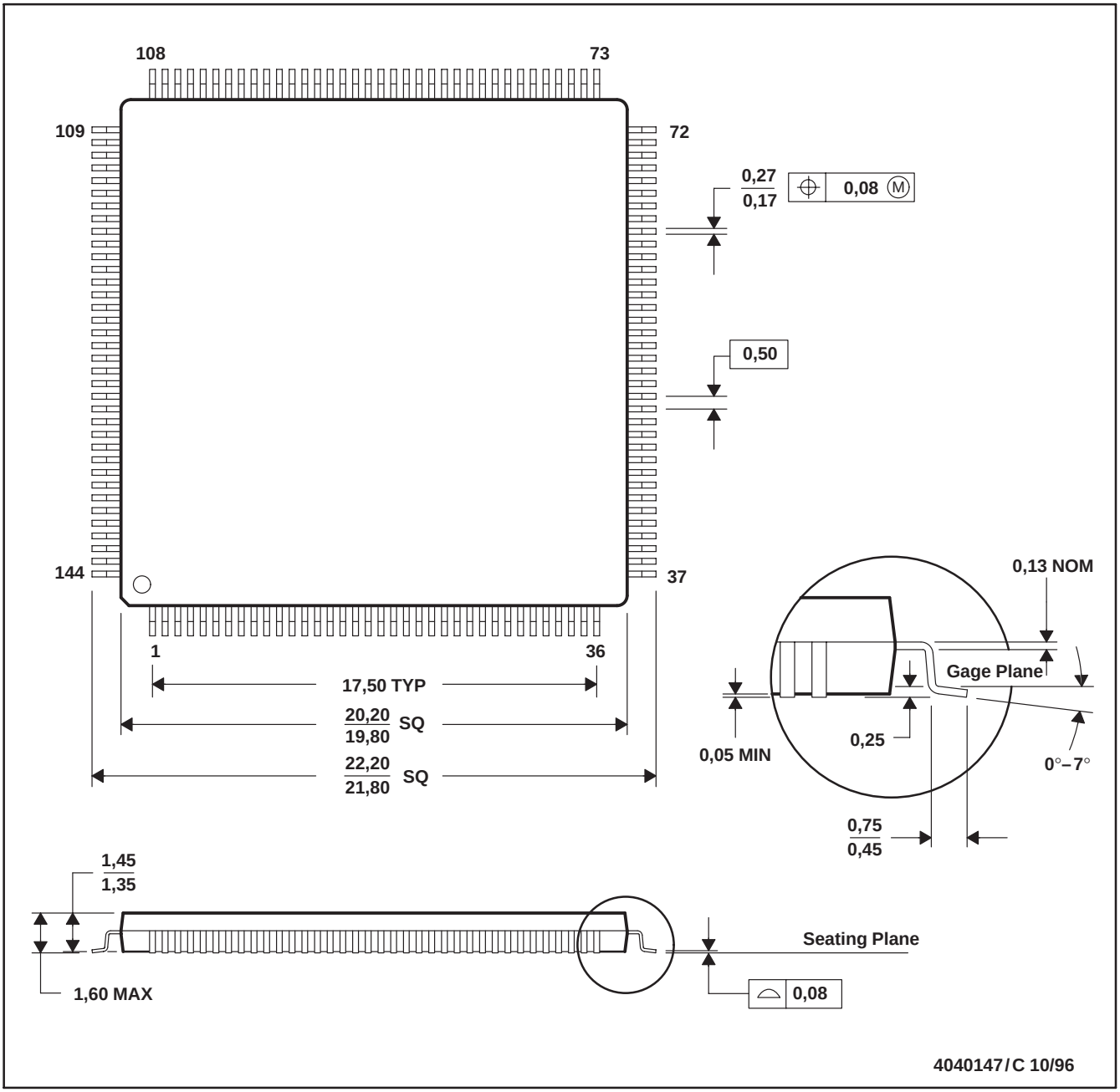



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

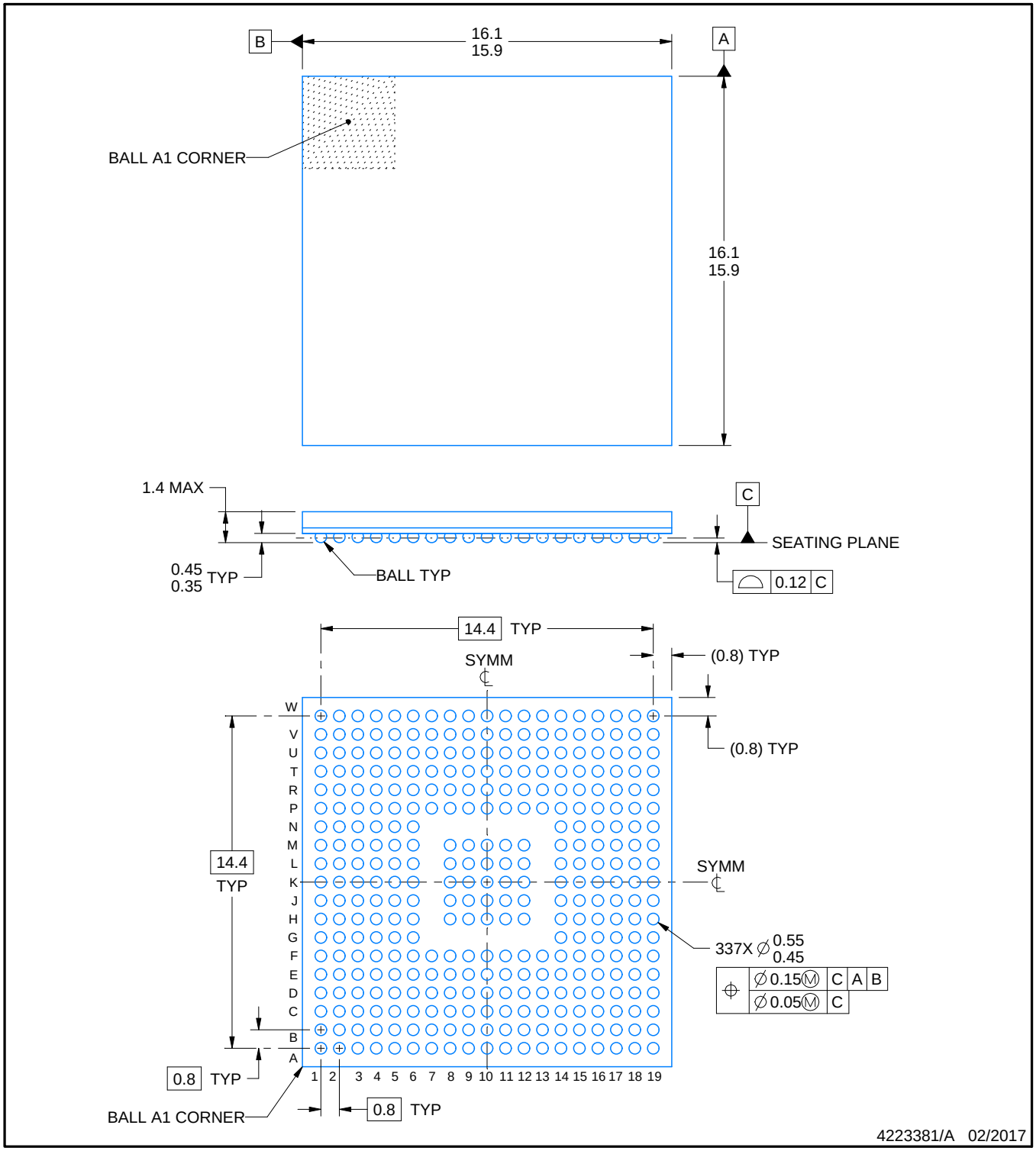
*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (µm) | P1 (mm) | CL (mm) | CW (mm) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TMS5703137CGWTMEP | GWT | NFBGA | 337 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 20 | 17.5 | 15.45 |
| TMS5703137CGWTQEP | GWT | NFBGA | 337 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 20 | 17.5 | 15.45 |
| TMS5703137DPGEQQ1 | PGE | LQFP | 144 | 60 | 5X12 | 150 | 315 | 135.9 | 7620 | 25.4 | 17.8 | 17.55 |
| TMS5703137DPGEQQ1.B | PGE | LQFP | 144 | 60 | 5X12 | 150 | 315 | 135.9 | 7620 | 25.4 | 17.8 | 17.55 |
| TMS5703137DZWTQQ1 | ZWT | NFBGA | 337 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 20 | 17.5 | 15.45 |
| TMS5703137DZWTQQ1.B | ZWT | NFBGA | 337 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 20 | 17.5 | 15.45 |
| V62/13629-01XE | GWT | NFBGA | 337 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 20 | 17.5 | 15.45 |
| V62/13629-02XE | GWT | NFBGA | 337 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 20 | 17.5 | 15.45 |

**PGE (S-PQFP-G144)** **PLASTIC QUAD FLATPACK**

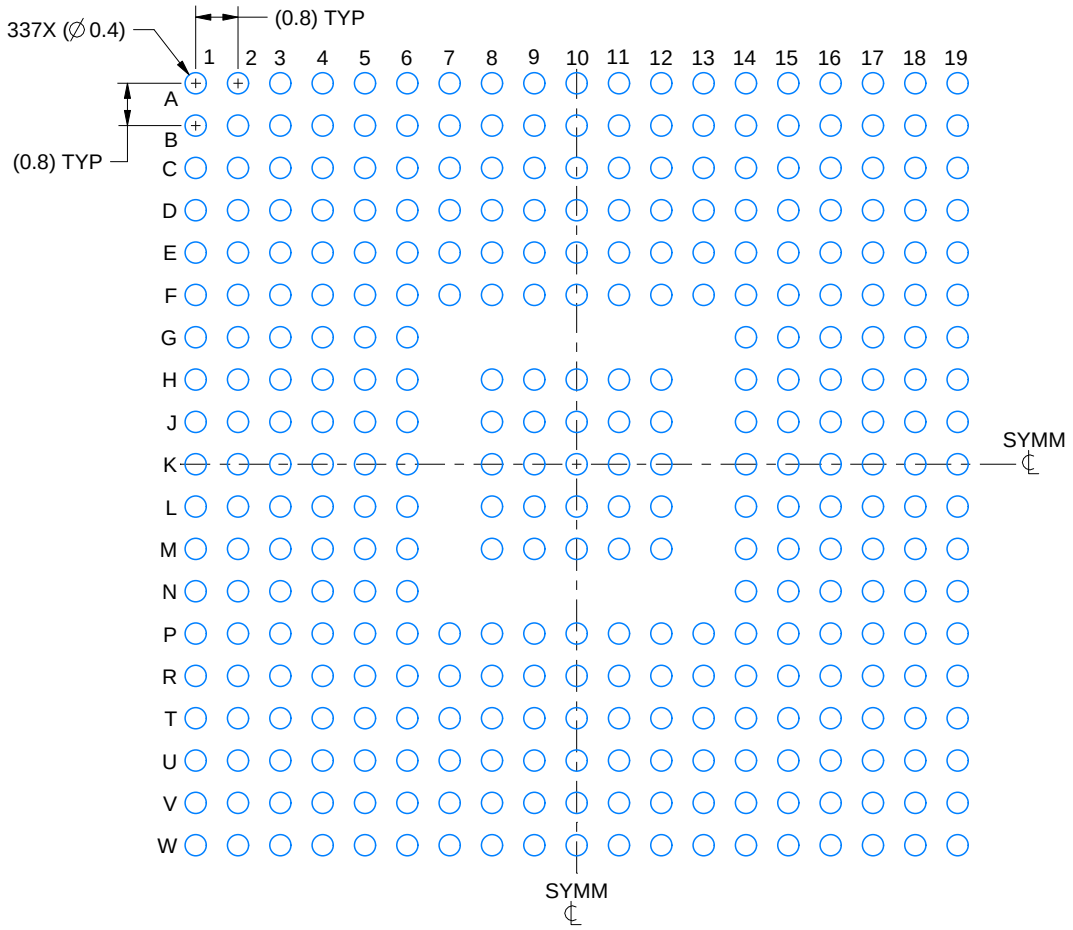



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

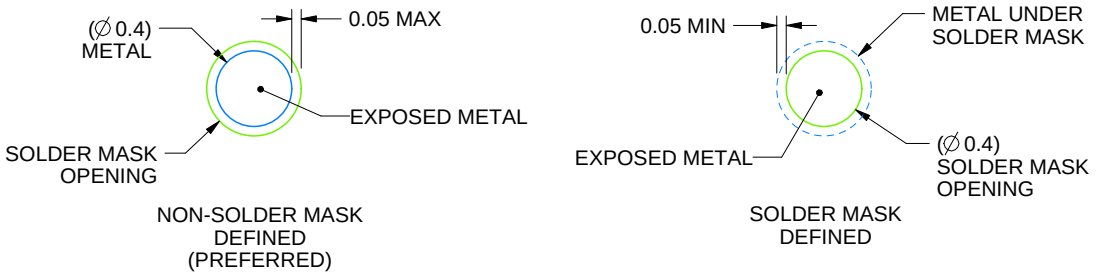



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:7X

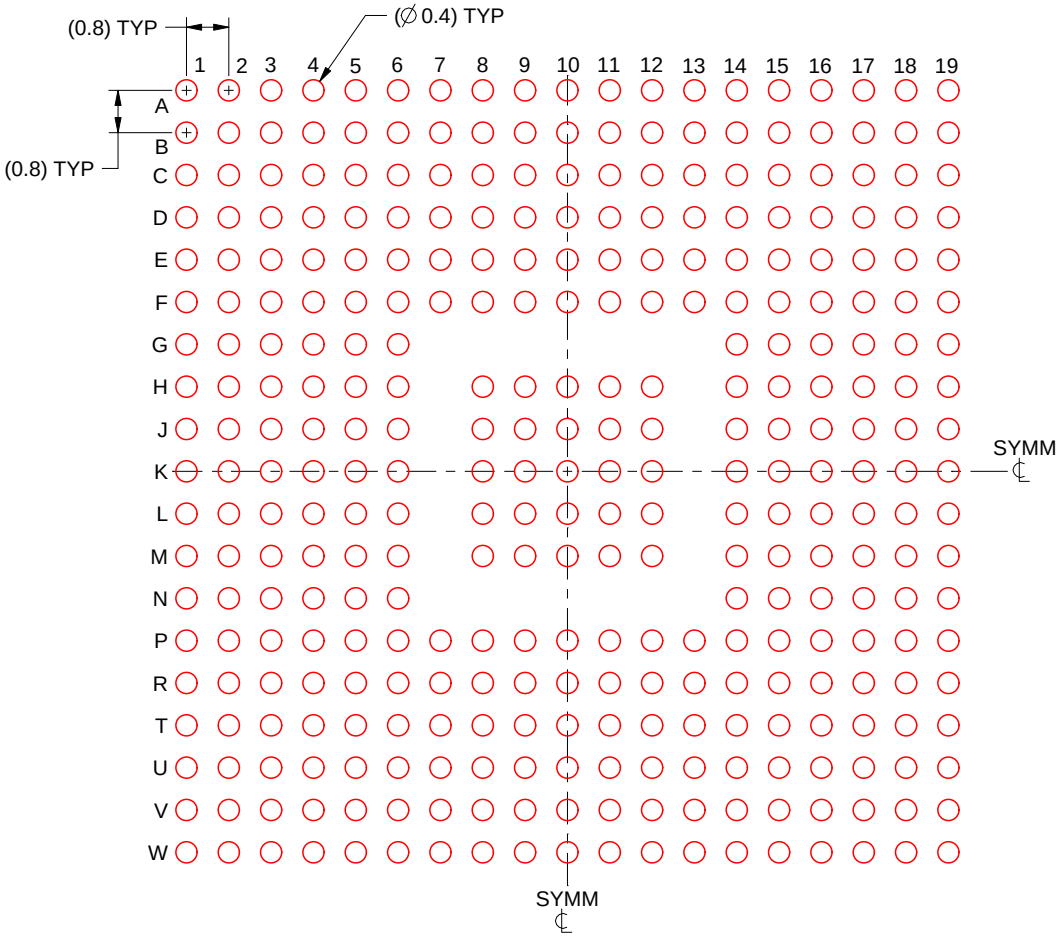



SOLDER MASK DETAILS
NOT TO SCALE

4223381/A 02/2017

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).




SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE:7X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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