TMS570LS0x32 16および32ビットRISCフラッシュ・マイクロコントローラ

1 デバイスの概要

1.1 特長

- 安全性が重要なアプリケーション用の高性能な車載グレード・マイクロコントローラ
  - ロックステップで動作するデュアルCPU
  - ECC付きのフラッシュとRAMインターフェイス
  - CPUおよびオンチップRAM用の内蔵セルフ・テスト
  - エラー・ピン付きのエラー通知モジュール
  - 電圧およびクロックの監視
- ARM® Cortex®-R4 32ビットRISC CPU
  - 8段パイプラインによる1.66DMIPS/MHzの効率
  - 8領域のメモリ保護ユニット(MPU)
  - サードパーティ・サポート付きのオープン・アーキテクチャ
- 動作条件
  - 80MHzのシステム・クロック
  - コア電源電圧(V_{CC}): 公称1.2V
  - I/O電源電圧(V_{CCIO}): 公称3.3V
  - ADC電源電圧(V_{CCAD}): 公称3.3V
- 内蔵メモリ
  - 最大384KBのECC付きプログラム用フラッシュ・メモリ
  - ECC付きの32KB RAM
  - ECC付きのEEPROMエミュレーション用16KBフラッシュ
- Hercules™共通プラットフォーム・アーキテクチャ
  - ファミリ間で一貫したメモリ・マップ
  - リアルタイム割り込み(RTI)タイマ(OSタイマ)
  - 96チャネル・ベクタ割り込みモジュール(VIM)
  - 2チャネルの巡回冗長性検査(CRC)
- スリップ検出機能を内蔵した周波数変調フェーズ・ロック・ループ(FMPLL)
- IEEE 1149.1 JTAG、バウンダリ・スキャンおよびARM CoreSight™コンポーネント
- 高度なJTAGセキュリティ・モジュール(AJSM)
- 複数の通信インターフェイス
  - 2つのCANコントローラ(DCAN)
    - DCAN1 - パリティ保護付きの32のメールボックス
    - DCAN2 - パリティ保護付きの16のメールボックス
    - CANプロトコル・バージョン2.0Bに準拠
  - マルチバッファ付きのシリアル・ペリフェラル・インターフェイス(MibSPI)モジュール
    - 128ワード、パリティ保護付き
  - 2つの標準シリアル・ペリフェラル・インターフェイス(SPI)モジュール
  - UART (SCI)インターフェイス、ローカル相互接続ネットワーク(LIN 2.1)インターフェイスをサポート
- 次世代型ハイエンド・タイマ(N2HET)モジュール
  - 最大19のプログラム可能ピン
  - パリティ保護付きの128ワードの命令RAM
  - ハードウェア角度ジェネレータを内蔵
  - MPU付きの専用ハイエンド・タイマ転送ユニット(HTU)
- 拡張直交エンコーダ・パルス(eQEP)モジュール
  - モータ位置エンコーダ・インターフェイス
- 12ビットのマルチバッファ付きアナログ/デジタル・コンバータ(ADC)モジュール
  - 16チャネル
  - 64個のパリティ保護付きリザルト・バッファ
- 最大45の汎用入力/出力(GPIO)ピン
  - 8つの専用の割り込み対応GPIOピン
- パッケージ
  - 100ピン・クワッド・フラットパック(PZ) [グリーン]

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1.2 アプリケーション

- ブレーキ・システム(ABSおよびESC)
- 電動パワー・ステアリング(EPS)
- 電動ポンプ制御
- バッテリ管理システム
- アクティブ運転支援システム
- 宇宙および航空
- 鉄道通信
- オフロード車両

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1.3 概要

TMS570LS0432/0332デバイスは、安全性システム用の高性能、車載グレードのマイクロコントローラです。安全性アーキテクチャには、ロックステップ内のデュアルCPU、CPUとメモリのBISTロジック、フラッシュとデータSRAMの両方のECC、ペリフェラル・メモリのパリティ、ペリフェラルI/Oのループバック機能が含まれます。

TMS570LS0432/0332デバイスには、ARM Cortex-R4 CPUが搭載されています。このCPUは1.66DMIPS/MHzの効率を持ち、最高80MHzで動作するよう構成でき、性能は132DMIPSに達します。このデバイスは、ビッグ・エンディアン(BE32)形式をサポートします。

TMS570LS0432/0332デバイスには、それぞれ384KBおよび256KBの統合フラッシュ・メモリと、32KBのデータRAMが搭載されています。フラッシュ・メモリとRAMはどちらも、単一ビット・エラーの訂正および2ビット・エラーの検出機能があります。このデバイスのフラッシュ・メモリは不揮発性、電気的に消去可能、プログラミング可能なメモリで、64ビット幅のデータ・バス・インターフェイスとともに実装されています。このフラッシュ・メモリは、読み取り、プログラム、消去のすべての操作を3.3V電源入力(I/O電源と同じレベル)で実行します。パイプライン・モードでは、フラッシュ・メモリは80MHzのシステム・クロック周波数で動作します。SRAMは、対応する周波数範囲の全体にわたって、バイト、ハーフワード、ワード、およびダブルワード・モードでの単一サイクル読み取り/書き込みアクセスをサポートしています。

TMS570LS0432/0332デバイスには、リアルタイム制御ベースのアプリケーション用に、最大19のI/O端子を持つ次世代型ハイエンド・タイマ(N2HET)タイミング・コプロセッサや、12ビットのアナログ/デジタル・コンバータ(ADC) (100ピン・パッケージで16の入力に対応)などのペリフェラルが搭載されています。

N2HETは、リアルタイム・アプリケーションに対応する洗練されたタイミング機能を搭載した先進のインテリジェント・タイマです。このタイマは、専用のタイマ・マイクロマシンや付属のI/Oポートを持ち、小さな命令セットでソフトウェア制御されます。N2HETは、パルス幅変調された出力、キャプチャ/コンペア入力、GPIOで使用できます。複数のセンサ情報や、複雑で正確な時間パルスを持つドライブ・アクチュエータを必要とするアプリケーションに最適です。ハイエンド・タイマ転送ユニット(HTU)では、DMA型のトランザクションにより、N2HETデータをメイン・メモリとの間で転送できます。HTUには、メモリ保護ユニット(MPU)が組み込まれています。

拡張直交エンコーダ・パルス(eQEP)モジュールを、リニアまたはロータリー・インクリメンタル・エンコーダとの直接インターフェイスとして使用すると、高性能な動作および位置制御システムに使用される位置、方向、速度の情報を、回転する機械から取得できます。

このデバイスには、12ビット分解能のMibADC (16チャネル)と、64ワードのパリティ保護されたバッファRAMが搭載されています。MibADCの各チャネルは、個別に変換を行うことも、ソフトウェアでグループ化を行い、連続変換シーケンスを実行することもできます。グループ化には3つの異なる方法があります。各シーケンスは、トリガごとに1回の変換を行うことも、連続変換モードに設定することもできます。 MibADCは、古いデバイスとの互換性が求められる場合や、より高速な変換が求められる場合のため、10ビット・モードにも対応しています。

このデバイスには、複数の通信インターフェイスとして1つのMibSPI、2つのSPI、1つのUART/LIN、2つのDCANが搭載されています。SPIにより、類似したシフト・レジスタ形デバイス間でのシリアル高速通信を簡単に実現できます。UART/LINは、Local Interconnect Standard 2.1をサポートし、標準のNon-Return-to-Zero (NRZ)形式を使用した全二重モードのUARTとして使用できます。DCANは、CAN 2.0 (AおよびB)プロトコル規格をサポートします。また、最高1Mbpsの堅牢な通信速度で分散リアルタイム制御を効率的にサポートする、シリアルのマルチマスタ通信プロトコルを使用します。DCANは、信頼性の高いシリアル通信や多重配線が必要な、ノイズの多い厳しい環境(自動車および工業分野など)で動作するアプリケーションに最適です。

周波数変調フェーズ・ロック・ループ(FMPLL)クロック・モジュールは、外部の基準周波数を、内部で使用するための高い周波数に逓倍します。FMPLLは、5つのクロック・ソース入力の1つを、グローバル・クロック・モジュール(GCM)に供給します。GCMは、使用可能なクロック・ソースとデバイス・クロック・ドメイン間のマッピングを管理します。

このデバイスには、外部クロック・プリスケーラ(ECP)モジュールも搭載されており、このモジュールを有効にすると、ECLKピンに連続的な外部クロックを出力します。ECLK周波数は、ユーザーによる設定が可能なペリフェラル・インターフェイス・クロック(VCLK)周波数の比率です。この低周波数出力は、デバイスの動作周波数のインジケータとして外部で監視することができます。

エラー通知モジュール(ESM)は、すべてのデバイス・エラーを監視し、障害が検出されたときに割り込みが生成されるか、外部のnERRORピンがトグルされるかを決定します。nERRORピンは、マイクロコントローラのフォルト条件のインジケータとして、外部から監視できます。

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I/O多重化および制御モジュール(IOMM)により、別の機能をサポートするよう入力/出力ピンを構成可能です。このデバイスで複数の機能をサポートするピンの一覧を、表 4-17に示します。

内蔵の安全性機能と、通信および制御ペリフェラルを広範に選択できることから、TMS570LS0432/0332デバイスは、安全性の要件が重要なリアルタイム制御アプリケーションに理想的なソリューションです。

製品情報(1)

型番	パッケージ	本体サイズ
TMS570LS0432PZ	LQFP (100)	14.00mm×14.00mm
TMS570LS0332PZ	LQFP (100)	14.00mm×14.00mm

(1) 詳細については、9、「*メカニカル、パッケージ、および注文情報*」を参照してください。

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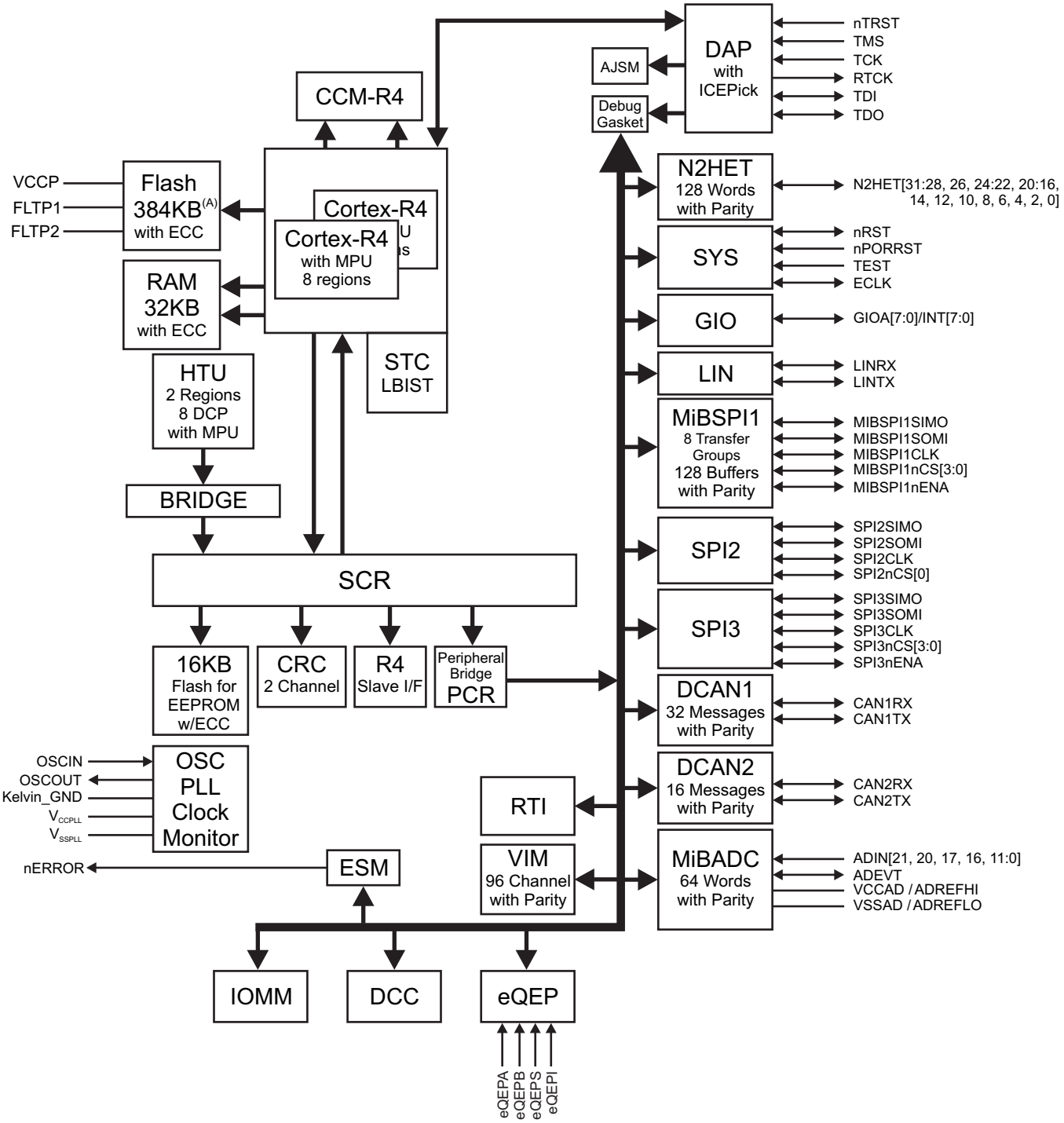
1.4 機能ブロック図

デバイスの機能ブロック図を図 1-1に示します。



A. TMS570LS0332デバイスでは、ECC付きの256KBフラッシュ・メモリのみがサポートされます。

図 1-1. 機能ブロック図

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2 改訂履歴

範囲: Hercules™ TMS570 MCUデバイス・ファミリへの該当する更新で、特に、現在開発の量産データ(PD)段階にあるTMS570LS0432デバイスに関連する更新が組み込まれています。

2015年6月30日発行分から2018年05月31日発行分への変更 (from B Revision (June 2015) to C Revision) **Page**

- Section 5.1 (Absolute Maximum Ratings): Updated/Changed Supply voltage, V_{CCAD} MAX value from "**3.6**" to "**4.6**" V 18
- Section 5.7 (Power Consumption): Clarified the conditions for the 3.3V current requirements when programming or erasing flash 21
- 6.20.6 (Advanced JTAG Security Module): Updated AJSM description..... 68
- 8.8(デバイス識別コード・レジスタ): デバイスIDレジスタのアドレスを追加。..... 100

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3 Device Comparison

表 3-1 lists the features of the TMS570LS0432/0332 devices.

表 3-1. TMS570LS0432/0332 Device Comparison(1)(2)

FEATURES	DEVICES						
Generic Part Number	**TMS570LS1227ZWT**(3)	TMS570LS0714ZWT	TMS570LS0714PGE	TMS570LS0714PZ	**TMS570LS0432PZ**(3)	TMS570LS0332PZ	TMS570LS0232PZ
Package	337 BGA	337 BGA	144 QFP	100 QFP	100 QFP	100 QFP	100 QFP
CPU	ARM Cortex-R4F	ARM Cortex-R4F	ARM Cortex-R4F	ARM Cortex-R4F	ARM Cortex-R4	ARM Cortex-R4	ARM Cortex-R4
Frequency (MHz)	180	180	160	100	80	80	80
Flash (KB)	1280	768	768	768	384	256	128
RAM (KB)	192	128	128	128	32	32	32
Data Flash [EEPROM] (KB)	64	64	64	64	16	16	16
EMAC	10/100	–	–	–	–	–	–
FlexRay	2-ch	–	–	–	–	–	–
CAN	3	3	3	2	2	2	2
MibADC 12-bit (Ch)	2 (24ch)	2 (24ch)	2 (24ch)	2 (16ch)	1 (16ch)	1 (16ch)	1 (16ch)
N2HET (Ch)	2 (44)	2 (44)	2 (40)	2 (21)	1 (19)	1 (19)	1 (19)
ePWM Channels	14	14	14	8	–	–	–
eCAP Channels	6	6	6	4	0	0	0
eQEP Channels	2	2	2	1	1	1	1
MibSPI (CS)	3 (6 + 6 + 4)	3 (6 + 6 + 4)	3 (5 + 6 + 4)	2 (5 + 1)	1 (4)	1 (4)	1 (4)
SPI (CS)	2 (2 + 1)	2 (2 + 1)	1 (1)	1 (1)	2	2	2
SCI (LIN)	2 (1 with LIN)	2 (1 with LIN)	2 (1 with LIN)	1 (with LIN)	1 (with LIN)	1 (with LIN)	1 (with LIN)
I2C	1	1	1	–	–	–	–
GPIO (INT)(4)	101 (with 16 interrupt capable)	101 (with 16 interrupt capable)	64 (with 10 interrupt capable)	45 (with 9 interrupt capable)	45 (with 8 interrupt capable)	45 (with 9 interrupt capable)	45 (with 8 interrupt capable)
EMIF	16-bit data	–	–	–	–	–	–
ETM (Trace)	–	–	–	–	–	–	–
RTP/DMM	–	–	–	–	–	–	–
Operating Temperature	–40ºC to 125ºC	–40ºC to 125ºC	–40ºC to 125ºC	–40ºC to 125ºC	–40ºC to 125ºC	–40ºC to 125ºC	–40ºC to 125ºC
Core Supply (V)	1.14 V – 1.32 V	1.14 V – 1.32 V	1.14 V – 1.32 V	1.14 V – 1.32 V	1.14 V – 1.32 V	1.14 V – 1.32 V	1.14 V – 1.32 V
I/O Supply (V)	3.0 V – 3.6 V	3.0 V – 3.6 V	3.0 V – 3.6 V	3.0 V – 3.6 V	3.0 V – 3.6 V	3.0 V – 3.6 V	3.0 V – 3.6 V

(1) For additional device variants, see www.ti.com/tms570
(2) This table reflects the maximum configuration for each peripheral. Some functions are multiplexed and not all pins are available at the same time.
(3) Superset device
(4) Total number of pins that can be used as general-purpose input or output when not used as part of a peripheral.

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4 Terminal Configuration and Functions

4.1 PZ QFP Package Pinout (100-Pin)

図 4-1 shows the 100-pin PZ QFP package pinout.

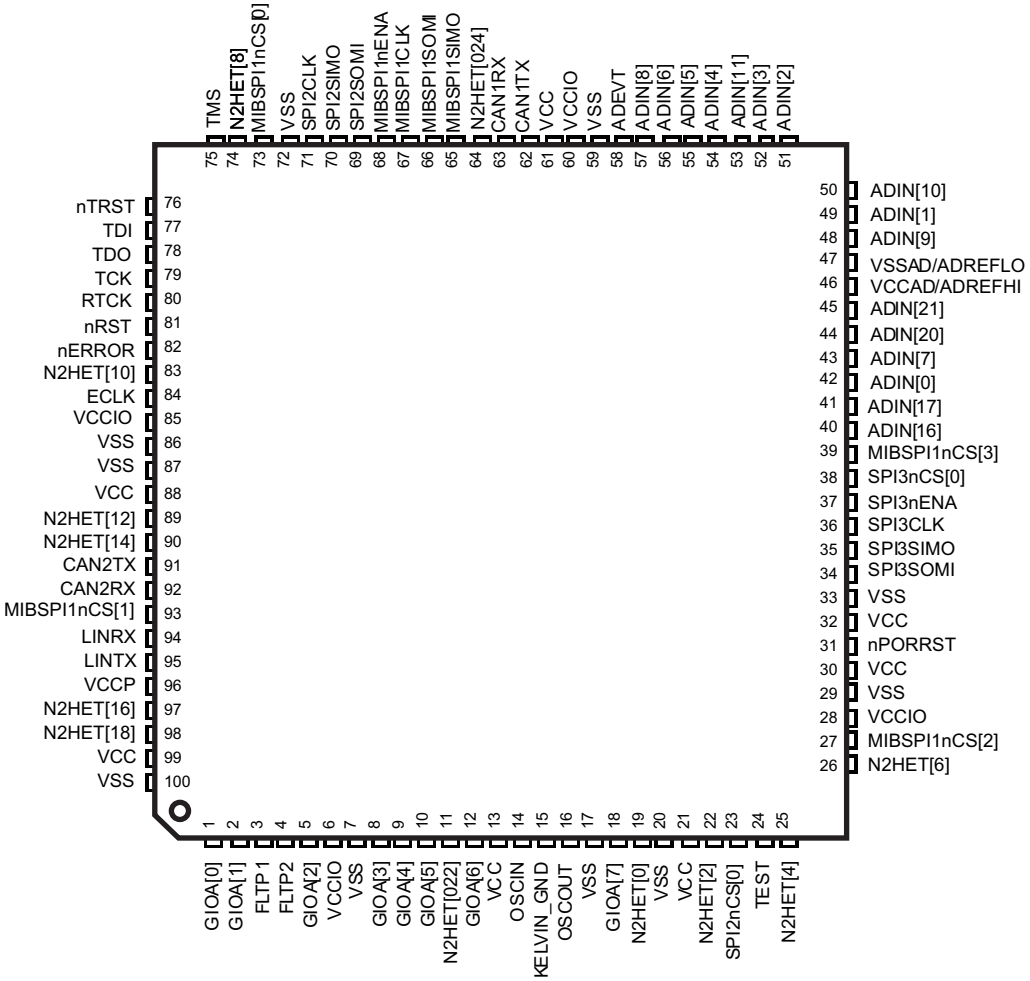

図 4-1. PZ QFP Package Pinout (100-Pin)

Note: Pins can have multiplexed functions. Only the default function is depicted in 図 4-1.

4.2 Terminal Functions

表 4-1 through 表 4-16 identify the external signal names, the associated pin numbers along with the mechanical package designator, the pin type (Input, Output, I/O, Power, or Ground), whether the pin has any internal pullup/pulldown, whether the pin can be configured as a GPIO, and a functional pin description.

注: In the Terminal Functions table below, the "Reset Pull State" is the state of the pull applied to the terminal while nPORRST is low and immediately after nPORRST goes High. The default pull direction may change when software configures the pin for an alternate function. The "Pull Type" is the type of pull asserted when the signal name in bold is enabled for the given terminal by the IOMM control registers.

All I/O signals except nRST are configured as inputs while nPORRST is low and immediately after nPORRST goes High. While nPORRST is low, the input buffers are disabled, and the output buffers are disabled with the default pulls enabled.

All output-only signals have the output buffer disabled and the default pull enabled while nPORRST is low, and are configured as outputs with the pulls disabled immediately after nPORRST goes High.

4.2.1 High-End Timer (N2HET)

表 4-1. High-End Timer (N2HET)

TERMINAL		SIGNAL TYPE	RESET PULL STATE	PULL TYPE	DESCRIPTION
SIGNAL NAME	100 PZ				
N2HET[0]	19	I/O	Pulldown	Programmable, 20 µA	Timer input capture or output compare. The N2HET applicable terminals can be programmed as general-purpose input/output (GPIO). Each terminal has a suppression filter with a programmable duration.
N2HET[2]	22				
N2HET[4]	25				
N2HET[6]	26				
N2HET[8]	74				
N2HET[10]	83				
N2HET[12]	89				
N2HET[14]	90				
N2HET[16]	97				
MIBSPI1nCS[1]/EQEPS/ **N2HET[17]**	93				
N2HET[18]	98				
MIBSPI1nCS[2]/N2HET[20]/ **N2HET[19]**	27				
MIBSPI1nCS[2]/**N2HET[20]**/ N2HET[19]	27				
N2HET[22]	11				
N2HET[24]	64				
MIBSPI1nCS[3]/**N2HET[26]**	39				
ADEVT/**N2HET[28]**	58				
GIOA[7]/**N2HET[29]**	18				
MIBSPI1nENA/N2HET[23]/ **N2HET[30]**	68				
GIOA[6]/SPI2nCS[1]/**N2HET[31]**	12				

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4.2.2 Enhanced Quadrature Encoder Pulse Modules (eQEP)

表 4-2. Enhanced Quadrature Encoder Pulse Modules (eQEP)

TERMINAL		SIGNAL TYPE	RESET PULL STATE	PULL TYPE	DESCRIPTION
SIGNAL NAME	100 PZ				
SPI3CLK/**EQEPA**	36	Input	Pullup	Fixed 20 µA	Enhanced QEP Input A
SPI3nENA/**EQEPB**	37	Input			Enhanced QEP Input B
SPI3nCS[0]/**EQEPI**	38	I/O			Enhanced QEP Index
MIBSPI1nCS[1]/**EQEPS**/N2HET [17]	93	I/O			Enhanced QEP Strobe

4.2.3 General-Purpose Input/Output (GPIO)

表 4-3. General-Purpose Input/Output (GPIO)

TERMINAL		SIGNAL TYPE	RESET PULL STATE	PULL TYPE	DESCRIPTION
SIGNAL NAME	100 PZ				
GIOA[0]/SPI3nCS[3]	1	I/O	Pulldown	Programmable, 20 µA	General-purpose input/output All GPIO terminals can generate interrupts to the CPU on rising/falling/both edges.
GIOA[1]/SPI3nCS[2]	2				
GIOA[2]/SPI3nCS[1]	5				
GIOA[3]/SPI2nCS[3]	8				
GIOA[4]/SPI2nCS[2]	9				
GIOA[5]/EXTCLKIN	10				
GIOA[6]/SPI2nCS[1]/N2HET[31]	12				
GIOA[7]/N2HET[29]	18				

4.2.4 Controller Area Network Interface Modules (DCAN1, DCAN2)

表 4-4. Controller Area Network Interface Modules (DCAN1, DCAN2)

TERMINAL		SIGNAL TYPE	RESET PULL STATE	PULL TYPE	DESCRIPTION
SIGNAL NAME	100 PZ				
CAN1RX	63	I/O	Pullup	Programmable, 20 µA	CAN1 Receive, or general-purpose I/O (GPIO)
CAN1TX	62				CAN1 Transmit, or GPIO
CAN2RX	92				CAN2 Receive, or GPIO
CAN2TX	91				CAN2 Transmit, or GPIO

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4.2.5 Multibuffered Serial Peripheral Interface (MibSPI1)

表 4-5. Multibuffered Serial Peripheral Interface (MibSPI1)

TERMINAL		SIGNAL TYPE	RESET PULL STATE	PULL TYPE	DESCRIPTION
SIGNAL NAME	100 PZ				
MIBSPI1CLK	67	I/O	Pullup	Programmable, 20 µA	MibSPI1 Serial Clock, or GPIO
MIBSPI1nCS[0]	73				MibSPI1 Chip Select, or GPIO
MIBSPI1nCS[1]/EQEPS/N2HET[17]	93				
MIBSPI1nCS[2]/N2HET[20]/N2HET[19]	27				
MIBSPI1nCS[3]/N2HET[26]	39				
MIBSPI1nENA/N2HET[23]/N2HET[30]	68				MibSPI1 Enable, or GPIO
MIBSPI1SIMO	65				MibSPI1 Slave-In-Master-Out, or GPIO
MIBSPI1SOMI	66				MibSPI1 Slave-Out-Master-In, or GPIO

4.2.6 Standard Serial Peripheral Interface (SPI2)

表 4-6. Standard Serial Peripheral Interface (SPI2)

TERMINAL		SIGNAL TYPE	RESET PULL STATE	PULL TYPE	DESCRIPTION
SIGNAL NAME	100 PZ				
SPI2CLK	71	I/O	Pullup	Programmable, 20 µA	SPI2 Serial Clock, or GPIO
SPI2nCS[0]	23				SPI2 Chip Select, or GPIO
GIOA[6]/**SPI2nCS[1]**/N2HET[31]	12				
GIOA[4]/**SPI2nCS[2]**	9				
GIOA[3]/**SPI2nCS[3]**	8				
SPI2SIMO	70				SPI2 Slave-In-Master-Out, or GPIO
SPI2SOMI	69				SPI2 Slave-Out-Master-In, or GPIO
The drive strengths for the SPI2CLK, SPI2SIMO, and SPI2SOMI signals are selected individually by configuring the respective SRS bits of the SPIPC9 register fo SPI2. SRS = 0 for 8-mA drive (fast). This is the default mode as the SRS bits in the SPIPC9 register default to 0. SRS = 1 for 2-mA drive (slow)					
SPI3CLK/EQEPA	36	I/O	Pullup	Programmable, 20 µA	SPI3 Serial Clock, or GPIO
SPI3nCS[0]/EQEPI	38				SPI3 Chip Select, or GPIO
GIOA[2]/**SPI3nCS[1]**	5				
GIOA[1]/**SPI3nCS[2]**	2				
GIOA[0]/**SPI3nCS[3]**	1				
SPI3nENA/EQEPB	37				SPI3 Enable, or GPIO
SPI3SIMO	35				SPI3 Slave-In-Master-Out, or GPIO
SPI3SOMI	34				SPI3 Slave-Out-Master-In, or GPIO

4.2.7 Local Interconnect Network Controller (LIN)

表 4-7. Local Interconnect Network Controller (LIN)

TERMINAL		SIGNAL TYPE	RESET PULL STATE	PULL TYPE	DESCRIPTION
SIGNAL NAME	100 PZ				
LINRX	94	I/O	Pullup	Programmable, 20 µA	LIN Receive, or GPIO
LINTX	95				LIN Transmit, or GPIO

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4.2.8 Multibuffered Analog-to-Digital Converter (MibADC)

表 4-8. Multibuffered Analog-to-Digital Converter (MibADC)

TERMINAL		SIGNAL TYPE	RESET PULL STATE	PULL TYPE	DESCRIPTION
SIGNAL NAME	100 PZ				
ADEVT/N2HET[28]	58	I/O	Pullup	Programmable, 20 µA	ADC event trigger or GPIO
ADIN[0]	42	Input	N/A	None	Analog inputs
ADIN[1]	49				
ADIN[2]	51				
ADIN[3]	52				
ADIN[4]	54				
ADIN[5]	55				
ADIN[6]	56				
ADIN[7]	43				
ADIN[8]	57				
ADIN[9]	48				
ADIN[10]	50				
ADIN[11]	53				
ADIN[16]	40				
ADIN[17]	41				
ADIN[20]	44				
ADIN[21]	45				
VCCAD/ADREFHI	46	Input/Power	N/A	None	ADC high reference level/ADC operating supply
VSSAD/ADREFLO	47	Input/Ground	N/A	None	ADC low reference level/ADC supply ground

4.2.9 System Module

表 4-9. System Module

TERMINAL		SIGNAL TYPE	RESET PULL STATE	PULL TYPE	DESCRIPTION
SIGNAL NAME	100 PZ				
ECLK	84	I/O	Pulldown	Programmable, 20 µA	External prescaled clock output, or GPIO.
GIOA[5]/**EXTCLKIN**	10	Input	Pulldown	20 µA	External Clock In
nPORRST	31	Input	Pulldown	100 µA	Power-on reset, cold reset External power supply monitor circuitry must drive nPORRST low when any of the supplies to the microcontroller fall out of the specified range. This terminal has a glitch filter.
nRST	81	I/O	Pullup	100 µA	The external circuitry can assert a system reset by driving nRST low. To ensure that an external reset is not arbitrarily generated, TI recommends that an external pullup resistor is connected to this terminal. This terminal has a glitch filter.

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4.2.10 Error Signaling Module (ESM)

表 4-10. Error Signaling Module (ESM)

TERMINAL		SIGNAL TYPE	RESET PULL STATE	PULL TYPE	DESCRIPTION
SIGNAL NAME	100 PZ				
nERROR	82	I/O	Pulldown	20 µA	ESM error signal. Indicates error of high severity.

4.2.11 Main Oscillator

表 4-11. Main Oscillator

TERMINAL		SIGNAL TYPE	RESET PULL STATE	PULL TYPE	DESCRIPTION
SIGNAL NAME	100 PZ				
OSCIN	14	Input	N/A	None	From external crystal/resonator, or external clock input
OSCOUT	16	Output	N/A	None	To external crystal/resonator
KELVIN_GND	15	Input	N/A	None	Dedicated ground for oscillator

4.2.12 Test/Debug Interface

表 4-12. Test/Debug Interface

TERMINAL		SIGNAL TYPE	RESET PULL STATE	PULL TYPE	DESCRIPTION
SIGNAL NAME	100 PZ				
nTRST	76	Input	Pulldown	Fixed, 100 µA	JTAG test hardware reset
RTCK	80	Output	N/A	None	JTAG return test clock
TCK	79	Input	Pulldown	Fixed, 100 µA	JTAG test clock
TDI	77	I/O	Pullup	Fixed, 100 µA	JTAG test data in
TDO	78	Output	Fixed, 100-µA Pulldown	None	JTAG test data out
TMS	75	I/O	Pullup	Fixed, 100 µA	JTAG test select
TEST	24	I/O	Pulldown	Fixed, 100 µA	Test enable. This terminal must be connected to ground directly or through a pulldown resistor.

4.2.13 Flash

表 4-13. Flash

TERMINAL		SIGNAL TYPE	RESET PULL STATE	PULL TYPE	DESCRIPTION
SIGNAL NAME	100 PZ				
FLTP1	3	Input	N/A	None	Flash test pins. For proper operation this terminal must connect only to a test pad or not be connected at all [no connect (NC)]. The test pad must not be exposed in the final product where it might be subjected to an ESD event.
FLTP2	4	Input	N/A	None	
VCCP	96	3.3-V Power	N/A	None	Flash external pump voltage (3.3 V). This terminal is required for both flash read and flash program and erase operations.

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4.2.14 Core Supply

表 4-14. Core Supply

TERMINAL		SIGNAL TYPE	RESET PULL STATE	PULL TYPE	DESCRIPTION
SIGNAL NAME	100 PZ				
VCC	13	1.2-V Power	N/A	None	Digital logic and RAM supply
VCC	21				
VCC	30				
VCC	32				
VCC	61				
VCC	88				
VCC	99				

4.2.15 I/O Supply

表 4-15. I/O Supply

TERMINAL		SIGNAL TYPE	RESET PULL STATE	PULL TYPE	DESCRIPTION
SIGNAL NAME	100 PZ				
VCCIO	6	3.3-V Power	N/A	None	I/O supply
VCCIO	28				
VCCIO	60				
VCCIO	85				

4.2.16 Core and I/O Supply Ground Reference

表 4-16. Core and I/O Supply Ground Reference

TERMINAL		SIGNAL TYPE	RESET PULL STATE	PULL TYPE	DESCRIPTION
SIGNAL NAME	100 PZ				
VSS	7	Ground	N/A	None	Device Ground Reference. This is a single ground reference for all supplies except for the ADC supply.
VSS	17				
VSS	20				
VSS	29				
VSS	33				
VSS	59				
VSS	72				
VSS	86				
VSS	87				
VSS	100				

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4.3 Output Multiplexing and Control

Output multiplexing will be used in the device. The multiplexing is used to allow development of additional package and feature combinations as well as to maintain pinout compatibility with the marketing device family.

In all cases indicated as multiplexed, the output buffers are multiplexed.

4.3.1 Notes on Output Multiplexing

表 4-17 shows the output signal multiplexing and control signals for selecting the desired functionality for each pin.

- The pins default to the signal defined by the DEFAULT FUNCTION column in 表 4-17
- The CONTROL 1, CONTROL 2, and CONTROL 3 columns indicate the multiplexing control register and the bit that must be set in order to select the corresponding functionality to be output on any particular pin.
  For example, consider the multiplexing on pin 18, shown in 表 4-18 .

表 4-17. Output Mux Options

100 PZ PIN	DEFAULT FUNCTION	CONTROL 1	OPTION2	CONTROL 2	OPTION 3	CONTROL 3
1	GIOA[0]	PINMMR0[8]	SPI3nCS[3]	PINMMR0[9]	–	–
2	GIOA[1]	PINMMR1[0]	SPI3nCS[2]	PINMMR1[1]	–	–
5	GIOA[2]	PINMMR1[8]	SPI3nCS[1]	PINMMR1[9]	–	–
8	GIOA[3]	PINMMR1[16]	SPI2nCS[3]	PINMMR1[17]	–	–
9	GIOA[4]	PINMMR1[24]	SPI2nCS[2]	PINMMR1[25]	–	–
10	GIOA[5]	PINMMR2[0]	EXTCLKIN	PINMMR2[1]	–	–
12	GIOA[6]	PINMMR2[8]	SPI2nCS[1]	PINMMR2[9]	N2HET[31]	PINMMR2[10]
18	GIOA[7]	PINMMR2[16]	N2HET[29]	PINMMR2[17]	–	–
93	MIBSPI1nCS[1]	PINMMR6[8]	EQEPS	PINMMR6[9]	N2HET[17]	PINMMR6[10]
27	MIBSPI1nCS[2]	PINMMR3[0]	N2HET[20]	PINMMR3[1]	N2HET[19]	PINMMR3[2]
39	MIBSPI1nCS[3]	PINMMR4[8]	N2HET[26]	PINMMR4[9]	–	–
68	MIBSPI1nENA	PINMMR5[8]	N2HET[23]	PINMMR5[9]	N2HET[30]	PINMMR5[10]
36	SPI3CLK	PINMMR3[16]	EQEPA	PINMMR3[17]	–	–
38	SPI3nCS[0]	PINMMR4[0]	EQEPI	PINMMR4[1]	–	–
37	SPI3nENA	PINMMR3[24]	EQEPB	PINMMR3[25]	–	–
58	ADEVT	PINMMR4[16]	N2HET[28]	PINMMR4[17]	–	–

表 4-18. Muxing Example

100 PZ PIN	DEFAULT FUNCTION	CONTROL 1	OPTION2	CONTROL 2	OPTION 3	CONTROL 3
18	GIOA[7]	PINMMR2[16]	N2HET[29]	PINMMR2[17]	–	–

- When GIOA[7] is configured as an output pin in the GPIO module control register, then the programmed output level appears on pin 18 by default. The PINMMR2[16] bit is set by default to indicate that the GIOA[7] signal is selected to be output.
- If the application must output the N2HET[29] signal on pin 18, it must clear PINMMR2[16] and set PINMMR2[17].
- The pin is connected as input to both the GPIO and N2HET modules. That is, there is no input multiplexing on this pin.

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4.3.2 General Rules for Multiplexing Control Registers

- The PINMMR control registers can only be written in privileged mode. A write in a nonprivileged mode will generate an error response.
- If the application writes all 0s to any PINMMR control register, then the default functions are selected for the affected pins.
- Each byte in a PINMMR control register is used to select the functionality for a given pin. If the application sets more than 1 bit within a byte for any pin, then the default function is selected for this pin.
- Some bits within the PINMMR registers could be associated with internal pads that are not brought out in the 100-pin package. As a result, bits marked reserved should not be written as 1.

4.4 Special Multiplexed Options

Special controls are implemented to affect particular functions on this microcontroller. These controls are described in this section.

4.4.1 Filtering for eQEP Inputs

4.4.1.1 eQEPA Input

- When PINMMR8[0] = 1, the eQEPA input is double-synchronized using VCLK.
- When PINMMR8[0] = 0 and PINMMR8[1] = 1, the eQEPA input is double-synchronized and then qualified through a fixed 6-bit counter using VCLK.
- PINMMR8[0] = 0 and PINMMR8[1] = 0 is an illegal combination and behavior defaults to PINMMR8[0] = 1.

4.4.1.2 eQEPB Input

- When PINMMR8[8] = 1, the eQEPB input is double-synchronized using VCLK.
- When PINMMR8[8] = 0 and PINMMR8[9] = 1, the eQEPB input is double-synchronized and then qualified through a fixed 6-bit counter using VCLK.
- PINMMR8[8] = 0 and PINMMR8[9] = 0 is an illegal combination and behavior defaults to PINMMR8[8] = 1.

4.4.1.3 eQEPI Input

- When PINMMR8[16] = 1, the eQEPI input is double-synchronized using VCLK.
- When PINMMR8[16] = 0 and PINMMR8[17] = 1, the eQEPI input is double-synchronized and then qualified through a fixed 6-bit counter using VCLK.
- PINMMR8[16] = 0 and PINMMR8[17] = 0 is an illegal combination and behavior defaults to PINMMR8[16] = 1.

4.4.1.4 eQEPS Input

- When PINMMR8[24] = 1, the eQEPS input is double-synchronized using VCLK.
- When PINMMR8[24] = 0 and PINMMR8[25] = 1, the eQEPS input is double-synchronized and then qualified through a fixed 6-bit counter using VCLK.
- PINMMR8[24] = 0 and PINMMR8[25] = 0 is an illegal combination and behavior defaults to PINMMR8[24] = 1.

4.4.2 N2HET PIN_nDISABLE Input Port

- When PINMMR9[0] = 1, GIOA[5] is connected directly to N2HET PIN_nDISABLE input of the N2HET module.
- When PINMMR9[0] = 0 and PINMMR9[1] = 1, EQEPERR is inverted and double-synchronized using VCLK before connecting directly to the N2HET PIN_nDISABLE input of the N2HET module.
- PINMMR9[0] = 0 and PINMMR9[1] = 0 is an illegal combination and behavior defaults to PINMMR9[0] = 1.

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5 Specifications

5.1 Absolute Maximum Ratings(1)

Over Operating Free-Air Temperature Range

		MIN	MAX	UNIT
Supply voltage	V_{CC}(2)	–0.3	1.43	V
	V_{CCIO}, V_{CCP}(2)	–0.3	4.6	
	V_{CCAD}	–0.3	4.6	
Input voltage	All input pins	–0.3	4.6	V
	ADC input pins	–0.3	4.6	
Input clamp current	I_{IK} (V_I < 0 or V_I > V_{CCIO}) All pins, except ADIN[21:20,17:16,11:0]	–20	20	mA
	I_{IK} (V_I < 0 or V_I > V_{CCAD}) ADIN[21:20,17:16,11:0]	–10	10	
	Total	–40	40	
Operating free-air temperature, T_A		–40	125	°C
Operating junction temperature, T_J		–40	150	°C
Latch-up performance	I-test, All I/O pins	–100	100	mA
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to their associated grounds.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge (ESD) performance:	Human Body Model (HBM), per AEC Q100-002(1)		±2	kV
		Charged Device Model (CDM), per AEC Q100-011	All pins except corner pins	±500	V
			Corner pins (1, 25, 26, 50, 51, 75, 76, 100)	±750	V

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Power-On Hours (POH)(1)(2)

NOMINAL CORE VOLTAGE (V_{CC})	JUNCTION TEMPERATURE (Tj)	LIFETIME POH
1.2	105ºC	100K

(1) This information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.
(2) To avoid significant degradation, the device power-on hours (POH) must be limited to those specified in this table. To convert to equivalent POH for a specific temperature profile, see the *Calculating Equivalent Power-on-Hours for Hercules Safety MCUs* Application Report (SPNA207).

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5.4 Recommended Operating Conditions(1)

		MIN	NOM	MAX	UNIT
V_{CC}	Digital logic supply voltage (Core)	1.14	1.2	1.32	V
V_{CCIO}	Digital logic supply voltage (I/O)	3	3.3	3.6	V
V_{CCAD} / $V_{ADREFHI}$	MibADC supply voltage / A-to-D high-voltage reference source	3	3.3	3.6	V
V_{CCP}	Flash pump supply voltage	3	3.3	3.6	V
V_{SS}	Digital logic supply ground		0		V
V_{SSAD} / $V_{ADREFLO}$	MibADC supply ground / A-to-D low-voltage reference source	–0.1		0.1	V
V_{SLEW}	Maximum positive slew rate for V_{CCIO}, V_{CCAD} and V_{CCP} supplies			1	V/µs
T_A	Operating free-air temperature	–40		125	°C
T_J	Operating junction temperature(2)	–40		150	°C

(1) All voltages are with respect to V_{SS}, except V_{CCAD}, which is with respect to V_{SSAD}
(2) Reliability data is based upon a temperature profile that is equivalent to 100,000 power-on hours at 105°C junction temperature.

5.5 Switching Characteristics Over Recommended Operating Conditions for Clock Domains

表 5-1. Clock Domains Timing Specifications

PARAMETER		CONDITIONS	MIN	MAX	UNIT
f_{HCLK}	HCLK - System clock frequency			80	MHz
f_{GCLK}	GCLK - CPU clock frequency (ratio f_{GCLK} : f_{HCLK} = 1:1)			f_{HCLK}	MHz
f_{VCLK}	VCLK - Primary peripheral clock frequency			80	MHz
f_{VCLK2}	VCLK2 - Secondary peripheral clock frequency			80	MHz
f_{VCLKA1}	VCLKA1 - Primary asynchronous peripheral clock frequency			80	MHz
f_{RTICLK}	RTICLK - clock frequency			f_{VCLK}	MHz

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5.6 Wait States Required

The TCM RAM can support program and data fetches at full CPU speed without any address or data wait states required. There are no registers which need to be programmed for RAM wait states.

The TCM flash can support zero address and data wait states up to a CPU speed of 45 MHz in nonpipelined mode.The flash supports a maximum CPU clock speed of 80 MHz in pipelined mode with no address wait states and one data wait state.

The proper wait states should be set in the register fields *Address Setup Wait State Enable* (ASWSTEN 0xFFF87000[4]), *Random Wait states* (RWAIT 0xFFF87000[11:8]), and *Emulation Wait states* (EWAIT 0xFFF872B8[19:16]) as shown in 図 5-1.

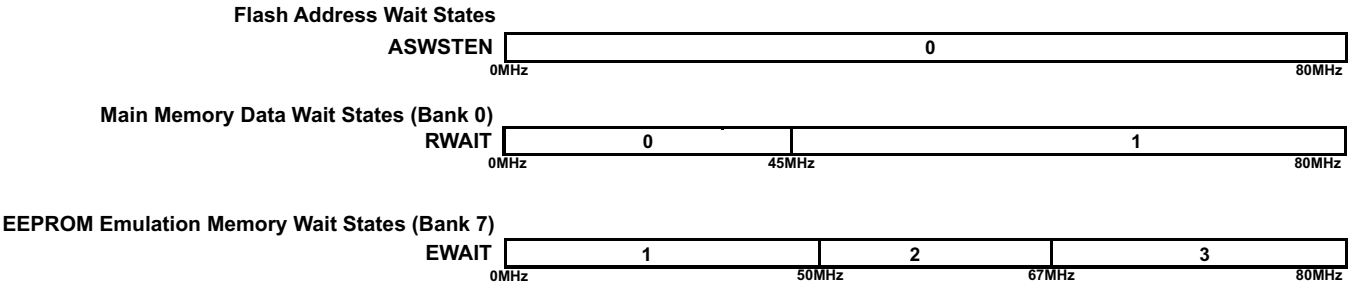

図 5-1. Wait States Scheme

The flash wrapper defaults to nonpipelined mode with address wait states disabled, ASWSTEN=0; the main memory random-read data wait state, RWAIT=1; and the emulation memory random-read wait states, EWAIT=1.

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5.7 Power Consumption

Over Recommended Operating Conditions

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	V_{CC} digital supply current (operating mode)	f_{HCLK} = 80 MHz f_{VCLK} = 80 MHz, Flash in pipelined mode, V_{CCmax}			135 (1)	mA
	V_{CC} digital supply current (LBIST mode)	LBIST clock rate = 45 MHz			145 (2) (3)	
	V_{CC} digital supply current (PBIST mode)	PBIST ROM clock frequency = 80 MHz			135 (2) (3)	
$I_{CCREFHI}$ + I_{CCAD} + I_{CCIO} + I_{CCP}	Sum of Flash, IO and ADC 3.3V supply currents	$V_{ADREFHI}$ = $V_{ADREFHImax}$ V_{CCAD} = $V_{CCADmax}$ V_{CCIO} = $V_{CCIOmax}$, No Load on output pins V_{CCP} = V_{CCPmax}, Reading from flash			48	mA
		$V_{ADREFHI}$ = $V_{ADREFHImax}$ V_{CCAD} = $V_{CCADmax}$ V_{CCIO} = $V_{CCIOmax}$, No Load on output pins V_{CCP} = V_{CCPmax}, Reading from one bank of flash while programming or erasing another bank			68	

(1) The maximum I_{CC}, value can be derated
- linearly with voltage
- by 0.76 mA/MHz for lower operating frequency when f_{HCLK}= f_{VCLK}
- for lower junction temperature by the equation below where T_{JK} is the junction temperature in Kelvin and the result is in milliamperes. **$60 - 0.001\ e^{0.026\ T_{JK}}$**

(2) The maximum I_{CC}, value can be derated
- linearly with voltage
- for lower junction temperature by the equation below where T_{JK} is the junction temperature in Kelvin and the result is in milliamperes. **$60 - 0.001\ e^{0.026\ T_{JK}}$**

(3) LBIST and PBIST currents are for a short duration, typically less than 10 ms. They are usually ignored for thermal calculations for the device and the voltage regulator

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5.8 Thermal Resistance Characteristics for PZ

表 5-2 shows the thermal resistance characteristics for the PQFP - PZ mechanical packages.

表 5-2. Thermal Resistance Characteristics (S-PQFP Package) [PZ]

PARAMETER	°C/W
$R_{\theta JA}$	48
$R_{\theta JC}$	5

5.9 Input/Output Electrical Characteristics(1)

Over Recommended Operating Conditions

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{hys}	Input hysteresis	All inputs		180			mV
V_{IL}	Low-level input voltage	All inputs(2)		–0.3		0.8	V
V_{IH}	High-level input voltage	All inputs(2)		2		V_{CCIO} + 0.3	V
V_{OL}	Low-level output voltage		I_{OL} = I_{OLmax}			0.2 V_{CCIO}	V
			I_{OL} = 50 µA, standard output mode			0.2	
V_{OH}	High-level output voltage		I_{OH} = I_{OHmax}	0.8 V_{CCIO}			V
			I_{OH} = 50 µA, standard output mode	V_{CCIO} - 0.3			
I_{IC}	Input clamp current (I/O pins)		V_I < V_{SSIO} - 0.3 or V_I > V_{CCIO} + 0.3	–3.5		3.5	mA
I_I	Input current (I/O pins)	I_{IH} 20-µA pulldown	V_I = V_{CCIO}	5		40	µA
		I_{IH} 100-µA pulldown	V_I = V_{CCIO}	40		195	
		I_{IL} 20-µA pullup	V_I = V_{SS}	–40		–5	
		I_{IL} 100-µA pullup	V_I = V_{SS}	–195		–40	
		All other pins	No pullup or pulldown	–1		1	
C_I	Input capacitance					2	pF
C_O	Output capacitance					3	pF

(1) Source currents (out of the device) are negative while sink currents (into the device) are positive.
(2) This does not apply to the nPORRST pin.

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5.10 Output Buffer Drive Strengths

表 5-3. Output Buffer Drive Strengths

LOW-LEVEL OUTPUT CURRENT, I_{OL} for $V_I=V_{OLmax}$ or HIGH-LEVEL OUTPUT CURRENT, I_{OH} for $V_I=V_{OHmin}$	SIGNALS
8 mA	EQEPI, EQEPS, TMS, TDI, TDO, RTCK, nERROR
4 mA	TEST, MIBSPI1SIMO, MIBSPI1SOMI, MIBSPI1CLK, SPI3CLK, SPI3SIMO, SPI3SOMI, nRST
2 mA zero-dominant	AD1EVT, CAN1RX, CAN1TX, CAN2RX, CAN2TX, GIOA[0-7], LINRX, LINTX, MIBSPI1nCS[0-3], MIBSPI1nENA N2HET[0], N2HET[2], N2HET[4], N2HET[6], N2HET[8], N2HET[10], N2HET[12], N2HET[14], N2HET[16], N2HET[18], N2HET[22], N2HET[24], SPI2nCS[0-3], SPI3nENA, SPI3nCS[0]
selectable 8 mA/ 2 mA	ECLK, SPI2CLK, SPI2SIMO, SPI2SOMI The default output buffer drive strength is 8 mA for these signals.

表 5-4. Selectable 8 mA/ 2 mA Control

SIGNAL	CONTROL BIT	ADDRESS	8 mA	2 mA
ECLK	SYSPC10[0]	0xFFFF FF78	0	1
SPI2CLK	SPI2PC9[9]	0xFFF7 F668	0	1
SPI2SIMO	SPI2PC9[10]	0xFFF7 F668	0	1
SPI2SOMI	SPI2PC9[11](1)	0xFFF7 F668	0	1

(1) Either SPI2PC9[11] or SPI2PC9[24] can change the output strength of the SPI2SOMI pin. In case of a 32-bit write where these 2 bits differ, SPI2PC9[11] determines the drive strength.

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5.11 Input Timings

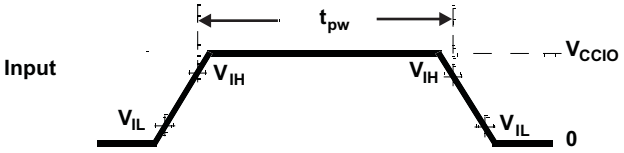

図 5-2. TTL-Level Inputs

表 5-5. Timing Requirements for Inputs(1)

		MIN	MAX	UNIT
t_{pw}	Input minimum pulse width	$t_{c(VCLK)}$ + 10(2)		ns

(1) $t_{c(VCLK)}$ = peripheral VBUS clock cycle time = 1 / $f_{(VCLK)}$
(2) The timing shown in 図 5-2 is only valid for pin used in GIO mode.

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5.12 Output Timings

表 5-6. Switching Characteristics for Output Timings versus Load Capacitance (CL)

PARAMETER				MIN	MAX	UNIT
Rise time, t_r	8-mA pins		CL = 15 pF		2.5	ns
			CL = 50 pF		4	
			CL = 100 pF		7.2	
			CL = 150 pF		12.5	
Fall time, t_f			CL = 15 pF		2.5	
			CL = 50 pF		4	
			CL = 100 pF		7.2	
			CL = 150 pF		12.5	
Rise time, t_r	4-mA pins		CL = 15 pF		5.6	ns
			CL = 50 pF		10.4	
			CL = 100 pF		16.8	
			CL = 150 pF		23.2	
Fall time, t_f			CL = 15 pF		5.6	
			CL= 50 pF		10.4	
			CL = 100 pF		16.8	
			CL = 150 pF		23.2	
Rise time, t_r	2-mA-z pins		CL = 15 pF		8	ns
			CL = 50 pF		15	
			CL = 100 pF		23	
			CL = 150 pF		33	
Fall time, t_f			CL = 15 pF		8	
			CL = 50 pF		15	
			CL = 100 pF		23	
			CL = 150 pF		33	
Rise time, t_r	Selectable 8-mA/ 2-mA-z pins	8-mA mode	CL = 15 pF		2.5	ns
			CL = 50 pF		4	
			CL = 100 pF		7.2	
			CL = 150 pF		12.5	
Fall time, t_f			CL = 15 pF		2.5	
			CL = 50 pF		4	
			CL = 100 pF		7.2	
			CL = 150 pF		12.5	
Rise time, t_r		2-mA-z mode	CL = 15 pF		8	
			CL = 50 pF		15	
			CL = 100 pF		23	
			CL = 150 pF		33	
Fall time, t_f			CL = 15 pF		8	
			CL = 50 pF		15	
			CL = 100 pF		23	
			CL = 150 pF		33	

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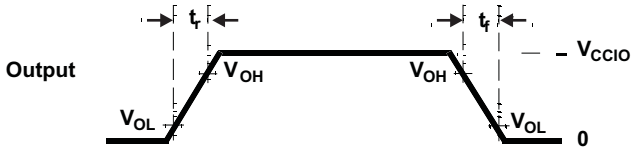

図 5-3. CMOS-Level Outputs

表 5-7. Timing Requirements for Outputs(1)

PARAMETER		MIN	MAX	UNIT
$t_{d(parallel_out)}$	Delay between low-to-high, or high-to-low transition of general-purpose output signals that can be configured by an application in parallel, for example, all signals in a GIOA port, or all N2HET signals.		5	ns

(1) This specification does not account for any output buffer drive strength differences or any external capacitive loading differences. Check 表 5-3 for output buffer drive strength information on each signal.

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6 System Information and Electrical Specifications

6.1 Voltage Monitor Characteristics

A voltage monitor is implemented on this device. The purpose of this voltage monitor is to eliminate the requirement for a specific sequence when powering up the core and I/O voltage supplies.

6.1.1 Important Considerations

- The voltage monitor does not eliminate the need of a voltage supervisor circuit to ensure that the device is held in reset when the voltage supplies are out of range.
- The voltage monitor only monitors the core supply (VCC) and the I/O supply (VCCIO). The other supplies are not monitored by the VMON. For example, if the VCCAD or VCCP are supplied from a source different from that for VCCIO, then there is no internal voltage monitor for the VCCAD and VCCP supplies.

6.1.2 Voltage Monitor Operation

The voltage monitor generates the Power Good MCU signal (PGMCU) as well as the I/Os Power Good I/O signal (PGIO) on the device. During power up or power down, the PGMCU and PGIO are driven low when the core or I/O supplies are lower than the specified minimum monitoring thresholds. The PGIO and PGMCU being low isolates the core logic as well as the I/O controls during the power up or power down of the supplies. This allows the core and I/O supplies to be powered up or down in any order.

When the voltage monitor detects a low voltage on the I/O supply, it will assert a power-on reset. When the voltage monitor detects an out-of-range voltage on the core supply, it asynchronously makes all output pins high impedance, and asserts a power-on reset. The voltage monitor is disabled when the device enters a low power mode.

The VMON also incorporates a glitch filter for the nPORRST input. Refer to 6.2.3.1 for the timing information on this glitch filter.

表 6-1. Voltage Monitoring Specifications

PARAMETER			MIN	TYP	MAX	UNIT
V_{MON}	Voltage monitoring thresholds	VCC low - VCC level below this threshold is detected as too low.	0.75	0.9	1.13	V
		VCC high - VCC level above this threshold is detected as too high.	1.40	1.7	2.1	
		VCCIO low - VCCIO level below this threshold is detected as too low.	1.85	2.4	2.9	

6.1.3 Supply Filtering

The VMON has the capability to filter glitches on the VCC and VCCIO supplies.

表 6-2 shows the characteristics of the supply filtering. Glitches in the supply larger than the maximum specification cannot be filtered.

表 6-2. VMON Supply Glitch Filtering Capability

PARAMETER	MIN	MAX	UNIT
Width of glitch on VCC that can be filtered	250	1000	ns
Width of glitch on VCCIO that can be filtered	250	1000	ns

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6.2 Power Sequencing and Power-On Reset

6.2.1 Power-Up Sequence

There is no timing dependency between the ramp of the VCCIO and the VCC supply voltage. The power-up sequence starts with the I/O voltage rising above the minimum I/O supply threshold, (for more details, see 表 6-4), core voltage rising above the minimum core supply threshold, and the release of power-on reset. The high-frequency oscillator will start up first and its amplitude will grow to an acceptable level. The oscillator start-up time is dependent on the type of oscillator and is provided by the oscillator vendor. The different supplies to the device can be powered up in any order.

During power up, the device goes through the sequential phases listed in 表 6-3.

表 6-3. Power-Up Phases

Oscillator start-up and validity check	1032 oscillator cycles
eFuse autoload	1160 oscillator cycles
Flash pump power up	688 oscillator cycles
Flash bank power up	617 oscillator cycles
Total	**3497 oscillator cycles**

The CPU reset is released at the end of this sequence and fetches the first instruction from address 0x00000000.

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6.2.2 Power-Down Sequence

The different supplies to the device can be powered down in any order.

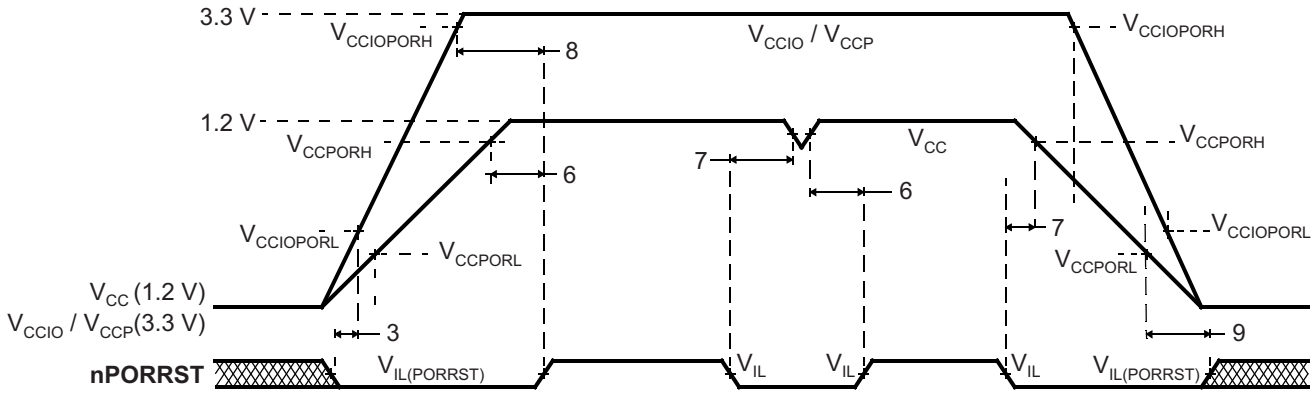
6.2.3 Power-On Reset: nPORRST

This reset must be asserted by an external circuitry whenever the I/O or core supplies are outside the recommended range. This signal has a glitch filter on it. It also has an internal pulldown.

6.2.3.1 nPORRST Electrical and Timing Requirements

表 6-4. Electrical Requirements for nPORRST

NO.	PARAMETER		MIN	MAX	UNIT
	V_{CCPORL}	V_{CC} low supply level when nPORRST must be active during power up		0.5	V
	V_{CCPORH}	V_{CC} high supply level when nPORRST must remain active during power up and become active during power down	1.14		V
	$V_{CCIOPORL}$	V_{CCIO} / V_{CCP} low supply level when nPORRST must be active during power up		1.1	V
	$V_{CCIOPORH}$	V_{CCIO} / V_{CCP} high supply level when nPORRST must remain active during power up and become active during power down	3.0		V
	$V_{IL(PORRST)}$	Low-level input voltage of nPORRST V_{CCIO} > 2.5 V		0.2 * V_{CCIO}	V
		Low-level input voltage of nPORRST V_{CCIO} < 2.5 V		0.5	V
3	$t_{su(PORRST)}$	Setup time, nPORRST active before V_{CCIO} and V_{CCP} > $V_{CCIOPORL}$ during power up	0		ms
6	$t_{h(PORRST)}$	Hold time, nPORRST active after V_{CC} > V_{CCPORH}	1		ms
7	$t_{su(PORRST)}$	Setup time, nPORRST active before V_{CC} < V_{CCPORH} during power down	2		µs
8	$t_{h(PORRST)}$	Hold time, nPORRST active after V_{CCIO} and V_{CCP} > $V_{CCIOPORH}$	1		ms
9	$t_{h(PORRST)}$	Hold time, nPORRST active after V_{CC} < V_{CCPORL}	0		ms
	$t_{f(nPORRST)}$	Filter time nPORRST pin; Pulses less than MIN will be filtered out, pulses greater than MAX will generate a reset.	475	2000	ns



Note: There is no timing dependency between the ramp of the V_{CCIO} and the V_{CC} supply voltage; this is just an example.

図 6-1. nPORRST Timing Diagram

6.3 Warm Reset (nRST)

This is a bidirectional reset signal. The internal circuitry drives the signal low on detecting any device reset condition. An external circuit can assert a device reset by forcing the signal low. On this terminal, the output buffer is implemented as an open drain (drives low only). To ensure an external reset is not arbitrarily generated, TI recommends that an external pullup resistor is connected to this terminal.

This terminal has a glitch filter. It also has an internal pullup

6.3.1 Causes of Warm Reset

表 6-5. Causes of Warm Reset

DEVICE EVENT	SYSTEM STATUS FLAG
Power-up reset	Exception Status Register, bit 15
Oscillator fail	Global Status Register, bit 0
PLL slip	Global Status Register, bits 8 and 9
Watchdog exception / Debugger reset	Exception Status Register, bit 13
CPU Reset (driven by the CPU STC)	Exception Status Register, bit 5
Software reset	Exception Status Register, bit 4
External reset	Exception Status Register, bit 3

6.3.2 nRST Timing Requirements

表 6-6. nRST Timing Requirements

		MIN	MAX	UNIT
$t_{v(RST)}$	Valid time, nRST active after nPORRST inactive	$2256t_{c(OSC)}$ (1)		ns
	Valid time, nRST active (all other system reset conditions)	$32t_{c(VCLK)}$		
$t_{f(nRST)}$	Filter time nRST pin; Pulses less than MIN will be filtered out, pulses greater than MAX will generate a reset	475	2000	ns

(1) Assumes the oscillator has started up and stabilized before nPORRST is released.

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6.4 ARM Cortex-R4 CPU Information

6.4.1 Summary of ARM Cortex-R4 CPU Features

The features of the ARM Cortex-R4 CPU include:

- An integer unit with integral Embedded ICE-RT logic.
- High-speed Advanced Microprocessor Bus Architecture (AMBA) Advanced eXtensible Interfaces (AXI) for Level two (L2) master and slave interfaces.
- Dynamic branch prediction with a global history buffer, and a 4-entry return stack
- Low interrupt latency.
- Nonmaskable interrupt.
- A Harvard Level one (L1) memory system with:
  - Tightly Coupled Memory (TCM) interfaces with support for error correction or parity checking memories
  - ARMv7-R architecture Memory Protection Unit (MPU) with 8 regions
- Dual core logic for fault detection in safety-critical applications.
- An L2 memory interface:
  - Single 64-bit master AXI interface
  - 64-bit slave AXI interface to TCM RAM blocks
- A debug interface to a CoreSight Debug Access Port (DAP).
- Six Hardware Breakpoints
- Two Watchpoints
- A Perfomance Monitoring Unit (PMU)
- A Vectored Interrupt Controller (VIC) port.

For more information on the ARM Cortex-R4 CPU, see www.arm.com.

6.4.2 ARM Cortex-R4 CPU Features Enabled by Software

The following CPU features are disabled on reset and must be enabled by the application if required.

- ECC On Tightly Coupled Memory (TCM) Accesses
- Hardware Vectored Interrupt (VIC) Port
- Memory Protection Unit (MPU)

6.4.3 Dual Core Implementation

The device has two Cortex-R4 cores, where the output signals of both CPUs are compared in the CCM-R4 unit. To avoid common mode impacts the signals of the CPUs to be compared are delayed by 2 clock cycles as shown in 図 6-3.

The CPUs have a diverse CPU placement given by following requirements:

- Different orientation; for example, CPU1 = "north" orientation, CPU2 = "flip west" orientation
- Dedicated guard ring for each CPU

図 6-2. Dual - CPU Orientation

6.4.4 Duplicate clock tree after GCLK

The CPU clock domain is split into two clock trees, one for each CPU, with the clock of the 2nd CPU running at the same frequency and in phase to the clock of CPU1. See 図 6-3.

6.4.5 ARM Cortex-R4 CPU Compare Module (CCM) for Safety

This device has two ARM Cortex-R4 CPU cores, where the output signals of both CPUs are compared in the CCM-R4 unit. To avoid common mode impacts the signals of the CPUs to be compared are delayed in a different way as shown in 図 6-3.

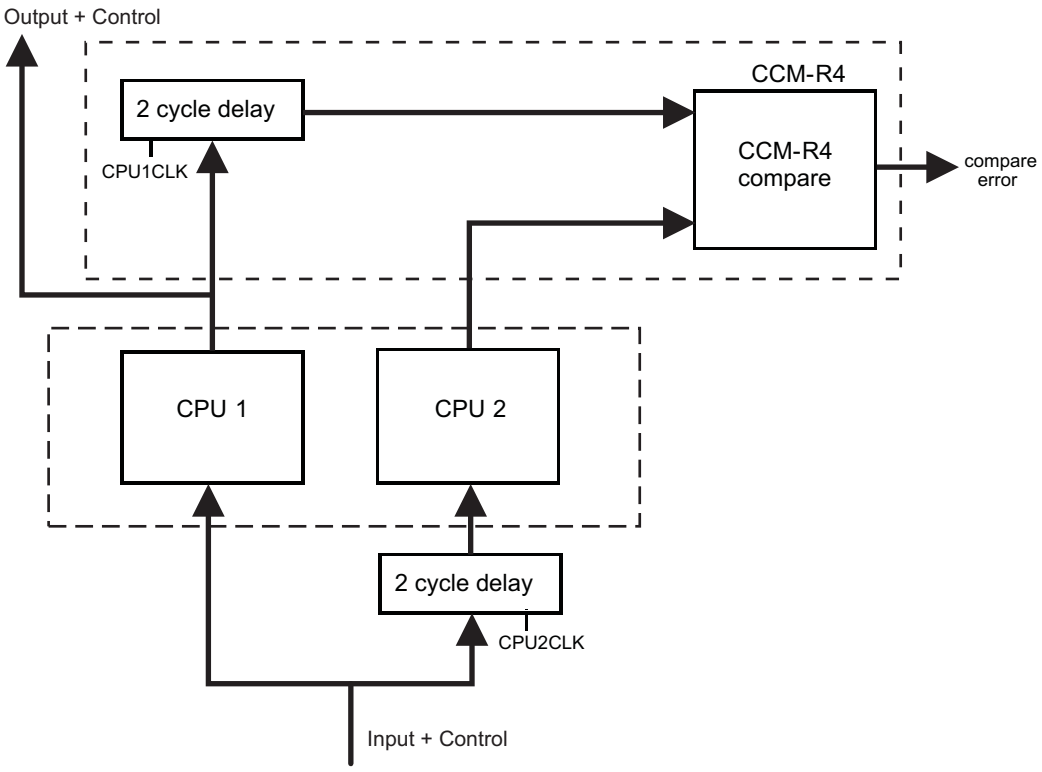

図 6-3. Dual Core Implementation

To avoid an erroneous CCM-R4 compare error, the application software must initialize the registers of both CPUs before the registers are used, including function calls where the register values are pushed onto the stack.

6.4.6 CPU Self-Test

The CPU STC (Self-Test Controller) is used to test the two Cortex-R4 CPU Cores using the Deterministic Logic BIST Controller as the test engine.

The main features of the self-test controller are:

- Ability to divide the complete test run into independent test intervals
- Capable of running the complete test or running a few intervals at a time
- Ability to continue from the last executed interval (test set) or to restart from the beginning (first test set)
- Complete isolation of the self-tested CPU core from the rest of the system during the self-test run
- Ability to capture the failure interval number
- Timeout counter for the CPU self-test run as a fail-safe feature

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6.4.6.1 Application Sequence for CPU Self-Test

1. Configure clock domain frequencies.
2. Select the number of test intervals to be run.
3. Configure the timeout period for the self-test run.
4. Save the CPU state if required
5. Enable self-test.
6. Wait for CPU reset.
7. In the reset handler, read CPU self-test status to identify any failures.
8. Retrieve CPU state if required.

For more information, see the *TMS570LS04x/03x 16/32-Bit RISC Flash Microcontroller Technical Reference Manual* (SPNU517).

6.4.6.2 CPU Self-Test Clock Configuration

The maximum clock rate for the self-test is 45 MHz. The STCCLK is divided down from the CPU clock, when necessary. This divider is configured by the STCCLKDIV register at address 0xFFFFE108.

6.4.6.3 CPU Self-Test Coverage

表 6-7 shows CPU test coverage achieved for each self-test interval. It also lists the cumulative test cycles. The test time can be calculated by multiplying the number of test cycles with the STC clock period.

表 6-7. CPU Self-Test Coverage

INTERVALS	TEST COVERAGE, %	TEST CYCLES
0	0	0
1	60.06	1365
2	68.71	2730
3	73.35	4095
4	76.57	5460
5	78.7	6825
6	80.4	8190
7	81.76	9555
8	82.94	10920
9	83.84	12285
10	84.58	13650
11	85.31	15015
12	85.9	16380
13	86.59	17745
14	87.17	19110
15	87.67	20475
16	88.11	21840
17	88.53	23205
18	88.93	24570
19	89.26	25935
20	89.56	27300
21	89.86	28665
22	90.1	30030
23	90.36	31395
24	90.62	32760

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表 6-7. CPU Self-Test Coverage (continued)

INTERVALS	TEST COVERAGE, %	TEST CYCLES
25	90.86	34125
26	91.06	35490

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6.5 Clocks

6.5.1 Clock Sources

The table below lists the available clock sources on the device. Each of the clock sources can be enabled or disabled using the CSDISx registers in the system module. The clock source number in the table corresponds to the control bit in the CSDISx register for that clock source.

The table also shows the default state of each clock source.

表 6-8. Available Clock Sources

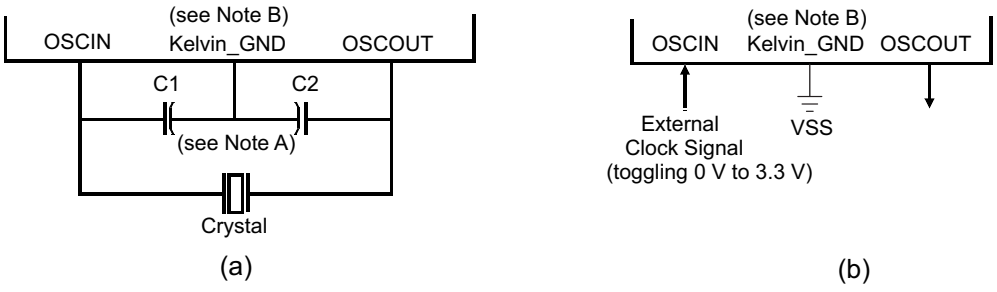
CLOCK SOURCE NO.	NAME	DESCRIPTION	DEFAULT STATE
0	OSCIN	Main Oscillator	Enabled
1	PLL1	Output From PLL1	Disabled
2	Reserved	Reserved	Disabled
3	EXTCLKIN1	External Clock Input #1	Disabled
4	CLK80K	Low-Frequency Output of Internal Reference Oscillator	Enabled
5	CLK10M	High-Frequency Output of Internal Reference Oscillator	Enabled
6	Reserved	Reserved	Disabled
7	Reserved	Reserved	Disabled

6.5.1.1 Main Oscillator

The oscillator is enabled by connecting the appropriate fundamental resonator/crystal and load capacitors across the external OSCIN and OSCOUT pins as shown in 図 6-4. The oscillator is a single stage inverter held in bias by an integrated bias resistor. This resistor is disabled during leakage test measurement and low power modes.

TI strongly encourages each customer to submit samples of the device to the resonator/crystal vendors for validation. The vendors are equipped to determine what load capacitors will best tune their resonator/crystal to the microcontroller device for optimum start-up and operation over temperature/voltage extremes.

An external oscillator source can be used by connecting a 3.3 V clock signal to the OSCIN pin and leaving the OSCOUT pin unconnected (open) as shown in 図 6-4.



Note A: The values of C1 and C2 should be provided by the resonator/crystal vendor.
Note B: Kelvin_GND should not be connected to any other GND when used with a crystal; however, when used with an external clock source, Kelvin_GND may be tied to VSS.

図 6-4. Recommended Crystal/Clock Connection

6.5.1.1.1 Timing Requirements for Main Oscillator

表 6-9. Timing Requirements for Main Oscillator

PARAMETER		MIN	TYP	MAX	UNIT
tc(OSC)	Cycle time, OSCIN (when using a sine-wave input)	50		200	ns
tc(OSC_SQR)	Cycle time, OSCIN, (when input to the OSCIN is a square wave)	50		200	ns
tw(OSCIL)	Pulse duration, OSCIN low (when input to the OSCIN is a square wave)	15			ns
tw(OSCIH)	Pulse duration, OSCIN high (when input to the OSCIN is a square wave)	15			ns

6.5.1.2 Low-Power Oscillator

The Low-Power Oscillator (LPO) is comprised of two oscillators — HF LPO and LF LPO.

6.5.1.2.1 Features

The main features of the LPO are:

- Supplies a clock at extremely low power for power-saving modes. This is connected as clock source # 4 of the Global Clock Module.
- Supplies a high-frequency clock for nontiming-critical systems. This is connected as clock source # 5 of the Global Clock Module.
- Provides a comparison clock for the crystal oscillator failure detection circuit.

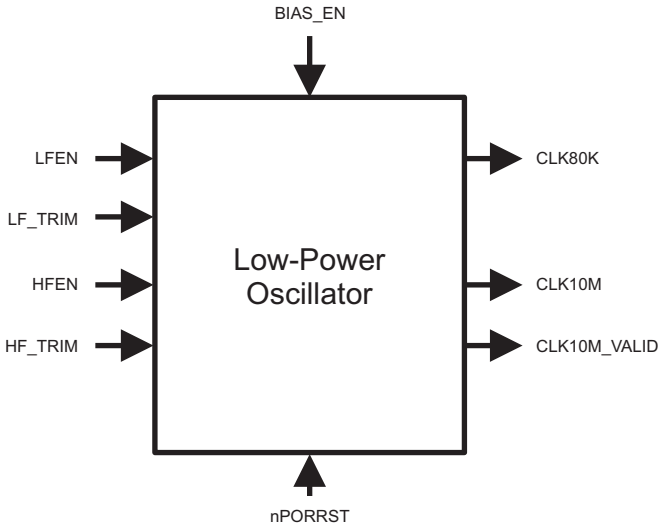


図 6-5. LPO Block Diagram

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図 6-5 shows a block diagram of the internal reference oscillator. This is an LPO and provides two clock sources: one nominally 80 kHz and one nominally 10 MHz.

6.5.1.2.2 LPO Electrical and Timing Specifications

表 6-10. LPO Specifications

PARAMETER		MIN	TYP	MAX	UNIT
Clock Detection	Oscillator fail frequency - lower threshold, using untrimmed LPO output	1.375	2.4	4.875	MHz
	Oscillator fail frequency - higher threshold, using untrimmed LPO output	22	38.4	78	
LPO - HF oscillator (f_{HFLPO})	Untrimmed frequency	5.5	9	19.5	MHz
	Trimmed frequency	8	9.6	11	MHz
	Start-up time from STANDBY (LPO BIAS_EN High for at least 900 µs)			10	µs
	Cold start-up time			900	µs
LPO - LF oscillator (f_{LFLPO})	Untrimmed frequency	36	85	180	kHz
	Start-up time from STANDBY (LPO BIAS_EN High for at least 900 µs)			100	µs
	Cold start-up time			2000	µs

6.5.1.3 Phase Locked Loop (PLL) Clock Modules

The PLL is used to multiply the input frequency to some higher frequency.

The main features of the PLL are:

- Frequency modulation can be optionally superimposed on the synthesized frequency of PLL.
- Configurable frequency multipliers and dividers.
- Built-in PLL Slip monitoring circuit.
- Option to reset the device on a PLL slip detection.

6.5.1.3.1 Block Diagram

図 6-6 shows a high-level block diagram of the PLL macro on this microcontroller.

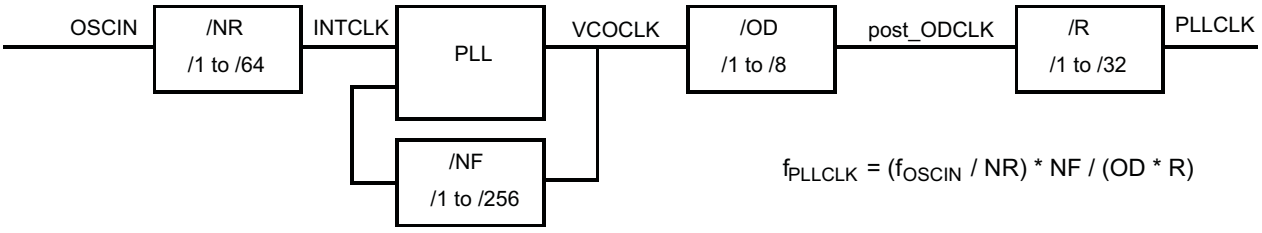

図 6-6. PLL Block Diagram

6.5.1.3.2 PLL Timing Specifications

表 6-11. PLL Timing Specifications

PARAMETER		MIN	MAX	UNIT
f_{INTCLK}	PLL1 Reference Clock frequency	1	20	MHz
f_{post_ODCLK}	Post-ODCLK – PLL1 Post-divider input clock frequency		400	MHz
f_{VCOCLK}	VCOCLK – PLL1 Output Divider (OD) input clock frequency	150	550	MHz

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6.5.2 Clock Domains

6.5.2.1 Clock Domain Descriptions

表 6-12 lists the device clock domains and their default clock sources. The table also shows the system module control register that is used to select an available clock source for each clock domain.

表 6-12. Clock Domain Descriptions

CLOCK DOMAIN NAME	DEFAULT CLOCK SOURCE	CLOCK SOURCE SELECTION REGISTER	DESCRIPTION
HCLK	OSCIN	GHVSRC	• Is disabled through the CDDISx registers bit 1
GCLK	OSCIN	GHVSRC	• Always the same frequency as HCLK • In phase with HCLK • Is disabled separately from HCLK through the CDDISx registers bit 0 • Can be divided by 1 up to 8 when running CPU self-test (LBIST) using the CLKDIV field of the STCCLKDIV register at address 0xFFFFE108
GCLK2	OSCIN	GHVSRC	• Always the same frequency as GCLK • 2 cycles delayed from GCLK • Is disabled along with GCLK • Gets divided by the same divider setting as that for GCLK when running CPU self-test (LBIST)
VCLK	OSCIN	GHVSRC	• Divided down from HCLK • Can be HCLK/1, HCLK/2, ... or HCLK/16 • Is disabled separately from HCLK through the CDDISx registers bit 2 • Can be disabled separately for eQEP using CDDISx registers bit 9
VCLK2	OSCIN	GHVSRC	• Divided down from HCLK • Can be HCLK/1, HCLK/2, ... or HCLK/16 • Frequency must be an integer multiple of VCLK frequency • Is disabled separately from HCLK through the CDDISx registers bit 3
VCLKA1	VCLK	VCLKASRC	• Defaults to VCLK as the source • Frequency can be as fast as HCLK frequency • Is disabled through the CDDISx registers bit 4
RTICLK	VCLK	RCLKSRC	• Defaults to VCLK as the source • If a clock source other than VCLK is selected for RTICLK, then the RTICLK frequency must be less than or equal to VCLK/3 – Application can ensure this by programming the RTI1DIV field of the RCLKSRC register, if necessary • Is disabled through the CDDISx registers bit 6

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6.5.2.2 Mapping of Clock Domains to Device Modules

Each clock domain has a dedicated functionality as shown in the figure below.

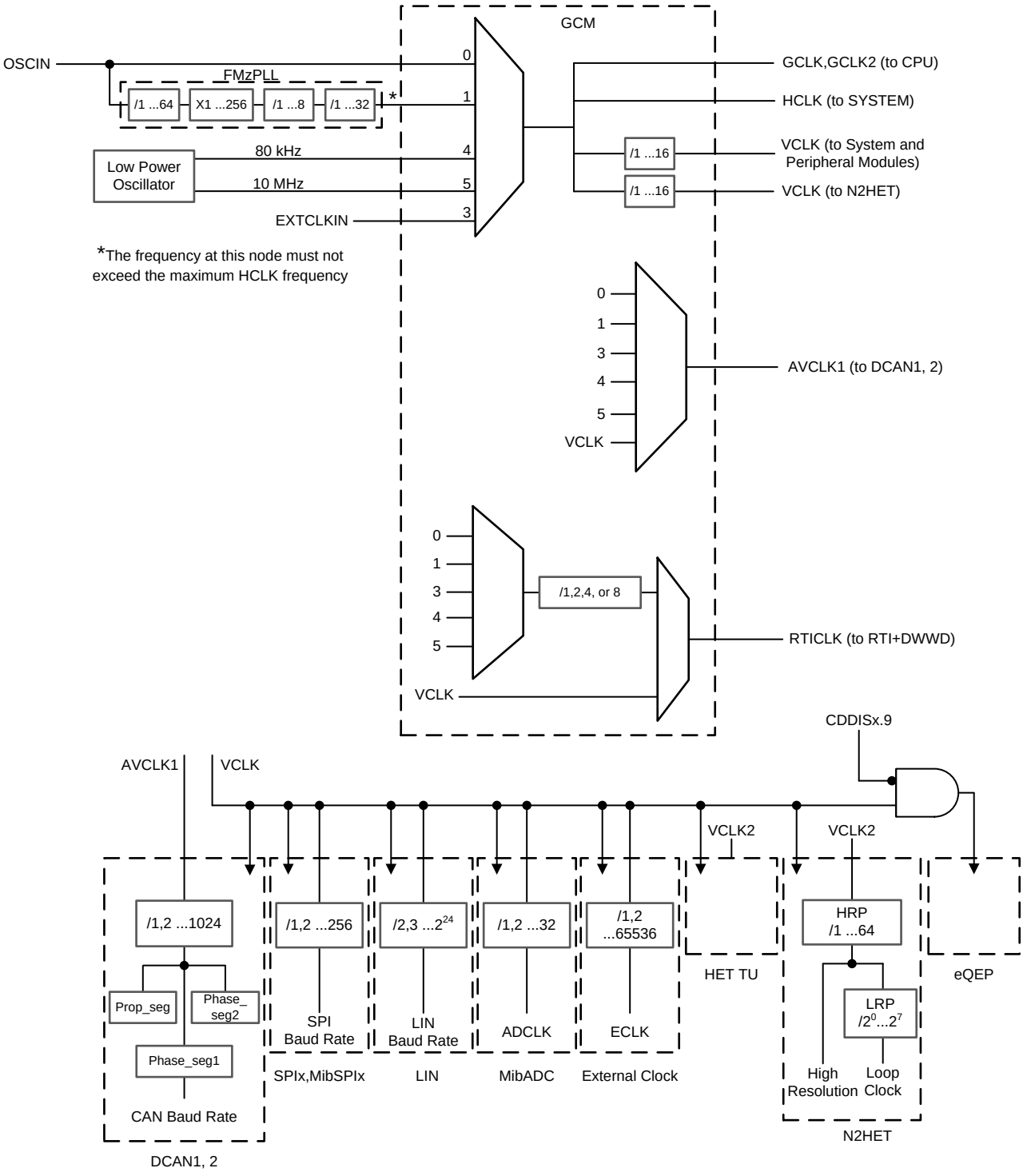

図 6-7. Device Clock Domains

6.5.3 Clock Test Mode

The TMS570 platform architecture defines a special mode that allows various clock signals to be brought out on to the ECLK pin and N2HET[2] device outputs. This mode is called the Clock Test mode. It is very useful for debugging purposes and can be configured through the CLKTEST register in the system module.

表 6-13. Clock Test Mode Options

CLKTEST[3-0]	SIGNAL ON ECLK		CLKTEST[11-8]	SIGNAL ON N2HET[2]
0000	Oscillator		0000	Oscillator Valid Status
0001	Main PLL free-running clock output (PLLCLK)		0001	Main PLL Valid status
0010	Reserved		0010	Reserved
0011	Reserved		0011	Reserved
0100	CLK80K		0100	Reserved
0101	CLK10M		0101	CLK10M Valid status
0110	Reserved		0110	Reserved
0111	Reserved		0111	Reserved
1000	GCLK		1000	CLK80K
1001	RTI Base		1001	Oscillator Valid status
1010	Reserved		1010	Oscillator Valid status
1011	VCLKA1		1011	Oscillator Valid status
1100	Reserved		1100	Oscillator Valid status
1101	Reserved		1101	Oscillator Valid status
1110	Reserved		1110	Oscillator Valid status
1111	Flash HD Pump Oscillator		1111	Oscillator Valid status

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6.6 Clock Monitoring

The LPO Clock Detect (LPOCLKDET) module consists of a clock monitor (CLKDET) and an internal low-power oscillator (LPO).

The LPO provides two different clock sources – a low frequency (LFLPO) and a high frequency (HFLPO).

The CLKDET is a supervisor circuit for an externally supplied clock signal (OSCIN). In case the OSCIN frequency falls out of a frequency window, the CLKDET flags this condition in the global status register (GLBSTAT bit 0: OSC FAIL) and switches all clock domains sourced by OSCIN to the HFLPO clock (limp mode clock).

The valid OSCIN frequency range is defined as: $f_{HFLPO} / 4 < f_{OSCIN} < f_{HFLPO} * 4$.

6.6.1 Clock Monitor Timings

For more information on LPO and Clock detection, refer to 表 6-10.

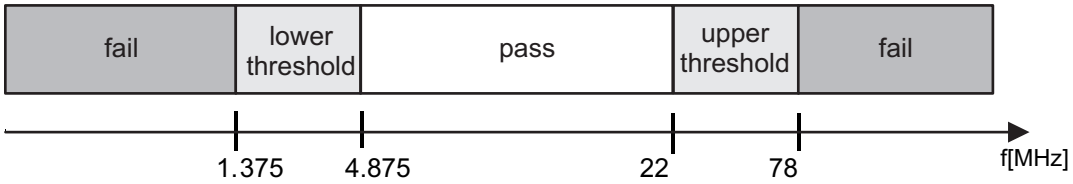

図 6-8. LPO and Clock Detection, Untrimmed HFLPO

6.6.2 External Clock (ECLK) Output Functionality

The ECLK pin can be configured to output a prescaled clock signal indicative of an internal device clock. This output can be externally monitored as a safety diagnostic.

6.6.3 Dual Clock Comparator

The Dual Clock Comparator (DCC) module determines the accuracy of selectable clock sources by counting the pulses of two independent clock sources (counter 0 and counter 1). If one clock is out of spec, an error signal is generated. For example, the DCC can be configured to use CLK10M as the reference clock (for counter 0) and VCLK as the "clock under test" (for counter 1). This configuration allows the DCC to monitor the PLL output clock when VCLK is using the PLL output as its source.

6.6.3.1 Features

- Takes two different clock sources as input to two independent counter blocks.
- One of the clock sources is the known-good, or reference clock; the second clock source is the "clock under test."
- Each counter block is programmable with initial, or seed values.
- The counter blocks start counting down from their seed values at the same time; a mismatch from the expected frequency for the clock under test generates an error signal which is used to interrupt the CPU.

6.6.3.2 Mapping of DCC Clock Source Inputs

表 6-14. DCC Counter 0 Clock Sources

TEST MODE	CLOCK SOURCE [3:0]	CLOCK NAME
0	Others	Oscillator (OSCIN)
	0x5	High-frequency LPO
	0xA	Test clock (TCK)
1	X	VCLK

表 6-15. DCC Counter 1 Clock Sources

TEST MODE	KEY [3:0]	CLOCK SOURCE [3:0]	CLOCK NAME
0	Others	–	N2HET[31]
	0xA	0x0	Main PLL free-running clock output
		0x1	n/a
		0x2	Low-frequency LPO
		0x3	High-frequency LPO
		0x4	Flash HD pump oscillator
		0x5	EXTCLKIN
		0x6	n/a
		0x7	Ring oscillator
		0x8 - 0xF	VCLK
1	X	X	HCLK

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6.7 Glitch Filters

A glitch filter is present on the following signals.

表 6-16. Glitch Filter Timing Specifications

PIN	PARAMETER		MIN	MAX	UNIT
nPORRST	$t_{f(nPORRST)}$	Filter time nPORRST pin; pulses less than MIN will be filtered out, pulses greater than MAX will generate a reset(1)	475	2000	ns
nRST	$t_{f(nRST)}$	Filter time nRST pin; pulses less than MIN will be filtered out, pulses greater than MAX will generate a reset	475	2000	ns
TEST	$t_{f(TEST)}$	Filter time TEST pin; pulses less than MIN will be filtered out, pulses greater than MAX will pass through	475	2000	ns

(1) The glitch filter design on the nPORRST signal is designed such that no size pulse will reset any part of the microcontroller (flash pump, I/O pins, and so forth) without also generating a valid reset signal to the CPU.

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6.8 Device Memory Map

6.8.1 Memory Map Diagram

図 6-9 shows the device memory map.

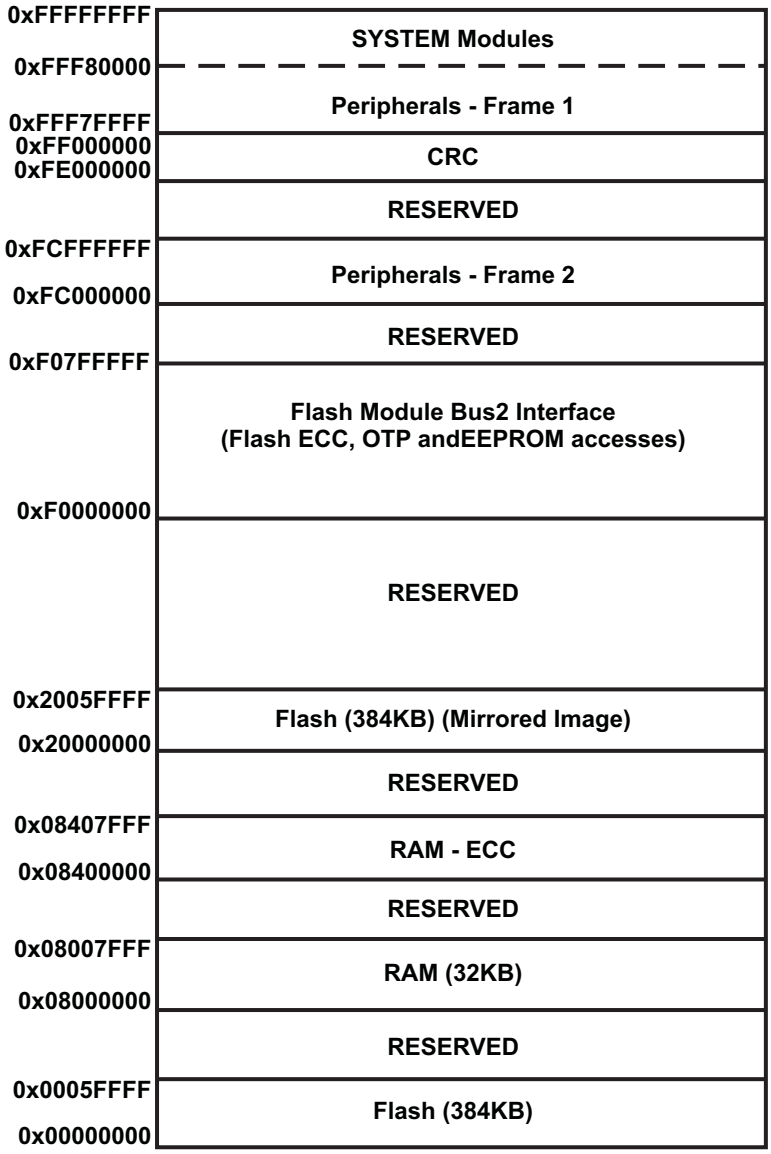

図 6-9. TMS570LS0432 Memory Map

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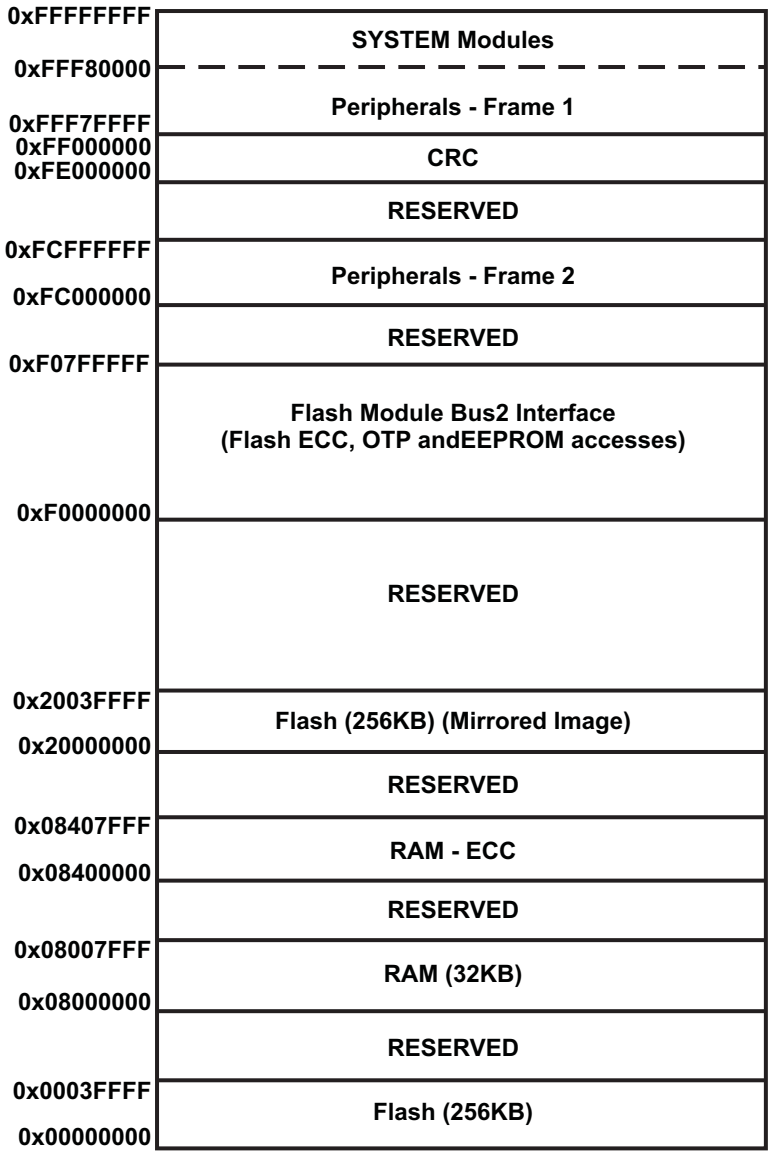

図 6-10. TMS570LS0332 Memory Map

The Flash memory in all configurations is mirrored to support ECC logic testing. The base address of the mirrored Flash image is 0x2000 0000.

6.8.2 Memory Map Table

See 図 1-1 for a block diagram showing the device interconnects.

表 6-17. Device Memory Map

MODULE NAME	FRAME CHIP SELECT	ADDRESS RANGE		FRAME SIZE	ACTUAL SIZE	RESPONSE FOR ACCESS TO UNIMPLEMENTED LOCATIONS IN FRAME
		START	END			
Memories tightly coupled to the ARM Cortex-R4 CPU						
TCM Flash	CS0	0x0000_0000	0x00FF_FFFF	16MB	384KB (1)	Abort
TCM RAM + RAM ECC	CSRAM0	0x0800_0000	0x0BFF_3FFF	64MB	32KB	
Mirrored Flash	Flash mirror frame	0x2000_0000	0x20FF_FFFF	16MB	384KB (1)	
Flash Module Bus2 Interface						
Customer OTP, TCM Flash Banks		0xF000_0000	0xF000_07FF	64KB	2KB	Abort
Customer OTP, EEPROM Bank		0xF000_E000	0xF000_E3FF		1KB	
Customer OTP–ECC, TCM Flash Banks		0xF004_0000	0xF004_00FF	8KB	256B	
Customer OTP–ECC, EEPROM Bank		0xF004_1C00	0xF004_1C7F		128B	
TI OTP, TCM Flash Banks		0xF008_0000	0xF008_07FF	64KB	2KB	
TI OTP, EEPROM Bank		0xF008_E000	0xF008_E3FF		1KB	
TI OTP–ECC, TCM Flash Banks		0xF00C_0000	0xF00C_00FF	8KB	256B	
TI OTP–ECC, EEPROM Bank		0xF00C_1C00	0xF00C_1C7F		128B	
EEPROM Bank–ECC		0xF010_0000	0xF010_07FF	256KB	2KB	
EEPROM Bank		0xF020_0000	0xF020_3FFF	2MB	16KB	
Flash Data Space ECC		0xF040_0000	0xF040_DFFF	1MB	48KB	
Cyclic Redundancy Checker (CRC) Module Registers						
CRC	CRC frame	0xFE00_0000	0xFEFF_FFFF	16MB	512B	Accesses above 0x200 generate abort.
Peripheral Memories						
MIBSPI1 RAM	PCS[7]	0xFF0E_0000	0xFF0F_FFFF	128KB	2KB	Abort for accesses above 2KB
DCAN2 RAM	PCS[14]	0xFF1C_0000	0xFF1D_FFFF	128KB	2KB	Wrap around for accesses to unimplemented address offsets lower than 0x7FF. Abort generated for accesses beyond offset 0x800.
DCAN1 RAM	PCS[15]	0xFF1E_0000	0xFF1F_FFFF	128KB	2KB	Wrap around for accesses to unimplemented address offsets lower than 0x7FF. Abort generated for accesses beyond offset 0x800.
MIBADC RAM	PCS[31]	0xFF3E_0000	0xFF3F_FFFF	128KB	8KB	Wrap around for accesses to unimplemented address offsets lower than 0x1FFF.
MIBADC Look-Up Table					384 bytes	Look-up table for ADC wrapper. Starts at offset 0x2000 ans ends at 0x217F. Wrap around for accesses between offsets 0x180 and 0x3FFF. Aborts generated for accesses beyond 0x4000

(1) The TMS570LS0332 device has only 256KB of flash.

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表 6-17. Device Memory Map (continued)

MODULE NAME	FRAME CHIP SELECT	ADDRESS RANGE		FRAME SIZE	ACTUAL SIZE	RESPONSE FOR ACCESS TO UNIMPLEMENTED LOCATIONS IN FRAME
		START	END			
N2HET RAM	PCS[35]	0xFF46_0000	0xFF47_FFFF	128KB	16KB	Wrap around for accesses to unimplemented address offsets lower than 0x3FFF. Abort generated for accesses beyond 0x3FFF.
HTU RAM	PCS[39]	0xFF4E_0000	0xFF4F_FFFF	128KB	1KB	Abort
Debug Components						
CoreSight Debug ROM	CSCS0	0xFFA0_0000	0xFFA0_0FFF	4KB	4KB	Reads return zeros, writes have no effect
Cortex-R4 Debug	CSCS1	0xFFA0_1000	0xFFA0_1FFF	4KB	4KB	Reads return zeros, writes have no effect
Peripheral Control Registers						
HTU	PS[22]	0xFFF7_A400	0xFFF7_A4FF	256B	256B	Reads return zeros, writes have no effect
N2HET	PS[17]	0xFFF7_B800	0xFFF7_B8FF	256B	256B	Reads return zeros, writes have no effect
GIO	PS[16]	0xFFF7_BC00	0xFFF7_BCFF	256B	256B	Reads return zeros, writes have no effect
MIBADC	PS[15]	0xFFF7_C000	0xFFF7_C1FF	512B	512B	Reads return zeros, writes have no effect
DCAN1	PS[8]	0xFFF7_DC00	0xFFF7_DDFF	512B	512B	Reads return zeros, writes have no effect
DCAN2	PS[8]	0xFFF7_DE00	0xFFF7_DFFF	512B	512B	Reads return zeros, writes have no effect
LIN	PS[6]	0xFFF7_E400	0xFFF7_E4FF	256B	256B	Reads return zeros, writes have no effect
MibSPI1	PS[2]	0xFFF7_F400	0xFFF7_F5FF	512B	512B	Reads return zeros, writes have no effect
SPI2	PS[2]	0xFFF7_F600	0xFFF7_F7FF	512B	512B	Reads return zeros, writes have no effect
SPI3	PS[1]	0xFFF7_F800	0xFFF7_F9FF	512B	512B	Reads return zeros, writes have no effect
EQEP	PS[25]	0xFFF7_9900	0xFFF7_99FF	256B	256B	Reads return zeros, writes have no effect
EQEP (Mirrored)	PS2[25]	0xFCF7_9900	0xFCF7_99FF	256B	256B	Reads return zeros, writes have no effect
System Modules Control Registers and Memories						
VIM RAM	PPCS2	0xFFF8_2000	0xFFF8_2FFF	4KB	1KB	Wrap around for accesses to unimplemented address offsets lower than 0x3FF. Accesses beyond 0x3FF will be ignored.
Flash Wrapper	PPCS7	0xFFF8_7000	0xFFF8_7FFF	4KB	4KB	Abort
eFuse Farm Controller	PPCS12	0xFFF8_C000	0xFFF8_CFFF	4KB	4KB	Abort
PCR registers	PPS0	0xFFFF_E000	0xFFFF_E0FF	256B	256B	Reads return zeros, writes have no effect
System Module - Frame 2 (see device TRM)	PPS0	0xFFFF_E100	0xFFFF_E1FF	256B	256B	Reads return zeros, writes have no effect
PBIST	PPS1	0xFFFF_E400	0xFFFF_E5FF	512B	512B	Reads return zeros, writes have no effect
STC	PPS1	0xFFFF_E600	0xFFFF_E6FF	256B	256B	Reads return zeros, writes have no effect
IOMM Multiplexing control module	PPS2	0xFFFF_EA00	0xFFFF_EBFF	512B	512B	Generates address error interrupt if enabled.

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表 6-17. Device Memory Map (continued)

MODULE NAME	FRAME CHIP SELECT	ADDRESS RANGE		FRAME SIZE	ACTUAL SIZE	RESPONSE FOR ACCESS TO UNIMPLEMENTED LOCATIONS IN FRAME
		START	END			
DCC	PPS3	0xFFFF_EC00	0xFFFF_ECFF	256B	256B	Reads return zeros, writes have no effect
ESM	PPS5	0xFFFF_F500	0xFFFF_F5FF	256B	256B	Reads return zeros, writes have no effect
CCMR4	PPS5	0xFFFF_F600	0xFFFF_F6FF	256B	256B	Reads return zeros, writes have no effect
RAM ECC even	PPS6	0xFFFF_F800	0xFFFF_F8FF	256B	256B	Reads return zeros, writes have no effect
RAM ECC odd	PPS6	0xFFFF_F900	0xFFFF_F9FF	256B	256B	Reads return zeros, writes have no effect
RTI + DWWD	PPS7	0xFFFF_FC00	0xFFFF_FCFF	256B	256B	Reads return zeros, writes have no effect
VIM Parity	PPS7	0xFFFF_FD00	0xFFFF_FDFF	256B	256B	Reads return zeros, writes have no effect
VIM	PPS7	0xFFFF_FE00	0xFFFF_FEFF	256B	256B	Reads return zeros, writes have no effect
System Module - Frame 1 (see device TRM)	PPS7	0xFFFF_FF00	0xFFFF_FFFF	256B	256B	Reads return zeros, writes have no effect

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6.8.3 Master/Slave Access Privileges

The table below lists the access permissions for each bus master on the device. A bus master is a module that can initiate a read or a write transaction on the device.

Each slave module on the main interconnect is listed in the table. A "Yes" indicates that the module listed in the "MASTERS" column can access that slave module.

表 6-18. Master / Slave Access Matrix

MASTERS	ACCESS MODE	SLAVES ON MAIN SCR			
		Flash Module Bus2 Interface: OTP, ECC, EEPROM Bank	Non-CPU Accesses to Program Flash and CPU Data RAM	CRC	Peripheral Control Registers, All Peripheral Memories, And All System Module Control Registers And Memories
CPU READ	User/Privilege	Yes	Yes	Yes	Yes
CPU WRITE	User/Privilege	No	Yes	Yes	Yes
HTU	Privilege	No	Yes	Yes	Yes

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6.9 Flash Memory

6.9.1 Flash Memory Configuration

Flash Bank: A separate block of logic consisting of 1 to 16 sectors. Each flash bank normally has a customer-OTP and a TI-OTP area. These flash sectors share input/output buffers, data paths, sense amplifiers, and control logic.

Flash Sector: A contiguous region of flash memory which must be erased simultaneously due to physical construction constraints.

Flash Pump: A charge pump which generates all the voltages required for reading, programming, or erasing the flash banks.

Flash Module: Interface circuitry required between the host CPU and the flash banks and pump module.

表 6-19. Flash Memory Banks and Sectors

MEMORY ARRAYS (or BANKS)	SECTOR NO.	SEGMENT	LOW ADDRESS	HIGH ADDRESS
BANK0 (384KB)(1)	0	8KB	0x0000_0000	0x0000_1FFF
	1	8KB	0x0000_2000	0x0000_3FFF
	2	8KB	0x0000_4000	0x0000_5FFF
	3	8KB	0x0000_6000	0x0000_7FFF
	4	8KB	0x0000_8000	0x0000_9FFF
	5	8KB	0x0000_A000	0x0000_BFFF
	6	8KB	0x0000_C000	0x0000_DFFF
	7	8KB	0x0000_E000	0x0000_FFFF
	8	8KB	0x0001_0000	0x0001_1FFF
	9	8KB	0x0001_2000	0x0001_3FFF
	10	8KB	0x0001_4000	0x0001_5FFF
	11	8KB	0x0001_6000	0x0001_7FFF
	12	32KB	0x0001_8000	0x0001_FFFF
	13	128KB	0x0002_0000	0x0003_FFFF
	14(2)	128KB	0x0004_0000	0x0005_FFFF
BANK7 (16KB) for EEPROM emulation(3)(4)	0	4KB	0xF020_0000	0xF020_0FFF
	1	4KB	0xF020_1000	0xF020_1FFF
	2	4KB	0xF020_2000	0xF020_2FFF
	3	4KB	0xF020_3000	0xF020_3FFF

(1) This Flash bank is 144-bit wide with ECC support.
(2) Sector 14 is not accessible or included in the TMS570LS0332 configuration.
(3) Flash bank7 is an FLEE bank and can be programmed while executing code from flash bank0. It is 72-bit wide with ECC support.
(4) Code execution is not allowed from flash bank7.

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6.9.2 Main Features of Flash Module

- Support for multiple flash banks for program and/or data storage
- Simultaneous read access on a bank while performing program or erase operation on any other bank
- Integrated state machines to automate flash erase and program operations
- Software interface for flash program and erase operations
- Pipelined mode operation to improve instruction access interface bandwidth
- Support for Single Error Correction Double Error Detection (SECDED) block inside Cortex-R4 CPU
  - Error address is captured for host system debugging
- Support for a rich set of diagnostic features

6.9.3 ECC Protection for Flash Accesses

All accesses to the program flash memory are protected by Single Error Correction Double Error Detection (SECDED) logic embedded inside the CPU. The flash module provides 8 bits of ECC code for 64 bits of instructions or data fetched from the flash memory. The CPU calculates the expected ECC code based on the 64 bits received and compares it with the ECC code returned by the flash module. A single-bit error is corrected and flagged by the CPU, while a multibit error is only flagged. The CPU signals an ECC error through its Event bus. This signaling mechanism is not enabled by default and must be enabled by setting the "X" bit of the Performance Monitor Control Register, c9.

```
MRC p15,#0,r1,c9,c12,#0    ;Enabling Event monitor states
ORR r1, r1, #0x00000010
MCR p15,#0,r1,c9,c12,#0    ;Set 4th bit (‘X’) of PMNC register
MRC p15,#0,r1,c9,c12,#0
```

The application must also explicitly enable the CPU's ECC checking for accesses on the CPU's ATCM and BTCM interfaces. These are connected to the program flash and data RAM respectively. ECC checking for these interfaces can be done by setting the B1TCMPCEN, B0TCMPCEN and ATCMPCEN bits of the System Control coprocessor's Auxiliary Control Register, c1.

```
MRC p15, #0, r1, c1, c0, #1
ORR r1, r1, #0x0e000000        ;Enable ECC checking for ATCM and BTCMs
DMB
MCR p15, #0, r1, c1, c0, #1
```

6.9.4 Flash Access Speeds

For information on flash memory access speeds and the relevant wait states required, see 5.6.

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6.10 Flash Program and Erase Timings for Program Flash

表 6-20. Timing Specifications for Program Flash

PARAMETER			MIN	NOM	MAX	UNIT
t_{prog} (144bit)	Wide Word (144 bit) programming time			40	300	µs
t_{prog} (Total)	384KByte programming time(1)	-40°C to 125°C			4	s
		0°C to 60°C, for first 25 cycles		1	2	
t_{erase}	Sector/Bank erase time(2)	-40°C to 125°C		0.30	4	s
		0°C to 60°C, for first 25 cycles		16	100	ms
t_{wec}	Write/erase cycles with 15 year Data Retention requirement	-40°C to 125°C			1000	cycles

(1) This programming time includes overhead of state machine, but does not include data transfer time. The programming time assumes programming 144 bits at a time at the maximum specified operating frequency.
(2) During bank erase, the selected sectors are erased simultaneously. The time to erase the bank is specified as equal to the time to erase a sector.

6.11 Flash Program and Erase Timings for Data Flash

表 6-21. Timing Specifications for Data Flash

PARAMETER			MIN	NOM	MAX	UNIT
t_{prog} (72 bit)	Wide Word (72 bit) programming time			47	300	µs
t_{prog} (Total)	16KB programming time(1)	–40°C to 125°C			330	ms
		0°C to 60°C, for first 25 cycles		100	165	
t_{erase}	Sector/Bank erase time(2)	–40°C to 125°C		0.200	8	s
		0°C to 60°C, for first 25 cycles		14	100	ms
t_{wec}	Write/erase cycles with 15 year Data Retention requirement	–40°C to 125°C			100000	cycles

(1) This programming time includes overhead of state machine, but does not include data transfer time. The programming time assumes programming 72 bits at a time at the maximum specified operating frequency.
(2) During bank erase, the selected sectors are erased simultaneously. The time to erase the bank is specified as equal to the time to erase a sector.

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6.12 Tightly Coupled RAM Interface Module

図 6-11 illustrates the connection of the Tightly Coupled RAM (TCRAM) to the Cortex-R4 CPU.

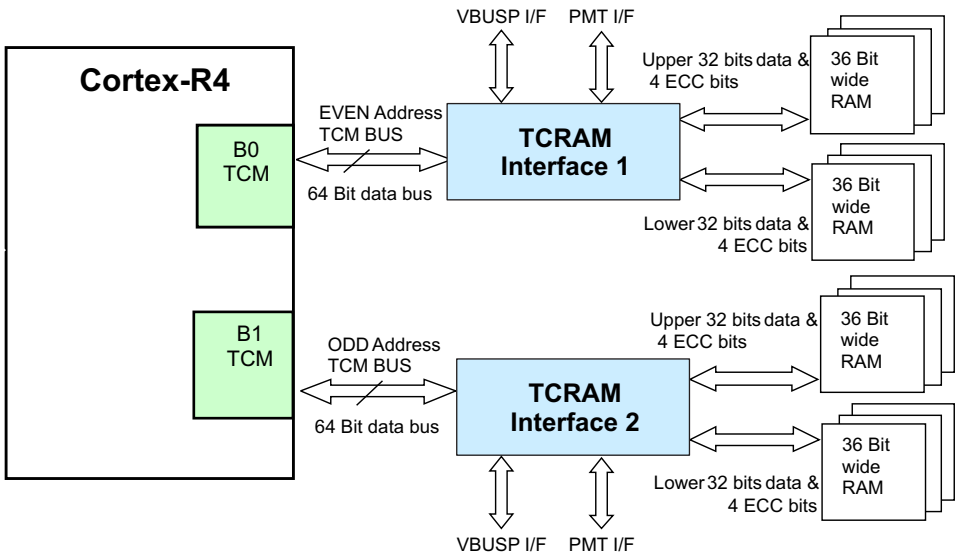

図 6-11. TCRAM Block Diagram

6.12.1 Features

The features of the Tightly Coupled RAM (TCRAM) module are:

- Acts as slave to the BTCM interface of the Cortex-R4 CPU
- Supports CPU's internal ECC scheme by providing 64-bit data and 8-bit ECC code
- Monitors CPU Event Bus and generates single-bit or multibit error interrupts
- Stores addresses for single-bit and multibit errors
- Provides CPU address bus integrity checking by supporting parity checking on the address bus
- Performs redundant address decoding for the RAM bank chip select and ECC select generation logic
- Provides enhanced safety for the RAM addressing by implementing two 36-bit wide byte-interleaved RAM banks and generating independent RAM access control signals to the two banks
- Supports auto-initialization of the RAM banks along with the ECC bits
- No support for bit-wise RAM accesses

6.12.2 TCRAMW ECC Support

The TCRAMW passes on the ECC code for each data read by the Cortex-R4 CPU from the RAM. It also stores the CPU's ECC port contents in the ECC RAM when the CPU does a write to the RAM. The TCRAMW monitors the CPU's event bus and provides registers for indicating single-bit and multibit errors and also for identifying the address that caused the single-bit or multibit error. The event signaling and the ECC checking for the RAM accesses must be enabled inside the CPU.

For more information see the device Technical Reference Manual.

6.13 Parity Protection for Accesses to peripheral RAMs

Accesses to some peripheral RAMs are protected by odd/even parity checking. During a read access the parity is calculated based on the data read from the peripheral RAM and compared with the good parity value stored in the parity RAM for that peripheral. If any word fails the parity check, the module generates a parity error signal that is mapped to the Error Signaling Module. The module also captures the peripheral RAM address that caused the parity error.

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The parity protection for peripheral RAMs is not enabled by default and must be enabled by the application. Each individual peripheral contains control registers to enable the parity protection for accesses to its RAM.

注

The CPU read access gets the actual data from the peripheral. The application can choose to generate an interrupt whenever a peripheral RAM parity error is detected.

6.14 On-Chip SRAM Initialization and Testing

6.14.1 On-Chip SRAM Self-Test Using PBIST

6.14.1.1 Features

- Extensive instruction set to support various memory test algorithms
- ROM-based algorithms allow the application to run TI production-level memory tests
- Independent testing of all on-chip SRAM

6.14.1.2 PBIST RAM Groups

表 6-22. PBIST RAM Grouping

MEMORY	RAM GROUP	TEST CLOCK	MEM TYPE	TEST PATTERN (ALGORITHM)			
				TRIPLE READ SLOW READ	TRIPLE READ FAST READ	MARCH 13N(1) TWO PORT (CYCLES)	MARCH 13N(1) SINGLE PORT (CYCLES)
				ALGO MASK 0x1	ALGO MASK 0x2	ALGO MASK 0x4	ALGO MASK 0x8
PBIST_ROM	1	ROM CLK	ROM	X	X		
STC_ROM	2	ROM CLK	ROM	X	X		
DCAN1	3	VCLK	Dual Port			12720	
DCAN2	4	VCLK	Dual Port			6480	
RAM	6	HCLK	Single Port				133160
MIBSPI1	7	VCLK	Dual Port			33440	
VIM	10	VCLK	Dual Port			12560	
MIBADC	11	VCLK	Dual Port			4200	
N2HET1	13	VCLK	Dual Port			25440	
HTU1	14	VCLK	Dual Port			6480	

(1) There are several memory testing algorithms stored in the PBIST ROM. However, TI recommends the March13N algorithm for application testing.

The PBIST ROM clock can be divided down from HCLK. The divider is selected by programming the ROM_DIV field of the Memory Self-Test Global Control Register (MSTGCR) at address 0xFFFFFF58.

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6.14.2 On-Chip SRAM Auto Initialization

This microcontroller allows some of the on-chip memories to be initialized through the Memory Hardware Initialization mechanism in the System module. This hardware mechanism allows an application to program the memory arrays with error detection capability to a known state based on their error detection scheme (odd/even parity or ECC).

The MINITGCR register enables the memory initialization sequence, and the MSINENA register selects the memories that are to be initialized.

For more information on these registers refer to the device Technical Reference Manual.

The mapping of the different on-chip memories to the specific bits of the MSINENA registers is shown in 表 6-23.

表 6-23. Memory Initialization

CONNECTING MODULE	ADDRESS RANGE		MSINENA REGISTER BIT NO.(1)
	BASE ADDRESS	ENDING ADDRESS	
RAM	0x08000000	0x08007FFF	0
MIBSPI1 RAM	0xFF0E0000	0xFF0FFFFF	7(2)
DCAN2 RAM	0xFF1C0000	0xFF1DFFFF	6
DCAN1 RAM	0xFF1E0000	0xFF1FFFFF	5
MIBADC RAM	0xFF3E0000	0xFF3FFFFF	8
N2HET RAM	0xFF460000	0xFF47FFFF	3
HTU RAM	0xFF4E0000	0xFF4FFFFF	4
VIM RAM	0xFFF82000	0xFFF82FFF	2

(1) Unassigned register bits are reserved.
(2) The MibSPI1 module performs an initialization of the transmit and receive RAMs as soon as the module is brought out of reset using the SPI Global Control Register 0 (SPIGCR0). This is independent of whether the application chooses to initialize the MibSPI1 RAMs using the system module auto-initialization method.

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6.15 Vectored Interrupt Manager

The vectored interrupt manager (VIM) provides hardware assistance for prioritizing and controlling the many interrupt sources present on this device. Interrupts are caused by events outside of the normal flow of program execution. Normally, these events require a timely response from the central processing unit (CPU); therefore, when an interrupt occurs, the CPU switches execution from the normal program flow to an interrupt service routine (ISR).

6.15.1 VIM Features

The VIM module has the following features:

- Supports 96 interrupt channels.
  - Provides programmable priority and enable for interrupt request lines.
- Provides a direct hardware dispatch mechanism for fastest IRQ dispatch.
- Provides two software dispatch mechanisms when the CPU VIC port is not used.
  - Index interrupt
  - Register vectored interrupt
- Parity protected vector interrupt table against soft errors.

6.15.2 Interrupt Request Assignments

表 6-24. Interrupt Request Assignments

MODULES	INTERRUPT SOURCES	DEFAULT VIM INTERRUPT CHANNEL
ESM	ESM High level interrupt (NMI)	0
Reserved	Reserved	1
RTI	RTI compare interrupt 0	2
RTI	RTI compare interrupt 1	3
RTI	RTI compare interrupt 2	4
RTI	RTI compare interrupt 3	5
RTI	RTI overflow interrupt 0	6
RTI	RTI overflow interrupt 1	7
Reserved	Reserved	8
GIO	GIO interrupt A	9
N2HET	N2HET level 0 interrupt	10
HTU	HTU level 0 interrupt	11
MIBSPI1	MIBSPI1 level 0 interrupt	12
LIN	LIN level 0 interrupt	13
MIBADC	MIBADC event group interrupt	14
MIBADC	MIBADC sw group 1 interrupt	15
DCAN1	DCAN1 level 0 interrupt	16
SPI2	SPI2 level 0 interrupt	17
Reserved	Reserved	18
Reserved	Reserved	19
ESM	ESM Low level interrupt	20
SYSTEM	Software interrupt (SSI)	21
CPU	PMU interrupt	22
GIO	GIO interrupt B	23
N2HET	N2HET level 1 interrupt	24
HTU	HTU level 1 interrupt	25

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表 6-24. Interrupt Request Assignments (continued)

MODULES	INTERRUPT SOURCES	DEFAULT VIM INTERRUPT CHANNEL
MIBSPI1	MIBSPI1 level 1 interrupt	26
LIN	LIN level 1 interrupt	27
MIBADC	MIBADC sw group 2 interrupt	28
DCAN1	DCAN1 level 1 interrupt	29
SPI2	SPI2 level 1 interrupt	30
MIBADC	MIBADC magnitude compare interrupt	31
Reserved	Reserved	32-34
DCAN2	DCAN2 level 0 interrupt	35
Reserved	Reserved	36
SPI3	SPI3 level 0 interrupt	37
SPI3	SPI3 level 1 interrupt	38
Reserved	Reserved	39-41
DCAN2	DCAN2 level 1 interrupt	42
Reserved	Reserved	43-60
FMC	FSM_DONE interrupt	61
Reserved	Reserved	62-79
HWAG	HWA_INT_REQ_H	80
Reserved	Reserved	81
DCC	DCC done interrupt	82
Reserved	Reserved	83
eQEPINTn	eQEP Interrupt	84
PBIST	PBIST Done Interrupt	85
Reserved	Reserved	86-87
HWAG	HWA_INT_REQ_L	88
Reserved	Reserved	89-95

注

Address location 0x00000000 in the VIM RAM is reserved for the phantom interrupt ISR entry; therefore only request channels 0..94 can be used and are offset by 1 address in the VIM RAM.

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6.16 Real-Time Interrupt Module

The real-time interrupt (RTI) module provides timer functionality for operating systems and for benchmarking code. The RTI module can incorporate several counters that define the timebases needed for scheduling an operating system.

The timers also allow you to benchmark certain areas of code by reading the values of the counters at the beginning and the end of the desired code range and calculating the difference between the values.

6.16.1 Features

The RTI module has the following features:

- Two independent 64 bit counter blocks
- Four configurable compares for generating operating system ticks. Each event can be driven by either counter block 0 or counter block 1.
- Fast enabling/disabling of events
- Two time-stamp (capture) functions for system or peripheral interrupts, one for each counter block

6.16.2 Block Diagrams

図 6-12 shows a high-level block diagram for one of the two 64-bit counter blocks inside the RTI module. Both the counter blocks are identical.

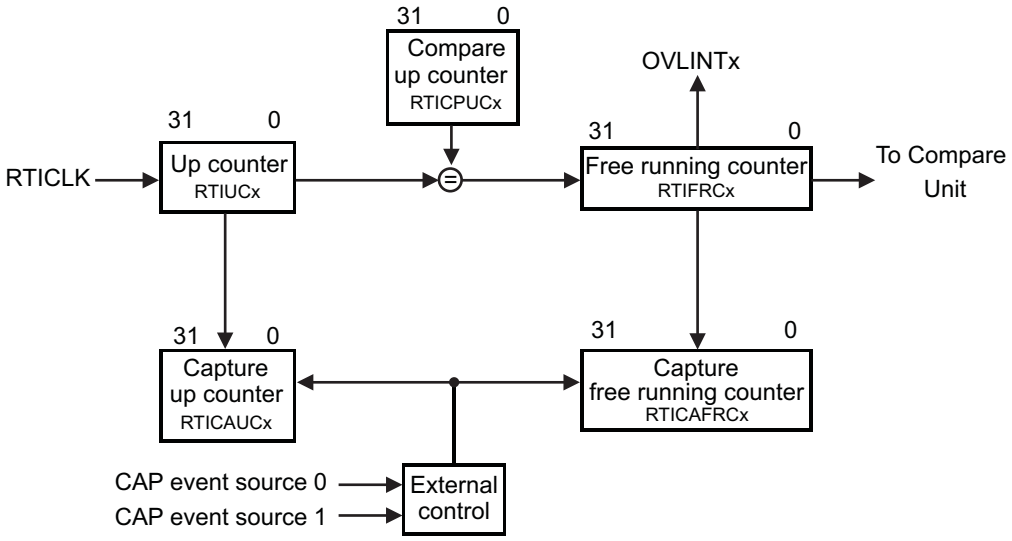

図 6-12. Counter Block Diagram

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Figure 6-13 shows a typical high-level block diagram for one of the four compares inside the RTI module. Each of the four compares are identical.

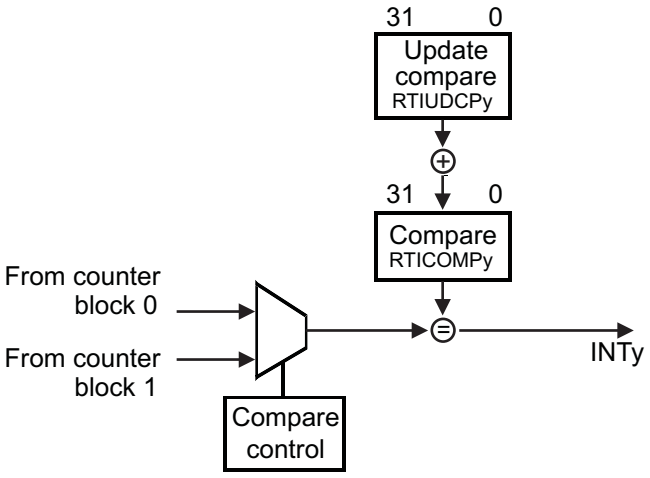

Figure 6-13. Compare Block Diagram

6.16.3 Clock Source Options

The RTI module uses the RTICLK clock domain for generating the RTI time bases.

The application can select the clock source for the RTICLK by configuring the RCLKSRC register in the System module at address 0xFFFFFF50. The default source for RTICLK is VCLK.

For more information, on the clock sources see 表 6-8 and 表 6-12.

6.17 Error Signaling Module

The Error Signaling Module (ESM) manages the various error conditions on the TMS570 microcontroller. The error condition is handled based on a fixed severity level assigned to it. Any severe error condition can be configured to drive a low level on a dedicated device terminal called nERROR. This can be used as an indicator to an external monitor circuit to put the system into a safe state.

6.17.1 Features

The features of the Error Signaling Module are:

- 128 interrupt/error channels are supported, divided into 3 different groups
  - 64 channels with maskable interrupt and configurable error pin behavior
  - 32 error channels with nonmaskable interrupt and predefined error pin behavior
  - 32 channels with predefined error pin behavior only
- Error pin to signal severe device failure
- Configurable timebase for error signal
- Error forcing capability

6.17.2 ESM Channel Assignments

The Error Signaling Module (ESM) integrates all the device error conditions and groups them in the order of severity. Group1 is used for errors of the lowest severity while Group3 is used for errors of the highest severity. The device response to each error is determined by the severity group it is connected to. 表 6-26 shows the channel assignment for each group.

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表 6-25. ESM Groups

ERROR GROUP	INTERRUPT CHARACTERISTICS	INFLUENCE ON ERROR PIN
Group1	Maskable, low or high priority	Configurable
Group2	Nonmaskable, high priority	Fixed
Group3	No interrupt generated	Fixed

表 6-26. ESM Channel Assignments

ERROR SOURCES	GROUP	CHANNELS
Reserved	Group1	0
Reserved	Group1	1
Reserved	Group1	2
Reserved	Group1	3
Reserved	Group1	4
Reserved	Group1	5
FMC - correctable error: bus1 and bus2 interfaces (does not include accesses to EEPROM bank)	Group1	6
N2HET - parity	Group1	7
HTU - parity	Group1	8
HTU - MPU	Group1	9
PLL - Slip	Group1	10
Clock Monitor - interrupt	Group1	11
Reserved	Group1	12
Reserved	Group1	13
Reserved	Group1	14
VIM RAM - parity	Group1	15
Reserved	Group1	16
MibSPI1 - parity	Group1	17
Reserved	Group1	18
MibADC - parity	Group1	19
Reserved	Group1	20
DCAN1 - parity	Group1	21
Reserved	Group1	22
DCAN2 - parity	Group1	23
Reserved	Group1	24
Reserved	Group1	25
RAM even bank (B0TCM) - correctable error	Group1	26
CPU - self-test	Group1	27
RAM odd bank (B1TCM) - correctable error	Group1	28
Reserved	Group1	29
DCC - error	Group1	30
CCM-R4 - self-test	Group1	31
Reserved	Group1	32
Reserved	Group1	33
Reserved	Group1	34
FMC - correctable error (EEPROM bank access)	Group1	35
FMC - uncorrectable error (EEPROM bank access)	Group1	36
IOMM - Mux configuration error	Group1	37
Reserved	Group1	38

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表 6-26. ESM Channel Assignments (continued)

ERROR SOURCES	GROUP	CHANNELS
Reserved	Group1	39
eFuse farm – this error signal is generated whenever any bit in the eFuse farm error status register is set. The application can choose to generate and interrupt whenever this bit is set in order to service any eFuse farm error condition.	Group1	40
eFuse farm - self test error. It is not necessary to generate a separate interrupt when this bit gets set.	Group1	41
Reserved	Group1	42
Reserved	Group1	43
Reserved	Group1	44
Reserved	Group1	45
Reserved	Group1	46
Reserved	Group1	47
Reserved	Group1	48
Reserved	Group1	49
Reserved	Group1	50
Reserved	Group1	51
Reserved	Group1	52
Reserved	Group1	53
Reserved	Group1	54
Reserved	Group1	55
Reserved	Group1	56
Reserved	Group1	57
Reserved	Group1	58
Reserved	Group1	59
Reserved	Group1	60
Reserved	Group1	61
Reserved	Group1	62
Reserved	Group1	63
Reserved	Group2	0
Reserved	Group2	1
CCMR4 - compare	Group2	2
Reserved	Group2	3
FMC - uncorrectable error (address parity on bus1 accesses)	Group2	4
Reserved	Group2	5
RAM even bank (B0TCM) - uncorrectable error	Group2	6
Reserved	Group2	7
RAM odd bank (B1TCM) - uncorrectable error	Group2	8
Reserved	Group2	9
RAM even bank (B0TCM) - address bus parity error	Group2	10
Reserved	Group2	11
RAM odd bank (B1TCM) - address bus parity error	Group2	12
Reserved	Group2	13
Reserved	Group2	14
Reserved	Group2	15
TCM - ECC live lock detect	Group2	16
Reserved	Group2	17
Reserved	Group2	18
Reserved	Group2	19

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表 6-26. ESM Channel Assignments (continued)

ERROR SOURCES	GROUP	CHANNELS
Reserved	Group2	20
Reserved	Group2	21
Reserved	Group2	22
Reserved	Group2	23
RTI_WWD_NMI	Group2	24
Reserved	Group2	25
Reserved	Group2	26
Reserved	Group2	27
Reserved	Group2	28
Reserved	Group2	29
Reserved	Group2	30
Reserved	Group2	31
Reserved	Group3	0
eFuse Farm - autoload error	Group3	1
Reserved	Group3	2
RAM even bank (B0TCM) - ECC uncorrectable error	Group3	3
Reserved	Group3	4
RAM odd bank (B1TCM) - ECC uncorrectable error	Group3	5
Reserved	Group3	6
FMC - uncorrectable error: bus1 and bus2 interfaces (does not include address parity error and errors on accesses to EEPROM bank)	Group3	7
Reserved	Group3	8
Reserved	Group3	9
Reserved	Group3	10
Reserved	Group3	11
Reserved	Group3	12
Reserved	Group3	13
Reserved	Group3	14
Reserved	Group3	15
Reserved	Group3	16
Reserved	Group3	17
Reserved	Group3	18
Reserved	Group3	19
Reserved	Group3	20
Reserved	Group3	21
Reserved	Group3	22
Reserved	Group3	23
Reserved	Group3	24
Reserved	Group3	25
Reserved	Group3	26
Reserved	Group3	27
Reserved	Group3	28
Reserved	Group3	29
Reserved	Group3	30
Reserved	Group3	31

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6.18 Reset / Abort / Error Sources

表 6-27. Reset/Abort/Error Sources

ERROR SOURCE	SYSTEM MODE	ERROR RESPONSE	ESM HOOKUP GROUP.CHANNEL
CPU TRANSACTIONS			
Precise write error (NCNB/Strongly Ordered)	User/Privilege	Precise Abort (CPU)	n/a
Precise read error (NCB/Device or Normal)	User/Privilege	Precise Abort (CPU)	n/a
Imprecise write error (NCB/Device or Normal)	User/Privilege	Imprecise Abort (CPU)	n/a
Illegal instruction	User/Privilege	Undefined Instruction Trap (CPU)(1)	n/a
MPU access violation	User/Privilege	Abort (CPU)	n/a
SRAM			
B0 TCM (even) ECC single error (correctable)	User/Privilege	ESM	1.26
B0 TCM (even) ECC double error (noncorrectable)	User/Privilege	Abort (CPU), ESM → nERROR	3.3
B0 TCM (even) uncorrectable error (that is, redundant address decode)	User/Privilege	ESM → NMI → nERROR	2.6
B0 TCM (even) address bus parity error	User/Privilege	ESM → NMI → nERROR	2.10
B1 TCM (odd) ECC single error (correctable)	User/Privilege	ESM	1.28
B1 TCM (odd) ECC double error (noncorrectable)	User/Privilege	Abort (CPU), ESM → nERROR	3.5
B1 TCM (odd) uncorrectable error (that is, redundant address decode)	User/Privilege	ESM → NMI → nERROR	2.8
B1 TCM (odd) address bus parity error	User/Privilege	ESM → NMI → nERROR	2.12
FLASH WITH CPU BASED ECC			
FMC correctable error - Bus1 and Bus2 interfaces (does not include accesses to EEPROM bank)	User/Privilege	ESM	1.6
FMC uncorrectable error - Bus1 accesses (does not include address parity error)	User/Privilege	Abort (CPU), ESM → nERROR	3.7
FMC uncorrectable error - Bus2 accesses (does not include address parity error and EEPROM bank accesses)	User/Privilege	ESM → nERROR	3.7
FMC uncorrectable error - address parity error on Bus1 accesses	User/Privilege	ESM → NMI → nERROR	2.4
FMC correctable error - Accesses to EEPROM bank	User/Privilege	ESM	1.35
FMC uncorrectable error - Accesses to EEPROM bank	User/Privilege	ESM	1.36
HIGH-END TIMER TRANSFER UNIT (HTU)			
NCNB (Strongly Ordered) transaction with slave error response	User/Privilege	Interrupt → VIM	n/a
External imprecise error (Illegal transaction with ok response)	User/Privilege	Interrupt → VIM	n/a
Memory access permission violation	User/Privilege	ESM	1.9
Memory parity error	User/Privilege	ESM	1.8
N2HET			
Memory parity error	User/Privilege	ESM	1.7
MIBSPI			
MibSPI1 memory parity error	User/Privilege	ESM	1.17
MIBADC			
MibADC Memory parity error	User/Privilege	ESM	1.19
DCAN			
DCAN1 memory parity error	User/Privilege	ESM	1.21

(1) The Undefined Instruction TRAP is NOT detectable outside the CPU. The trap is taken only if the instruction reaches the execute stage of the CPU.

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表 6-27. Reset/Abort/Error Sources (continued)

ERROR SOURCE	SYSTEM MODE	ERROR RESPONSE	ESM HOOKUP GROUP.CHANNEL
DCAN2 memory parity error	User/Privilege	ESM	1.23
PLL			
PLL slip error	User/Privilege	ESM	1.10
CLOCK MONITOR			
Clock monitor interrupt	User/Privilege	ESM	1.11
DCC			
DCC error	User/Privilege	ESM	1.30
CCM-R4			
Self test failure	User/Privilege	ESM	1.31
Compare failure	User/Privilege	ESM → NMI → nERROR	2.2
VIM			
Memory parity error	User/Privilege	ESM	1.15
VOLTAGE MONITOR			
VMON out of voltage range	n/a	Reset	n/a
CPU SELF-TEST (LBIST)			
CPU Self-test (LBIST) error	User/Privilege	ESM	1.27
PIN MULTIPLEXING CONTROL			
Mux configuration error	User/Privilege	ESM	1.37
eFuse CONTROLLER			
eFuse Controller Autoload error	User/Privilege	ESM → nERROR	3.1
eFuse Controller - Any bit set in the error status register	User/Privilege	ESM	1.40
eFuse Controller self-test error	User/Privilege	ESM	1.41
WINDOWED WATCHDOG			
WWD Nonmaskable Interrupt exception	n/a	ESM => NMI => nERROR	2.24
ERRORS REFLECTED IN THE SYSESR REGISTER			
Power-Up Reset	n/a	Reset	n/a
Oscillator fail / PLL slip(2)	n/a	Reset	n/a
Watchdog exception	n/a	Reset	n/a
CPU Reset (driven by the CPU STC)	n/a	Reset	n/a
Software Reset	n/a	Reset	n/a
External Reset	n/a	Reset	n/a

(2) Oscillator fail/PLL slip can be configured in the system register (SYS.PLLCTL1) to generate a reset.

6.19 Digital Windowed Watchdog

This device includes a digital windowed watchdog (DWWD) module that protects against runaway code execution.

The DWWD module allows the application to configure the time window within which the DWWD module expects the application to service the watchdog. A watchdog violation occurs if the application services the watchdog outside of this window, or fails to service the watchdog at all. The application can choose to generate a system reset or a nonmaskable interrupt to the CPU in case of a watchdog violation.

The watchdog is disabled by default and must be enabled by the application. Once enabled, the watchdog can only be disabled upon a system reset.

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6.20 Debug Subsystem

6.20.1 Block Diagram

The device contains an ICEPICK module to allow JTAG access to the scan chains (see 図 6-14).

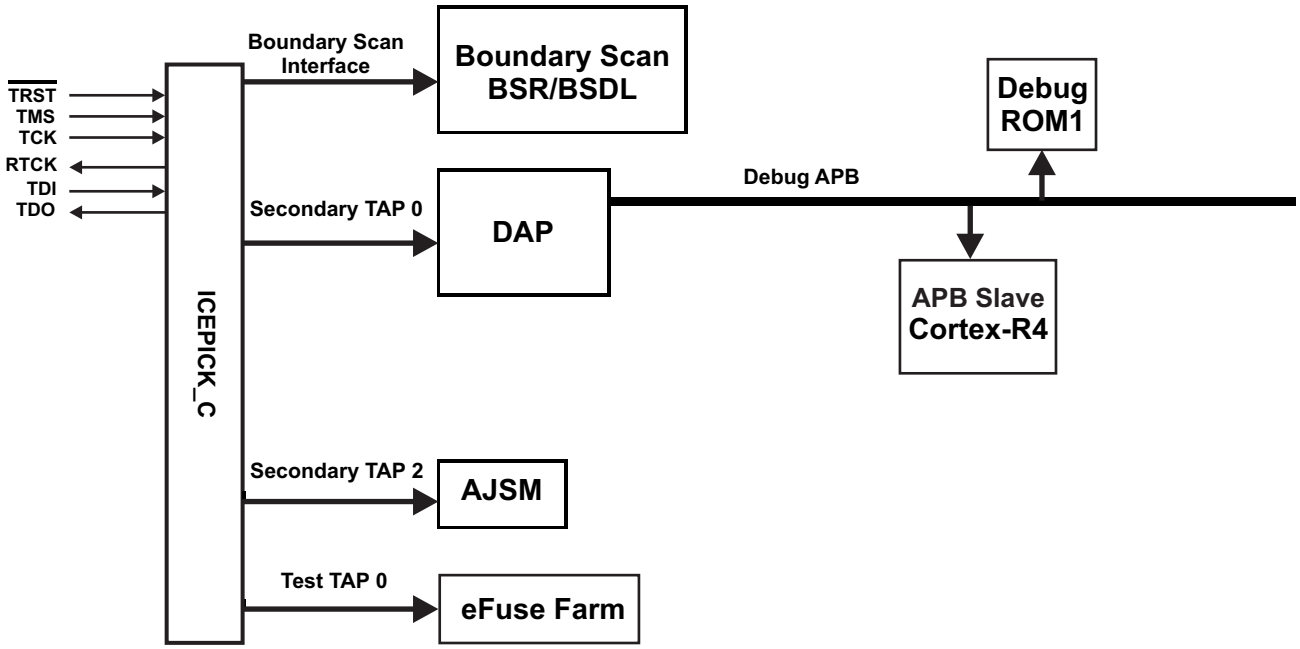

図 6-14. Debug Subsystem Block Diagram

6.20.2 Debug Components Memory Map

表 6-28. Debug Components Memory Map

MODULE NAME	FRAME CHIP SELECT	FRAME ADDRESS RANGE		FRAME SIZE	ACTUAL SIZE	RESPONSE FOR ACCESS TO UNIMPLEMENTED LOCATIONS IN FRAME
		START	END			
CoreSight Debug ROM	CSCS0	0xFFA0_0000	0xFFA0_0FFF	4KB	4KB	Reads return zeros, writes have no effect
Cortex-R4 Debug	CSCS1	0xFFA0_1000	0xFFA0_1FFF	4KB	4KB	Reads return zeros, writes have no effect

6.20.3 JTAG Identification Code

The JTAG ID code for this device is the same as the device ICEPick Identification Code.

表 6-29. JTAG Identification Code

SILICON REVISION	IDENTIFICATION CODE
Initial Silicon	0x0B97102F
Revision A	0x1B97102F
Revision B	0x2B97102F

6.20.4 Debug ROM

The Debug ROM stores the location of the components on the Debug APB bus:

表 6-30. Debug ROM table

ADDRESS	DESCRIPTION	VALUE
0x000	Pointer to Cortex-R4	0x0000 1003
0x001	Reserved	0x0000 2002
0x002	Reserved	0x0000 3002
0x003	Reserved	0x0000 4002
0x004	End of table	0x0000 0000

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6.20.5 JTAG Scan Interface Timings

表 6-31. JTAG Scan Interface Timing(1)

NO.	PARAMETER		MIN	MAX	UNIT
	f_{TCK}	TCK frequency (at HCLKmax)		12	MHz
	f_{RTCK}	RTCK frequency (at TCKmax and HCLKmax)	10		MHz
1	$t_{d(TCK\ -RTCK)}$	Delay time, TCK to RTCK		24	ns
2	$t_{su(TDI/TMS\ -\ RTCKr)}$	Setup time, TDI, TMS before RTCK rise (RTCKr)	26		ns
3	$t_{h(RTCKr\ -TDI/TMS)}$	Hold time, TDI, TMS after RTCKr	0		ns
4	$t_{h(RTCKr\ -TDO)}$	Hold time, TDO after RTCKf	0		ns
5	$t_{d(TCKf\ -TDO)}$	Delay time, TDO valid after RTCK fall (RTCKf)		12	ns

(1) Timings for TDO are specified for a maximum of 50 pF load on TDO

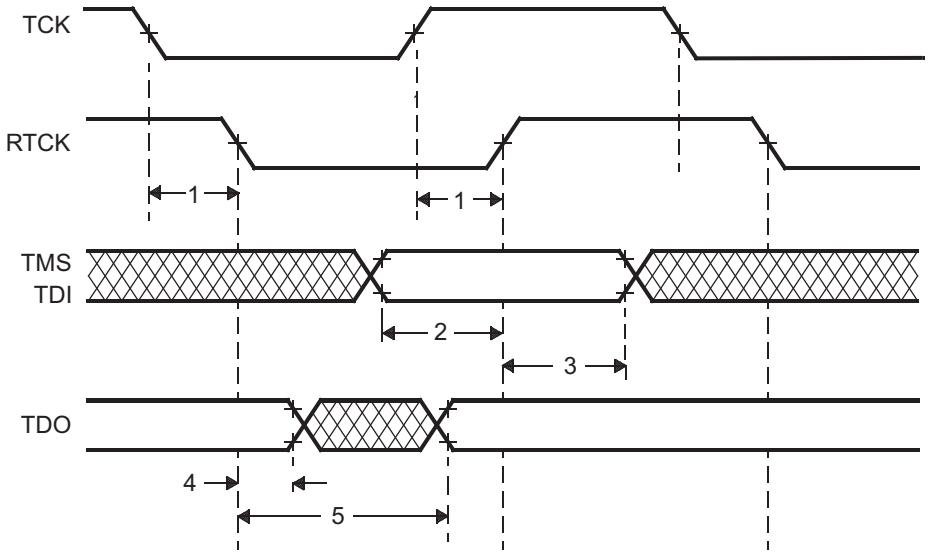

図 6-15. JTAG Timing

6.20.6 Advanced JTAG Security Module

This device includes an Advanced JTAG Security Module (AJSM), which lets the user limit JTAG access to the device after programming.

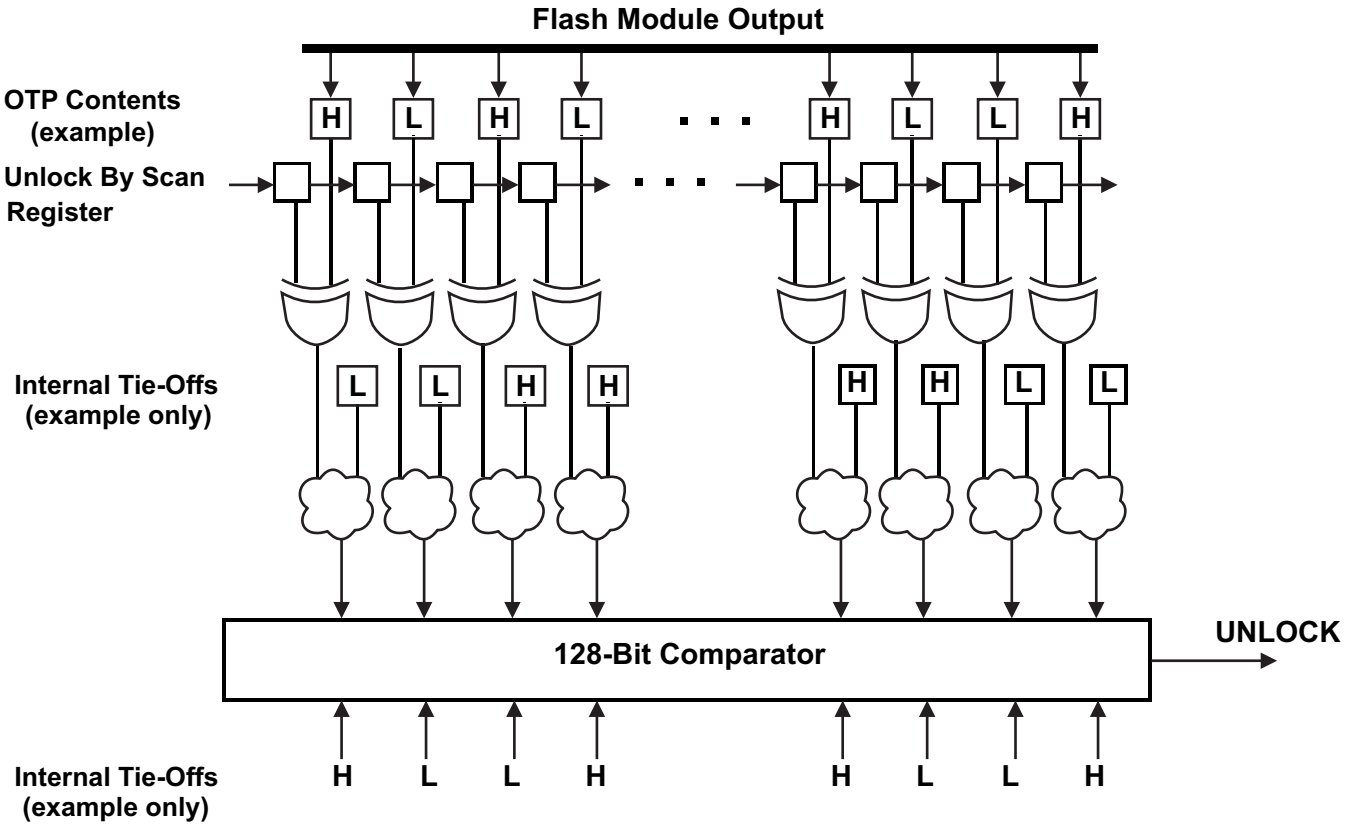

図 6-16. AJSM Unlock

The device is unlocked by default by virtue of a 128-bit visible unlock code programmed in the One-Time Programmable (OTP) address 0xF000 0000.The OTP contents are XOR-ed with the contents of the Unlock-By-Scan register. The outputs of these XOR gates are again combined with a set of secret internal tie-offs. The output of this combinational logic is compared against a secret, hard-wired, 128-bit value. A match asserts the UNLOCK signal, so that the device is now unlocked.

A user can lock the device by changing bits in the visible unlock code from 1 to 0. Changing a 0 to 1 is not possible because the visible unlock code is stored in the OTP flash region. Also, changing all the 128 bits to zeros is not a valid condition and will permanently lock the device.

Once locked, a user can unlock the device by scanning an appropriate value into the Unlock-By-Scan register of the AJSM module. This register is accessible by configuring an IR value of 0b1011 on the AJSM TAP. The value to be scanned is such that the XOR of the OTP contents and the contents of the Unlock-By-Scan register results in the original visible unlock code.

The Unlock-By-Scan register is reset only by asserting power-on reset (nPORRST).

A locked device only permits JTAG accesses to the AJSM scan chain through the Secondary TAP 2 of the ICEPick module. All other secondary TAPs, test TAPs, and the boundary scan interface are not accessible in this state.

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6.20.7 Boundary Scan Chain

The device supports BSDL-compliant boundary scan for testing pin-to-pin compatibility. The boundary scan chain is connected to the Boundary Scan Interface of the ICEPICK module.

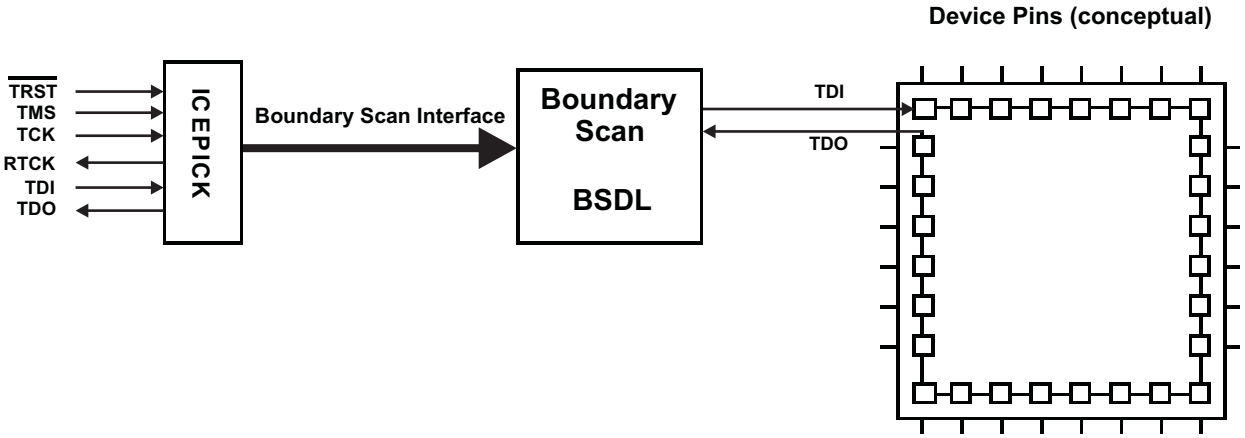

図 6-17. Boundary Scan Implementation (Conceptual Diagram)

Data is serially shifted into all boundary-scan buffers through TDI, and out through TDO.

7 Peripheral Information and Electrical Specifications

7.1 Peripheral Legend

表 7-1. Peripheral Legend

ABBREVIATION	FULL NAME
MibADC	Multibuffered Analog-to-Digital Converter
CCM-R4	CPU Compare Module – Cortex-R4
CRC	Cyclic Redundancy Check
DCAN	Controller Area Network
DCC	Dual Clock Comparator
ESM	Error Signaling Module
GIO	General-Purpose Input/Output
HTU	High-End Timer Transfer Unit
LIN	Local Interconnect Network
MibSPI	Multibuffered Serial Peripheral Interface
N2HET	Platform High-End Timer
RTI	Real-Time Interrupt Module
SCI	Serial Communications Interface
SPI	Serial Peripheral Interface
VIM	Vectored Interrupt Manager
eQEP	Enhanced Quadrature Encoder Pulse

7.2 Multibuffered 12-Bit Analog-to-Digital Converter

The multibuffered A-to-D converter (MibADC) has a separate power bus for its analog circuitry that enhances the A-to-D performance by preventing digital switching noise on the logic circuitry which could be present on V_{SS} and V_{CC} from coupling into the A-to-D analog stage. All A-to-D specifications are given with respect to AD_{REFLO} unless otherwise noted.

表 7-2. MibADC Overview

DESCRIPTION	VALUE
Resolution	12 bits
Monotonic	Assured
Output conversion code	00h to FFFh [00 for $V_{AI} \le AD_{REFLO}$; FFF for $V_{AI} \ge AD_{REFHI}$]

7.2.1 Features

- 12-bit resolution
- AD_{REFHI} and AD_{REFLO} pins (high and low reference voltages)
- Total Sample/Hold/Convert time: 600 ns Typical Minimum at 30 MHz ADCLK
- One memory region per conversion group is available (event, group 1, group 2)
- Allocation of channels to conversion groups is completely programmable
- Memory regions are serviced by interrupt
- Programmable interrupt threshold counter is available for each group
- Programmable magnitude threshold interrupt for each group for any one channel
- Option to read either 8-, or 10-, or 12-bit values from memory regions
- Single or continuous conversion modes
- Embedded self-test
- Embedded calibration logic
- Enhanced power-down mode
  - Optional feature to automatically power down ADC core when no conversion is in progress

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- External event pin (ADEVT) programmable as general-purpose I/O

7.2.2 Event Trigger Options

The ADC module supports three conversion groups: Event Group, Group1, and Group2. Each of these three groups can be configured to be hardware event-triggered. In that case, the application can select from among eight event sources to be the trigger for the conversions of a group.

7.2.2.1 MIBADC Event Trigger Hookup

表 7-3. MIBADC Event Trigger Hookup

EVENT NUMBER	SOURCE SELECT BITS For G1, G2, or EVENT (G1SRC[2:0], G2SRC[2:0], or EVSRC[2:0])	TRIGGER
1	000	ADEVT
2	001	N2HET[8]
3	010	N2HET[10]
4	011	RTI compare 0 interrupt
5	100	N2HET[12]
6	101	N2HET[14]
7	110	N2HET[17]
8	111	N2HET[19]

注

For ADEVT, N2HET trigger sources, the connection to the MibADC module trigger input is made from the output side of the input buffer. This way, a trigger condition can be generated either by configuring the function as output onto the pad, or by driving the function from an external trigger source as input. If the mux controller module is used to select different functionality instead of ADEVT or N2HET[x], care must be taken to disable these signals from triggering conversions; there is no multiplexing on input connections.

注

For the RTI compare 0 interrupt source, the connection is made directly from the output of the RTI module. That is, the interrupt condition can be used as a trigger source even if the actual interrupt is not signaled to the CPU.

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7.2.3 ADC Electrical and Timing Specifications

表 7-4. MibADC Recommended Operating Conditions

PARAMETER		MIN	MAX	UNIT
AD_{REFHI}	A-to-D high-voltage reference source	AD_{REFLO}	V_{CCAD}	V
AD_{REFLO}	A-to-D low-voltage reference source	V_{SSAD}	AD_{REFHI}	V
V_{AI}	Analog input voltage	AD_{REFLO}	AD_{REFHI}	V
I_{AIC}	Analog input clamp current ($VAI < V_{SSAD} - 0.3$ or $VAI > V_{CCAD} + 0.3$)	–2	2	mA

表 7-5. MibADC Electrical Characteristics Over Full Ranges of Recommended Operating Conditions(1)

PARAMETER		DESCRIPTION/CONDITIONS		MIN	TYP	MAX	UNIT
R_{mux}	Analog input mux on-resistance	See 図 7-1			95	250	Ω
R_{samp}	ADC sample switch on-resistance	See 図 7-1			60	250	Ω
C_{mux}	Input mux capacitance	See 図 7-1			7	16	pF
C_{samp}	ADC sample capacitance	See 図 7-1			8	13	pF
I_{AIL}	Analog off-state input leakage current	V_{CCAD} = 3.6 V MAX	$V_{SSAD} < V_{IN} < V_{SSAD}$ + 100 mV	–300	–1	200	nA
			V_{SSAD} + 100 mV < V_{IN} < V_{CCAD} - 200 mV	–200	–0.3	200	
			V_{CCAD} - 200 mV < V_{IN} < V_{CCAD}	–200	1	500	
I_{AOSB}	Analog on-state input bias	V_{CCAD} = 3.6 V MAX	$V_{SSAD} < V_{IN} < V_{SSAD}$ + 100 mV	–8		2	µA
			V_{SSAD} + 100 mV < V_{IN} < V_{CCAD} - 200 mV	–4		2	
			V_{CCAD} - 200 mV < V_{IN} < V_{CCAD}	–4		12	
$I_{ADREFHI}$	AD_{REFHI} input current	$AD_{REFHI} = V_{CCAD}$, $AD_{REFLO} = V_{SSAD}$				3	mA
I_{CCAD}	Static supply current	Normal operating mode				(2)	mA
		ADC core in power-down mode				5	µA

(1) 1 LSB = $(AD_{REFHI} - AD_{REFLO})/ 2^n$ where n = 10 in 10-bit mode and 12 in 12-bit mode
(2) See Section 5.7.

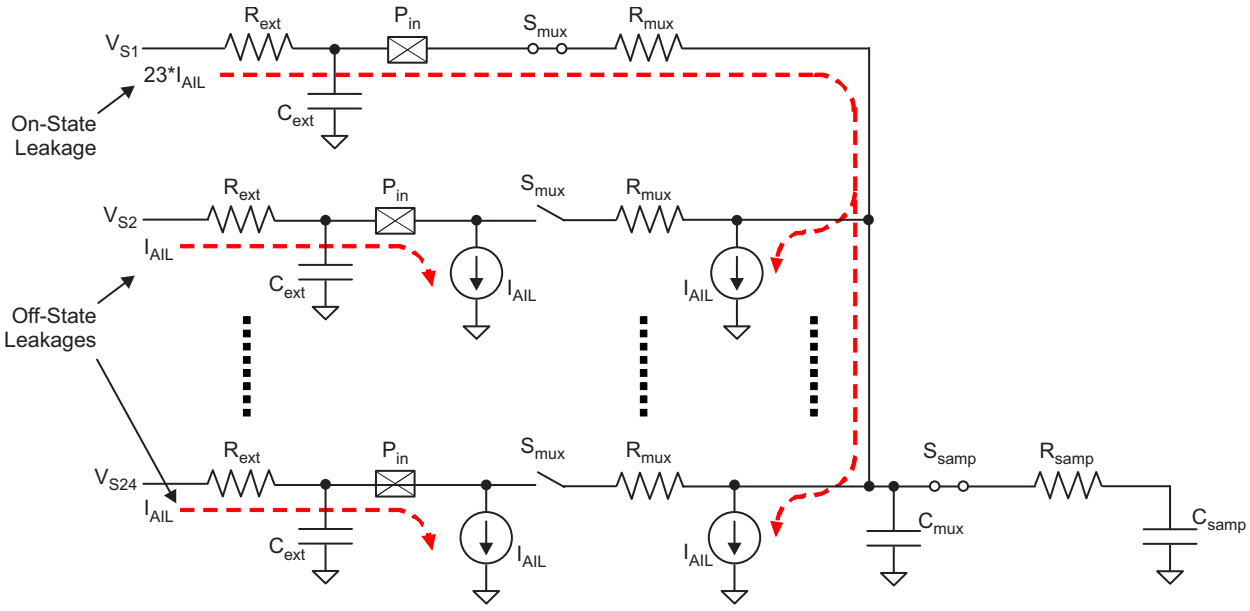

図 7-1. MibADC Input Equivalent Circuit

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表 7-6. MibADC Timing Specifications

PARAMETER		MIN	NOM	MAX	UNIT
$t_{c(ADCLK)}$ (1)	Cycle time, MibADC clock	33			ns
$t_{d(SH)}$ (2)	Delay time, sample and hold time	200			ns
$t_{d(PU-ADV)}$	Delay time from ADC power on until first input can be sampled	1			µs
12-BIT MODE					
$t_{d(C)}$	Delay time, conversion time	400			ns
$t_{d(SHC)}$ (3)	Delay time, total sample/hold and conversion time	600			ns
10-BIT MODE					
$t_{d(C)}$	Delay time, conversion time	330			ns
$t_{d(SHC)}$ (3)	Delay time, total sample/hold and conversion time	530			ns

(1) The MibADC clock is the ADCLK, generated by dividing down the VCLK by a prescale factor defined by the ADCLOCKCR register bits 4:0.
(2) The sample and hold time for the ADC conversions is defined by the ADCLK frequency and the AD<GP>SAMP register for each conversion group. The sample time must be determined by accounting for the external impedance connected to the input channel as well as the internal impedance of the ADC.
(3) This is the minimum sample/hold and conversion time that can be achieved. These parameters are dependent on many factors for example, the prescale settings.

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表 7-7. MibADC Operating Characteristics Over Full Ranges of Recommended Operating Conditions

PARAMETER		DESCRIPTION/CONDITIONS			MIN	TYP	MAX	UNIT
CR	Conversion range over which specified accuracy is maintained	AD_{REFHI} - AD_{REFLO}			3		3.6	V
Z_{SET}	Offset Error	Difference between the first ideal transition (from code 000h to 001h) and the actual transition	10-bit mode	With ADC Calibration			1	LSB (1)
				Without ADC Calibration			2	
			12-bit mode	With ADC Calibration			2	
				Without ADC Calibration			4	
F_{SET}	Gain Error	Difference between the last ideal transition (from code FFEh to FFFh) and the actual transition minus offset.	10-bit mode				2	LSB
			12-bit mode				3	
E_{DNL}	Differential nonlinearity error	Difference between the actual step width and the ideal value. (See 図 7-2)	10-bit mode				± 1.5	LSB
			12-bit mode				± 2	
E_{INL}	Integral nonlinearity error	Maximum deviation from the best straight line through the MibADC. MibADC transfer characteristics, excluding the quantization error. (See 図 7-3)	10-bit mode				± 2	LSB
			12-bit mode				± 2	
E_{TOT}	Total unadjusted error	Maximum value of the difference between an analog value and the ideal midstep value. (See 図 7-4)	10-bit mode	With ADC Calibration			± 2	LSB
				Without ADC Calibration			± 4	
			12-bit mode	With ADC Calibration			± 4	
				Without ADC Calibration			± 7	

(1) 1 LSB = $(AD_{REFHI} – AD_{REFLO})/ 2^n$ where n = 10 in 10-bit mode and 12 in 12-bit mode

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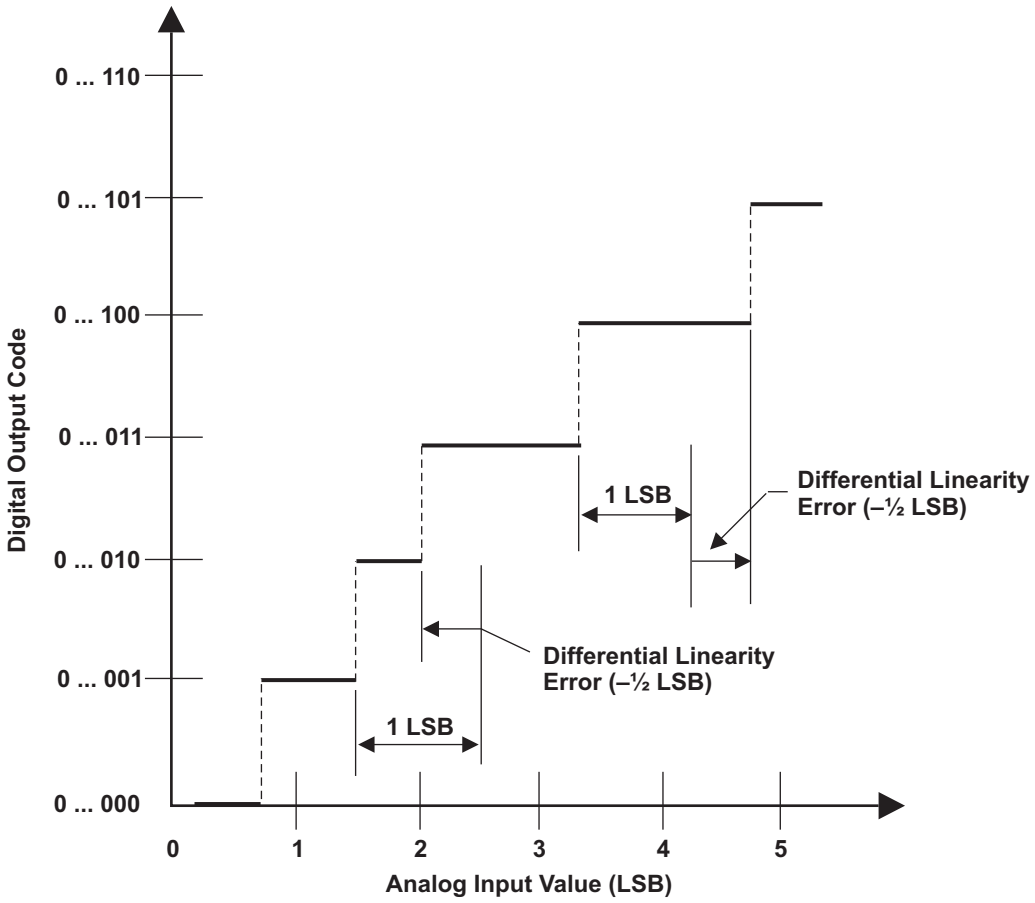
7.2.4 Performance (Accuracy) Specifications

7.2.4.1 MibADC Nonlinearity Errors

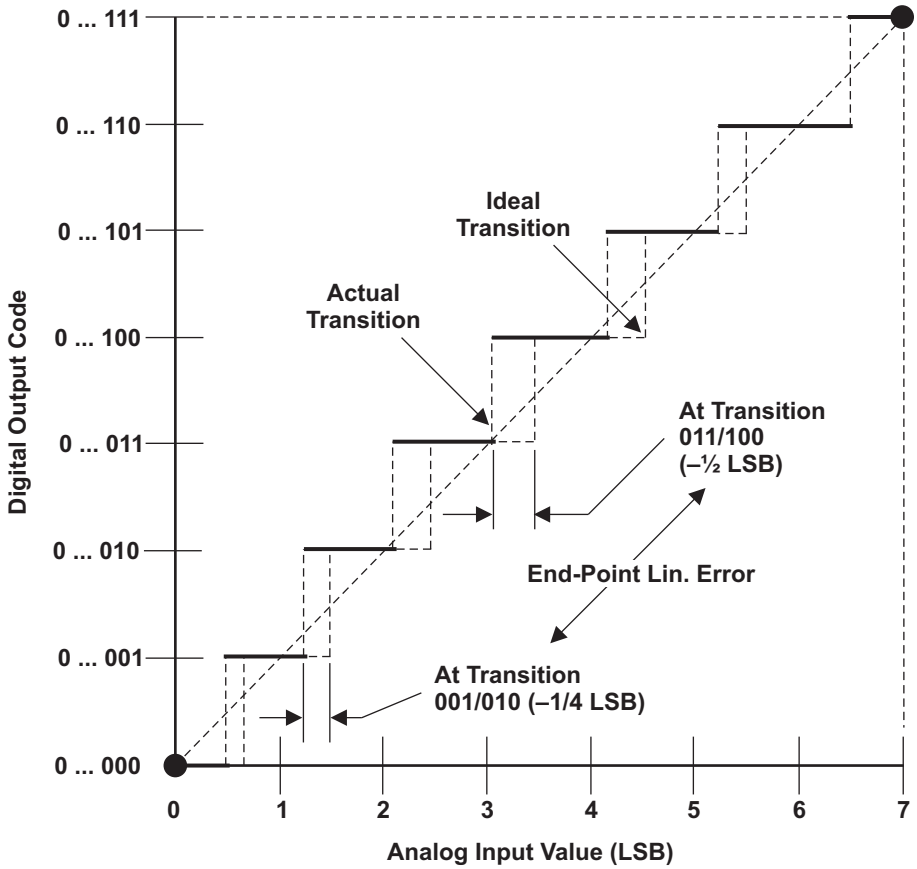
The differential nonlinearity error shown in 図 7-2 (sometimes referred to as differential linearity) is the difference between an actual step width and the ideal value of 1 LSB.



NOTE A: 1 LSB = $(AD_{REFHI} - AD_{REFLO})/2^n$ where n=10 in 10-bit mode and 12 in 12-bit mode

図 7-2. Differential Nonlinearity (DNL) Error

The integral nonlinearity error shown in 図 7-3 (sometimes referred to as linearity error) is the deviation of the values on the actual transfer function from a straight line.



NOTE A: 1 LSB = $(AD_{REFHI} - AD_{REFLO})/2^n$ where n=10 in 10-bit mode and 12 in 12-bit mode

図 7-3. Integral Nonlinearity (INL) Error

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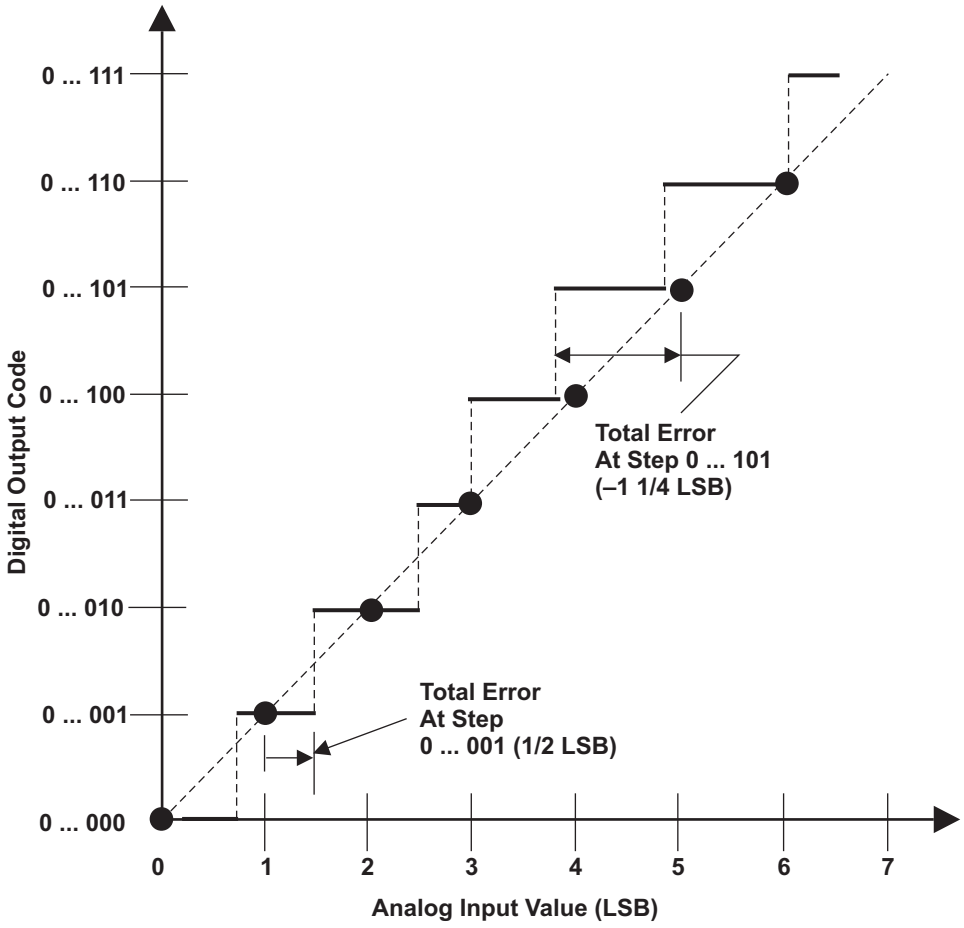
7.2.4.2 MibADC Total Error

The absolute accuracy or total error of an MibADC as shown in 図 7-4 is the maximum value of the difference between an analog value and the ideal midstep value.



NOTE A: 1 LSB = $(AD_{REFHI} - AD_{REFLO})/2^n$ where n=10 in 10-bit mode and 12 in 12-bit mode

図 7-4. Absolute Accuracy (Total) Error

7.3 General-Purpose Input/Output

The GPIO module on this device supports one port GIOA. The I/O pins are bidirectional and bit-programmable. GIOA supports external interrupt capability.

7.3.1 Features

The GPIO module has the following features:

- Each I/O pin can be configured as:
  - Input
  - Output
  - Open Drain
- The interrupts have the following characteristics:
  - Programmable interrupt detection either on both edges or on a single edge (set in GIOINTDET)
  - Programmable edge-detection polarity, either rising or falling edge (set in GIOPOL register)
  - Individual interrupt flags (set in GIOFLG register)
  - Individual interrupt enables, set and cleared through GIOENASET and GIOENACLR registers respectively
  - Programmable interrupt priority, set through GIOLVLSET and GIOLVLCLR registers
- Internal pullup/pulldown allows unused I/O pins to be left unconnected

For information on input and output timings see 5.11 and 5.12

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7.4 Enhanced High-End Timer (N2HET)

The N2HET is an advanced intelligent timer that provides sophisticated timing functions for real-time applications. The timer is software-controlled, using a reduced instruction set, with a specialized timer micromachine and an attached I/O port. The N2HET can be used for pulse width modulated outputs, capture or compare inputs, or general-purpose I/O.. It is especially well suited for applications requiring multiple sensor information and drive actuators with complex and accurate time pulses.

7.4.1 Features

The N2HET module has the following features:

- Programmable timer for input and output timing functions
- Reduced instruction set (30 instructions) for dedicated time and angle functions
- 128 words of instruction RAM protected by parity
- User defined number of 25-bit virtual counters for timer, event counters and angle counters
- 7-bit hardware counters for each pin allow up to 32-bit resolution in conjunction with the 25-bit virtual counters
- Up to 19 pins usable for input signal measurements or output signal generation
- Programmable suppression filter for each input pin with adjustable limiting frequency
- Low CPU overhead and interrupt load
- Efficient data transfer to or from the CPU memory with dedicated High-End-Timer Transfer Unit (HTU)
- Diagnostic capabilities with different loopback mechanisms and pin status readback functionality

7.4.2 N2HET RAM Organization

The timer RAM uses 4 RAM banks, where each bank has two port access capability. This means that one RAM address may be written while another address is read. The RAM words are 96-bits wide, which are split into three 32-bit fields (program, control, and data).

7.4.3 Input Timing Specifications

The N2HET instructions PCNT and WCAP impose some timing constraints on the input signals.

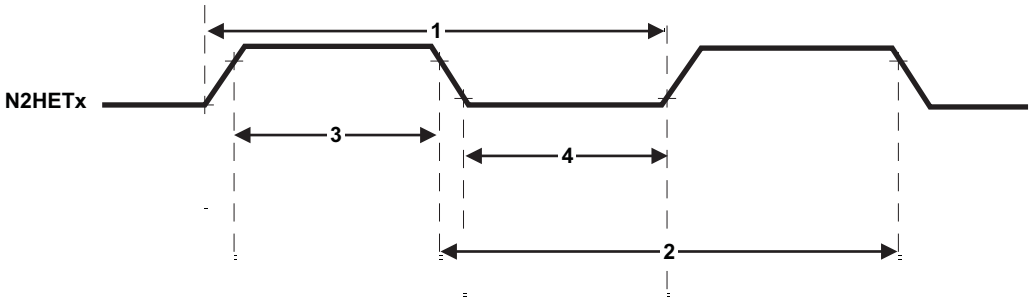

図 7-5. N2HET Input Capture Timings

表 7-8. Dynamic Characteristics for the N2HET Input Capture Functionality

PARAMETER		MIN(1) (2)	MAX(1) (2)	UNIT
1	Input signal period, PCNT or WCAP for rising edge to rising edge	(hr)(lr) $t_{c(VCLK2)}$ + 2	2^{25}(hr)(lr)$t_{c(VCLK2)}$ - 2	ns
2	Input signal period, PCNT or WCAP for falling edge to falling edge	(hr) (lr) $t_{c(VCLK2)}$ + 2	2^{25} (hr)(lr) $t_{c(VCLK2)}$ - 2	ns
3	Input signal high phase, PCNT or WCAP for rising edge to falling edge	2(hr) $t_{c(VCLK2)}$ + 2	2^{25} (hr)(lr) $t_{c(VCLK2)}$ - 2	ns
4	Input signal low phase, PCNT or WCAP for falling edge to rising edge	2(hr) $t_{c(VCLK2)}$ + 2	2^{25} (hr)(lr) $t_{c(VCLK2)}$ - 2	ns

(1) hr = High-resolution prescaler, configured using the HRPFC field of the Prescale Factor Register (HETPFR).
(2) lr = Loop-resolution prescaler, configured using the LFPRC field of the Prescale Factor Register (HETPFR).

7.4.4 N2HET Checking

7.4.4.1 Output Monitoring using Dual Clock Comparator (DCC)

N2HET[31] is connected as a clock source for counter 1 in DCC1. This allows the application to measure the frequency of the pulse-width modulated (PWM) signal on N2HET[31].

N2HET[31] can be configured to be an internal-only channel. That is, the connection to the DCC module is made directly from the output of the N2HET module (from the input of the output buffer).

For more information on DCC, see 6.6.3.

7.4.5 Disabling N2HET Outputs

Some applications require the N2HET outputs to be disabled under some fault condition. The N2HET module provides this capability through the "Pin Disable" input signal. This signal, when driven low, causes the N2HET outputs identified by a programmable register (HETPINDIS) to be tri-stated.

For more details on the "N2HET Pin Disable" feature, see the device-specific Technical Reference Manual listed in 8.2.1.

GIOA[5] and EQEPERR are connected to the "Pin Disable" input for N2HET. In the case of GIOA[5] connection, this connection is made from the output of the input buffer. In the case of EQEPERR, the EQEPERR output signal is asserted in the event of a phase error. This signal is inverted and double-synchronized to VCLK2 for input into the N2HET PIN_nDISABLE port.

The PIN_nDISABLE port input source is selectable between the GIOA[5] and EQEPERR sources. This is achieved through the PINMMR9[1:0] bits.

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7.4.6 High-End Timer Transfer Unit (N2HET)

A High-End Timer Transfer Unit (N2HET) can perform DMA type transactions to transfer N2HET data to or from main memory. A Memory Protection Unit (MPU) is built into the N2HET.

7.4.6.1 Features

- CPU independent
- Master Port to access system memory
- 8 control packets supporting dual buffer configuration
- Control packet information is stored in RAM protected by parity
- Event synchronization (N2HET transfer requests)
- Supports 32- or 64-bit transactions
- Addressing modes for N2HET address (8 byte or 16 byte) and system memory address (fixed, 32-bit or 64-bit)
- One shot, circular, and auto switch buffer transfer modes
- Request lost detection

7.4.6.2 Trigger Connections

表 7-9. N2HET Request Line Connection

MODULES	REQUEST SOURCE	HTU REQUEST
N2HET	HTUREQ[0]	HTU DCP[0]
N2HET	HTUREQ[1]	HTU DCP[1]
N2HET	HTUREQ[2]	HTU DCP[2]
N2HET	HTUREQ[3]	HTU DCP[3]
N2HET	HTUREQ[4]	HTU DCP[4]
N2HET	HTUREQ[5]	HTU DCP[5]
N2HET	HTUREQ[6]	HTU DCP[6]
N2HET	HTUREQ[7]	HTU DCP[7]

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7.5 Controller Area Network (DCAN)

The DCAN supports the CAN 2.0B protocol standard and uses a serial, multimaster communication protocol that efficiently supports distributed real-time control with robust communication rates of up to 1 Mbps. The DCAN is ideal for applications operating in noisy and harsh environments (for example, automotive and industrial fields) that require reliable serial communication or multiplexed wiring.

7.5.1 Features

Features of the DCAN module include:

- Supports CAN protocol version 2.0 part A, B
- Bit rates up to 1 Mbps
- The CAN kernel can be clocked by the oscillator for baud-rate generation.
- 32 and 16 mailboxes on DCAN1 and DCAN2, respectively
- Individual identifier mask for each message object
- Programmable FIFO mode for message objects
- Programmable loop-back modes for self-test operation
- Automatic bus on after Bus-Off state by a programmable 32-bit timer
- Message RAM protected by parity
- Direct access to Message RAM during test mode
- CAN RX / TX pins configurable as general-purpose I/O pins
- Message RAM Auto Initialization

For more information on the DCAN, see the device-specific Technical Reference Manual listed in 8.2.1.

7.5.2 Electrical and Timing Specifications

表 7-10. Dynamic Characteristics for the DCANx TX and RX pins

PARAMETER		MIN	MAX	UNIT
$t_{d(CANnTX)}$	Delay time, transmit shift register to CANnTX pin(1)		15	ns
$t_{d(CANnRX)}$	Delay time, CANnRX pin to receive shift register		5	ns

(1) These values do not include rise/fall times of the output buffer.

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7.6 Local Interconnect Network Interface (LIN)

The SCI/LIN module can be programmed to work either as an SCI or as a LIN. The core of the module is an SCI. The SCI's hardware features are augmented to achieve LIN compatibility.

The SCI module is a universal asynchronous receiver-transmitter that implements the standard nonreturn to zero format. The SCI can be used to communicate, for example, through an RS-232 port or over a K-line.

The LIN standard is based on the SCI (UART) serial data link format. The communication concept is single-master/multiple-slave with a message identification for multicast transmission between any network nodes.

7.6.1 LIN Features

The following are features of the LIN module:

- Compatible to LIN 1.3, 2.0 and 2.1 protocols
- Multibuffered receive and transmit units
- Identification masks for message filtering
- Automatic Master Header Generation
  - Programmable Synch Break Field
  - Synch Field
  - Identifier Field
- Slave Automatic Synchronization
  - Synch break detection
  - Optional baudrate update
  - Synchronization Validation
- 2^{31} programmable transmission rates with 7 fractional bits
- Error detection
- 2 Interrupt lines with priority encoding

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7.7 Multibuffered / Standard Serial Peripheral Interface

The MibSPI is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length (2 to 16 bits) to be shifted in and out of the device at a programmed bit-transfer rate. Typical applications for the SPI include interfacing to external peripherals, such as I/Os, memories, display drivers, and ADCs.

7.7.1 Features

Both Standard and MibSPI modules have the following features:

- 16-bit shift register
- Receive buffer register
- 11-bit baud clock generator
- SPICLK can be internally generated (master mode) or received from an external clock source (slave mode)
- Each word transferred can have a unique format
- SPI I/Os not used in the communication can be used as digital input/output signals

表 7-11. MibSPI/SPI Default Configurations

MibSPIx/SPIx	I/Os
MibSPI1	MIBSPI1SIMO[0], MIBSPI1SOMI[0], MIBSPI1CLK, MIBSPI1nCS[3:0], MIBSPI1nENA
SPI2	SPI2SIMO, SPI2SOMI, SPI2CLK, SPI2nCS[0]
SPI3	SPI3SIMO, SPI3SOMI, SPI3CLK, SPI3nENA, SPI3nCS[0]

7.7.2 MibSPI Transmit and Receive RAM Organization

The Multibuffer RAM is comprised of 128 buffers. Each entry in the Multibuffer RAM consists of four parts: a 16-bit transmit field, a 16-bit receive field, a 16-bit control field, and a 16-bit status field. The Multibuffer RAM can be partitioned into multiple transfer group with variable number of buffers each.

7.7.3 MibSPI Transmit Trigger Events

Each of the transfer groups can be configured individually. For each of the transfer groups a trigger event and a trigger source can be chosen. A trigger event can be, for example, a rising edge or a permanent low level at a selectable trigger source. Up to 15 trigger sources are available which can be used by each transfer group. These trigger options are listed in 表 7-12.

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7.7.3.1 MIBSPI1 Event Trigger Hookup

表 7-12. MIBSPI1 Event Trigger Hookup

EVENT NO.	TGxCTRL TRIGSRC[3:0]	TRIGGER
Disabled	0000	No trigger source
EVENT0	0001	GIOA[0]
EVENT1	0010	GIOA[1]
EVENT2	0011	GIOA[2]
EVENT3	0100	GIOA[3]
EVENT4	0101	GIOA[4]
EVENT5	0110	GIOA[5]
EVENT6	0111	GIOA[6]
EVENT7	1000	GIOA[7]
EVENT8	1001	N2HET[8]
EVENT9	1010	N2HET[10]
EVENT10	1011	N2HET[12]
EVENT11	1100	N2HET[14]
EVENT12	1101	N2HET[16]
EVENT13	1110	N2HET[18]
EVENT14	1111	Internal Tick counter

注

For N2HET trigger sources, the connection to the MibSPI1 module trigger input is made from the input side of the output buffer (at the N2HET module boundary). This way, a trigger condition can be generated even if the N2HET signal is not selected to be output on the pad.

注

For GIOx trigger sources, the connection to the MibSPI1 module trigger input is made from the output side of the input buffer. This way, a trigger condition can be generated either by selecting the GIOx pin as an output pin, or by driving the GIOx pin from an external trigger source.

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7.7.4 MibSPI/SPI Master Mode I/O Timing Specifications

表 7-13. SPI Master Mode External Timing Parameters (CLOCK PHASE = 0, SPICLK = output, SPISIMO = output, and SPISOMI = input)(1)(2)(3)

NO.	PARAMETER			MIN	MAX	UNIT
1	$t_{c(SPC)M}$	Cycle time, SPICLK(4)		40	$256t_{c(VCLK)}$	ns
2(5)	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 0)		$0.5t_{c(SPC)M} - t_{r(SPC)M} - 3$	$0.5t_{c(SPC)M} + 3$	ns
	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 1)		$0.5t_{c(SPC)M} - t_{f(SPC)M} - 3$	$0.5t_{c(SPC)M} + 3$	
3(5)	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 0)		$0.5t_{c(SPC)M} - t_{f(SPC)M} - 3$	$0.5t_{c(SPC)M} + 3$	ns
	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 1)		$0.5t_{c(SPC)M} - t_{r(SPC)M} - 3$	$0.5t_{c(SPC)M} + 3$	
4(5)	$t_{d(SPCH-SIMO)M}$	Delay time, SPISIMO valid before SPICLK low (clock polarity = 0)		$0.5t_{c(SPC)M} - 6$		ns
	$t_{d(SPCL-SIMO)M}$	Delay time, SPISIMO valid before SPICLK high (clock polarity = 1)		$0.5t_{c(SPC)M} - 6$		
5(5)	$t_{v(SPCL-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK low (clock polarity = 0)		$0.5t_{c(SPC)M} - t_{f(SPC)} - 4$		ns
	$t_{v(SPCH-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK high (clock polarity = 1)		$0.5t_{c(SPC)M} - t_{r(SPC)} - 4$		
6(5)	$t_{su(SOMI-SPCL)M}$	Setup time, SPISOMI before SPICLK low (clock polarity = 0)		$t_{f(SPC)} + 2.2$		ns
	$t_{su(SOMI-SPCH)M}$	Setup time, SPISOMI before SPICLK high (clock polarity = 1)		$t_{r(SPC)} + 2.2$		
7(5)	$t_{h(SPCL-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity = 0)		10		ns
	$t_{h(SPCH-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 1)		10		
8(6)	$t_{C2TDELAY}$	Setup time CS active until SPICLK high (clock polarity = 0)	CSHOLD = 0	$C2TDELAY*t_{c(VCLK)} + 2*t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} - 7$	$(C2TDELAY+2) * t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} + 5.5$	ns
			CSHOLD = 1	$C2TDELAY*t_{c(VCLK)} + 3*t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} - 7$	$(C2TDELAY+3) * t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} + 5.5$	
		Setup time CS active until SPICLK low (clock polarity = 1)	CSHOLD = 0	$C2TDELAY*t_{c(VCLK)} + 2*t_{c(VCLK)} - t_{f(SPICS)} + t_{f(SPC)} - 7$	$(C2TDELAY+2) * t_{c(VCLK)} - t_{f(SPICS)} + t_{f(SPC)} + 5.5$	ns
			CSHOLD = 1	$C2TDELAY*t_{c(VCLK)} + 3*t_{c(VCLK)} - t_{f(SPICS)} + t_{f(SPC)} - 7$	$(C2TDELAY+3) * t_{c(VCLK)} - t_{f(SPICS)} + t_{f(SPC)} + 5.5$	
9(6)	$t_{T2CDELAY}$	Hold time SPICLK low until CS inactive (clock polarity = 0)		$0.5*t_{c(SPC)M} + T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{f(SPC)} + t_{r(SPICS)} - 7$	$0.5*t_{c(SPC)M} + T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{f(SPC)} + t_{r(SPICS)} + 11$	ns
		Hold time SPICLK high until CS inactive (clock polarity = 1)		$0.5*t_{c(SPC)M} + T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{r(SPC)} + tr(SPICS) - 7$	$0.5*t_{c(SPC)M} + T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{r(SPC)} + t_{r(SPICS)} + 11$	ns
10	t_{SPIENA}	SPIENAn Sample point		$(C2TDELAY+1) * t_{c(VCLK)} - t_{f(SPICS)} - 29$	$(C2TDELAY+1)*t_{c(VCLK)}$	ns
11	$t_{SPIENAW}$	SPIENAn Sample point from write to buffer			$(C2TDELAY+2)*t_{c(VCLK)}$	ns

(1) The MASTER bit (SPIGCR1.0) is set and the CLOCK PHASE bit (SPIFMTx.16) is cleared.
(2) $t_{c(VCLK)}$ = interface clock cycle time = 1 / $f_{(VCLK)}$
(3) For rise and fall timings, see 表 5-6.
(4) When the SPI is in Master mode, the following must be true:
For PS values from 1 to 255: $t_{c(SPC)M} \geq (PS + 1)t_{c(VCLK)} \geq 40$ ns, where PS is the prescale value set in the SPIFMTx.[15:8] register bits.
For PS values of 0: $t_{c(SPC)M} = 2t_{c(VCLK)} \geq 40$ ns.
The external load on the SPICLK pin must be less than 60 pF.
(5) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).
(6) C2TDELAY and T2CDELAY is programmed in the SPIDELAY register

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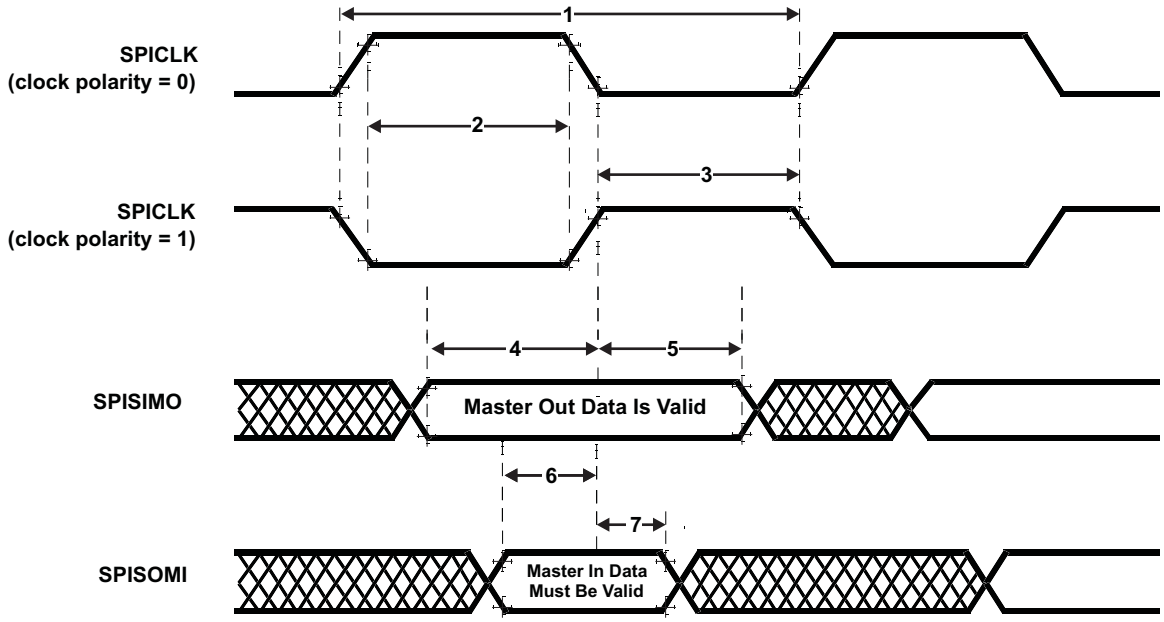

図 7-6. SPI Master Mode External Timing (CLOCK PHASE = 0)

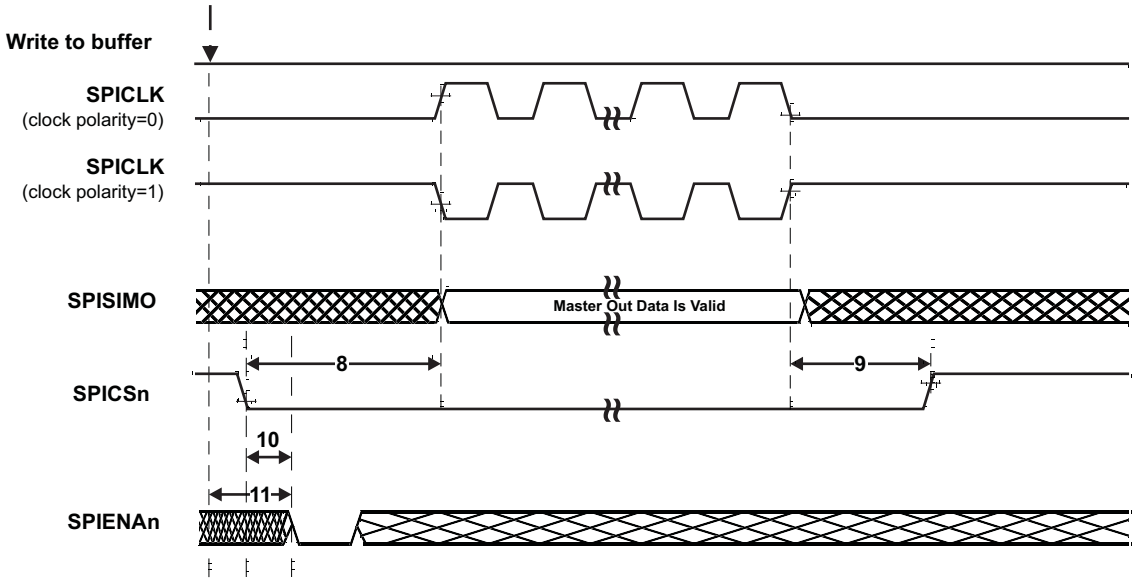

図 7-7. SPI Master Mode Chip Select Timing (CLOCK PHASE = 0)

表 7-14. SPI Master Mode External Timing Parameters (CLOCK PHASE = 1, SPICLK = output, SPISIMO = output, and SPISOMI = input)(1)(2)(3)

NO.	PARAMETER			MIN	MAX	UNIT
1	$t_{c(SPC)M}$	Cycle time, SPICLK (4)		40	$256t_{c(VCLK)}$	ns
2(5)	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 0)		$0.5t_{c(SPC)M} - t_{r(SPC)M} - 3$	$0.5t_{c(SPC)M} + 3$	ns
	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 1)		$0.5t_{c(SPC)M} - t_{f(SPC)M} - 3$	$0.5t_{c(SPC)M} + 3$	
3(5)	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 0)		$0.5t_{c(SPC)M} - t_{f(SPC)M} - 3$	$0.5t_{c(SPC)M} + 3$	ns
	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 1)		$0.5t_{c(SPC)M} - t_{r(SPC)M} - 3$	$0.5t_{c(SPC)M} + 3$	
4(5)	$t_{v(SIMO-SPCH)M}$	Valid time, SPICLK high after SPISIMO data valid (clock polarity = 0)		$0.5t_{c(SPC)M} - 6$		ns
	$t_{v(SIMO-SPCL)M}$	Valid time, SPICLK low after SPISIMO data valid (clock polarity = 1)		$0.5t_{c(SPC)M} - 6$		
5(5)	$t_{v(SPCH-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK high (clock polarity = 0)		$0.5t_{c(SPC)M} - t_{r(SPC)} - 4$		ns
	$t_{v(SPCL-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK low (clock polarity = 1)		$0.5t_{c(SPC)M} - t_{f(SPC)} - 4$		
6(5)	$t_{su(SOMI-SPCH)M}$	Setup time, SPISOMI before SPICLK high (clock polarity = 0)		$t_{r(SPC)} + 2.2$		ns
	$t_{su(SOMI-SPCL)M}$	Setup time, SPISOMI before SPICLK low (clock polarity = 1)		$t_{f(SPC)} + 2.2$		
7(5)	$t_{v(SPCH-SOMI)M}$	Valid time, SPISOMI data valid after SPICLK high (clock polarity = 0)		10		ns
	$t_{v(SPCL-SOMI)M}$	Valid time, SPISOMI data valid after SPICLK low (clock polarity = 1)		10		
8(6)	$t_{C2TDELAY}$	Setup time CS active until SPICLK high (clock polarity = 0)	CSHOLD = 0	$0.5*t_{c(SPC)M} + (C2TDELAY+2) * t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} - 7$	$0.5*t_{c(SPC)M} + (C2TDELAY+2) * t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} + 5.5$	ns
			CSHOLD = 1	$0.5*t_{c(SPC)M} + (C2TDELAY+3) * t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} - 7$	$0.5*t_{c(SPC)M} + (C2TDELAY+3) * t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} + 5.5$	
		Setup time CS active until SPICLK low (clock polarity = 1)	CSHOLD = 0	$0.5*t_{c(SPC)M} + (C2TDELAY+2) * t_{c(VCLK)} - t_{f(SPICS)} + t_{f(SPC)} - 7$	$0.5*t_{c(SPC)M} + (C2TDELAY+2) * t_{c(VCLK)} - t_{f(SPICS)} + t_{f(SPC)} + 5.5$	ns
			CSHOLD = 1	$0.5*t_{c(SPC)M} + (C2TDELAY+3) * t_{c(VCLK)} - t_{f(SPICS)} + t_{f(SPC)} - 7$	$0.5*t_{c(SPC)M} + (C2TDELAY+3) * t_{c(VCLK)} - t_{f(SPICS)} + t_{f(SPC)} + 5.5$	
9(6)	$t_{T2CDELAY}$	Hold time SPICLK low until CS inactive (clock polarity = 0)		$T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{f(SPC)} + t_{r(SPICS)} - 7$	$T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{f(SPC)} + t_{r(SPICS)} + 11$	ns
		Hold time SPICLK high until CS inactive (clock polarity = 1)		$T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{r(SPC)} + t_{r(SPICS)} - 7$	$T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{r(SPC)} + t_{r(SPICS)} + 11$	ns
10	t_{SPIENA}	SPIENAn Sample Point		$(C2TDELAY+1)* t_{c(VCLK)} - t_{f(SPICS)} - 29$	$(C2TDELAY+1)*t_{c(VCLK)}$	ns
11	$t_{SPIENAW}$	SPIENAn Sample point from write to buffer			$(C2TDELAY+2)*t_{c(VCLK)}$	ns

(1) The MASTER bit (SPIGCR1.0) is set and the CLOCK PHASE bit (SPIFMTx.16) is set.
(2) $t_{c(VCLK)}$ = interface clock cycle time = 1 / $f_{(VCLK)}$
(3) For rise and fall timings, see the 表 5-6.
(4) When the SPI is in Master mode, the following must be true:
For PS values from 1 to 255: $t_{c(SPC)M} \geq (PS + 1)t_{c(VCLK)} \geq 40$ ns, where PS is the prescale value set in the SPIFMTx.[15:8] register bits.
For PS values of 0: $t_{c(SPC)M} = 2t_{c(VCLK)} \geq 40$ ns.
The external load on the SPICLK pin must be less than 60 pF.
(5) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).
(6) C2TDELAY and T2CDELAY is programmed in the SPIDELAY register

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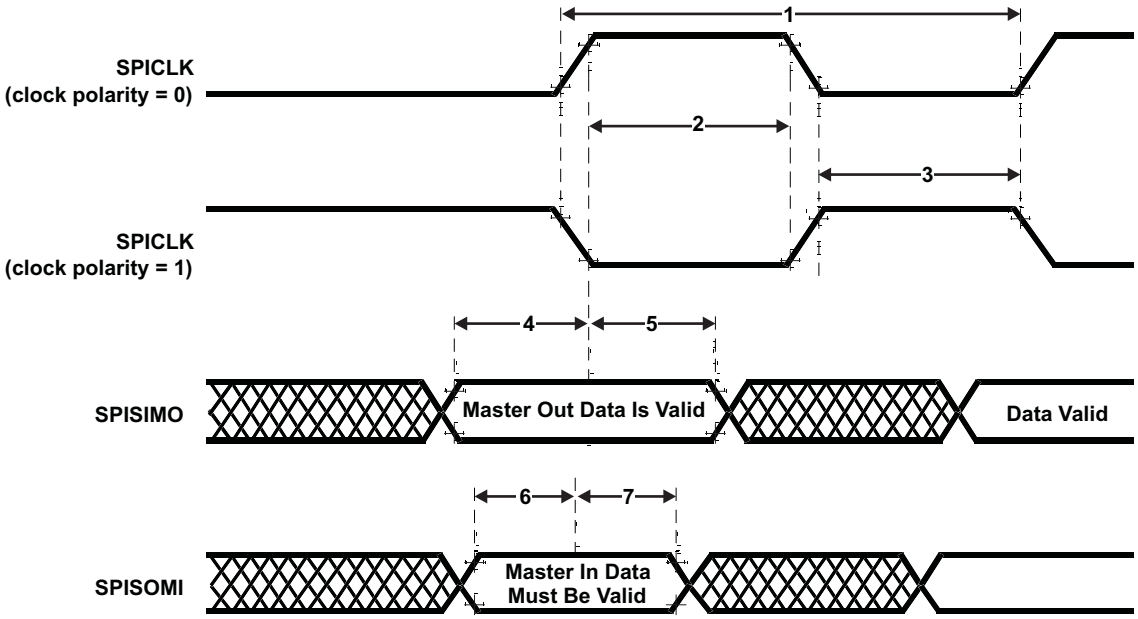

図 7-8. SPI Master Mode External Timing (CLOCK PHASE = 1)

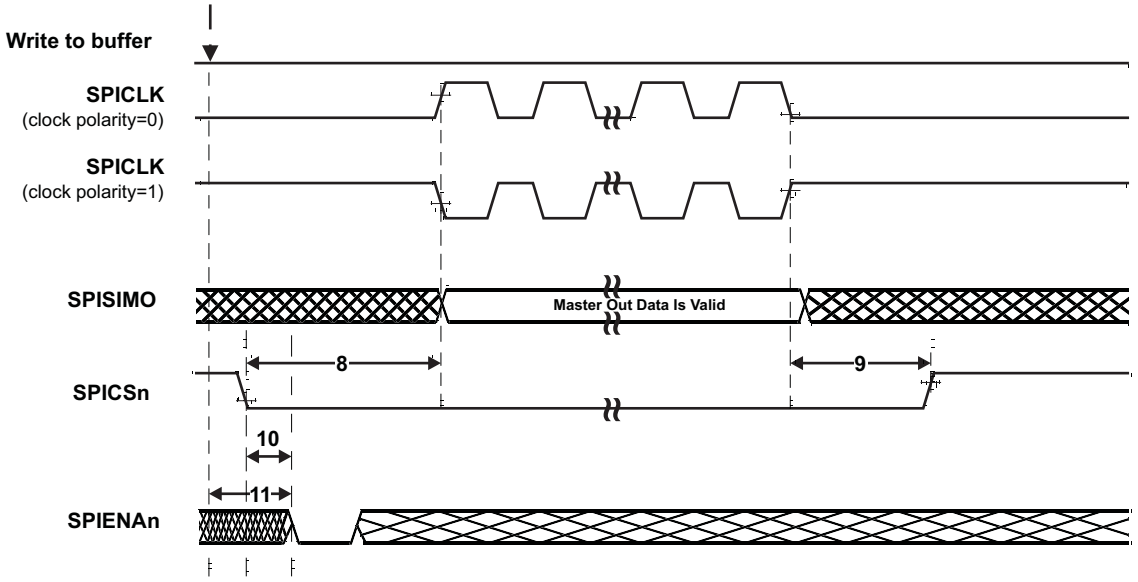

図 7-9. SPI Master Mode Chip Select Timing (CLOCK PHASE = 1)

7.7.5 SPI Slave Mode I/O Timings

表 7-15. SPI Slave Mode External Timing Parameters (CLOCK PHASE = 0, SPICLK = input, SPISIMO = input, and SPISOMI = output)(1)(2)(3)(4)

NO.	PARAMETER		MIN	MAX	UNIT
1	$t_{c(SPC)S}$	Cycle time, SPICLK(5)	40		ns
2(6)	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 0)	14		ns
	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 1)	14		
3(6)	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 0)	14		ns
	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 1)	14		
4(6)	$t_{d(SPCH-SOMI)S}$	Delay time, SPISOMI valid after SPICLK high (clock polarity = 0)		$t_{rf(SOMI)}$ + 20	ns
	$t_{d(SPCL-SOMI)S}$	Delay time, SPISOMI valid after SPICLK low (clock polarity = 1)		$t_{rf(SOMI)}$ + 20	
5(6)	$t_{h(SPCH-SOMI)S}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity =0)	2		ns
	$t_{h(SPCL-SOMI)S}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity =1)	2		
6(6)	$t_{su(SIMO-SPCL)S}$	Setup time, SPISIMO before SPICLK low (clock polarity = 0)	4		ns
	$t_{su(SIMO-SPCH)S}$	Setup time, SPISIMO before SPICLK high (clock polarity = 1)	4		
7(6)	$t_{h(SPCL-SIMO)S}$	Hold time, SPISIMO data valid after SPICLK low (clock polarity = 0)	2		ns
	$t_{h(SPCH-SIMO)S}$	Hold time, SPISIMO data valid after S PICLK high (clock polarity = 1)	2		
8	$t_{d(SPCL-SENAH)S}$	Delay time, SPIENAn high after last SPICLK low (clock polarity = 0)	$1.5t_{c(VCLK)}$	$2.5t_{c(VCLK)}+t_{r(ENAn)}+22$	ns
	$t_{d(SPCH-SENAH)S}$	Delay time, SPIENAn high after last SPICLK high (clock polarity = 1)	$1.5t_{c(VCLK)}$	$2.5t_{c(VCLK)}+t_{r(ENAn)}+22$	
9	$t_{d(SCSL-SENAL)S}$	Delay time, SPIENAn low after SPICSn low (if new data has been written to the SPI buffer)	$t_{f(ENAn)}$	$t_{c(VCLK)}+t_{f(ENAn)}+27$	ns

(1) The MASTER bit (SPIGCR1.0) is cleared and the CLOCK PHASE bit (SPIFMTx.16) is cleared.
(2) If the SPI is in slave mode, the following must be true: $t_{c(SPC)S} \geq (PS + 1)\ t_{c(VCLK)}$, where PS = prescale value set in SPIFMTx.[15:8].
(3) For rise and fall timings, see 表 5-6.
(4) $t_{c(VCLK)}$ = interface clock cycle time = $1 / f_{(VCLK)}$
(5) When the SPI is in Slave mode, the following must be true:
For PS values from 1 to 255: $t_{c(SPC)S} \geq (PS + 1)t_{c(VCLK)} \geq 40$ ns, where PS is the prescale value set in the SPIFMTx.[15:8] register bits.
For PS values of 0: $t_{c(SPC)S} = 2t_{c(VCLK)} \geq 40$ ns.
(6) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).

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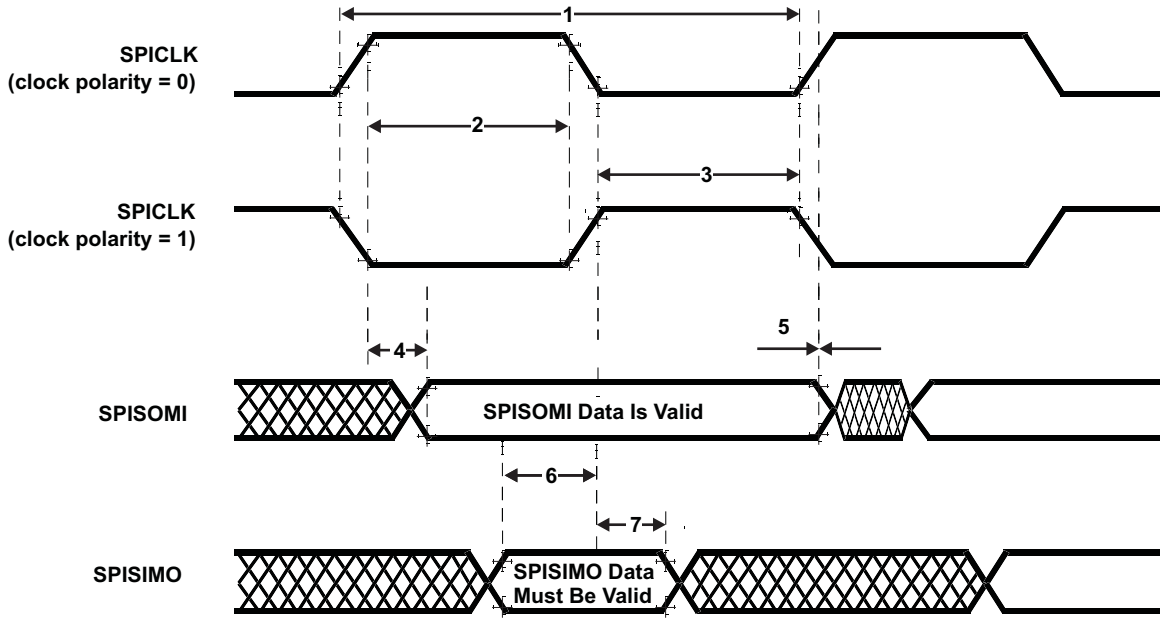

図 7-10. SPI Slave Mode External Timing (CLOCK PHASE = 0)

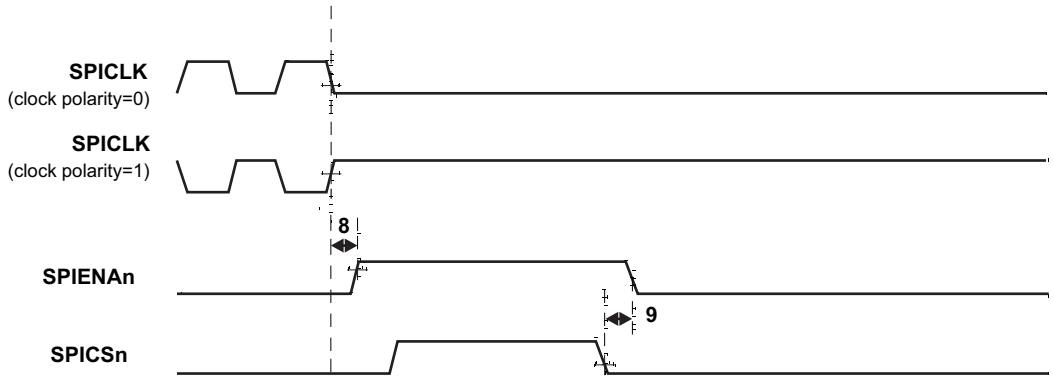

図 7-11. SPI Slave Mode Enable Timing (CLOCK PHASE = 0)

表 7-16. SPI Slave Mode External Timing Parameters (CLOCK PHASE = 1, SPICLK = input, SPISIMO = input, and SPISOMI = output)(1)(2)(3)(4)

NO.	PARAMETER		MIN	MAX	UNIT
1	$t_{c(SPC)S}$	Cycle time, SPICLK(5)	40		ns
2(6)	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 0)	14		ns
	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 1)	14		
3(6)	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 0)	14		ns
	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 1)	14		
4(6)	$t_{d(SOMI-SPCL)S}$	Dealy time, SPISOMI data valid after SPICLK low (clock polarity = 0)		$t_{rf(SOMI)}$ + 20	ns
	$t_{d(SOMI-SPCH)S}$	Delay time, SPISOMI data valid after SPICLK high (clock polarity = 1)		$t_{rf(SOMI)}$ + 20	
5(6)	$t_{h(SPCL-SOMI)S}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity =0)	2		ns
	$t_{h(SPCH-SOMI)S}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity =1)	2		
6(6)	$t_{su(SIMO-SPCH)S}$	Setup time, SPISIMO before SPICLK high (clock polarity = 0)	4		ns
	$t_{su(SIMO-SPCL)S}$	Setup time, SPISIMO before SPICLK low (clock polarity = 1)	4		
7(6)	$t_{v(SPCH-SIMO)S}$	High time, SPISIMO data valid after SPICLK high (clock polarity = 0)	2		ns
	$t_{v(SPCL-SIMO)S}$	High time, SPISIMO data valid after SPICLK low (clock polarity = 1)	2		
8	$t_{d(SPCH-SENAH)S}$	Delay time, SPIENAn high after last SPICLK high (clock polarity = 0)	$1.5t_{c(VCLK)}$	$2.5t_{c(VCLK)}+t_{r(ENAn)}$ + 22	ns
	$t_{d(SPCL-SENAH)S}$	Delay time, SPIENAn high after last SPICLK low (clock polarity = 1)	$1.5t_{c(VCLK)}$	$2.5t_{c(VCLK)}+t_{r(ENAn)}$ + 22	
9	$t_{d(SCSL-SENAL)S}$	Delay time, SPIENAn low after SPICSn low (if new data has been written to the SPI buffer)	$t_{f(ENAn)}$	$t_{c(VCLK)}+t_{f(ENAn)}$+ 27	ns
10	$t_{d(SCSL-SOMI)S}$	Delay time, SOMI valid after SPICSn low (if new data has been written to the SPI buffer)	$t_{c(VCLK)}$	$2t_{c(VCLK)}+t_{rf(SOMI)}$+ 28	ns

(1) The MASTER bit (SPIGCR1.0) is cleared and the CLOCK PHASE bit (SPIFMTx.16) is set.
(2) If the SPI is in slave mode, the following must be true: tc(SPC)S ≤ (PS + 1) tc(VCLK), where PS = prescale value set in SPIFMTx.[15:8].
(3) For rise and fall timings, see 表 5-6.
(4) $t_{c(VCLK)}$ = interface clock cycle time = 1 /$f_{(VCLK)}$
(5) When the SPI is in Slave mode, the following must be true:
For PS values from 1 to 255: $t_{c(SPC)S}$ ≥ (PS +1)$t_{c(VCLK)}$ ≥ 40 ns, where PS is the prescale value set in the SPIFMTx.[15:8] register bits.
For PS values of 0: $t_{c(SPC)S}$ = $2t_{c(VCLK)}$ ≥ 40 ns.
(6) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).

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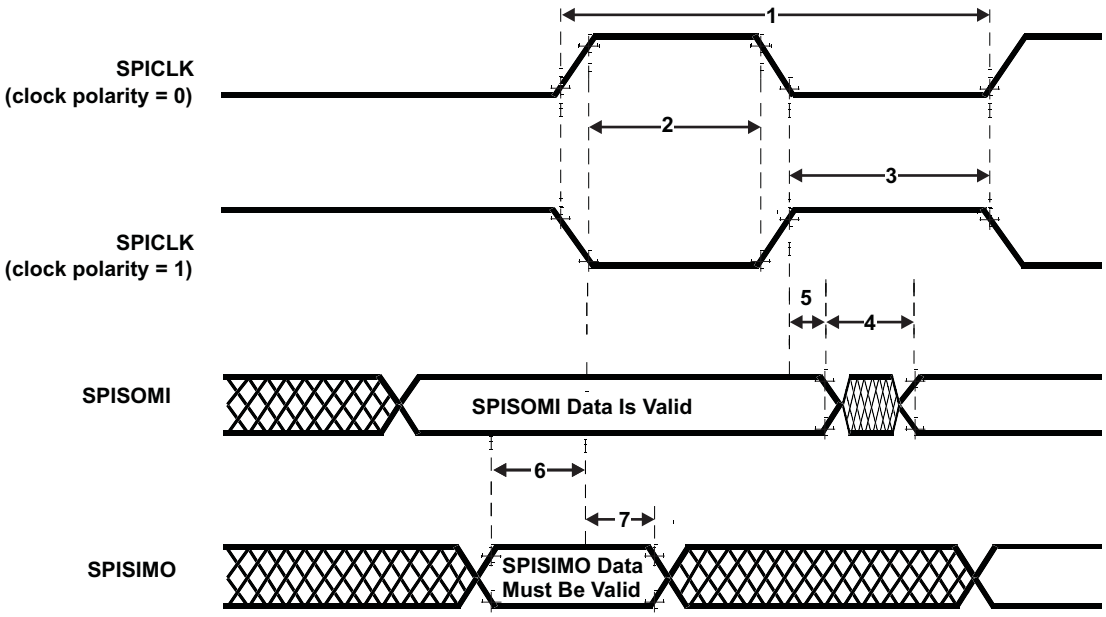

図 7-12. SPI Slave Mode External Timing (CLOCK PHASE = 1)

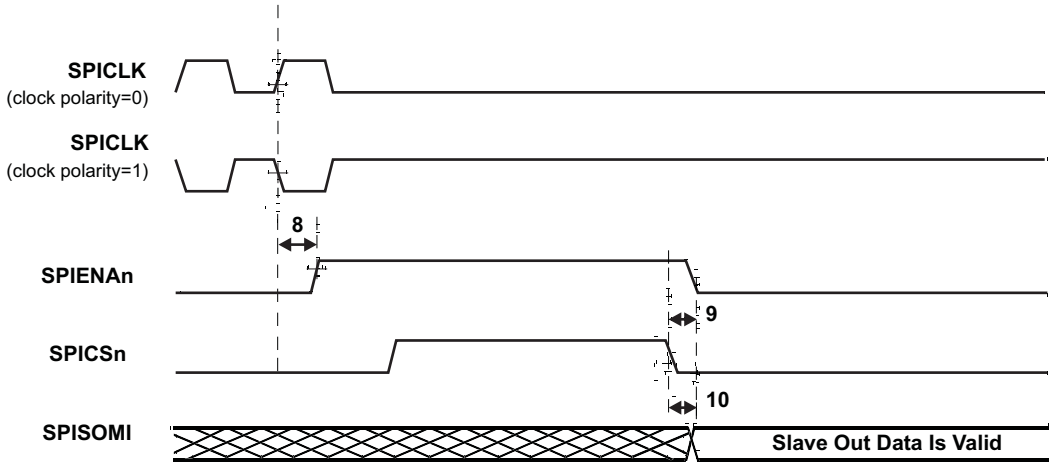

図 7-13. SPI Slave Mode Enable Timing (CLOCK PHASE = 1)

7.8 Enhanced Quadrature Encoder (eQEP)

図 7-14 shows the eQEP module interconnections on the device.

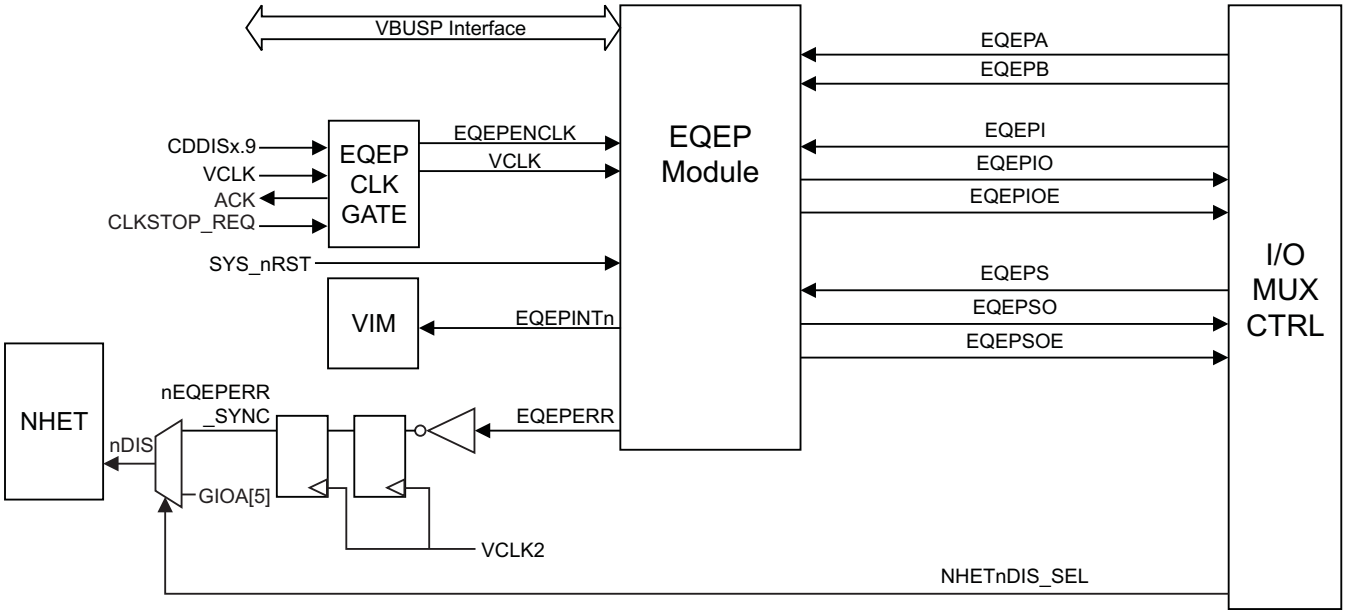

図 7-14. eQEP Module Interconnections

7.8.1 Clock Enable Control for eQEPx Modules

The device level control of the eQEP clock is accomplished through the enable/disable of the VCLK clock domain for eQEP only. This is realized using bit 9 of the CLKDDIS register. The eQEP clock source is enabled by default.

7.8.2 Using eQEPx Phase Error

The eQEP module sets the EQEPERR signal output whenever a phase error is detected in its inputs EQEPxA and EQEPxB. This error signal from both the eQEP modules is input to the connection selection multiplexor. As shown in 図 7-14, the output of this selection multiplexor is inverted and connected to the N2HET module. This connection allows the application to define the response to a phase error indicated by the eQEP modules.

7.8.3 Input Connections to eQEPx Modules

The input connections to each of the eQEP modules can be selected between a double-VCLK-synchronized input or a double-VCLK-synchronized and filtered input, as shown in 表 7-17.

表 7-17. Device-Level Input Synchronization

INPUT SIGNAL	CONTROL FOR DOUBLE-SYNCHRONIZED CONNECTION TO eQEPx	CONTROL FOR DOUBLE-SYNCHRONIZED AND FILTERED CONNECTION TO eQEPx
eQEPA	PINMMR8[0] = 1	PINMMR8[0] = 0 and PINMMR8[1] = 1
eQEPB	PINMMR8[8] = 1	PINMMR8[8] = 0 and PINMMR8[9] = 1
eQEPI	PINMMR8[16] = 1	PINMMR8[16] = 0 and PINMMR8[17] = 1
eQEPS	PINMMR8[24] = 1	PINMMR8[24] = 0 and PINMMR8[25] = 1

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7.8.4 Enhanced Quadrature Encoder Pulse (eQEPx) Timing

表 7-18. eQEPx Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{w(QEPP)}$	QEP input period	Synchronous	2 $t_{c(VCLK)}$		cycles
		Synchronous, with input filter	2 $t_{c(VCLK)}$ + filter width		cycles
$t_{w(INDEXH)}$	QEP Index Input High Time	Synchronous	2 $t_{c(VCLK)}$		cycles
		Synchronous, with input filter	2 $t_{c(VCLK)}$ + filter width		cycles
$t_{w(INDEXL)}$	QEP Index Input Low Time	Synchronous	2 $t_{c(VCLK)}$		cycles
		Synchronous, with input filter	2 $t_{c(VCLK)}$ + filter width		cycles
$t_{w(STROBH)}$	QEP Strobe Input High Time	Synchronous	2 $t_{c(VCLK)}$		cycles
		Synchronous, with input filter	2 $t_{c(VCLK)}$ + filter width		cycles
$t_{w(STROBL)}$	QEP Strobe Input Low Time	Synchronous	2 $t_{c(VCLK)}$		cycles
		Synchronous, with input filter	2 $t_{c(VCLK)}$ + filter width		cycles

表 7-19. eQEPx Switching Characteristics

PARAMETER		MIN	MAX	UNIT
$t_{d(CNTR)xin}$	Delay time, external clock to counter increment		4 $t_{c(VCLK)}$	cycles
$t_{d(PCS-OUT)QEP}$	Delay time, QEP input edge to position compare sync output		6 $t_{c(VCLK)}$	cycles

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8 デバイスおよびドキュメントのサポート

8.1 デバイス・サポート

8.1.1 開発サポート

テキサス・インスツルメンツ(TI)は、Hercules™ Safety世代のMCU用に広範な開発ツールを提供しており、プロセッサの性能評価、コードの生成、アルゴリズム実装の開発、ソフトウェアおよびハードウェア・モジュールの完全な統合とデバッグなどの用途に利用できます。

以下の製品は、Hercules™ベースのアプリケーション開発をサポートしています。

ソフトウェア開発ツール

- Code Composer Studio™統合開発環境(IDE)
  - C/C++コンパイラ
  - コード生成ツール
  - アセンブラ/リンカ
  - サイクル精度シミュレータ
- アプリケーションのアルゴリズム
- アプリケーションのサンプル・コード

ハードウェア開発ツール

- 開発および評価ボード
- JTAGベースのエミュレータ - XDS100™v2、XDS200、XDS560™v2エミュレータ
- フラッシュ・プログラミング・ツール
- 電源
- ドキュメントとケーブル

8.1.1.1 はじめに

このセクションでは、TMS570 MCUデバイス用の開発を最初に行うときの手順について、概要を簡単に説明します。各手順の詳細については、次の資料を参照してください。

- 『*TMS570LS043x、TMS570LS033x、RM42L432 Hercules ARM Cortex-R4マイクロコントローラの初期化*』(SPNA163)
- 『*互換性の考慮点: TMS570LS31x/21xまたはTMS570LS12x/11xからTMS570LS04x/03x Safetyマイクロコントローラへの移行*』(SPNA175)

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8.1.2 デバイスの項目表記

製品開発サイクルの段階を示すために、TIではデバイスのすべての型番に接頭辞が割り当てられています。商用ファミリの各製品には、TMX、TMP、XMSのいずれかの接頭辞があります。これらの接頭辞は、製品開発の進展段階を表します。段階には、エンジニアリング・プロトタイプ(TMX)から、完全認定済みの量産デバイス(TMS)までがあります。

デバイス開発の段階は次のとおりです。

TMX 実験的デバイス。最終デバイスの電気的特性を必ずしも表しません。

TMP 最終シリコン・ダイ。デバイスの電気的特性に適合しますが、品質および信頼性の検証は完了していません。

TMS 認定済み製品デバイス。

TMXおよびTMPデバイスは、以下の免責事項付きで出荷されます。

「開発中の製品は、社内での評価用です。」

TMSデバイスの特性は完全に明確化されており、デバイスの品質と信頼性が十分に示されています。TIの標準保証が適用されます。

プロトタイプ・デバイス(TMXまたはTMP)の方が標準的な製品版デバイスに比べて故障率が大きいと予測されます。これらのデバイスは予測される最終使用時の故障率が未定義であるため、テキサス・インスツルメンツではそれらのデバイスを量産システムで使用しないよう推奨しています。正規の製品版デバイスのみを使用する必要があります。

図 8-1は、TMS570LS0432/0332の番号と記号の表記規則を表しています。

Full Part #	TMS	570	LS	04	3	2	B	PZ	Q	Q1	R
Orderable Part #	TMS	570		04	3	2	B	PZ	Q	Q1	R

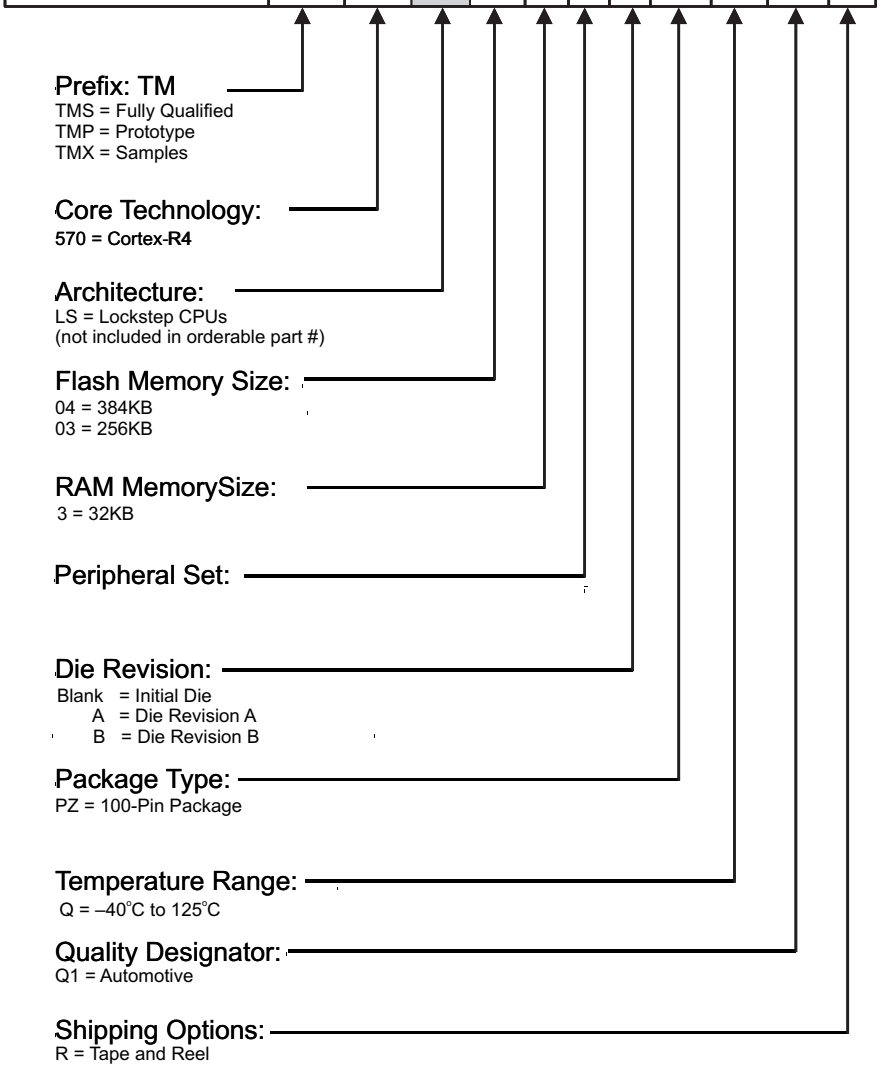

図 8-1. デバイスの番号付け規則

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8.2 ドキュメントのサポート

8.2.1 テキサス・インスツルメンツの関連資料

次のドキュメントには、*TMS570LS0432/0332*マイクロコントローラについて記載されています。

SPNU517 *『TMS570LS04x/03x 16/32ビットRISCフラッシュ・マイクロコントローラ テクニカル・リファレンス・マニュアル』*には、デバイスの各ペリフェラルとサブシステムの統合、環境、機能説明、プログラミング・モデルが詳しく記載されています。

SPNZ197 *『TMS570LS0x32マイクロコントローラのシリコン・リビジョンA、シリコン正誤表』*には、デバイスのシリコン・リビジョンについての使用上の注記と、機能仕様に対する既知の例外事項が記載されています。

SPNZ226 *『TMS570LS0x32マイクロコントローラのシリコン・リビジョンB、シリコン正誤表』*には、デバイスのシリコン・リビジョンについての使用上の注記と、機能仕様に対する既知の例外事項が記載されています。

SPNA207 *『Hercules™ Safety MCUの等価パワーオン時間の計算』*には、テキサス・インスツルメンツ製のHercules Safety MCUの温度が経年劣化に及ぼす影響を、スプレッドシートで計算する方法が詳しく説明されています。

8.3 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 8-1. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
TMS570LS0432	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TMS570LS0332	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

8.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community The TI engineer-to-engineer (E2E) community was created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

TI Embedded Processors Wiki Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

8.5 商標

Hercules, Code Composer Studio, XDS100, XDS560, E2E are trademarks of Texas Instruments.
CoreSight is a trademark of ARM Limited.
ARM, Cortex are registered trademarks of ARM Limited (or its subsidiaries) in the EU and/or elsewhere.
All rights reserved.
All other trademarks are the property of their respective owners.

8.6 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

8.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

8.8 デバイス識別コード・レジスタ

アドレス0xFFFFFFF0のデバイス識別コード・レジスタは、デバイスについてシリコン・バージョンなど、いくつかの要素を識別します。デバイス識別コード・レジスタの詳細を、表 8-2に示します。このデバイスのデバイス識別コード・レジスタは次のとおりです。

- Rev 0 = 0x8048AD05
- Rev A = 0x8048AD0D
- Rev B = 0x8048AD15

図 8-2. デバイスIDビット割り当てレジスタ

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CP-15	固有ID														TECH
R-1	R-00000000100100														R-0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
テクノロジ			I/O 電圧	周辺機器パリティ	フラッシュECC		RAM ECC	バージョン					1	0	1
R-101			R-0	R-1	R-10		R-1	R-00001					R-1	R-0	R-1

凡例: R/W = 読み出し/書き込み、R = 読み出し専用、*-n* = リセット後の値

表 8-2. デバイスIDビット割り当てレジスタのフィールドの説明

ビット	フィールド	値	説明
31	CP15		コプロセッサ15の存在を示します。
		1	CP15が存在
30-17	固有ID	100100	シリコン・バージョン(リビジョン)ビット。
			このビット・フィールドは、専用デバイス構成(ダイ)に固有の番号を示しています。
16-13	テクノロジ		デバイスの製造に使用されたプロセス・テクノロジ。
		0101	F021
12	I/O電圧		デバイスのI/O電圧
		0	I/Oは3.3V
11	周辺機器パリティ		周辺機器パリティ
		1	周辺機器のメモリのパリティ
10-9	フラッシュECC		フラッシュECC
		10	ECC付きのプログラム・メモリ
8	RAM ECC		RAMメモリにECCが存在するかどうかを示します。
		1	ECCが実装されています。
7-3	リビジョン	0	デバイスのリビジョン。
2-0	ファミリID	101	プラットフォーム・ファミリIDは常に0b101です。

8.9 ダイ識別レジスタ

アドレス0xFFFFFF7Cおよび0xFFFFFF80にある2つのダイIDレジスタは64ビットのダイIDを形成し、表 8-3のような情報を示します。

表 8-3. ダイIDレジスタ

項目	ビット数	ビット位置
ウェハ上のX座標	12	0xFFFFFF7C[11:0]
ウェハ上のY座標	12	0xFFFFFF7C[23:12]
ウェハ番号	8	0xFFFFFF7C[31:24]
ロット番号	24	0xFFFFFF80[23:0]
予約	8	0xFFFFFF80[31:24]

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8.10 モジュール認定

次の通信モジュールは、標準に準拠していることが認定済みです。

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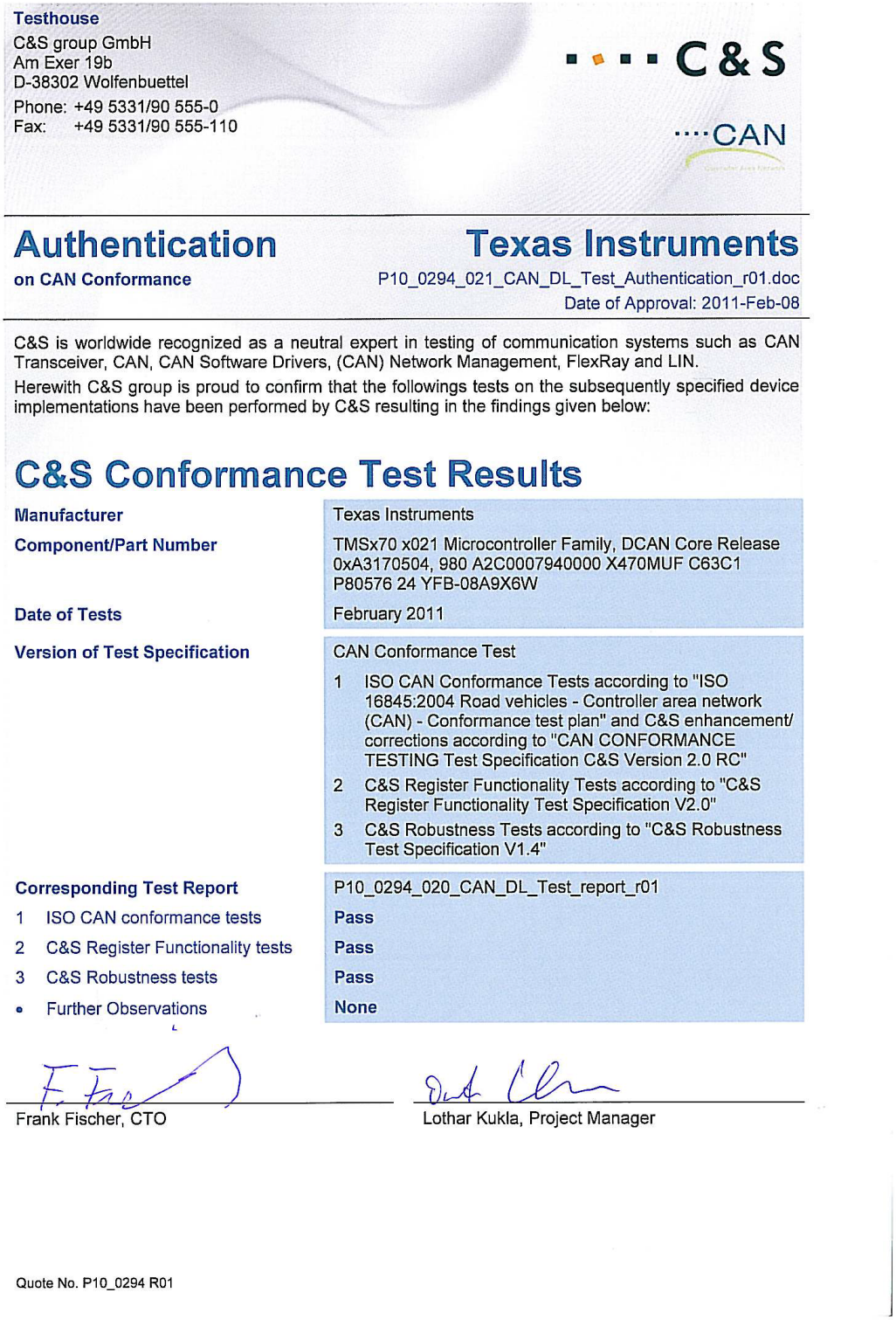
8.10.1 DCAN認定



Testhouse
C&S group GmbH
Am Exer 19b
D-38302 Wolfenbuettel
Phone: +49 5331/90 555-0
Fax: +49 5331/90 555-110

C&S
CAN

Authentication
on CAN Conformance

Texas Instruments
P10_0294_021_CAN_DL_Test_Authentication_r01.doc
Date of Approval: 2011-Feb-08

C&S is worldwide recognized as a neutral expert in testing of communication systems such as CAN Transceiver, CAN, CAN Software Drivers, (CAN) Network Management, FlexRay and LIN.

Herewith C&S group is proud to confirm that the followings tests on the subsequently specified device implementations have been performed by C&S resulting in the findings given below:

C&S Conformance Test Results

Manufacturer	Texas Instruments
Component/Part Number	TMSx70 x021 Microcontroller Family, DCAN Core Release 0xA3170504, 980 A2C0007940000 X470MUF C63C1 P80576 24 YFB-08A9X6W
Date of Tests	February 2011
Version of Test Specification	CAN Conformance Test 1 ISO CAN Conformance Tests according to "ISO 16845:2004 Road vehicles - Controller area network (CAN) - Conformance test plan" and C&S enhancement/ corrections according to "CAN CONFORMANCE TESTING Test Specification C&S Version 2.0 RC" 2 C&S Register Functionality Tests according to "C&S Register Functionality Test Specification V2.0" 3 C&S Robustness Tests according to "C&S Robustness Test Specification V1.4"
Corresponding Test Report	P10_0294_020_CAN_DL_Test_report_r01
1 ISO CAN conformance tests	**Pass**
2 C&S Register Functionality tests	**Pass**
3 C&S Robustness tests	**Pass**
• Further Observations	**None**

Frank Fischer, CTO

Lothar Kukla, Project Manager

Quote No. P10_0294 R01

図 8-3. DCAN認定

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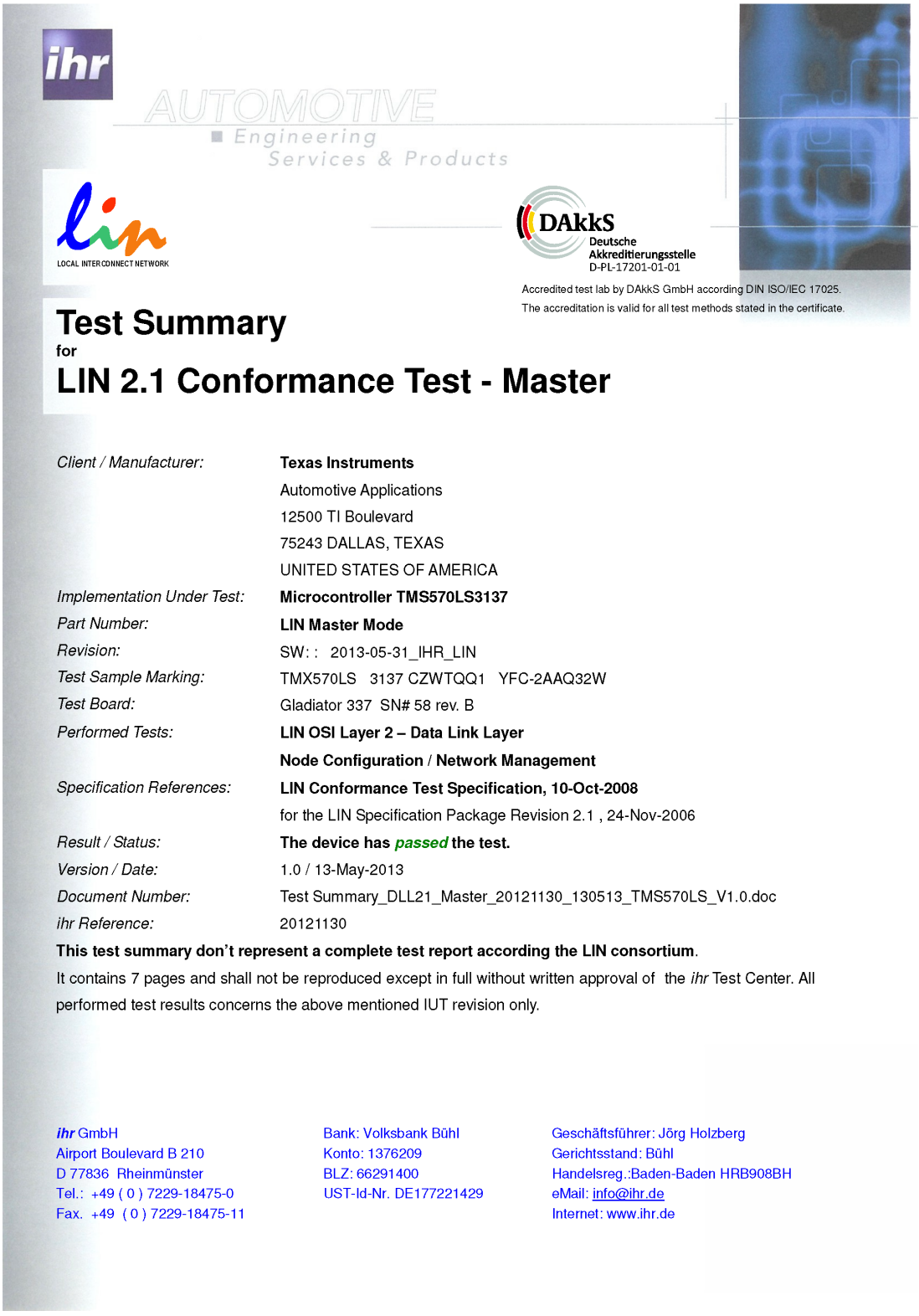
8.10.2 LIN認定

8.10.2.1 LINマスタ・モード



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DAkkS
Deutsche
Akkreditierungsstelle
D-PL-17201-01-01

Accredited test lab by DAkkS GmbH according DIN ISO/IEC 17025.
The accreditation is valid for all test methods stated in the certificate.

Test Summary
for
LIN 2.1 Conformance Test - Master

Client / Manufacturer:	**Texas Instruments**
	Automotive Applications
	12500 TI Boulevard
	75243 DALLAS, TEXAS
	UNITED STATES OF AMERICA
Implementation Under Test:	**Microcontroller TMS570LS3137**
Part Number:	**LIN Master Mode**
Revision:	SW: : 2013-05-31_IHR_LIN
Test Sample Marking:	TMX570LS 3137 CZWTQQ1 YFC-2AAQ32W
Test Board:	Gladiator 337 SN# 58 rev. B
Performed Tests:	**LIN OSI Layer 2 – Data Link Layer**
	Node Configuration / Network Management
Specification References:	**LIN Conformance Test Specification, 10-Oct-2008**
	for the LIN Specification Package Revision 2.1 , 24-Nov-2006
Result / Status:	**The device has *passed* the test.**
Version / Date:	1.0 / 13-May-2013
Document Number:	Test Summary_DLL21_Master_20121130_130513_TMS570LS_V1.0.doc
ihr Reference:	20121130

This test summary don't represent a complete test report according the LIN consortium.
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eMail: info@ihr.de
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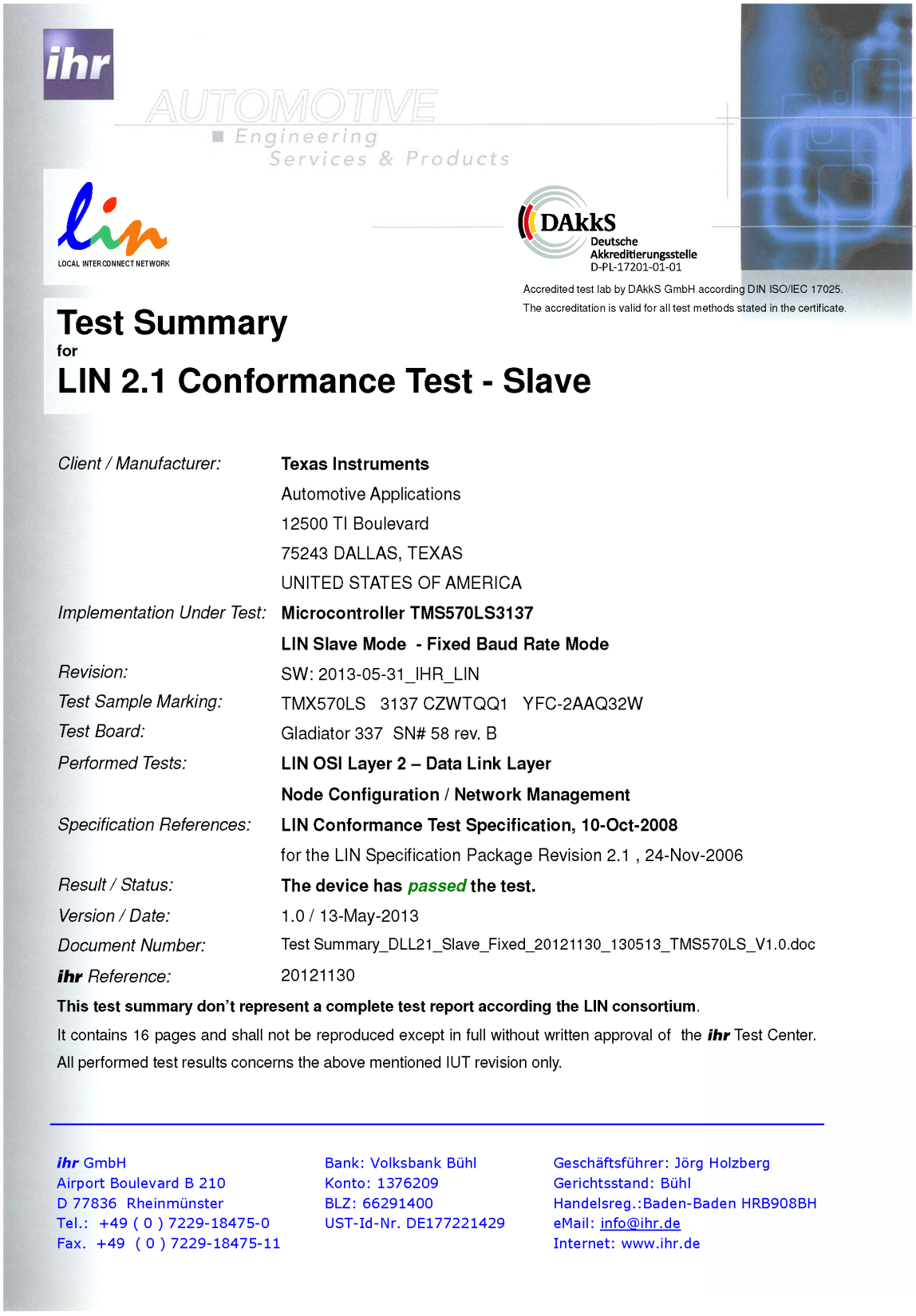
図 8-4. LIN認定 - マスタ・モード

8.10.2.2 LINスレーブ・モード - 固定ボーレート



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Test Summary
for
LIN 2.1 Conformance Test - Slave

Client / Manufacturer:	**Texas Instruments**
	Automotive Applications
	12500 TI Boulevard
	75243 DALLAS, TEXAS
	UNITED STATES OF AMERICA
Implementation Under Test:	**Microcontroller TMS570LS3137**
	LIN Slave Mode - Fixed Baud Rate Mode
Revision:	SW: 2013-05-31_IHR_LIN
Test Sample Marking:	TMX570LS 3137 CZWTQQ1 YFC-2AAQ32W
Test Board:	Gladiator 337 SN# 58 rev. B
Performed Tests:	**LIN OSI Layer 2 – Data Link Layer**
	Node Configuration / Network Management
Specification References:	**LIN Conformance Test Specification, 10-Oct-2008**
	for the LIN Specification Package Revision 2.1 , 24-Nov-2006
Result / Status:	**The device has *passed* the test.**
Version / Date:	1.0 / 13-May-2013
Document Number:	Test Summary_DLL21_Slave_Fixed_20121130_130513_TMS570LS_V1.0.doc
***ihr** Reference:*	20121130

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図 8-5. LIN認定 - スレーブ・モード - 固定ボーレート

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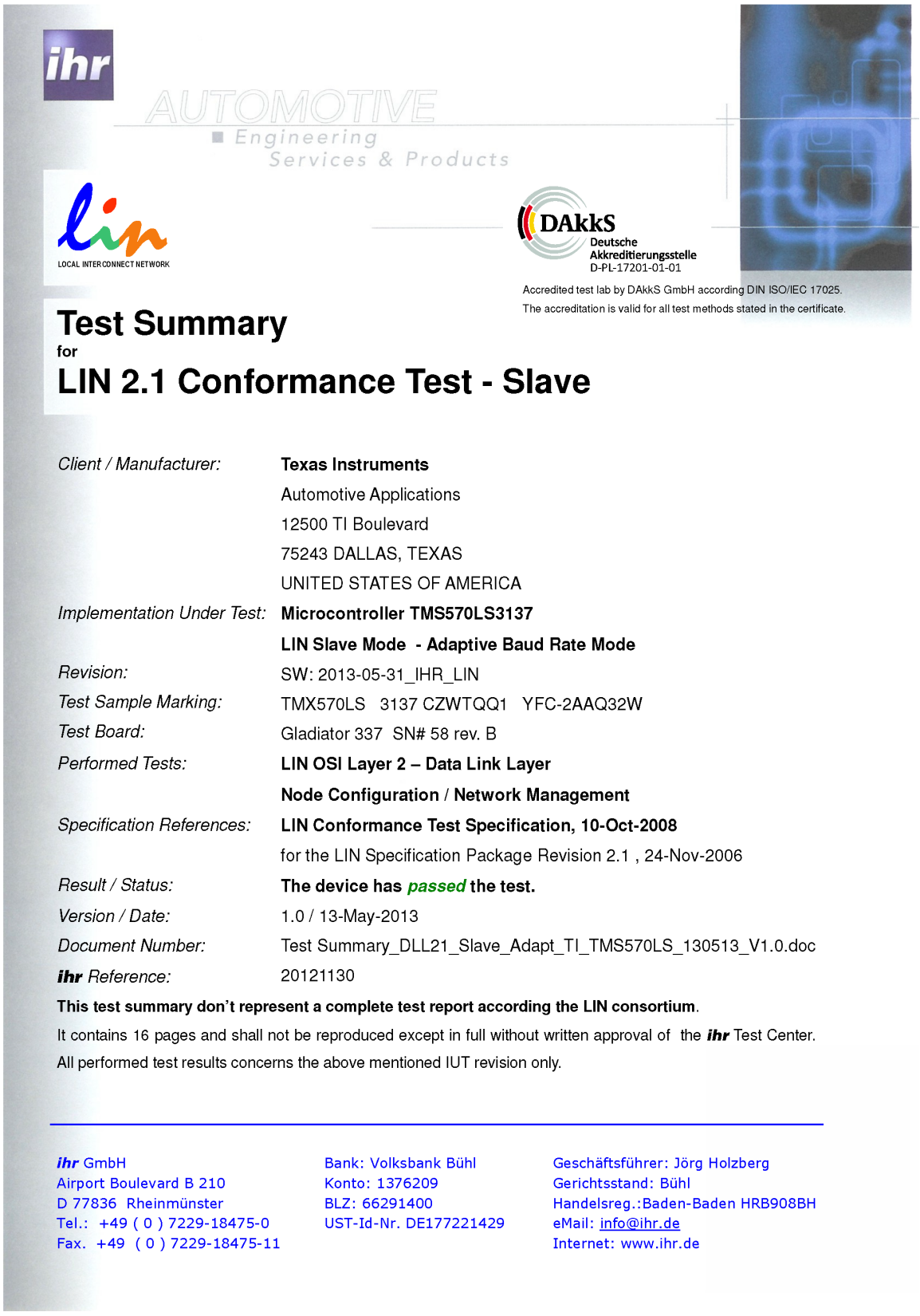
8.10.2.3 LINスレーブ・モード - 適応型ボーレート



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The accreditation is valid for all test methods stated in the certificate.

Test Summary
for
LIN 2.1 Conformance Test - Slave

Client / Manufacturer:	**Texas Instruments**
	Automotive Applications
	12500 TI Boulevard
	75243 DALLAS, TEXAS
	UNITED STATES OF AMERICA
Implementation Under Test:	**Microcontroller TMS570LS3137**
	LIN Slave Mode - Adaptive Baud Rate Mode
Revision:	SW: 2013-05-31_IHR_LIN
Test Sample Marking:	TMX570LS 3137 CZWTQQ1 YFC-2AAQ32W
Test Board:	Gladiator 337 SN# 58 rev. B
Performed Tests:	**LIN OSI Layer 2 – Data Link Layer**
	Node Configuration / Network Management
Specification References:	**LIN Conformance Test Specification, 10-Oct-2008**
	for the LIN Specification Package Revision 2.1 , 24-Nov-2006
Result / Status:	**The device has *passed* the test.**
Version / Date:	1.0 / 13-May-2013
Document Number:	Test Summary_DLL21_Slave_Adapt_TI_TMS570LS_130513_V1.0.doc
***ihr** Reference:*	20121130

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図 8-6. LIN認定 - スレーブ・モード - 適応型ボーレート

9 メカニカル、パッケージ、および注文に関する付録

9.1 パッケージ情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMS5700332BPZQQ1	Active	Production	LQFP (PZ) | 100	90 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TMS570LS 0332BPZQQ1
TMS5700332BPZQQ1.B	Active	Production	LQFP (PZ) | 100	90 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TMS570LS 0332BPZQQ1
TMS5700432BPZQQ1	Active	Production	LQFP (PZ) | 100	90 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TMS570LS 0432BPZQQ1
TMS5700432BPZQQ1.B	Active	Production	LQFP (PZ) | 100	90 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TMS570LS 0432BPZQQ1
TMS5700432BPZQQ1R	Active	Production	LQFP (PZ) | 100	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TMS570LS 0432BPZQQ1
TMS5700432BPZQQ1R.B	Active	Production	LQFP (PZ) | 100	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TMS570LS 0432BPZQQ1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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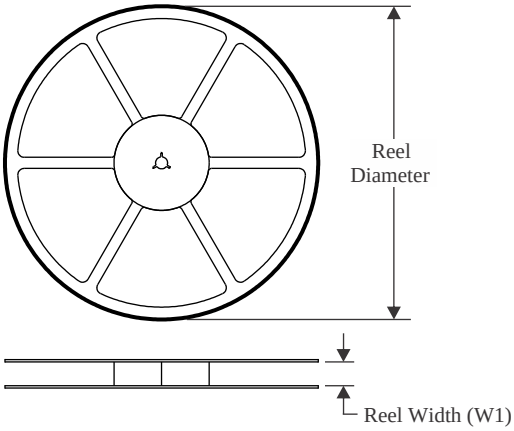
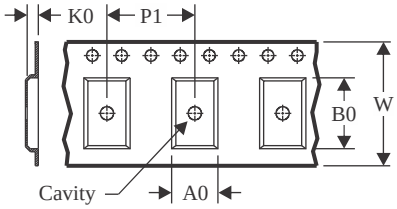
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

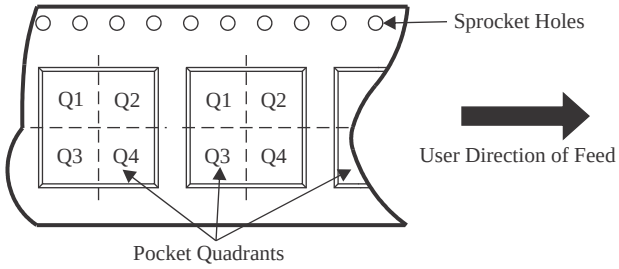


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

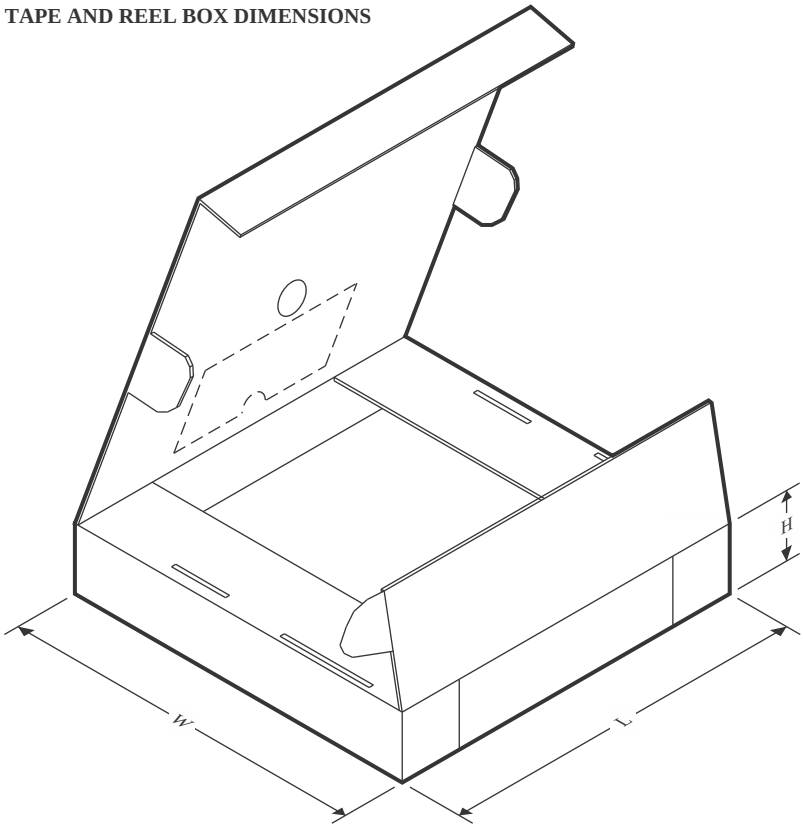
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMS5700432BPZQQ1R	LQFP	PZ	100	1000	330.0	32.4	16.9	16.9	2.0	24.0	32.0	Q2

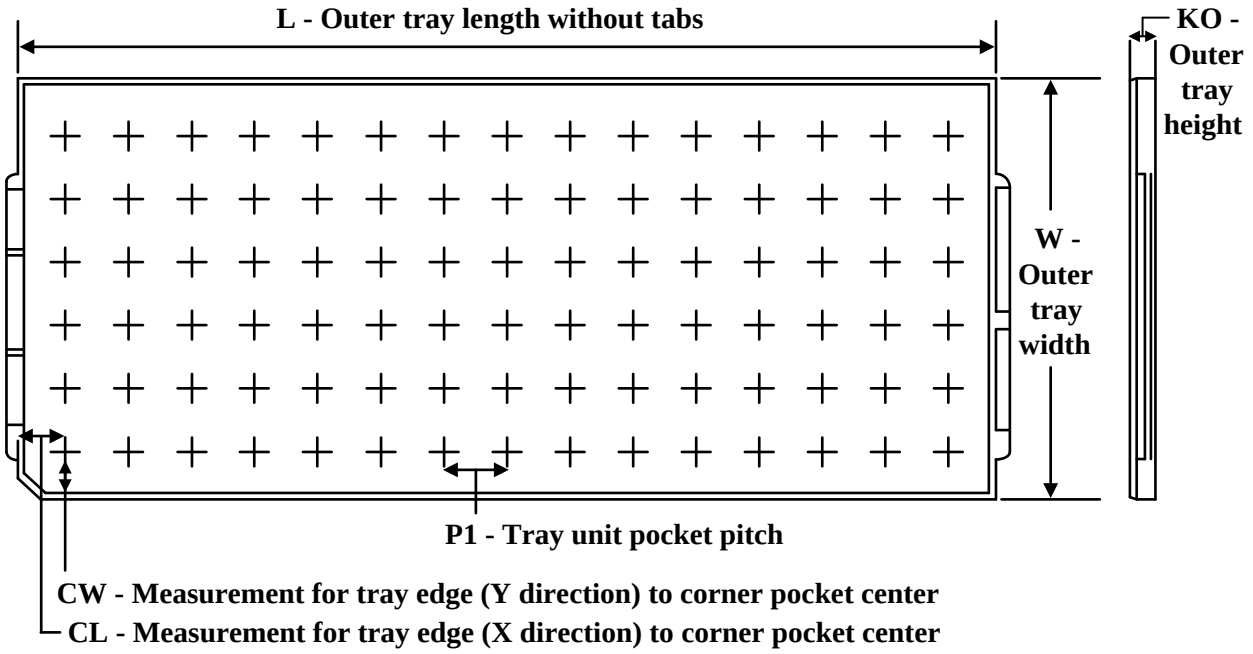
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMS5700432BPZQQ1R	LQFP	PZ	100	1000	367.0	367.0	55.0

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

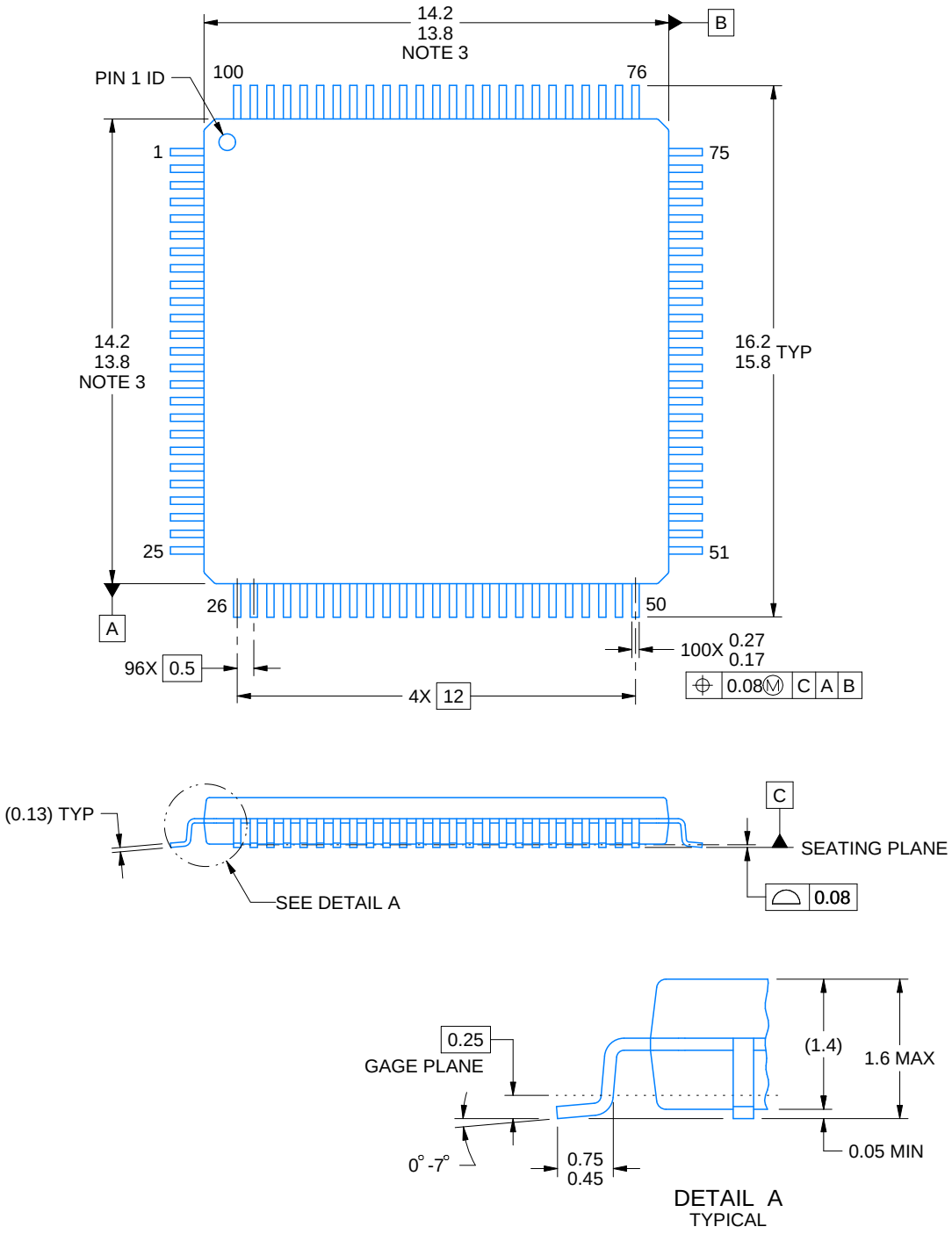
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
TMS5700332BPZQQ1	PZ	LQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.4
TMS5700332BPZQQ1.B	PZ	LQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.4
TMS5700432BPZQQ1	PZ	LQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.4
TMS5700432BPZQQ1.B	PZ	LQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.4

PACKAGE OUTLINE

PZ0100A

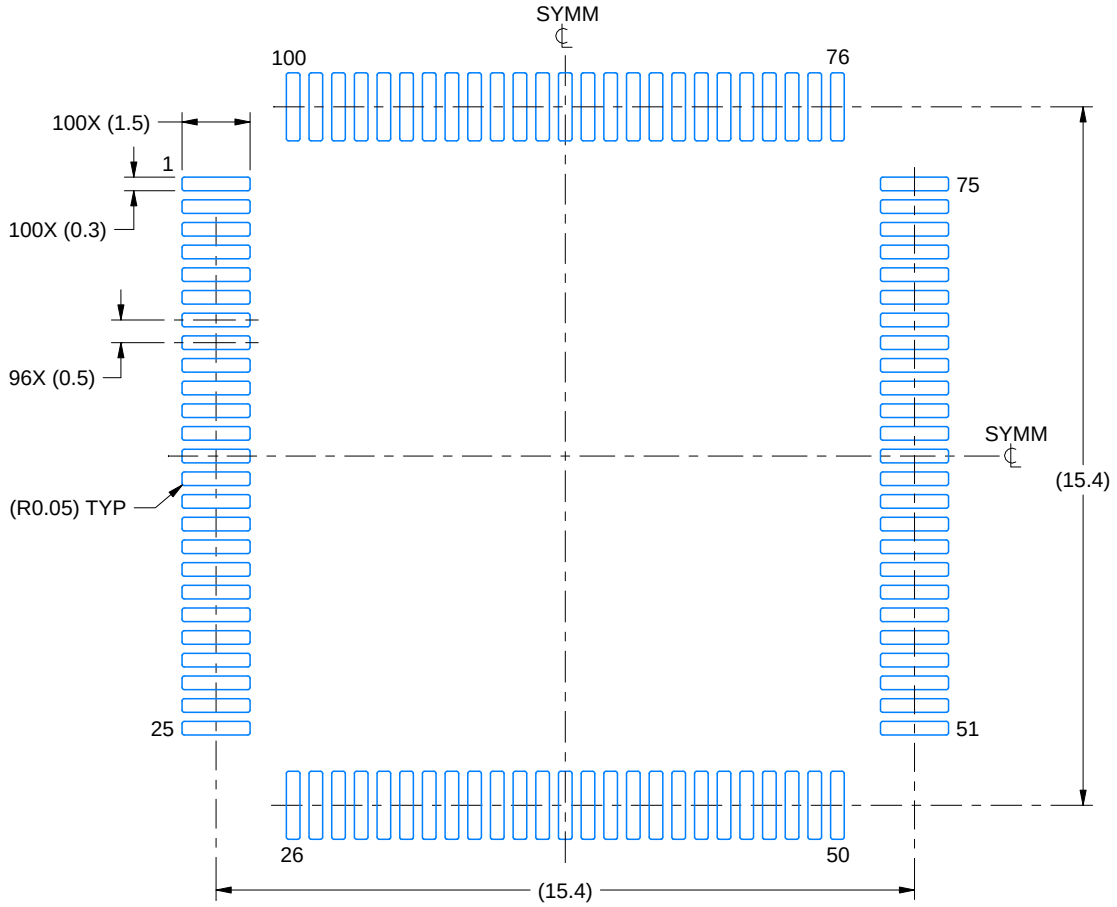
LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK

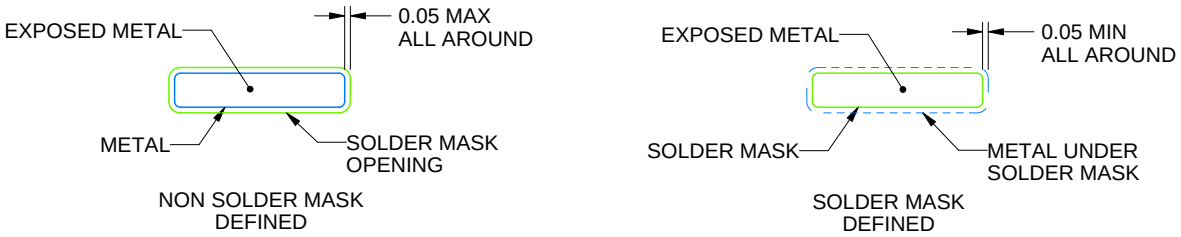


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



SOLDER MASK DETAILS

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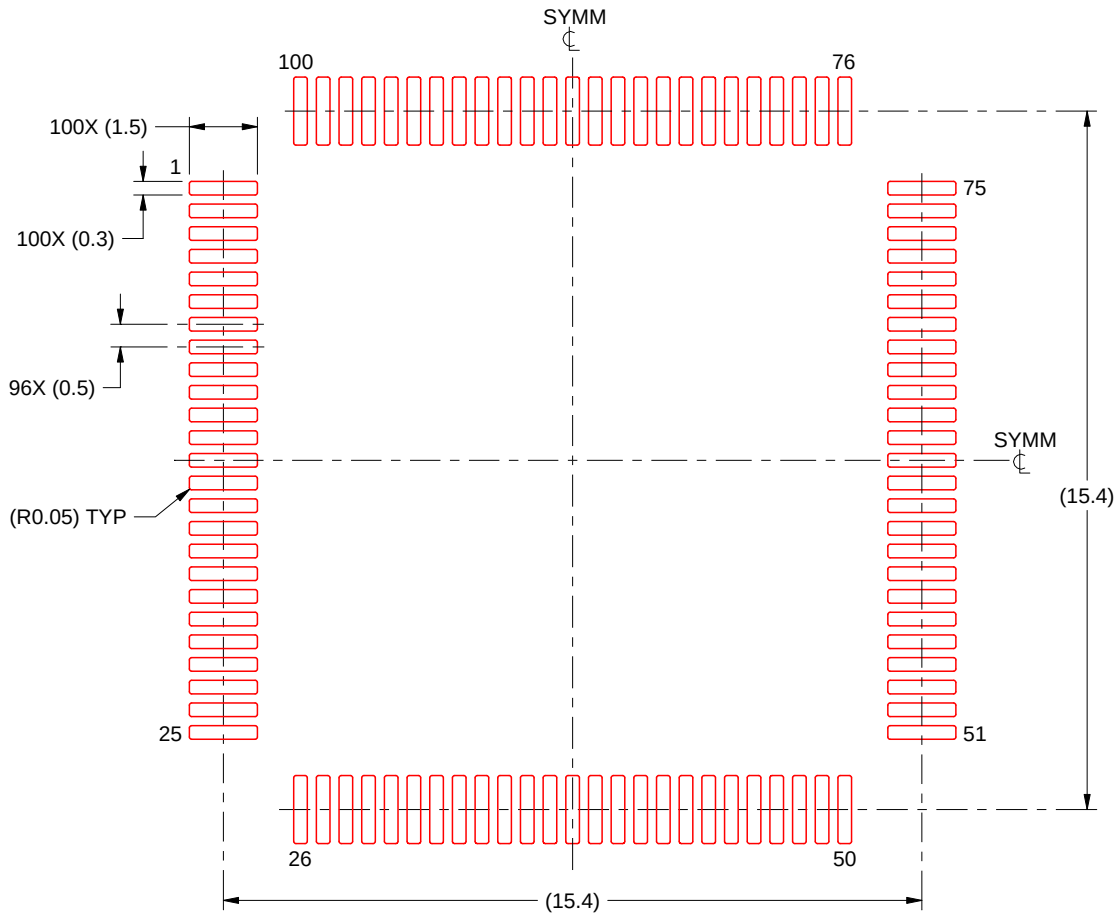
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月