TMP75B 1.8-V Digital Temperature Sensor with Two-Wire Interface and Alert

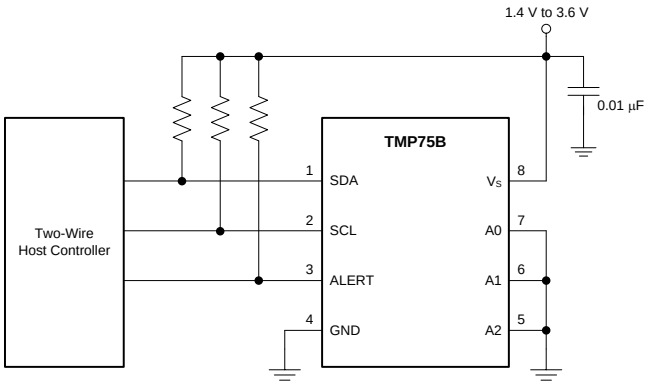
1 Features

- Low-Voltage Alternative to LM75 and TMP75
- Digital Output with Standard Two-Wire Serial Interface
- Up to 8 Pin-Programmable Bus Addresses
- Overtemperature ALERT Pin with Programmable Trip Values
- Shutdown Mode for Battery Power Saving
- One-Shot Conversion Mode for Custom Update Rates
- Operating Temperature Range: –55°C to +125°C
- Operating Supply Range: 1.4 V to 3.6 V
- Quiescent Current:
  - 45 µA Active (typ)
  - 0.3 µA Shutdown (typ)
- Accuracy:
  - ±0.5°C (typ) from –20°C to +85°C
  - ±1°C (typ) from –55°C to +125°C
- Resolution: 12 Bits (0.0625°C)
- Packages: SOIC-8 and VSSOP-8

2 Applications

- Server and Computer Thermal Management
- Telecommunication Equipment
- Office Machines
- Video Game Consoles
- Set-Top Boxes
- Power Supply and Battery Thermal Protection
- Thermostat Control
- Environmental Monitoring and HVAC
- Electrical Motor Driver Thermal Protection

Simplified Schematic



3 Description

The TMP75B is an integrated digital temperature sensor with a 12-bit analog-to-digital converter (ADC) that can operate at a 1.8-V supply, and is pin and register compatible with the industry-standard LM75 and TMP75. This device is available in SOIC-8 and VSSOP-8 packages, and requires no external components to sense the temperature. The TMP75B is capable of reading temperatures with a resolution of 0.0625°C and is specified over a temperature range of –55°C to +125°C.

The TMP75B features SMBus and two-wire interface compatibility, and allows up to eight devices on the same bus with the SMBus overtemperature alert function. The programmable temperature limits and the ALERT pin allow the sensor to operate as a stand-alone thermostat, or an overtemperature alarm for power throttling or system shutdown.

The factory-calibrated temperature accuracy and the noise-immune digital interface make the TMP75B the preferred solution for temperature compensation of other sensors and electronic components, without the need for additional system-level calibration or elaborate board layout for distributed temperature sensing.

The TMP75B is ideal for thermal management and protection of a variety of consumer, computer, communication, industrial, and environmental applications.

Device Information[1]

DEVICE NAME	PACKAGE	BODY SIZE (NOM)
TMP75B	SOIC (8)	4.90 mm × 3.90 mm
	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the package option addendum at the end of the datasheet.

Temperature Accuracy (Error) vs Ambient Temperature

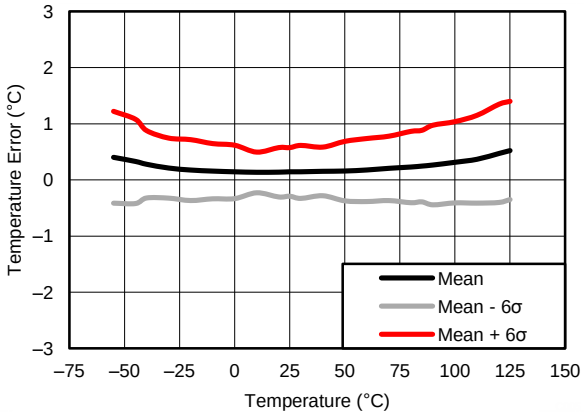


Table of Contents

4 Revision History

Changes from Revision A (April 2014) to Revision B **Page**

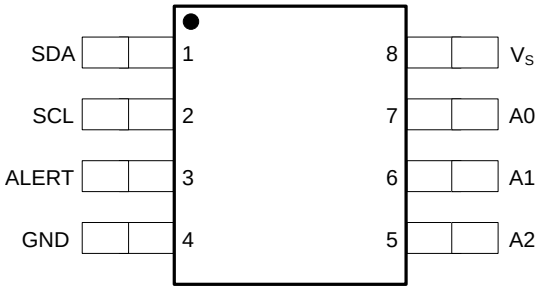
- Added DGK (VSSOP-8) package to data sheet ... 1

Changes from Original (April 2014) to Revision A **Page**

- Changed from product preview to production data ... 1

5 Pin Configuration and Functions

D and DGK Packages
SOIC-8 and VSSOP-8
(Top View)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A0	7	I	Address select. Connect to GND or V_S.
A1	6	I	Address select. Connect to GND or V_S.
A2	5	I	Address select. Connect to GND or V_S.
ALERT	3	O	Overtemperature alert. Open-drain output; requires a pull-up resistor.
GND	4	—	Ground.
SCL	2	I	Serial clock.
SDA	1	I/O	Serial data. Open-drain output; requires a pull-up resistor.
V_S	8	I	Supply voltage, 1.4 V to 3.6 V.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage, V_S			4	V
Input voltage	SDA, SCL, ALERT, A2, A1	-0.3	4	V
	A0	-0.3	(V_S) + 0.3	V
Sink current	SDA, ALERT		10	mA
Operating junction temperature		-55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		-60	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	–2000	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	–1000	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage	1.4	1.8	3.6	V
Operating free-air temperature, T_A	-55		125	°C

6.4 Thermal Information

THERMAL METRIC (1)		TMP75B		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	125.4	188.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	71.5	79.1	
$R_{\theta JB}$	Junction-to-board thermal resistance	65.8	109.6	
ψ_{JT}	Junction-to-top characterization parameter	21.1	15.3	
ψ_{JB}	Junction-to-board characterization parameter	65.3	108	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

At T_A = –55°C to +125°C and V_S = +1.4 V to +3.6 V, unless otherwise noted. Typical values at T_A = 25°C and V_S = +1.8 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE INPUT						
	Temperature range		–55		+125	°C
	Temperature resolution			0.0625		°C
	Temperature accuracy (error)	–20°C to +85°C		±0.5	±2	°C
		–55°C to +125°C		±1	±3	°C
DIGITAL INPUT/OUTPUT						
V_{IH}	High-level input voltage		0.7(V_S)		V_S	V
V_{IL}	Low-level input voltage		-0.3		0.3(V_S)	V
I_{IN}	Input current	0 V < V_{IN} < (V_S) + 0.3 V			1	µA
V_{OL}	Low-level output voltage	V_S ≥ 2 V, I_{OUT} = 3 mA			0.4	V
		V_S < 2 V, I_{OUT} = 3 mA			0.2(V_S)	V
	ADC resolution			12		Bit
	Conversion time	One-shot mode	20	27	35	ms
	Conversion modes	CR1 = 0, CR0 = 0 (default)		37		Conv/s
		CR1 = 0, CR0 = 1		18		Conv/s
		CR1 = 1, CR0 = 0		9		Conv/s
		CR1 = 1, CR0 = 1		4		Conv/s
	Timeout time		38	54	70	ms
POWER SUPPLY						
	Operating supply range		1.4		3.6	V
I_Q	Quiescent current	Serial bus inactive, CR1 = 0, CR0 = 0 (default)		45	89	µA
		Serial bus inactive, CR1 = 0, CR0 = 1		22	48	µA
		Serial bus inactive, CR1 = 1, CR0 = 0		12	30	µA
		Serial bus inactive, CR1 = 1, CR0 = 1		6.5	21	µA
I_{SD}	Shutdown current	Serial bus inactive		0.3	8	µA
		Serial bus active, SCL frequency = 400 kHz		10		µA
		Serial bus active, SCL frequency = 3.4 MHz		80		µA

6.6 Typical Characteristics

At T_A = 25°C and V_S = +1.8 V (unless otherwise noted).

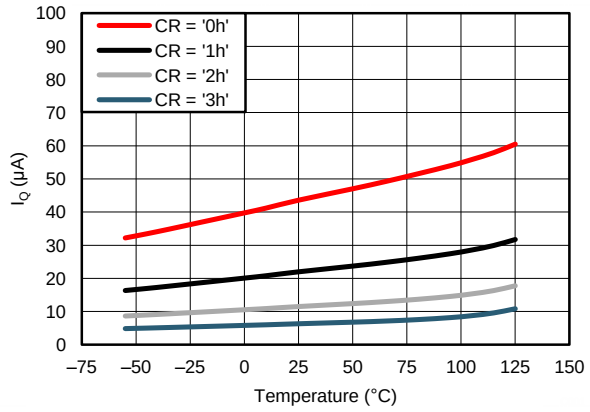


Figure 1. Quiescent Current vs Temperature

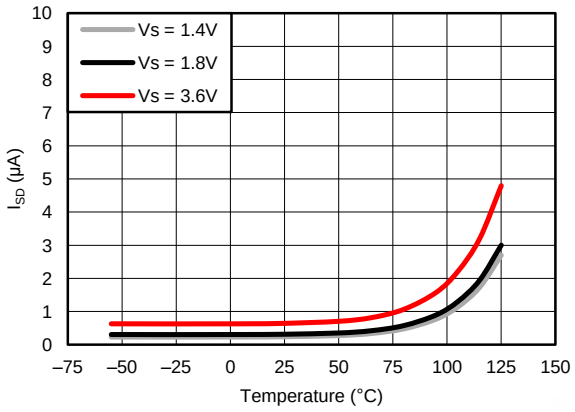


Figure 2. Shutdown Current vs Temperature

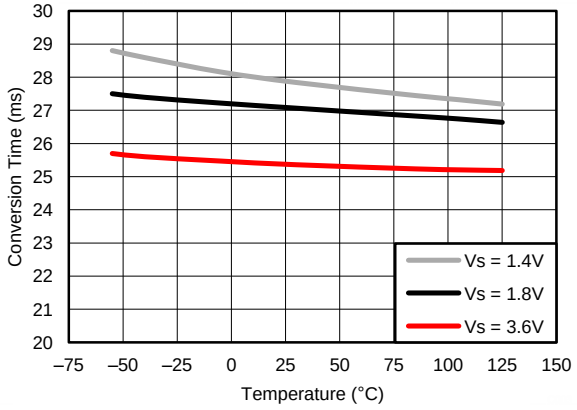


Figure 3. Conversion Time vs Temperature

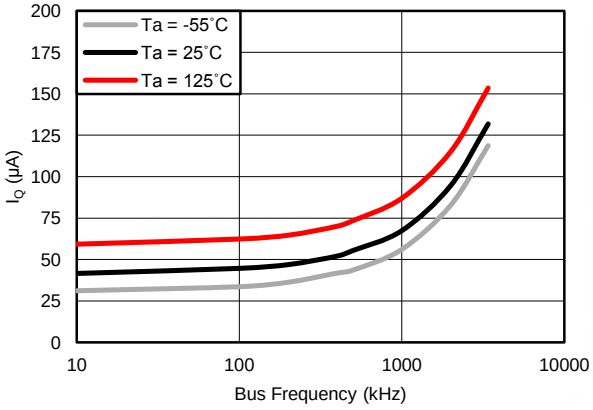


Figure 4. Quiescent Current vs Bus Frequency

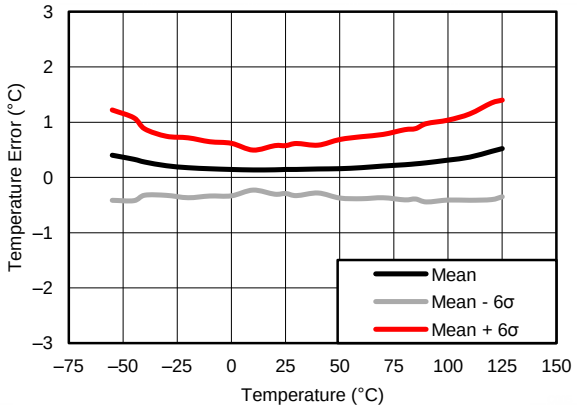


Figure 5. Temperature Error vs Temperature

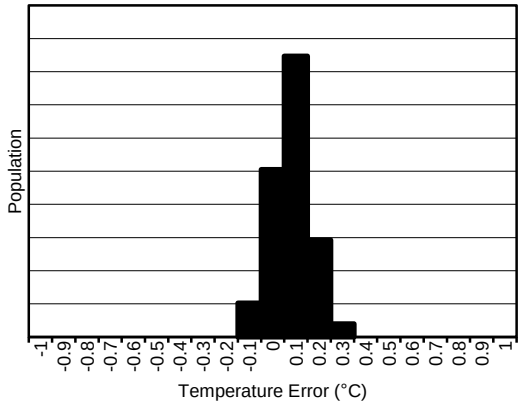


Figure 6. Temperature Error at 25°C

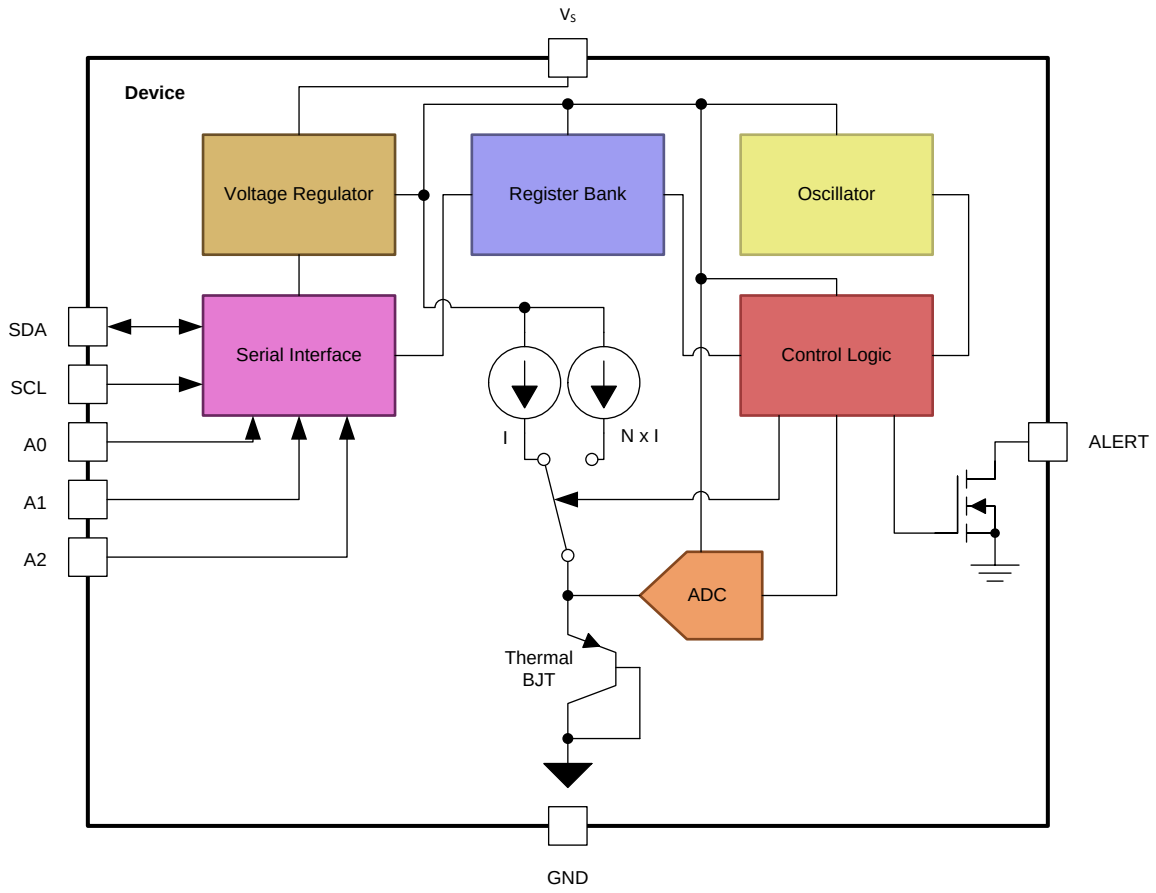
7 Detailed Description

7.1 Overview

The TMP75B is a digital temperature sensor optimal for thermal management and thermal protection applications. The TMP75B is two-wire and SMBus interface compatible, and is specified over a temperature range of –55°C to +125°C.

The temperature sensing device for the TMP75B is the chip itself. A bipolar junction transistor (BJT) inside the chip is used in a band-gap configuration to produce a voltage proportional to the chip temperature. The voltage is digitized and converted to a 12-bit temperature result in degrees Celsius, with a resolution of 0.0625°C. The package leads provide the primary thermal path because of the lower thermal resistance of the metal. Thus, the temperature result is equivalent to the local temperature of the printed circuit board (PCB) where the sensor is mounted.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Digital Temperature Output

The 12-bit digital output from each temperature measurement conversion is stored in the read-only temperature register. Two bytes must be read to obtain the data, as shown in Figure 15. Note that byte 1 is the most significant byte, followed by byte 2, the least significant byte. The temperature result is left-justified with the 12 most significant bits used to indicate the temperature. There is no need to read the second byte if resolution below 1°C is not required. Table 1 summarizes the temperature data format. One LSB equals 0.0625°C. Negative numbers are represented in binary twos complement format.

Table 1. Temperature Data Format(1)

TEMPERATURE (°C)	DIGITAL OUTPUT	
	BINARY	HEX
128	0111 1111 1111	7FF
127.9375	0111 1111 1111	7FF
100	0110 0100 0000	640
80	0101 0000 0000	500
75	0100 1011 0000	4B0
50	0011 0010 0000	320
25	0001 1001 0000	190
0.25	0000 0000 0100	004
0	0000 0000 0000	000
–0.25	1111 1111 1100	FFC
–25	1110 0111 0000	E70
–55	1100 1001 0000	C90

(1) The temperature sensor resolution is 0.0625°C/LSB.

Table 1 does not supply a full list of all temperatures. Use the following rules to obtain the digital data format for a given temperature, and vice versa.

To convert positive temperatures to a digital data format:

Divide the temperature by the resolution. Then, convert the result to binary code with a 12-bit, left-justified format, and MSB = 0 to denote a positive sign.

Example: (+50°C) / (0.0625°C / LSB) = 800 = 320h = 0011 0010 0000

To convert a positive digital data format to temperature:

Convert the 12-bit, left-justified binary temperature result, with the MSB = 0 to denote a positive sign, to a decimal number. Then, multiply the decimal number by the resolution to obtain the positive temperature.

Example: 0011 0010 0000 = 320h = 800 × (0.0625°C / LSB) = +50°C

To convert negative temperatures to a digital data format:

Divide the absolute value of the temperature by the resolution, and convert the result to binary code with a 12-bit, left-justified format. Then, generate the twos complement of the result by complementing the binary number and adding one. Denote a negative number with MSB = 1.

Example: (|–25°C|) / (0.0625°C / LSB) = 400 = 190h = 0001 1001 0000

Two's complement format: 1110 0110 1111 + 1 = 1110 0111 0000

To convert a negative digital data format to temperature:

Generate the twos compliment of the 12-bit, left-justified binary number of the temperature result (with MSB = 1, denoting negative temperature result) by complementing the binary number and adding one. This represents the binary number of the absolute value of the temperature. Convert to decimal number and multiply by the resolution to get the absolute temperature, then multiply by –1 for the negative sign.

Example: 1110 0111 0000 has twos compliment of 0001 1001 0000 = 0001 1000 1111 + 1

Convert to temperature: 0001 1001 0000 = 190h = 400; 400 × (0.0625°C / LSB) = 25°C = (|–25°C|); (|–25°C|) × (–1) = –25°C

7.3.2 Temperature Limits and Alert

The temperature limits are stored in the T_{LOW} and T_{HIGH} registers (Table 8 and Table 9) in the same format as the temperature result, and their values are compared to the temperature result on every conversion. The outcome of the comparison drives the behavior of the ALERT pin, which can operate as a comparator output or an interrupt, and is set by the TM bit in the configuration register (Table 7).

In comparator mode (TM = 0, default), the ALERT pin becomes active when the temperature is equal to or exceeds the value in T_{HIGH} (fault conditions) for a consecutive number of conversions as set by the FQ bits of the configuration register. ALERT clears when the temperature falls below T_{LOW} for the same consecutive number of conversions. The difference between the two limits acts as a hysteresis on the comparator output, and a fault counter prevents false alerts as a result of environmental noise.

In interrupt mode (TM = 1), the ALERT pin becomes active when the temperature equals or exceeds the value in T_{HIGH} for a consecutive number of fault conditions. The ALERT pin remains active until a read operation of any register occurs, or the device successfully responds to the SMBus alert response address. The ALERT pin is also cleared if the device is placed in shutdown mode (see Shutdown Mode section for shutdown mode description). After the ALERT pin is cleared, this pin becomes active again only when the temperature falls below T_{LOW} for a consecutive number of fault conditions, and remains active until cleared by a read operation of any register, or a successful response to the SMBus alert response address. After the ALERT pin is cleared, the cycle repeats with the ALERT pin becoming active when the temperature equals or exceeds T_{HIGH}, and so on. The ALERT pin can also be cleared by resetting the device with the general-call reset command. This action also clears the state of the internal registers in the device and the fault counter memory, returning the device to comparator mode (TM = 0).

The active state of the ALERT pin is set by the POL bit in the configuration register. When POL = 0 (default), the ALERT pin is active low. When POL = 1, the ALERT pin is active high. The operation of the ALERT pin in various modes is illustrated in Figure 7.

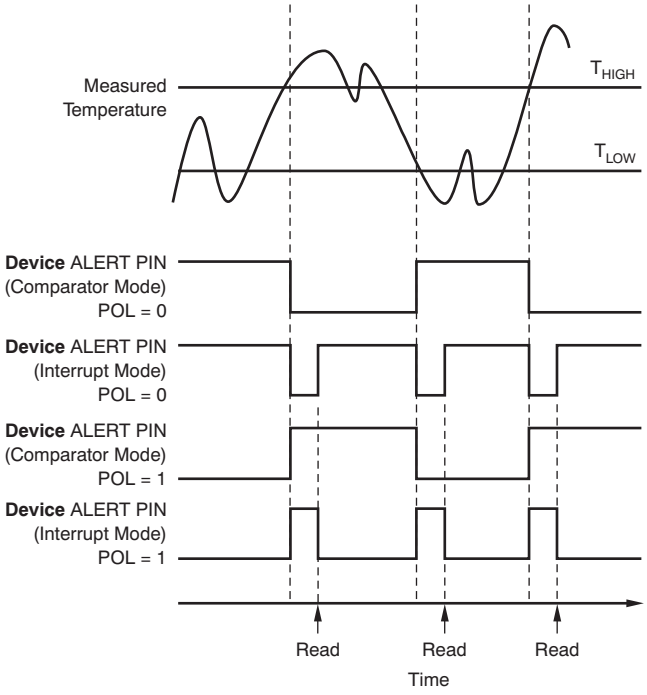


Figure 7. ALERT Pin Modes of Operation

7.3.3 Serial Interface

The TMP75B operates as a slave device only on the two-wire bus and SMBus. Connections to the bus are made using the open-drain I/O lines, SDA and SCL. The SDA and SCL pins feature integrated spike-suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. The TMP75B supports the transmission protocol for both fast (1 kHz to 400 kHz) and high-speed (1 kHz to 3 MHz) modes. All data bytes are transmitted MSB first.

7.3.3.1 Bus Overview

The device that initiates the transfer is called a *master*, and the devices controlled by the master are *slaves*. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the start and stop conditions.

To address a specific device, initiate a start condition by pulling the data line (SDA) from a high to a low logic level while SCL is high. All slaves on the bus shift in the slave address byte; the last bit indicates whether a read or write operation follows. During the ninth clock pulse, the slave being addressed responds to the master by generating an acknowledge bit and pulling SDA low.

Data transfer is then initiated and sent over eight clock pulses followed by an acknowledge bit. During data transfer, SDA must remain stable while SCL is high because any change in SDA while SCL is high is interpreted as a start or stop signal.

After all data have been transferred, the master generates a stop condition indicated by pulling SDA from low to high, while SCL is high.

7.3.3.2 Serial Bus Address

To communicate with the TMP75B, the master must first communicate with slave devices using a slave address byte. The slave address byte consists of seven address bits, and a direction bit indicating the intent of executing either a read or write operation. The TMP75B features three address pins that allow up to eight devices to be addressed on a single bus. The TMP75B latches the status of the address pins at the start of a communication. Table 2 describes the pin logic levels and the corresponding address values.

Table 2. Address Pin Connections and Slave Addresses

DEVICE TWO-WIRE ADDRESS	A2	A1	A0
1001000	GND	GND	GND
1001001	GND	GND	V_S
1001010	GND	V_S	GND
1001011	GND	V_S	V_S
1001100	V_S	GND	GND
1001101	V_S	GND	V_S
1001110	V_S	V_S	GND
1001111	V_S	V_S	V_S

7.3.3.3 Writing and Reading Operation

Accessing a particular register on the TMP75B is accomplished by writing the appropriate value to the pointer register. The value for the pointer register is the first byte transferred after the slave address byte with the R/$\overline{W}$ bit low. Every write operation to the TMP75B requires a value for the pointer register (see Figure 9).

When reading from the TMP75B, the last value stored in the pointer register by a write operation is used to determine which register is read by a read operation. To change the register pointer for a read operation, a new value must be written to the pointer register. This action is accomplished by issuing a slave address byte with the R/$\overline{W}$ bit low, followed by the pointer register byte. No additional data are required. The master can then generate a start condition and send the slave address byte with the R/$\overline{W}$ bit high to initiate the read command. See Figure 10 for details of this sequence. If repeated reads from the same register are desired, there is no need to continually send the pointer register bytes because the TMP75B stores the pointer register value until it is changed by the next write operation.

Note that register bytes are sent with the most significant byte first, followed by the least significant byte.

7.3.3.4 Slave-Mode Operations

The TMP75B can operate as a slave receiver or slave transmitter.

7.3.3.4.1 Slave Receiver Mode:

The first byte transmitted by the master is the slave address, with the R/$\overline{W}$ bit low. The TMP75B then acknowledges reception of a valid address. The next byte transmitted by the master is the pointer register. The TMP75B then acknowledges reception of the pointer register byte. The next byte or bytes are written to the register addressed by the pointer register. The TMP75B acknowledges reception of each data byte. The master can terminate data transfer by generating a start or stop condition.

7.3.3.4.2 Slave Transmitter Mode:

The first byte transmitted by the master is the slave address, with the R/$\overline{W}$ bit high. The slave acknowledges reception of a valid slave address. The next byte is transmitted by the slave and is the most significant byte of the register indicated by the pointer register. The master acknowledges reception of the data byte. The next byte transmitted by the slave is the least significant byte. The master acknowledges reception of the data byte. The master can terminate data transfer by generating a not-acknowledge bit on reception of any data byte, or by generating a start or stop condition.

7.3.3.5 SMBus Alert Function

The TMP75B supports the SMBus alert function. When the TMP75B operates in interrupt mode (TM = 1), the ALERT pin may be connected as an SMBus alert signal. When a master senses that an alert condition is present on the ALERT line, the master sends an SMBus alert command (00011001) to the bus. If the ALERT pin is active, the device acknowledges the SMBus alert command and responds by returning its slave address on the SDA line. The eighth bit (LSB) of the slave address byte indicates whether the alert condition is caused by the temperature exceeding T_{HIGH} or falling below T_{LOW}. The LSB is high if the temperature is greater than T_{HIGH}, or low if the temperature is less than T_{LOW}. See Figure 11 for details of this sequence.

If multiple devices on the bus respond to the SMBus alert command, arbitration during the slave address portion of the SMBus alert command determines which device clears its alert status first. If the TMP75B wins the arbitration, its ALERT pin becomes inactive at the completion of the SMBus alert command. If the TMP75B loses the arbitration, its ALERT pin remains active.

7.3.3.6 General Call

The TMP75B responds to a two-wire general call address (0000000) if the eighth bit is 0. The device acknowledges the general call address and responds to commands in the second byte. If the second byte is 00000100, the TMP75B latches the status of the address pin, but does not reset. If the second byte is 00000110, the TMP75B internal registers are reset to power-up values.

7.3.3.7 High-Speed (Hs) Mode

In order for the two-wire bus to operate at frequencies above 400 kHz, the master device must issue an SMBus Hs-mode master code (00001xxx) as the first byte after a start condition to switch the bus to high-speed operation. The TMP75B does not acknowledge this byte, but does switch its input filters on SDA and SCL and its output filters on SDA to operate in Hs-mode, allowing transfers at up to 3 MHz. After the Hs-mode master code has been issued, the master transmits a two-wire slave address to initiate a data-transfer operation. The bus continues to operate in Hs-mode until a stop condition occurs on the bus. Upon receiving the stop condition, the TMP75B switches the input and output filters back to fast-mode operation.

7.3.3.8 Timeout Function

The TMP75B resets the serial interface if SCL or SDA are held low for 54 ms (typ) between a start and stop condition. If the TMP75B is pulled low, it releases the bus and then waits for a start condition. To avoid activating the timeout function, it is necessary to maintain a communication speed of at least 1 kHz for the SCL operating frequency.

7.3.3.9 Two-Wire Timing

The TMP75B is two-wire and SMBus compatible. Figure 8 to Figure 11 describe the various operations on the TMP75B. Parameters for Figure 8 are defined in Table 3. Bus definitions are:

Bus Idle Both SDA and SCL lines remain high.

Start Data Transfer A change in the state of the SDA line, from high to low, while the SCL line is high defines a start condition. Each data transfer is initiated with a start condition.

Stop Data Transfer A change in the state of the SDA line from low to high while the SCL line is high defines a stop condition. Each data transfer is terminated with a repeated start or stop condition.

Data Transfer The number of data bytes transferred between a start and a stop condition is not limited, and is determined by the master device.

The receiver acknowledges the transfer of data. It is also possible to use the TMP75B for single-byte updates. To update only the MS byte, terminate communication by issuing a start or stop condition on the bus.

Acknowledge Each receiving device, when addressed, must generate an acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse so that the SDA line is stable low during the high period of the acknowledge clock pulse. Setup and hold times must be taken into account. When a master receives data, the termination of the data transfer can be signaled by the master generating a *not-acknowledge* (1) on the last byte transmitted by the slave.

Table 3. Timing Diagram Requirements

SYMBOL	PARAMETER		FAST MODE		HIGH-SPEED MODE		UNIT
			MIN	MAX	MIN	MAX	
$f_{(SCL)}$	SCL operating frequency	$V_S \geq 1.8$ V	0.001	0.4	0.001	3	MHz
		$V_S < 1.8$ V	0.001	0.4	0.001	2.5	MHz
$t_{(BUF)}$	Bus free time between stop and start conditions	$V_S \geq 1.8$ V	1300		160		ns
		$V_S < 1.8$ V	1300		260		ns
$t_{(HDSTA)}$	Hold time after repeated start condition. After this period, the first clock is generated.		600		160		ns
$t_{(SUSTA)}$	Repeated start condition setup time		600		160		ns
$t_{(SUSTO)}$	Stop condition setup time		600		160		ns
$t_{(HDDAT)}$	Data hold time	$V_S \geq 1.8$ V	0	900	0	100	ns
		$V_S < 1.8$ V	0	900	0	140	ns
$t_{(SUDAT)}$	Data setup time	$V_S \geq 1.8$ V	100		10		ns
		$V_S < 1.8$ V	100		20		ns
$t_{(LOW)}$	SCL clock low period	$V_S \geq 1.8$ V	1300		190		ns
		$V_S < 1.8$ V	1300		240		ns
$t_{(HIGH)}$	SCL clock high period		600		60		ns
$t_{R(SDA)}$, $t_{F(SDA)}$	Data rise and fall time			300		80	ns
$t_{R(SCL)}$, $t_{F(SCL)}$	Clock rise and fall time			300		40	ns
t_R	Clock and data rise time for SCLK ≤ 100 kHz			1000			ns

7.3.3.10 Two-Wire Timing Diagrams

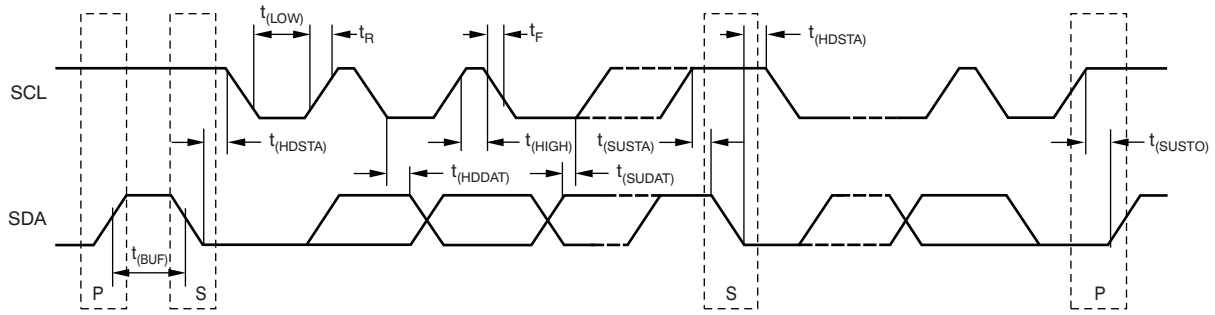
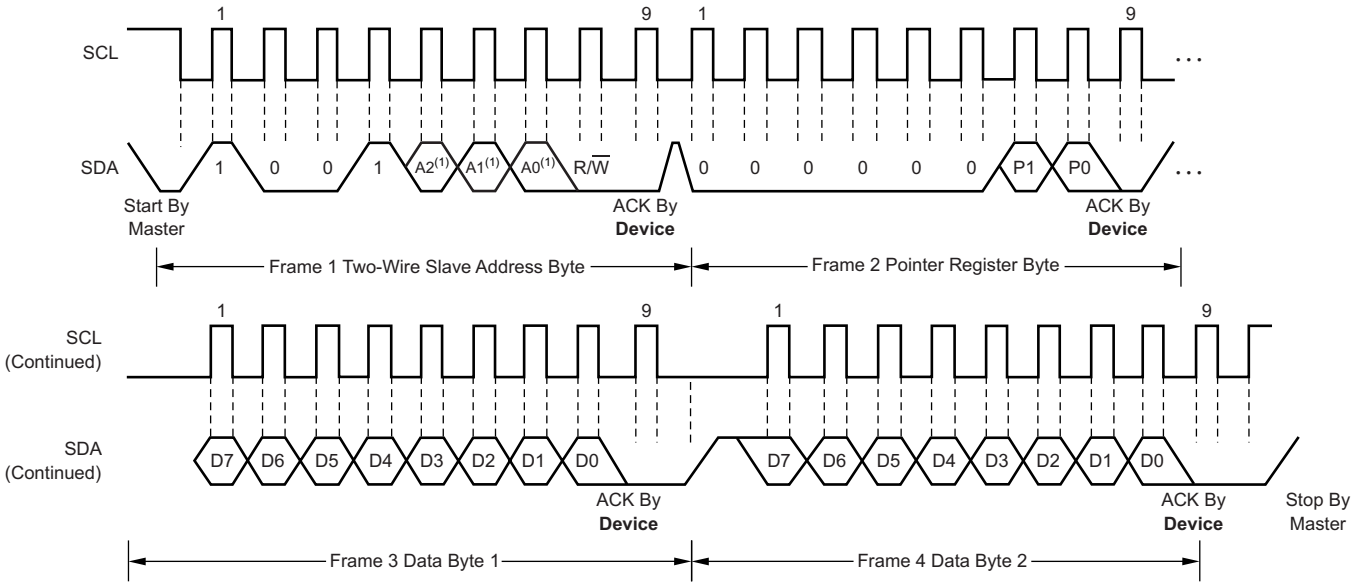
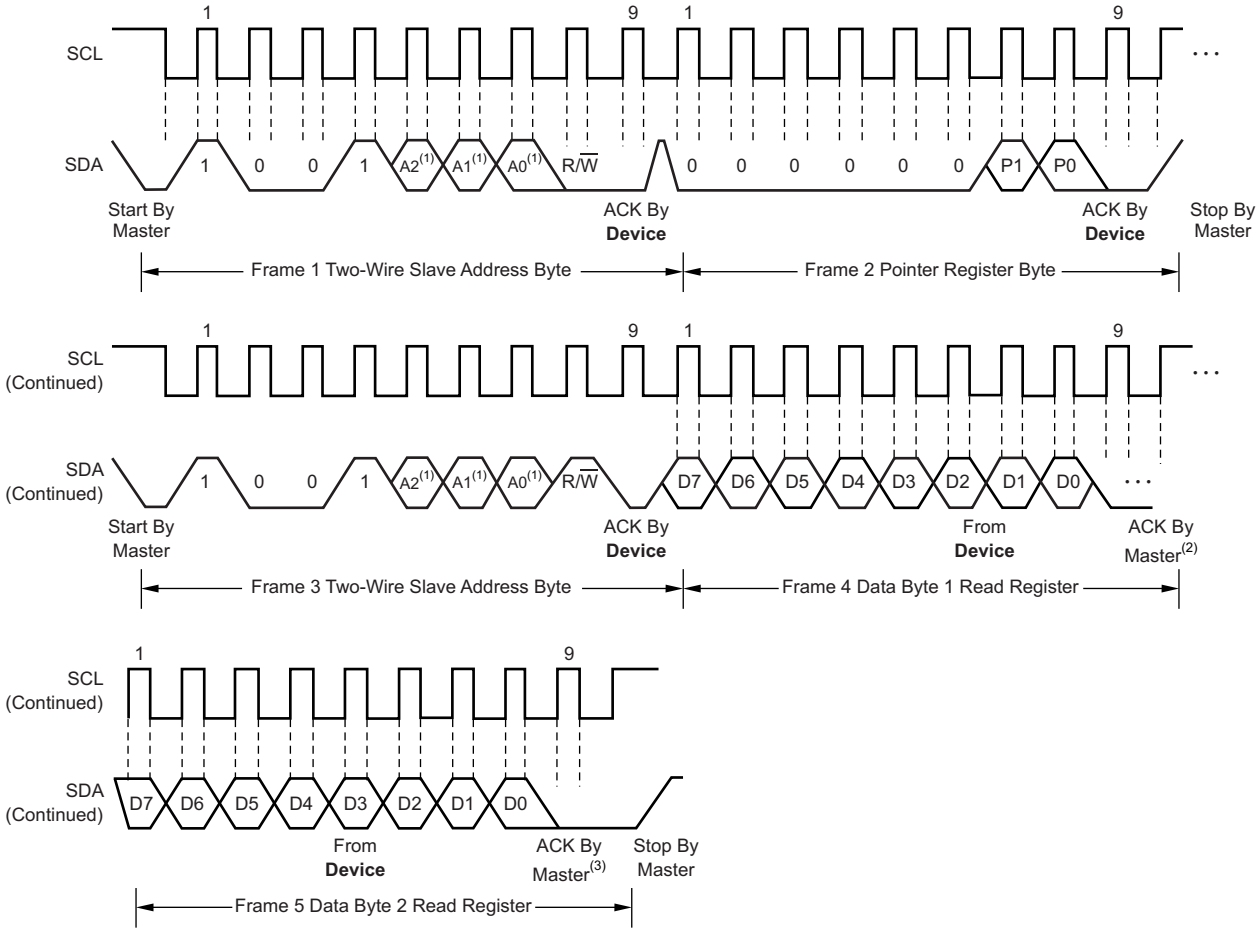


Figure 8. Two-Wire Timing Diagram



(1) The value of A0, A1, and A2 are determined by the connections of the corresponding pins.

Figure 9. Two-Wire Timing Diagram for Write Word Format

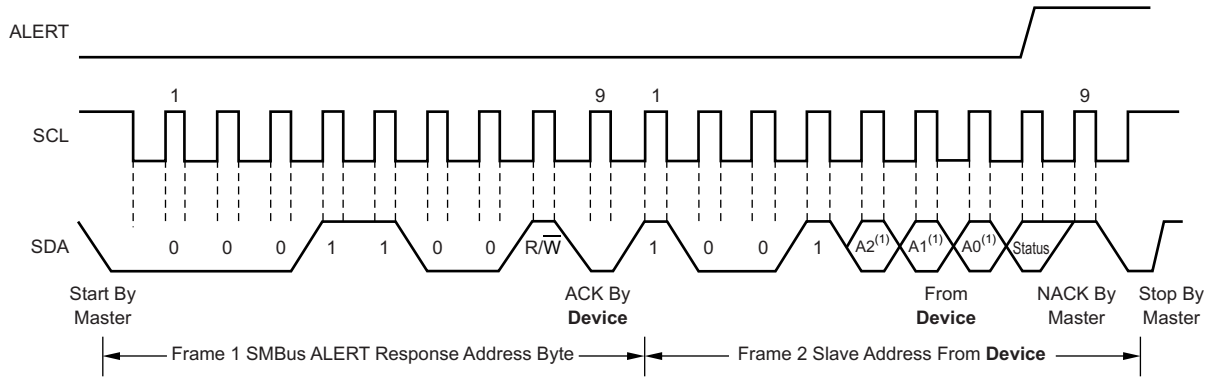


(1) The value of A0, A1, and A2 are determined by the connections of the corresponding pins.

(2) Master should leave SDA high to terminate a single-byte read operation.

(3) Master should leave SDA high to terminate a two-byte read operation.

Figure 10. Two-Wire Timing Diagram for Read Word Format



(1) The value of A0, A1, and A2 are determined by the connections of the corresponding pins.

Figure 11. Timing Diagram for SMBus Alert

7.4 Device Functional Modes

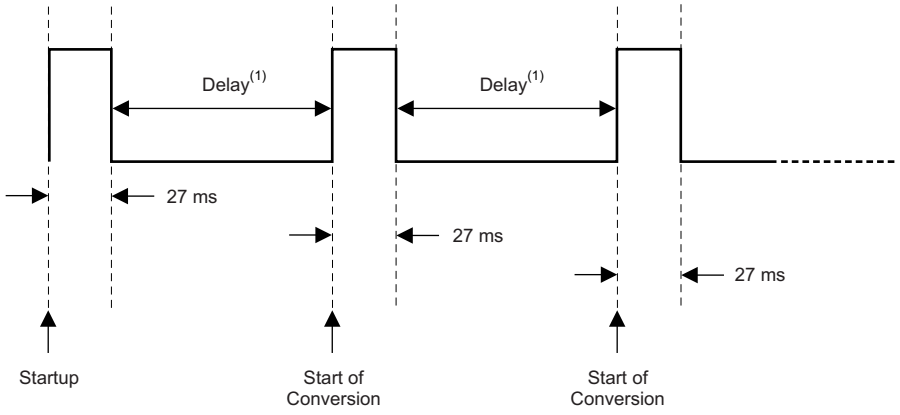
7.4.1 Continuous-Conversion Mode

The default mode of the TMP75B is continuous conversion, where the ADC performs continuous temperature conversions and stores each result to the temperature register, overwriting the result from the previous conversion. Conversion rate bits CR1 and CR0 in the configuration register configure the TMP75B for typical conversion rates of 37 Hz, 18 Hz, 9 Hz, or 4 Hz. The TMP75B has a typical conversion time of 27 ms. To achieve different conversion rates, the TMP75B makes a conversion, and then powers down and waits for the appropriate delay set by CR1 and CR0. The default rate is 37 Hz (no delay between conversions).Table 4 shows the settings for CR1 and CR0.

Table 4. Conversion Rate Settings

CR1	CR0	CONVERSION RATE (TYP)	I_Q (TYP)
0	0	37 Hz (continuous conversion, default)	45 µA
0	1	18 Hz	22 µA
1	0	9 Hz	12 µA
1	1	4 Hz	6.5 µA

After power-up or a general-call reset, the TMP75B immediately starts a conversion, as shown in Figure 12. The first result is available after 27 ms (typical). The active quiescent current during conversion is 45 µA (typical at +25°C). The quiescent current during delay is 1 µA (typical at +25°C).



(1) Delay is set by the CR bits in the configuration register.

Figure 12. Conversion Start

7.4.2 Shutdown Mode

Shutdown mode saves maximum power by shutting down all device circuitry other than the serial interface, and reduces current consumption to typically less than 0.3 µA. Shutdown mode is enabled when the SD bit in the configuration register is set to 1; the device shuts down after the current conversion is completed. When SD is equal to 0, the device operates in continuous-conversion mode. When shutdown mode is enabled, the ALERT pin and fault counter clear in both comparator and interrupt modes; however, this clearing occurs with the rising edge of the shutdown signal. After shutdown is enabled, reprogramming shutdown does not clear the ALERT pin and the fault counter until a rising edge is generated on the shutdown signal.

7.4.3 One-Shot Mode

The TMP75B features a *one-shot* temperature measurement mode. When the device is in shutdown mode, writing a 1 to the OS bit starts a single temperature conversion. The device returns to the shutdown state at the completion of the single conversion. This mode reduces power consumption in the TMP75B when continuous temperature monitoring is not required. When the configuration register is read, the OS bit always reads zero.

7.5 Programming

Figure 13 shows the internal register structure of the TMP75B. Use the 8-bit pointer register to address a given data register. The pointer register uses the two LSBs to identify which of the data registers respond to a read or write command. Figure 14 identifies the bits of the pointer register byte.

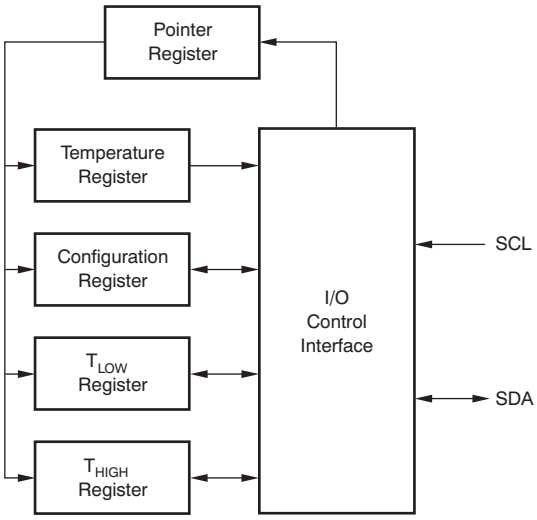


Figure 13. Internal Register Structure

7.6 Register Map

Table 5 describes the registers available in the TMP75B with their pointer addresses, followed by the description of the bits in each register.

Table 5. Register Map and Pointer Addresses

P1	P0	REGISTER
0	0	Temperature register (read only, default)
0	1	Configuration register (read/write)
1	0	T_{LOW} register (read/write)
1	1	T_{HIGH} register (read/write)

Figure 14. Pointer Register (pointer = N/A) [reset = 00h]

7	6	5	4	3	2	1	0
Reserved						P1	P0
W-0h						W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

Figure 15. Temperature Register (pointer = 0h) [reset = 0000h]

15	14	13	12	11	10	9	8
T11	T10	T9	T8	T7	T6	T5	T4
R-0h							
7	6	5	4	3	2	1	0
T3	T2	T1	T0	Reserved			
R-0h				R-0h			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6. Temperature Register Description

Name	Description
T11 to T4	The 8 MSBs of the temperature result (resolution of 1°C)
T3 to T0	The 4 LSBs of the temperature result (resolution of 0.0625°C)

Figure 16. Configuration Register (pointer = 1h) [reset = 00FFh]

15	14	13	12	11	10	9	8
OS	CR		FQ		POL	TM	SD
R/W-0h	R/W-0h		R/W-0h		R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
Reserved							
R-FFh							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7. Configuration Register Description

Name	Description
OS	One-shot mode In shutdown (SD = 1), write 1 to start a conversion. OS always reads back 0.
CR	Conversion rate control CR = 0h: 37-Hz conversion rate (typ) (default) CR = 1h: 18-Hz conversion rate (typ) CR = 2h: 9-Hz conversion rate (typ) CR = 3h: 4-Hz conversion rate (typ)
FQ	Fault queue to trigger the ALERT pin FQ = 0h: 1 fault (default) FQ = 1h: 2 faults FQ = 2h: 4 faults FQ = 3h: 6 faults
POL	ALERT polarity control POL = 0: ALERT is active low (default) POL = 1: ALERT is active high
TM	ALERT thermostat mode control TM = 0: ALERT is in comparator mode (default) TM = 1: ALERT is in interrupt mode
SD	Shutdown control bit SD = 0: Device is in continuous conversion mode (default) SD = 1: Device is in shutdown mode

Figure 17. T_{LOW} - Temperature Low Limit Register (pointer = 2h) [reset = 4B00h](1)

15	14	13	12	11	10	9	8
L11	L10	L9	L8	L7	L6	L5	L4
R/W-4Bh							
7	6	5	4	3	2	1	0
L3	L2	L1	L0	Reserved			
R/W-0h				R-0h			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

(1) 4B00h = 75°C.

Table 8. T_{LOW} Register Description

Name	Description
L11 to L4	The 8 MSBs of the temperature low limit (resolution of 1°C)
L3 to L0	The 4 LSBs of the temperature low limit (resolution of 0.0625°C)

Figure 18. T_{HIGH} - Temperature High Limit Register (pointer = 3h) [reset = 5000h](1)

15	14	13	12	11	10	9	8
H11	H10	H9	H8	H7	H6	H5	H4
R/W-50h							
7	6	5	4	3	2	1	0
H3	H2	H1	H0	Reserved			
R/W-0h				R-0h			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

(1) 5000h = 80°C.

Table 9. T_{HIGH} Register Description

Name	Description
H11 to H4	The 8 MSBs of the temperature high limit (resolution of 1°C)
H3 to H0	The 4 LSBs of the temperature high limit (resolution of 0.0625°C)

8 Application and Implementation

8.1 Application Information

The TMP75B is used to measure the PCB temperature of the location it is mounted. The programmable address options allow up to eight locations on the board to be monitored on a single serial bus. Connecting the ALERT pins together and programming the temperature limit registers to desired values allows for a temperature watchdog operation of all devices, interrupting the host controller only if the temperature exceeds the limits.

8.2 Typical Application

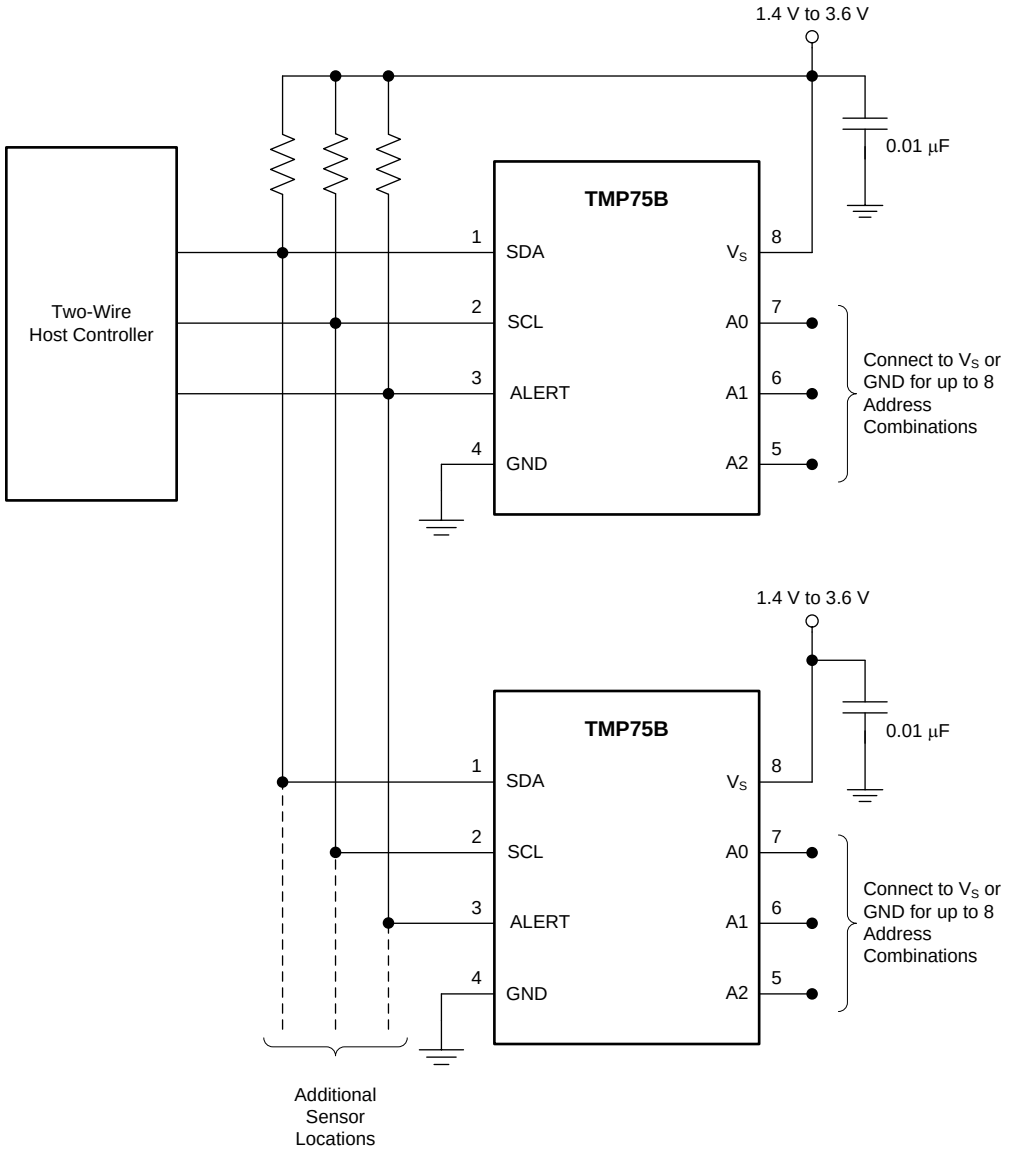


Figure 19. Temperature Monitoring of Multiple Locations on a PCB

Typical Application (continued)

8.2.1 Design Requirements

The TMP75B only requires pull-up resistors on SDA and ALERT, although a pull-up resistor is typically present on the SCL as well. A 0.01-µF bypass capacitor on the supply is recommended, as shown in Figure 19. The SCL, SDA, and ALERT lines can be pulled up to a supply that is equal to or higher than V_S through the pull-up resistors. To configure one of eight different addresses on the bus, connect A0, A1, and A2 to either V_S or GND.

8.2.2 Detailed Design Procedure

The TMP75B should be placed in close proximity to the heat source to be monitored, with a proper layout for good thermal coupling. This ensures that temperature changes are captured within the shortest possible time interval.

8.2.3 Application Curves

Figure 20 shows the step response of the TMP75B to a submersion in an oil bath of 100°C from room temperature (27°C). The time-constant, or the time for the output to reach 63% of the input step, is 1.5 seconds.

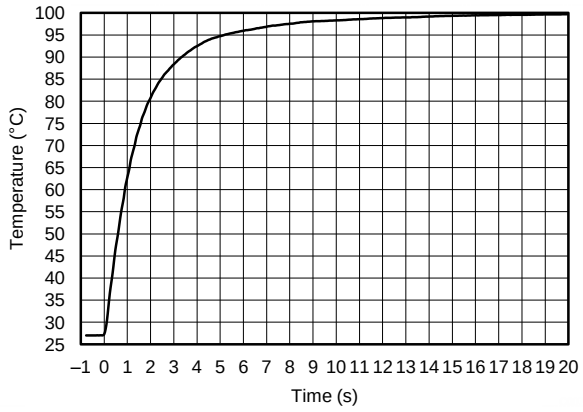


Figure 20. Temperature Step Response

9 Power Supply Recommendations

The TMP75B operates with power supply in the range of 1.4 V to 3.6 V. It is optimized for operation at 1.8-V supply but can measure temperature accurately in the full supply range.

A power-supply bypass capacitor is required for stability; place this capacitor as close as possible to the supply and ground pins of the device. A typical value for this supply bypass capacitor is 0.01 µF. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise.

10 Layout

10.1 Layout Guidelines

Place the power-supply bypass capacitor as close as possible to the supply and ground pins. The recommended value of this bypass capacitor is 0.01 µF. Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies.

Pull up the open-drain output pins (SDA and ALERT) to a supply voltage rail (V_S or higher but up to 3.6 V) through 10-kΩ pull-up resistors.

10.2 Layout Example

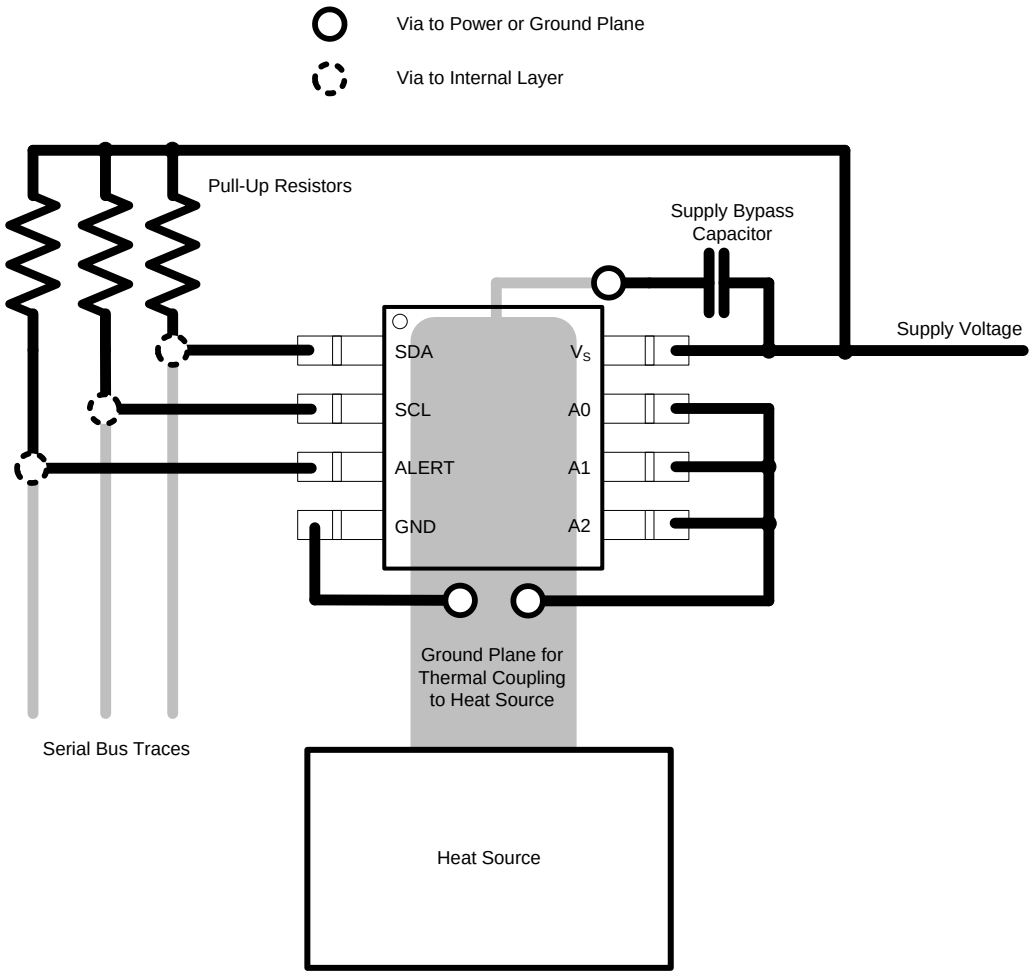


Figure 21. Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

SBOU141 — TMP75xEVM User's Guide

11.2 Trademarks

All trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMP75BID	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-55 to 125	TMP75B
TMP75BIDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-2-260C-1 YEAR	-55 to 125	T75B
TMP75BIDGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	T75B
TMP75BIDGKT	Obsolete	Production	VSSOP (DGK) | 8	-	-	Call TI	Call TI	-55 to 125	T75B
TMP75BIDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	TMP75B
TMP75BIDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	TMP75B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TMP75B :

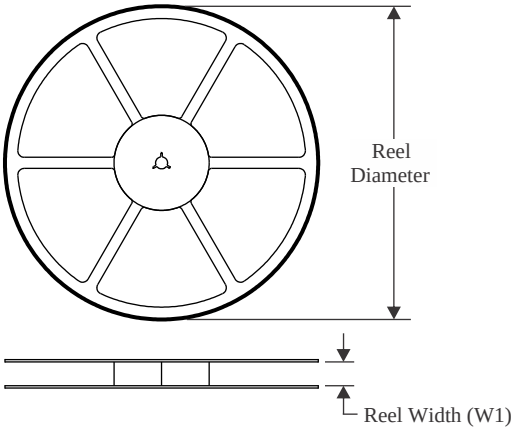
- Automotive : TMP75B-Q1

NOTE: Qualified Version Definitions:

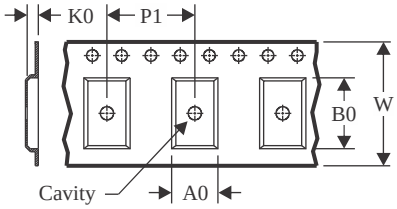
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

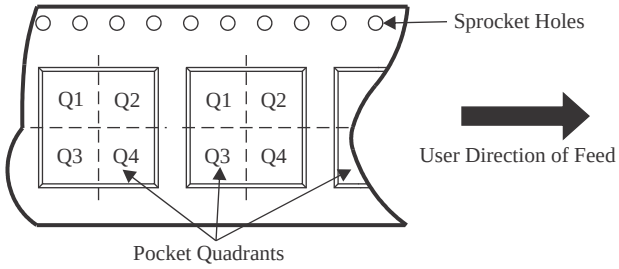


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

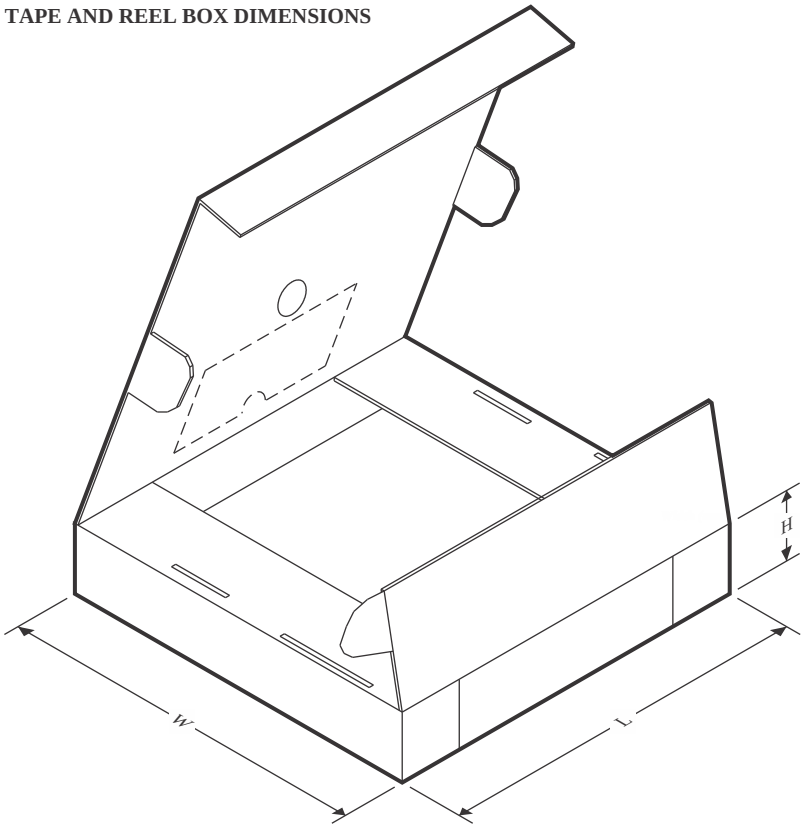
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP75BIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TMP75BIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TMP75BIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

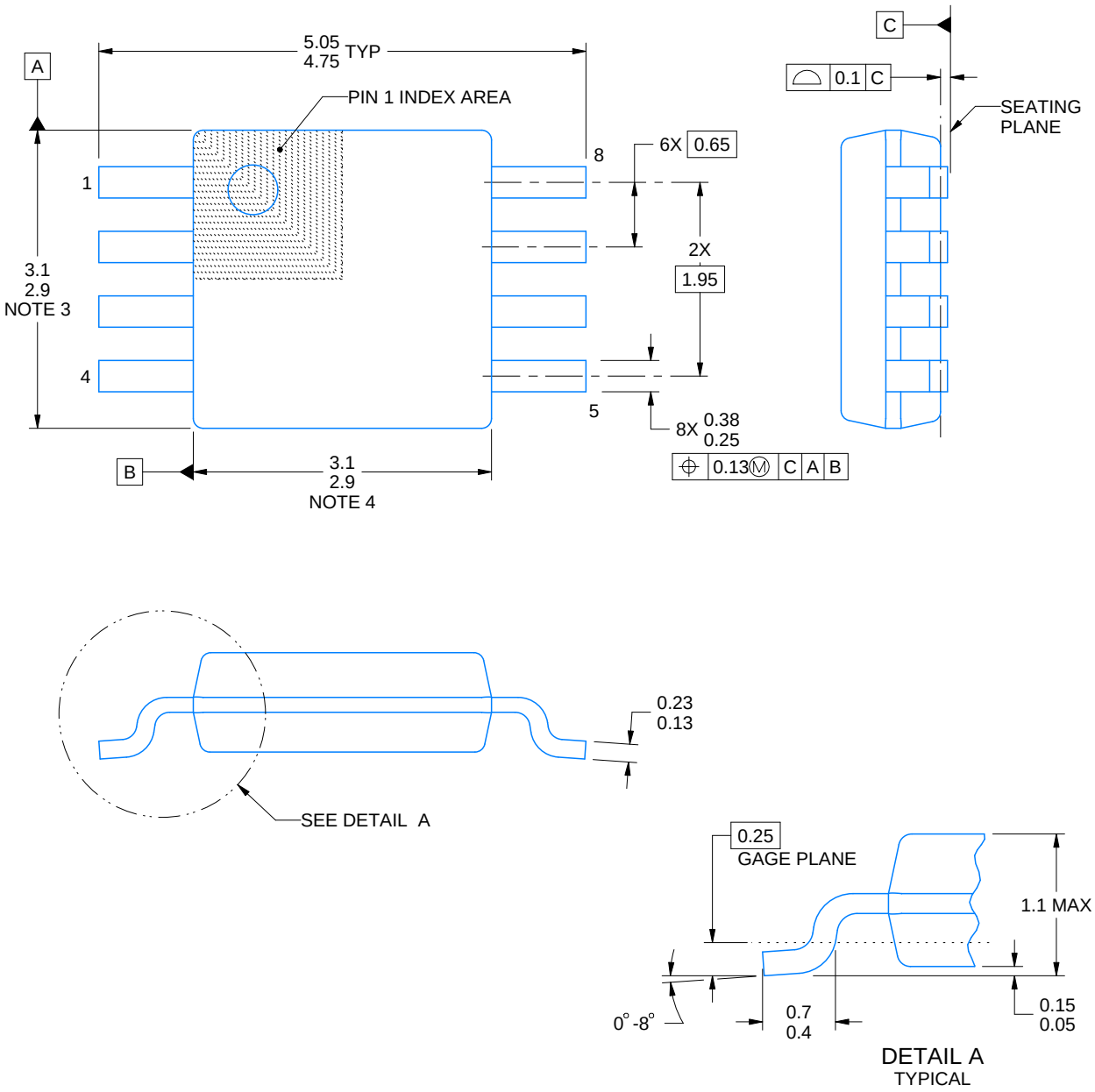
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP75BIDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
TMP75BIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
TMP75BIDR	SOIC	D	8	2500	353.0	353.0	32.0

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

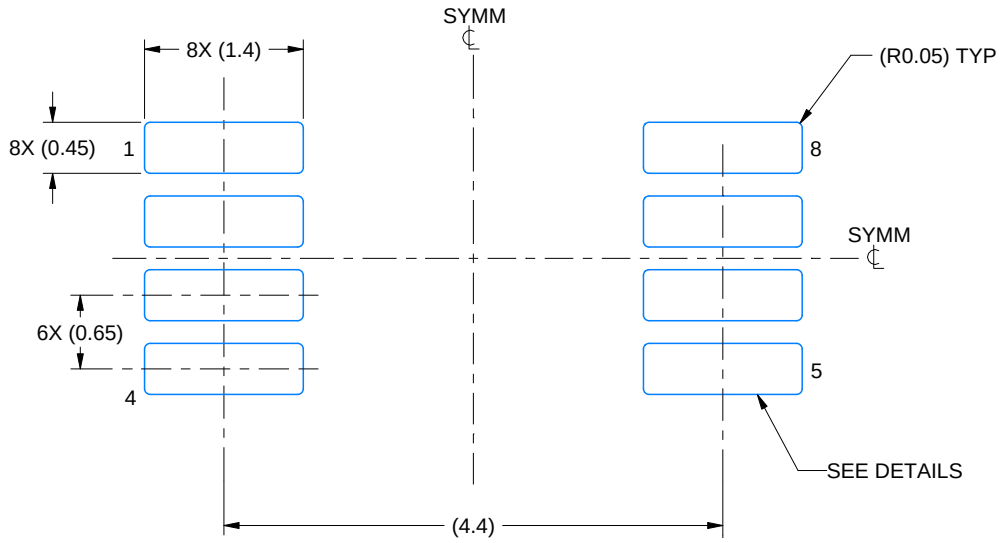
SMALL OUTLINE PACKAGE



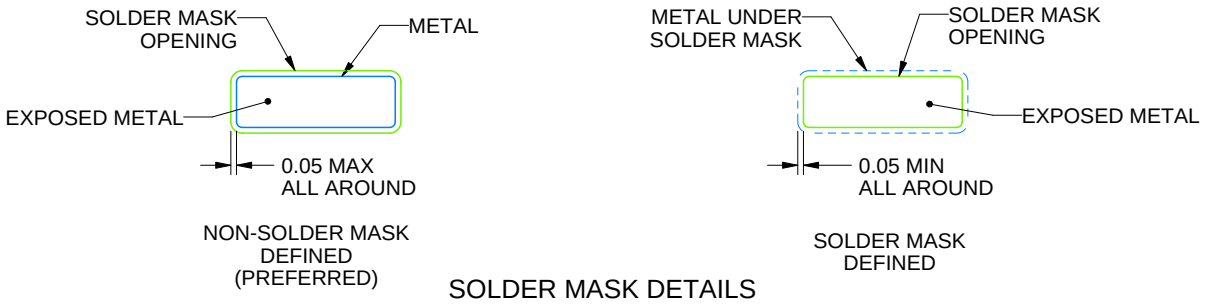
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

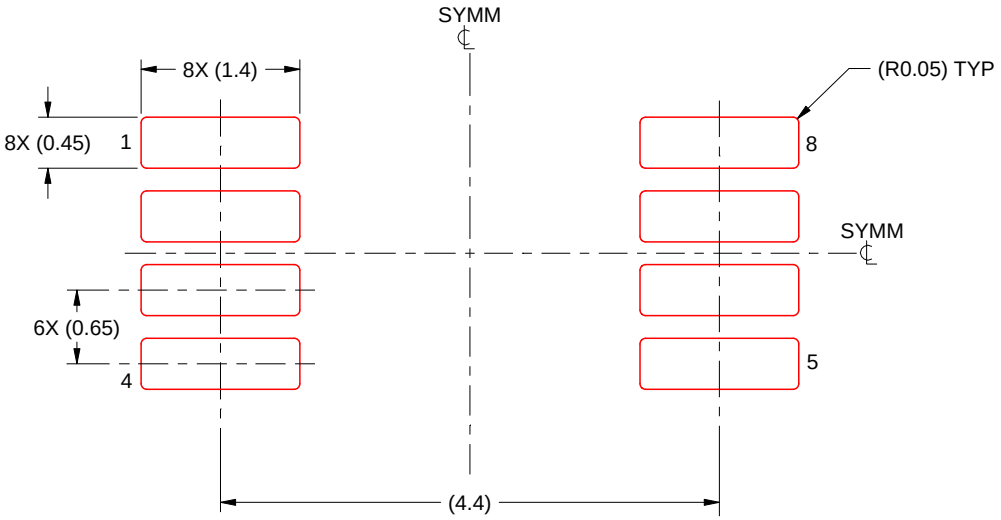


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

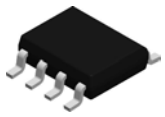


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

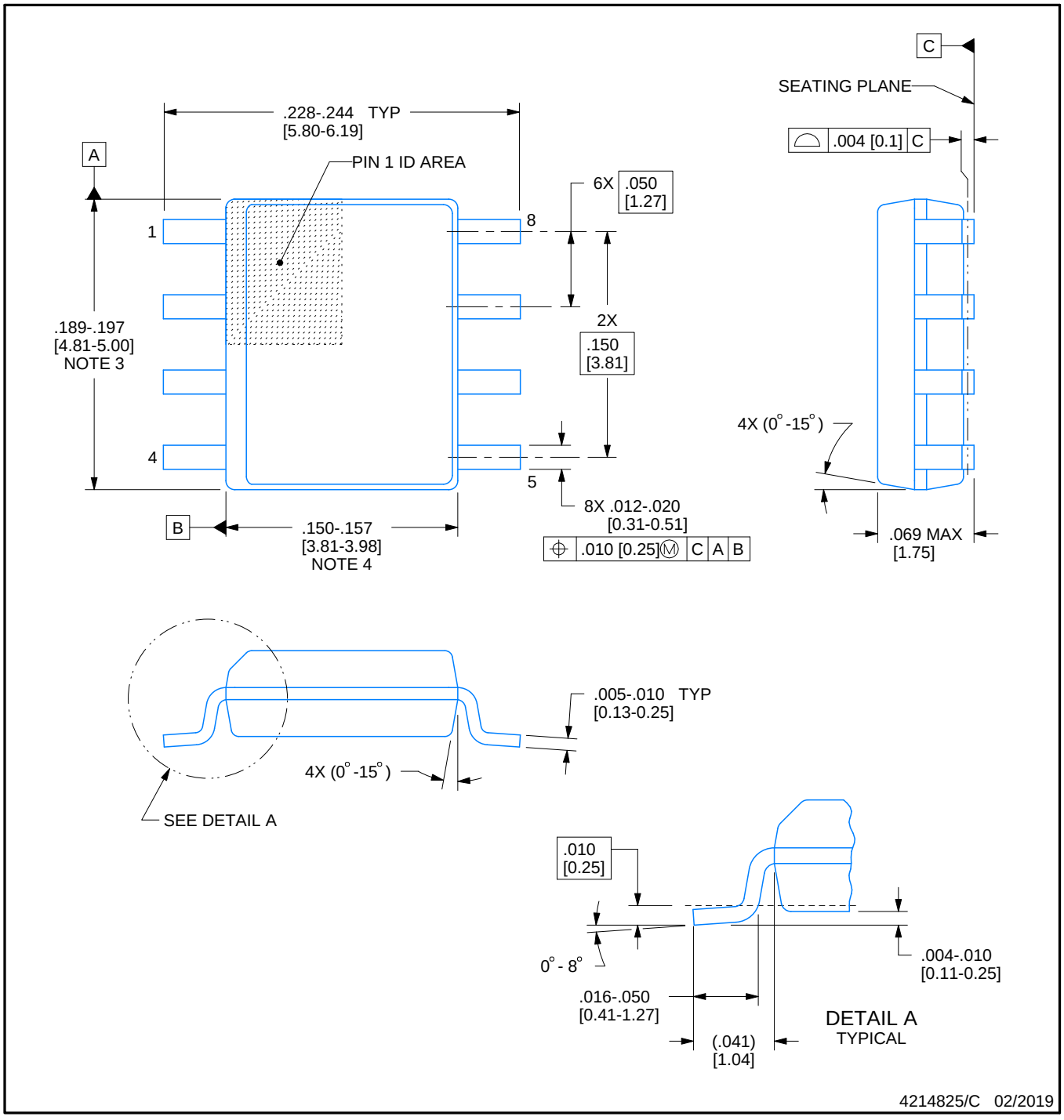


PACKAGE OUTLINE

D0008A

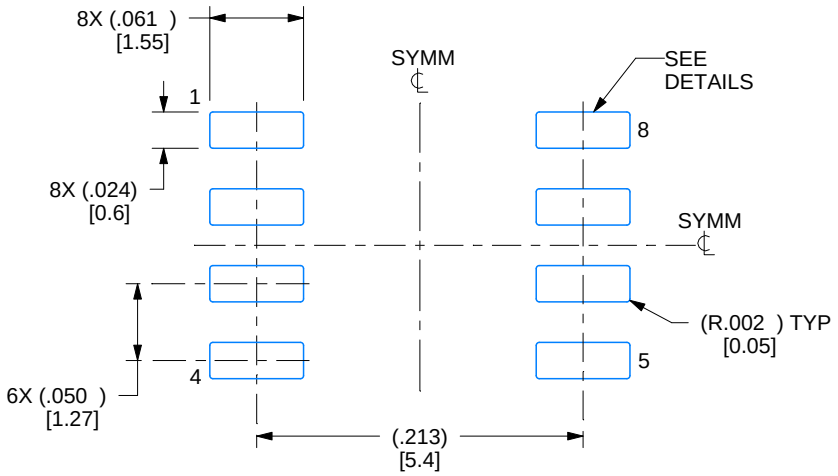
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

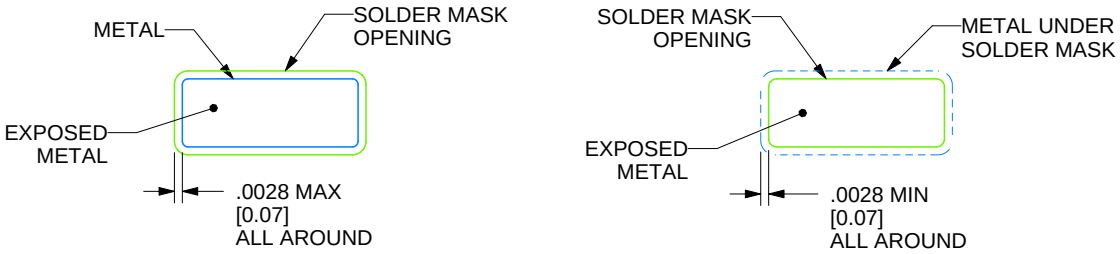


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

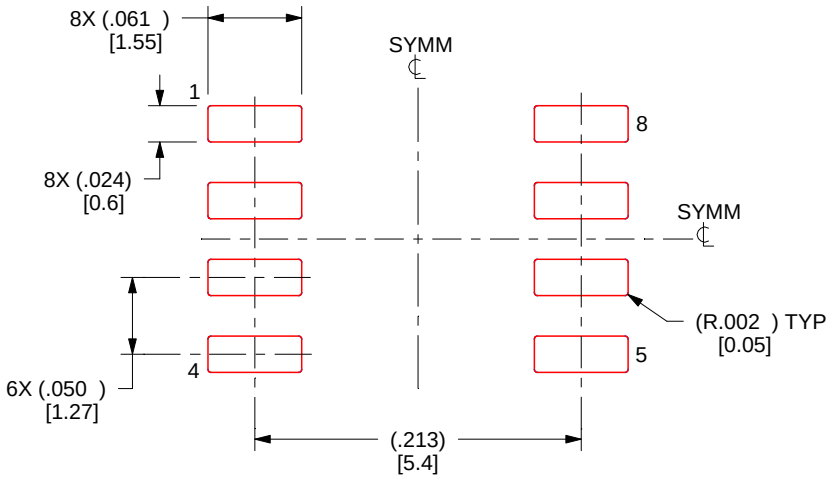
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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