

TMP708-Q1 車載用、抵抗によりプログラム可能なSOTパッケージの温度スイッチ

1 特長

- 車載アプリケーションに対応
- 下記内容でAEC-Q100認定済み:
 - デバイス温度グレード1: 動作時周囲温度範囲 $-40^{\circ}\text{C} \sim 125^{\circ}\text{C}$
 - デバイスHBM ESD分類レベル3A
 - デバイスCDM ESD分類レベルC6
- スレッシュホールド精度:
 - $\pm 0.5^{\circ}\text{C}$ (標準値)
 - $\pm 3.5^{\circ}\text{C}$ (最大値、 $60^{\circ}\text{C} \sim 100^{\circ}\text{C}$)
- 1%の外付け抵抗により温度スレッシュホールドを設定
- 低い静止電流: $40\mu\text{A}$ (標準値)
- オープン・ドレイン、アクティブLOWの出力ステージ
- 10°C または 30°C のヒステリシスをピンで選択可能
- $V_{\text{CC}} = 0.8\text{V}$ でリセット動作を規定
- 電源電圧範囲: $2.7\text{V} \sim 5.5\text{V}$
- パッケージ: 5ピンのSOT-23

2 アプリケーション

- コンピュータ (ラップトップおよびデスクトップ)
- サーバー
- 産業用および医療用機器
- ストレージ・エリア・ネットワーク
- 車載

3 概要

TMP708-Q1は完全に統合された、抵抗によりプログラム可能な温度スイッチで、1つの外付け抵抗だけで温度範囲全体に温度スレッシュホールドを設定できます。TMP708-Q1には、オープン・ドレイン、アクティブLOWの出力があり、 $2.7\text{V} \sim 5.5\text{V}$ の電源電圧範囲で動作します。

温度スレッシュホールド精度は標準で $\pm 0.5^{\circ}\text{C}$ 、最大値は $\pm 3.5^{\circ}\text{C}$ です($60^{\circ}\text{C} \sim 100^{\circ}\text{C}$)。待機時消費電流は、標準で $40\mu\text{A}$ です。ヒステリシスは、ピンによって 10°C または 30°C に設定できます。

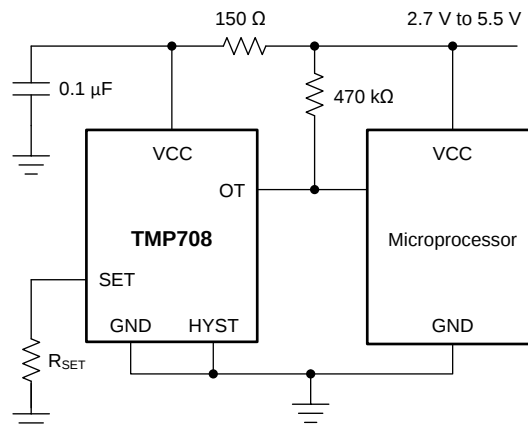
TMP708-Q1は5ピンのSOT-23パッケージで供給されます。

製品情報⁽¹⁾

型番	パッケージ	本体サイズ(公称)
TMP708-Q1	SOT-23 (5)	2.90mm×1.60mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にあるパッケージ・オプションについての付録を参照してください。

代表的なアプリケーション



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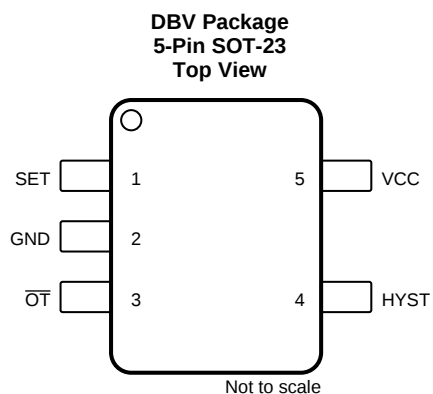
目次

1	特長	1	7.4	Device Functional Modes.....	8
2	アプリケーション	1	8	Application and Implementation	9
3	概要	1	8.1	Application Information.....	9
4	改訂履歴	2	8.2	Typical Application	9
5	Pin Configuration and Functions	3	9	Power Supply Recommendations	11
6	Specifications	4	10	Layout	11
6.1	Absolute Maximum Ratings	4	10.1	Layout Guidelines	11
6.2	ESD Ratings.....	4	10.2	Layout Example	11
6.3	Recommended Operating Conditions.....	4	10.3	Thermal Considerations	11
6.4	Thermal Information	4	11	デバイスおよびドキュメントのサポート	12
6.5	Electrical Characteristics.....	5	11.1	ドキュメントの更新通知を受け取る方法.....	12
6.6	Typical Characteristics	6	11.2	コミュニティ・リソース	12
7	Detailed Description	7	11.3	商標	12
7.1	Overview	7	11.4	静電気放電に関する注意事項	12
7.2	Functional Block Diagram	7	11.5	用語集	12
7.3	Feature Description.....	8	12	メカニカル、パッケージ、および注文情報	12

4 改訂履歴

日付	改訂内容	注
2016年12月	*	初版

5 Pin Configuration and Functions



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
GND	2	Analog power	Device ground
HYST	4	Digital input	Hysteresis selection. For 10°C, HYST = VCC; for 30°C, HYST = GND.
$\overline{\text{OT}}$	3	Digital output	Open-drain, active low output
SET	1	Analog input	Temperature set point. Connect an external 1% resistor between SET and GND.
VCC	5	Analog power	Power-supply voltage (2.7 V to 5.5 V)

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
Voltage	Supply, V _{CC}	−0.3	6	V
	Input, SET and HYST	−0.3	V _{CC} + 0.3	
	Output, OT	−0.3	6	
Current	Input		20	mA
	Output		20	
Temperature	Operating, T _A	−40	125	°C
	Junction, T _J		150	
	Storage, T _{stg}	−65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD) Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	±4000	V
	Charged-device model (CDM), per AEC Q100-011	±1000	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	2.7		5.5	V
T _A	Operating temperature	0		125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TMP708-Q1	UNIT
		DBV (SOT-23)	
		5 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	217.9	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	86.3	°C/W
R _{θJB}	Junction-to-board thermal resistance	44.6	°C/W
ψ _{JT}	Junction-to-top characterization parameter	4.4	°C/W
ψ _{JB}	Junction-to-board characterization parameter	43.8	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

at $T_A = 0^{\circ}\text{C}$ to 125°C and $V_{CC} = 2.7\text{ V}$ to 5.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
POWER SUPPLY							
I _{CC}	Supply current	V _{CC} = 5 V		40	55	μA	
		V _{CC} = 2.7 V		40	55	μA	
TEMPERATURE							
T _E	Temperature error	T _A = 60°C to 100°C		±0.5	±3.5	°C	
DIGITAL INPUT (HYST)							
V _{IH}	High-level input voltage		0.7 × V _{CC}			V	
V _{IL}	Low-level input voltage		0.3 × V _{CC}			V	
I _{lkg_in}	Input leakage current		1			μA	
C _{IN}	Input capacitance		10			pF	
ANALOG INPUT (SET)							
V _{IN}	Input voltage range		0			V _{CC}	V
DIGITAL OPEN-DRAIN OUTPUT (OT)							
I _(OT_SINK)	Output sink current	V _{OT} = 0.3 V	5	12		mA	
I _{lka(OT)}	Output leakage current	V _{OT} = V _{CC}		1		μA	

6.6 Typical Characteristics

at $T_A = 25^\circ\text{C}$ and $V_{CC} = 2.7\text{ V}$ to 5.5 V (unless otherwise noted)

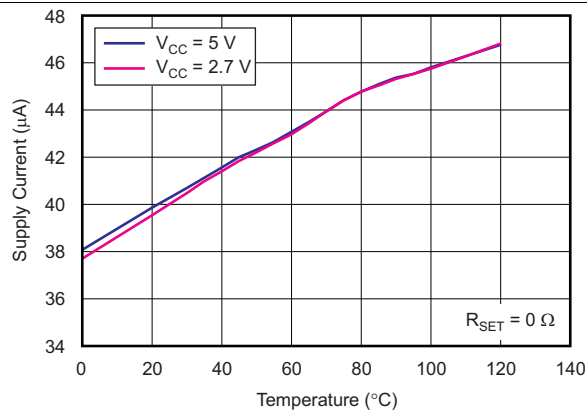


Figure 1. Supply Current vs Temperature

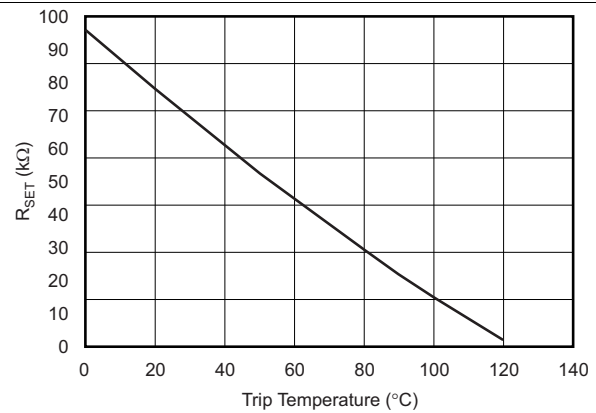


Figure 2. R_{SET} vs Trip Temperature

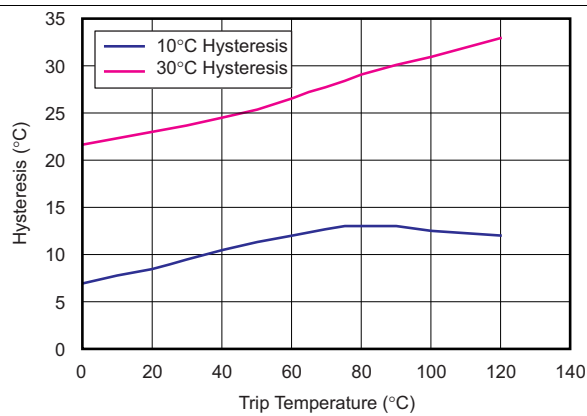


Figure 3. Hysteresis vs Trip Temperature

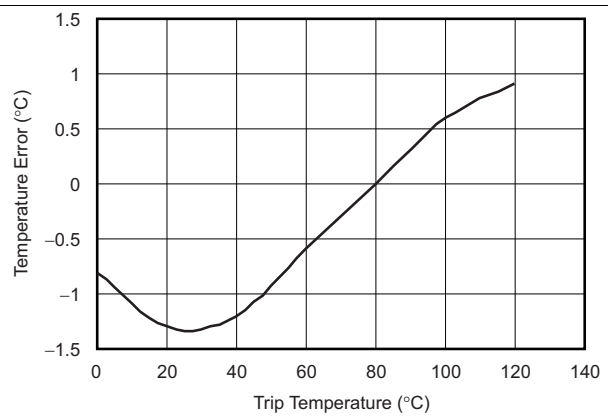


Figure 4. Temperature Error vs Trip Temperature

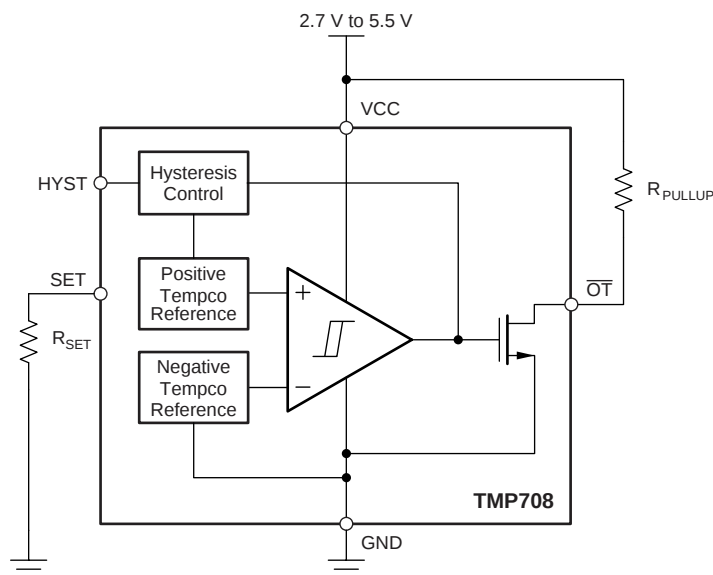
7 Detailed Description

7.1 Overview

The TMP708-Q1 is a fully-integrated, resistor-programmable temperature switch that incorporates two temperature-dependent voltage references and one comparator. One voltage reference exhibits a positive temperature coefficient (tempco), and the other voltage reference exhibits a negative tempco. The temperature at which both voltage references are equal determines the temperature trip point.

The [Functional Block Diagram](#) shows the comparator, the NFET open-drain device connected to the $\overline{\text{OT}}$ pin, the positive tempco reference using the external R_{SET} resistor, the negative tempco reference, and the hysteresis control. The voltage of the positive tempco reference is controlled by external resistor R_{SET} .

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Temperature Switch

The TMP708-Q1 temperature threshold is programmable from 0°C to 125°C and is set by an external 1% resistor from the SET pin to the GND pin. The TMP708-Q1 has an open-drain, active-low output structure that easily interfaces with a microprocessor.

The TMP708-Q1 reaches the temperature trip point when the voltage from the positive tempco reference exceeds the voltage from the negative tempco reference. This difference causes the output of the comparator to switch from logic 0 to logic 1. The comparator output drives the gate of the NFET open-drain device, and pulls the voltage on the $\overline{\text{OT}}$ pin from logic 1 to logic 0 under these conditions; in other words, the output *trips*. Furthermore, the logic 1 output from the comparator causes the hysteresis control to increase the voltage of the positive tempco reference by an amount set by the logic setting on the HYST pin (10°C for logic 1 on the HYST pin; 30°C for logic 0 on the HYST pin). Increase the voltage of the positive tempco reference after the TMP708-Q1 trips to stop the TMP708-Q1 from untripping (voltage on the $\overline{\text{OT}}$ pin changing from logic 0 to logic 1) until the local temperature reduces by the amount set by the HYST pin. After the local temperature reduces, and the voltage from the positive tempco reference is less than the voltage from the negative tempco reference, the output of the comparator switches from logic 1 to logic 0. This condition causes the voltage on the $\overline{\text{OT}}$ pin to change from logic 0 to logic 1 (device untrips).

7.3.2 Hysteresis Input

The HYST pin is a digital input that allows the input hysteresis to be set at either 10°C (when HYST = VCC) or 30°C (when HYST = GND). The hysteresis function keeps the $\overline{\text{OT}}$ pin from oscillating when the temperature is near the threshold. Thus, always connect the HYST pin to either VCC or GND. Other input voltages on this pin can cause abnormal supply currents or a device malfunction.

7.3.3 Set-Point Resistor (R_{SET})

Set the temperature threshold by connecting R_{SET} from the SET pin to GND. The value of R_{SET} is determined using either [Figure 2](#) or [Equation 1](#):

$$R_{\text{SET}} (\text{k}\Omega) = 0.0012T^2 - 0.9308T + 96.147$$

where

- T = temperature threshold in degrees Celsius. (1)

7.4 Device Functional Modes

The TMP708-Q1 device has a single functional mode. Normal operation for the TMP708-Q1 device occurs when the power-supply voltage applied across the VCC and GND pins is within the specified operating range of 2.7 V to 5.5 V.

8 Application and Implementation

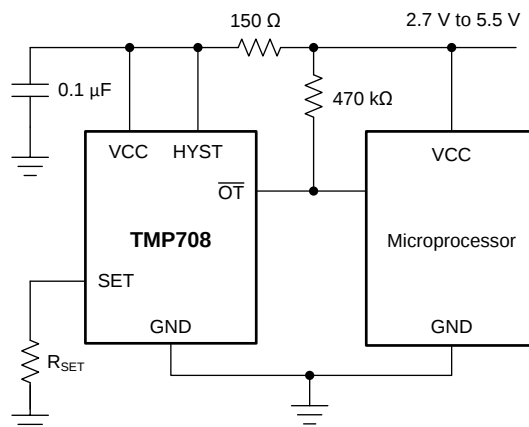
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TMP708-Q1 device is simple to configure. The only external components that the device requires are a bypass capacitor and pullup resistor. Power-supply bypassing is strongly recommended. Use a 0.1- μ F capacitor placed as close as possible to the VCC supply pin. To minimize the internal power dissipation of the TMP708-Q1 family of devices, use a pullup resistor value greater than 10 k Ω from the $\overline{OT}$ pin to the VCC pin. See the [Hysteresis Input](#) section for hysteresis configuration, and the [Set-Point Resistor \(\$R_{SET}\$ \)](#) section for configuring the temperature threshold.

8.2 Typical Application



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Figure 5. Overtemperature Protection for a 60°C Trip Point

8.2.1 Design Requirements

For this design example, a 2.7-V to 5.5-V power supply, 60°C trip point, and 10°C hysteresis are used.

Typical Application (continued)

8.2.2 Detailed Design Procedure

Connect the HYST pin to VCC for 10°C hysteresis. For a 60°C temperature threshold, see the [Set-Point Resistor \(\$R_{SET}\$ \)](#) section to compute an ideal R_{SET} resistor value of 44.619 k Ω . Select the closest standard value resistor available; in this case, 44.2 k Ω . Use a 10-k Ω pullup resistor from the $\overline{OT}$ pin to the VCC pin. To minimize power, a larger-value pullup resistor can be used, but must not exceed 470 k Ω . Place a 0.1- μ F bypass capacitor close to the TMP708-Q1 device in order to reduce noise coupled from the power supply.

8.2.3 Application Curves

Figure 6 shows an example of the hysteresis feature. The HYST pin is connected to VCC, so the TMP708-Q1 device is configured for 10°C of hysteresis. The device is configured for a 60°C trip temperature by the R_{SET} resistor value; therefore, the $\overline{OT}$ output asserts low when the 60°C threshold is exceeded. The $\overline{OT}$ output remains asserted low until the sensor reaches 50°C.

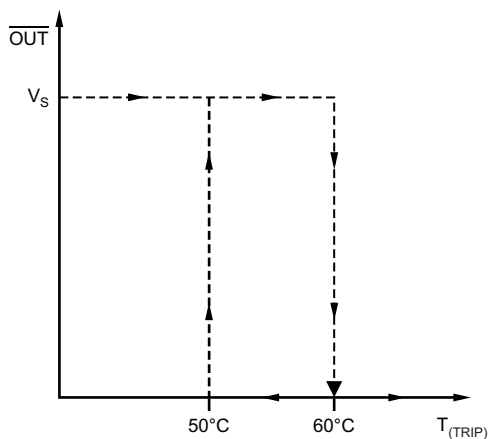


Figure 6. TMP708-Q1 Hysteresis Function

9 Power Supply Recommendations

The TMP708-Q1 low supply current and supply range allow this device to be powered from many sources. Any significant noise on the VCC pin can result in a trip-point error. Minimize this noise by low-pass filtering the device supply (V_{CC}) using a 150-Ω resistor and a 0.1-μF capacitor.

10 Layout

10.1 Layout Guidelines

The TMP708-Q1 is extremely simple to lay out. [Figure 7](#) shows the recommended board layout.

10.2 Layout Example

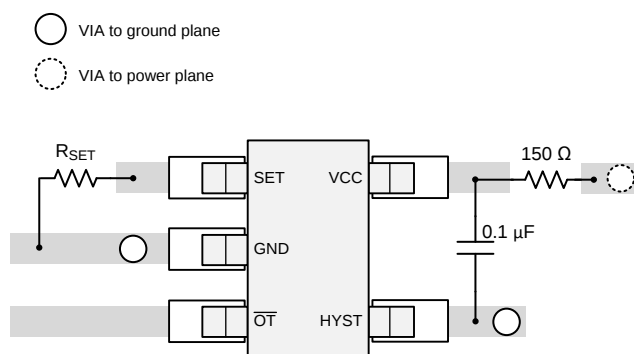


Figure 7. Recommended Layout

10.3 Thermal Considerations

The TMP708-Q1 quiescent current is typically 40 μA. The device dissipates negligible power when the output drives a high-impedance load. Thus, the die temperature is the same as the package temperature. In order to maintain accurate temperature monitoring, provide a good thermal contact between the TMP708-Q1 package and the device being monitored. The rise in die temperature as a result of self-heating is given by [Equation 2](#):

$$\Delta T_J = P_{DISS} \times \theta_{JA}$$

where

- P_{DISS} = power dissipated by the device.
- θ_{JA} = package thermal resistance. Typical thermal resistance for SOT-23 package is 217.9°C/W. (2)

To limit the effects of self-heating, keep the output current at a minimum level.

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.2 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

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設計サポート *TIの設計サポート* 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

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静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.5 用語集

SLYZ022 — *TI用語集*.

この用語集には、用語や略語の一覧および定義が記載されています。

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMP708AQDBVRQ1	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	708Q
TMP708AQDBVRQ1.B	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	708Q

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TMP708-Q1 :

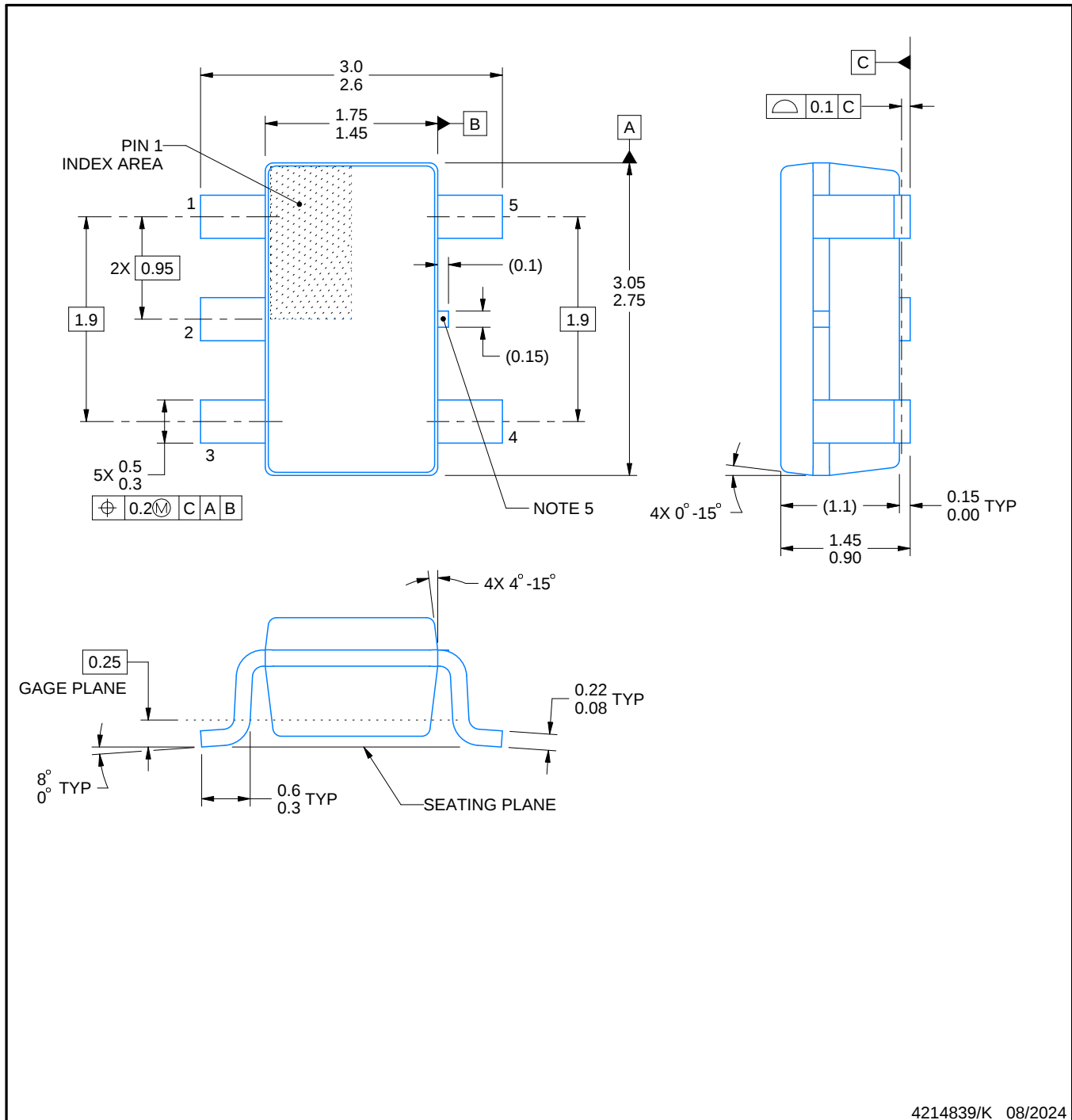
- Catalog : [TMP708](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

DBV0005A**PACKAGE OUTLINE****SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR



4214839/K 08/2024

NOTES:

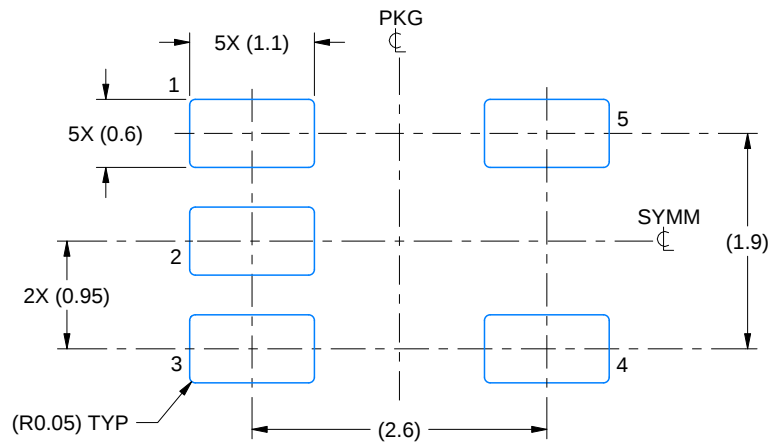
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

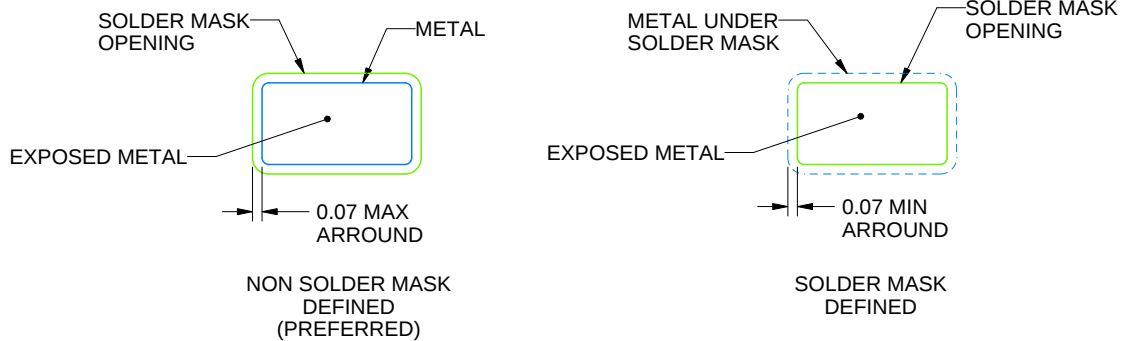
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

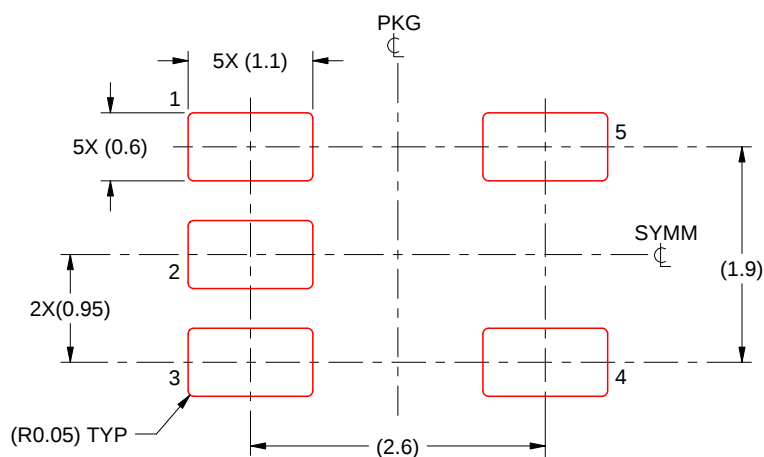
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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