参考資料

TMP411-Q1 N 係数および直列抵抗補正機能付き ±1℃リモート / ローカル温度センサ

1 特長

- 車載アプリケーション用に認定済み
- 下記内容で AEC-Q100 認定済み
  - デバイス温度グレード 1:-40℃～125℃の周囲動作温度範囲
  - デバイス HBM ESD 分類レベル H2
  - デバイス CDM ESD 分類レベル C4B
- ±1℃のリモート ダイオード センサ
- ±1℃ のローカル温度センサ
- プログラム可能な非理想係数
- 直列抵抗のキャンセル
- アラート機能
- プログラム可能な分解能:9～12 ビット
- スレッショルド値をプログラム可能
- 2 線式 / SMBus™ シリアル インターフェイス
- 最高および最低温度モニタ
- 複数のインターフェイス アドレス
- ALERT/ THERM2 ピン構成
- ダイオードのフォルト検出

2 アプリケーション

- 先進運転支援システム (ADAS)
- ボディ エレクトロニクス / ライティング
- ハイブリッド、電気、パワートレイン システム
- インフォテインメント / クラスタ
  - ヘッド ユニット / デジタル コックピット
  - オートモーティブ ディスプレイ
- エンタープライズ システム
- プロセッサおよび FPGA の温度監視

3 概要

TMP411-Q1 デバイスは、ローカル温度センサを内蔵したリモート温度センサ モニタです。リモート温度センサのダイオード接続トランジスタは、一般に低コストな NPN 型または PNP 型トランジスタまたはダイオードであり、これらはマイクロコントローラ、マイクロプロセッサ、または FPGA に不可欠な要素です。

複数の IC 製造元についてリモート精度 ±1℃で、較正は必要ありません。2 線式シリアル インターフェイスは SMBus のバイト書き込み、バイト読み取り、バイト送信、バイト受信の各コマンドを受け付け、アラーム スレッショルドのプログラミングや温度データの読み取り出しが可能です。

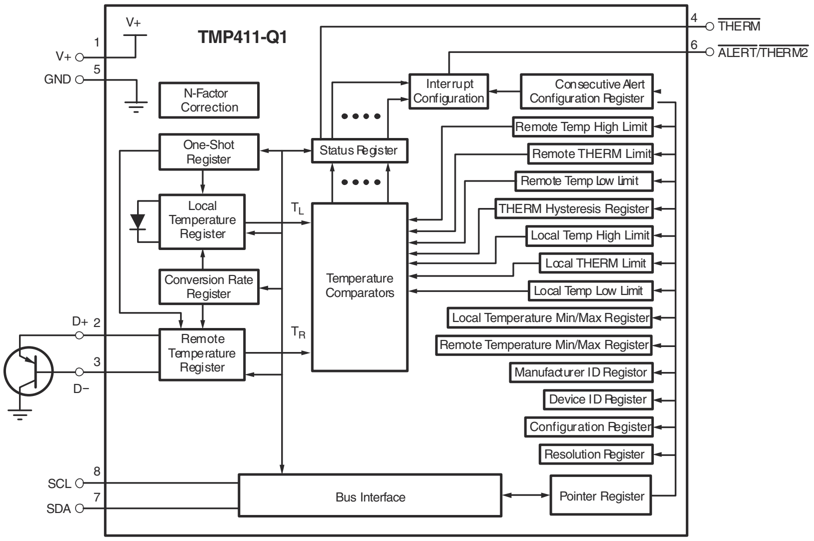
TMP411-Q1 には、直列抵抗の相殺、プログラム可能な非理想係数、プログラム可能な分解能、プログラム可能なスレッショルド値、最低温度と最高温度のモニタ、広いリモート温度測定範囲 (最高 150℃)、ダイオード フォルト検出、温度アラート機能などの機能が搭載されています。

TMP411-Q1 は、VSSOP-8 パッケージで供給されます。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
TMP411-Q1	DGK (VSSOP、8)	3.00mm × 4.90mm

(1) 供給されているすべてのパッケージについては、セクション 13 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



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4 Device Comparison

ORDERABLE PART NUMBER	I^{2}C ADDRESS	DEFAULT LOCAL HIGH TEMPERATURE LIMIT	DEFAULT REMOTE HIGH TEMPERATURE LIMIT	DEFAULT TEMPERATURE RANGE
TMP411AQDGKRQ1	100 1100	+85°C	+85°C	Standard
TMP411BQDGKRQ1	100 1101	+85°C	+85°C	Standard
TMP411CQDGKRQ1	100 1110	+85°C	+85°C	Standard
TMP411DQDGKRQ1	100 1100	+110°C	+110°C	Standard

5 Pin Configuration and Functions

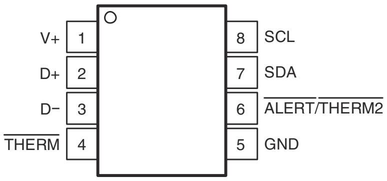


図 5-1. DGK Package 8-Pin VSSOP (TOP VIEW)

Pin Functions

PIN	NAME	Type(1)	DESCRIPTION
1	V+	I	Positive supply (2.7V to 5.5V)
2	D+	I	Positive connection to remote temperature sensor
3	D−	I	Negative connection to remote temperature sensor
4	$\overline{\text{THERM}}$	O	Thermal flag, active-low, open-drain; requires pullup resistor to V+
5	GND	G	Ground
6	$\overline{\text{ALERT}}$/ $\overline{\text{THERM2}}$	O	Alert (reconfigurable as second thermal flag), active-low, open-drain; requires pullup resistor to V+
7	SDA	I/O	Serial data line for SMBus, open-drain; requires pullup resistor to V+
8	SCL	I	Serial clock line for SMBus, open-drain; requires pullup resistor to V+

(1) O = Output, I = Input; I/O = Input or Output; G = Ground

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	Pins 2, 3 only	–0.5	2	V
Input voltage	Pins 4, 6, 7, 8 only	–0.5	6	V
Input current			10	mA
Power supply, V+			7	V
Operating temperature range		–55	127	°C
Junction temperature, $T_{J(max)}$			150	°C
Storage temperature, T_{stg}		–60	130	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 2	±3000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±1000	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V+	Supply voltage	2.7	3.3	5.5	V
T_A	Operating free-air temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TMP411-Q1 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	161.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	71.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	96.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	9.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	95.0	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

6.5 Electrical Characteristics

At T_A = -40°C to +125°C and V+ = 2.7V to 5.5V, over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE ERROR							
$T_{ERROR(LOCAL)}$	Local temperature sensor		T_A = -40°C to 125°C	–2.5	±1.25	2.5	°C
			T_A = 15°C to 85°C V+ = 3.3V	–1	±0.0625	1	
$T_{ERROR(REMOTE)}$	Remote temperature sensor(1)		T_A = 15°C to 75°C T_{DIODE} = -40°C to 150°C V+ = 3.3V	–1	±0.0625	1	°C
			T_A = -40°C to 100°C T_{DIODE} = -40°C to 150°C V+ = 3.3V	–3	±1	3	
			T_A = -40°C to 125°C T_{DIODE} = -40°C to 150°C V+ = 3.3V	–5	±3	5	
T_{ERROR_PS}	Temperature error power supply sensitivity (local and remote)		V+ = 2.7V to 5.5V T_{DIODE} = -40°C to 150°C	–0.5	±0.2	0.5	°C/V
TEMPERATURE MEASUREMENT							
	Conversion time		One-Shot mode	30	35	40	ms
	Resolution	Local temperature sensor (programmable)		9		12	Bits
		Remote temperature sensor			12		
	Remote sensor source current	High	Series resistance: 3kΩ maximum		120		µA
		Medium			60		
		Low			6		
η	Remote transistor ideality factor		Optimized ideality factor		1.008		
SMBus INTERFACE							
V_{IH}	Logic input high voltage (SCL, SDA)			2.1			V
V_{IL}	Logic input low voltage (SCL, SDA)					0.8	V
	Hysteresis				170		mV
	SMBus output low sink current			6			mA
	Logic input current			–1		1	µA
	SMBus input capacitance (SCL, SDA)				3		pF
	SMBus clock frequency					3.4	MHz
	SMBus timeout			25	30	35	ms
	SCL falling edge to SDA valid time					1	µs
DIGITAL OUTPUTS							
V_{OL}	Output low voltage		I_{OUT} = 6mA		0.15	0.4	V
I_{OH}	High-level output leakage current		V_{OUT} = V+		0.1	1	µA
	$\overline{\text{ALERT}}$ or $\overline{\text{THERM2}}$ output low sink current		$\overline{\text{ALERT}}/\overline{\text{THERM2}}$ forced to 0.4V	6			mA
	$\overline{\text{THERM}}$ output low sink current		$\overline{\text{THERM}}$ forced to 0.4V	6			mA
POWER SUPPLY							
V+	Specific voltage range			2.7		5.5	V

At T_A = -40°C to +125°C and V+ = 2.7V to 5.5V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_Q	Quiescent current	0.0625 conversions per second V+ = 3.3V		1.5	5.5	μA
		Eight conversions per second V+ = 3.3V		45	70	
		Serial bus inactive, shutdown mode		3	5	
		Serial bus active, f_s = 400kHz, Shutdown mode		9		
		Serial bus active, f_s = 3.4MHz, Shutdown mode		60		
	Undervoltage lockout (2)	There is no limitation on this specification, please see the footnote (2)				V
POR	Power-on-reset threshold			1.23	1.4	V
	Brownout detect		1	1.14		

(1) Tested with less than 5Ω effective series resistance and 100pF differential input capacitance. T_A is the ambient temperature of the TMP411-Q1. T_{DIODE} is the temperature at the remote diode sensor.

(2) When there is no remote diode connected, the first remote conversion should be ignored with the power supply ramp rate less than 240V/s.

6.6 Timing Characteristics

		FAST MODE		HIGH-SPEED MODE		UNIT
		MIN	MAX	MIN	MAX	
$f_{(SCL)}$	SCL operating frequency	0.001	0.4	0.001	3.4	MHz
$t_{(BUF)}$	Bus free time between STOP and START condition	600		160		ns
$t_{(HDSTA)}$	Hold time after repeated START condition. After this period, the first clock is generated.	100		100		ns
$t_{(SUSTA)}$	Repeated START condition setup time	100		100		ns
$t_{(SUSTO)}$	STOP condition setup time	100		100		ns
$t_{(HDDAT)}$	Data hold time	0(1)		0(2)		ns
$t_{(SUDAT)}$	Data setup time	100		20		ns
$t_{(LOW)}$	SCL clock LOW period	1300		160		ns
$t_{(HIGH)}$	SCL clock HIGH period	600		60		ns
t_F	Clock and data fall time		300		160	ns
t_R	Clock and data rise time		300		160	ns
	SCLK ≤ 100kHz		1000			ns

(1) For cases with an SCL fall time of less than 20ns, or an SDA rise or fall time of less than 20ns, the hold time must be greater than 20ns.

(2) For cases with an SCL fall time of less than 10ns, or an SDA rise or fall time of less than 10ns, the hold time must be greater than 10ns.

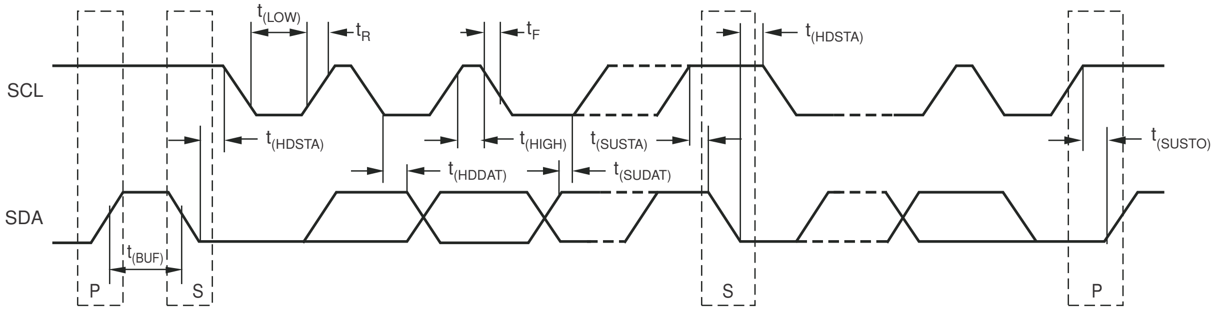


図 6-1. Two-Wire Timing Diagram

7 Typical Characteristics

At T_A = 25°C and V+ = V_S = 5V, unless otherwise noted.

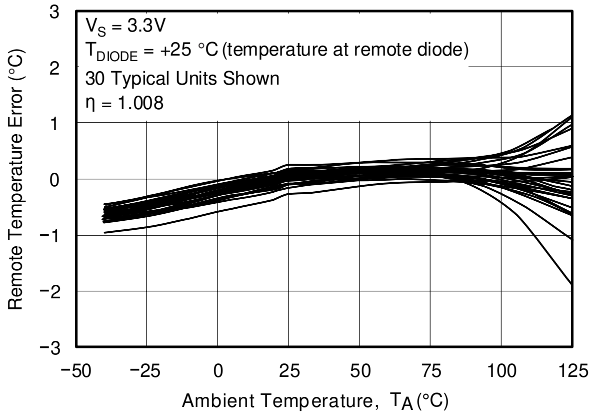


図 7-1. Remote Temperature Error vs TMP411-Q1 Ambient Temperature

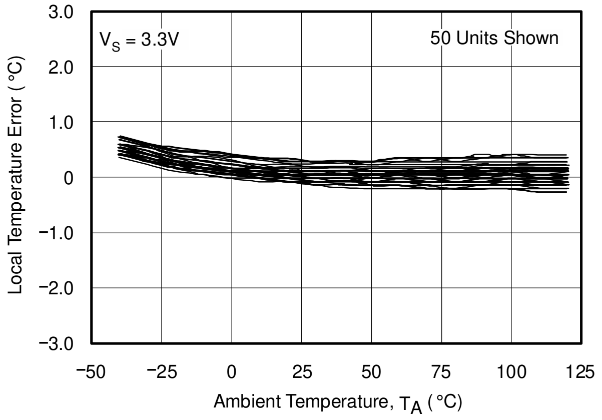


図 7-2. Local Temperature Error vs TMP411-Q1 Ambient Temperature

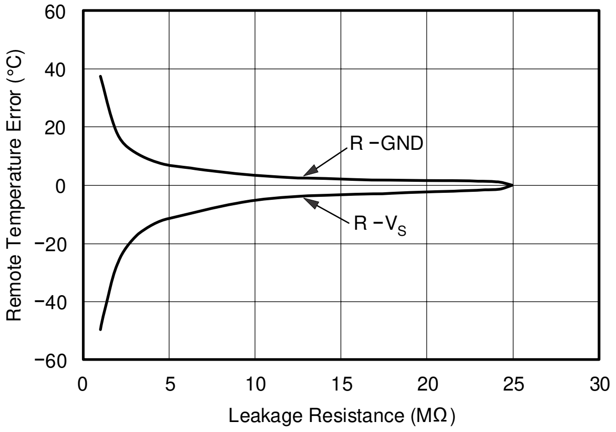


図 7-3. Remote Temperature Error vs Leakage Resistance

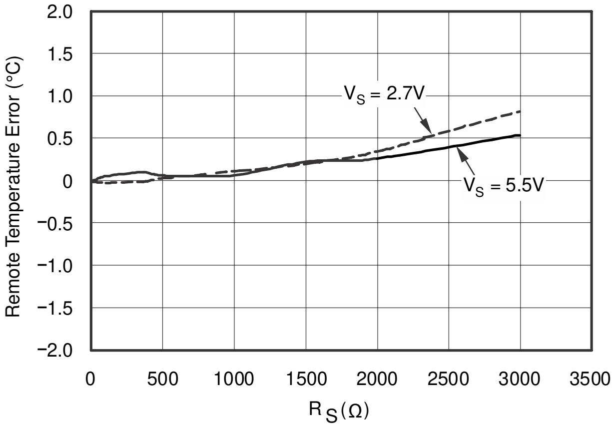


図 7-4. Remote Temperature Error vs Series Resistance (Diode-Connected Transistor, 2N3906 PNP)

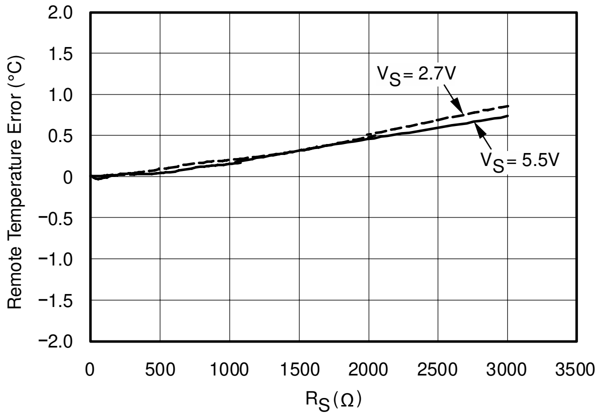


図 7-5. Remote Temperature Error vs Series Resistance (GND Collector-Connected Transistor, 2N3906 PNP)

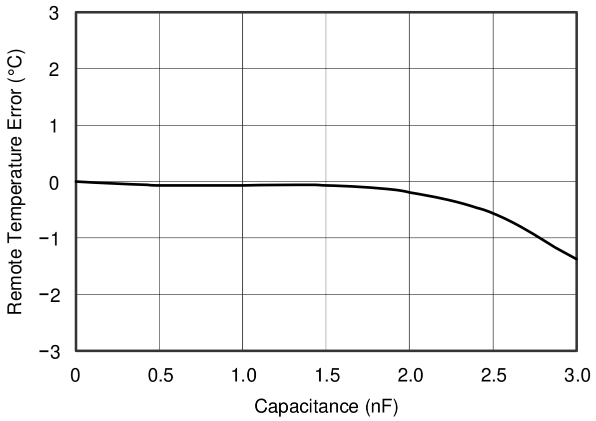


図 7-6. Remote Temperature Error vs Differential Capacitance

7 Typical Characteristics (continued)

At T_A = 25°C and V+ = V_S = 5V, unless otherwise noted.

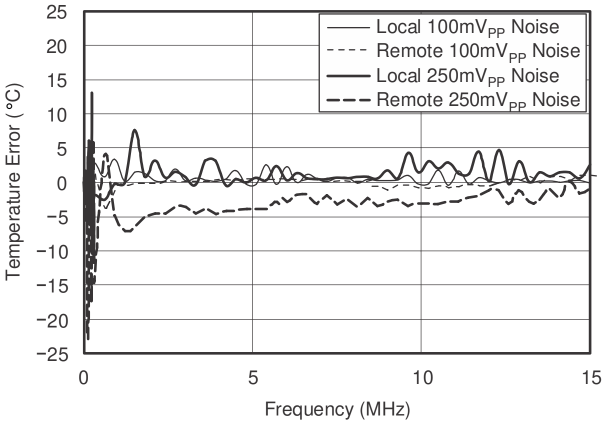


図 7-7. Temperature Error vs Power-Supply Noise Frequency

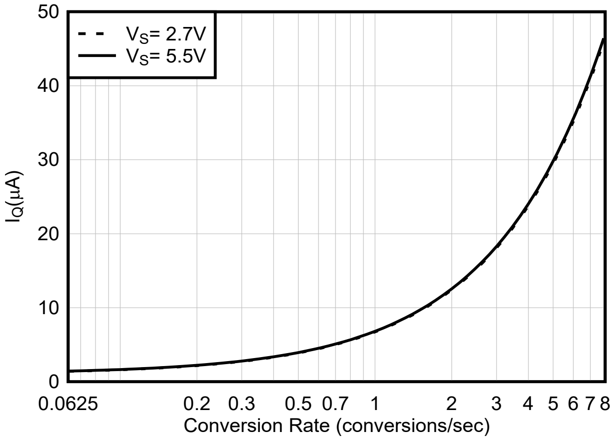


図 7-8. Quiescent Current vs Conversion Rate

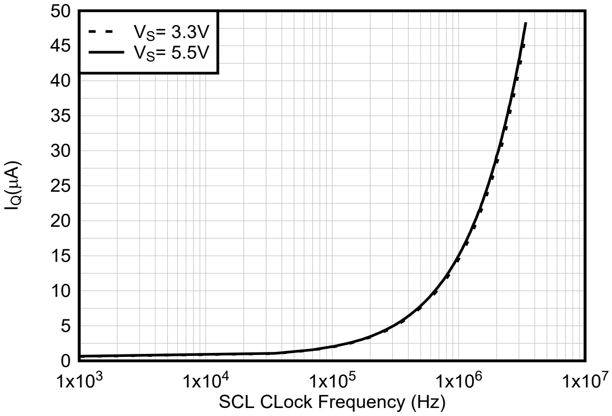


図 7-9. Shutdown Quiescent Current vs SCL Clock Frequency

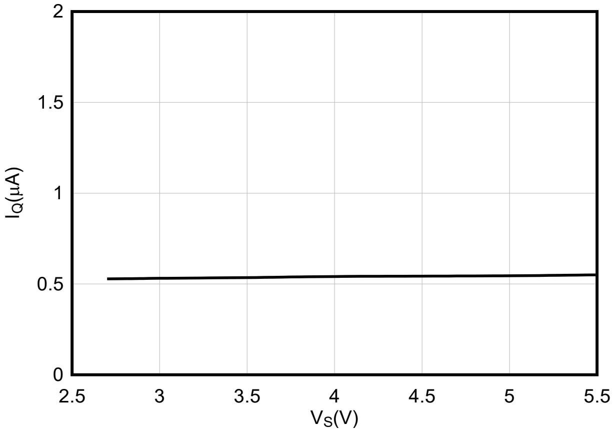


図 7-10. Shutdown Quiescent Current vs Supply Voltage

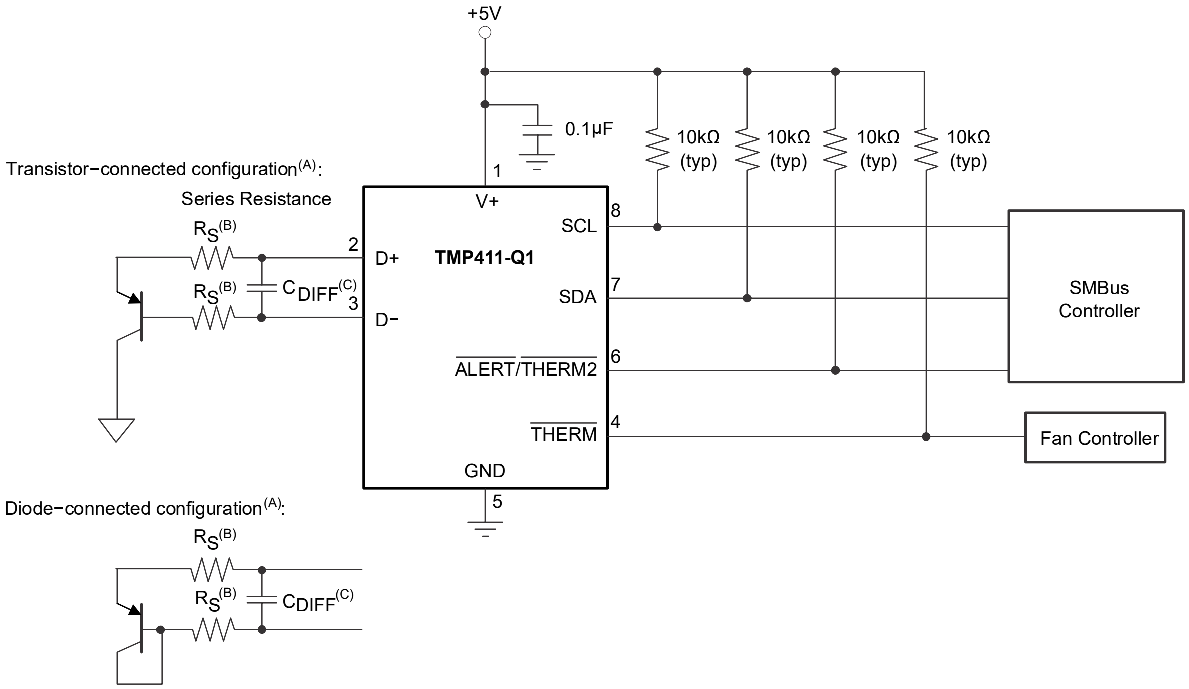
8 Detailed Description

8.1 Overview

The TMP411-Q1 is a dual-channel digital temperature sensor that combines a local die-temperature measurement channel and a remote junction-temperature measurement channel in a single VSSOP-8 package. The TMP411-Q1 is two-wire- and SMBus interface-compatible and is specified over an ambient temperature range of −40°C to 125°C. The TMP411-Q1 contains multiple registers for holding configuration information, temperature measurement results, temperature comparator maximum/minimum limits, and status information.

User-programmed high- and low-temperature limits stored in the TMP411-Q1 can be used to trigger an over- or undertemperature alarm (ALERT) on local and remote temperatures. Additional thermal limits can be programmed into the TMP411-Q1 and used to trigger another flag (THERM) that can be used to initiate a system response to rising temperatures.

The TMP411-Q1 requires only a transistor connected between D+ and D− for proper remote temperature-sensing operation. The SCL and SDA interface pins require pullup resistors as part of the communication bus, whereas ALERT and THERM are open-drain outputs that also need pullup resistors. ALERT and THERM can be shared with other devices if desired for a wired-OR implementation. A 0.1µF power-supply bypass capacitor is recommended for good local bypassing. 図 8-1 shows a typical configuration for the TMP411-Q1.



A. Diode−connected configuration provides better settling time. Transistor−connected configuration provides better series resistance cancellation.

B. R_S (optional) must be < 1.5kΩ in most applications. Selection of R_S depends on specific application; see Filtering section.

C. C_{DIFF} (optional) must be < 1000pF in most applications. Selection of C_{DIFF} depends on specific application; see Filtering section and 図 7-6, *Remote Temperature Error vs Differential Capacitance*.

図 8-1. Basic Connections

8.2 Functional Block Diagram

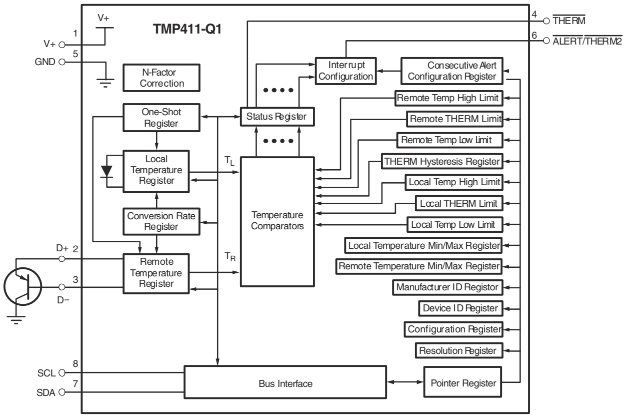


図 8-2. Functional Block Diagram

8.3 Feature Description

8.3.1 Series Resistance Cancellation

Series resistance in an application circuit that typically results from printed circuit board (PCB) trace resistance and remote line length (see 図 8-1) is automatically canceled by the TMP411-Q1, preventing what otherwise results in a temperature offset.

A total of up to 3kΩ of series line resistance is canceled by the TMP411-Q1, eliminating the need for additional characterization and temperature offset correction.

See the two Remote Temperature Error vs Series Resistance typical characteristics curves (図 7-4 and 図 7-5) for details on the effect of series resistance and power-supply voltage on sensed remote temperature error.

8.3.2 Differential Input Capacitance

The TMP411-Q1 tolerates differential input capacitance of up to 1000pF with minimal change in temperature error. The effect of capacitance on sensed remote temperature error is illustrated in typical characteristic Remote Temperature Error vs Differential Capacitance (図 7-6).

8.3.3 Temperature Measurement Data

Temperature measurement data are taken over a default range of 0°C to 127°C for both local and remote locations. Measurements from –55°C to 150°C can be made both locally and remotely by reconfiguring the TMP411-Q1 for the extended temperature range. To change the TMP411-Q1 configuration from the standard to the extended temperature range, switch bit 2 (RANGE) of the Configuration Register from low to high.

Temperature data resulting from conversions within the default measurement range are represented in binary form, as shown in 表 8-1, Standard Binary column. Note that any temperature below 0°C results in a data value of zero (00h). Likewise, temperatures above 127°C result in a value of 127 (7Fh). The device can be set to measure over an extended temperature range by changing bit 2 of the Configuration Register from low to high. The change in measurement range and data format from standard binary to extended binary occurs at the next temperature conversion. For data captured in the extended temperature range configuration, an offset of 64 (40h) is added to the standard binary value, as shown in 表 8-1, Extended Binary column. This configuration allows measurement of temperatures below 0°C. Note that binary values corresponding to temperatures as low as –64°C, and as high as 191°C are possible; however, most temperature-sensing diodes only measure with the range of –55°C to 150°C. Additionally, the TMP411-Q1 is rated only for ambient local temperatures ranging from –40°C to 125°C. Parameters in the Absolute Maximum Ratings table must be observed.

表 8-1. Temperature Data Format (Local and Remote Temperature High Bytes)

TEMP (°C)	LOCAL/REMOTE TEMPERATURE REGISTER HIGH BYTE VALUE (1°C RESOLUTION)			
	STANDARD BINARY		EXTENDED BINARY	
	BINARY	HEX	BINARY	HEX
−64	0000 0000	00	0000 0000	00
−50	0000 0000	00	0000 1110	0E
−25	0000 0000	00	0010 0111	27
0	0000 0000	00	0100 0000	40
1	0000 0001	01	0100 0001	41
5	0000 0101	05	0100 0101	45
10	0000 1010	0A	0100 1010	4A
25	0001 1001	19	0101 1001	59
50	0011 0010	32	0111 0010	72
75	0100 1011	4B	1000 1011	8b
100	0110 0100	64	1010 0100	A4
125	0111 1101	7D	1011 1101	BD
127	0111 1111	7F	1011 1111	BF
150	0111 1111	7F	1101 0110	D6
175	0111 1111	7F	1110 1111	EF
191	0111 1111	7F	1111 1111	FF

注

Whenever changing between standard and extended temperature ranges, be aware that the temperatures stored in the temperature limit registers are NOT automatically reformatted to correspond to the new temperature range format. These temperature limit values must be reprogrammed in the appropriate binary or extended binary format.

Both local and remote temperature data use two bytes for data storage. The high byte stores the temperature with 1°C resolution. The second or low byte stores the decimal fraction value of the temperature and allows a higher measurement resolution; see 表 8-2. The measurement resolution for the remote channel is 0.0625°C, and is not adjustable. The measurement resolution for the local channel is adjustable; the resolution can be set for 0.5°C, 0.25°C, 0.125°C, or 0.0625°C by setting the RES1 and RES0 bits of the Resolution Register; see the Resolution Register section.

表 8-2. Decimal Fraction Temperature Data Format (Local and Remote Temperature Low Bytes)

TEMP (°C)	REMOTE TEMPERATURE REGISTER LOW BYTE VALUE		LOCAL TEMPERATURE REGISTER LOW BYTE VALUE							
	0.0625°C RESOLUTION		0.5°C RESOLUTION		0.25°C RESOLUTION		0.125°C RESOLUTION		0.0625°C RESOLUTION	
	STANDARD AND EXTENDED BINARY	HEX	STANDARD AND EXTENDED BINARY	HEX	STANDARD AND EXTENDED BINARY	HEX	STANDARD AND EXTENDED BINARY	HEX	STANDARD AND EXTENDED BINARY	HEX
0.0000	0000 0000	00	0000 0000	00	0000 0000	00	0000 0000	00	0000 0000	00
0.0625	0001 0000	10	0000 0000	00	0000 0000	00	0000 0000	00	0001 0000	10
0.1250	0010 0000	20	0000 0000	00	0000 0000	00	0010 0000	20	0010 0000	20
0.1875	0011 0000	30	0000 0000	00	0000 0000	00	0010 0000	20	0011 0000	30

表 8-2. Decimal Fraction Temperature Data Format (Local and Remote Temperature Low Bytes) (続き)

TEMP (°C)	REMOTE TEMPERATURE REGISTER LOW BYTE VALUE		LOCAL TEMPERATURE REGISTER LOW BYTE VALUE							
	0.0625°C RESOLUTION		0.5°C RESOLUTION		0.25°C RESOLUTION		0.125°C RESOLUTION		0.0625°C RESOLUTION	
	STANDARD AND EXTENDED BINARY	HEX	STANDARD AND EXTENDED BINARY	HEX	STANDARD AND EXTENDED BINARY	HEX	STANDARD AND EXTENDED BINARY	HEX	STANDARD AND EXTENDED BINARY	HEX
0.2500	0100 0000	40	0000 0000	00	0100 0000	40	0100 0000	40	0100 0000	40
0.3125	0101 0000	50	0000 0000	00	0100 0000	40	0100 0000	40	0101 0000	50
0.3750	0110 0000	60	0000 0000	00	0100 0000	40	0110 0000	60	0110 0000	60
0.4375	0111 0000	70	0000 0000	00	0100 0000	40	0110 0000	60	0111 0000	70
0.5000	1000 0000	80	1000 0000	80	1000 0000	80	1000 0000	80	1000 0000	80
0.5625	1001 0000	90	1000 0000	80	1000 0000	80	1000 0000	80	1001 0000	90
0.6250	1010 0000	A0	1000 0000	80	1000 0000	80	1010 0000	A0	1010 0000	A0
0.6875	1011 0000	B0	1000 0000	80	1000 0000	80	1010 0000	A0	1011 0000	B0
0.7500	1100 0000	C0	1000 0000	80	1100 0000	C0	1100 0000	C0	1100 0000	C0
0.8125	1101 0000	D0	1000 0000	80	1100 0000	C0	1100 0000	C0	1101 0000	D0
0.8750	1110 0000	E0	1000 0000	80	1100 0000	C0	1110 0000	E0	1110 0000	E0
0.9375	1111 0000	F0	1000 0000	80	1100 0000	C0	1110 0000	E0	1111 0000	F0

8.3.4 THERM (PIN 4) and ALERT/ THERM2 (PIN 6)

The TMP411-Q1 has two pins dedicated to alarm functions, the THERM and ALERT/ THERM2 pins. Both pins are open-drain outputs that each require a pullup resistor to V+. These pins can be wire-ORed together with other alarm pins for system monitoring of multiple sensors. The THERM pin provides a thermal interrupt that cannot be software-disabled. The ALERT pin is intended for use as an earlier warning interrupt, and can be software disabled, or masked. The ALERT/ THERM2 pin can also be configured for use as THERM2, a second THERM pin (Configuration Register: AL/TH bit = 1). The default setting configures pin 6 to function as ALERT (AL/TH = 0).

The THERM pin asserts low when either the measured local or remote temperature is outside of the temperature range programmed in the corresponding Local or Remote THERM Limit Register. The THERM temperature limit range can be programmed with a wider range than that of the limit registers, which allows ALERT to provide an earlier warning than THERM. The THERM alarm resets automatically when the measured temperature returns to within the THERM temperature limit range minus the hysteresis value stored in the THERM Hysteresis Register. The allowable values of hysteresis are shown in 表 9-8. The default hysteresis is 10°C. When the ALERT/ THERM2 pin is configured as a second thermal alarm (Configuration Register: bit 7 = 0, bit 5 = 1), the pin functions the same as THERM, but uses the temperatures stored in the Local/Remote Temperature High/Low Limit Registers to set the comparison range.

When ALERT/ THERM2 (pin 6) is configured as ALERT (Configuration Register: bit 7 = 0, bit 5 = 0), the pin asserts low when either the measured local or remote temperature violates the range limit set by the corresponding Local/Remote Temperature High/Low Limit Registers. This alert function can be configured to assert only if the range is violated a specified number of consecutive times (1, 2, 3, or 4). The consecutive violation limit is set in the Consecutive Alert Register. False alerts that occur as a result of environmental noise can be prevented by requiring consecutive faults. ALERT also asserts low if the remote temperature sensor is open-circuit. When the MASK function is enabled (Configuration Register: bit 7 = 1), ALERT is disabled (that is, masked). ALERT resets when the controller reads the device address, as long as the condition that caused the alert no longer persists, and the Status Register has been reset.

8.3.5 Sensor Fault

The TMP411-Q1 senses a fault at the D+ input resulting from incorrect diode connection or an open circuit. The detection circuitry consists of a voltage comparator that trips when the voltage at D+ exceeds (V+) − 0.6V (typical). The comparator output is continuously checked during a conversion. If a fault is detected, the last valid measured temperature is used for the temperature measurement result, the OPEN bit (Status Register, bit 2) is set high, and, if the alert function is enabled, $\overline{\text{ALERT}}$ asserts low.

When not using the remote sensor with the TMP411-Q1, the D+ and D− inputs must be connected together to prevent meaningless fault warnings.

8.3.6 Undervoltage Lockout

There is no limitation on the Undervoltage lockout. However, when there is no remote diode connected, the first remote conversion should be ignored with the power supply ramp rate less than 240V/s.

8.3.7 Filtering

Remote junction temperature sensors are typically implemented in a noisy environment. Noise is most often created by fast digital signals, and noise can corrupt measurements. The TMP411-Q1 has a built-in 65kHz filter on the inputs of D+ and D− to minimize the effects of noise. However, a bypass capacitor placed differentially across the inputs of the remote temperature sensor is recommended to make the application more robust against unwanted coupled signals. The value of the capacitor must be between 100pF and 1nF. Some applications attain better overall accuracy with additional series resistance; however, this increased accuracy is setup-specific. When series resistance is added, the value must not be greater than 3kΩ.

If filtering is needed, the suggested component values are 100pF and 50Ω on each input. Exact values are application-specific.

8.4 Device Functional Modes

8.4.1 Shutdown Mode (SD)

The TMP411-Q1 shutdown mode allows the user to save maximum power by shutting down all device circuitry other than the serial interface, reducing current consumption to typically less than 3μA; see typical characteristic curve Shutdown Quiescent Current vs Supply Voltage. Shutdown mode is enabled when the SD bit of the Configuration Register is high; the device shuts down once the current conversion is completed. When SD is low, the device maintains a continuous conversion state.

8.4.2 One-shot Conversion

When the TMP411-Q1 is in shutdown mode (SD = 1 in the Configuration Register), a single conversion on both channels is started by writing any value to the One-Shot Start Register, pointer address 0Fh. This write operation starts one conversion; the TMP411-Q1 returns to shutdown mode when that conversion completes. The value of the data sent in the write command is irrelevant and is not stored by the TMP411-Q1. When the TMP411-Q1 is in shutdown mode, an initial 200μs is required before a one-shot command can be given. (NOTE: When a shutdown command is issued, the TMP411-Q1 completes the current conversion before shutting down.) This wait time only applies to the 200μs immediately following shutdown. One-shot commands can be issued without delay thereafter.

8.5 Programming

8.5.1 Serial Interface

The TMP411-Q1 operates only as a target device on either the two-wire bus or the SMBus. Connections to either bus are made via the open-drain I/O lines, SDA and SCL. The SDA and SCL pins feature integrated spike suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. The TMP411-Q1 supports the transmission protocol for fast (1kHz to 400kHz) and high-speed (1kHz to 3.4MHz) modes. All data bytes are transmitted MSB-first.

8.5.2 Bus Overview

The TMP411-Q1 is SMBus interface-compatible. In SMBus protocol, the device that initiates the transfer is called a controller, and the devices controlled by the controller are targets. The bus must be controlled by a controller device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions.

To address a specific device, a START condition is initiated. START is indicated by pulling the data line (SDA) from a high to low logic level while SCL is high. All targets on the bus shift in the target address byte, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the target being addressed responds to the controller by generating an Acknowledge and pulling SDA low.

Data transfer is then initiated and sent over eight clock pulses followed by an Acknowledge bit. During data transfer, SDA must remain stable while SCL is high, because any change in SDA while SCL is high is interpreted as a control signal.

Once all data has been transferred, the controller generates a STOP condition. STOP is indicated by pulling SDA from low to high while SCL is high

8.5.3 Timing Diagrams

The TMP411-Q1 is two-wire and SMBus-compatible. 図 8-3 to 図 8-6 describe the various operations on the TMP411-Q1. Bus definitions are given as follows:

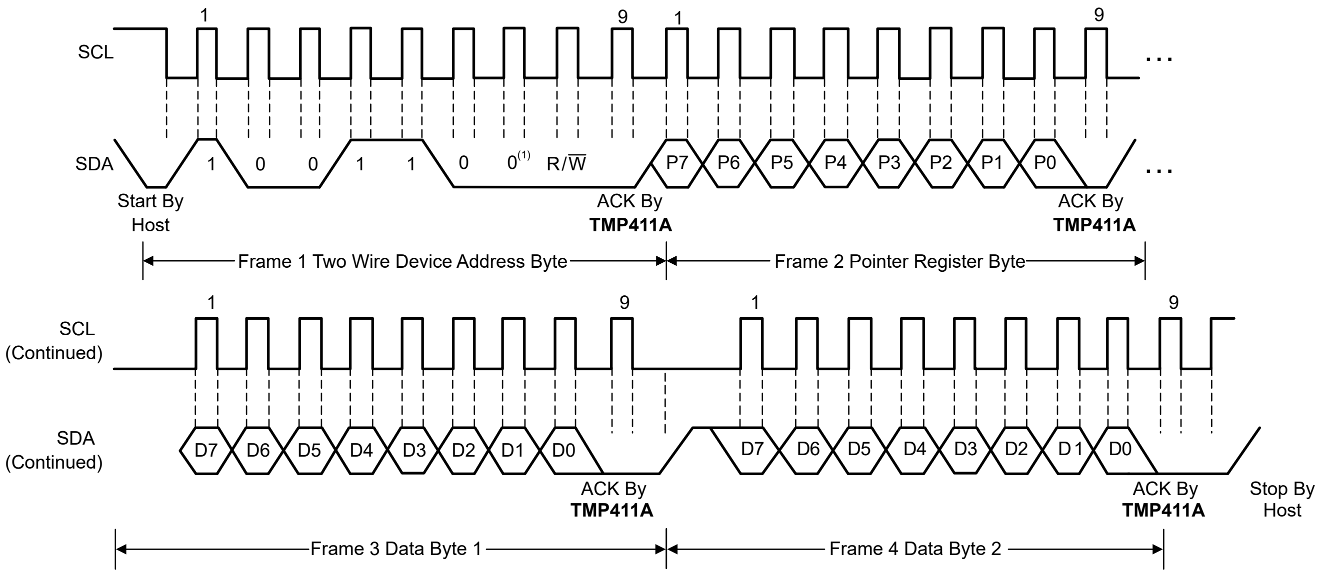
Bus Idle: Both SDA and SCL lines remain high.

Start Data Transfer: A change in the state of the SDA line, from high to low, while the SCL line is high, defines a START condition. Each data transfer is initiated with a START condition.

Stop Data Transfer: A change in the state of the SDA line from low to high while the SCL line is high defines a STOP condition. Each data transfer terminates with a STOP or a repeated START condition.

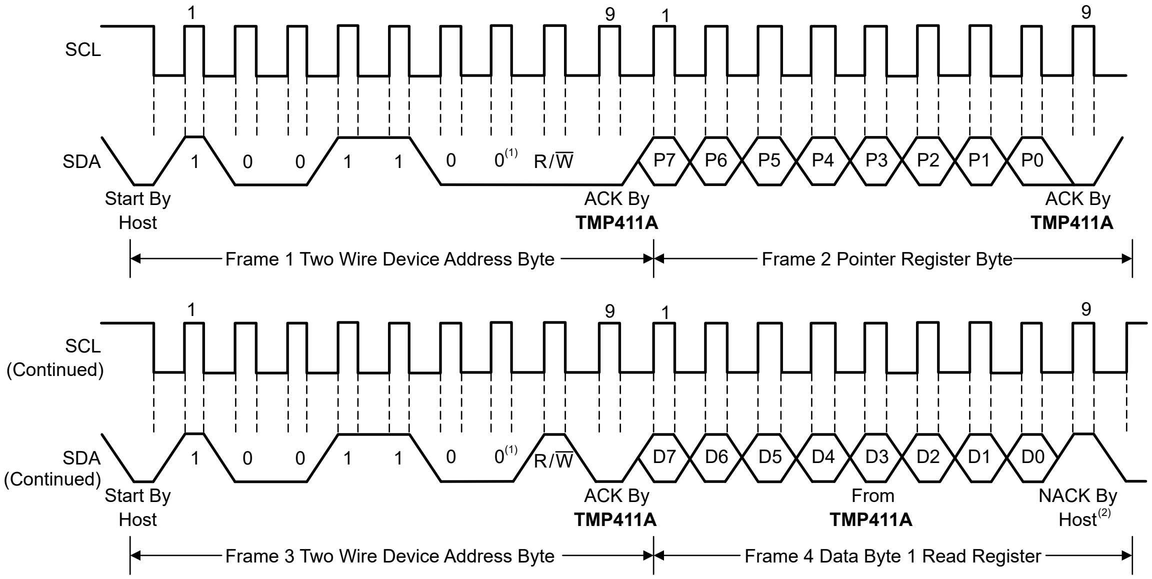
Data Transfer: The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the controller device. The receiver acknowledges the transfer of data.

Acknowledge: Each receiving device, when addressed, is obliged to generate an Acknowledge bit. A device that acknowledges must pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the Acknowledge clock pulse. Setup and hold times must be taken into account. On a controller receive, data transfer termination can be signaled by the controller generating a Not-Acknowledge on the last byte that has been transmitted by the target.



A. Target address 1001 100 (TMP411A and TMP411D) shown. Target address changes for TMP411B and TMP411C. See Ordering Information table for more details.

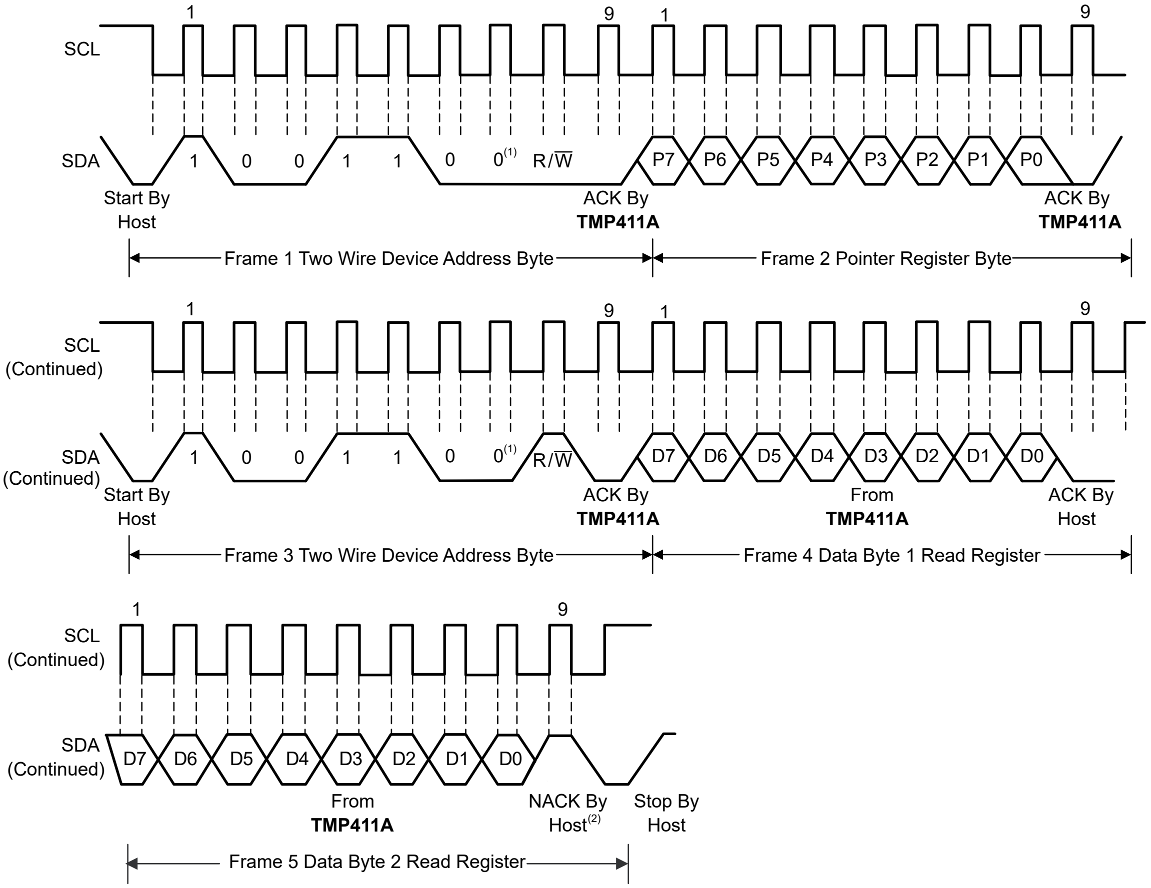
図 8-3. Two-Wire Timing Diagram for Write Word Format



A. Target address 1001 100 (TMP411A and TMP411D) shown

B. Host must leave SDA high to terminate a single-byte read operation.

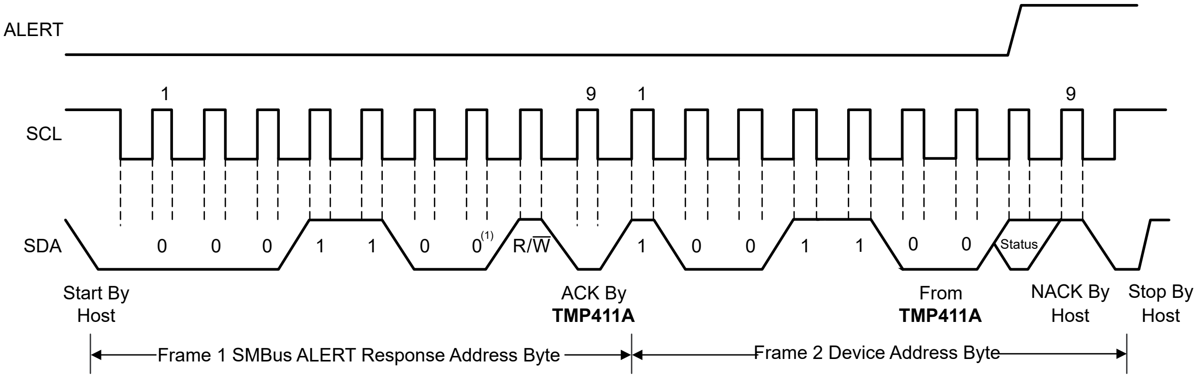
図 8-4. Two-Wire Timing Diagram for Single-Byte Read Format



A. Target address 1001 100 (TMP411A and TMP411D) shown

B. Host must leave SDA high to terminate a two−byte read operation.

図 8-5. Two-Wire Timing Diagram for Two-Byte Read Format



A. Target address 1001 100 (TMP411A) shown

図 8-6. Timing Diagram for SMBus $\overline{\text{ALERT}}$

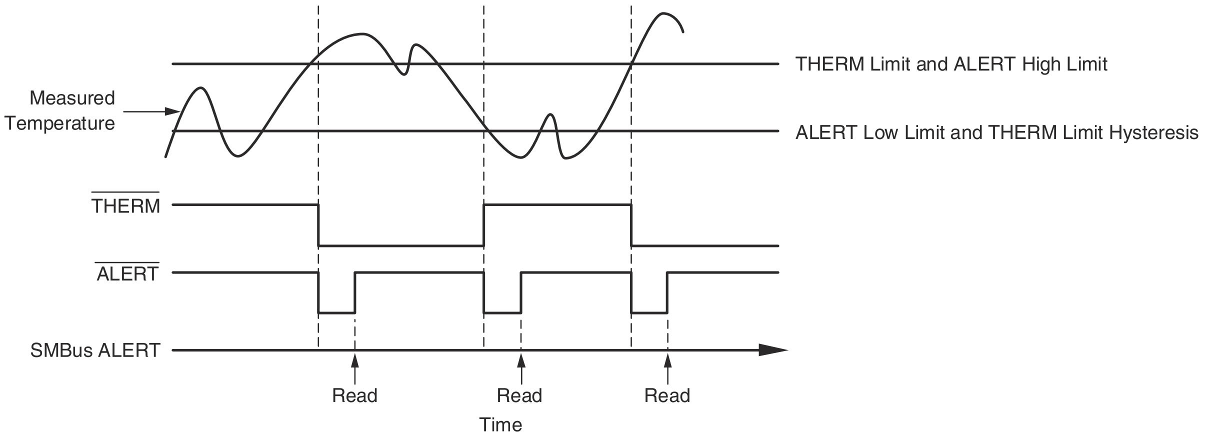


図 8-7. SMBus Alert Timing Diagram

8.5.4 Serial Bus Address

To communicate with the TMP411-Q1, the controller must first address target devices through a target address byte. The target address byte consists of seven address bits and a direction bit that indicates whether the operation is read or write. The address of the TMP411A-Q1 and TMP411D-Q1 is 4Ch (1001100b).

8.5.5 Read/Write Operations

Accessing a particular register on the TMP411-Q1 is accomplished by writing the appropriate value to the Pointer Register. The value for the Pointer Register is the first byte transferred after the target address byte with the R/W bit low. Every write operation to the TMP411-Q1 requires a value for the Pointer Register (see 図 8-3).

When reading from the TMP411-Q1, the last value stored in the Pointer Register by a write operation is used to determine which register is read by a read operation. To change the register pointer for a read operation, a new value must be written to the Pointer Register. This transaction is accomplished by issuing a target address byte with the R/W bit low, followed by the Pointer Register byte. No additional data are required. The controller can then generate a START condition and send the target address byte with the R/W bit high to initiate the read command. See 図 8-4 for details of this sequence. Continually sending the Pointer Register bytes is not necessary if repeated reads from the same register is desired, because the TMP411-Q1 retains the Pointer Register value until the value is changed by the next write operation. Note that register bytes are sent MSB-first, followed by the LSB.

8.5.6 Time-Out Function

When bit 7 of the Consecutive Alert Register is set high, the TMP411-Q1 time-out function is enabled. The TMP411-Q1 resets the serial interface if either SCL or SDA is held low for 30ms (typical) between a START and STOP condition. If the TMP411-Q1 is holding the bus low, the device releases the bus and waits for a START condition. To avoid activating the time-out function, maintain a communication speed of at least 1kHz for the SCL operating frequency. The default state of the time-out function is enabled (bit 7 = high).

8.5.7 High-Speed Mode

For the two-wire bus to operate at frequencies above 400kHz, the controller device must issue a high-speed mode (Hs-mode) controller code (00001XXX) as the first byte after a START condition to switch the bus to high-speed operation. The TMP411-Q1 does not acknowledge this byte, but switches the input filters on SDA and SCL and the output filter on SDA to operate in Hs-mode, allowing transfers at up to 3.4MHz. After the Hs-mode controller code has been issued, the controller transmits a two-wire target address to initiate a data transfer operation. The bus continues to operate in Hs-mode until a STOP condition occurs on the bus. Upon receiving the STOP condition, the TMP411-Q1 switches the input and output filters back to fast-mode operation.

8.5.8 General-Call Reset

The TMP411-Q1 supports reset via the two-wire general-call address 00h (0000 0000b). The TMP411-Q1 acknowledges the general-call address and responds to the second byte. If the second byte is 06h (0000 0110b), the TMP411-Q1 executes a software reset. This software reset restores the power-on-reset state to all TMP411-Q1 registers, aborts any conversion in progress, and clears the $\overline{\text{ALERT}}$ and $\overline{\text{THERM}}$ pins. The TMP411-Q1 takes no action in response to other values in the second byte.

8.5.9 Software Reset

The TMP411-Q1 resets by writing any value to Pointer Register FCh. This restores the power-on-reset state to all of the TMP411-Q1 registers, aborts any conversion in process, and clears the $\overline{\text{ALERT}}$ and $\overline{\text{THERM}}$ pins.

8.5.10 SMBUS Alert Function

The TMP411-Q1 supports the SMBus alert function. When pin 6 is configured as an alert output, the $\overline{\text{ALERT}}$ pin of the TMP411-Q1 can be connected as an SMBus alert signal. When a controller detects an alert condition on the $\overline{\text{ALERT}}$ line, the controller sends an SMBus alert command (0001 1001) on the bus. If the $\overline{\text{ALERT}}$ pin of the TMP411-Q1 is active, the device acknowledges the SMBus alert command and responds by returning the target address on the SDA line. The eighth bit (LSB) of the target address byte indicates whether the temperature exceeding one of the temperature high limit settings or falling below one of the temperature low limit settings caused the alert condition. The bit is high if the temperature is greater than or equal to one of the temperature high-limit settings; this bit is low if the temperature is less than one of the temperature low-limit settings. See 図 8-6 for details of this sequence.

If multiple devices on the bus respond to the SMBus alert command, arbitration during the target address portion of the SMBus alert command determines which device clears the alert status. If the TMP411-Q1 wins the arbitration, the $\overline{\text{ALERT}}$ pin becomes inactive at the completion of the SMBus alert command. If the TMP411-Q1 loses the arbitration, the $\overline{\text{ALERT}}$ pin remains active.

9 Register Map

表 9-1. Register Map Summary

POINTER ADDRESS (HEX)		POWER-ON RESET (HEX) FOR A,B, AND C	POWER-ON RESET (HEX) FOR D	BIT DESCRIPTIONS								REGISTER DESCRIPTIONS
READ	WRITE			D7	D6	D5	D4	D3	D2	D1	D0	
00	NA(1)	00	00	LT11	LT10	LT9	LT8	LT7	LT6	LT5	LT4	Local Temperature (High Byte)
01	NA	00	00	RT11	RT10	RT9	RT8	RT7	RT6	RT5	RT4	Remote Temperature (High Byte)
02	NA	XX	XX	BUSY	LHIGH	LLOW	RHIGH	RLOW	OPEN	RTHRM	LTHRM	Status Register
03	09	00	00	MASK1	SD	AL/TH	0	0	RANGE	0	0	Configuration Register
04	0A	08	08	0	0	0	0	R3	R2	R1	R0	Conversion Rate Register
05	0B	55	6E	LTH11	LTH10	LTH9	LTH8	LTH7	LTH6	LTH5	LTH4	Local Temperature High Limit (High Byte)
06	0C	00	00	LTL11	LTL10	LTL9	LTL8	LTL7	LTL6	LTL5	LTL4	Local Temperature Low Limit (High Byte)
07	0D	55	6E	RTH11	RTH10	RTH9	RTH8	RTH7	RTH6	RTH5	RTH4	Remote Temperature High Limit (High Byte)
08	0E	00	00	RTL11	RTL10	RTL9	RTL8	RTL7	RTL6	RTL5	RTL4	Remote Temperature Low Limit (High Byte)
NA	0F	XX	XX	X(2)	X	X	X	X	X	X	X	One-Shot Start
10	NA	00	00	RT3	RT2	RT1	RT0	0	0	0	0	Remote Temperature (Low Byte)
13	13	00	00	RTH3	RTH2	RTH1	RTH0	0	0	0	0	Remote Temperature High Limit (Low Byte)
14	14	00	00	RTL3	RTL2	RTL1	RTL0	0	0	0	0	Remote Temperature Low Limit (Low Byte)
15	NA	00	00	LT3	LT2	LT1	LT0	0	0	0	0	Local Temperature (Low Byte)
16	16	00	00	LTH3	LTH2	LTH1	LTH0	0	0	0	0	Local Temperature High Limit (Low Byte)
17	17	00	00	LTL3	LTL2	LTL1	LTL0	0	0	0	0	Local Temperature Low Limit (Low Byte)
18	18	00	00	NC7	NC6	NC5	NC4	NC3	NC2	NC1	NC0	N-factor Correction
19	19	55	6E	RTHL11	RTHL10	RTHL9	RTHL8	RTHL7	RTHL6	RTHL5	RTHL4	Remote $\overline{\text{THERM}}$ Limit
1A	1A	1C	1C	0	0	0	1	1	1	RES1	RES0	Resolution Register
20	20	55	6E	LTHL11	LTHL10	LTHL9	LTHL8	LTHL7	LTHL6	LTHL5	LTHL4	Local $\overline{\text{THERM}}$ Limit
21	21	0A	0A	TH11	TH10	TH9	TH8	TH7	TH6	TH5	TH4	$\overline{\text{THERM}}$ Hysteresis
22	22	81	81	TO_EN	0	0	0	C2	C1	C0	1	Consecutive Alert Register
30	30	FF	FF	LMT11	LMT10	LMT9	LMT8	LMT7	LMT6	LMT5	LMT4	Local Temperature Minimum (High Byte)
31	31	F0	F0	LMT3	LMT2	LMT1	LMT0	0	0	0	0	Local Temperature Minimum (Low Byte)
32	32	00	00	LXT11	LXT10	LXT9	LXT8	LXT7	LXT6	LXT5	LXT4	Local Temperature Maximum (High Byte)
33	33	00	00	LXT3	LXT2	LXT1	LXT0	0	0	0	0	Local Temperature Maximum (Low Byte)
34	34	FF	FF	RMT11	RMT10	RMT9	RMT8	RMT7	RMT6	RMT5	RMT4	Remote Temperature Minimum (High Byte)
35	35	F0	F0	RMT3	RMT2	RMT1	RMT0	0	0	0	0	Remote Temperature Minimum (Low Byte)
36	36	00	00	RXT11	RXT10	RXT9	RXT8	RXT7	RXT6	RXT5	RXT4	Remote Temperature Maximum (High Byte)
37	37	00	00	RXT3	RXT2	RXT1	RXT0	0	0	0	0	Remote Temperature Maximum (Low Byte)
NA	FC	XX	XX	X(2)	X	X	X	X	X	X	X	Software Reset
FE	NA	55	55	0	1	0	1	0	1	0	1	Manufacturer ID
FF	NA	12	12	0	0	0	1	0	0	1	0	Device ID for TMP411-Q1A
FF	NA	13	13	0	0	0	1	0	0	1	1	Device ID for TMP411-Q1B

表 9-1. Register Map Summary (続き)

POINTER ADDRESS (HEX)		POWER-ON RESET (HEX) FOR A,B, AND C	POWER-ON RESET (HEX) FOR D	BIT DESCRIPTIONS								REGISTER DESCRIPTIONS
READ	WRITE			D7	D6	D5	D4	D3	D2	D1	D0	
FF	NA	10	10	0	0	0	1	0	0	0	0	Device ID for TMP411-Q1C

(1) NA = not applicable; register is write- or read-only.
(2) X = indeterminate state

9.1 Register Information

The TMP411-Q1 contains multiple registers for holding configuration information, temperature measurement results, temperature comparator maximum and minimum, limits, and status information. These registers are described in 図 9-1 and 表 9-1.

9.2 Pointer Register

図 9-1 shows the internal register structure of the TMP411-Q1. The 8-bit Pointer Register is used to address a given data register. The Pointer Register identifies which of the data registers must respond to a read or write command on the two-wire bus. This register is set with every write command. A write command must be issued to set the proper value in the Pointer Register before executing a read command. 表 9-1 describes the pointer address of the registers available in the TMP411-Q1. Please note read pointer address 0x05, 0x07, 0x19, and 0x20 have different power-on-reset values for A, B, C vs D. The power-on-reset (POR) value of the Pointer Register is 00h (0000 0000b).

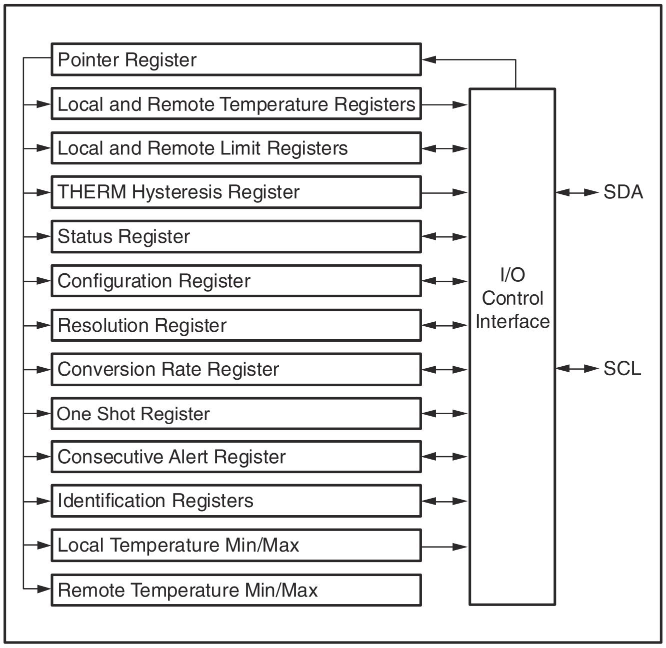


図 9-1. Internal Register Structure

9.3 Temperature Registers

The TMP411-Q1 has four 8-bit registers that hold temperature measurement results. Both the local channel and the remote channel have a high-byte register that contains the most-significant bits (MSBs) of the temperature analog-to-digital converter (ADC) result and a low-byte register that contains the least-significant bits (LSBs) of the temperature ADC result. The local-channel high-byte address is 00h; the local-channel low-byte address is 15h. The remote-channel high byte is at address 01h; the remote-channel low-byte address is 10h. These registers are read-only and are updated by the ADC each time a temperature measurement is completed.

The TMP411-Q1 contains circuitry to verify that a low-byte register-read command returns data from the same ADC conversion as the immediately preceding high-byte read command. This verification remains valid only until another register is read. For proper operation, the high byte of a temperature register must be read first. The low-byte register must be read in the next read command. The low byte register can be left unread if the LSBs are not needed. Alternatively, the temperature registers can be read as a 16-bit register by using a single two-byte read command from address 00h for the local-channel result or from address 01h for the remote-channel result. The high byte is output first, followed by the low byte. Both bytes of this read operation are from the same ADC conversion. The power-on-reset value of both temperature registers is 00h.

9.4 Limit Registers

The TMP411-Q1 has 11 registers for setting comparator limits for both the local and remote measurement channels. These registers have read and write capability. The High and Low Limit Registers for both channels span two registers, as do the temperature registers. The local-temperature high limit is set by writing the high byte to pointer address 0Bh and writing the low byte to pointer address 16h, or by using a single two-byte write command (high byte first) to pointer address 0Bh. The local-temperature high limit is obtained by reading the high byte from pointer address 05h and the low byte from pointer address 16h or by using a two-byte read command from pointer address 05h. The power-on-reset value of the local temperature high limit is 55h/6Eh/00h (85°C in standard temperature mode for TMP411A-Q1 to TMP411C-Q1; 110°C in standard temperature mode for TMP411D-Q1, 21°C in extended temperature range).

Similarly, the local-temperature low limit is set by writing the high byte to pointer address 0Ch and writing the low byte to pointer address 17h, or by using a single two-byte write command to pointer address 0Ch. The local-temperature low limit is read by reading the high byte from pointer address 06h and the low byte from pointer address 17h, or by using a two-byte read from pointer address 06h. The power-on-reset value of the local-temperature low-limit register is 00h/00h (0°C in standard temperature mode; –64°C in extended mode).

The remote-temperature high limit is set by writing the high byte to pointer address 0Dh and writing the low byte to pointer address 13h, or by using a two-byte write command to pointer address 0Dh. The remote-temperature high limit is obtained by reading the high byte from pointer address 07h and the low byte from pointer address 13h, or by using a two-byte read command from pointer address 07h. The power-on-reset value of the Remote Temperature High Limit Register is 55h/6Eh/00h (85°C in standard temperature mode for TMP411A-Q1 to TMP411C-Q1; 110°C in standard temperature mode for TMP411D-Q1; 21°C in extended temperature mode).

The remote-temperature low limit is set by writing the high byte to pointer address 0Eh and writing the low byte to pointer address 14h, or by using a two-byte write to pointer address 0Eh. The remote-temperature low limit is read by reading the high byte from pointer address 08h and the low byte from pointer address 14h, or by using a two-byte read from pointer address 08h. The power-on-reset value of the Remote Temperature Low Limit Register is 00h/00h (0°C in standard temperature mode; –64°C in extended mode).

The TMP411-Q1 also has $\overline{\text{THERM}}$ limit registers for both the local and the remote channels. These registers are eight bits and allow for $\overline{\text{THERM}}$ limits set to 1°C resolution. The local-channel $\overline{\text{THERM}}$ limit is set by writing to pointer address 20h. The remote-channel $\overline{\text{THERM}}$ limit is set by writing to pointer address 19h. The local channel $\overline{\text{THERM}}$ limit is obtained by reading from pointer address 20h; the remote channel $\overline{\text{THERM}}$ limit is read by reading from pointer address 19h. The power-on-reset value of the $\overline{\text{THERM}}$ limit registers is 55h/6Eh/00h (85°C in standard temperature mode for TMP411A-Q1 to TMP411C-Q1; 110°C in standard temperature mode for TMP411D-Q1; 21°C in extended temperature mode). The $\overline{\text{THERM}}$ limit comparators also have hysteresis. The hysteresis of both comparators is set by writing to pointer address 21h. The hysteresis value is obtained by reading from pointer address 21h. The value in the Hysteresis Register is an unsigned number (always positive). The power-on-reset value of this register is 0Ah (10°C).

Whenever changing between standard and extended temperature ranges, be aware that the temperatures stored in the temperature limit registers are not automatically reformatted to correspond to the new temperature range format. These values must be reprogrammed in the appropriate binary or extended binary format.

9.5 Status Register

The TMP411-Q1 has a Status Register to report the state of the temperature comparators. 表 9-2 shows the Status Register bits. The Status Register is read-only and is read by reading from pointer address 02h.

The BUSY bit reads as 1 if the ADC is making a conversion. The BUSY bit reads as 0 if the ADC is not converting.

The OPEN bit reads as 1 if the remote transistor is detected as open since the last read of the Status Register. The OPEN status is only detected when the ADC is attempting to convert a remote temperature.

The RTHRM bit reads as 1 if the remote temperature has exceeded the remote $\overline{\text{THERM}}$ limit and remains greater than the remote $\overline{\text{THERM}}$ limit less the value in the shared Hysteresis Register; see 図 8-7.

The LTHRM bit reads as 1 if the local temperature has exceeded the local $\overline{\text{THERM}}$ limit and remains greater than the local $\overline{\text{THERM}}$ limit less the value in the shared Hysteresis Register; see 図 8-7.

The LHIGH and RHIGH bit values depend on the state of the AL/TH bit in the Configuration Register. If the AL/TH bit is 0, the LHIGH bit reads as 1 if the local high limit is exceeded since the last clearing of the Status Register. The RHIGH bit reads as 1 if the remote high limit is exceeded since the last clearing of the Status Register. If the AL/TH bit is 1, the remote high limit and the local high limit are used to implement a $\overline{\text{THERM2}}$ function. LHIGH reads as 1 if the local temperature has exceeded the local high limit and remains greater than the local high limit less the value in the Hysteresis Register.

The RHIGH bit reads as 1 if the remote temperature has exceeded the remote high limit and remains greater than the remote high limit less the value in the Hysteresis Register. The LLOW and RLOW bits are not affected by the AL/TH bit.

The LLOW bit reads as 1 if the local low limit is exceeded since the last clearing of the Status Register. The RLOW bit reads as 1 if the remote low limit is exceeded since the last clearing of the Status Register. When there is no remote diode connected and the power supply ramp rate is less than 240V/s, RLOW flag will be set as well and should be ignored.

The values of the LLOW, RLOW, and OPEN (as well as LHIGH and RHIGH when AL/TH is 0) are latched and read as 1 until the Status Register is read or a device reset occurs. These bits are cleared by reading the Status Register, provided that the condition causing the flag to be set no longer exists. The values of BUSY, LTHRM, and RTHRM (as well as LHIGH and RHIGH when $\overline{\text{ALERT}}$/ $\overline{\text{THERM2}}$ is 1) are not latched and are not cleared by reading the Status Register. The values of BUSY, LTHRM, and RTHRM always indicate the current state, and are updated appropriately at the end of the corresponding ADC conversion. Clearing the Status Register bits does not clear the state of the $\overline{\text{ALERT}}$ pin; an SMBus alert response address command must be used to clear the $\overline{\text{ALERT}}$ pin.

The TMP411-Q1 NORs LHIGH, LLOW, RHIGH, RLOW, and OPEN, so a status change for any of these flags from 0 to 1 automatically causes the $\overline{\text{ALERT}}$ pin to go low (only applies when the $\overline{\text{ALERT}}$/ $\overline{\text{THERM2}}$ pin is configured for $\overline{\text{ALERT}}$ mode).

表 9-2. Status Register Format

STATUS REGISTER (Read = 02h, Write = NA)								
BIT #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BIT NAME	BUSY	LHIGH	LLOW	RHIGH	RLOW	OPEN	RTHRM	LTHRM
POR VALUE	0(1)	0	0	0	0	0	0	0

(1) The BUSY bit changes to 1 almost immediately (<<100µs) following power up, as the TMP411-Q1 begins the first temperature conversion. The BUSY bit is high whenever the TMP411-Q1 is converting a temperature reading.

9.6 Configuration Register

The Configuration Register sets the temperature range, controls shutdown mode, and determines how the $\overline{\text{ALERT}}$/ $\overline{\text{THERM2}}$ pin functions. The Configuration Register is set by writing to pointer address 09h and read by reading from pointer address 03h.

The MASK bit (bit 7) enables or disables the ALERT pin output if AL/TH = 0. If AL/TH = 1, then the MASK bit has no effect. If MASK is set to 0, the ALERT pin goes low when one of the temperature measurement channels exceeds the high or low limits for the chosen number of consecutive conversions. If the MASK bit is set to 1, the TMP411-Q1 retains the ALERT pin status, but the ALERT pin does not go low.

The shutdown (SD) bit (bit 6) enables or disables the temperature measurement circuitry. If SD = 0, the TMP411-Q1 converts continuously at the rate set in the conversion rate register. When SD is set to 1, the TMP411-Q1 immediately stops converting and enters a shutdown mode. When SD is set to 0 again, the TMP411-Q1 resumes continuous conversions. A single conversion can be started when SD = 1 by writing to the One-Shot Register.

The AL/TH bit (bit 5) controls whether the ALERT pin functions in ALERT mode or THERM2 mode. If AL/TH = 0, the ALERT pin operates as an interrupt pin. In this mode, the ALERT pin goes low after the set number of consecutive out-of-limit temperature measurements occurs.

If AL/TH = 1, the ALERT/ THERM2 pin implements a THERM function (THERM2). In this mode, THERM2 functions similarly to the THERM pin except that the local high limit and remote high limit registers are used for the thresholds. THERM2 goes low when either RHIGH or LHIGH is set.

The temperature range is set by configuring bit 2 of the Configuration Register. Setting this bit low configures the TMP411-Q1 for the standard measurement range (0°C to 127°C), and temperature conversions are stored in the standard binary format. Setting bit 2 high configures the TMP411-Q1 for the extended measurement range (–55°C to 150°C) temperature conversions are stored in the extended binary format (see 表 8-1).

The remaining bits of the Configuration Register are reserved and must always be set to 0. The power-on-reset value for this register is 00h. 表 9-3 summarizes the bits of the Configuration Register.

注

The TMP411x-Q1 device family is set to standard temperature range as default. Therefore, the device always needs to be configured to extended temperature range after power-up if this feature is used.

表 9-3. Configuration Register Bit Descriptions

CONFIGURATION REGISTER (Read = 03h, Write = 09h, POR = 00h)			
BIT	**NAME**	**FUNCTION**	**POWER-ON RESET VALUE**
7	MASK	0 = ALERT enabled; 1 = ALERT masked	0
6	SD	0 = Run; 1 = Shut down	0
5	AL/TH	0 = ALERT mode; 1 = THERM mode	0
4, 3	Reserved	—	0
2	Temperature range	0 = 0°C to 127°C; 1 = –55°C to 150°C	0
1, 0	Reserved	—	0

9.7 Resolution Register

The RES1 and RES0 bits (resolution bits 1 and 0) of the Resolution Register set the resolution of the local temperature measurement channel. Remote temperature measurement channel resolution is not affected. Changing the local channel resolution also affects the conversion time and rate of the TMP411-Q1. The Resolution Register is set by writing to pointer address 1Ah and is read by reading from pointer address 1Ah. 表 9-4 shows the resolution bits for the Resolution Register.

表 9-4. Resolution Register: Local Channel Programmable Resolution

RESOLUTION REGISTER (Read = 1Ah, Write = 1Ah, POR = 1Ch)			
RES1	**RES0**	**RESOLUTION**	**CONVERSION TIME (Typical)**
0	0	9 bits (0.5°C)	16.8ms
0	1	10 bits (0.25°C)	16.8ms

表 9-4. Resolution Register: Local Channel Programmable Resolution (続き)

RESOLUTION REGISTER (Read = 1Ah, Write = 1Ah, POR = 1Ch)			
RES1	RES0	RESOLUTION	CONVERSION TIME (Typical)
1	0	11 bits (0.125°C)	16.8ms
1	1	12 bits (0.0625°C)	16.8ms

Bits 2 through 4 of the Resolution Register must always be set to 1. Bits 5 through 7 of the Resolution Register must always be set to 0. The power-on-reset value of this register is 1Ch.

9.8 Conversion Rate Register

The Conversion Rate Register controls the rate at which temperature conversions are performed. This register adjusts the idle time between conversions but not the conversion timing, thereby allowing the TMP411-Q1 power dissipation to be balanced with the temperature register update rate. 表 9-5 shows the conversion rate options and corresponding current consumption.

表 9-5. Conversion Rate Register

CONVERSION RATE REGISTER (Read = 04h, Write = 0Ah, POR = 08h)									
R7	R6	R5	R4	R3	R2	R1	R0	CONVERSIONS PER SECOND	AVERAGE IQ (TYP) (µA)
									V+ = 2.7V and 5.5V
0	0	0	0	0	0	0	0	0.0625	1.5
0	0	0	0	0	0	0	1	0.125	1.8
0	0	0	0	0	0	1	0	0.25	2.5
0	0	0	0	0	0	1	1	0.5	3.8
0	0	0	0	0	1	0	0	1	6.5
0	0	0	0	0	1	0	1	2	12
0	0	0	0	0	1	1	0	4	23
07h to 0Fh								8	45

9.9 N-factor Correction Register

The TMP411-Q1 allows for a different *n*-factor value to be used for converting remote-channel measurements to temperature. The remote channel uses sequential current excitation to extract a differential V_{BE} voltage measurement to determine the temperature of the remote transistor. 式 1 relates this voltage and temperature.

$$V_{BE2} - V_{BE1} = \frac{nkT}{q} \times \ln\left(\frac{I_2}{I_1}\right) \quad (1)$$

The value *n* in 式 1 is a characteristic of the particular transistor used for the remote channel. The default value for the TMP411-Q1 is *n* = 1.008. The value in the N-Factor Correction Register can be used to adjust the effective n-factor according to 式 2 and 式 3.

$$n_{eff} = \frac{1.008 \times 300}{300 - N_{ADJUST}} \quad (2)$$

$$N_{ADJUST} = 300 - \frac{300 \times 1.008}{n_{eff}} \quad (3)$$

The *n*-correction value must be stored in twos-complement format, yielding an effective data range from −128 to 127, as shown in 表 9-6. The n-correction value can be written to and read from pointer address 18h. The register power-on-reset value is 00h, thus having no effect unless written to.

表 9-6. N-Factor Range

N_{ADJUST}			N
BINARY	**HEX**	**DECIMAL**	
0111 1111	7F	127	1.747977
0000 1010	0A	10	1.042759
0000 1000	08	8	1.035616
0000 0110	06	6	1.028571
0000 0100	04	4	1.021622
0000 0010	02	2	1.014765
0000 0001	01	1	1.011371
0000 0000	00	0	1.008
1111 1111	FF	−1	1.004651
1111 1110	FE	−2	1.001325
1111 1100	FC	−4	0.994737
1111 1010	FA	−6	0.988235
1111 1000	F8	−8	0.981818
1111 0110	F6	−10	0.975484
1000 0000	80	−128	0.706542

9.10 Minimum and Maximum Registers

The TMP411-Q1 stores the minimum and maximum temperature measured since power on, chip reset, or minimum and maximum register reset for both the local and remote channels. The Local Temperature Minimum Register can be read by reading the high byte from pointer address 30h and the low byte from pointer address 31h. The Local Temperature Minimum Register can also be read by using a two-byte read command from pointer address 30h. The Local Temperature Minimum Register is reset at power on, by executing the chip-reset command, or by writing any value to any of pointer addresses 30h through 37h. The reset value for these registers is FFh/F0h.

The Local Temperature Maximum Register can be read by reading the high byte from pointer address 32h and the low byte from pointer address 33h. The Local Temperature Maximum Register can also be read by using a two-byte read command from pointer address 32h. The Local Temperature Maximum Register is reset at power on by executing the chip reset command, or by writing any value to any of pointer addresses 30h through 37h. The reset value for these registers is 00h/00h.

The Remote Temperature Minimum Register can be read by reading the high byte from pointer address 34h and the low byte from pointer address 35h. The Remote Temperature Minimum Register can also be read by using a two-byte read command from pointer address 34h. The Remote Temperature Minimum Register is reset at power on by executing the chip reset command, or by writing any value to any of pointer addresses 30h through 37h. The reset value for these registers is FFh/F0h.

The Remote Temperature Maximum Register can be read by reading the high byte from pointer address 36h and the low byte from pointer address 37h. The Remote Temperature Maximum Register can also be read by using a two-byte read command from pointer address 36h. The Remote Temperature Maximum Register is reset at power on by executing the chip reset command, or by writing any value to any of pointer addresses 30h through 37h. The reset value for these registers is 00h/00h.

9.11 Consecutive Alert Register

The value in the Consecutive Alert Register (address 22h) determines how many consecutive out-of-limit measurements must occur on a measurement channel before the $\overline{\text{ALERT}}$ signal is activated. The value in this register does not affect bits in the Status Register. Values of one, two, three, or four consecutive conversions can be selected; one conversion is the default. This function allows additional filtering for the $\overline{\text{ALERT}}$ pin. The consecutive alert bits are shown in 表 9-7.

表 9-7. Consecutive Alert Register

CONSECUTIVE ALERT REGISTER (READ = 22h, WRITE = 22h, POR = 01h)			NUMBER OF CONSECUTIVE OUT-OF-LIMIT MEASUREMENTS
C2	C1	C0	
0	0	0	1
0	0	1	2
0	1	1	3
1	1	1	4

注

Bit 7 of the Consecutive Alert Register controls the enable/disable of the timeout function. See the Timeout Function section for a description of this feature.

9.12 $\overline{\text{THERM}}$ Hysteresis Register

The $\overline{\text{THERM}}$ Hysteresis Register, shown in 表 9-9, stores the hysteresis value used for the $\overline{\text{THERM}}$ pin alarm function. This register must be programmed with a value that is less than the Local Temperature High Limit Register value, Remote Temperature High Limit Register value, Local THERM Limit Register value, or Remote THERM Limit Register value; otherwise, the respective temperature comparator does not trip on the measured temperature falling edges. Allowable hysteresis values are shown in 表 9-8. The default hysteresis value is 10°C, whether the device is operating in the standard or extended mode setting.

表 9-8. Allowable $\overline{\text{THERM}}$ Hysteresis Values

TEMPERATURE (°C)	$\overline{\text{THERM}}$ HYSTERESIS VALUE	
	TH[11:4] (STANDARD BINARY)	(HEX)
0	0000 0000	00
1	0000 0001	01
5	0000 0101	05
10	0000 1010	0A
25	0001 1001	19
50	0011 0010	32
75	0100 1011	4B
100	0110 0100	64
125	0111 1101	7D
127	0111 1111	7F
150	1001 0110	96
175	1010 1111	AF
200	1100 1000	C8
225	1110 0001	E1
255	1111 1111	FF

表 9-9. $\overline{\text{THERM}}$ Hysteresis Register Format

$\overline{\text{THERM}}$ HYSTERESIS REGISTER (Read = 21h, Write = 21h, POR = 0Ah)								
BIT #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BIT NAME	TH11	TH10	TH9	TH8	TH7	TH6	TH5	TH4
POR VALUE	0	0	0	0	1	0	1	0

9.13 Identification Registers

The TMP411-Q1 allows for the two-wire bus controller to query the device for manufacturer and device IDs. This feature allows for software identification of the device at the particular two-wire bus address. The manufacturer ID is obtained by reading from pointer address FEh. The TMP411-Q1 manufacturer code is 55h. The device ID depends on the specific model; see the Register Map (表 9-1). These registers are read-only.

10 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

10.1 Application Information

The TMP411-Q1 only requires a transistor connected between the D+ and D– pins for remote temperature measurement. Tie the D+ pin to D– if the remote channel is not used and only the local temperature is measured. The SDA, $\overline{\text{ALERT}}$ and $\overline{\text{THERM}}$ pins (and SCL, if driven by an open-drain output) require pullup resistors as part of the communication bus. TI recommends using a 0.1µF power-supply decoupling capacitor for local bypassing. 図 8-1 illustrates the typical configurations for the TMP411-Q1.

10.2 Typical Application

10.2.1 Design Requirements

The TMP411-Q1 is designed to be used with either discrete transistors or substrate transistors built into processor chips and ASICs. Either NPN or PNP transistors can be used, as long as the base-emitter junction is used as the remote temperature sense. Either a transistor or diode connection can also be used; see 図 8-1.

Errors in remote temperature-sensor readings are the consequence of the ideality factor and current excitation used by the TMP411-Q1 versus the manufacturer-specified operating current for a given transistor. Some manufacturers specify a high-level and low-level current for the temperature-sensing substrate transistors. The TMP411-Q1 uses 6µA for I_{LOW} and 120µA for I_{HIGH}. The TMP411-Q1 allows for different n-factor values; see the N-Factor Correction Register section.

The ideality factor (n) is a measured characteristic of a remote temperature sensor diode as compared to an ideal diode. The ideality factor for the TMP411-Q1 is trimmed to be 1.008. For transistors whose ideality factor does not match the TMP411-Q1, 式 4 can be used to calculate the temperature error. Note that for the equation to be used correctly, actual temperature (°C) must be converted to Kelvin (K).

$$T_{ERR} = \frac{n - 1.008}{1.008} \times (273.15 + T(°C)) \quad (4)$$

where:

n = Ideality factor of remote temperature sensor

T(°C) = actual temperature

T_{ERR} = Error in TMP411-Q1 reading due to $n \neq 1.008$

Degree delta is the same for °C and °K

For n = 1.004 and T(°C) = 100°C:

$$T_{ERR} = \frac{1.004 - 1.008}{1.008} \times (273.15 + 100°C) \quad (5)$$

$$T_{ERR} = -1.48°C \quad (6)$$

If a discrete transistor is used as the remote temperature sensor with the TMP411-Q1, the best accuracy can be achieved by selecting the transistor according to the following criteria:

1. Base-emitter voltage > 0.25V at 6µA, at the highest sensed temperature.
2. Base-emitter voltage < 0.95V at 120µA, at the lowest sensed temperature.

3. Base resistance < 100Ω.
4. Tight control of V_{BE} characteristics indicated by small variations in h_{FE} (that is, 50 to 150).

Based on these criteria, two recommended small-signal transistors are the 2N3904 (NPN) or 2N3906 (PNP).

10.2.2 Detailed Design Procedure

The temperature measurement accuracy of the TMP411-Q1 depends on the remote and/or local temperature sensor being at the same temperature as the system point being monitored. If the temperature sensor is not in good thermal contact with the part of the system being monitored, then there is a delay in the response of the sensor to a temperature change in the system. For remote temperature sensing applications using a substrate transistor (or a small, SOT23 transistor) placed close to the device being monitored, this delay is typically not a concern.

The local temperature sensor inside the TMP411-Q1 monitors the ambient air around the device. The thermal time constant for the TMP411-Q1 is approximately 2 seconds. This constant implies that if the ambient air changes quickly by 100°C, the TMP411-Q1 takes about 10 seconds (that is, five thermal time constants) to settle to within 1°C of the final value. In most applications, the TMP411-Q1 package is in electrical and therefore thermal contact with the printed circuit board (PCB), as well as subjected to forced airflow. The accuracy of the measured temperature directly depends on how accurately the PCB and forced airflow temperatures represent the temperature that the TMP411-Q1 is measuring. Additionally, the internal power dissipation of the TMP411-Q1 can cause the temperature to rise above the ambient or PCB temperature. The internal power dissipated as a result of exciting the remote temperature sensor is negligible because of the small currents used. For a 5.5V supply and maximum conversion rate of eight conversions per second, the TMP411-Q1 dissipates 0.248mW (PD_{IQ} = 5.5V × 45μA). If both the $\overline{\text{ALERT}}$/ $\overline{\text{THERM2}}$ and $\overline{\text{THERM}}$ pins are each sinking 1mA, an additional power of 0.8mW is dissipated (PD_{OUT} = 1mA × 0.4V + 1mA × 0.4V = 0.8mW). Total power dissipation is then 1.048mW (PD_{IQ} + PD_{OUT}) and, with a θ_{JA} of 162°C/W, causes the junction temperature to rise approximately 0.170°C above the ambient.

10.2.3 Application Curves

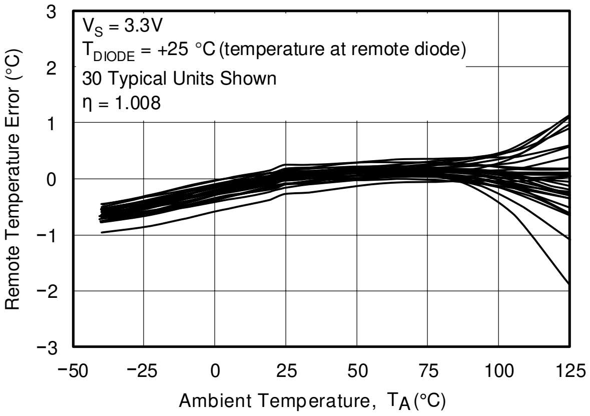


図 10-1. Remote Temperature Error vs TMP411-Q1 Ambient Temperature

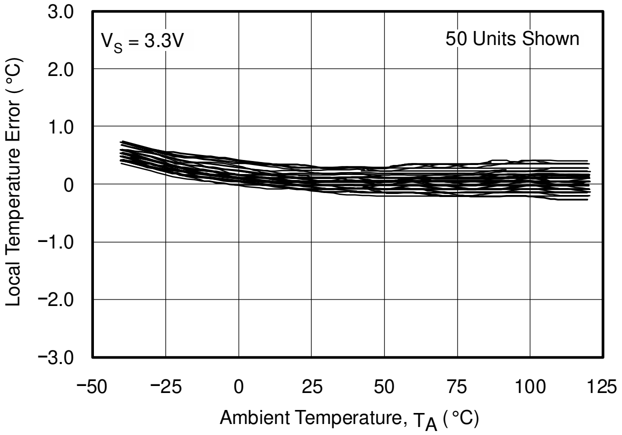


図 10-2. Local Temperature Error vs TMP411-Q1 Ambient Temperature

10.3 Power Supply Recommendations

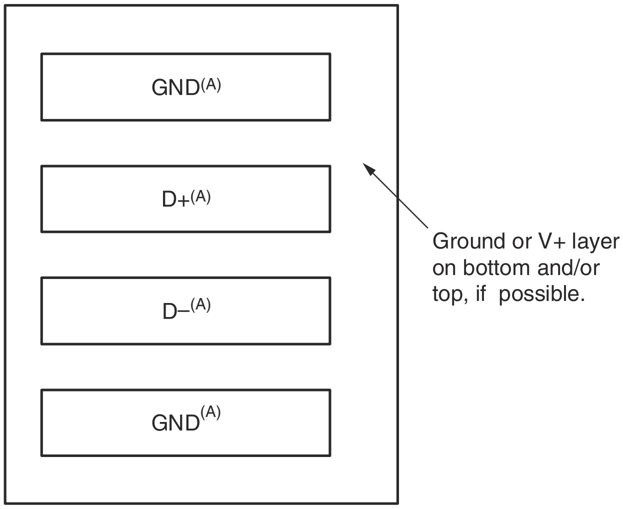
The TMP411-Q1 operates with a power supply range of 2.7V to 5.5V. The device is optimized for operation at a 3.3V supply, but measures temperature accurately in the full supply range. TI recommends using a power supply bypass capacitor. Place the capacitor as close as possible to the supply and ground pins of the device. 0.1µF is a typical value for the supply bypass capacitor. Applications with noisy or high-impedance power supplies can require additional decoupling capacitors to reject power-supply noise.

10.4 Layout

10.4.1 Layout Guidelines

Remote temperature sensing on the TMP411-Q1 measures very small voltages using very low currents; therefore, noise at the IC inputs must be minimized. Most applications using the TMP411-Q1 have high digital content, with several clocks and logic-level transitions creating a noisy environment. The layout must adhere to the following guidelines:

1. Place the TMP411-Q1 as close to the remote junction sensor as possible.
2. Route the D+ and D− traces next to each other and shield them from adjacent signals through the use of ground guard traces, as shown in 図 10-3. If a multilayer PCB is used, bury these traces between ground or VDD planes to shield them from extrinsic noise sources. Five-mil (0.127mm) PCB traces are recommended.
3. Minimize additional thermocouple junctions caused by copper-to-solder connections. If these junctions are used, make the same number and approximate locations of copper-to-solder connections in both the D+ and D− connections to cancel any thermocouple effects.
4. Use a 0.1µF local bypass capacitor directly between the V+ and GND of the TMP411-Q1, as shown in 図 10-4. Minimize filter capacitance between D+ and D− to 1000pF or less for optimum measurement performance. This capacitance includes any cable capacitance between the remote temperature sensor and TMP411-Q1.
5. If the connection between the remote temperature sensor and the TMP411-Q1 is less than 8 inches (20cm), use a twisted-wire pair connection. Beyond 8 inches (20cm), use a twisted, shielded pair with the shield grounded as close to the TMP411-Q1 as possible. Leave the remote sensor connection end of the shield wire open to avoid ground loops and 60Hz pickup.



A. 5mil (0.127mm) traces with 5mil (0.127mm) spacing

図 10-3. Example Signal Traces

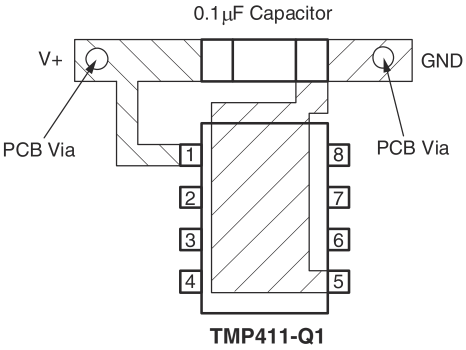


図 10-4. Suggested Bypass Capacitor Placement

10.4.2 Layout Example

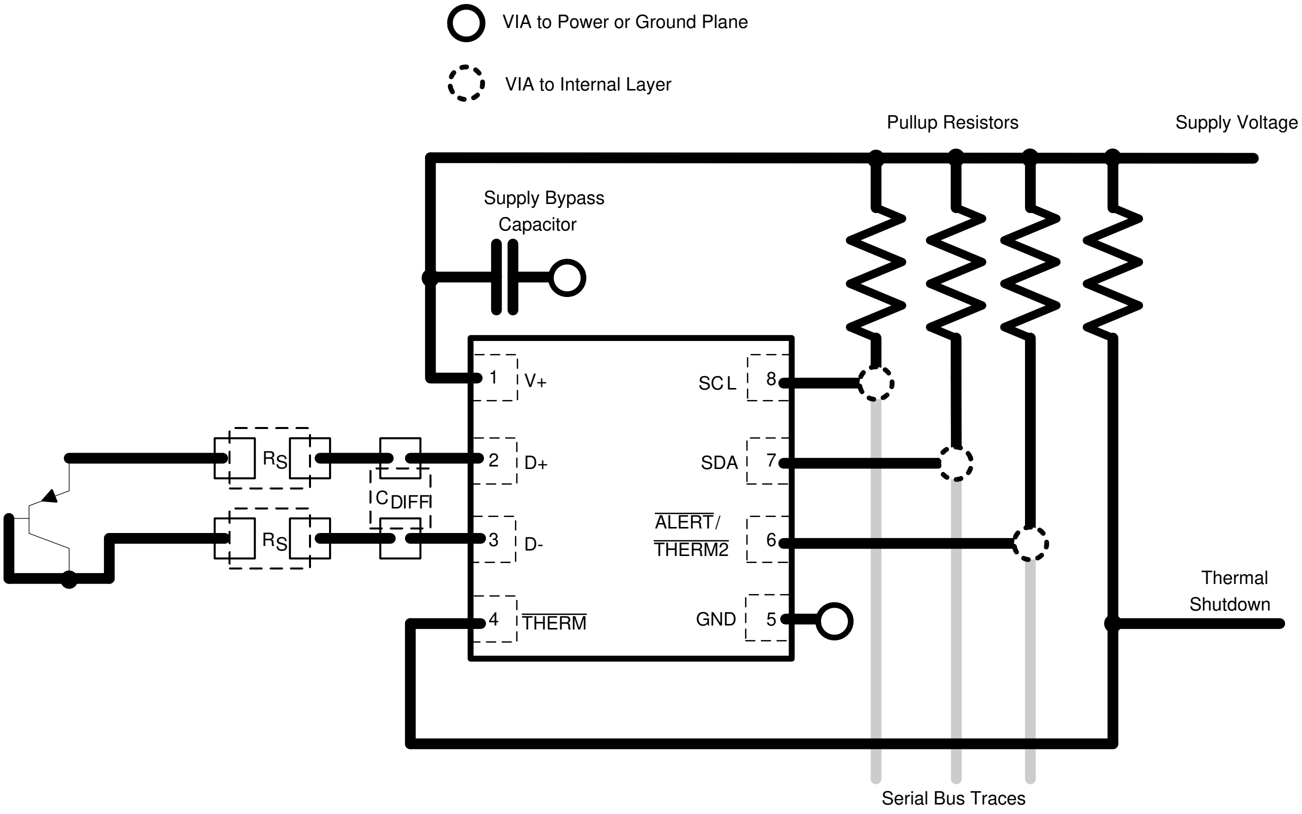


図 10-5. TMP411-Q1 Device Layout

11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

11.1 Documentation Support

11.1.1 Related Documentation

- Texas Instruments, *Optimizing Remote Temperature Sensor Design*, application note
- Texas Instruments, *TMP451 ±1°C Remote and Local Temperature Sensor With η-Factor and Offset Correction, Series-Resistance Cancellation, and Programmable Digital Filter*, data sheet
- Texas Instruments, *TMP411 ±1°C Remote and Local Temperature Sensor With N-Factor and Series Resistance Correction*, data sheet
- Texas Instruments, *TMP411-Q1 Functional Safety FIT Rate, FMD and Pin FMA*, Functional safety information

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 サポート・リソース

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11.6 用語集

テキサス・インスツルメンツ用語集	この用語集には、用語や略語の一覧および定義が記載されています。

12 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision F (November 2013) to Revision G (September 2024)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新	1
• 「概要」セクションに「パッケージ情報」表を追加	1
• Added *Pin Configurations and Functions* section	3
• Added "Type" column to *Pin Functions* table	3
• Updated the maximum voltage rating on D+/D- pins to 2V	4

- Updated the maximum voltage rating on pins 4, 6, 7, 8 to 6V.........4
- Added DGK package Thermal Information section.........4
- Changed "Conversion time" in Electrical Characteristics table.........5
- Deleted Medium low from "Remote sensor source currents" in the Electrical Characteristics table.........5
- Updated the typo for Hysteresis typical value from 500mV to 170mV.........5
- Changed Quiescent current values for all test conditions in the Electrical Characteristics table.........5
- Updated the typo for fs=40KHz and changed to fs=400KHz.........5
- Removed limitation on Undervoltage lockout.........5
- Changed Power-on-reset threshold values in the Electrical Characteristics table.........5
- Changed t(SUDAT) in High-Speed Mode from 10ns to 20ns.........6
- Added an overview in the *Detailed Description* section.........10
- Added *Functional Block Diagram* section.........11
- Added *Feature Description* section and relocated feature information to this section.........11
- Added *Device Functional Modes* section.........14
- Added *Timing Diagrams* to the *Specifications* section.........15
- Changed *REGISTER INFORMATION* section to *Register Maps* section and centralized register information in this section.........21
- Added *Application and Implementation* section.........29
- Added *Typical Application* section.........29
- Added *Design Requirements* section.........29
- Added *Application Curves* section.........30
- Added *Power Supply Recommendations* section.........31
- Changed from *Layout Considerations* to *Layout Guidelines* 31
- Added the *Device and Documentation Support* section and sub-sections.........34
- Added the *Mechanical, packaging, and Orderable Information* section.........38

Changes from Revision E (December 2012) to Revision F (November 2013) **Page**

- ドキュメント全体にわたって表、図、相互参照の採番方法を更新.........1
- ドキュメント全体を通してパッケージを MSOP から VSSOP に変更。.........1
- Deleted TA and Top-Side Marking columns from the *Device Comparison* section.........2
- Changed device CDM ESD Classification Level from C3B to C4B in Section 1 list item and in the ABSOLUTE MAXIMUM RATINGS table.........4

Changes from Revision D (November 2012) to Revision E (December 2012) **Page**

- 「広いリモート温度測定範囲 (最高 150℃)」を再追加。.........1
- Added Brownout detect value in the *Electrical Characteristics* table.........5
- Removed ", which is referred to as standard temperature mode" in first paragraph of Temperature Measurement Data section.........11
- Added last two sentences of first paragraph back in to Temperature Measurement Data section.........11
- Added paragraph after "Likewise, temperatures above 127°C result in a value of 127 (7Fh)." back into Temperature Measurement Data section.........11
- Added Extended Binary columns back into Table 1.........11
- Added note after Table 1.........11
- Added "AND EXTENDED" back in to the STANDARD BINARY column headers in Table 2.........11
- Replaced last sentence of first paragraph in Limit Registers section with: The power-on-reset value of the local temperature high limit is 55h/00h (85°C in standard temperature mode for TMP411A-Q1 to TMP411C-Q1; 110°C in standard temperature mode for TMP411D-Q1, 21°C in extended temperature range).........22
- Added –64°C in extended mode back in to second and fourth paragraphs in Limit Registers section.........22

- Replaced last sentence of fourth paragraph in Limit Registers section with: The power-on-reset value of the Remote Temperature High Limit Register is 55h/00h (85°C in standard temperature mode for TMP411A-Q1 to TMP411C-Q1; 110°C in standard temperature mode for TMP411D-Q1; 21°C in extended temperature mode)... 22
- Replaced sentence in fifth paragraph of Limit Registers section with: The power-on-reset value of the $\overline{\text{THERM}}$ limit registers is 55h (85°C in standard temperature mode for TMP411A-Q1 to TMP411C-Q1; 110°C in standard temperature mode for TMP411D-Q1; 21°C in extended temperature mode). ... 22
- Added last paragraph back into Limit Registers section... 22
- Replaced this sentence: This bit is set to 0 by default and cannot be changed, with this sentence: Setting bit 2 high configures the TMP411-Q1 for the extended measurement range (–55°C to 150°C) temperature conversions are stored in the extended binary format (see Table 1)... 23
- Added note to Configuration Register section... 23
- Added 1 = –55°C to 150°C back to temperature range row in table 5. ... 23
- Added: whether the device is operating in the standard or extended mode setting to last sentence in Therm Hysteresis Register section... 27

Changes from Revision C (September 2012) to Revision D (November 2012) **Page**

- Added default local high temp limit and default remote high temp limit columns to ordering information table.. 2
- Changed last column header from default local temperature high limit to default temperature range... 2
- Changed *Ordering Information* section to *Device Comparison* section... 2

Changes from Revision B (July 2012) to Revision C (September 2012) **Page**

- 「広いリモート温度測定範囲 (最高 150℃)」を削除... 1
- Changed extended default local temperature high limit to standard, deleted table note... 2
- Deleted package columns from ordering information table... 2
- Removed the last two sentences in the first paragraph, added "which is referred to as standard temperature mode."... 11
- Deleted paragraph after "Likewise, temperatures above 127°C result in a value of 127 (7Fh)."... 11
- Deleted extended binary from Table 1 and first paragraph beginning with "Note:" underneath the table... 11
- Removed "AND EXTENDED" from Table 2 ... 11
- Added the sentence "Please note read pointer address 0x05, 0x07, 0x19, and 0x20 have different power-on-reset values for A, B, C vs D" before last sentence under pointer register. ... 21
- Added space in between one and shot in figure 12... 21
- Changed last sentence of first, and third paragraph, and the 6th sentence of the last paragraph under limit registers to: "The power-on-reset value of the local-temperature high limit is 55h for TMP411A-Q1 and 6Eh for TMP411D-Q1 (85°C for TMP411A-Q1 and 110°C for TMP411D-Q1)” ... 22
- Removed –64°C in extended mode from the second and fourth paragraphs under limit registers. ... 22
- Deleted last paragraph under limit registers... 22
- Replaced last sentence of 6th paragraph under configuration register with "This bit is set to 0 by default and cannot be changed."... 23
- Removed ; 1 = −55°C to 150°C from temperature range row in table 5... 23

Changes from Revision A (February 2012) to Revision B (July 2012) **Page**

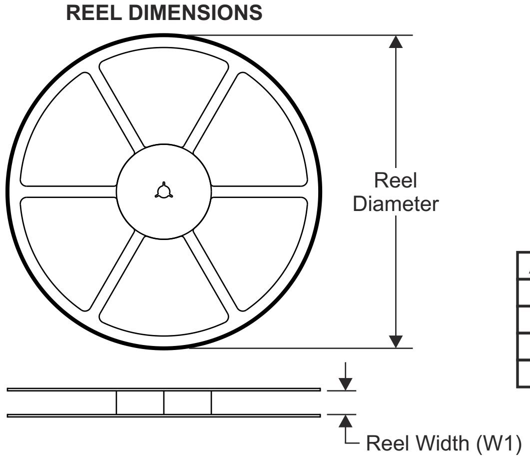
- Added table note to ordering information table; added default to local temperature high limit column header.. 2
- Added another column: Power-on Reset (HEX) for D... 21

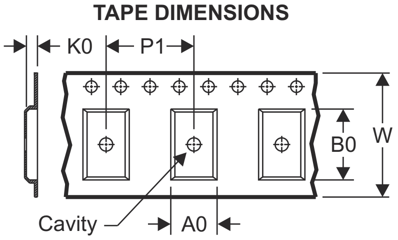
Changes from Revision * (December 2012) to Revision A (February 2012)	Page
• Changed the Ordering Information Table. Deleted Preview devices TMP411xQDRQ1, and added device TPM411DQDGKRQ1	2

13 Mechanical, Packaging, and Orderable Information

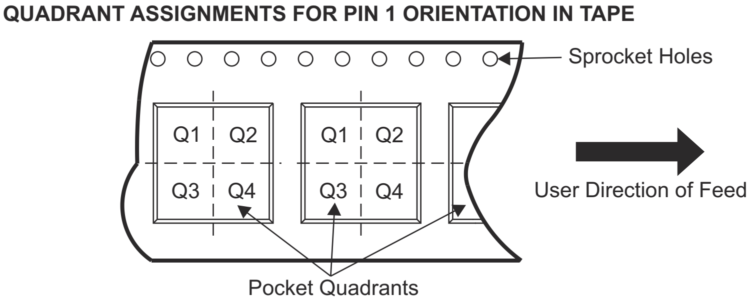
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

13.1 Tape and Reel Information



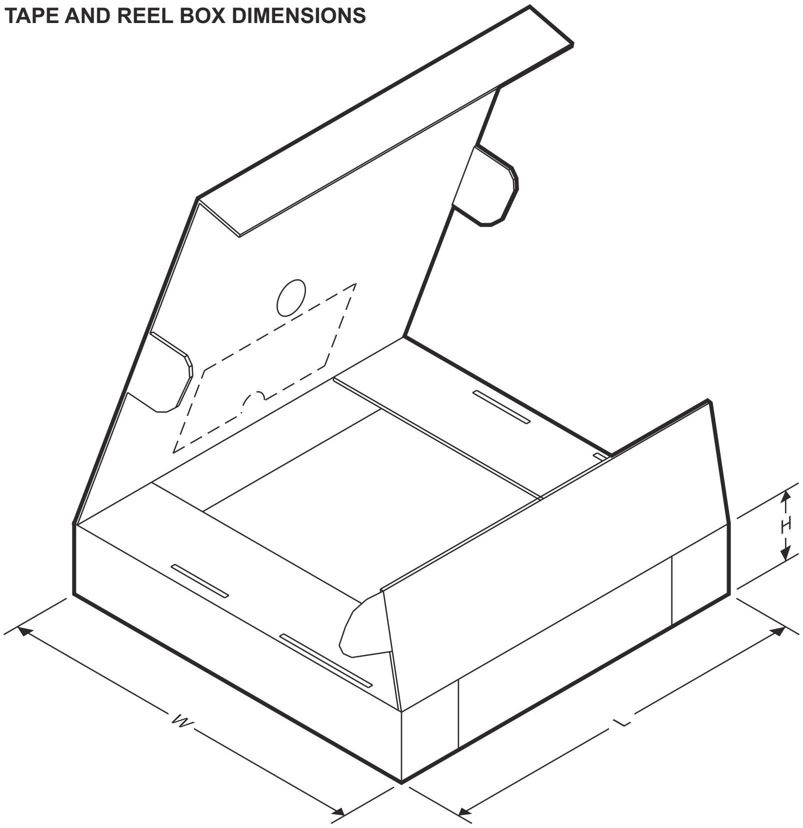


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP411AQDGKRQ1	VSSOP	DGK	8	2500	330	12.4	5.3	3.3	1.3	8	12	Q1
TMP411BQDGKRQ1	VSSOP	DGK	8	2500	330	12.4	5.3	3.4	1.4	8	12	Q1
TMP411CQDGKRQ1	VSSOP	DGK	8	2500	330	12.4	5.3	3.4	1.4	8	12	Q1
TMP411DQDGKRQ1	VSSOP	DGK	8	2500	330	12.4	5.3	3.3	1.3	8	12	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP411AQDGKRQ1	VSSOP	DGK	8	2500	367	367	38
TMP411BQDGKRQ1	VSSOP	DGK	8	2500	366	364	50
TMP411CQDGKRQ1	VSSOP	DGK	8	2500	366	364	50
TMP411DQDGKRQ1	VSSOP	DGK	8	2500	367	367	38

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PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMP411AQDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	125 to -40	411AQ
TMP411AQDGKRQ1.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	125 to -40	411AQ
TMP411BQDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	411BQ
TMP411BQDGKRQ1.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	411BQ
TMP411CQDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	411CQ
TMP411CQDGKRQ1.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	411CQ
TMP411DQDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 125	411DQ
TMP411DQDGKRQ1.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 125	411DQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TMP411-Q1 :

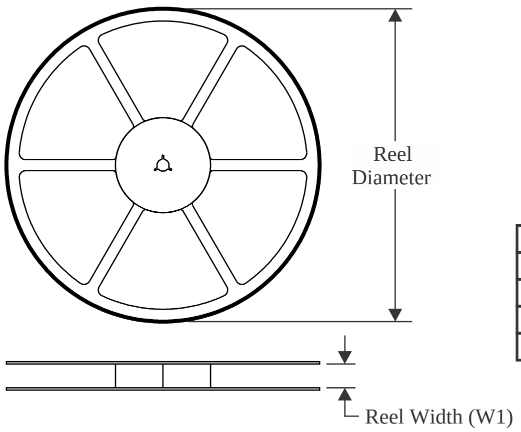
- Catalog : TMP411

NOTE: Qualified Version Definitions:

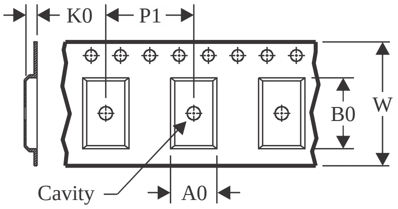
  - Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

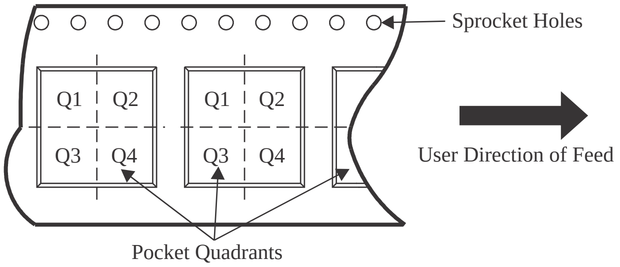


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

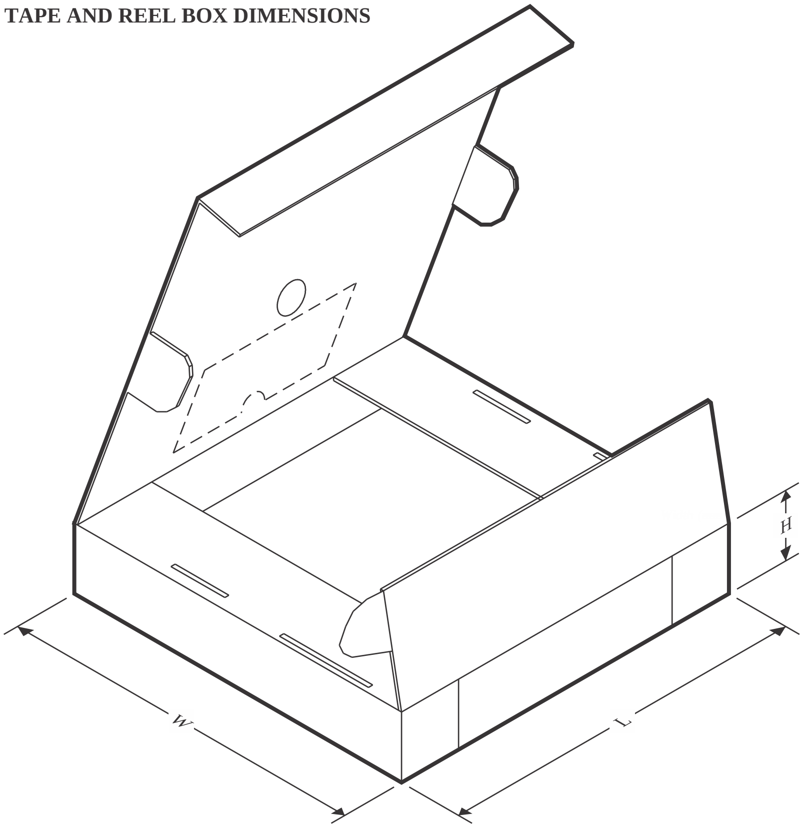
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP411AQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TMP411BQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TMP411CQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TMP411DQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



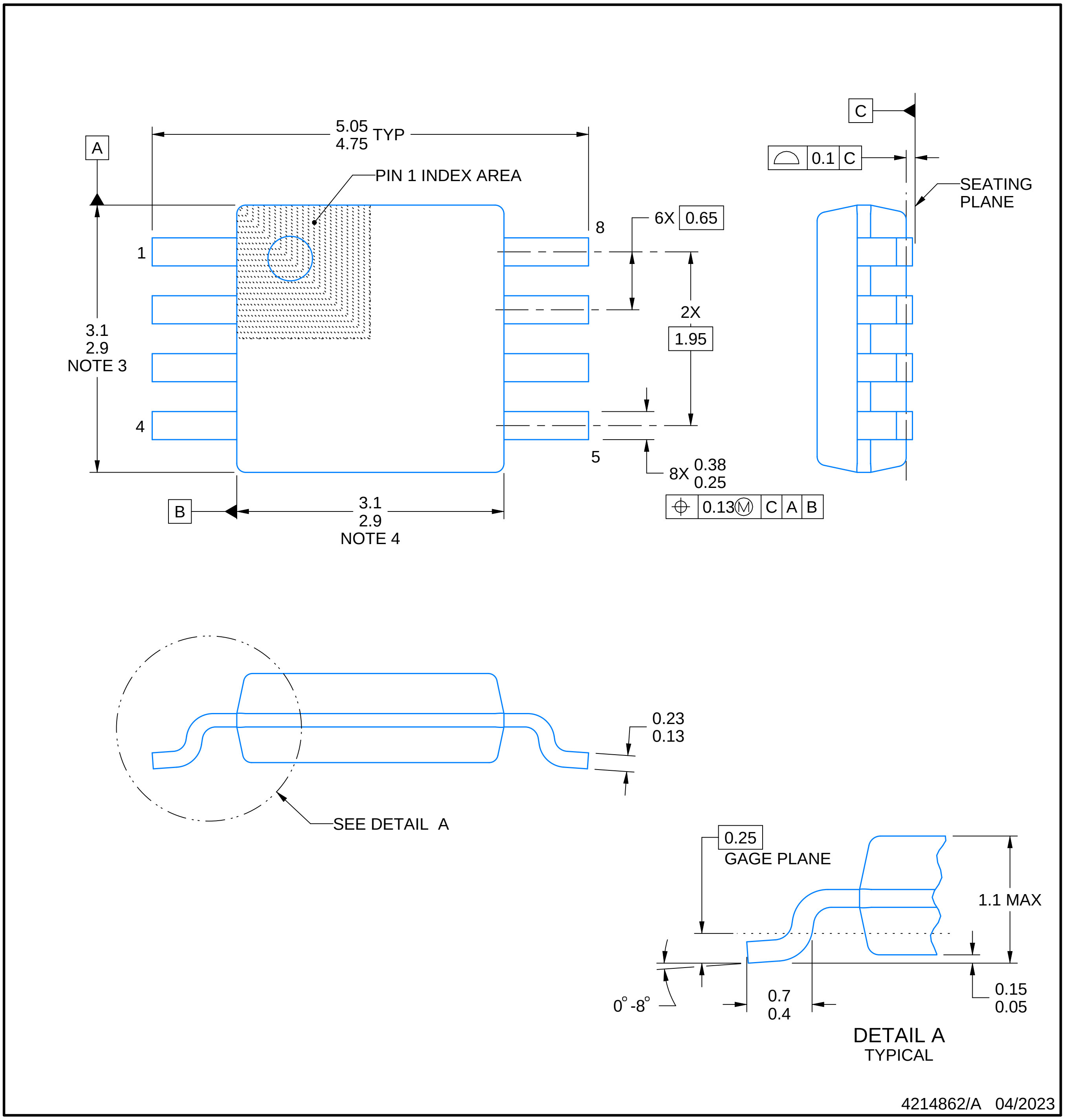
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP411AQDGKRQ1	VSSOP	DGK	8	2500	367.0	367.0	38.0
TMP411BQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
TMP411CQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
TMP411DQDGKRQ1	VSSOP	DGK	8	2500	367.0	367.0	38.0

PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

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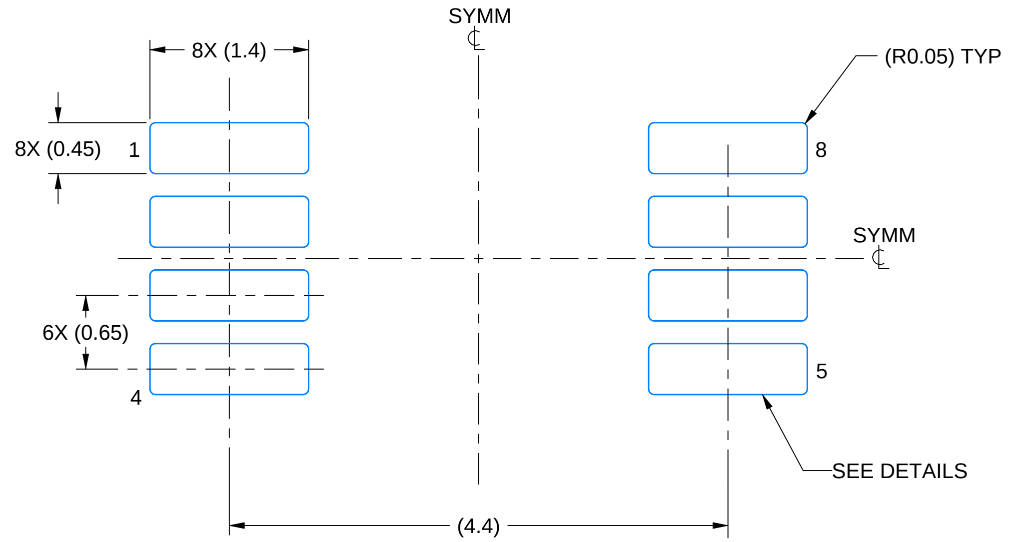
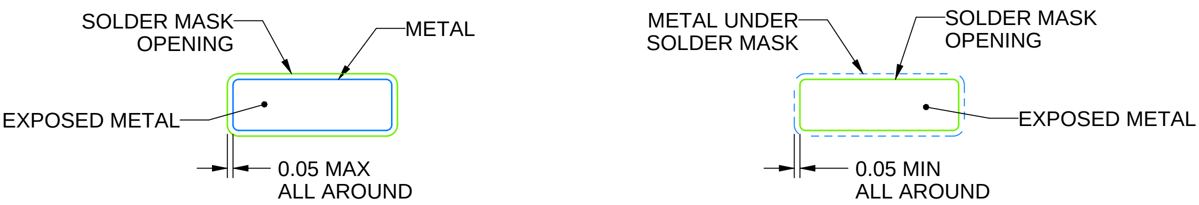
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



NON-SOLDER MASK
DEFINED
(PREFERRED)

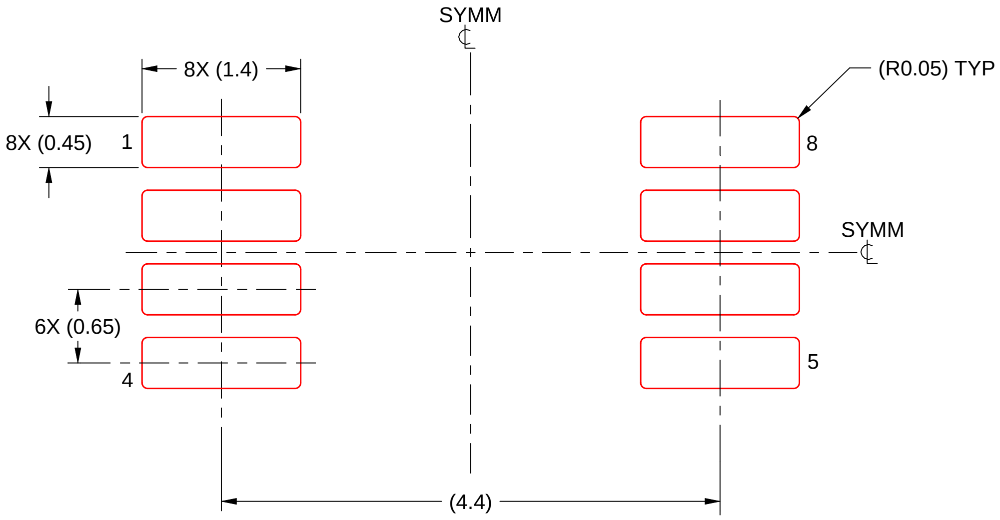
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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