TMP110 低コスト システム向け、超小型、±1.0℃精度、I²C デジタル温度センサ

1 特長

- 超小型、リードレス X2SON-5 パッケージ
  - パッケージ サイズ:0.8 × 0.8 × 0.4mm
- 広い動作範囲
  - V+ 動作範囲:1.14V～5.5V
  - 温度範囲:-40℃～125℃
- 動作温度全域で精度を確保
  - -40℃～125℃で ±1.0℃ (最大値)
- 12 ビット分解能:0.0625℃ (LSB)
- 柔軟なデジタル インターフェイス
  - I²C バスおよび SMBus 互換
  - I3C 混在バス上での共存に対応
- ピン配置とソフトウェアの互換性があるアップグレード
  - ±0.5°C → TMP112 (X2SON パッケージ)
- 低い電源電流
  - アクティブ電流:55μA (標準値)
  - シャットダウン電流:0.15μA (標準値)
  - 平均電流 (1Hz 時):3.2μA (標準値)
- 業界標準とソフトウェア互換
  - TMP102、TMP112
- 2 種類のピン配置を選択可能
  - ALERT ピン:TMP110D0、TMP110D1、TMP110D2、TMP110D3
  - アドレス ピン:TMP110D
- GUI ベースの C コード ジェネレータ

2 アプリケーション

- ビル オートメーション
  - 物体検出
  - ビデオ ドアベル
  - HVAC:ワイヤレス環境センサ
- ファクトリ オートメーション & 制御
  - マシン ビジョン カメラ
  - 産業用 PC:シングル ボード コンピュータ
  - CPU (PLC コントローラ)
- コールド チェーン
- データ センター & エンタープライズ コンピューティング
  - ソリッド ステート ドライブ (SSD)
  - ラック サーバー向けマザーボード
- パーソナル エレクトロニクス
  - PC & ノート PC、タブレット
  - デジタル スチル カメラ & デジタル ビデオ カメラ
  - 拡張現実 (AR) メガネ
  - スマート スピーカ

3 概要

TMP110 は、超小型 (0.64mm²) 5 ピン パッケージの I²C 互換デジタル温度センサです。その小型低背パッケージは、DSBGA パッケージでは適さないような容積に制約のあるシステムに最適化されています。同等サイズの DSBGA パッケージとは異なり、TMP110 は、アドレス ピンと ALERT ピンのどちらとしても使用できる第 5 のピンを持っているため、センサの数を拡張することにも、重要な熱イベントを監視することにも柔軟に対応できます。

TMP110 は、温度分解能 0.0625℃の内蔵 12 ビット A/D コンバータ (ADC) により、動作温度の全域で ±1.0℃の精度を達成しています。

TMP110 は最小 1.14V の電源電圧で動作するように設計されています。平均電流、シャットダウン電流はそれぞれ 3.2μA (1Hz 時)、0.15μA と小さいため、オンデマンドの温度変換が可能であり、バッテリ寿命を最大化できます。また、各種産業用アプリケーション向けに、電源電圧を最大 5.5V まで上げることもできます。

パッケージ情報

部品番号	パッケージ [1]	パッケージ サイズ [2]
TMP110	X2SON (5)	0.8mm × 0.8mm

(1) 詳細については、セクション 12 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。

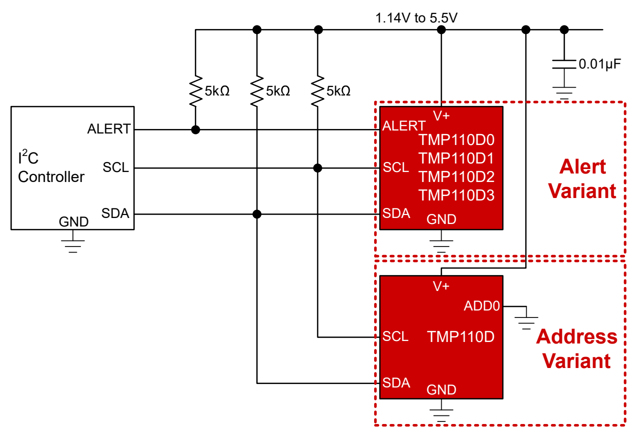


図 3-1. 概略回路図

Table of Contents

4 Related Products

Pin-to-pin and software compatible options are available.

表 4-1. Related Temperature Sensors

DEVICE	BEST ACCURACY (MAXIMUM)	SOFTWARE COMPATIBLE	ADDRESS/ALERT PIN FUNCTIONALITY	PACKAGE OPTIONS
TMP102	2.0 °C	Yes	Address + Alert	DRL (6-pin SOT563) (1.6mm × 1.6mm)
TMP110	1.0 °C	Yes	Separate (Address & Alert)	DPW (5-pin X2SON) (0.8mm × 0.8mm)
TMP112	0.5 °C	Yes	Address + Alert (DRL)	DRL (6-pin SOT563) (1.6mm × 1.6mm)
			Separate (Address & Alert) (DPW)	DPW (5-pin X2SON) (0.8mm × 0.8mm)

5 Pin Configuration and Functions

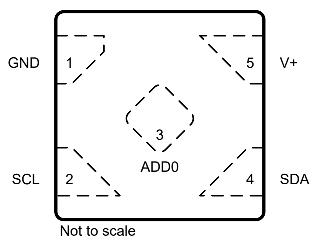


図 5-1. DPW Package 5-Pin X2SON Address variant (Top View)

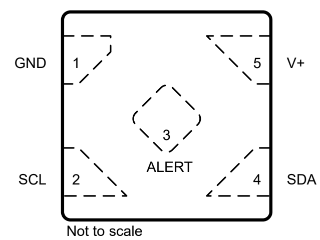


図 5-2. DPW Package 5-Pin X2SON Alert variant (Top View)

表 5-1. Pin Functions

PIN			TYPE(1)	DESCRIPTION
NAME	**NO.**	**NO.**		
GND	1	1	—	Ground **Pin-1 has curved edges**.
SCL	2	2	I	Serial clock
ADD0 (**TMP110D**)	3	—	I	Address select. Connect to GND, SCL, SDA or V+. **Only for Address variant**.
ALERT (**TMP110D0**, **TMP110D1**, **TMP110D2**, **TMP110D3**)	—	3	O	Overtemperature alert(2). Open-drain output; requires a pullup resistor. **Only for Alert variant**. **Note:** Connecting to GND if Alert pin is not used is preferred.
SDA	4	4	I/O	Serial data input. Open-drain output; requires a pullup resistor.
V+	5	5	I	Supply voltage

(1) I = Input, O = Output, I/O = Input or Output.
(2) For more information see セクション 7.3.3

6 Specifications

6.1 Absolute Maximum Ratings

Over free-air temperature range unless otherwise noted[(1)]

		MIN	MAX	UNIT
Supply voltage	V+	–0.3	6	V
Input/Output voltage	SCL, SDA, ADD0, ALERT	–0.3	6	V
Output current			±10	mA
Operating temperature, T_A		–40	125	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V+	Supply voltage	1.14	3.3	5.5	V
$V_{I/O}$	SCL, SDA, ADD0, ALERT	0		5.5	V
I_{OL}	SDA, ALERT	0		3	mA
T_A	Operating ambient temperature	-40		125	°C

6.4 Thermal Information

THERMAL METRIC[(1)]		TMP110	UNIT
		DPW	
		5-pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	230	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	194	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	158.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	20	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	158.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	108.4	°C/W
M_T	Thermal Mass	0.46	mJ/°C

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics application note*.

6.5 Electrical Characteristics

Over free-air temperature range and V+ = 1.14V to 5.5V (unless otherwise noted); Typical specifications are at T_A = 25°C and V+ = 3.3V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
TEMPERATURE SENSOR							
T_{ERR}	Accuracy (temperature error)	-40°C to 125°C	1.14V ≤ V+ ≤ 1.4V			± 2.0	°C
			1.4V < V+ ≤ 5.5V			± 1.0	°C
PSR	DC power supply rejection	V+ ≥ 1.4V			0.02		°C/V
T_{RES}	Temperature resolution				12		Bits
					62.5		m°C
T_{REPEAT}	Repeatability(1)	V+ = 3.3V 3 sigma distribution			±1		LSB
T_{LTD}	Long-term stability and drift	1000 hours at 125°C(2)			±1		LSB
t_{RESP_L}	Response time (Stirred Liquid)	2-layer FR4 PCB 1.5748 mm thickness	τ = 63% for step response from 25°C to 75°C		1.45		s
T_{HYST}	Temperature cycling and hysteresis(3)				0.0625		°C
t_{ACT}	Active conversion time	V+ ≥ 1.4V			10.25	11.25	ms
		V+ < 1.4V			10.5	12	ms
t_{VAR}	Timing variation of all device settings	V+ ≥ 1.4V		-10		10	%
		V+ < 1.4V		-15		15	%
DIGITAL INPUT/OUTPUT							
C_{IN}	Input capacitance				3		pF
V_{IH}	Input logic high	V+ < 1.4V		0.8 × V+			V
		1.4V ≤ V+		0.7 × V+			V
V_{IL}	Input logic low	V+ < 1.4V		-0.3		0.2 × V+	V
		1.4V ≤ V+		-0.3		0.3 × V+	V
V_{HYST}	Hysteresis				0.1		V
I_{IN}	Input current					± 0.1	µA
V_{OL}	Output logic	V+ ≥ 1.4V	I_{OL} = –3mA		0.13	0.4	V
		V+ < 1.4V	I_{OL} = –0.75mA			0.2	V
POWER SUPPLY							
I_{DD_ACTIVE}	Supply current during active conversion	Active Conversion, serial bus idle			55	90	µA
I_{DD_AVG}	Average current consumption	Continous conversion mode 1Hz conversion period	Serial bus idle		3.2		µA
			SCL = 1MHz		13.5		µA
I_{DD_SB}	Standby current(4)	Continous conversion mode Serial bus idle			2.6	5	µA
I_{DD_SD}	Shutdown current	T_A = +25°C, Serial bus inactive			0.15	0.35	µA
		T_A = -40°C to 125°C				1.5	µA
		Serial bus active, SCL frequency = 400kHz			5.5		µA
		Serial bus active, SCL frequency = 1MHz			13		µA
V_{POR}	Power-on reset threshold voltage	Supply rising			1.02	1.06	V
	Brownout detect	Supply falling		0.94	0.97		V
t_{INIT}	Power-on reset time				0.5		ms

6.5 Electrical Characteristics (続き)

Over free-air temperature range and V+ = 1.14V to 5.5V (unless otherwise noted); Typical specifications are at T_A = 25°C and V+ = 3.3V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{RESET}	Reset Time	General Call Reset		0.1		ms

(1) Repeatability is the ability to reproduce a reading when the measured temperature is applied consecutively, under the same conditions.
(2) Long term stability is determined using accelerated operational life testing at a junction temperature of 150°C.
(3) Hysteresis is defined as the ability to reproduce a temperature reading as the temperature varies from room → hot →room→cold→ room. The temperatures used for this test are -40°C, 25°C, and 125°C.
(4) Quiescent current between periods

6.6 I²C Interface Timing

minimum and maximum specifications are over –40°C to 125°C and V+ = 1.14V to 5.5V (unless otherwise noted)[(1)]

		FAST MODE		FAST MODE PLUS		UNIT
		MIN	MAX	MIN	MAX	
$f_{(SCL)}$	SCL operating frequency	1	400	1	1000	kHz
$t_{(BUF)}$	Bus-free time between STOP and START conditions	0.6		0.5		µs
$t_{(SUSTA)}$	Repeated START condition setup time	0.6		0.26		µs
$t_{(HDSTA)}$	Hold time after repeated START condition. After this period, the first clock is generated.	0.6		0.26		µs
$t_{(SUSTO)}$	STOP condition setup time	0.6		0.26		µs
$t_{(HDDAT)}$	Data hold time[(2)]	100	900	12	150	ns
$t_{(SUDAT)}$	Data setup time	100		50		ns
$t_{(LOW)}$	SCL clock low period	1.3		0.5		µs
$t_{(HIGH)}$	SCL clock high period	0.6		0.26		µs
$t_{(VDAT)}$	Data valid time (data response time)[(3)]		0.9		0.45	µs
t_R	SDA, SCL rise time		300		120	ns
t_F	SDA, SCL fall time		300	20 x (V+ / 5.5V)	120	ns
$t_{timeout}$	Timeout (SCL = GND or SDA = GND)	30		30		ms
t_{LPF}	Glitch suppression filter	50		50		ns

(1) The controller and device have the same V+ value. Values are based on statistical analysis of samples tested during initial release.
(2) The maximum $t_{(HDDAT)}$ can be 0.9µs for fast mode, and is less than the maximum $t_{(VDAT)}$ by a transition time.
(3) $t_{(VDAT)}$ = time for data signal from SCL LOW to SDA output (HIGH to LOW, depending on which is worse).

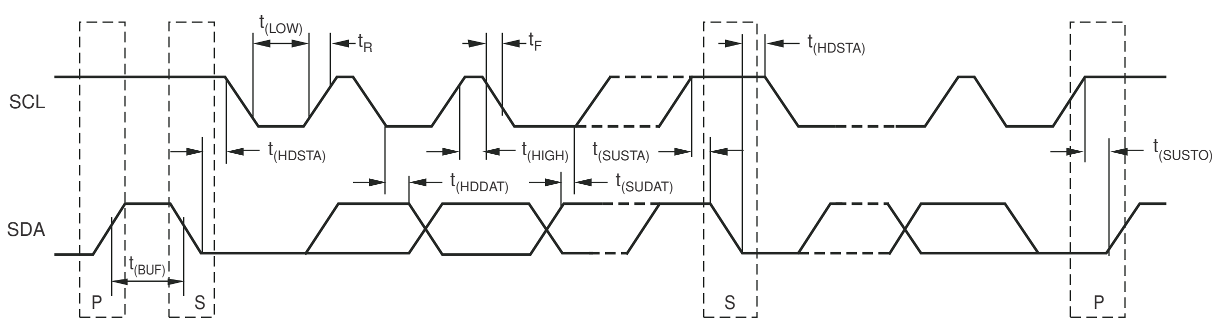


図 6-1. Two-Wire Timing Diagram

6.8 Typical Characteristics

at T_A = 25°C and V_+ = 3.3V (unless otherwise noted)

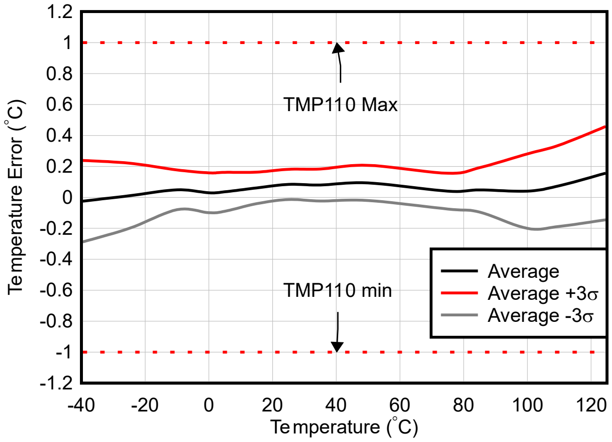


図 6-2. Temperature Error vs Temperature

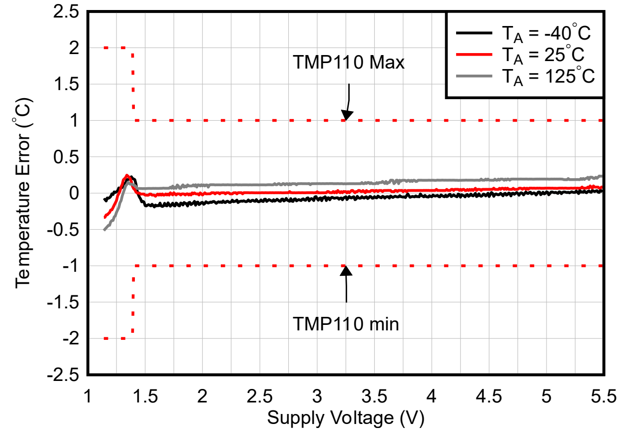


図 6-3. Temperature Error vs Supply Voltage

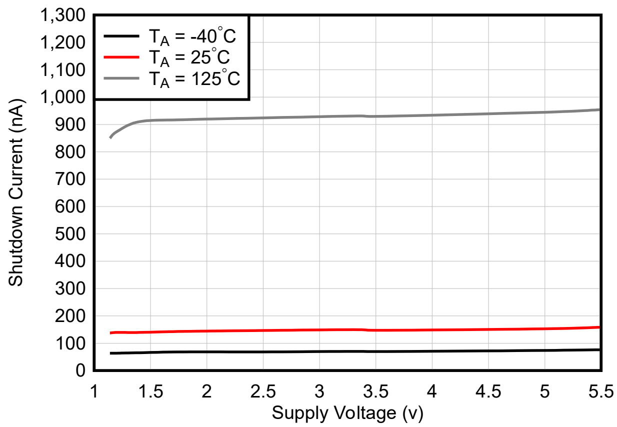
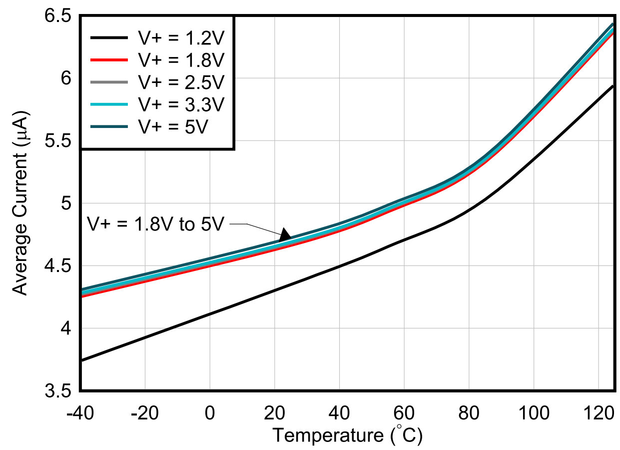


図 6-4. Shutdown Current vs Supply Voltage



Four conversions per second (continuous conversion mode)

図 6-5. Average Quiescent Current vs Temperature

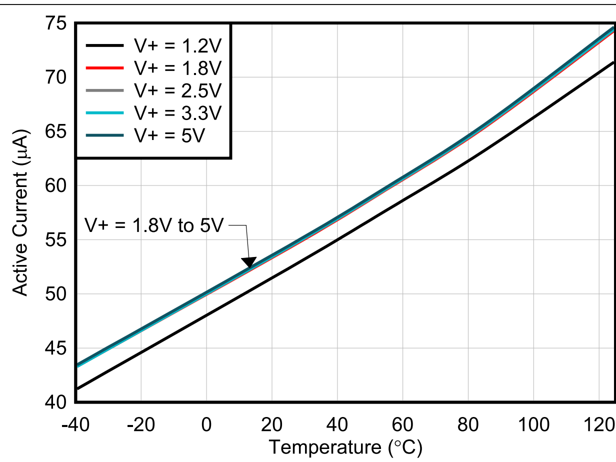


図 6-6. Active Conversion Current vs Temperature

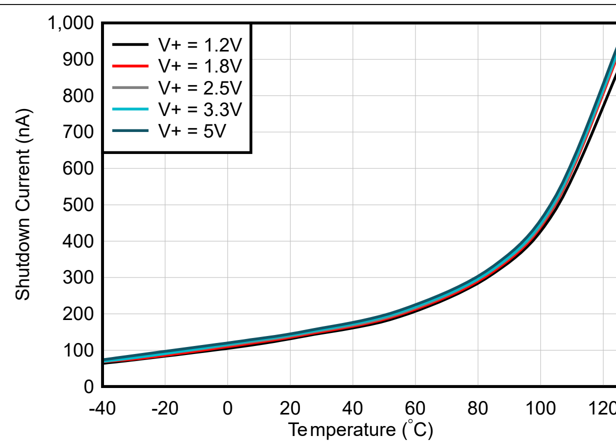


図 6-7. Shutdown Current vs Temperature

6.8 Typical Characteristics (continued)

at T_A = 25°C and V_+ = 3.3V (unless otherwise noted)

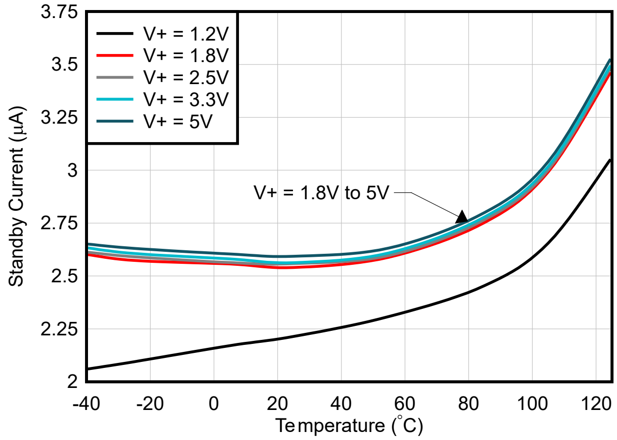


図 6-8. Standby Current vs Temperature

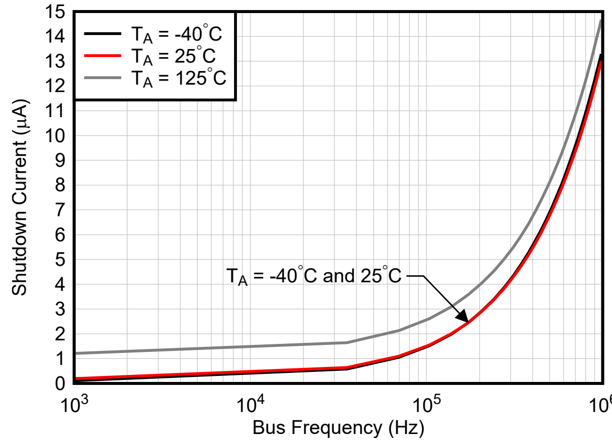


図 6-9. Shutdown Current vs Bus Frequency (Temperature at 3.3V Supply)

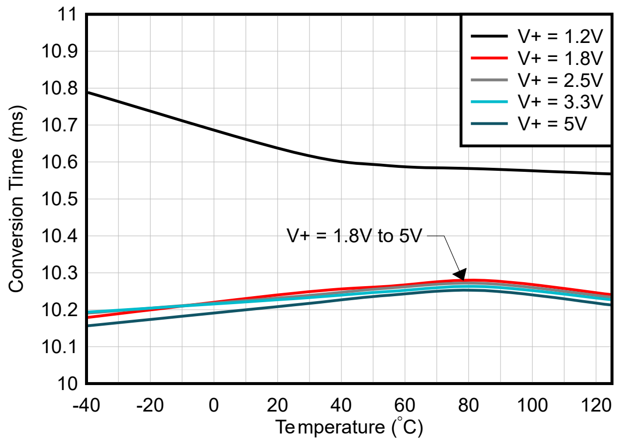


図 6-10. Conversion Time vs Temperature

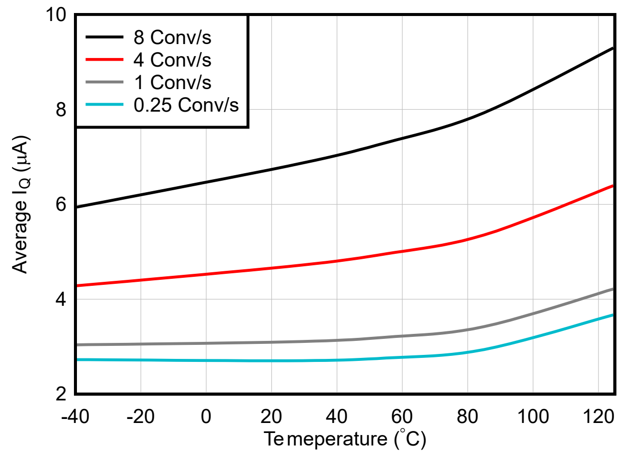


図 6-11. Average Supply Current vs Conversion Rate

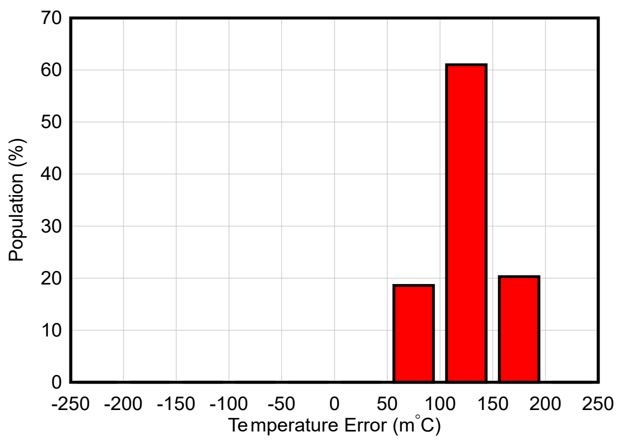


図 6-12. Temperature Error at 25°C

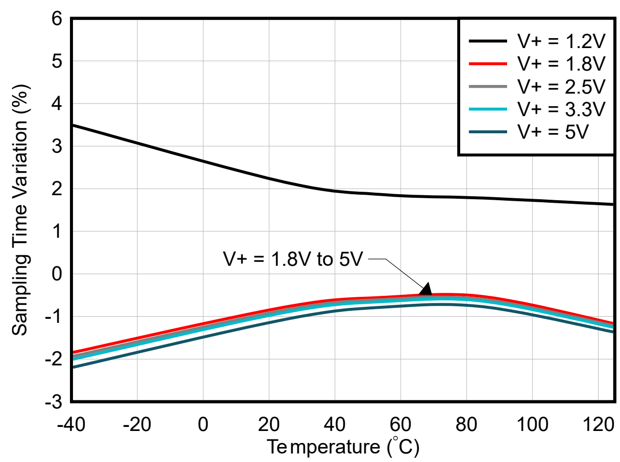


図 6-13. Sampling Time vs Temperature

6.8 Typical Characteristics (continued)

at T_A = 25°C and V_+ = 3.3V (unless otherwise noted)

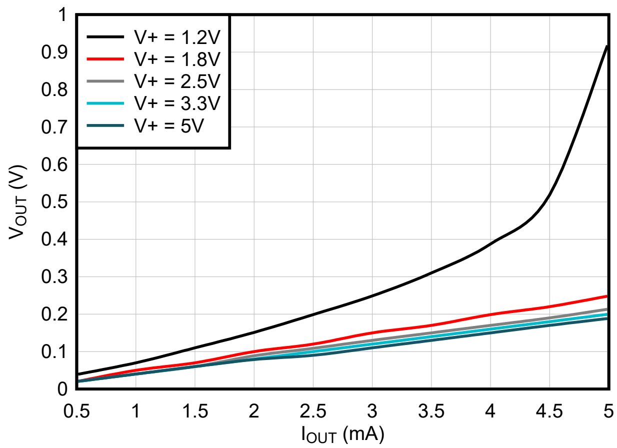


図 6-14. ALERT Pin Output Voltage vs Pin Sink Current

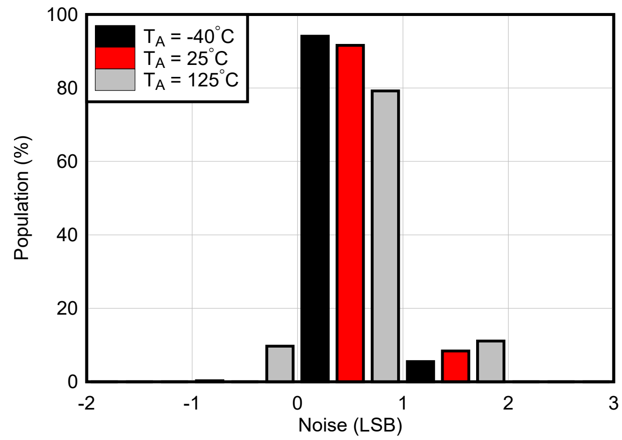


図 6-15. Noise Histogram (Oil bath measurement)

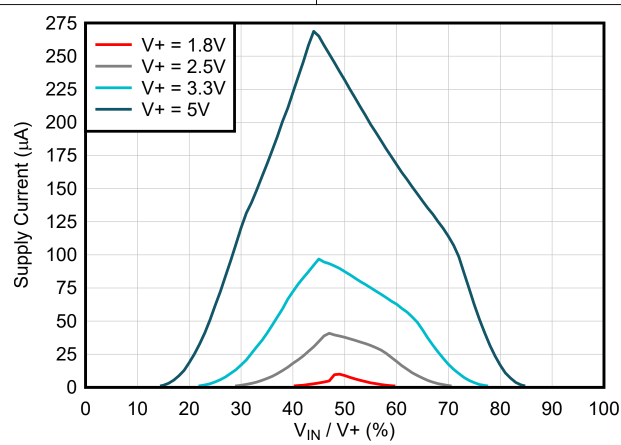


図 6-16. Supply Current vs Input Cell Input Voltage

7 Detailed Description

7.1 Overview

The TMP110 is a digital output temperature sensor that comes factory calibrated for accuracy. The device features a two-wire, SMBus and I^{2}C compatible interface with two modes of operation: continuous conversion mode and one-shot conversion mode, designed for thermal management and thermal protection applications. The TMP110 also includes an alert status register with individual high and low thresholds. Depending on the application requirement the 5th pin is either a device address input pin for multiple devices on the same bus or an open-drain alert output pin for thermal switch application.

7.2 Functional Block Diagram

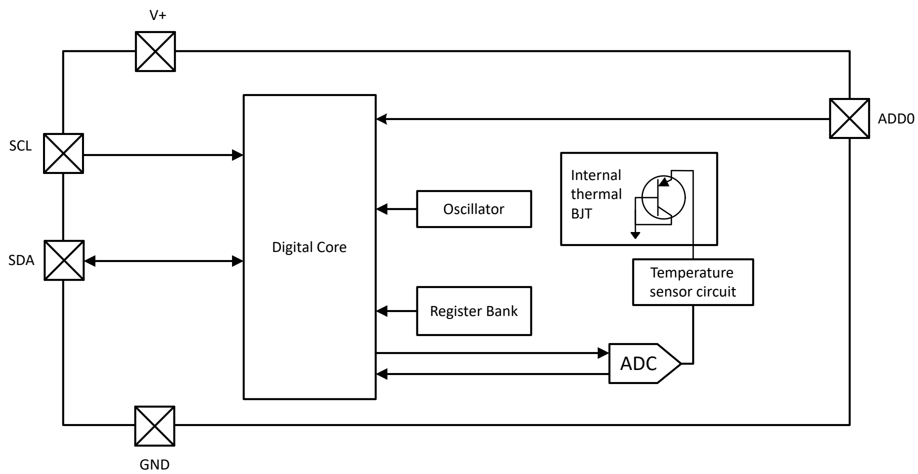


図 7-1. Address Variant

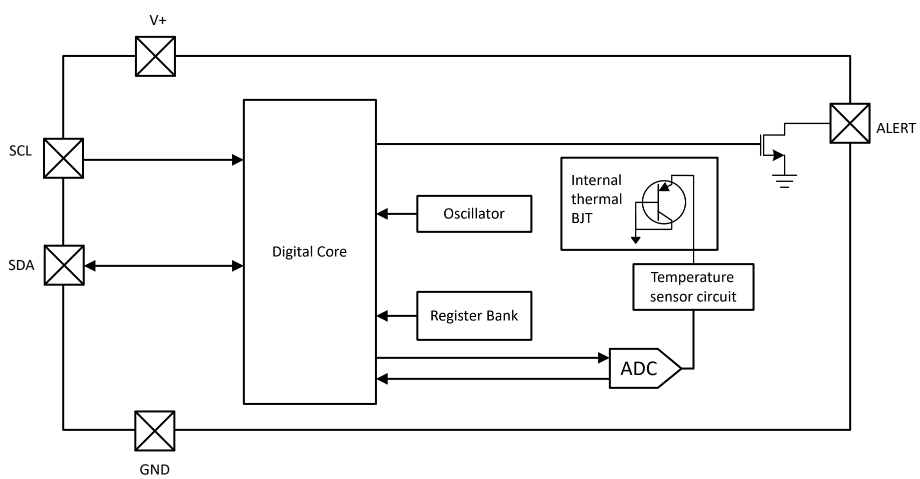


図 7-2. Alert Variant

7.3 Feature Description

7.3.1 Digital Temperature Output

The digital output from each temperature measurement is stored in the read-only temperature register. The temperature register of the TMP110 device is configured as a 12-bit, read-only register (configuration register EM bit = 0), or as a 13-bit, read-only register (configuration register EM bit = 1) that stores the output of the most recent conversion. Note that the EM bit defaults to 0 (12-bit format). As this value limits the highest temperature digital code, the device output is as shown in 表 7-1.

表 7-1. 12/13-Bit Temperature Data Guidelines

EM Bit	Temperature Bit Length	Q Notation	LSB (°C)	Range (+)
0	12	4	0.0625	127.93475
1	13	4	0.0625	256

Two bytes must be read to obtain data. Byte 1 is the most significant byte (MSB), followed by byte 2, the least significant byte (LSB). The first 12 bits (13 bits in extended mode) are used to indicate temperature. The least significant byte does not have to be read if that information is not needed. The data format for temperature is summarized in 表 7-2 and 表 7-3. One LSB equals 0.0625°C. Negative numbers are represented in binary twos-complement format. Following power-up or reset, the temperature register reads 0°C until the first conversion is complete. Bit D0 of byte 2 indicates normal mode (EM bit = 0) or extended mode (EM bit = 1), and can be used to distinguish between the two temperature register data formats. The unused bits in the temperature register always read 0.

表 7-2. 12-Bit Temperature Data Format

TEMPERATURE (°C)	DIGITAL OUTPUT (BINARY)	HEX
>127.9375	0111 1111 1111	7FF
127.9375	0111 1111 1111	7FF
100	0110 0100 0000	640
80	0101 0000 0000	500
75	0100 1011 0000	4B0
50	0011 0010 0000	320
25	0001 1001 0000	190
0.25	0000 0000 0100	004
0.0625	0000 0000 0001	001
0	0000 0000 0000	000
-0.0625	1111 1111 1111	FFF
–0.25	1111 1111 1100	FFC
–25	1110 0111 0000	E70
–55	1100 1001 0000	C90

表 7-2 does not list all temperatures. Use the following rules to obtain the digital data format for a given temperature or the temperature for a given digital data format.

To convert positive temperatures to a digital data format:

1. Divide the temperature by the resolution
2. Convert the result to binary code with a 12-bit, left-justified format, and MSB = 0 to denote a positive sign.

   Example: (50°C) / (0.0625°C / LSB) = 800 = 320h = 0011 0010 0000

To convert a positive digital data format to temperature:

1. Convert the 12-bit, left-justified binary temperature result, with the MSB = 0 to denote a positive sign, to a decimal number.
2. Multiply the decimal number by the resolution to obtain the positive temperature.

   Example: 0011 0010 0000 = 320h = 800 × (0.0625°C / LSB) = 50°C

To convert negative temperatures to a digital data format:

1. Divide the absolute value of the temperature by the resolution, and convert the result to binary code with a 12-bit, left-justified format.
2. Generate the twos complement of the result by complementing the binary number and adding one. Denote a negative number with MSB = 1.

   Example: (|–25°C|) / (0.0625°C / LSB) = 400 = 190h = 0001 1001 0000

   Two's complement format: 1110 0110 1111 + 1 = 1110 0111 0000

To convert a negative digital data format to temperature:

1. Generate the twos compliment of the 12-bit, left-justified binary number of the temperature result (with MSB = 1, denoting negative temperature result) by complementing the binary number and adding one. This represents the binary number of the absolute value of the temperature.
2. Convert to decimal number and multiply by the resolution to get the absolute temperature, then multiply by –1 for the negative sign.

   Example: 1110 0111 0000 has twos compliment of 0001 1001 0000 = 0001 1000 1111 + 1

   Convert to temperature: 0001 1001 0000 = 190h = 400; 400 × (0.0625°C / LSB) = 25°C = (|–25°C|); (|–25°C|) × (–1) = –25°C

表 7-3. 13-Bit Temperature Data Format

TEMPERATURE (°C)	DIGITAL OUTPUT (BINARY)	HEX
150	0 1001 0110 0000	0960
128	0 1000 0000 0000	0800
127.9375	0 0111 1111 1111	07FF
100	0 0110 0100 0000	0640
80	0 0101 0000 0000	0500
75	0 0100 1011 0000	04B0
50	0 0011 0010 0000	0320
25	0 0001 1001 0000	0190
0.25	0 0000 0000 0100	0004
0.0625	0 0000 0000 0001	0001
0	0 0000 0000 0000	0000
–0.0625	1 1111 1111 1111	1FFF
–0.25	1 1111 1111 1100	1FFC
–25	1 1110 0111 0000	1E70
–55	1 1100 1001 0000	1C90

7.3.2 Decoding Temperature Data

The TMP110 temperature registers use a 12-bit format. The 12 bits are aligned to the left side, or most significant side, of the 16-bit word. The four unused bits are on the right side, or least significant side. For this reason, a shift is needed to discard the extra bits. 2's Complement is employed to describe negative temperatures. C code can easily convert the 2's Complement data when the data is typecast into the correct signed data type. Q notation describes the number of bits which represent a fractional result. 4 bits of fractional data, known as Q4, offers 0.0625°C resolution.

表 7-4. 12-Bit Q4 Encoding Parameters

PARAMETER	VALUE
Bits	12
Q	4
Resolution	0.0625

表 7-4. 12-Bit Q4 Encoding Parameters (続き)

PARAMETER	VALUE
Range (+)	127.9375
Range (–)	-128
25˚C	0x0190

表 7-5. 12-Bit Q4 Bit Values in °C

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sign	64	32	16	8	4	2	1	0.5	0.25	0.125	0.0625	-	-	-	-
-128	64	32	16	8	4	2	1	1/2	1/4	1/8	1/16	-	-	-	-
-2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	-	-	-	-

```
/* 12-bit format will have 4 bits discarded by right shift
 q4 is 0.062500 resolution
 the following bytes represent 24.5C */
uint8_t byte1 = 0x18;
uint8_t byte2 = 0x80;
float f = (((int8_t) byte1 << 8 | byte2) >> 4) * 0.0625f;
int mC = (((int8_t) byte1 << 8 | byte2) >> 4) * 1000 >> 4;
int C = (int8_t) byte1;
```

Similarly, in extended mode, the temperature register is extended to a 13-bit format with the same resolution (Q4). This changes the range and effective bits but the resolution remains the same. For this reason, the bit shift also changes. Encoding and C code examples for extended mode are shown below.

表 7-6. 13-Bit Q4 Encoding Parameters

PARAMETER	VALUE
Bits	13
Q	4
Resolution	0.0625
Range (+)	255.9375
Range (–)	-256
25˚C	0xC80

表 7-7. 13-Bit Q4 Bit Values in °C

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sign	128	64	32	16	8	4	2	1	0.5	0.25	0.125	0.0625	-	-	-
-256	128	64	32	16	8	4	2	1	1/2	1/4	1/8	1/16	-	-	-
-2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	-	-	-

```
/* 13-bit format will have 3 bits discarded by right shift
 q4 is 0.062500 resolution
 the following bytes represent 24.5C */
uint8_t byte1 = 0xC;
uint8_t byte2 = 0x40;
float f = (((int8_t) byte1 << 8 | byte2) >> 3) * 0.0625f;
int mC = (((int8_t) byte1 << 8 | byte2) >> 3) * 1000 >> 4;
int C = (((int8_t) byte1 << 8 | byte2) >> 3) >> 4;
```

7.3.3 Temperature Limits and Alert

The TMP110 has alert feature and uses the TLow_limit register for low threshold comparison and THigh_Limit register for high threshold comparison. The alert limit is programmed in the TMP110 in a 12-bit or 13-bit two's complement format based on the Extended_Mode setting in the configuration register, with a resolution of 62.5 m°C. At the end of each temperature conversion, the temperature result is compared with the high limit and low limit registers, and the alert status flag and/or ALERT pin is updated.

The alert status flag in configuration register and/or the ALERT pin are updated based on the Alert_Mode and Polarity bit setting in the configuration register after every temperature conversion.

As shown in 図 7-3, in comparator mode (Alert_Mode = 0b), the ALERT pin and status flag become active when the temperature equals or exceeds the value in THigh_Limit for Fault number of consecutive conversions. The ALERT pin and status flag remain active until the temperature falls below the TLow_Limit for the same number of consecutive conversions.

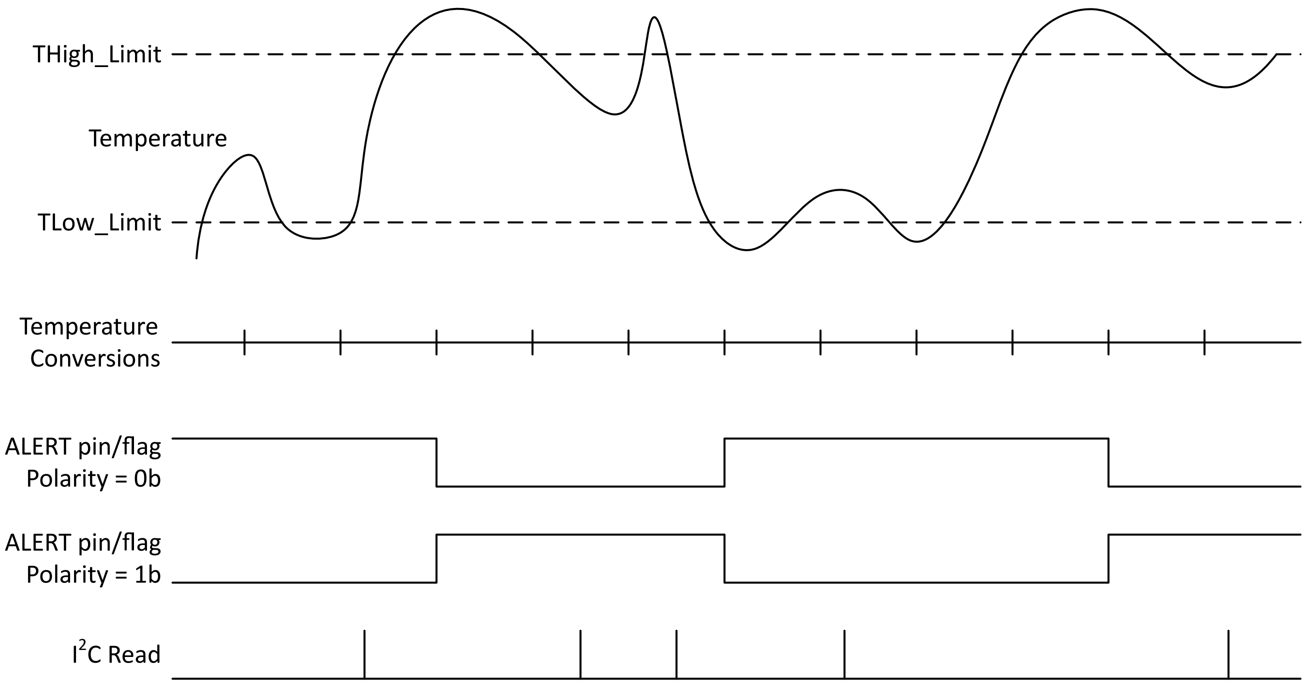


図 7-3. Comparator Mode

As shown in 図 7-4, in alert mode (Alert_Mode = 1b), the ALERT pin becomes active only when the temperature equals or exceeds the THigh_Limit for Fault number of consecutive conversion. The ALERT pin remains active, until a read operation of any register occurs, or the device responds to the SMBus Alert Response. When the ALERT pin is cleared, the pin becomes active only when the temperature is less than the TLow_Limit for Fault number of consecutive conversion and remains active, until a read operation of any register occurs, or the device responds to the SMBus Alert Response. When the ALERT pin is cleared after a TLow_Limit crossing, the above cycle repeats. The ALERT pin and status can also be cleared by issuing the General Call Reset command.

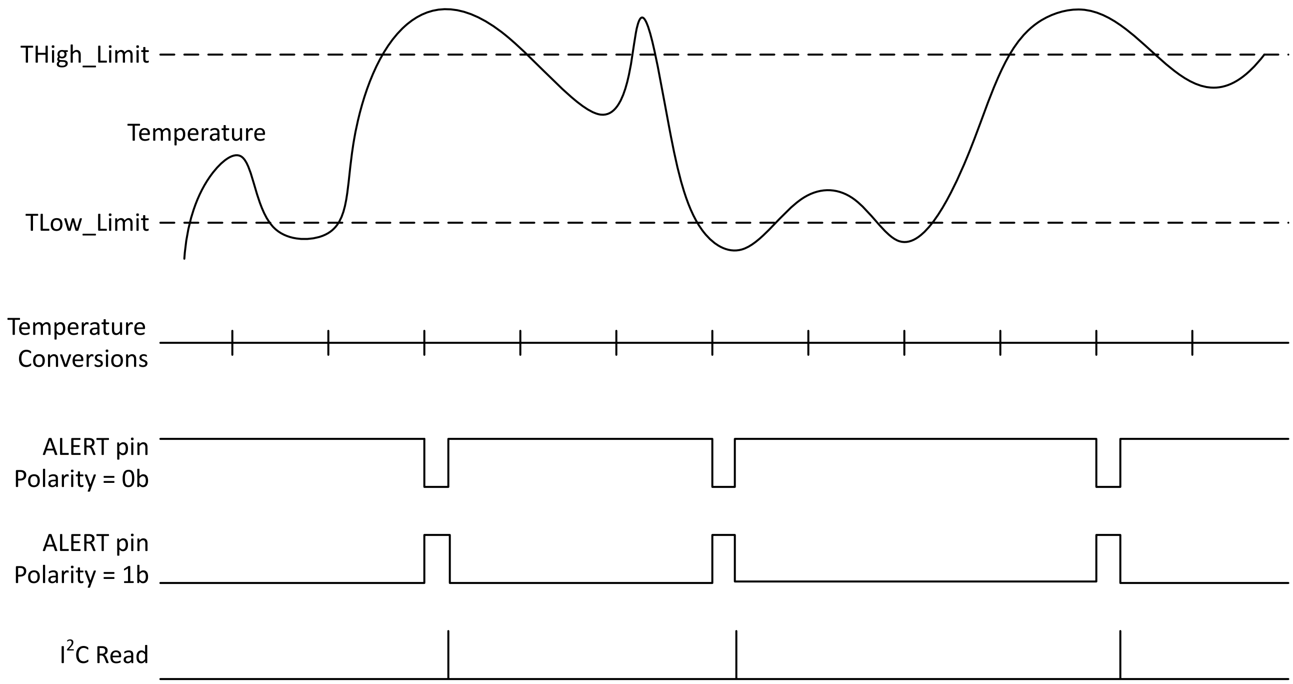


図 7-4. Alert Mode

7.4 Device Functional Modes

The TMP110 can be configured to operate in continuous or one-shot mode. This flexibility enables users to balance the requirements of power efficiency and performance.

7.4.1 Continuous-Conversion Mode

When the Shutdown bit is set to 0b in the configuration register, the device operates in continuous conversion mode. 図 7-5 shows the device in a continuous conversion cycle. In this mode, the device performs conversion at fixed intervals and updates the temperature result register, ALERT pin and flag at the end of every conversion. The typical active conversion time is around 10ms.

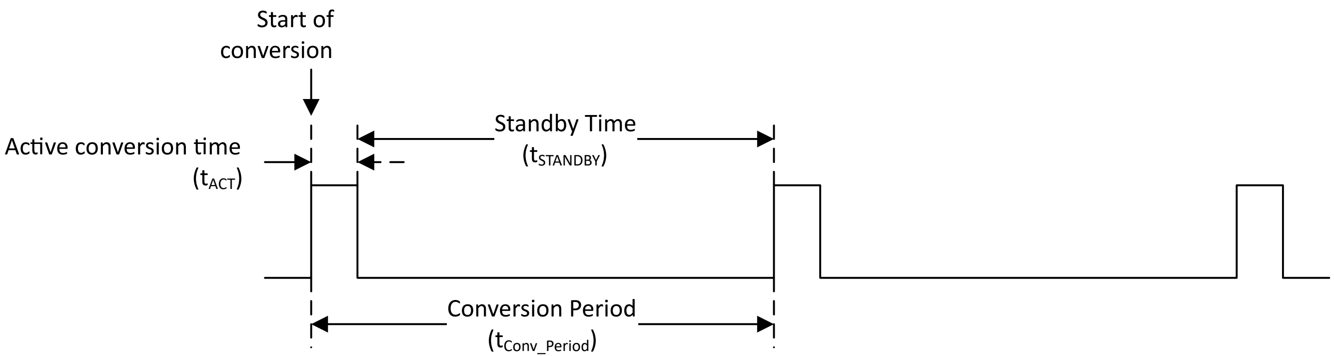


図 7-5. Continuous Conversion Cycle Timing Diagram

The Conversion_Rate[1:0] bits in the configuration register controls the rate at which the conversions are performed. The device typically consumes 55μA during conversion and 2.6μA during the low power standby period. By decreasing the rate at which the conversion are performed, the application can benefit from reduced average current consumption in continuous mode.

Use 式 1 to calculate the average current in continuous mode.

$$\text{Average Current} = ((I_{DD\_ACTIVE} \times t_{ACT}) + (I_{DD\_SB} \times t_{STANDBY})) / t_{Conv\_Period} \quad (1)$$

Where

- t_{ACT} = Active conversion time
- t_{Conv_Period} = Conversion Period
- $t_{STANDBY}$ = Standby time between conversions calculated as t_{Conv_Period} - t_{ACT}

7.4.2 One-Shot Mode

When a 1 is written to the One_Shot bit in the configuration register, the TMP110 immediately starts a one-shot temperature conversion as shown in 図 7-6. Requesting another conversion when the TMP110 is performing a temperature conversion, the device does not stop the active conversion. After completing the one-shot conversion the TMP110 enters shutdown mode, and the One_Shot bit is set to 1b.

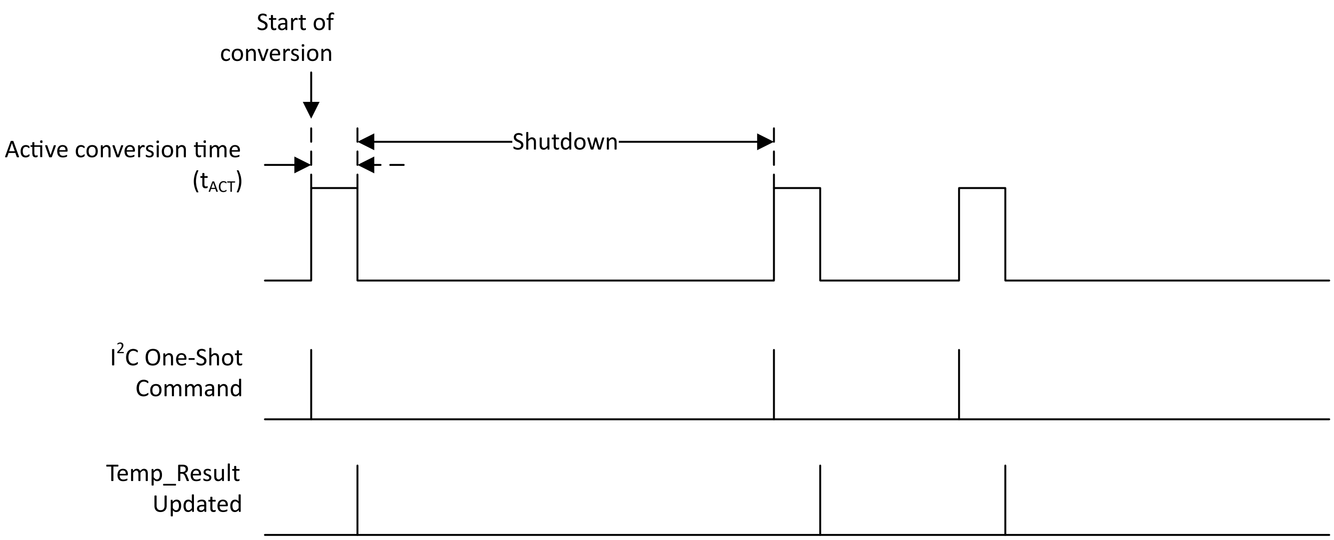


図 7-6. One-Shot Timing Diagram

The one-shot conversion is only supported when the Shutdown bit is set to 1b. Due to the short conversion time, the TMP110 device achieves a higher conversion rate. A single conversion typically takes 10ms and a read can take place in less than 20µs. When using the one-shot mode, 50 or more conversions per second are possible.

7.5 Programming

7.5.1 Serial Interface

The TMP110 has a standard bidirectional I^2C interface that is controlled by a controller device in order to be configured or read the status of TMP110 device. Each target device on the I^2C bus has a specific device address to differentiate between other target devices that are on the same I^2C bus. Many target devices require configuration upon start-up to set the behavior of the device. This is typically done when the controller accesses internal register map of the target, which have unique register pointer. A device can have one or multiple registers where data is stored, written, or read. The TMP110 includes 50ns glitch suppression filters, allowing the device to coexist on an I3C mixed bus. The TMP110 supports transmission data rates up to 1MHz.

7.5.2 Bus Overview

The physical I^2C interface consists of the serial clock (SCL) and serial data (SDA) lines. The SDA line must be connected to a supply through a pullup resistor. The size of the pullup resistor is determined by the amount of capacitance on the I^2C lines, the communication frequency and I^2C bus voltage. For further details, see the I^2C Pullup Resistor Calculation application note. Data transfer can be initiated only when the bus is idle. A bus is considered idle if both SDA and SCL lines are high after a STOP condition or time out events (see 図 7-7 and 図 7-8).

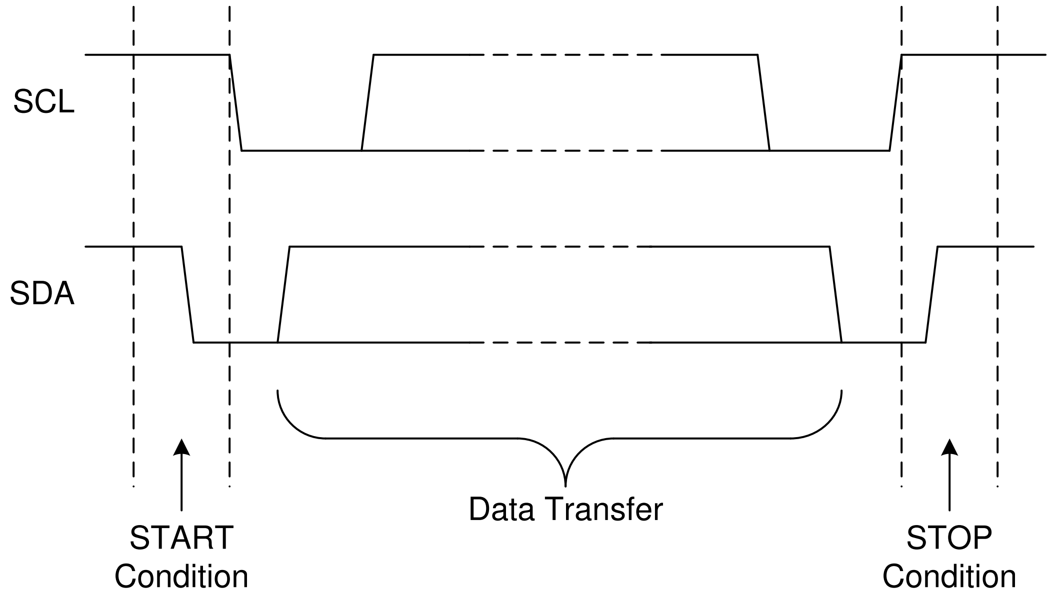


図 7-7. Definition of Start and Stop Conditions

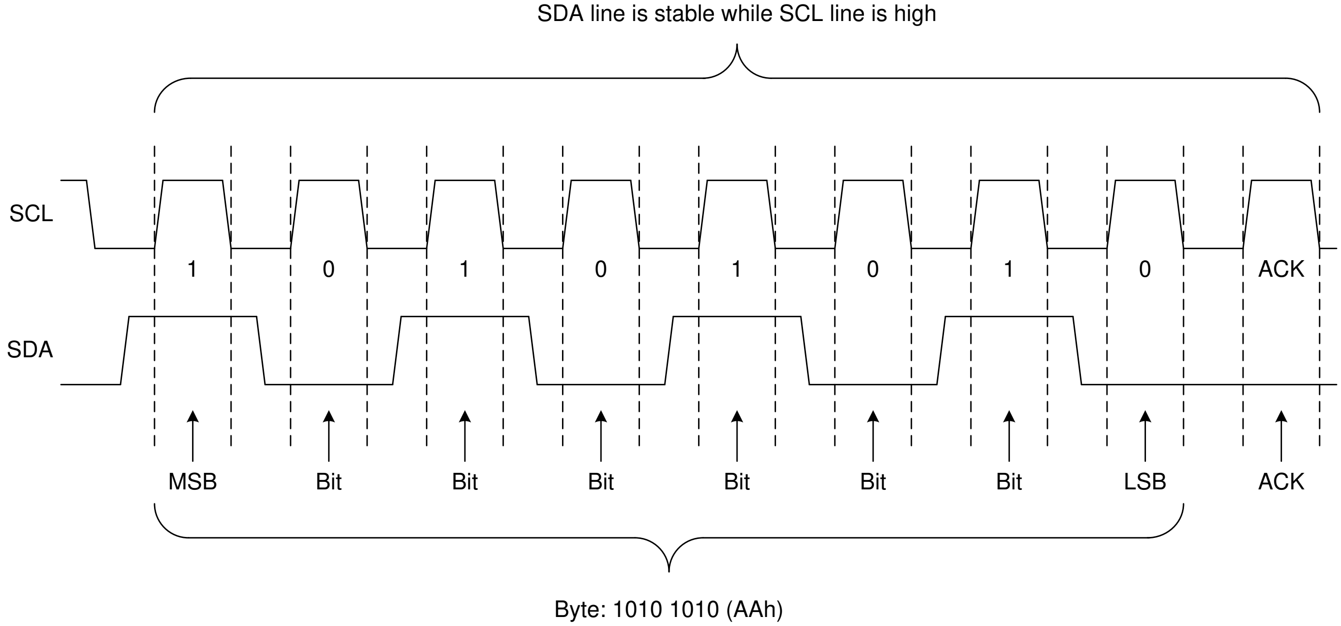


図 7-8. Bit Transfer

7.5.3 Device Address

To communicate with the TMP110, the controller must first address target devices through an address byte. The address byte has seven address bits and a read-write (R/W) bit that indicates the intent of executing a read or write operation. The TMP110D features an address pin to allow up to four devices to be addressed on a single bus. 表 7-8 describes the pin logic levels used to properly connect up to eight devices on the same I^{2}C bus. This table also describes four different address options available when ALERT pin is used.

表 7-8. Address and Alert Variant Device Target Address

DEVICE ORDERABLE		ADD0 PIN CONNECTION	DEVICE I²C BUS ADDRESS	DEVICE I²C BUS ADDRESS (7-bit Hex)
Address Variant	TMP110D	GND	1000000	40h
		V+	1000001	41h
		SDA	1000010	42h
		SCL	1000011	43h
Alert Variant	TMP110D0	N/A	1001000	48h
	TMP110D1		1001001	49h
	TMP110D2		1001010	4Ah
	TMP110D3		1001011	4Bh

7.5.4 Bus Transactions

7.5.4.1 Writes

To write on the I²C bus, the controller sends a START condition on the bus with the address of the target, as well as the last bit (the R/W bit) set to 0b, which signifies a write. The target acknowledges, letting the controller know the target is ready. After this operation, the controller starts sending the register pointer and data to the target, and the controller terminates the transmission with a STOP condition.

Writes to read-only registers or register locations outside of the register map is ignored. The TMP110 still performs and acknowledge when writing outside of the register map. 図 7-9 shows an example of writing a single word write communication.

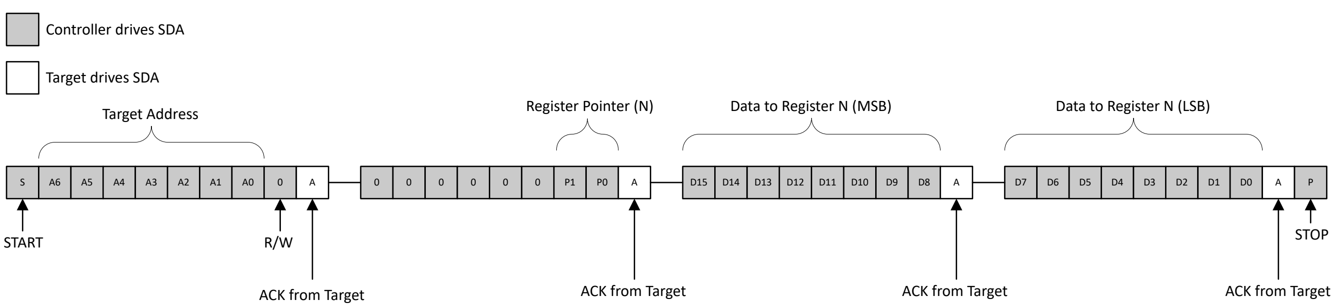


図 7-9. Write to Single Register

7.5.4.2 Reads

For a read operation the controller sends a START condition, followed by the target address with the R/W bit set to 0b (signifying a write). The target acknowledges the write request, and the controller sends the register pointer. The controller initiates a restart followed by the target address with the R/W bit set to 1b (signifying a read). The controller continues to send out clock pulses but releases the SDA line so that the target can transmit data. At the end of every byte of data, the controller sends an ACK to the target, letting the target know that the controller is ready for more data. For repeated read operation from the same register (like temperature register), it is not needed to resend the register pointer. The read operation from the same register can be repeated as many time as the controller needs when the pointer is set. Once the controller has received the expected number of bytes, the controller sends a NACK, signaling to the target to halt communications and release the SDA line. The controller follows this up with a STOP condition. 図 7-10 shows an example of reading a single word from a target register.

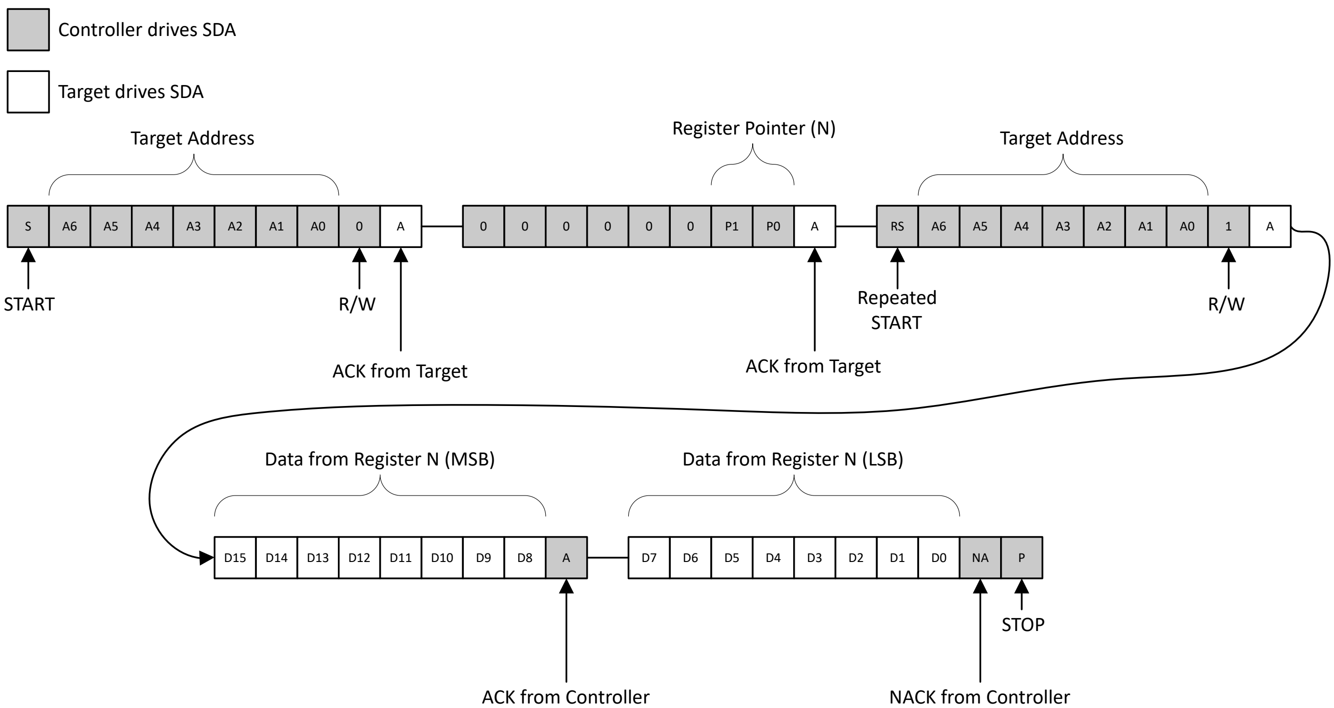


図 7-10. Read from Single Register

7.5.4.3 General Call Reset Function

The TMP110 responds to a general-call address (0000 000) if the eighth bit is 0b. The device acknowledges the general-call address and responds to commands in the second byte. If the second byte is 0000b 0110b, the TMP110 internal registers are reset to power-up values as shown in SMBus General Call Reset Timing Diagram . The serial address is unaffected by the general call reset.

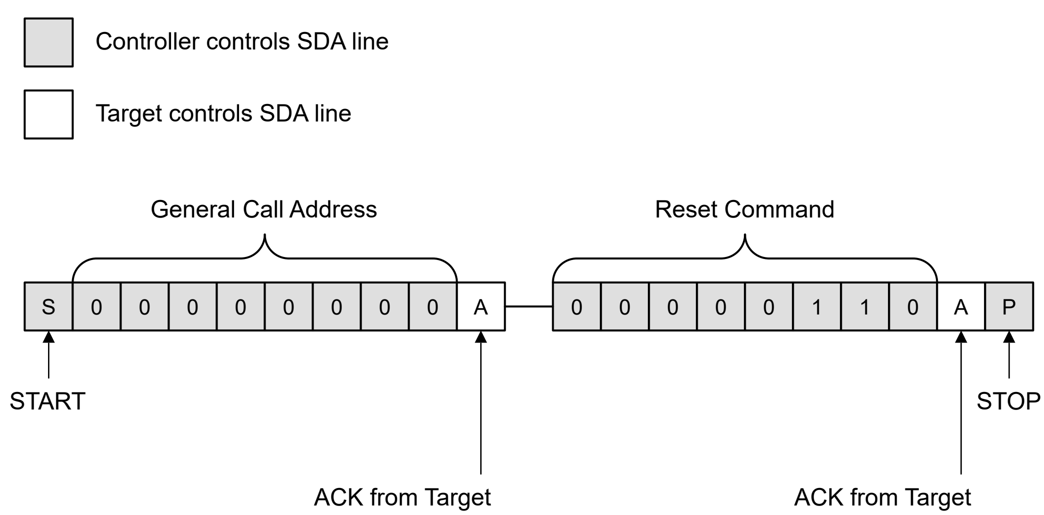


図 7-11. SMBus General Call Reset Timing Diagram

7.5.4.4 SMBus Alert Response

The TMP110 device supports the SMBus alert response. When the TMP110 operates in Alert Mode, and the ALERT pin is available, the controller can sense that an alert condition is present. Irrespective of the availability of the ALERT pin, the alert status is set. As shown in 図 7-12, if the controller sends an SMBus alert command (19h or 00011001b) on the bus, and the target is set, the device acknowledges the SMBus alert command and responds by returning the device addess on the SDA line. The eigth bit (LSB) of the device address byte indicates if the alert condition was caused by the temperature exceeding THigh_Limit or falling below the TLow_Limit. The value of the eight bit follows the Polarity bit setting.

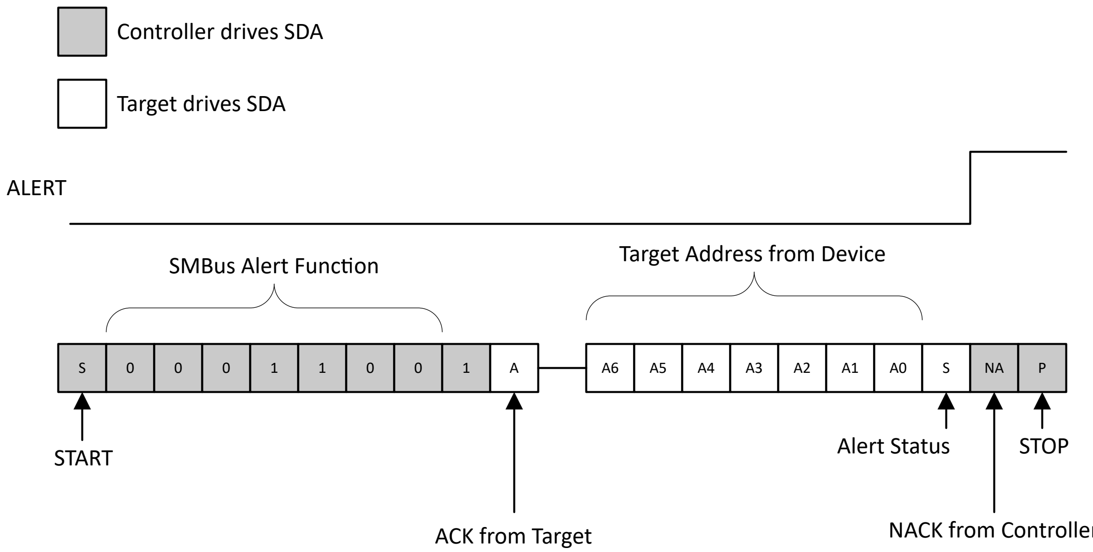


図 7-12. SMBus Alert Response

If multiple devices on the bus respond to the SMBus alert command, arbitration during the device address portion of the SMBus alert command determines which devices the ALERT pin is activated. The device with the lowest address wins the arbitration. On winning the arbitration, the TMP110 inactivates the ALERT pin and/or clears the status bit. To prevent the device with lowest I^2C address in continuous conversion mode sees the alert line and halt others with higher I^2C address to report the alert, the controller has to temporarily disable the Alert mode in device with smallest I^2C address until all alerts in the system are cleared.

7.5.4.5 Time-Out Function

The TMP110 resets the serial interface if the SCL line is held low by the controller or the SDA line is held low by the TMP110 for 30ms (typical) between a START and STOP condition. The TMP110 releases the SDA line if the SCL pin is pulled low and waits for a START condition from the controller. To avoid activating the timeout function, maintain a communication speed of at least 1kHz for the SCL operating frequency. If another device on the bus is holding the SDA pin low, the TMP110 does not reset.

7.5.4.6 Coexist on I3C Mixed Bus

A bus with both I3C and I^2C interfaces is referred to as a mixed with clock speeds up to 12.5MHz. The TMP110 is an I^2C device that can be on the same bus that has an I3C device attached as the TMP110 incorporates a spike suppression filter of 50ns on the SDA and SCL pins to avoid any interference to the bus when communicating with I3C devices.

8 Register Map

表 8-1. TMP110 Register Map

ADDRESS	TYPE	RESET	ACRONYM	REGISTER NAME	SECTION
00h	R	xxxxh	Temp_Result	Temperature result register	Go
01h	R/W	60A0h	Configuration	Configuration register	Go
02h	R/W	4B00h	TLow_Limit	Temperature low limit register	Go
03h	R/W	5000h	THigh_Limit	Temperature high limit register	Go
04h - FFh	R	xxxxh	Reserved	Reserved	

表 8-2. TMP110 Register Section/Block Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	R C	Read to Clear
R-0	R -0	Read Returns 0s
Write Type		
W	W	Write
W0CP	W 0C P	W 0 to clear Requires privileged access
Reset or Default Value		
-n		Value after reset or the default value

8.1 Temp_Result Register (address = 00h) [reset = xxxxh]

This register stores the latest temperature conversion result in a 12-bit or 13-bit two's complement format with a LSB equal to 0.0625°C depending on the Extended_Mode bit setting in the configuration register. The default format for the register at power up is normal mode.

Return to Register Map.

表 8-3. Temp_Result Register (Normal Mode)

15	14	13	12	11	10	9	8
Temp_Result[11:4]							
R-xxh							
7	6	5	4	3	2	1	0
Temp_Result[3:0]				Reserved			
R-xh				R-0000b			

表 8-4. Temp_Result Register (Extended Mode)

15	14	13	12	11	10	9	8
Temp_Result[12:5]							
R-xxh							
7	6	5	4	3	2	1	0
Temp_Result[4:0]					Reserved		
R-xxh					R-001b		

表 8-5. Temp_Result Register Field Description (Normal Mode)

Bit	Field	Type	Reset	Description
15:4	Temp_Result[11:0]	R	xxxh	12-bit temperature conversion result Temperature data is represented by a 12-bit, two's complement word with an LSB equal to 0.0625°C when Extended_Mode bit is 0b
3:0	Reserved	R	0000b	Reserved

表 8-6. Temp_Result Register Field Description (Extended Mode)

Bit	Field	Type	Reset	Description
15:3	Temp_Result[12:0]	R	xxxxh	13-bit temperature conversion result Temperature data is represented by a 13-bit, two's complement word with an LSB equal to 0.0625°C when Extended_Mode bit is 1b
2:0	Reserved	R	001b	Reserved (The LSB is 1b)

8.2 Configuration Register (address = 01h) [reset = 60A0h]

This register is used to configure the operation of the TMP110 and also provides the alert status when ALERT pin is not available on the pin-out.

Return to Register Map.

表 8-7. Configuration Register

15	14	13	12	11	10	9	8
One_Shot	Reserved		Fault[1:0]		Polarity	Alert_Mode	Shutdown
R/W-0b	R-11b		R/W-00b		R/W-0b	R/W-0b	R/W-0b
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Conversion_Rate[1:0]		Alert	Extended_Mode	Reserved			
R/W-10b		R-1b	R/W-0b	R-0000b			

表 8-8. Configuration Register Field Description

Bit	Field	Type	Reset	Description
15	One_Shot	R/W	0b	One-shot conversion trigger applicable in shutdown mode only. In continuous conversion mode the bit reads 0b. In shutdown mode the bit reads 1b. Triggering a one-shot conversion happens only when the TMP110 is in shutdown mode. 0b = Active conversion ongoing 1b = Trigger a one-shot conversion or active conversion complete
14:13	Reserved	R	11b	Reserved
12:11	Fault[1:0]	R/W	00b	The fault bit is used to count the number of consecutive conversions for which the alert condition exists before the ALERT pin is asserted or status bit is set. 00b = 1 fault 01b = 2 faults 10b = 4 faults 11b = 6 faults
10	Polarity	R/W	0b	The polarity bit allows the host to adjust the polarity of the ALERT pin/flag output. 0b = ALERT pin/flag output is active low 1b = ALERT pin/flag output is active high
9	Alert_Mode	R/W	0b	The alert mode bit indicates the how the temperature limits operate. 0b = Comparator mode 1b = Alert mode
8	Shutdown	R/W	0b	The shutdown bit is used to change the device conversion mode. 0b = Continuous conversion mode 1b = Shutdown mode
7:6	Conversion_Rate[1:0]	R/W	10b	The conversion rate bits configure the TMP110 conversion period. The default is conversion every 250ms. 00b = 4s / 0.25Hz 01b = 1s / 1Hz 10b = 0.25s / 4Hz 11b = 0.125s / 8Hz
5	Alert flag	R	1b	The alert is a read-only bit which provides the information about the alert status in comparator mode and is not affected by Alert_Mode setting. The polarity bit affects the alert flag.
4	Extended_Mode	R/W	0b	The extended mode bit configures the temperature format. 0b = Normal format with 12-bit 1b = Extended format with 13-bit
3:0	Reserved	R	0000b	Reserved

8.3 TLow_Limit Register (address = 02h) [reset = 4B00h]

This register is used to configure the low temperature alert limit of the TMP110. The limit is formatted in a 12-bit or 13-bit two's complement format with a LSB equal to 62.5 m°C depending on the Extended_Mode bit setting in the configuration register. The default value on start-up is 4B00h or 75 °C in normal mode format.

Note: If the temperature register format is changed, the low limit register value must be updated accordingly.

Return to Register Map.

表 8-9. TLow_Limit Register (Normal Mode)

15	14	13	12	11	10	9	8
TLow_Limit[11:4]							
R/W-4Bh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TLow_Limit[3:0]				Reserved			
R/W-0h				R-0000b			

表 8-10. TLow_Limit Register (Extended Mode)

15	14	13	12	11	10	9	8
TLow_Limit[12:5]							
R/W-4Bh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TLow_Limit[4:0]					Reserved		
R/W-00h					R-000b		

表 8-11. TLow_Limit Register Field Description (Normal Mode)

Bit	Field	Type	Reset	Description
15:4	TLow_Limit[11:0]	R/W	4B0h	12-bit temperature low limit setting. Temperature low limit is represented by a 12-bit, two's complement word with an LSB equal to 62.5 m°C when Extended_Mode bit is 0b. The default setting for this is 75°C.
3:0	Reserved	R	0000b	Reserved

表 8-12. TLow_Limit Register Field Description (Extended Mode)

Bit	Field	Type	Reset	Description
15:3	TLow_Limit[12:0]	R/W	4B00h	13-bit temperature low limit setting. Temperature low limit is represented by a 13-bit, two's complement word with an LSB equal to 62.5 m°C when Extended_Mode bit is 1b.
2:0	Reserved	R	000b	Reserved

8.4 THigh_Limit Register (address = 03h) [reset = 5000h]

This register is used to configure the high temperature alert limit of the TMP110. The limit is formatted in a 12-bit or 13-bit two's complement format with a LSB equal to 62.5 m°C depending on the Extended_Mode bit setting in the configuration register. The default value on start-up is 5000h or 80 °C in normal mode format.

Note: If the temperature register format is changed, the high limit register value must be updated accordingly.

Return to Register Map.

表 8-13. THigh_Limit Register (Normal Mode)

15	14	13	12	11	10	9	8
THigh_Limit[11:4]							
R/W-50h							
7	6	5	4	3	2	1	0
THigh_Limit[3:0]				Reserved			
R/W-0h				R-0000b			

表 8-14. THigh_Limit Register (Extended Mode)

23	22	21	20	19	18	17	16
THigh_Limit[12:5]							
R/W-50h							
7	6	5	4	3	2	1	0
THigh_Limit[4:0]					Reserved		
R/W-0h					R-000b		

表 8-15. THigh_Limit Register Field Description (Normal Mode)

Bit	Field	Type	Reset	Description
15:4	THigh_Limit[11:0]	R/W	500h	12-bit temperature high limit setting. Temperature high limit is represented by a 12-bit, two's complement word with an LSB equal to 62.5 m°C when Extended_Mode bit is 0b. The default setting for this is 80 °C.
3:0	Reserved	R	0000b	Reserved

表 8-16. THigh_Limit Register Field Description (Extended Mode)

Bit	Field	Type	Reset	Description
15:3	THigh_Limit[12:0]	R/W	5000h	13-bit temperature low limit setting. Temperature low limit is represented by a 13-bit, two's complement word with an LSB equal to 62.5 m°C.
2:0	Reserved	R	000b	Reserved

9 Application and Implementation

注

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9.1 Application Information

The TMP110 can be operated with a two-wire I^2C or SMBus compatible interface and features the ability to operate with a 1.2V bus voltage. The TMP110 features a uniquely small size of 0.8mm × 0.8mm with a 0.4mm z-height for space-constrained applications.

9.2 Equal I^2C Pullup and Supply Application

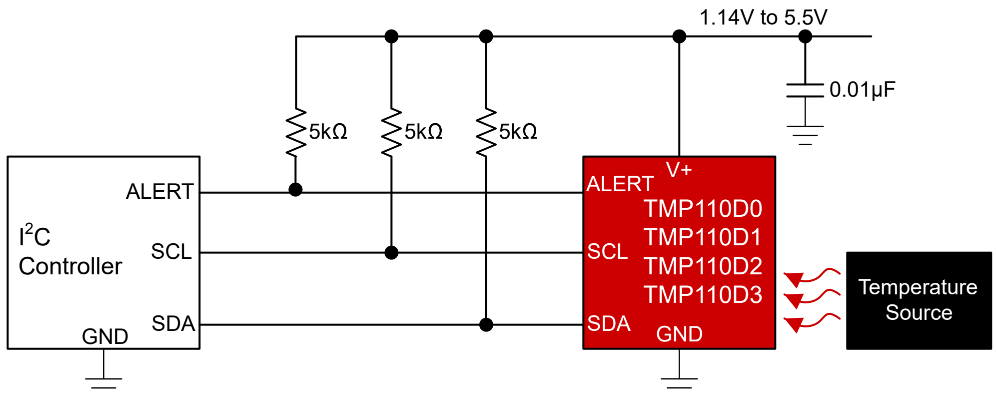

図 9-1. Equal I^2C Pullup and Supply Voltage Application

9.2.1 Design Requirements

For this design example, use the parameters listed below.

表 9-1. Design Parameters

PARAMETER	VALUE
Supply (V+)	1.14V to 5.5V
SDA, SCL V_{PULLUP}	V+
SDA SCL R_{PULLUP}	5kΩ

9.2.2 Detailed Design Procedure

The SDA and SCL pin voltage of the TMP110 can be the same as the supply voltage V+. The accuracy of the TMP110 is not affected by the pullup voltage. However, using a minimal SDA and ALERT pins pull-up current is recommended to prevent self-heating and temperature accuracy reduction. In addition, it is recommended to not have any communication on I^2C bus during temperature conversion to minimize measurement noise.

9.2.3 Application Curve

図 9-2 shows the step response of the TMP110 to a submersion in an oil bath of 75ºC from room temperature (25ºC). The time-constant, or the time for the output to reach 63% of the input step, is 1.45s. The time-constant result depends on the printed-circuit board (PCB) size that the TMP110 is mounted. For this test, the TMP110 is soldered to a two-layer PCB that measured 0.5 inches × 0.5 inches.

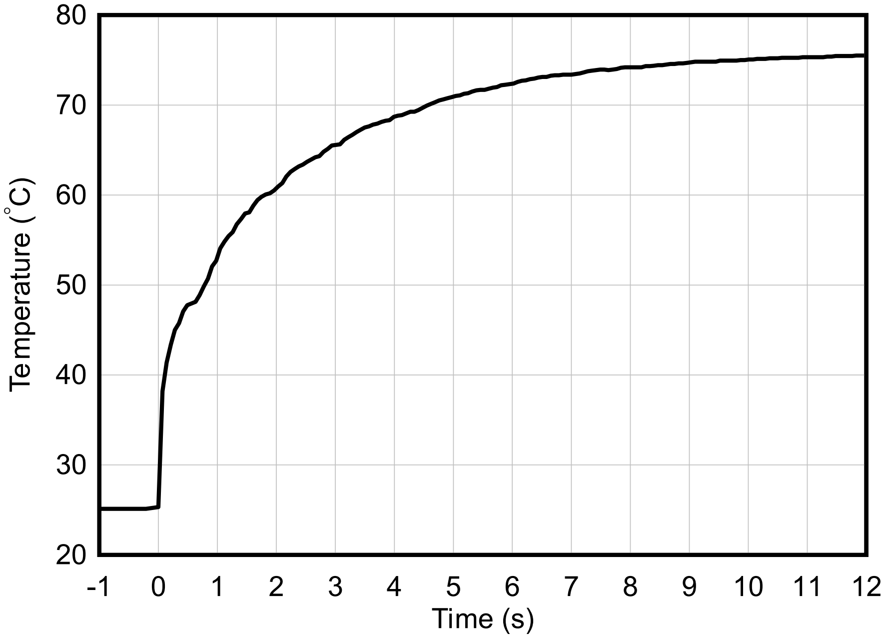

図 9-2. Temperature Step Response

9.2.4 Power Supply Recommendations

The TMP110 operates with power supply in the range of 1.14V to 5.5V. The device can measure temperature accurately in the full supply range. A power-supply bypass capacitor is required for proper operation. Place this capacitor as close as possible to the supply and ground pins of the device. A typical value for this supply bypass capacitor is 0.01µF. Applications with noisy or high-impedance power supplies can require additional decoupling capacitors to reject power-supply noise.

9.3 Layout

9.3.1 Layout Guidelines

The TMP110 is a simple device to layout. Place the power supply bypass capacitor as close to the device as possible. Pull up the open-drain output pin SDA through pullup resistor.

9.3.2 Layout Example

There are special considerations that need to be taken for the TMP110 X2SON package. These considerations are due to the center pad being electrically connected to either address or alert (depending on the orderables shown in 表 7-8) and because of the dimensions of the package and the pads. With the address option, the center pad can be directly connected with a trace on the same layer to one of the 4 edge pins for setting the device address as shown in 図 9-3.

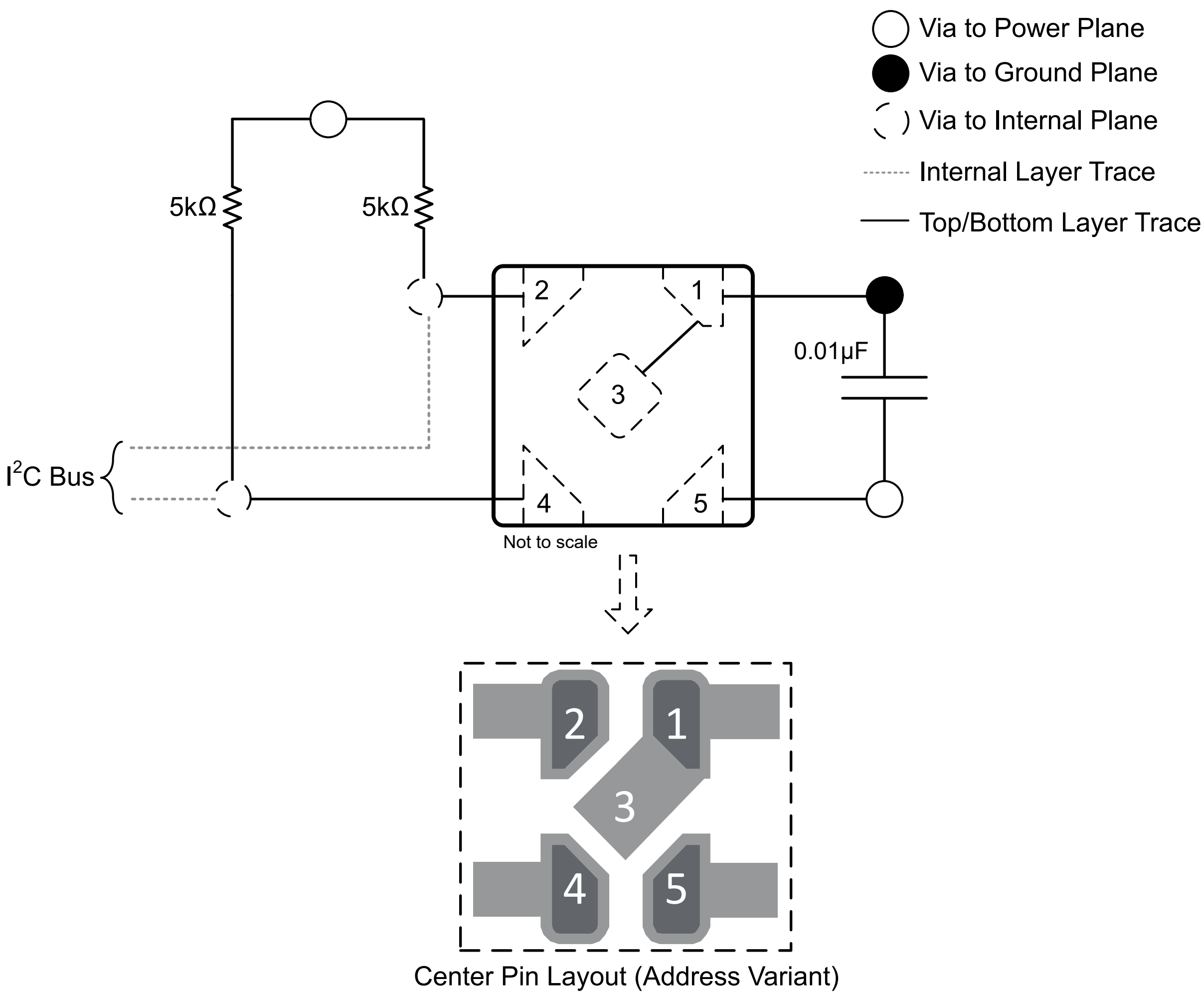

図 9-3. ADD0 Pin Layout Example

When using the ALERT pin of the device, a 4 mil trace can be routed between pins 1 and 5 or pins 2 and 4. This signal can be either routed out in between the pads or on a different layer using a via within the center pad as shown in 図 9-4. Both of these methods have constraints that must be considered as explained below. Ultimately, choosing one of these methods depends on the specifications of the board manufacturing process:

- **Option 1 (Routing in between pads):** introduces trace clearance and trace width limitations. As the maximum space between pads is 0.26mm (10.2 mil), assuming a trace width of 0.1mm (4 mil) limits the minimum clearance to 0.08mm (3.15 mil).
- **Option 2 (Routing on a different layer using a via):** has specific benefits to the user application. For instance, minimum trace clearance and trace width are higher but require a via on the center pad with specific dimensions. The via diameter must be less than 0.305mm (13.78 mil) to keep the via smaller than the center pad and a minimum drill diameter of 0.1mm (4 mil) can be assumed to avoid manufacturing issues. With this scenario, a minimum annular ring width specification of 0.125mm (5 mil) is required: Anullar Ring Width (mm) = (0.305-0.1)/2.

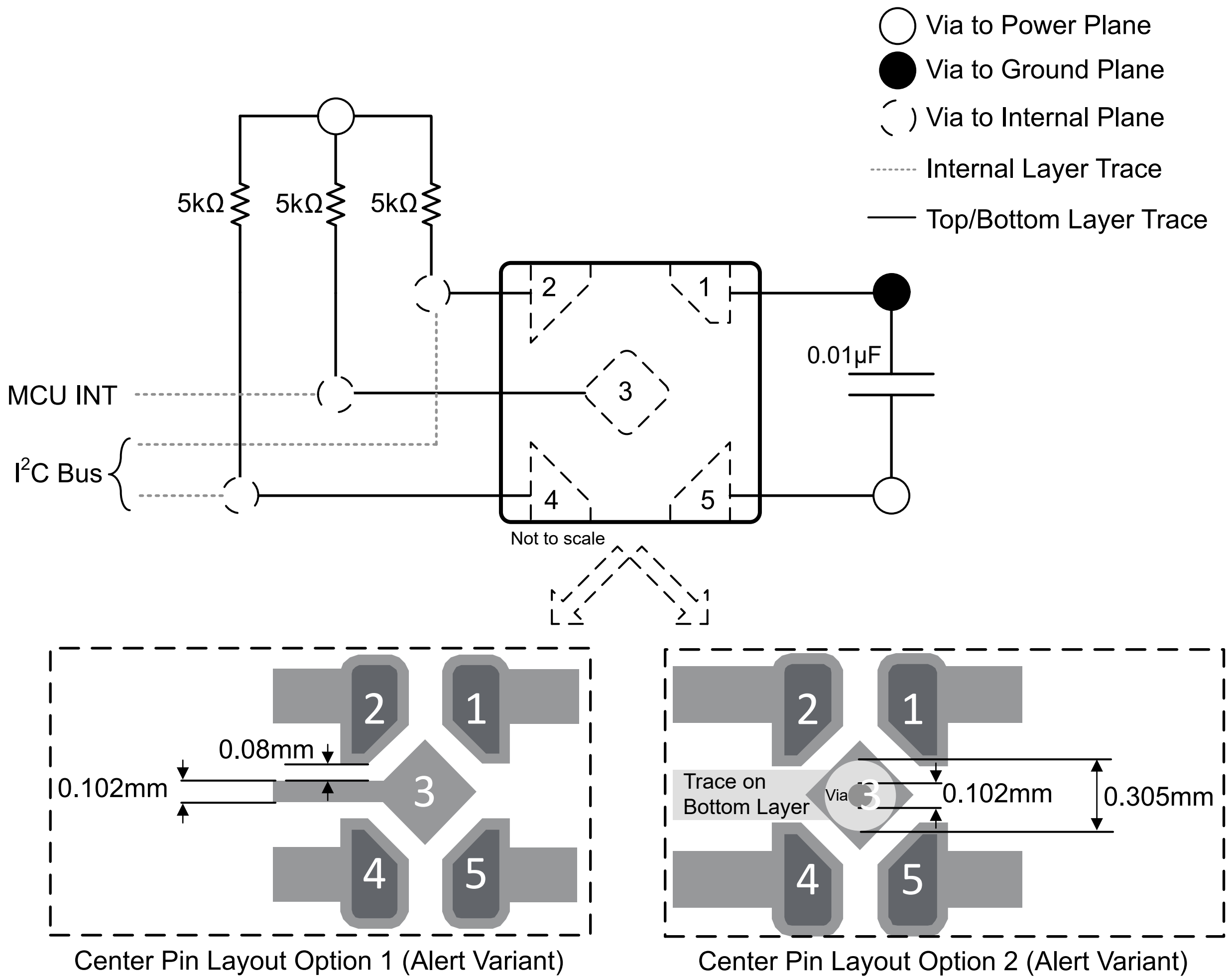

図 9-4. ALERT Pin Layout Example

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TMP102 Low-Power Digital Temperature Sensor With SMBus and Two-Wire Serial Interface in SOT563* , data sheet
- Texas Instruments, *TMP112x High-Accuracy, Low-Power, Digital Temperature Sensors With SMBus and TwoWire Serial Interface in SOT563* , data sheet
- Texas Instruments, *TMP1075 Temperature Sensor With I2C and SMBus Interface in Industry Standard LM75 Form Factor and Pinout* , data sheet
- Texas Instruments, *TMP LM 75 Comparison Common FAQs* , application note
- Texas Instruments, *TMP110 Evaluation Module* , EVM user's guide
- Texas Instruments, *Small-Size TMP110 Versus TI's Temperature Sensors* , product overview

10.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

10.3 サポート・リソース

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10.5 静電気放電に関する注意事項

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10.6 用語集

テキサス・インスツルメンツ用語集	この用語集には、用語や略語の一覧および定義が記載されています。

11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (February 2024) to Revision A (July 2024) **Page**

- ドキュメント全体にわたって表、図、相互参照の採番方法を更新.. 1

12 メカニカル、パッケージ、および注文情報

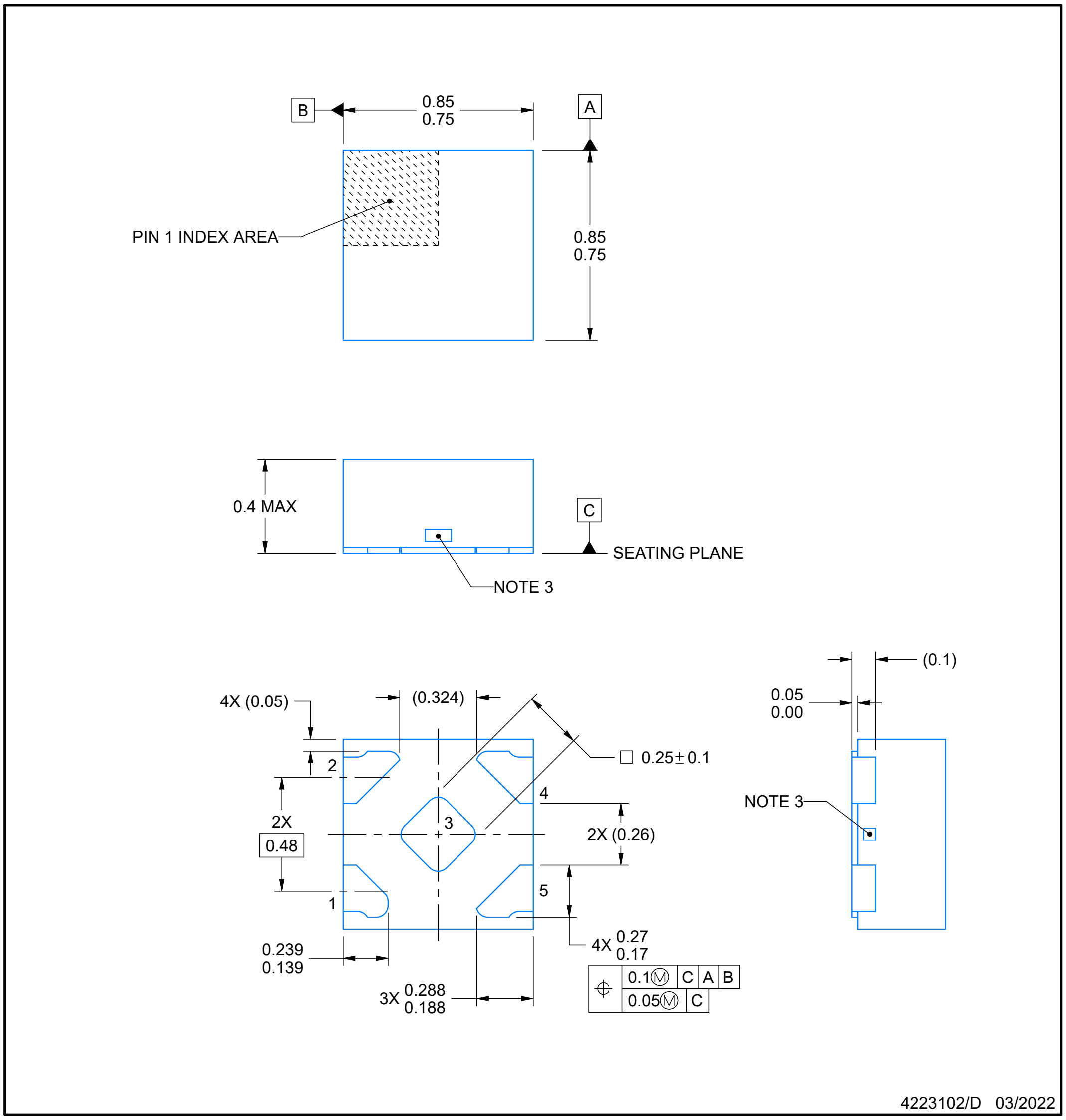
以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は指定のデバイスに使用できる最新のデータです。このデータは、予告なく、このドキュメントを改訂せずに変更される場合があります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGE OUTLINE

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.

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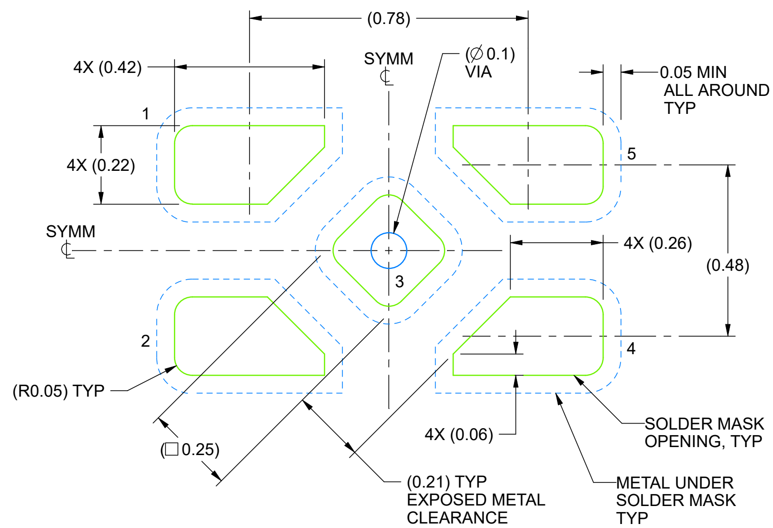
www.ti.com

EXAMPLE BOARD LAYOUT

DPW0005A **X2SON - 0.4 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4223102/D 03/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).

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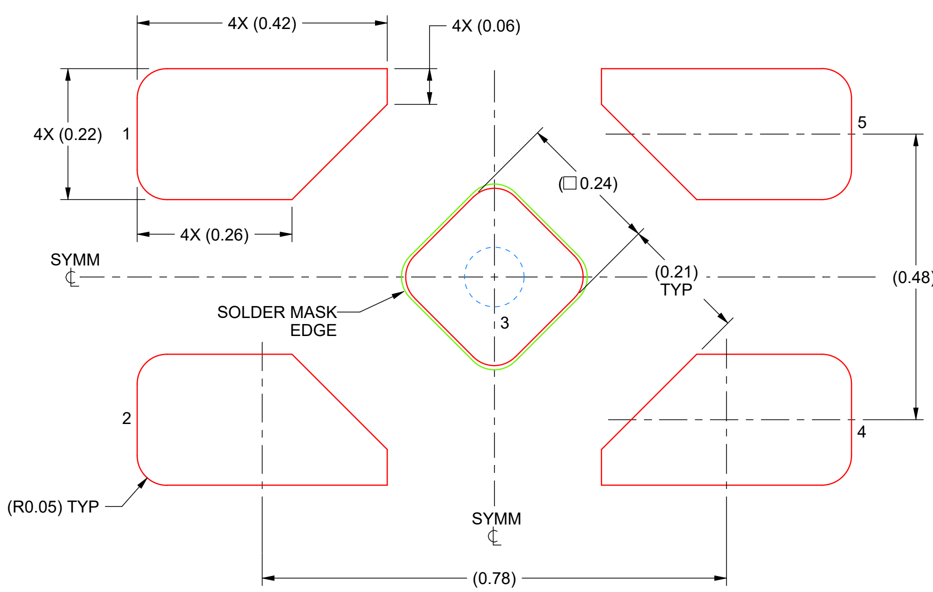
EXAMPLE STENCIL DESIGN

DPW0005A **X2SON - 0.4 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 3
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:100X

4223102/D 03/2022

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMP110D0IDPWR	Active	Production	X2SON (DPW) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Q
TMP110D0IDPWR.A	Active	Production	X2SON (DPW) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Q
TMP110D1IDPWR	Active	Production	X2SON (DPW) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	R
TMP110D1IDPWR.A	Active	Production	X2SON (DPW) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	R
TMP110D2IDPWR	Active	Production	X2SON (DPW) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	S
TMP110D2IDPWR.A	Active	Production	X2SON (DPW) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	S
TMP110D3IDPWR	Active	Production	X2SON (DPW) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T
TMP110D3IDPWR.A	Active	Production	X2SON (DPW) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T
TMP110DIDPWR	Active	Production	X2SON (DPW) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	A
TMP110DIDPWR.A	Active	Production	X2SON (DPW) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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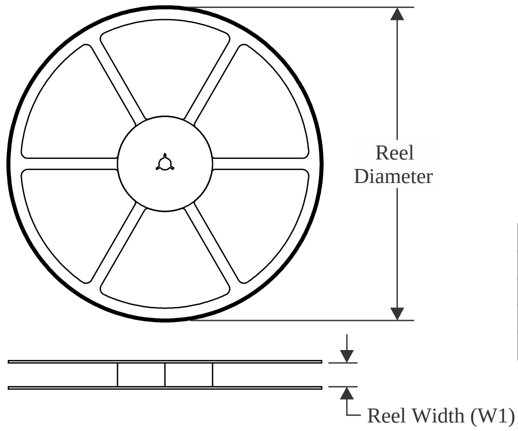
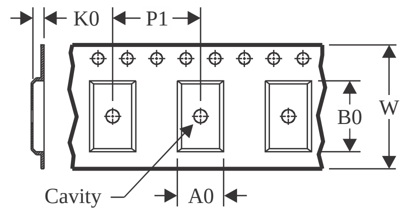
TAPE AND REEL INFORMATION

REEL DIMENSIONS

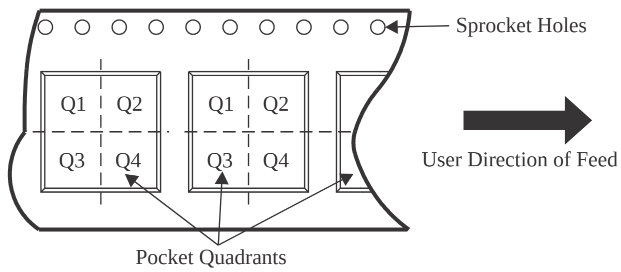


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

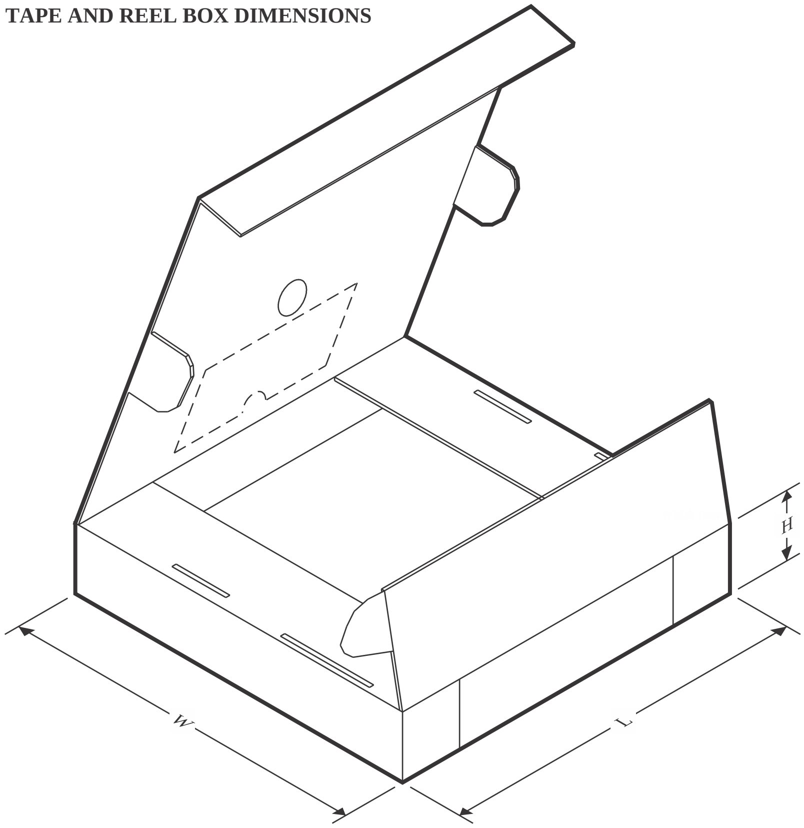
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP110D0IDPWR	X2SON	DPW	5	3000	180.0	8.4	0.91	0.91	0.5	2.0	8.0	Q2
TMP110D1IDPWR	X2SON	DPW	5	3000	180.0	8.4	0.91	0.91	0.5	2.0	8.0	Q2
TMP110D2IDPWR	X2SON	DPW	5	3000	180.0	8.4	0.91	0.91	0.5	2.0	8.0	Q2
TMP110D3IDPWR	X2SON	DPW	5	3000	180.0	8.4	0.91	0.91	0.5	2.0	8.0	Q2
TMP110DIDPWR	X2SON	DPW	5	3000	180.0	8.4	0.91	0.91	0.5	2.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

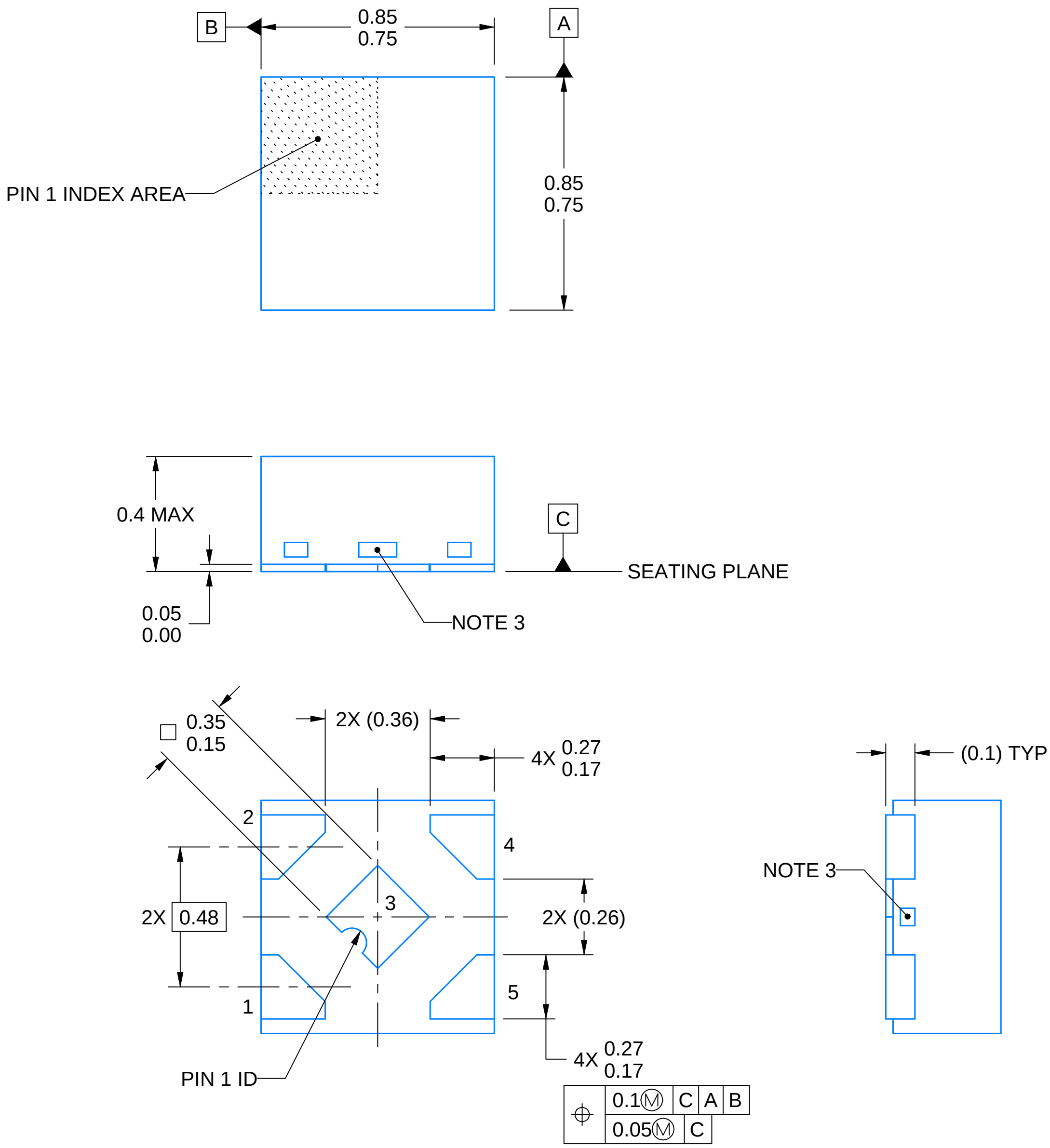
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP110D0IDPWR	X2SON	DPW	5	3000	210.0	185.0	35.0
TMP110D1IDPWR	X2SON	DPW	5	3000	210.0	185.0	35.0
TMP110D2IDPWR	X2SON	DPW	5	3000	210.0	185.0	35.0
TMP110D3IDPWR	X2SON	DPW	5	3000	210.0	185.0	35.0
TMP110DIDPWR	X2SON	DPW	5	3000	210.0	185.0	35.0

DPW 5

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

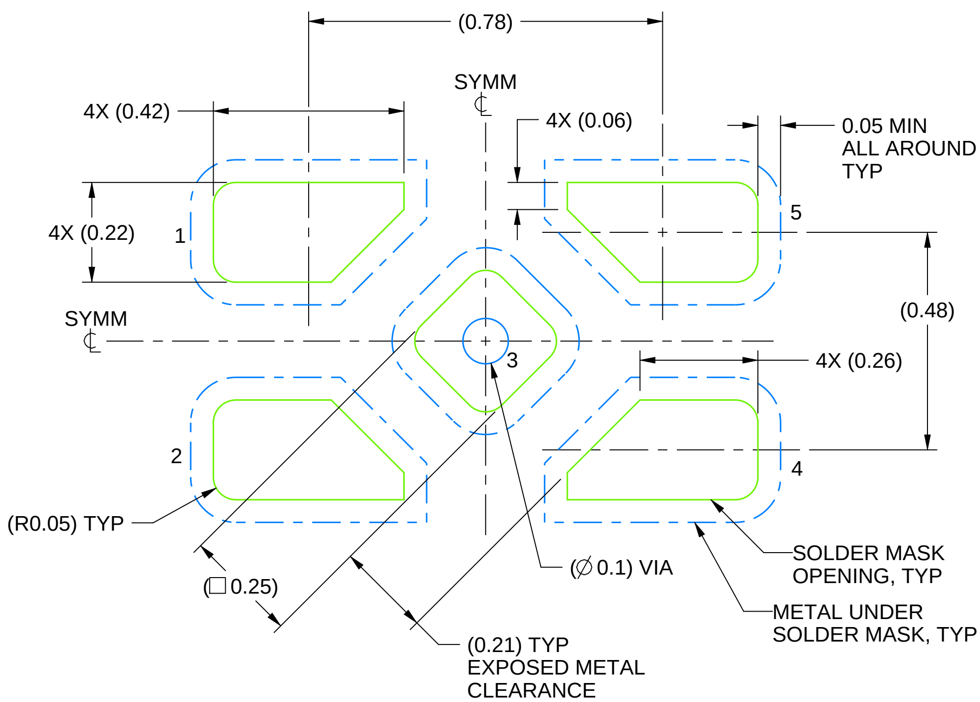
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4228233/D 09/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.

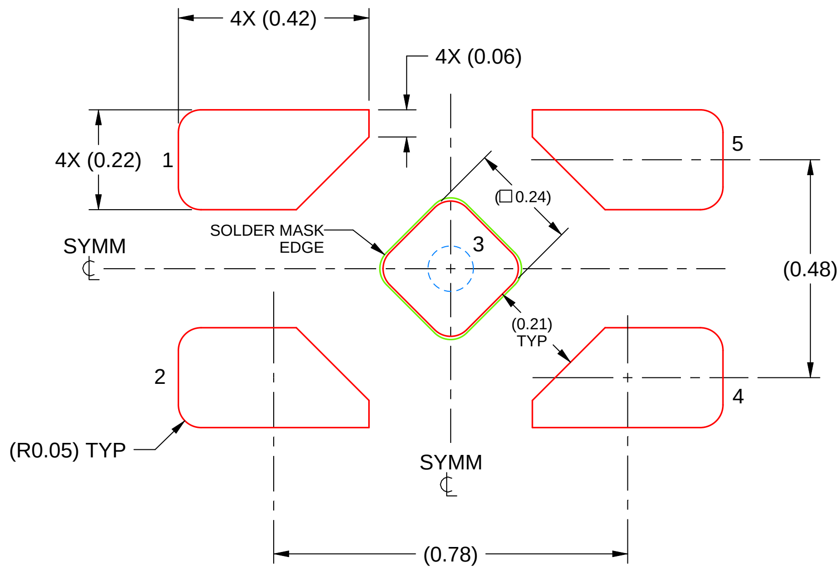


LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4228233/D 09/2023

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 5
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:60X

4228233/D 09/2023

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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