TMP100-Q1 および TMP101-Q1 温度センサ、I²C および SMBus インタフェース付き、アラート機能付き、SOT-23 パッケージ

1 特長

- 下記内容で AEC-Q100 認定済み
  - 温度グレード 1:-55°C～+125°C の動作温度範囲
  - HMB ESD コンポーネント分類レベル 2
  - CDM ESD コンポーネント分類レベル C5
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- デジタル出力:SMBus™、2 線式、I²C インターフェイス互換
- 分解能:9～12 ビット、ユーザー選択可能
- 精度:
  - -55°C～125°C で±1°C (標準値)
  - -55°C～125°C で ±2°C (最大値)
- 低い静止電流:45µA、0.1µA スタンバイ
- 広い電源電圧範囲:2.7V～5.5V
- TMP100-Q1:2 本のアドレス・ピン
- TMP101-Q1:1 本のアドレス・ピンと 1 本の ALERT ピン
- 6 ピンの SOT-23 パッケージ

2 アプリケーション

- 電源温度のモニタリング
- バッテリ管理
- サーモスタット制御
- 車載用:
  - ヘッド・ユニット
  - クラスタ
  - ボディ・エレクトロニクス
  - 照明

3 概要

TMP100-Q1 および TMP101-Q1 デバイスは、負の温度係数 (NTC) と正の温度係数 (PTC) のサーミスタの代替品に理想的なデジタル温度センサです。このデバイスは、校正および外部コンポーネントの信号調整を必要とすることなく、±1°C の標準的精度を提供します。デバイス温度センサは線形性が高く、複雑な計算やルックアップ・テーブルなしに温度を導き出すことができます。オンチップの 12 ビット ADC は最小 0.0625℃の分解能を実現できます。これらのデバイスは、6 ピンの SOT-23 パッケージで供給されます。

TMP100-Q1 および TMP101-Q1 デバイスは、SMBus、2 線式、I²C インターフェイス互換性を備えています。TMP100-Q1 デバイスの場合、1 つのバスに最大 8 つのデバイスを接続できます。TMP100-Q1 デバイスは、バスあたり最大 3 つのデバイスを接続できる SMBus アラート機能を備えています。

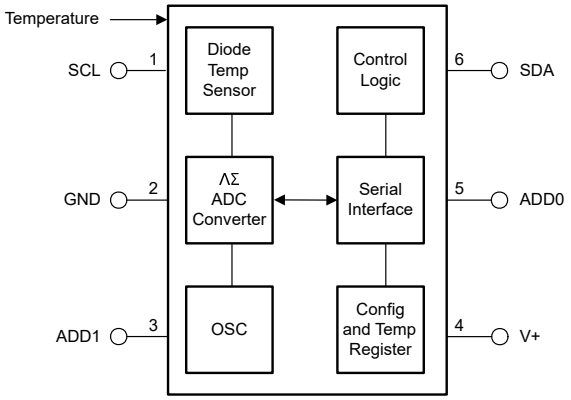
TMP100-Q1 および TMP101-Q1 デバイスは、通信、コンピュータ、コンシューマ、環境、工業、計測など、さまざまなアプリケーションの広範囲の温度測定向けに設計されています。

TMP100-Q1 および TMP101-Q1 デバイスは、-55°C～125°C の温度範囲で動作が規定されています。

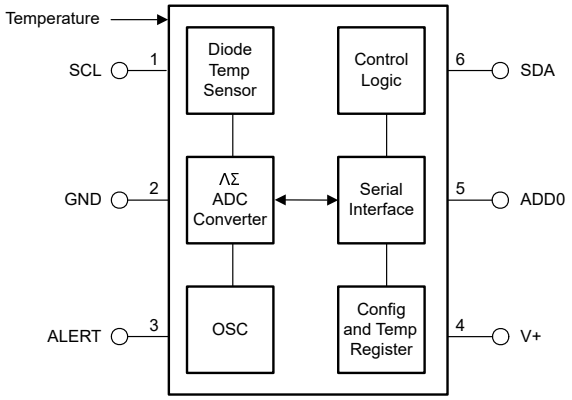
デバイス情報(1)

部品番号	パッケージ	本体サイズ (公称)
TMP100-Q1	SOT-23 (6)	2.90mm × 1.60mm
TMP101-Q1	SOT-23 (6)	2.90mm × 1.60mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



TMP100-Q1 のブロック図



TMP101-Q1 のブロック図

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- 「*特長*」セクションに機能安全の情報を追加 ... 1

Changes from Revision * (September 2011) to Revision A (May 2017) **Page**

- 「*製品情報*」表、「*ピン構成および機能*」セクション、「*取り扱い定格*」表、「*タイミング要件*」表、「*スイッチング特性*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加 ... 1

5 Pin Configuration and Functions

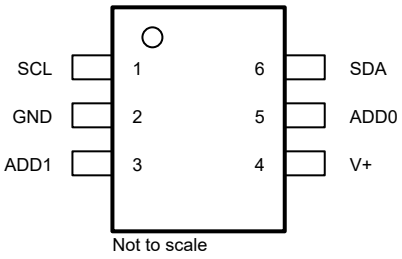

図 5-1. TMP100-Q1 DBV Package 6-Pin SOT-23 Top View

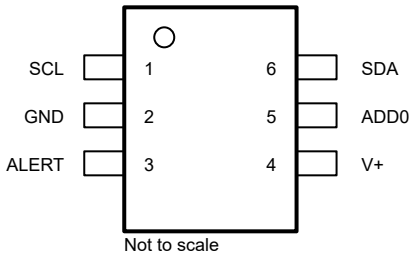

図 5-2. TMP101-Q1 DBV Package 6-Pin SOT-23 Top View

表 5-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO.			
	TMP100-Q1	TMP101-Q1		
ADD0	5	5	I	Address select. Connect to GND, V+, or leave floating.
ADD1	3	—	I	Address select. Connect to GND, V+, or leave floating.
ALERT	—	3	O	Overtemperature alert. Open-drain output; requires a pullup resistor.
GND	2	2	—	Ground
SCL	1	1	I	Serial clock. Open-drain output; requires a pullup resistor.
SDA	6	6	I/O	Serial data. Open-drain output; requires a pullup resistor.
V+	4	4	I	Supply voltage, 2.7 V to 5.5 V

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Power supply, V+		7.5	V
Input voltage(2)	–0.5	7.5	V
Operating temperature	–55	125	°C
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input voltage rating applies to all TMP100-Q1 and TMP101-Q1 input voltages.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage	2.7		5.5	V
Operating free-air temperature, T_A	–55		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TMP100-Q1, TMP101-Q1 DBV (SOT-23) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	182.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	115	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	30.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	17.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	29.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

At T_A = −55°C to 125°C and V+ = 2.7 V to 5.5 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE INPUT						
	Range		–55		125	°C
	Accuracy (temperature error)	−25°C to 85°C		±0.5	±2	°C
		−55°C to 125°C		±1	±2	
	Accuracy (temperature error) vs. supply			0.2	±0.5	°C/V
	Resolution	Selectable		0.0625		°C
DIGITAL INPUT/OUTPUT						
	Input capacitance			3		pF
V_{IH}	High-level input logic		0.7 (V+)		6	V
V_{IL}	Low-level input logic		−0.5		0.3 (V+)	V
I_{IN}	Input current	0 V ≤ V_{IN} ≤ 6 V			1	µA
V_{OL}	Low-level output logic SDA	I_{OL} = 3 mA	0	0.15	0.4	V
V_{OL}	Low-level output logic ALERT	I_{OL} = 4 mA	0	0.15	0.4	V
	Resolution	Selectable	9		12	Bits
	Conversion time	9 bits		40	75	ms
		10 bits		80	150	
		11 bits		160	300	
		12 bits		320	600	
	Conversion rate	9 bits		25		s/s
		10 bits		12		
		11 bits		6		
		12 bits		3		
POWER SUPPLY						
	Operating range		2.7		5.5	V
I_Q	Quiescent current	Serial bus inactive		45	75	µA
		Serial bus active, SCL frequency = 400 kHz		70		
		Serial bus active, SCL frequency = 3.4 MHz		150		
I_{SD}	Shutdown current	Serial bus inactive		0.1	13	µA
		Serial bus active, SCL frequency = 400 kHz		20		
		Serial bus active, SCL frequency = 3.4 MHz		100		
TEMPERATURE RANGE						
	Specified range		–55		125	°C
	Storage range		–60		150	°C

6.6 Timing Requirements

PARAMETER		FAST MODE		HIGH-SPEED MODE		UNIT
		MIN	MAX	MIN	MAX	
$f_{(SCL)}$	SCL operating frequency		0.4		2	MHz
$t_{(BUF)}$	Bus free time between STOP and START condition	1300		160		ns
$t_{(HDSTA)}$	Hold time after repeated START condition. After this period, the first clock is generated.	600		160		ns
$t_{(SUSTA)}$	Repeated START condition setup time	600		160		ns
$t_{(SUSTO)}$	STOP condition setup time	600		160		ns
$t_{(HDDAT)}$	Data hold time	20	900	20	170	ns
$t_{(SUDAT)}$	Data setup time	100		20		ns
$t_{(LOW)}$	SCL clock LOW period	1300		360		ns
$t_{(HIGH)}$	SCL clock HIGH period	600		60		ns
t_{RC}, t_{FC}	Clock rise and fall time		300		40	ns
t_{RD}, t_{FD}	Data rise and fall time		300		170	ns

6.7 Typical Characteristics

At T_A = 25°C and V+ = 5 V, unless otherwise noted.

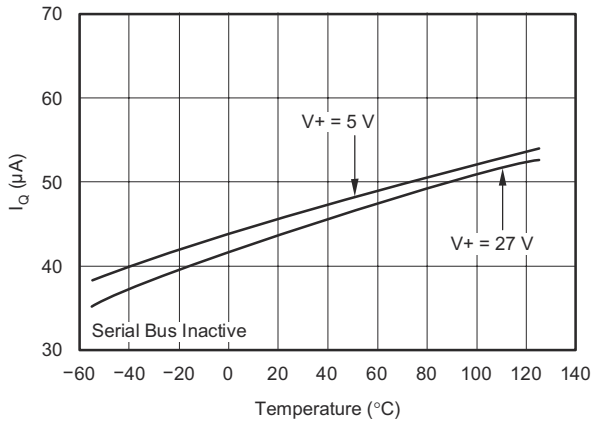

図 6-1. Quiescent Current vs. Temperature

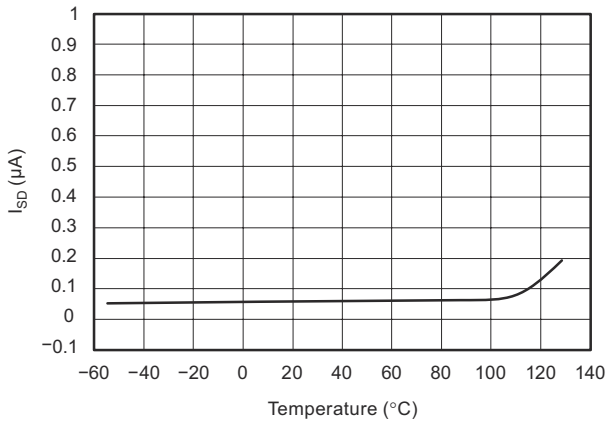

図 6-2. Shutdown Current vs. Temperature

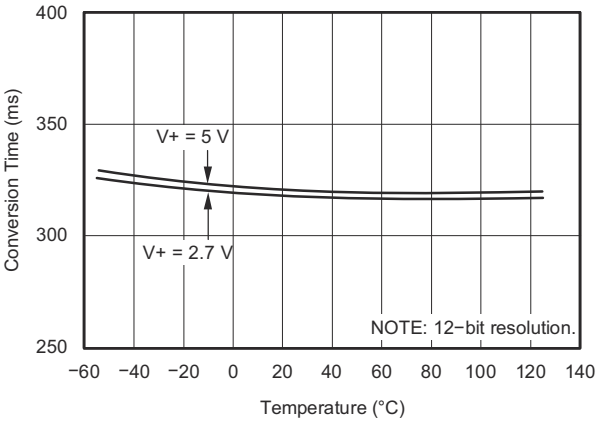

図 6-3. Conversion Time vs. Temperature

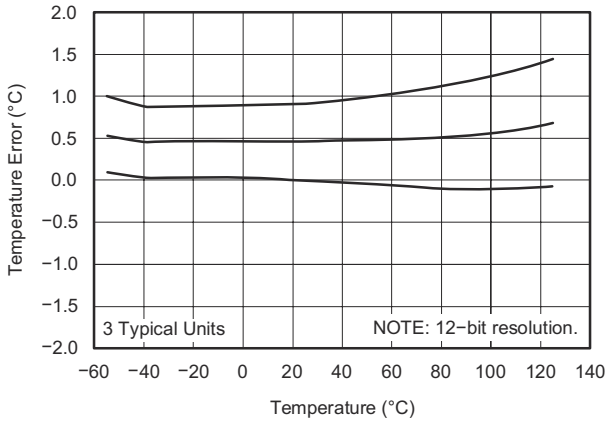

図 6-4. Temperature Accuracy vs. Temperature

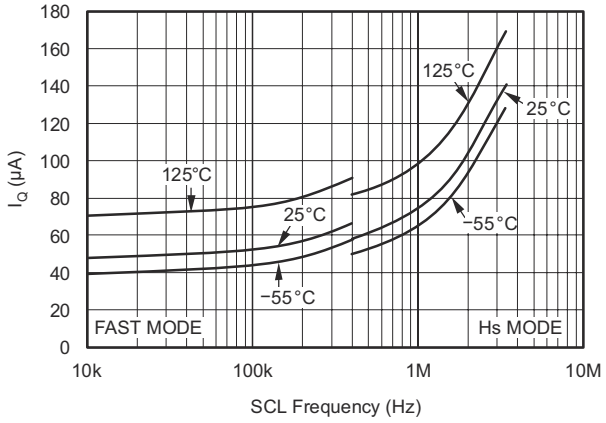

図 6-5. Quiescent Current With Bus Activity vs. Temperature

7 Detailed Description

7.1 Overview

The TMP100-Q1 and TMP101-Q1 devices are digital temperature sensors optimal for thermal management and thermal protection applications. The TMP100-Q1 and TMP101-Q1 devices are Two-Wire, SMBus, and I^2C interface-compatible. These devices are specified over a operating temperature range of −55°C to 125°C. The *Functional Block Diagram* section shows the internal block diagrams of the TMP100-Q1 and TMP101-Q1 devices.

The temperature sensor in the TMP100-Q1 and TMP101-Q1 devices is the chip itself. Thermal paths run through the package leads as well as the plastic package. The package leads provide the primary thermal path because of the lower thermal resistance of the metal. The GND pin of the TMP100-Q1 or TMP101-Q1 is directly connected to the metal lead frame, and is the best choice for thermal input.

7.2 Functional Block Diagram

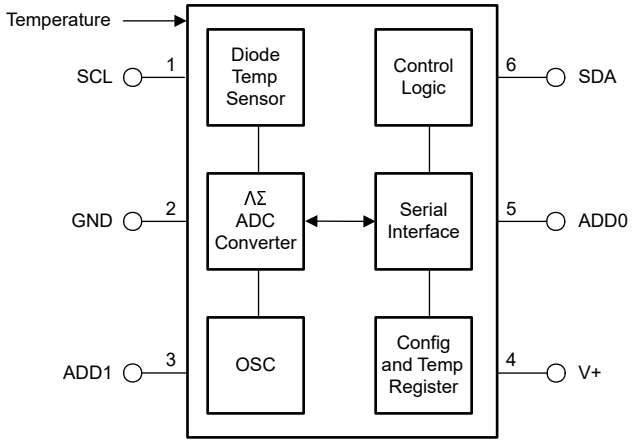

図 7-1. TMP100-Q1 Block Diagram

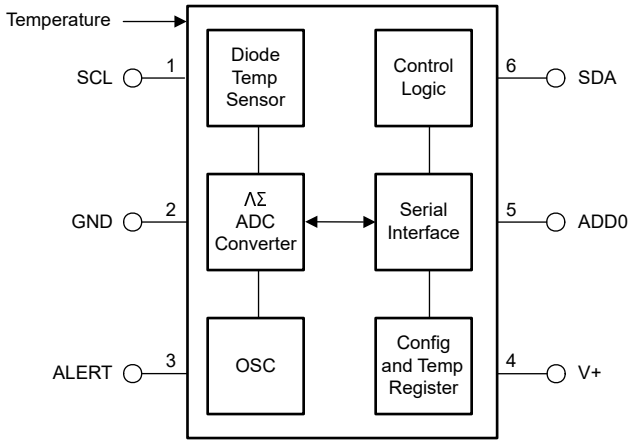

図 7-2. TMP101-Q1 Block Diagram

7.3 Feature Description

7.3.1 Digital Temperature Output

The digital output from each temperature measurement conversion is stored in the read-only Temperature Register. The Temperature Register of the TMP100-Q1 or TMP101-Q1 device is a 12-bit, read-only register that stores the output of the most recent conversion. Two bytes must be read to obtain data and are listed in 表 7-6 and 表 7-7. The first 12 bits are used to indicate temperature with all the remaining bits equal to zero. The data format for temperature is listed in 表 7-1. Negative numbers are represented in binary twos complement format. Following power-up or reset, the temperature register reads 0°C until the first conversion is complete.

The user can obtain 9, 10, 11, or 12 bits of resolution by addressing the Configuration Register and setting the resolution bits accordingly. For 9-, 10-, or 11-bit resolution, the most significant bits (MSBs) in the Temperature Register are used with the unused least significant bits (LSBs) set to zero.

表 7-1. Temperature Data Format

TEMPERATURE (°C)	DIGITAL OUTPUT	
	BINARY	HEX
128	0111 1111 1111	7FF
127.9375	0111 1111 1111	7FF
100	0110 0100 0000	640
80	0101 0000 0000	500
75	0100 1011 0000	4B0
50	0011 0010 0000	320
25	0001 1001 0000	190
0.25	0000 0000 0100	004
0	0000 0000 0000	000
–0.25	1111 1111 1100	FFC
–25	1110 0111 0000	E70
–55	1100 1001 0000	C90
–128	1000 0000 0000	800

7.3.2 Serial Interface

The TMP100-Q1 and TMP101-Q1 devices operate only as target devices on the SMBus, Two-Wire, and I^2C interface-compatible bus. Connections to the bus are made through the open-drain I/O lines SDA and SCL. The TMP100-Q1 and TMP101-Q1 devices support the transmission protocol for fast (up to 400 kHz) and high-speed (up to 2 MHz) modes. All data bytes are transmitted MSB first.

7.3.3 Bus Overview

The device that initiates the transfer is called a *controller*, and the devices controlled by the controller are *targets*. The bus must be controlled by a controller device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions.

To address a specific device, a START condition is initiated, indicated by pulling the data line (SDA) from a HIGH to LOW logic level while SCL is HIGH. All targets on the bus shift in the target address byte, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the target being addressed responds to the controller by generating an Acknowledge and pulling SDA LOW.

Data transfer is then initiated and sent over eight clock pulses followed by an Acknowledge Bit. During data transfer, SDA must remain stable while SCL is HIGH because any change in SDA while SCL is HIGH is interpreted as a control signal.

When all data are transferred, the controller generates a STOP condition indicated by pulling SDA from LOW to HIGH, while SCL is HIGH.

7.3.4 Serial Bus Address

To program the TMP100-Q1 and TMP101-Q1 devices, the controller must first address target devices through a target address byte. The target address byte consists of seven address bits and a direction bit indicating the intent of executing a read or write operation.

The TMP100-Q1 device features two address pins to allow up to eight devices to be addressed on a single I^2C interface. 表 7-2 describes the pin logic levels used to properly connect up to eight devices. *Float* indicates the pin is left unconnected. The state of pins ADD0 and ADD1 is sampled on the first I^2C bus communication and must be set before any activity on the interface.

表 7-2. Address Pins and Target Addresses for the TMP100-Q1

ADD1	ADD0	TARGET ADDRESS
0	0	1001000
0	Float	1001001
0	1	1001010
1	0	1001100
1	Float	1001101
1	1	1001110
Float	0	1001011
Float	1	1001111

The TMP101-Q1 device features one address pin and an ALERT pin, allowing up to three devices to be connected per bus. Pin logic levels are described in 表 7-3. The address pins of the TMP100-Q1 and TMP101-Q1 devices are read after reset or in response to an I^2C address acquire request. Following reading, the state of the address pins is latched to minimize power dissipation associated with detection.

表 7-3. Address Pins and Target Addresses for the TMP101-Q1

ADD0	TARGET ADDRESS
0	1001000
Float	1001001
1	1001010

7.3.5 Writing and Reading to the TMP100-Q1 and TMP101-Q1

Accessing a particular register on the TMP100-Q1 and TMP101-Q1 devices is accomplished by writing the appropriate value to the Pointer Register. The value for the Pointer Register is the first byte transferred after the I^2C target address byte with the R/ $\overline{W}$ bit LOW. Every write operation to the TMP100-Q1 and TMP101-Q1 devices requires a value for the Pointer Register (see 図 7-4).

When reading from the TMP100-Q1 and TMP101-Q1 devices, the last value stored in the Pointer Register by a write operation is used to determine which register is read by a read operation. To change the register pointer for a read operation, a new value must be written to the Pointer Register. This action is accomplished by issuing an I^2C target address byte with the R/ $\overline{W}$ bit LOW, followed by the Pointer Register Byte. No additional data are required. The controller can then generate a START condition and send the I^2C target address byte with the R/ $\overline{W}$ bit HIGH to initiate the read command; see 図 7-5 for details of this sequence. If repeated reads from the same register are desired, the Pointer Register bytes do not have to be continually sent because the TMP100-Q1 and TMP101-Q1 devices remember the Pointer Register value until that value is changed by the next write operation.

7.3.6 Target Mode Operations

The TMP100-Q1 and TMP101-Q1 devices can operate as a target receiver or target transmitter.

7.3.6.1 Target Receiver Mode

The first byte transmitted by the controller is the target address, with the R/ $\overline{W}$ bit LOW. The TMP100-Q1 or TMP101-Q1 devices then acknowledges reception of a valid address. The next byte transmitted by the controller is the Pointer Register. The TMP100-Q1 or TMP101-Q1 devices then acknowledges reception of the Pointer Register byte. The next byte or bytes are written to the register addressed by the Pointer Register. The TMP100-Q1 and TMP101-Q1 devices acknowledge reception of each data byte. The controller can terminate data transfer by generating a START or STOP condition.

7.3.6.2 Target Transmitter Mode

The first byte is transmitted by the controller and is the target address, with the R/ $\overline{W}$ bit HIGH. The target acknowledges reception of a valid target address. The next byte is transmitted by the target and is the most significant byte of the register indicated by the Pointer Register. The controller acknowledges reception of the data byte. The next byte transmitted by the target is the least significant byte. The controller acknowledges reception of the data byte. The controller can terminate data transfer by generating a Not-Acknowledge on reception of any data byte, or generating a START or STOP condition.

7.3.7 SMBus Alert Function

The TMP101-Q1 device supports the SMBus Alert function. When the TMP101-Q1 device is operating in Interrupt Mode (TM = 1), the ALERT pin of the TMP101-Q1 device can be connected as an SMBus Alert signal. When a controller senses that an ALERT condition is present on the ALERT line, the controller sends an SMBus Alert command (00011001) on the bus. If the ALERT pin of the TMP101-Q1 device is active, the TMP101-Q1 device acknowledges the SMBus Alert command and responds by returning its target address on the SDA line. The eighth bit (LSB) of the target address byte indicates if the temperature exceeding T_{HIGH} or falling below T_{LOW} caused the ALERT condition. For POL = 0, this bit is LOW if the temperature is greater than or equal to THIGH. This bit is HIGH if the temperature is less than TLOW. The polarity of this bit is inverted if POL = 1; see 図 7-6 for details of this sequence.

If multiple devices on the bus respond to the SMBus Alert command, arbitration during the target address portion of the SMBus alert command determine which device clears its ALERT status. If the TMP101-Q1 device wins the arbitration, its ALERT pin becomes inactive at the completion of the SMBus Alert command. If the TMP101-Q1 loses the arbitration, its ALERT pin remains active.

The TMP100-Q1 device also responds to the SMBus ALERT command if its TM bit is set to 1. Because the device does not have an ALERT pin, the device must periodically poll the device by issuing an SMBus Alert command. If the TMP100-Q1 device generates an ALERT, the device acknowledges the SMBus Alert command and returns its target address in the next byte.

7.3.8 General Call

The TMP100-Q1 and TMP101-Q1 devices respond to the I^2C General Call address (0000000) if the eighth bit is 0. The device acknowledges the General Call address and responds to commands in the second byte. If the second byte is 00000100, the TMP100-Q1 and TMP101-Q1 devices latch the status of their address pins, but do not reset. If the second byte is 00000110, the TMP100-Q1 and TMP101-Q1 devices latch the status of their address pins and reset their internal registers.

7.3.9 High-Speed Mode

In order for the I^2C bus to operate at frequencies above 400 kHz, the controller device must issue an Hs-mode controller code (00001XXX) as the first byte after a START condition to switch the bus to high-speed operation. The TMP100-Q1 and TMP101-Q1 devices do not acknowledge this byte as required by the I^2C specification, but do switch their input filters on SDA and SCL and their output filters on SDA to operate in Hs-mode, allowing transfers at up to 2 MHz. After the Hs-mode controller code is issued, the controller transmits an I^2C target address to initiate a data transfer operation. The bus continues to operate in Hs-mode until a STOP condition

occurs on the bus. Upon receiving the STOP condition, the TMP100-Q1 and TMP101-Q1 devices switch the input and output filter back to fast-mode operation.

7.3.10 POR (Power-On Reset)

The TMP100-Q1 and TMP101-Q1 devices both have on-chip, power-on reset circuits that reset the device to default settings when the device is powered on. This circuit activates when the power supply is less than 0.3 V for more than 100 ms. If the TMP100-Q1 and TMP101-Q1 devices are powered down by removing supply voltage from the device, but the supply voltage is not assured to be less than 0.3 V, TI recommends issuing a General Call reset command on the I^2C interface bus to ensure that the TMP100-Q1 and TMP101-Q1 devices are completely reset.

7.3.11 Timing Diagrams

The TMP100-Q1 and TMP101-Q1 devices are Two-Wire, SMBUs, and I^2C interface-compatible. 図 7-3 to 図 7-6 describe the various operations on the TMP100-Q1 and TMP101-Q1. The following list provides bus definitions. Parameters for 図 7-3 are defined in the *Timing Requirements* table.

Bus Idle: Both SDA and SCL lines remain HIGH.

Start Data Transfer: A change in the state of the SDA line, from HIGH to LOW, while the SCL line is HIGH, defines a START condition. Each data transfer is initiated with a START condition.

Stop Data Transfer: A change in the state of the SDA line from LOW to HIGH while the SCL line is HIGH defines a STOP condition. Each data transfer is terminated with a repeated START or STOP condition.

Data Transfer: The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the controller device. The receiver acknowledges the transfer of data.

Acknowledge: Each receiving device, when addressed, is obliged to generate an Acknowledge bit. A device that acknowledges must pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the Acknowledge clock pulse. Setup and hold times must be taken into account. On a controller receive, the termination of the data transfer can be signaled by the controller generating a Not-Acknowledge on the last byte that is transmitted by the target.

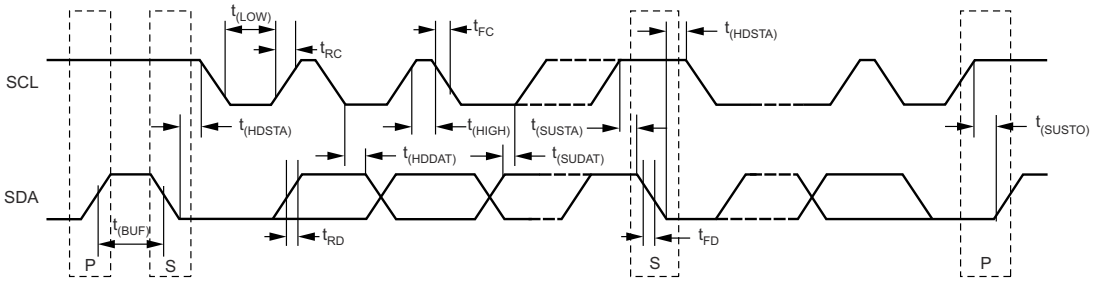

図 7-3. I^2C Timing Diagram

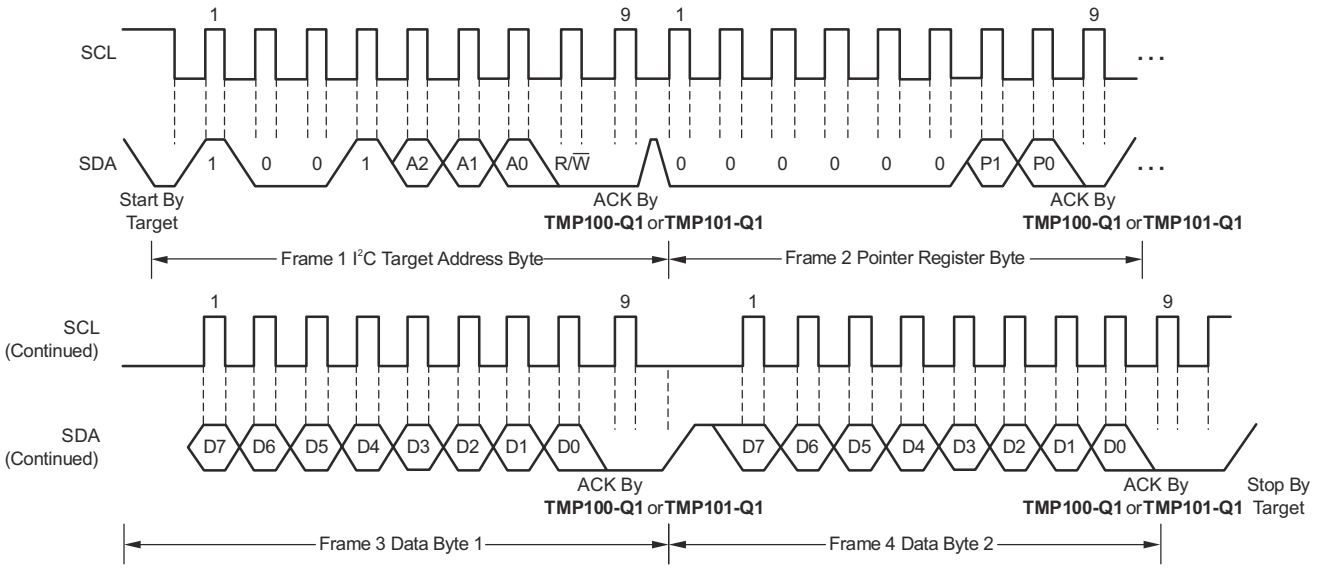

図 7-4. I²C Timing Diagram for Write Word Format

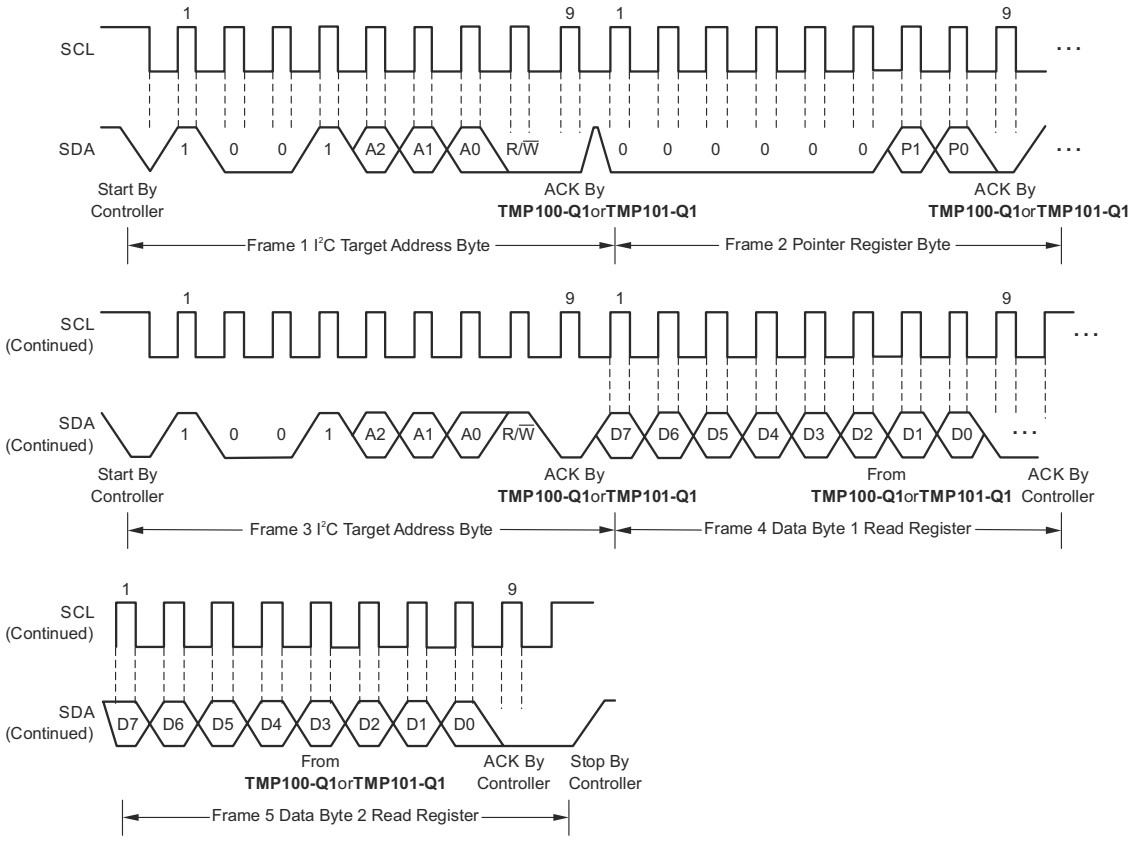

図 7-5. I²C Timing Diagram for Read Word Format

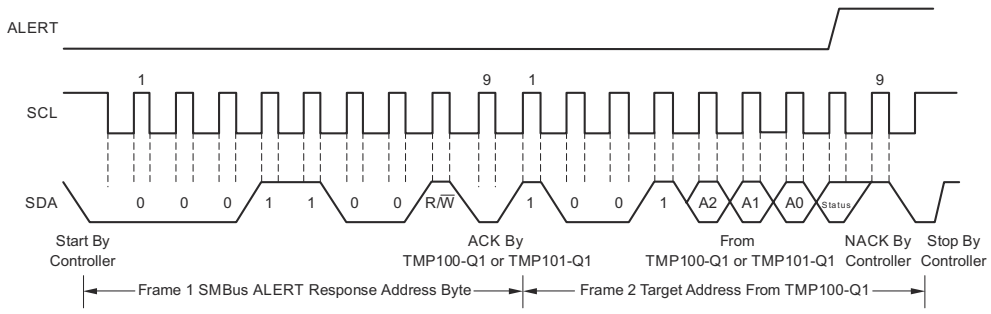

図 7-6. Timing Diagram for SMBus ALERT

7.4 Device Functional Modes

7.4.1 Shutdown Mode (SD)

The Shutdown Mode of the TMP100-Q1 and TMP101-Q1 devices lets the user save maximum power by shutting down all device circuitry other than the serial interface, which reduces current consumption to less than 1 µA. For the TMP100-Q1 and TMP101-Q1 devices, Shutdown Mode is enabled when the SD bit is 1. The device shuts down when the current conversion is completed. For SD equal to 0, the device maintains continuous conversion.

7.4.2 OS/ALERT (OS)

The TMP100-Q1 and TMP101-Q1 devices feature a One-Shot Temperature Measurement Mode. When the device is in Shutdown Mode, writing 1 to the OS/ALERT bit starts a single temperature conversion. The device returns to the shutdown state at the completion of the single conversion. This feature is useful to reduce power consumption in the TMP100-Q1 and TMP101-Q1 devices when continuous monitoring of temperature is not required.

Reading the OS/ALERT bit provides information about the Comparator Mode status. The state of the POL bit inverts the polarity of data returned from the OS/ALERT bit. For POL = 0, the OS/ALERT reads as 1 until the temperature equals or exceeds T_{HIGH} for the programmed number of consecutive faults, causing the OS/ALERT bit to read as 0. The OS/ALERT bit continues to read as 0 until the temperature falls below T_{LOW} for the programmed number of consecutive faults when the OS/ALERT bit again reads as 1. The status of the TM bit does not affect the status of the OS/ALERT bit.

7.4.3 Thermostat Mode (TM)

The Thermostat Mode bit of the TMP101-Q1 device indicates to the device whether to operate in Comparator Mode (TM = 0) or Interrupt Mode (TM = 1). For more information on comparator and interrupt modes, see the *High- and Low-Limit Registers* section.

7.4.4 Comparator Mode (TM = 0)

In Comparator Mode (TM = 0), the ALERT pin is activated when the temperature equals or exceeds the value in the T_{HIGH} register and remains active until the temperature falls below the value in the T_{LOW} register. For more information on the Comparator Mode, see the *High- and Low-Limit Registers* section.

7.4.5 Interrupt Mode (TM = 1)

In Interrupt Mode (TM = 1), the ALERT pin is activated when the temperature exceeds T_{HIGH} or goes below the T_{LOW} registers. The ALERT pin is cleared when the host controller reads the temperature register. For more information on the interrupt mode, see the *High- and Low-Limit Registers* section.

7.5 Programming

7.5.1 Pointer Register

図 7-7 shows the internal register structure of the TMP100-Q1 and TMP101-Q1 devices. The 8-bit Pointer Register of the TMP100-Q1 and TMP101-Q1 devices is used to address a given data register. The Pointer Register uses the two LSBs to identify which of the data registers respond to a read or write command. 表 7-4

identifies the bits of the Pointer Register byte. 表 7-5 describes the pointer address of the registers available in the TMP100-Q1 and TMP101-Q1 devices. The power-up reset value of P1 and P0 is 00.

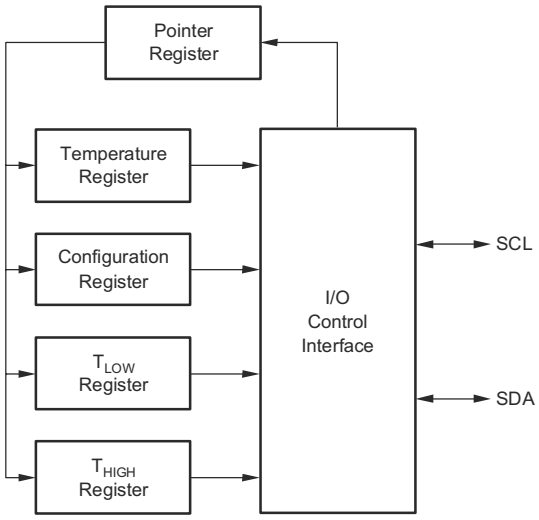

図 7-7. Internal Register Structure of the TMP100-Q1 and TMP101-Q1

7.5.1.1 Pointer Register Byte (pointer = N/A) [reset = 00h]

表 7-4. Pointer Register Byte

P7	P6	P5	P4	P3	P2	P1	P0
0	0	0	0	0	0	Register Bits	

7.5.1.2 Pointer Addresses of the TMP100-Q1 and TMP101-Q1 Registers

表 7-5. Pointer Addresses of the TMP100-Q1 and TMP101-Q1 Registers

P1	P0	TYPE	REGISTER
0	0	R only, default	Temperature Register
0	1	R/W	Configuration Register
1	0	R/W	T_{LOW} Register
1	1	R/W	T_{HIGH} Register

7.5.2 Temperature Register

The Temperature Register of the TMP100-Q1 or TMP101-Q1 devices is a 12-bit, read-only register that stores the output of the most recent conversion. Two bytes must be read to obtain data, and are described in 表 7-6 and 表 7-7. The first 12 bits are used to indicate temperature, with all remaining bits equal to zero. Data format for temperature is summarized in 表 7-1. Following power-up or reset, the Temperature Register reads 0°C until the first conversion is complete.

表 7-6. Byte 1 of the Temperature Register

D7	D6	D5	D4	D3	D2	D1	D0
T11	T10	T9	T8	T7	T6	T5	T4

表 7-7. Byte 2 of the Temperature Register

D7	D6	D5	D4	D3	D2	D1	D0
T3	T2	T1	T0	0	0	0	0

7.5.3 Configuration Register

The Configuration Register is an 8-bit read and write register used to store bits that control the operational modes of the temperature sensor. Read and write operations are performed MSB-first. The format of the Configuration Register for the TMP100-Q1 and TMP101-Q1 devices is shown in 表 7-8, followed by a breakdown of the register bits. The power-up or reset value of the Configuration Register is all bits equal to 0. The OS/ALERT bit reads as 1 after power-up or reset value.

表 7-8. Configuration Register Format

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	OS/ALERT	R1	R0	F1	F0	POL	TM	SD

7.5.3.1 Shutdown Mode (SD)

The Shutdown Mode of the TMP100-Q1 and TMP101-Q1 devices allows the user to save maximum power by shutting down all device circuitry other than the serial interface, which reduces current consumption to less than 1 µA. For the TMP100-Q1 and TMP101-Q1 devices, Shutdown Mode is enabled when the SD bit is 1. The device shuts down when the current conversion is completed. For SD equal to 0, the device maintains continuous conversion.

7.5.3.2 Thermostat Mode (TM)

The Thermostat Mode bit of the TMP101-Q1 device indicates to the device whether to operate in Comparator Mode (TM = 0) or Interrupt Mode (TM = 1). For more information on comparator and interrupt modes, see *High- and Low-Limit Registers*.

7.5.3.3 Polarity (POL)

The Polarity bit of the TMP101-Q1 device lets the user adjust the polarity of the ALERT pin output. If the POL bit is set to 0 (default), the ALERT pin becomes active low. When the POL bit is set to 1, the ALERT pin becomes active high and the state of the ALERT pin is inverted. The operation of the ALERT pin in various modes is illustrated in 図 7-8.

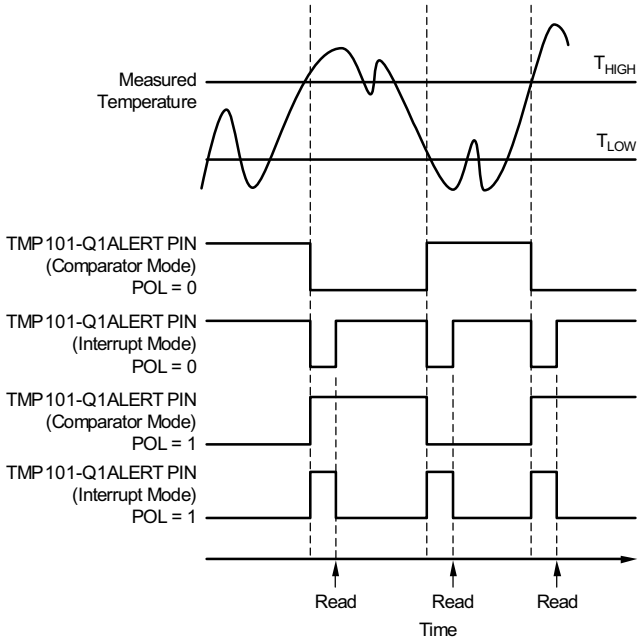

図 7-8. Output Transfer Function Diagrams

7.5.3.4 Fault Queue (F1, F0)

A fault condition occurs when the measured temperature exceeds the user-defined limits set in the T_{HIGH} and T_{LOW} Registers. Additionally, the number of fault conditions required to generate an alert can be programmed using the Fault Queue. The Fault Queue is provided to prevent a false alert resulting from environmental noise. The Fault Queue requires consecutive fault measurements in order to trigger the alert function. If the temperature falls below T_{LOW} before reaching the number of programmed consecutive faults limit, the count is reset to 0. 表 7-9 defines the number of measured faults that can be programmed to trigger an alert condition in the device.

表 7-9. Fault Settings of the TMP100-Q1 and TMP101-Q1

F1	F0	CONSECUTIVE FAULTS
0	0	1
0	1	2
1	0	4
1	1	6

7.5.3.5 Converter Resolution (R1, R0)

The Converter Resolution bits control the resolution of the internal analog-to-digital converter (ADC), thus allowing the user to maximize efficiency by programming for higher resolution or faster conversion time. 表 7-10 identifies the Resolution bits and the relationship between resolution and conversion time.

表 7-10. Resolution of the TMP100-Q1 and TMP101-Q1

R1	R0	RESOLUTION	CONVERSION TIME (Typical)
0	0	9 bits (0.5°C)	40 ms
0	1	10 bits (0.25°C)	80 ms
1	0	11 bits (0.125°C)	160 ms
1	1	12 bits (0.0625°C)	320 ms

7.5.3.6 OS/ALERT (OS)

The TMP100-Q1 and TMP101-Q1 devices feature a One-Shot Temperature Measurement Mode. When the device is in Shutdown Mode, writing 1 to the OS/ALERT bit starts a single temperature conversion. The device returns to the shutdown state at the completion of the single conversion. This feature is useful to reduce power consumption in the TMP100-Q1 and TMP101-Q1 when continuous temperature monitoring is not required.

Reading the OS/ALERT bit provides information about the Comparator Mode status. The state of the POL bit inverts the polarity of data returned from the OS/ALERT bit. For POL = 0, the OS/ALERT reads as 1 until the temperature equals or exceeds T_{HIGH} for the programmed number of consecutive faults, causing the OS/ALERT bit to read as 0. The OS/ALERT bit continues to read as 0 until the temperature falls below T_{LOW} for the programmed number of consecutive faults when the OS/ALERT bit again reads as 1. The status of the TM bit does not affect the status of the OS/ALERT bit.

7.5.4 High- and Low-Limit Registers

In Comparator Mode (TM = 0), the ALERT pin of the TMP101-Q1 becomes active when the temperature equals or exceeds the value in T_{HIGH} and generates a consecutive number of faults according to fault bits F1 and F0. The ALERT pin remains active until the temperature falls below the indicated T_{LOW} value for the same number of faults.

In Interrupt Mode (TM = 1) the ALERT pin becomes active when the temperature equals or exceeds T_{HIGH} for a consecutive number of fault conditions. The ALERT pin remains active until a read operation of any register occurs or the device successfully responds to the SMBus Alert Response Address. The ALERT pin is also cleared if the device is placed in Shutdown Mode. When the ALERT pin is cleared, it only becomes active again by the temperature falling below TLOW. When the temperature falls below T_{LOW}, the ALERT pin becomes active and remains active until cleared by a read operation of any register or a successful response to the SMBus Alert Response Address. When the ALERT pin is cleared, the above cycle repeats with the ALERT pin becoming active when the temperature equals or exceeds T_{HIGH}. The ALERT pin can also be cleared by resetting the device with the General Call Reset command. This action also clears the state of the internal registers in the device, returning the device to Comparator Mode (TM = 0).

Both operational modes are represented in 図 7-8. 表 7-11, 表 7-12, 表 7-13, and 表 7-14 describe the format for the T_{HIGH} and T_{LOW} registers. Power-up reset values for T_{HIGH} and T_{LOW} are: T_{HIGH} = 80°C and T_{LOW} = 75°C. The format of the data for T_{HIGH} and T_{LOW} is the same as for the Temperature Register.

表 7-11. Byte 1 of the T_{HIGH} Register

D7	D6	D5	D4	D3	D2	D1	D0
H11	H10	H9	H8	H7	H6	H5	H4

表 7-12. Byte 2 of the T_{HIGH} Register

D7	D6	D5	D4	D3	D2	D1	D0
H3	H2	H1	H0	0	0	0	0

表 7-13. Byte 1 of the T_{LOW} Register

D7	D6	D5	D4	D3	D2	D1	D0
L11	L10	L9	L8	L7	L6	L5	L4

表 7-14. Byte 2 of the T_{LOW} Register

D7	D6	D5	D4	D3	D2	D1	D0
L3	L2	L1	L0	0	0	0	0

All 12 bits for the Temperature, T_{HIGH}, and T_{LOW} registers are used in the comparisons for the ALERT function for all converter resolutions. The three LSBs in T_{HIGH} and T_{LOW} can affect the ALERT output even if the converter is configured for 9-bit resolution.

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The TMP100-Q1 and TMP101-Q1 devices are used to measure the printed circuit board (PCB) temperature of the board location where the devices are mounted. The TMP100-Q1 features two address pins to allow up to eight devices to be addressed on a single I^2C interface. The TMP101-Q1 device features one address pin and an ALERT pin, allowing up to three devices to be connected per bus. The TMP100-Q1 and TMP101-Q1 devices require no external components for operation except for pullup resistors on SCL, SDA, and ALERT (TMP101-Q1 device), although a 0.1-µF bypass capacitor is recommended.

The sensing device of the TMP100-Q1 and TMP101-Q1 devices is the chip itself. Thermal paths run through the package leads as well as the plastic package. The die flag of the lead frame is connected to GND. The lower thermal resistance of metal causes the leads to provide the primary thermal path. The GND pin of the TMP100-Q1 or TMP101-Q1 device is directly connected to the metal lead frame, and is the best choice for thermal input.

8.2 Typical Application

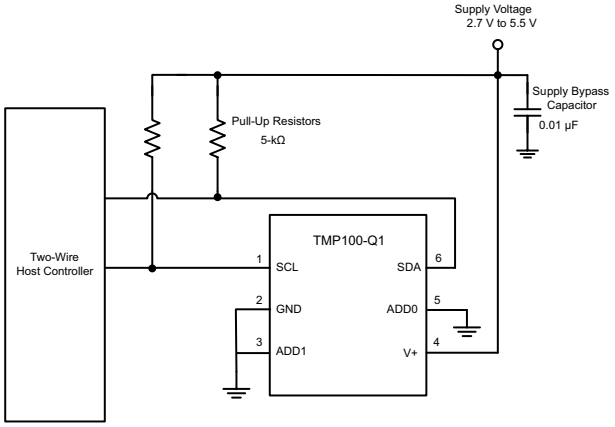

図 8-1. Typical Connections of the TMP100-Q1

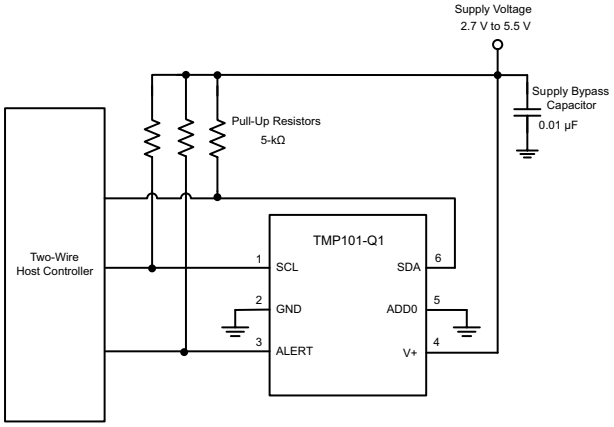

図 8-2. Typical Connections of the TMP101-Q1

8.2.1 Design Requirements

The TMP100-Q1 and TMP101-Q1 devices require pullup resistors on the SCL, SDA, and ALERT (TMP101-Q1 device) pins. The recommended value for the pullup resistor is 5-kΩ. In some applications, the pullup resistor can be lower or higher than 5-kΩ but must not exceed 3 mA of current on the SCL and SDA pins, and must not exceed 4 mA on the ALERT (TMP101-Q1) pin. A 0.1-µF bypass capacitor is recommended, as shown in 図 8-1 and 図 8-2. The SCL, SDA, and ALERT lines can be pulled up to a supply that is equal to or higher than V_S through the pullup resistors. For the TMP100-Q1, to configure one of eight different addresses on the bus, connect ADD0 and ADD1 to either the GND pin, V+ pin, or float. Float indicates the pin is left unconnected. For the TMP101-Q1 device, to configure one of three different addresses on the bus, connect ADD0 to either the GND pin, V+ pin, or float.

8.2.2 Detailed Design Procedure

Place the TMP100-Q1 and TMP101-Q1 devices in close proximity to the heat source that must be monitored, with a proper layout for good thermal coupling. This placement ensures that temperature changes are captured within the shortest possible time interval. To maintain accuracy in applications that require air or surface

temperature measurement, care must be taken to isolate the package and leads from ambient air temperature. A thermally-conductive adhesive is helpful in achieving accurate surface temperature measurement.

8.2.3 Application Curve

図 8-3 shows the step response of the TMP100-Q1 and TMP101-Q1 devices to a submersion in an oil bath of 100°C from room temperature (27°C). The time constant, or the time for the output to reach 63% of the input step, is 0.9 s. The time-constant result depends on the PCB that the TMP100-Q1 and TMP101-Q1 devices are mounted. For this test, the TMP100-Q1 and TMP101-Q1 devices are soldered to a two-layer PCB that measures 0.375 inch × 0.437 inch.

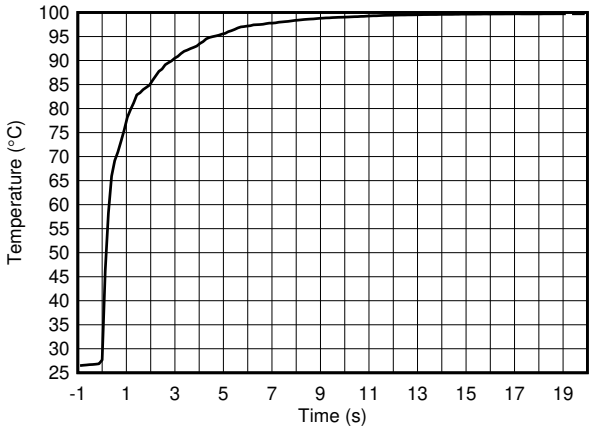

図 8-3. Temperature Step Response

9 Power Supply Recommendations

The TMP100-Q1 and TMP101-Q1 devices operate with power supply in the range of 2.7 V to 5.5 V. A power-supply bypass capacitor is required for stability; place this capacitor as close as possible to the supply and ground pins of the device. A typical value for this supply bypass capacitor is 0.01 µF. Applications with noisy or high-impedance power supplies can require additional decoupling capacitors to reject power-supply noise.

10 Layout

10.1 Layout Guidelines

Place the power-supply bypass capacitor as close as possible to the supply and ground pins. The recommended value of this bypass capacitor is 0.01 µF. Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies. Pull up the open-drain output pins SDA , SCL, and ALERT (TMP101-Q1) through 5-kΩ pullup resistors.

10.2 Layout Examples

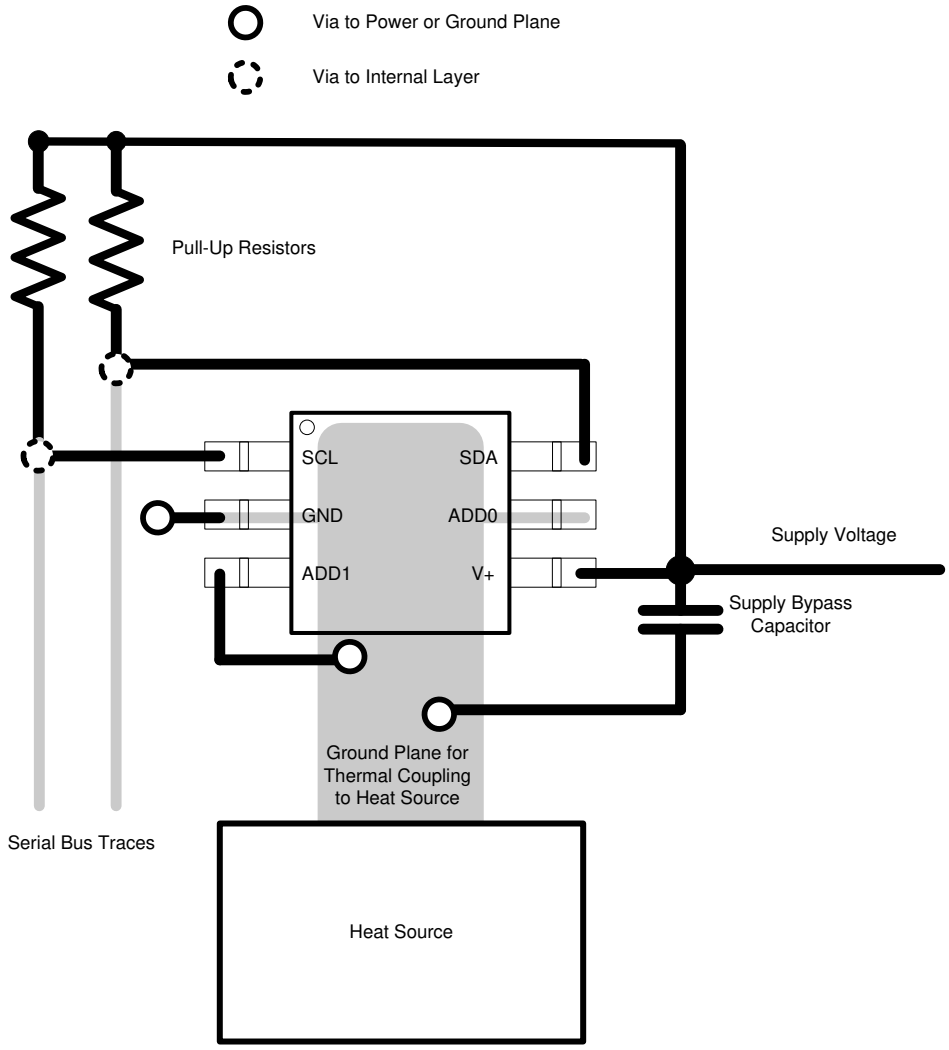

図 10-1. TMP100-Q1 Layout Example

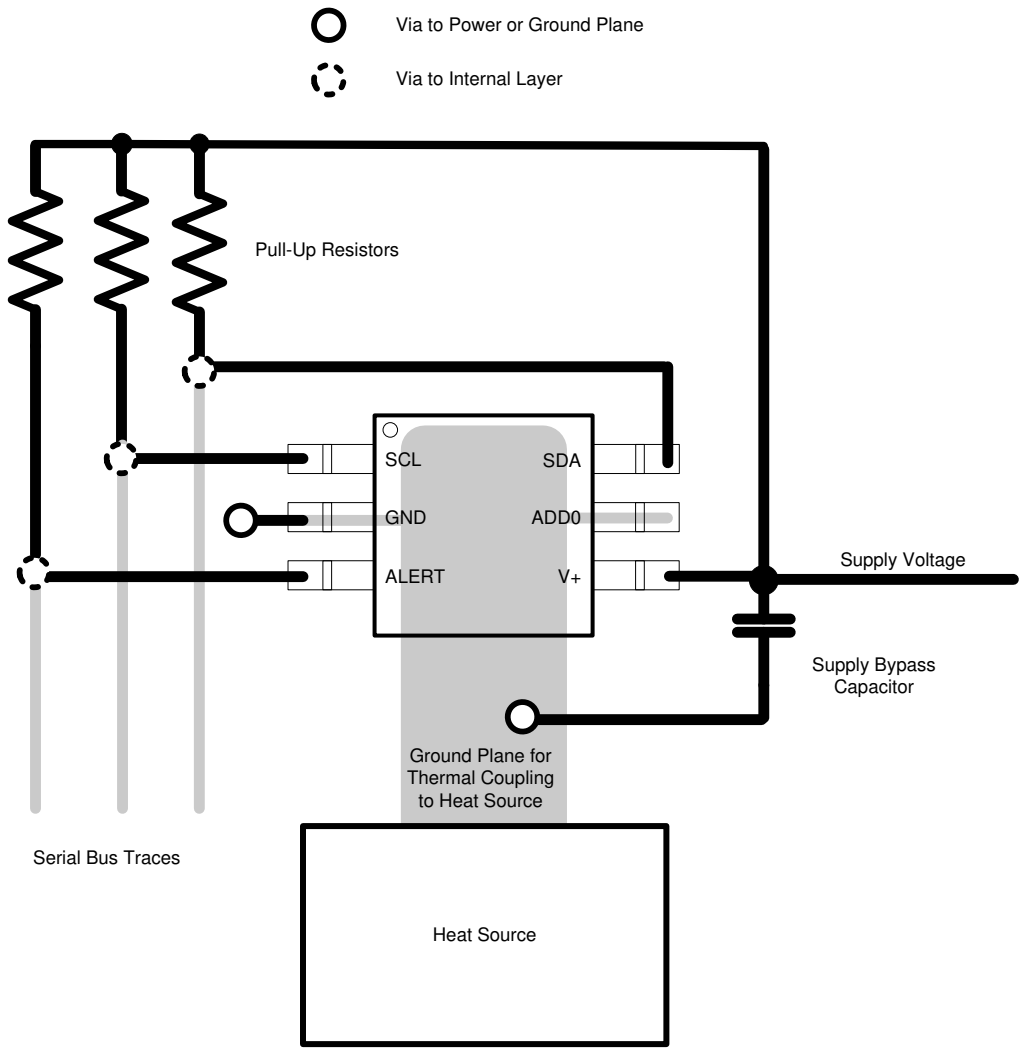

図 10-2. TMP101-Q1 Layout Example

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 サポート・リソース

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TI E2E™ is a trademark of Texas Instruments.
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11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMP100AQDBVRQ1	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	100Q
TMP100AQDBVRQ1.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	100Q
TMP101NAQDBVRQ1	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DUGQ
TMP101NAQDBVRQ1.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DUGQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TMP100-Q1, TMP101-Q1 :

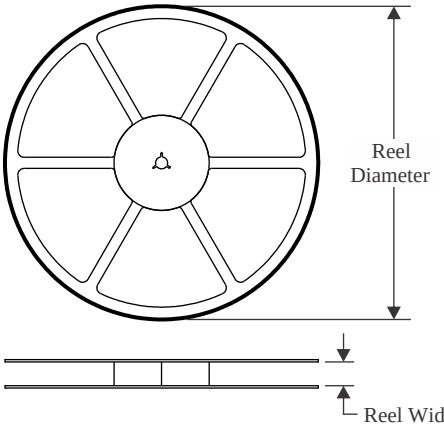
- Catalog : TMP100, TMP101
- Enhanced Product : TMP100-EP

NOTE: Qualified Version Definitions:

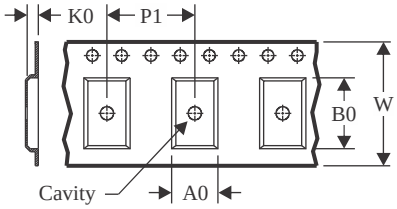
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

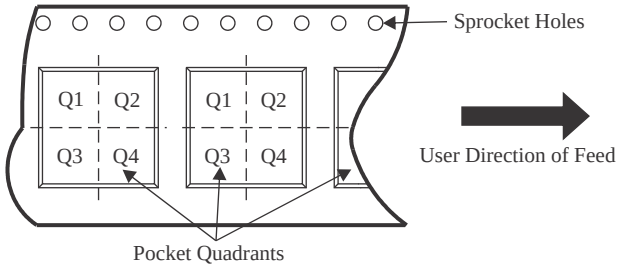


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

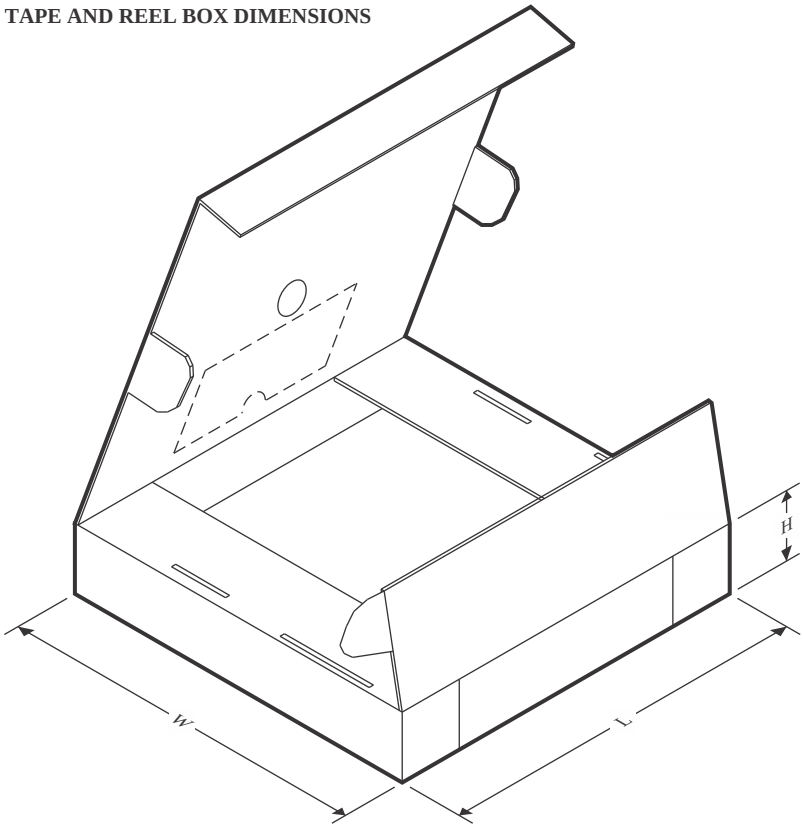
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP100AQDBVRQ1	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TMP101NAQDBVRQ1	SOT-23	DBV	6	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

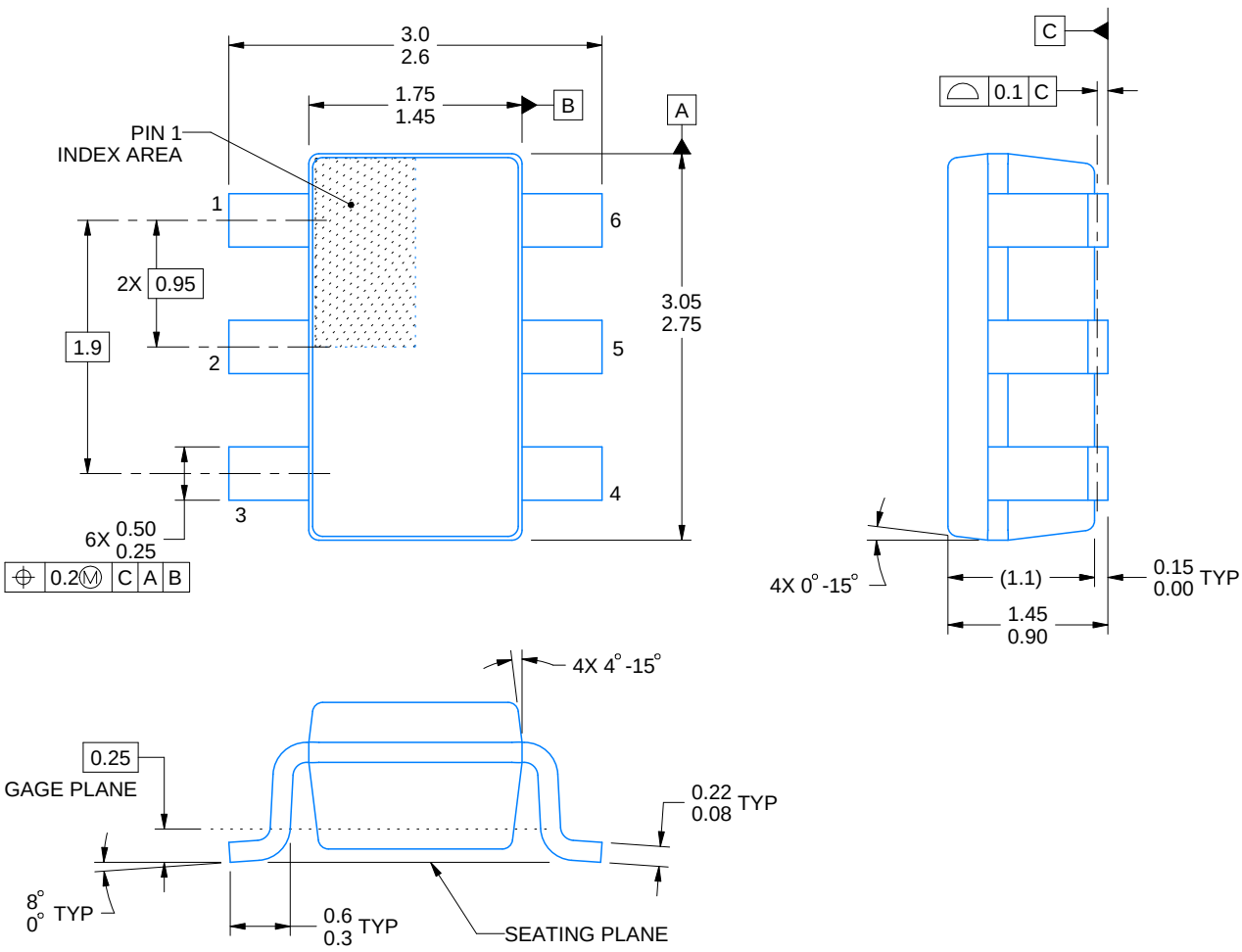
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP100AQDBVRQ1	SOT-23	DBV	6	3000	445.0	220.0	345.0
TMP101NAQDBVRQ1	SOT-23	DBV	6	3000	445.0	220.0	345.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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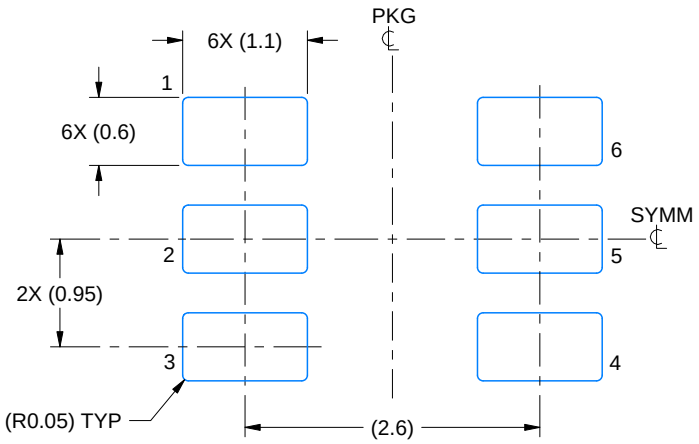
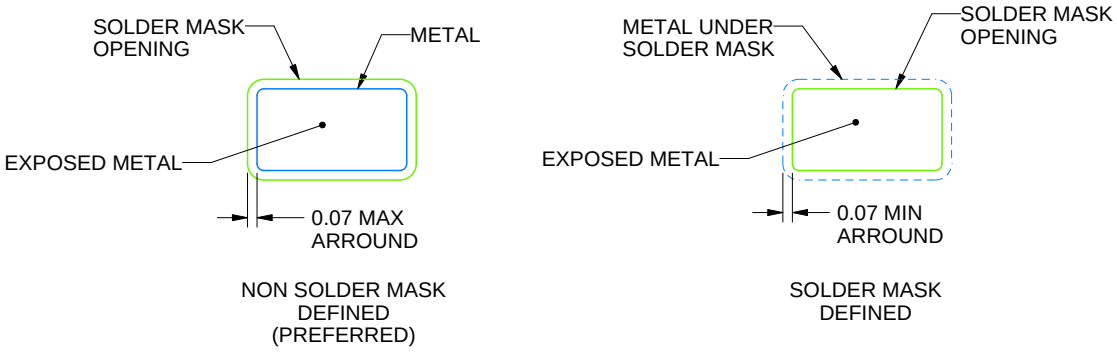
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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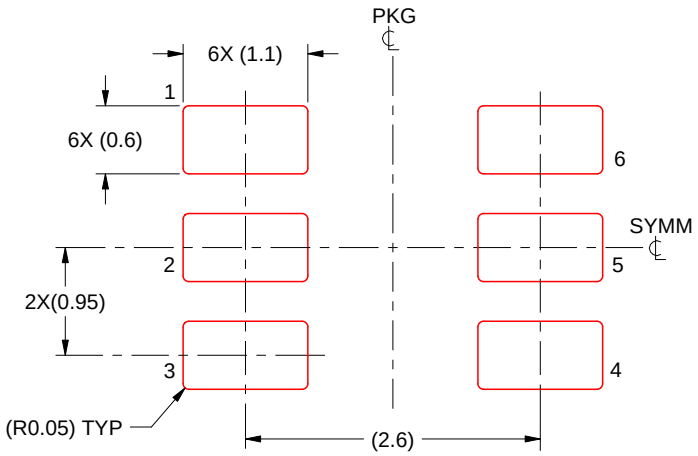
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月