TLV930x-Q1 コスト重視システム向け 40V、1MHz、RRO オペアンプ

1 特長

- 低いオフセット電圧:±0.5mV
- 低いオフセット電圧ドリフト:±2µV/℃
- 低ノイズ:1kHz で 33nV/√Hz
- 大きい同相除去:110dB
- 低いバイアス電流:±10pA
- レール ツー レール出力
- 広い帯域幅:1MHz GBW
- 高いスルーレート:3V/µs
- 低い静止電流:アンプ 1 個あたり 150µA
- 広い電源範囲:±2.25V～±20V、4.5V～40V
- 堅牢な EMI 性能:1GHz 時に 72dB
- 多重化対応 / コンパレータ入力
  - 差動および同相入力電圧範囲は電源レールまで
- 業界標準パッケージ:
  - シングル:SOT-23-5、SC70
  - デュアル:SOIC-8、TSSOP-8、VSSOP-8
  - クワッド:SOIC-14、TSSOP-14

2 アプリケーション

- 商用ネットワークとサーバーの PSU (電源)
- 産業用 AC-DC
- 商用 DC/DC
- モータードライブ:AC およびサーボ ドライブの電源
- ビル オートメーション

3 概要

TLV930x-Q1 ファミリ (TLV9301-Q1、TLV9302-Q1、TLV9304-Q1) は、コスト最適化された 40V オペアンプ ファミリです。これらのデバイスは、レール ツー レール出力、低いオフセット (±0.5mV、標準値)、低いオフセット ドリフト (±2µV/℃、標準値)、1MHz の帯域幅など、優れた汎用 DC および AC 仕様を備えています。

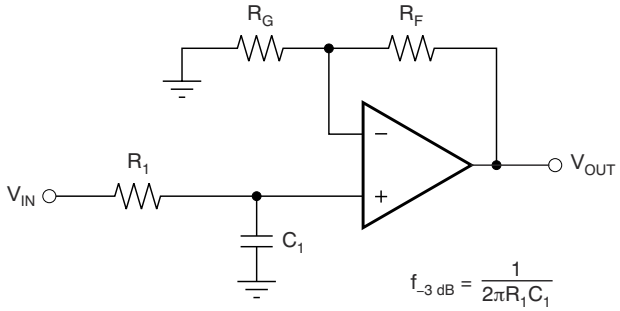
広い差動入力電圧範囲、大きな出力電流 (±60mA)、高いスルーレート (3V/µs) などの便利な特長から、TLV930x-Q1 は高電圧でコストの制約が厳しいアプリケーションに適した堅牢なオペアンプです。

TLV930x-Q1 ファミリのオペアンプは標準パッケージで供給され、-40℃～125℃で動作が規定されています。

製品情報

部品番号(1)	チャネル数	パッケージ	パッケージ サイズ(2)
TLV9301-Q1(4)	シングル	DBV (SOT-23、5)(3)	2.9mm × 2.8mm
		DCK (SC70、5)(3)	2mm × 2.1mm
TLV9302-Q1(4)	デュアル	D (SOIC、8)(3)	4.9mm × 6mm
		PW (TSSOP、8)(3)	3mm × 6.4mm
TLV9304-Q1	クワッド	D (SOIC、14)(3)	8.65mm × 6mm
		PW (TSSOP、14)	5mm × 6.4mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値で、該当する場合はピンも含まれます。
(3) このパッケージはプレビューのみです。
(4) このデバイスはプレビューのみです。



単極、ローパス フィルタの TLV930x-Q1

Table of Contents

1 特長.....1
2 アプリケーション.....1
3 概要.....1
4 Pin Configuration and Functions.....3
5 Specifications.....6
5.1 Absolute Maximum Ratings.....6
5.2 ESD Ratings.....6
5.3 Recommended Operating Conditions.....6
5.4 Thermal Information for Quad Channel.....6
5.5 Electrical Characteristics.....7
5.6 Typical Characteristics.....9
6 Detailed Description.....16
6.1 Overview.....16
6.2 Functional Block Diagram.....16
6.3 Feature Description.....17
6.4 Device Functional Modes.....24
7 Application and Implementation.....25
7.1 Application Information.....25
7.2 Typical Applications.....25
7.3 Power Supply Recommendations.....26
7.4 Layout.....26
8 Device and Documentation Support.....29
8.1 Device Support.....29
8.2 Documentation Support.....29
8.3 ドキュメントの更新通知を受け取る方法.....29
8.4 サポート・リソース.....29
8.5 Trademarks.....29
8.6 静電気放電に関する注意事項.....29
8.7 用語集.....29
9 Revision History.....30
10 Mechanical, Packaging, and Orderable Information.....30

4 Pin Configuration and Functions

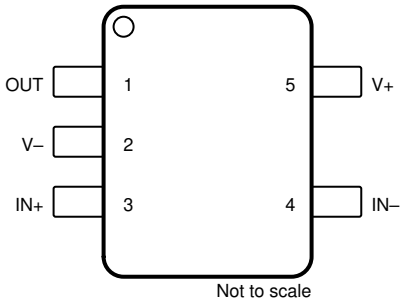


図 4-1. TLV9301-Q1 DBV Package
5-Pin SOT-23(1)
Top View

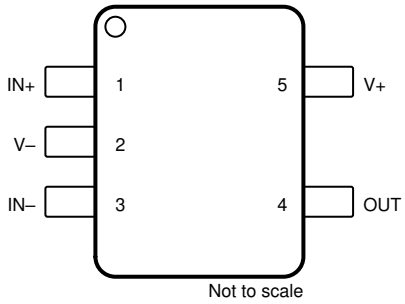


図 4-2. TLV9301-Q1 DCK Package
5-Pin SC70(2)
Top View

表 4-1. Pin Functions: TLV9301-Q1

PIN			I/O	DESCRIPTION
NAME	DBV	DCK		
+IN	3	1	I	Noninverting input
–IN	4	3	I	Inverting input
OUT	1	4	O	Output
V+	5	5	—	Positive (highest) power supply
V–	2	2	—	Negative (lowest) power supply

(1) DBV (SOT-23) package is preview only.
(2) DCK (SC70) package is preview only.

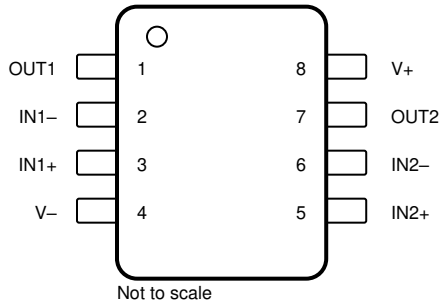


図 4-3. TLV9302-Q1 D and PW Package 8-Pin SOIC and TSSOP(1) Top View

表 4-2. Pin Functions: TLV9302-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
+IN A	3	I	Noninverting input, channel A
+IN B	5	I	Noninverting input, channel B
–IN A	2	I	Inverting input, channel A
–IN B	6	I	Inverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V+	8	—	Positive (highest) power supply
V–	4	—	Negative (lowest) power supply

(1) D (SOIC) and PW (TSSOP) packages are preview only.

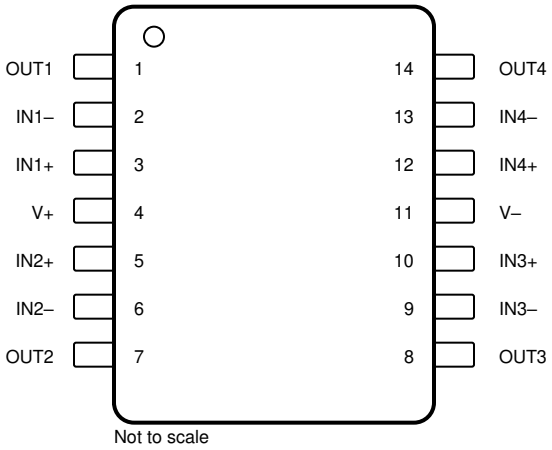


図 4-4. TLV9304-Q1 D and PW Package 14-Pin SOIC(1) and TSSOP Top View

表 4-3. Pin Functions: TLV9304-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
+IN A	3	I	Noninverting input, channel A
+IN B	5	I	Noninverting input, channel B
+IN C	10	I	Noninverting input, channel C
+IN D	12	I	Noninverting input, channel D
–IN A	2	I	Inverting input, channel A
–IN B	6	I	Inverting input, channel B
–IN C	9	I	Inverting input, channel C
–IN D	13	I	Inverting input, channel D
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
OUT C	8	O	Output, channel C
OUT D	14	O	Output, channel D
V+	4	—	Positive (highest) power supply
V–	11	—	Negative (lowest) power supply

(1) D (SOIC) package is preview only.

5 Specifications

5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)		0	42	V
Signal input pins	Common-mode voltage(3)	(V–) – 0.5	(V+) + 0.5	V
	Differential voltage(3)		V_S + 0.2	V
	Current(3)	–10	10	mA
Output short-circuit(2)		Continuous		
Operating ambient temperature, T_A		–55	150	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Short-circuit to ground, one amplifier per package.
(3) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5V beyond the supply rails must be current limited to 10mA or less.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC specification JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage, (V+) – (V–)	4.5	40	V
V_I	Input voltage range	(V–) – 0.1	(V+) – 2	V
T_A	Specified temperature	–40	125	°C

5.4 Thermal Information for Quad Channel

THERMAL METRIC(1)		TLV9304-Q1		UNIT
		D (SOIC)(2)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	105.5	134.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	61.4	55.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	61.0	79.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	21.6	9.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	60.3	78.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.
(2) This package option is preview for TLV9304-Q1.

5.5 Electrical Characteristics

For V_S = (V+) – (V–) = 4.5V to 40V (±2.25V to ±20V) at T_A = 25°C, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

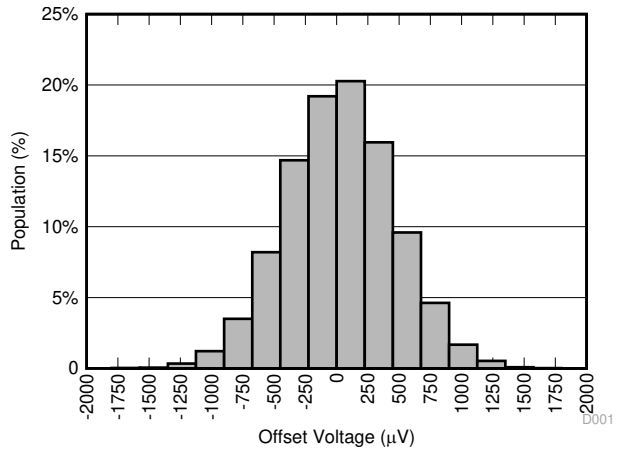
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_{CM} = V–			±0.5	±2.5	mV
			T_A = –40°C to 125°C			±2.75	
dV_{OS}/dT	Input offset voltage drift		T_A = –40°C to 125°C		±2		µV/°C
PSRR	Input offset voltage versus power supply	V_{CM} = V–	T_A = –40°C to 125°C		±2	±5	µV/V
	Channel separation	f = 0Hz			5		µV/V
INPUT BIAS CURRENT							
I_B	Input bias current				±10		pA
I_{OS}	Input offset current				±10		pA
NOISE							
E_N	Input voltage noise	f = 0.1Hz to 10Hz			6		μV_{PP}
					1		μV_{RMS}
e_N	Input voltage noise density	f = 1kHz			33		nV/√Hz
		f = 10kHz			30		
i_N	Input current noise	f = 1kHz			5		fA/√Hz
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range			(V–) – 0.2		(V+) – 2	V
CMRR	Common-mode rejection ratio	V_S = 40V, (V–) – 0.1V < V_{CM} < (V+) – 2V	T_A = –40°C to 125°C	95	110		dB
		V_S = 4.5V, (V–) – 0.1V < V_{CM} < (V+) – 2V			90		
		(V+) – 2V < V_{CM} < (V+) + 0.1V		See *Common-Mode Voltage Range*			
INPUT CAPACITANCE							
Z_{ID}	Differential				110 || 4		MΩ || pF
Z_{ICM}	Common-mode				6 || 1.5		TΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = 40V, V_{CM} = V– (V–) + 0.1V < V_O < (V+) – 0.1V		120	130		dB
			T_A = –40°C to 125°C	116	127		
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product				1		MHz
SR	Slew rate	V_S = 40V, G = +1, C_L = 20 pF			3		V/µs
t_S	Settling time	To 0.1%, V_S = 40V, V_{STEP} = 10V , G = +1, CL = 20pF			5		µs
		To 0.1%, V_S = 40V, V_{STEP} = 2V , G = +1, CL = 20pF			2.5		
		To 0.01%, V_S = 40V, V_{STEP} = 10V , G = +1, CL = 20pF			6		
		To 0.01%, V_S = 40V, V_{STEP} = 2V , G = +1, CL = 20pF			3.5		
	Phase margin	G = +1, R_L = 10kΩ, C_L = 20pF			60		°
	Overload recovery time	V_{IN} × gain > V_S			1		µs
THD+N	Total harmonic distortion + noise	V_S = 40V, V_O = 1V_{RMS}, G = -1, f = 1kHz			0.003%		

For V_S = (V+) – (V–) = 4.5V to 40V (±2.25V to ±20V) at T_A = 25°C, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
	Voltage output swing from rail	Positive and negative rail headroom	V_S = 40V, R_L = no load		3		mV
			V_S = 40V, R_L = 10kΩ		50	75	
			V_S = 40V, R_L = 2kΩ		250	350	
			V_S = 4.5V, R_L = no load		1		
			V_S = 4.5V, R_L = 10kΩ		20	30	
			V_S = 4.5V, R_L = 2kΩ		40	75	
I_{SC}	Short-circuit current				±60		mA
C_{LOAD}	Capacitive load drive				See *Typical Characteristics*		
Z_O	Open-loop output impedance	f = 1MHz, I_O = 0A			600		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0A			150	175	µA
			T_A = –40°C to 125°C			175	

5.6 Typical Characteristics

at T_A = 25°C, V_S = ±20V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ connected to V_S / 2, and C_L = 100pF (unless otherwise noted)



T_A = 25°C

図 5-1. Offset Voltage Production Distribution

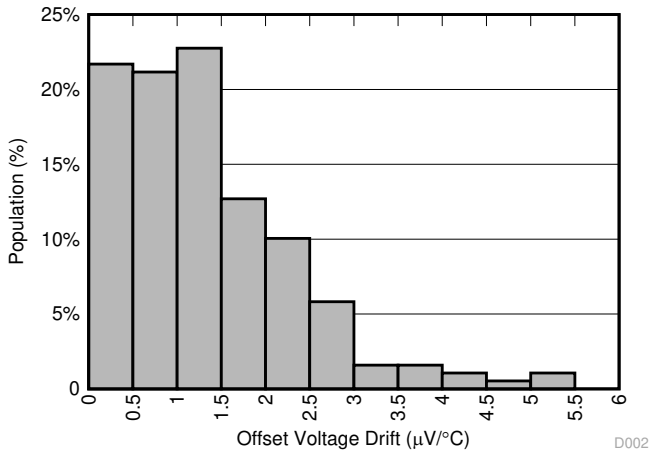
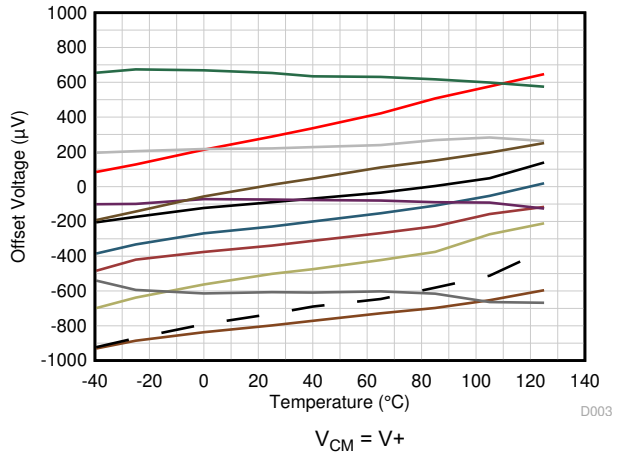
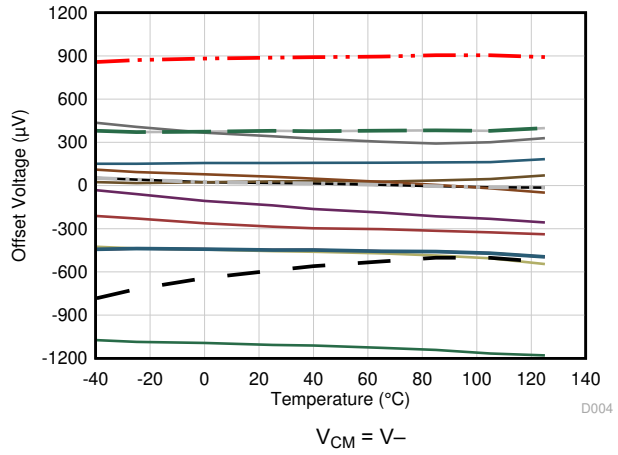


図 5-2. Offset Voltage Drift Distribution



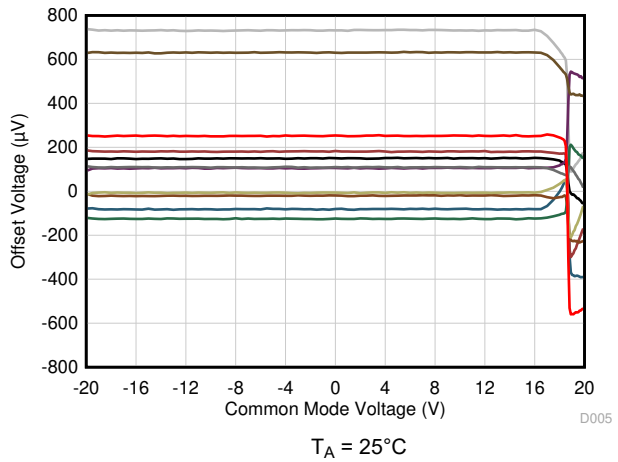
V_{CM} = V+

図 5-3. Offset Voltage vs Temperature



V_{CM} = V–

図 5-4. Offset Voltage vs Temperature



T_A = 25°C

図 5-5. Offset Voltage vs Common-Mode Voltage

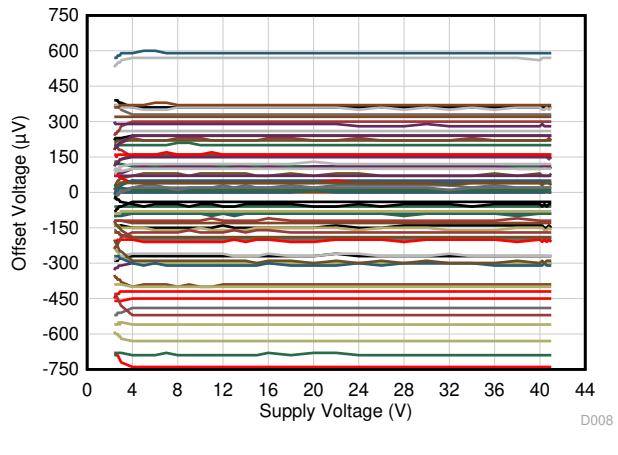
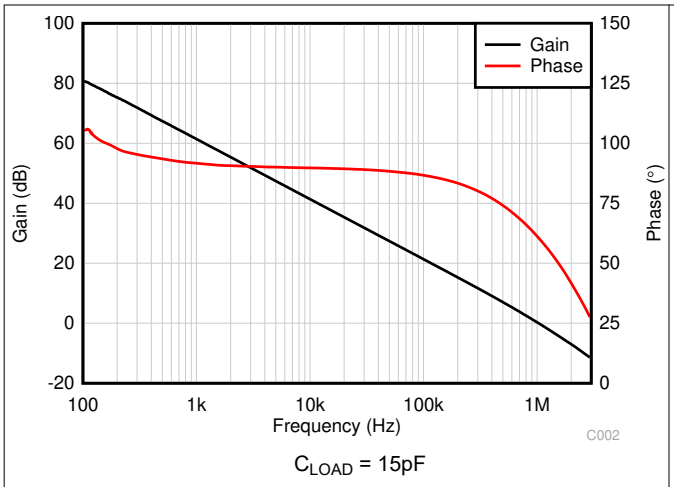


図 5-6. Offset Voltage vs Power Supply

5.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±20V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ connected to V_S / 2, and C_L = 100pF (unless otherwise noted)



C_{LOAD} = 15pF

図 5-7. Open-Loop Gain and Phase vs Frequency

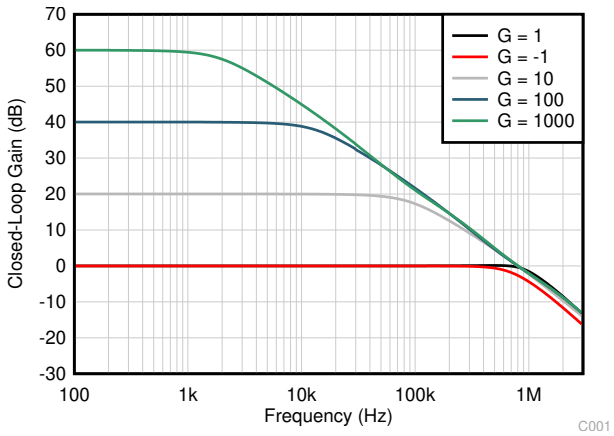


図 5-8. Closed-Loop Gain and Phase vs Frequency

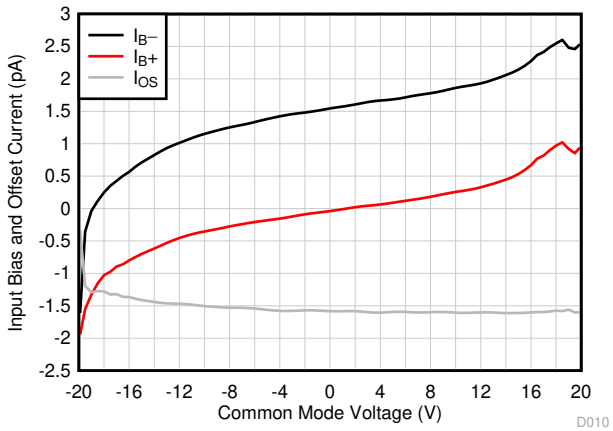


図 5-9. Input Bias Current vs Common-Mode Voltage

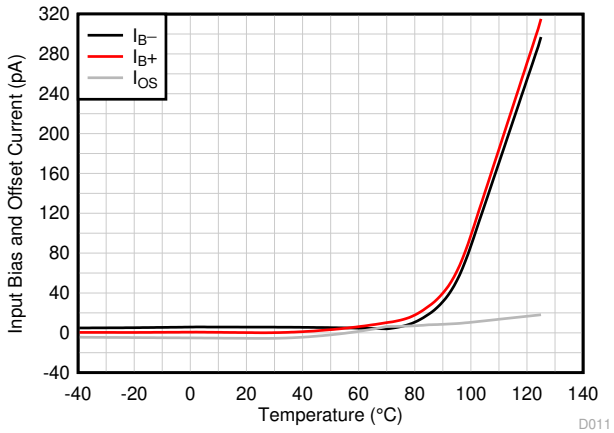


図 5-10. Input Bias Current vs Temperature

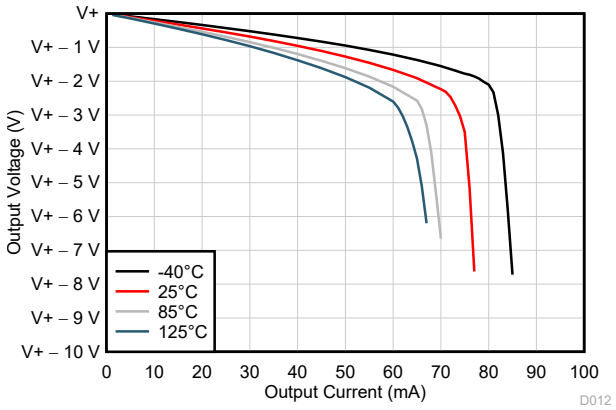


図 5-11. Output Voltage Swing vs Output Current (Sourcing)

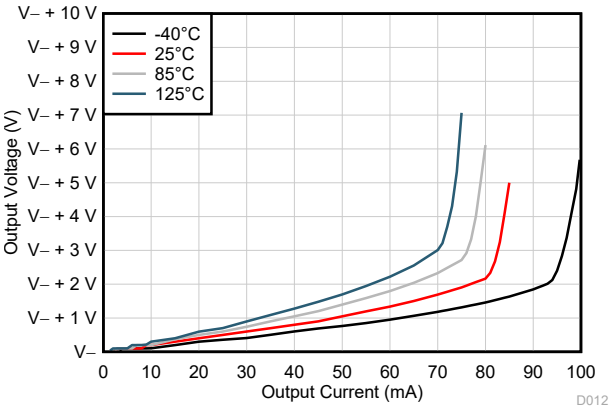
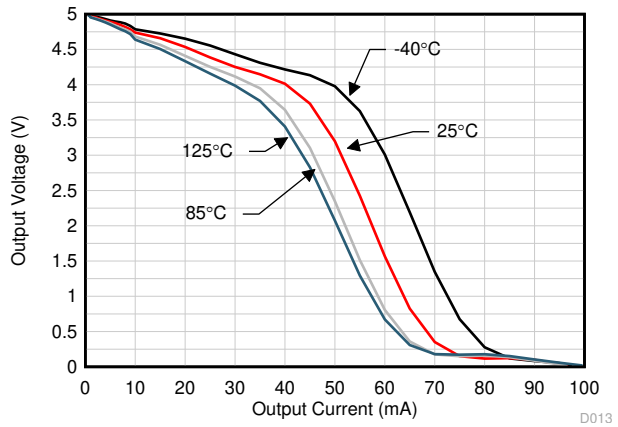


図 5-12. Output Voltage Swing vs Output Current (Sinking)

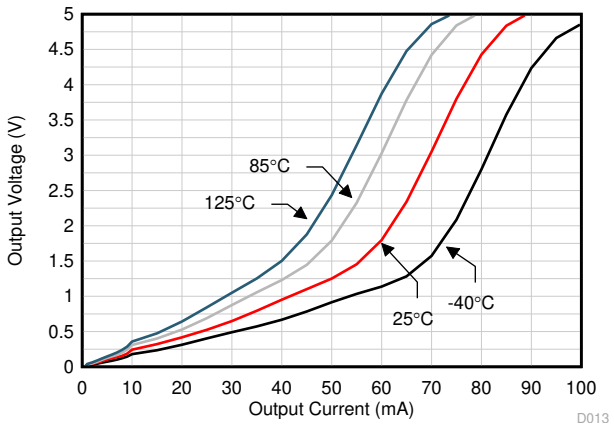
5.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±20V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ connected to V_S / 2, and C_L = 100pF (unless otherwise noted)



V_S = 5V

図 5-13. Output Voltage Swing vs Output Current (Sourcing)



V_S = 5V

図 5-14. Output Voltage Swing vs Output Current (Sinking)

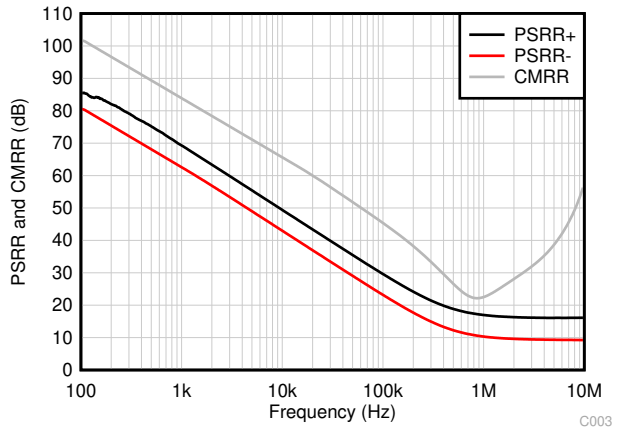
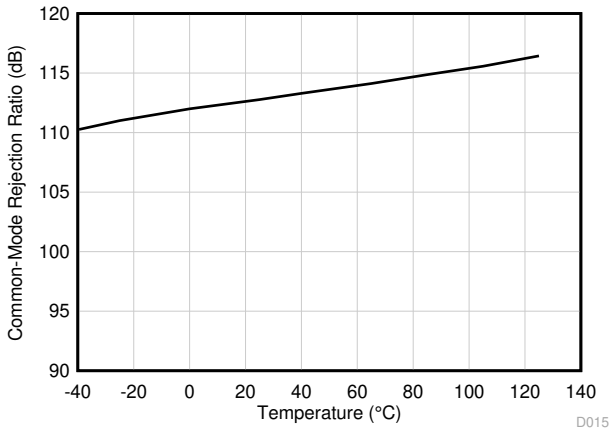
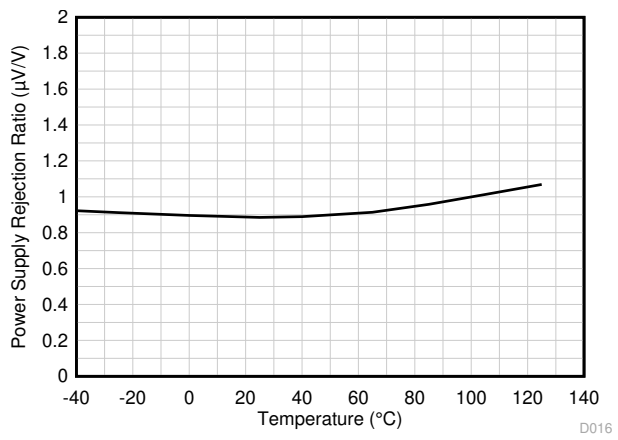


図 5-15. CMRR and PSRR vs Frequency



f = 0Hz

図 5-16. CMRR vs Temperature (dB)



f = 0Hz

図 5-17. PSRR vs Temperature (dB)

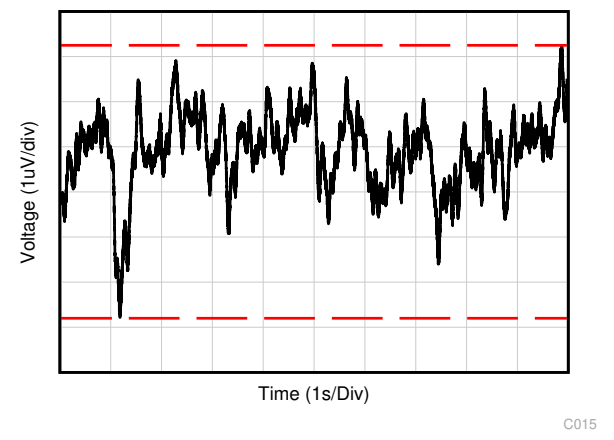


図 5-18. 0.1Hz to 10Hz Noise

5.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±20V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ connected to V_S / 2, and C_L = 100pF (unless otherwise noted)

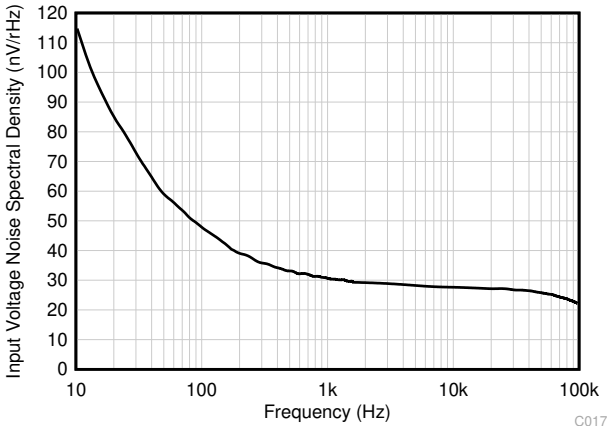
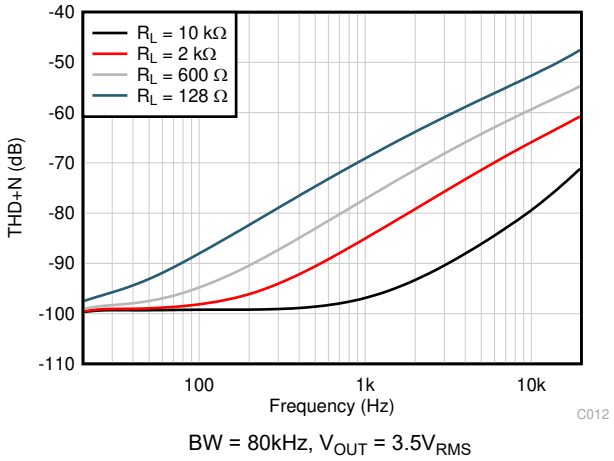
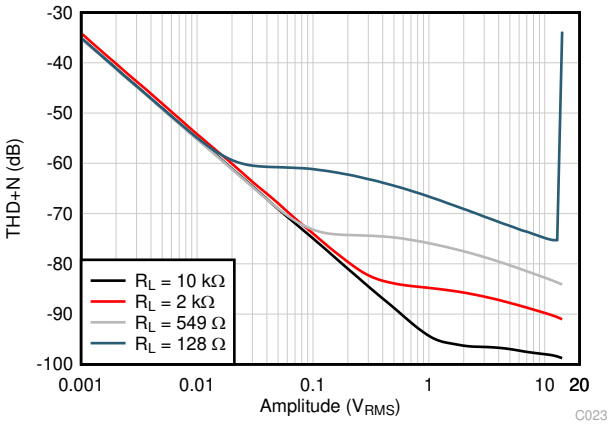


図 5-19. Input Voltage Noise Spectral Density vs Frequency



BW = 80kHz, V_{OUT} = 3.5V_{RMS}

図 5-20. THD+N Ratio vs Frequency



BW = 80kHz, f = 1kHz

図 5-21. THD+N vs Output Amplitude

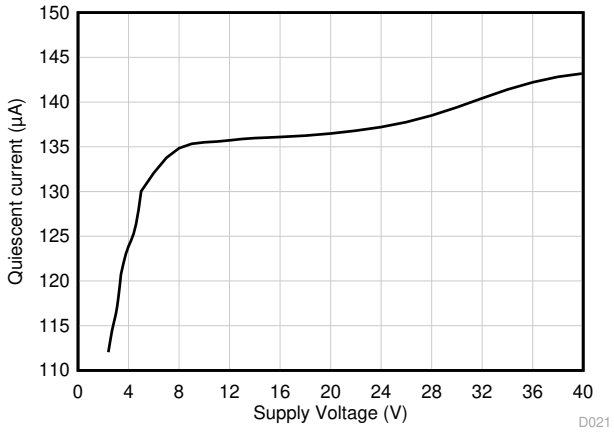


図 5-22. Quiescent Current vs Supply Voltage

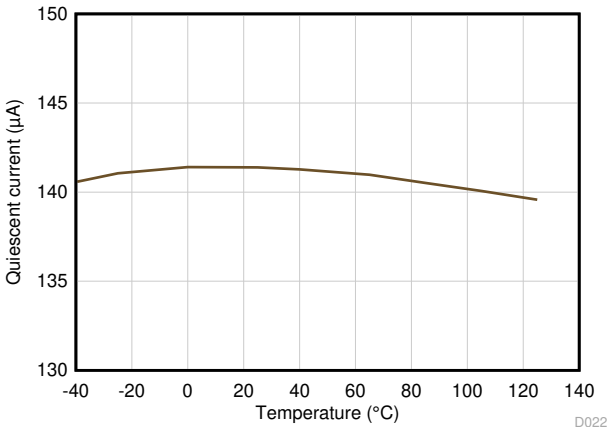


図 5-23. Quiescent Current vs Temperature

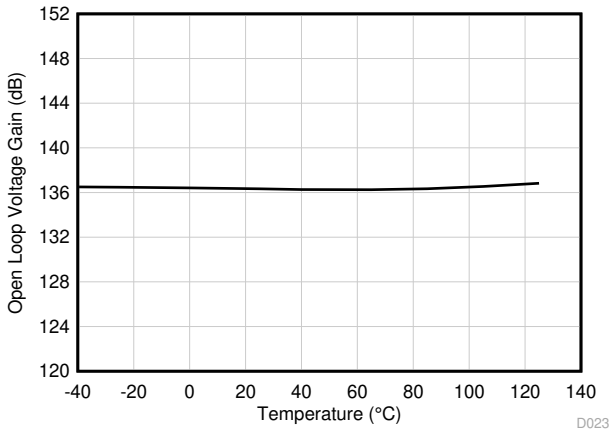


図 5-24. Open-Loop Voltage Gain vs Temperature (dB)

5.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±20V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ connected to V_S / 2, and C_L = 100pF (unless otherwise noted)

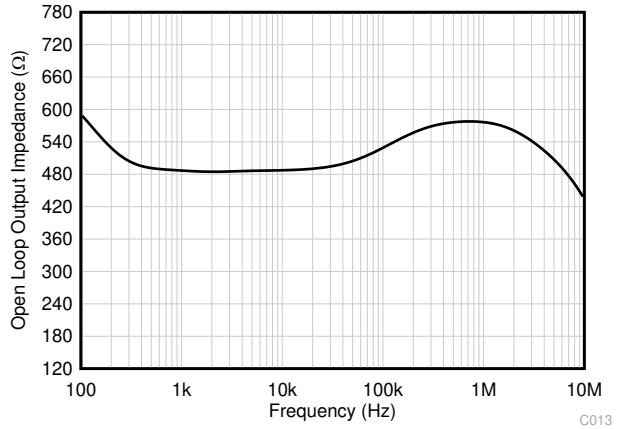
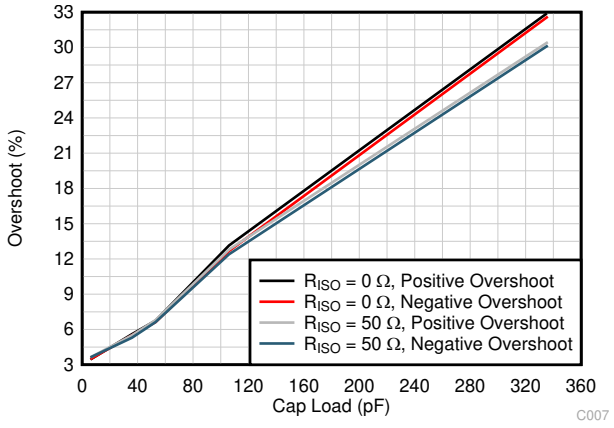
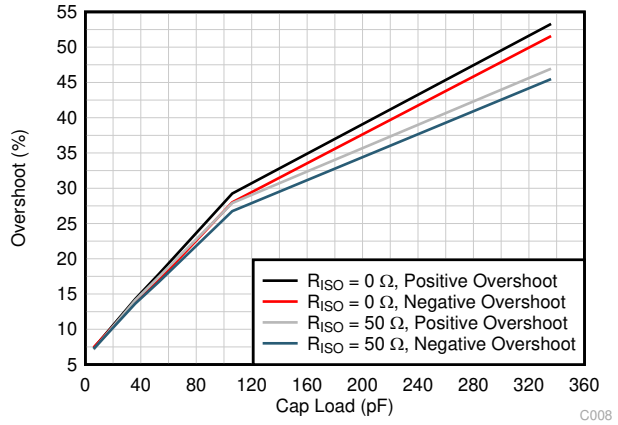


図 5-25. Open-Loop Output Impedance vs Frequency



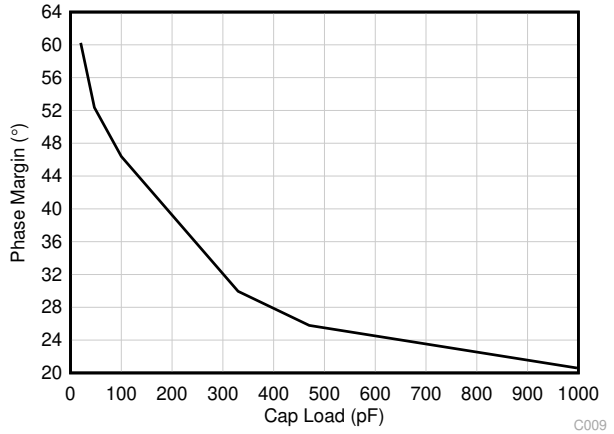
G = –1, 100mV output step

図 5-26. Small-Signal Overshoot vs Capacitive Load



G = 1, 100mV output step

図 5-27. Small-Signal Overshoot vs Capacitive Load



G = –1, 100mV output step

図 5-28. Small-Signal Overshoot vs Capacitive Load

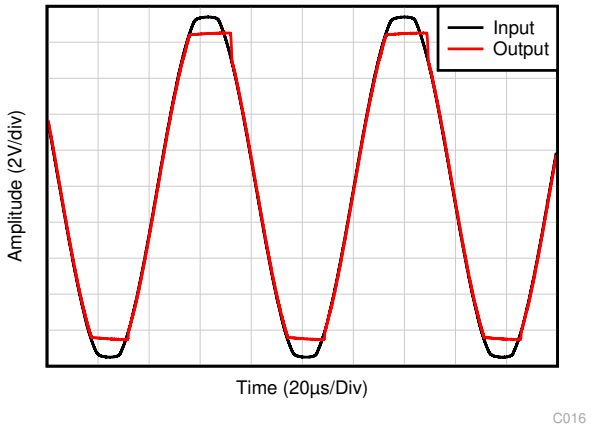
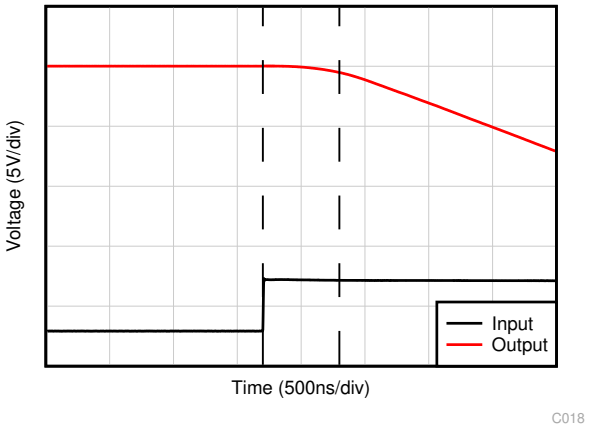


図 5-29. No Phase Reversal

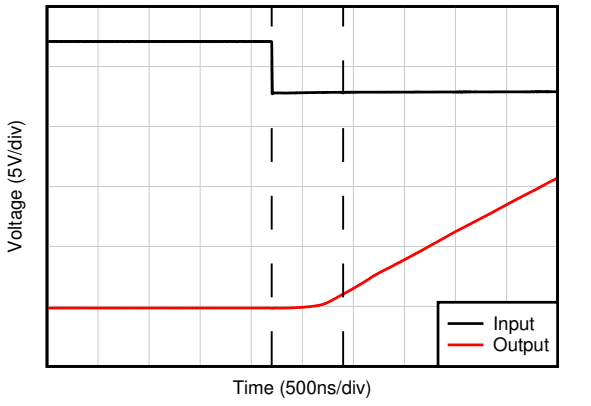


G = –10

図 5-30. Positive Overload Recovery

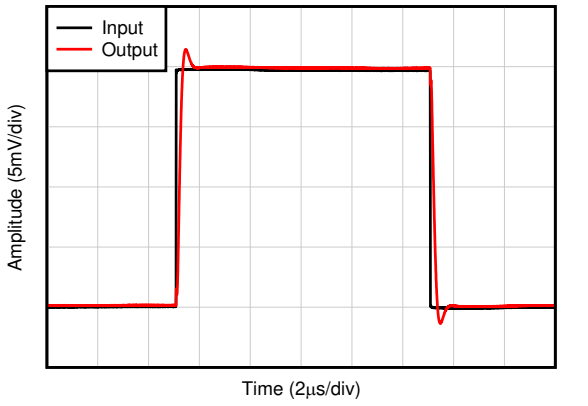
5.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±20V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ connected to V_S / 2, and C_L = 100pF (unless otherwise noted)



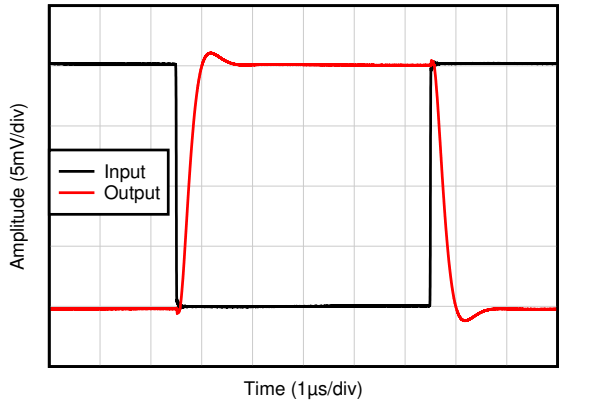
G = –10

図 5-31. Negative Overload Recovery



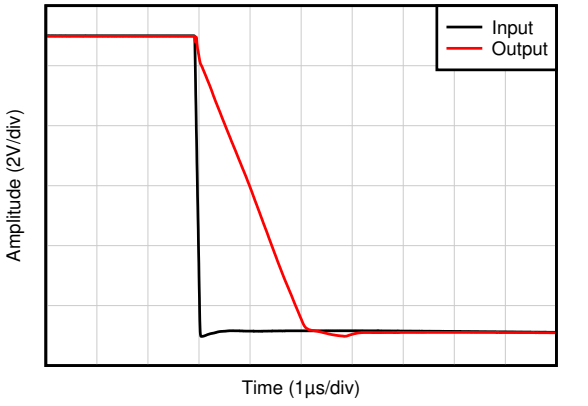
C_L = 20pF, G = 1, 20mV step response

図 5-32. Small-Signal Step Response



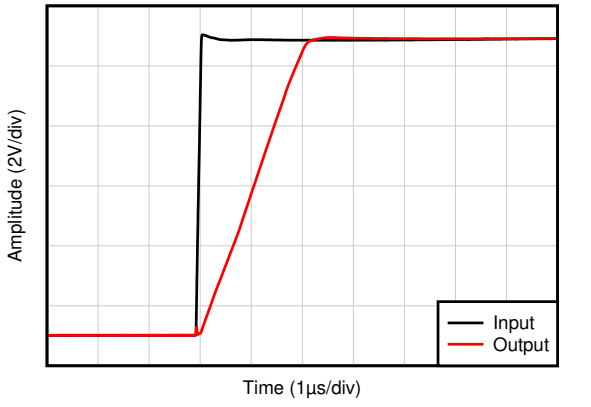
R_L = 1kΩ, C_L = 20pF, G = –1, 10mV step response

図 5-33. Small-Signal Step Response



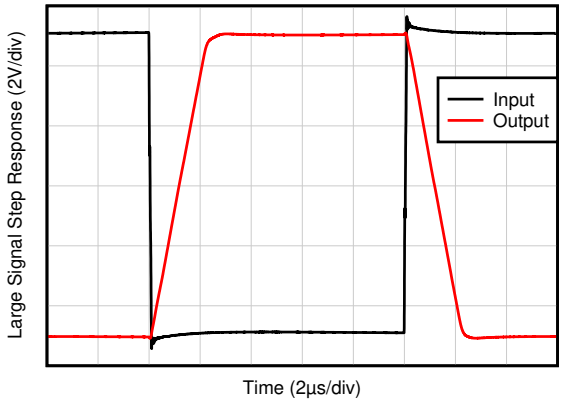
C_L = 20pF, G = 1

図 5-34. Large-Signal Step Response (Falling)



C_L = 20pF, G = 1

図 5-35. Large-Signal Step Response (Rising)



C_L = 10pF, G = –1

図 5-36. Large-Signal Step Response

5.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±20V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ connected to V_S / 2, and C_L = 100pF (unless otherwise noted)

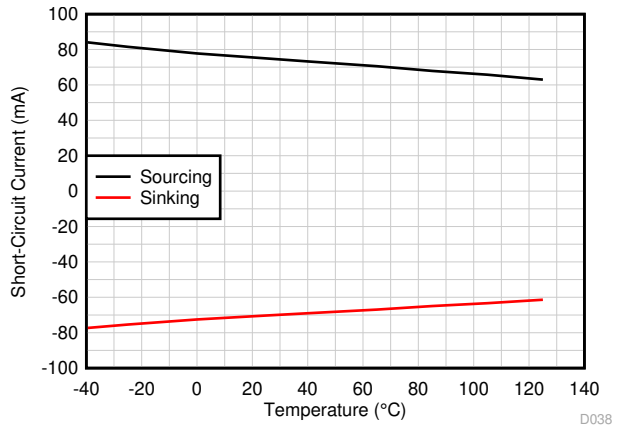


図 5-37. Short-Circuit Current vs Temperature

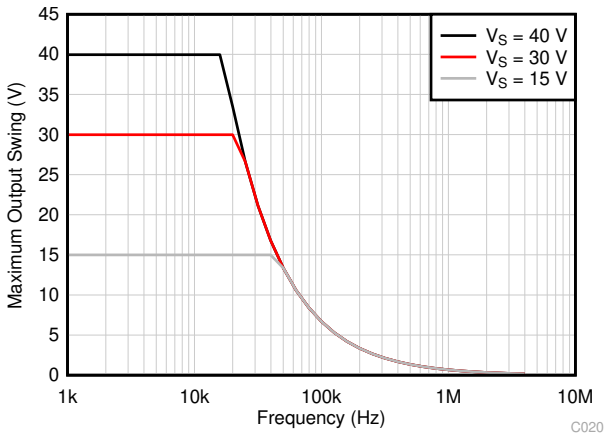


図 5-38. Maximum Output Voltage vs Frequency

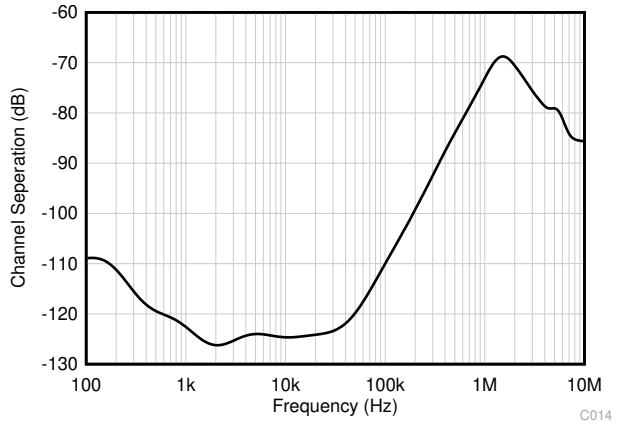


図 5-39. Channel Separation vs Frequency

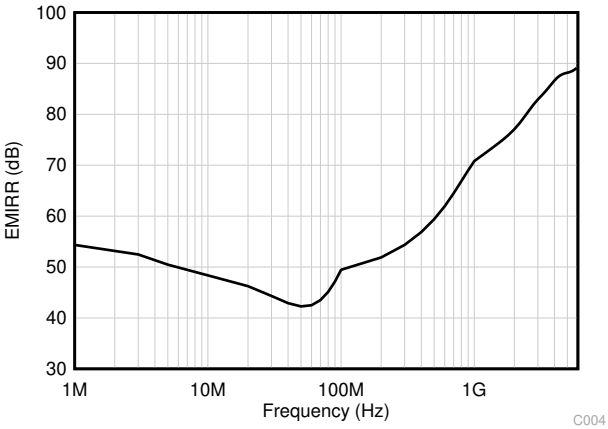


図 5-40. EMIRR (Electromagnetic Interference Rejection Ratio) vs Frequency

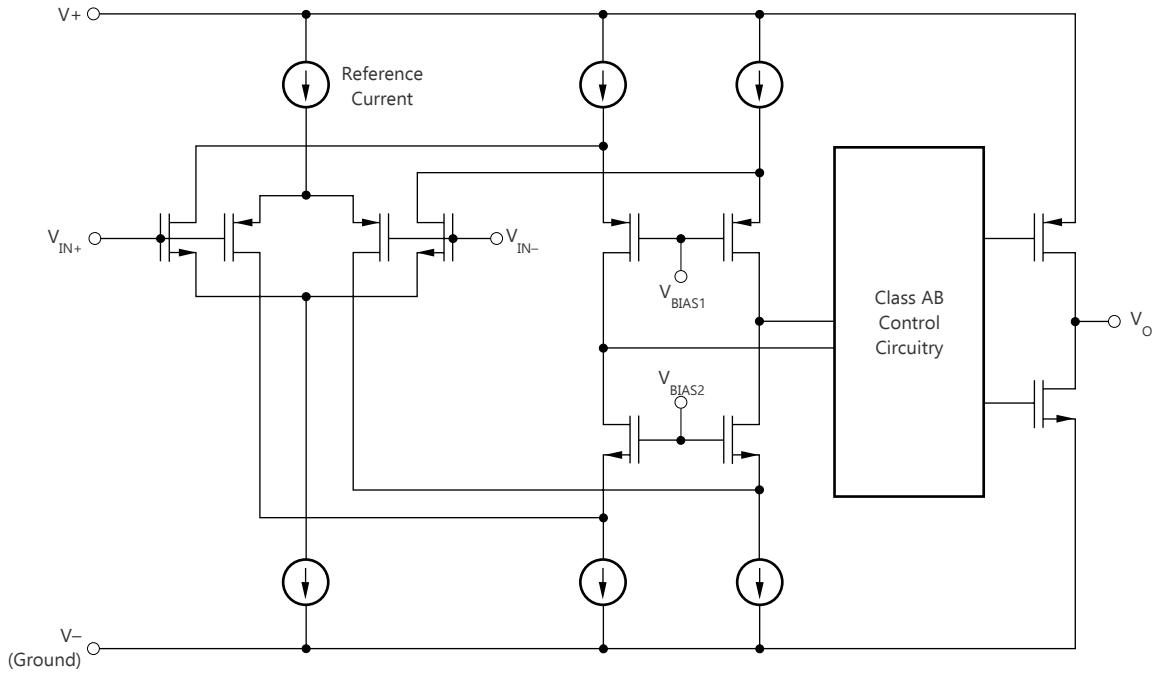
6 Detailed Description

6.1 Overview

The TLV930x-Q1 family (TLV9301-Q1, TLV9302-Q1, and TLV9304-Q1) is a family of 40V, cost-optimized operational amplifiers. These devices offer strong general-purpose DC and AC specifications, including rail-to-rail output, low offset (±0.5mV, typical), low offset drift (±2µV/°C, typical), and 1MHz bandwidth. The TLV930x-Q1 implements a complementary input stage consisting of a matched PMOS pair and matched NMOS pair. The PMOS is optimized for performance and is operational over the majority of the common-mode range, but the TLV930x-Q1 also operates (at reduced performance) when the common mode is within the NMOS region.

The TLV930x-Q1 device family offers flexibility in a range of applications. For example, a high output current (60mA, typical) can be used in a variety of biasing and driving applications with low load impedance. Wide output voltage swing across supply voltage range allows the TLV930x-Q1 to maximize dynamic range and to operate with a variety of output loads. The output impedance of the device has a very resistive frequency response, meaning the output impedance across frequency is nearly flat, which makes the device simple to stabilize with any capacitive load. The TLV930x-Q1 integrates circuitry that protects the inputs under high differential voltage, a feature uncommon to cost-optimized devices. Anti-phase reversal and thermal protection circuitry are integrated, making the device a strong option in rugged environments. This family also includes slew boost functionality, which improves transient performance under large step response and input changes while reducing quiescent current.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Input Protection Circuitry

The TLV930x-Q1 uses a patented input architecture to eliminate the requirement for input protection diodes but still provides robust input protection under transient conditions. 図 6-1 shows conventional input diode protection schemes that are activated by fast transient step responses and introduce signal distortion and settling time delays because of alternate current paths, as shown in 図 6-2. For low-gain circuits, these fast-ramping input signals forward-bias back-to-back diodes, causing an increase in input current and resulting in extended settling time.

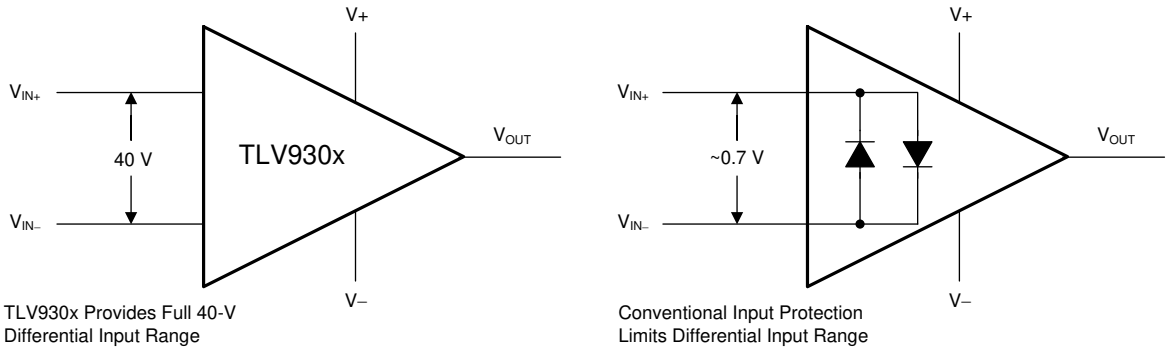


図 6-1. TLV930x-Q1 Input Protection Does Not Limit Differential Input Capability

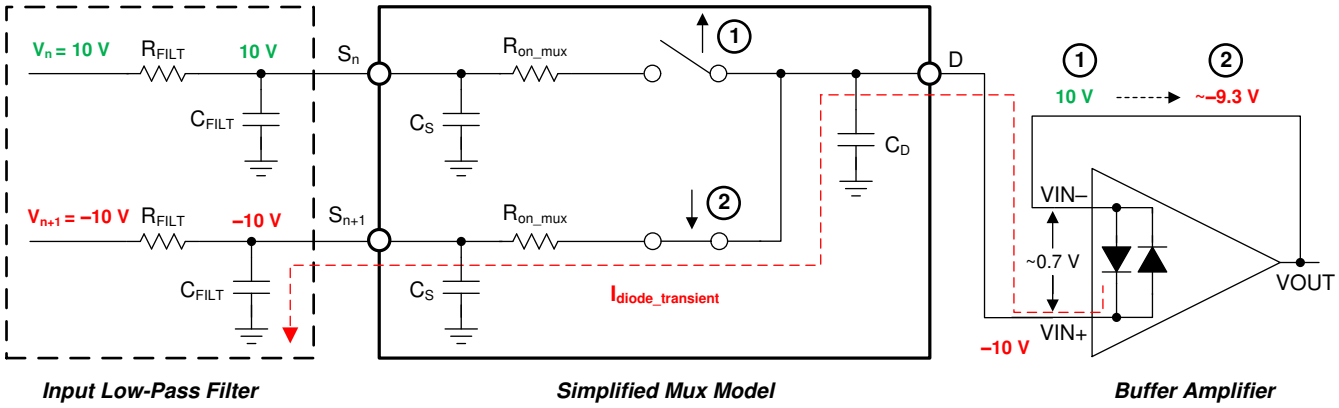


図 6-2. Back-to-Back Diodes Create Settling Issues

The TLV930x-Q1 family of operational amplifiers provides a true high-impedance differential input capability for high-voltage applications. This patented input protection architecture does not introduce additional signal distortion or delayed settling time, as the device is designed for multichannel, high-switched, input applications. The TLV930x-Q1 also tolerates a maximum differential swing (voltage between inverting and noninverting pins of the op amp) of up to 40V, therefore the device can be used as a comparator or in applications with fast-ramping input signals.

6.3.2 EMI Rejection

The TLV930x-Q1 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the TLV930x-Q1 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10MHz to 6GHz. 図 6-3 shows the results of this testing on the TLV930x-Q1. 表 6-1 shows the EMIRR IN+ values for the TLV930x-Q1 at particular frequencies commonly encountered in real-world applications. 表 6-1 lists applications that may be centered on or operated near the particular frequency shown. The *EMI Rejection Ratio of Operational Amplifiers* application note contains detailed information on the topic of EMIRR performance as it relates to operational amplifiers.

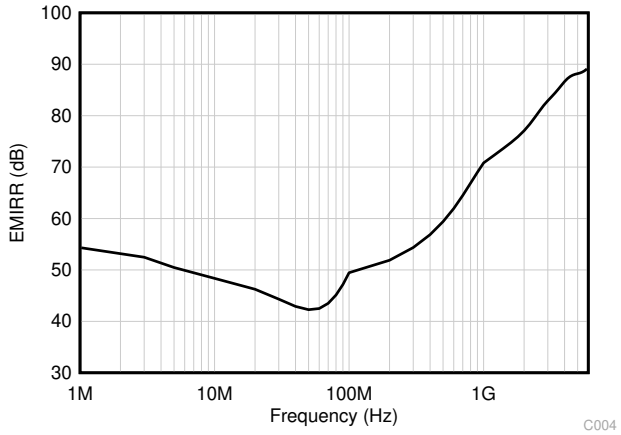


図 6-3. EMIRR Testing

表 6-1. TLV930x-Q1 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	59.5dB
900MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6GHz), GSM, aeronautical mobile, UHF applications	68.9dB
1.8GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1GHz to 2GHz)	77.8dB
2.4GHz	802.11b, 802.11g, 802.11n, Bluetooth® wireless technology, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2GHz to 4GHz)	78.0dB
3.6GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	88.8dB
5GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4GHz to 8GHz)	87.6dB

6.3.3 Phase Reversal Protection

The TLV930x-Q1 family has internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The TLV930x-Q1 is a rail-to-rail input op amp; therefore, the common-mode range can extend up to the rails. Input signals beyond the rails do not cause phase reversal; instead, the output limits into the appropriate rail. 図 6-4 shows this performance.

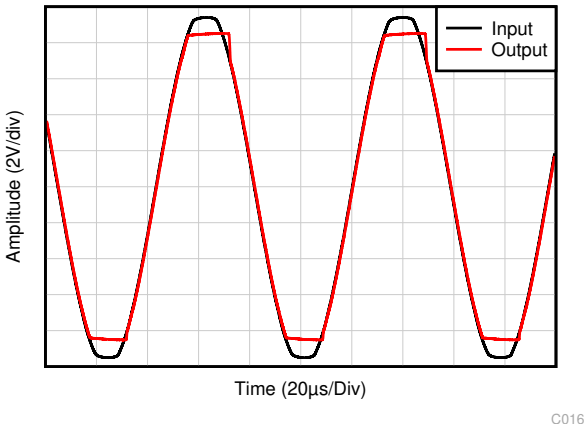


図 6-4. No Phase Reversal

6.3.4 Thermal Protection

The internal power dissipation of any amplifier causes the internal (junction) temperature to rise. This phenomenon is called *self heating*. The absolute maximum junction temperature of the TLV930x-Q1 is 150°C. Exceeding this temperature causes damage to the device. The TLV930x-Q1 has a thermal protection feature that prevents damage from self heating. The protection works by monitoring the temperature of the device and turning off the op amp output drive for temperatures above 140°C. 図 6-5 shows an application example for the TLV9301-Q1 that has significant self heating (159°C) because of the power dissipation (0.81W). Thermal calculations indicate that for an ambient temperature of 65°C the device junction temperature must reach 187°C. The actual device, however, turns off the output drive to maintain a safe junction temperature. 図 6-5 shows how the circuit behaves during thermal protection. During normal operation, the device acts as a buffer so the output is 3V. When self heating causes the device junction temperature to increase above 140°C, the thermal protection forces the output to a high-impedance state and the output is pulled to ground through resistor RL.

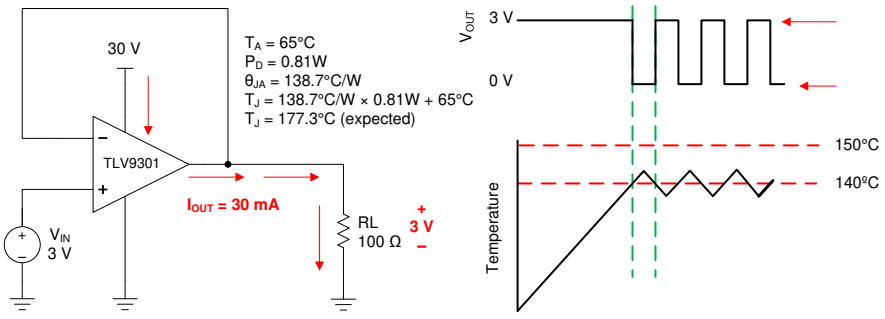


図 6-5. Thermal Protection

6.3.5 Capacitive Load and Stability

The TLV930x-Q1 features a resistive output stage capable of driving smaller capacitive loads, and by leveraging an isolation resistor, the device can easily be configured to drive large capacitive loads. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads; see 図 6-6 and 図 6-7. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier is stable in operation.

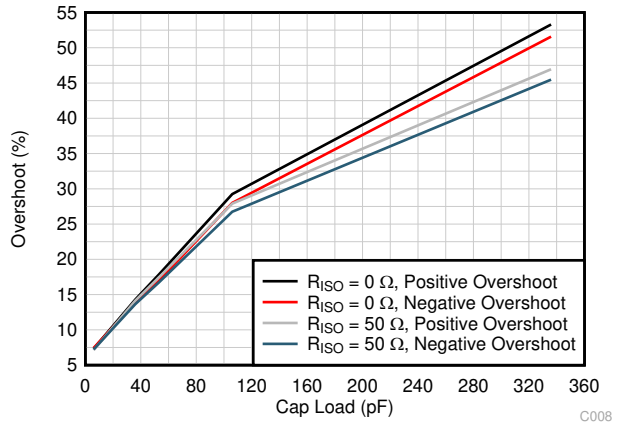


図 6-6. Small-Signal Overshoot vs Capacitive Load (100mV Output Step, G = 1)

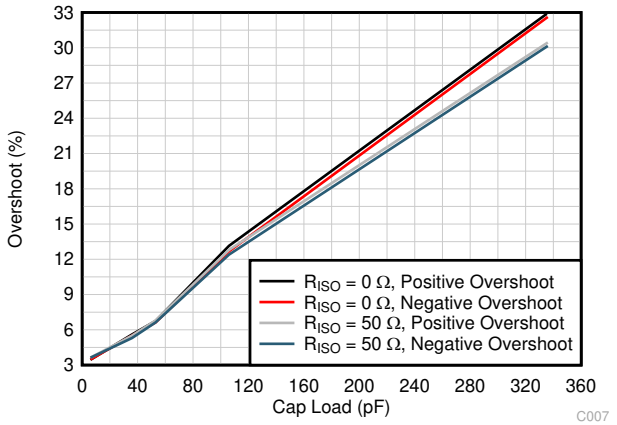


図 6-7. Small-Signal Overshoot vs Capacitive Load (100mV Output Step, G = –1)

For additional drive capability in unity-gain configurations, improve capacitive load drive by inserting a small (10Ω to 20Ω) resistor, R_{ISO}, in series with the output, as shown in 図 6-8. This resistor significantly reduces ringing and maintains DC performance for purely capacitive loads. However, if a resistive load is in parallel with the capacitive load, then a voltage divider is created, thus introducing a gain error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio R_{ISO} / R_L, and is generally negligible at low output levels. The high capacitive load drive of the TLV930x-Q1 is designed for applications such as reference buffers, MOSFET gate drives, and cable-shield drives. The circuit shown in 図 6-8 uses an isolation resistor, R_{ISO}, to stabilize the output of an op amp. R_{ISO} modifies the open-loop gain of the system for increased phase margin. For additional information on techniques to optimize and design using this circuit, TI Precision Design TIDU032 details complete design goals, simulation, and test results.

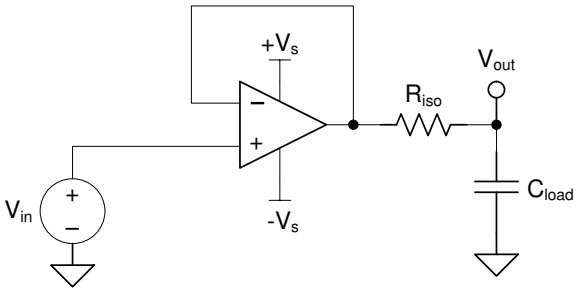


図 6-8. Extending Capacitive Load Drive With the TLV9301-Q1

6.3.6 Common-Mode Voltage Range

The TLV930x-Q1 is a 40V, rail-to-rail output operational amplifier with an input common-mode range that extends 100mV beyond V– and within 2V of V+ for normal operation. The device accomplishes this performance through a complementary input stage, using a P-channel differential pair. Additionally, a complementary N-channel differential pair has been included in parallel with the P-channel pair to eliminate common undesirable op amp behaviors, such as phase reversal.

The TLV930x-Q1 can operate with common mode ranges beyond 100mV of the top rail, but with reduced performance above (V+) – 2V. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1V to 100mV above the positive supply. The P-channel pair is active for inputs from 100mV below the negative supply to approximately (V+) – 2V. There is a small transition region, typically (V+) –2V to (V+) – 1V in which both input pairs are on. This transition region can vary modestly with process variation, and within the transition region and N-channel region, many specifications of the op amp (including PSRR, CMRR, offset voltage, offset drift, noise and THD performance) can be degraded compared to operation within the P-channel region.

表 6-2. Typical Performance for Common-Mode Voltages Within 2V of the Positive Supply

PARAMETER	MIN	TYP	MAX	UNIT
Input common-mode voltage	(V+) – 2		(V+) + 0.1	V
Offset voltage		1.5		mV
Offset voltage drift		2		µV/°C
Common-mode rejection		75		dB
Open-loop gain		75		dB
Gain-bandwidth product		0.7		MHz

6.3.7 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress (EOS). These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

A good understanding of this basic ESD circuitry and the relevance to an electrical overstress event is helpful. 図 6-9 shows an illustration of the ESD circuits contained in the TLV930x-Q1 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device or the power-supply ESD cell, internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

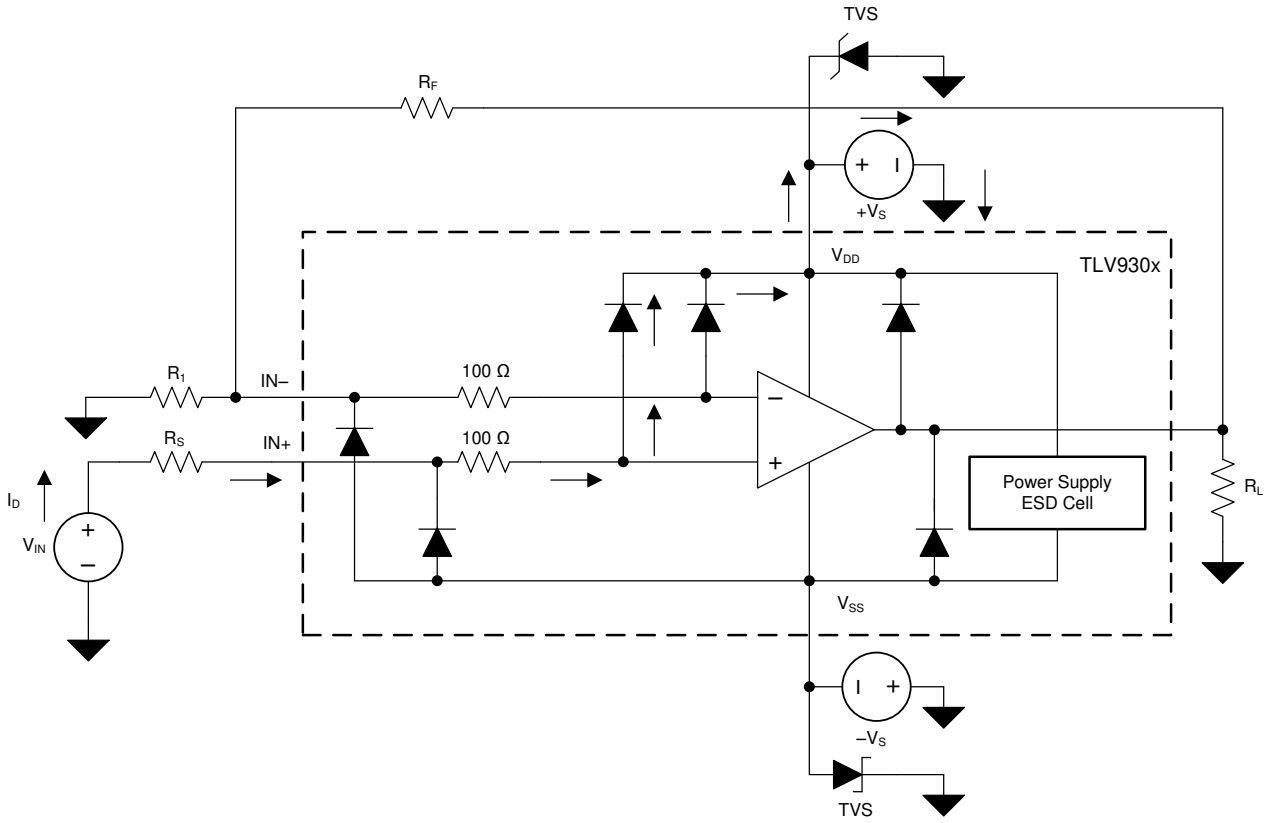


図 6-9. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event is very short in duration and very high voltage (for example, 1kV, 100ns), whereas an EOS event is long duration and lower voltage (for example, 50V, 100ms). The ESD diodes are designed for out-of-circuit ESD protection (that is, during assembly, test, and storage of the device before being soldered to the PCB). During an ESD event, the ESD signal is passed through the ESD steering diodes to an absorption circuit (labeled ESD power-supply circuit). The ESD absorption circuit clamps the supplies to a safe level.

Although this behavior is necessary for out-of-circuit protection, excessive current and damage is caused if activated in-circuit. Designers can use transient voltage suppressors (TVS) to prevent the device against damage caused by turning on the ESD absorption circuit during an in-circuit ESD event.

Make sure to use the appropriate current limiting resistors and TVS diodes to use the device ESD diodes and protect the device against EOS events.

6.3.8 Overload Recovery

Overload recovery is defined as the time required for the op amp output to recover from a saturated state to a linear state. The output devices of the op amp enter a saturation region when the output voltage exceeds the rated operating voltage, either due to the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the TLV930x-Q1 is approximately 1µs.

6.3.9 Typical Specifications and Distributions

Designers often ask about a typical specification of an amplifier when trying to design a more robust circuit. Due to natural variation in process technology and manufacturing procedures, every specification of an amplifier exhibits some amount of deviation from the ideal value, like the input offset voltage of an amplifier. These deviations often follow *Gaussian* ("bell curve"), or *normal* distributions, and circuit designers can leverage this information to guardband their system, even when there is not a minimum or maximum specification in *Electrical Characteristics*.

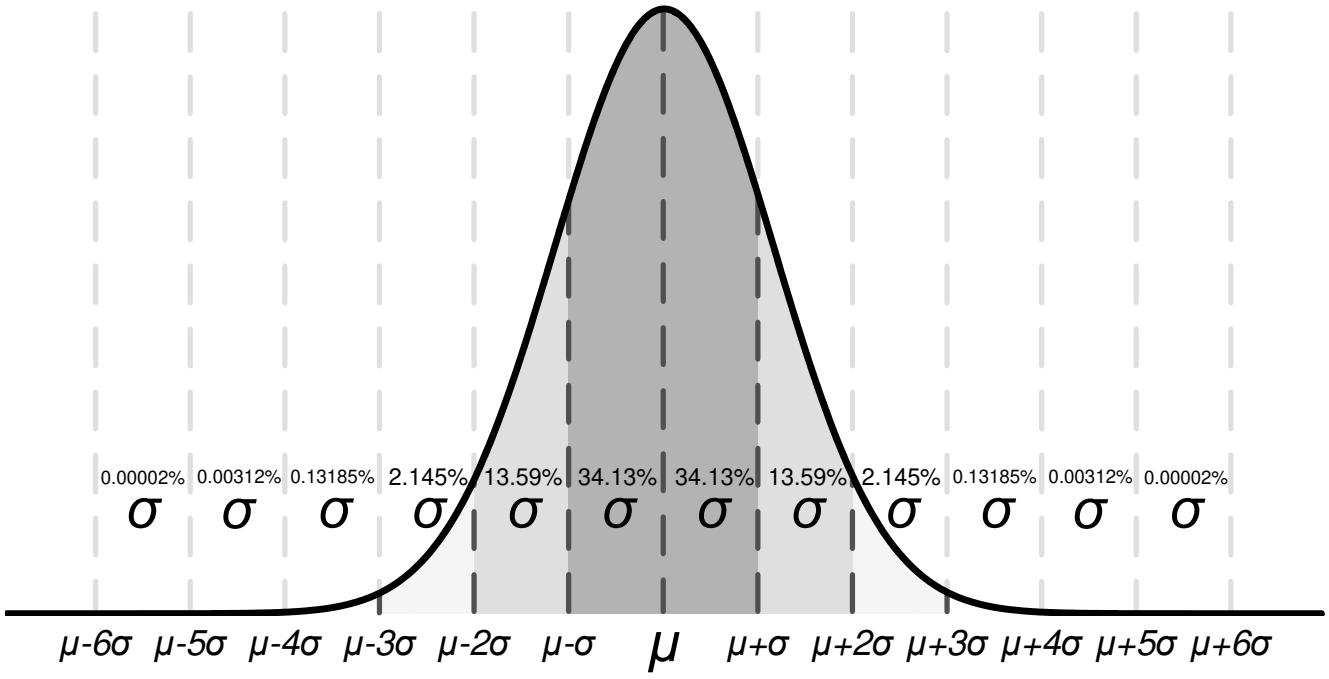


図 6-10. Ideal Gaussian Distribution

図 6-10 shows an example distribution, where *μ*, or *mu*, is the mean of the distribution, and where *σ*, or *sigma*, is the standard deviation of a system. For a specification that exhibits this kind of distribution, approximately two-thirds (68.26%) of all units can be expected to have a value within one standard deviation, or one sigma, of the mean (from *μ–σ* to *μ+σ*).

Depending on the specification, values listed in the *typical* column in *Electrical Characteristics* are represented in different ways. As a general rule, if a specification naturally has a nonzero mean (for example, like gain bandwidth), then the typical value is equal to the mean (μ). However, if a specification naturally has a mean near zero (like input offset voltage), then the typical value is equal to the mean plus one standard deviation (μ + σ) to more accurately represent the typical value.

Use this chart to calculate approximate probability of a specification in a unit; for example, the typical input voltage offset for the TLV930x- Q1 is 500µV, so 68.2% of all TLV930x-Q1 devices are expected to have an offset from –500µV to +500µV. At 4σ (±2000µV), 99.9937% of the distribution has an offset voltage less than ±2000µV, which means 0.0063% of the population is outside of these limits, which corresponds to about 1 in 15,873 units.

If specifications have a value listed in the minimum or maximum columns, make sure your design specifications are not outside of these ranges.

For specifications with no value listed in the minimum or maximum column, consider selecting a sigma value of sufficient guardband for your application, and design worst-case conditions using this value. For example, the 6σ value corresponds to about 1 in 500 million units, which is an extremely unlikely chance, and can be an option as a wide guardband to design a system around. The TLV930x-Q1 family does not have a maximum or minimum for offset voltage drift in this case, but based on 図 5-2 and the typical value of 2µV/°C in *Electrical Characteristics*, calculations show that the 6σ value for offset voltage drift is about 12µV/°C. When designing for worst-case system conditions, this value can be used to estimate the worst possible offset across temperature without having an actual minimum or maximum value.

However, process variation and adjustments over time can shift typical means and standard deviations, therefore only use this information to estimate the performance of a device if no minimum or maximum values are listed.

6.4 Device Functional Modes

The TLV930x-Q1 has a single functional mode and is operational when the power-supply voltage is greater than 4.5V (±2.25V). The maximum power supply voltage for the TLV930x-Q1 is 40V (±20V).

7 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TLV930x-Q1 family offers excellent DC precision and DC performance. These devices operate up to 40V supply rails and offer true rail-to-rail input/output, low offset voltage and offset voltage drift, as well as 1MHz bandwidth and high output drive. These features make the TLV930x-Q1 a robust, high-performance operational amplifier for high-voltage industrial applications.

7.2 Typical Applications

7.2.1 High Voltage Precision Comparator

Many different systems require controlled voltages across numerous system nodes to ensure robust operation. A comparator can be used to monitor and control voltages by comparing a reference threshold voltage with an input voltage and providing an output when the input crosses this threshold.

The MUX-friendly input stage of TLV930x-Q1 op amp family allow designers to use these devices as high voltage comparators (see *Input Protection Circuitry*). Previous generation high-voltage op amps often use back-to-back diodes across the inputs to prevent damage to the op amp, which greatly limited a designer's capability to use these op amps as comparators. The patented input stage of the TLV930x-Q1, however, allows the device to have a wide differential voltage between the inputs.

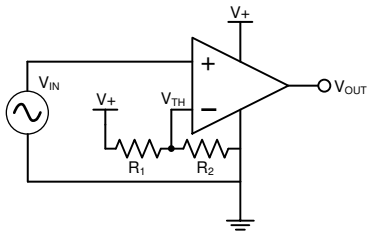


図 7-1. Typical Comparator Application

7.2.1.1 Design Requirements

The primary objective is to design a 40V precision comparator.

- System supply voltage (V+): 40V
- Resistor 1 value: 100kΩ
- Resistor 2 value: 100kΩ
- Reference threshold voltage (V_{TH}): 20V
- Input voltage range (V_{IN}): 0V – 40V
- Output voltage range (V_{OUT}): 0V – 40V

7.2.1.2 Detailed Design Procedure

This noninverting comparator circuit applies the input voltage (V_{IN}) to the noninverting terminal of the op amp. Two resistors (R_1 and R_2) divide the supply voltage (V+) to create a mid-supply threshold voltage (V_{TH}) as calculated in 式 1. 図 7-1 shows the circuit. When V_{IN} is less then V_{TH}, the output voltage transitions to the negative supply and equals the low-level output voltage. When V_{IN} is greater than V_{TH}, the output voltage transitions to the positive supply and equals the high-level output voltage.

In this example, resistor 1 and 2 reach 100kΩ, which sets the reference threshold at 20V. However, resistor 1 and 2 can be adjusted to modify the threshold using 式 1. The values of resistors 1 and 2 were selected to reduce power consumption, but these values can be further increased to reduce power consumption, or reduced to improve noise performance.

$$V_{TH} = \frac{R_2}{R_1 + R_2} \times V_+ \tag{1}$$

7.2.1.3 Application Curve

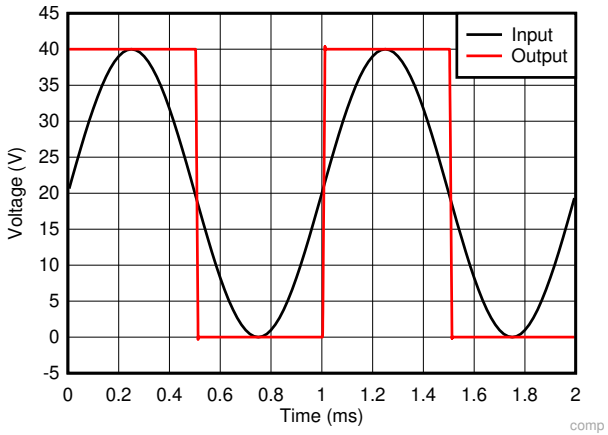


図 7-2. Comparator Output Response to Input Voltage

7.3 Power Supply Recommendations

The TLV930x-Q1 is specified for operation from 4.5V to 40V (±2.25V to ±20V); many specifications apply from –40°C to 125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in *Electrical Characteristics*.

> **注意**
>
> Supply voltages larger than 40V can permanently damage the device; see the *Absolute Maximum Ratings* table.

Place 0.1µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to *Layout*.

7.4 Layout

7.4.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself, therefore use bypass capacitors to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.

  - Connect low-ESR, 0.1µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry for one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in 図 7-4, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Clean the PCB following the board assembly for best performance.
- Any precision integrated circuit can experience performance shifts due to moisture ingress into the plastic package, therefore bake the PCB assembly after any aqueous PCB cleaning process to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

7.4.2 Layout Example

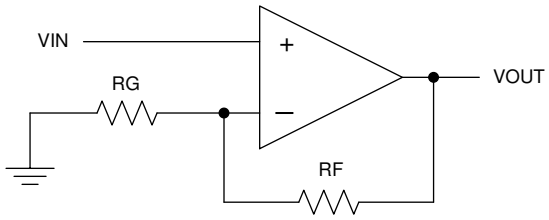


図 7-3. Schematic Representation

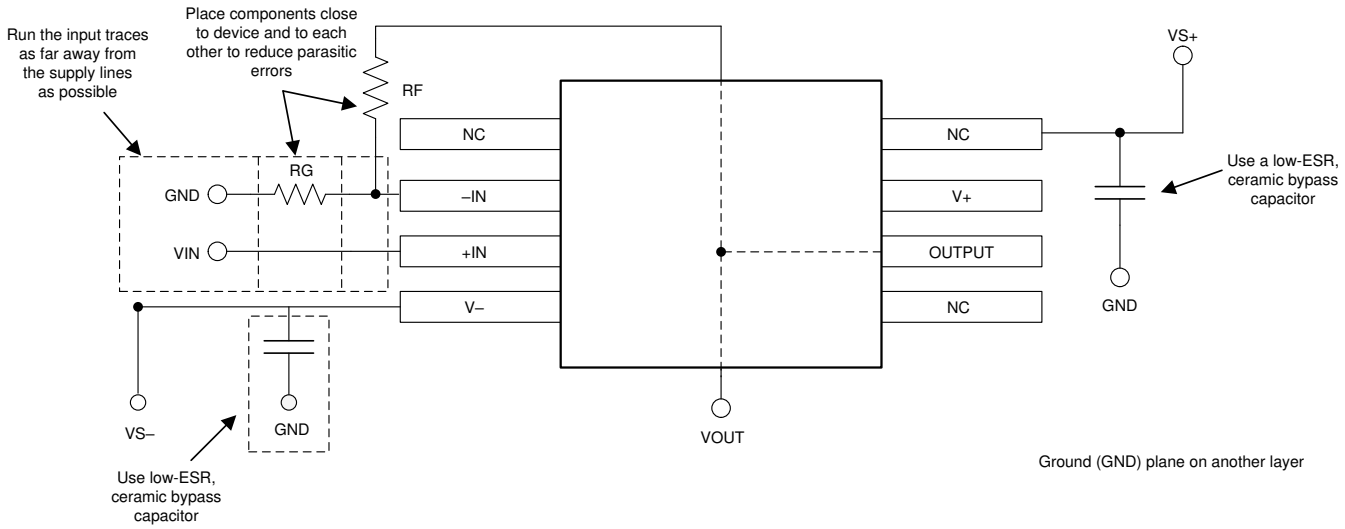


図 7-4. Operational Amplifier Board Layout for Noninverting Configuration

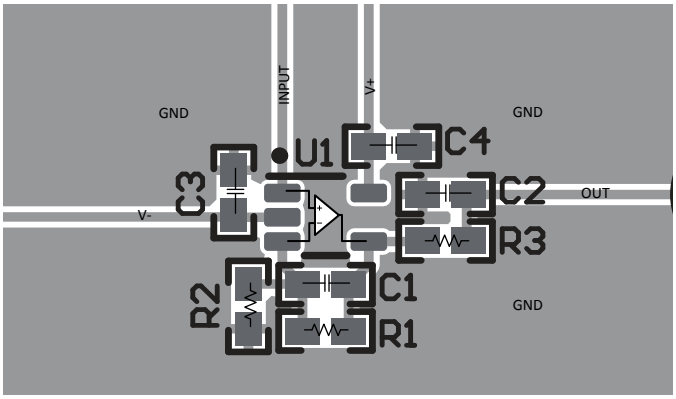


図 7-5. Example Layout for SC70 (DCK) Package

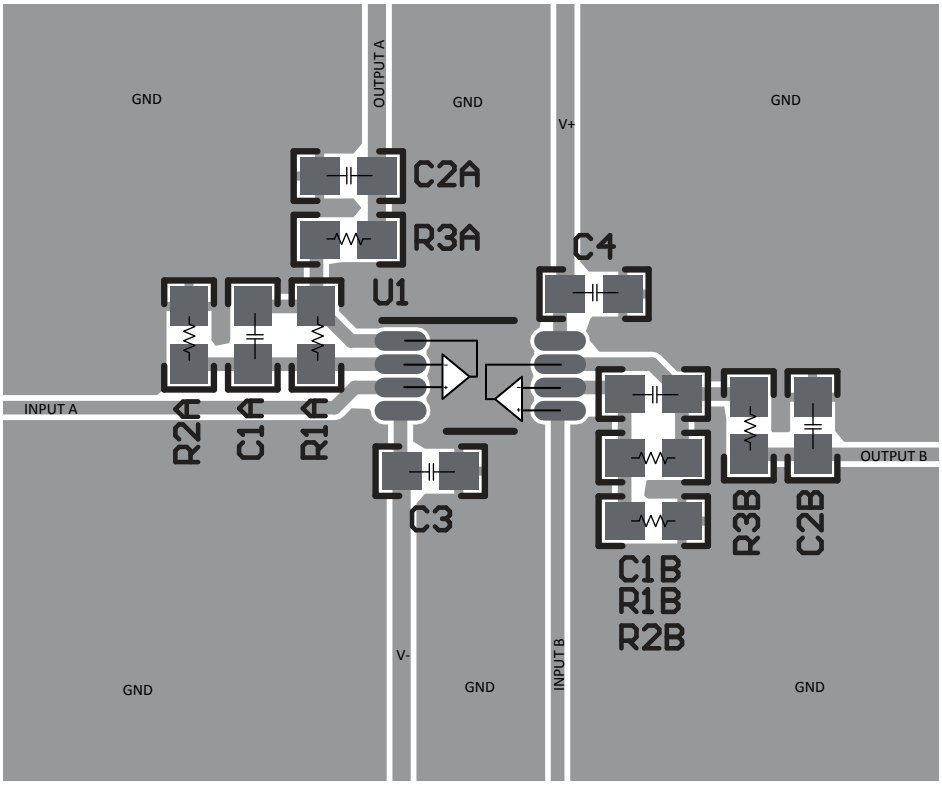


図 7-6. Example Layout for VSSOP-8 (DGK) Package

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

注

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

8.2 Documentation Support

8.2.1 Related Documentation

Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers* application note

Texas Instruments, *Capacitive Load Drive Solution using an Isolation Resistor* reference design

8.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.4 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

8.5 Trademarks

TINA-TI™ is a trademark of Texas Instruments, Inc and DesignSoft, Inc.
TINA™ and DesignSoft™ are trademarks of DesignSoft, Inc.
テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.
Bluetooth® is a registered trademark of Bluetooth SIG, Inc.
すべての商標は、それぞれの所有者に帰属します。

8.6 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.7 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
June 2024	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、テキサス・インスツルメンツの販売条件、または ti.com やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用されるテキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV9304QPWRQ1	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9304PW
TLV9304QPWRQ1.A	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9304PW

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TLV9304-Q1 :

- Catalog : TLV9304

NOTE: Qualified Version Definitions:

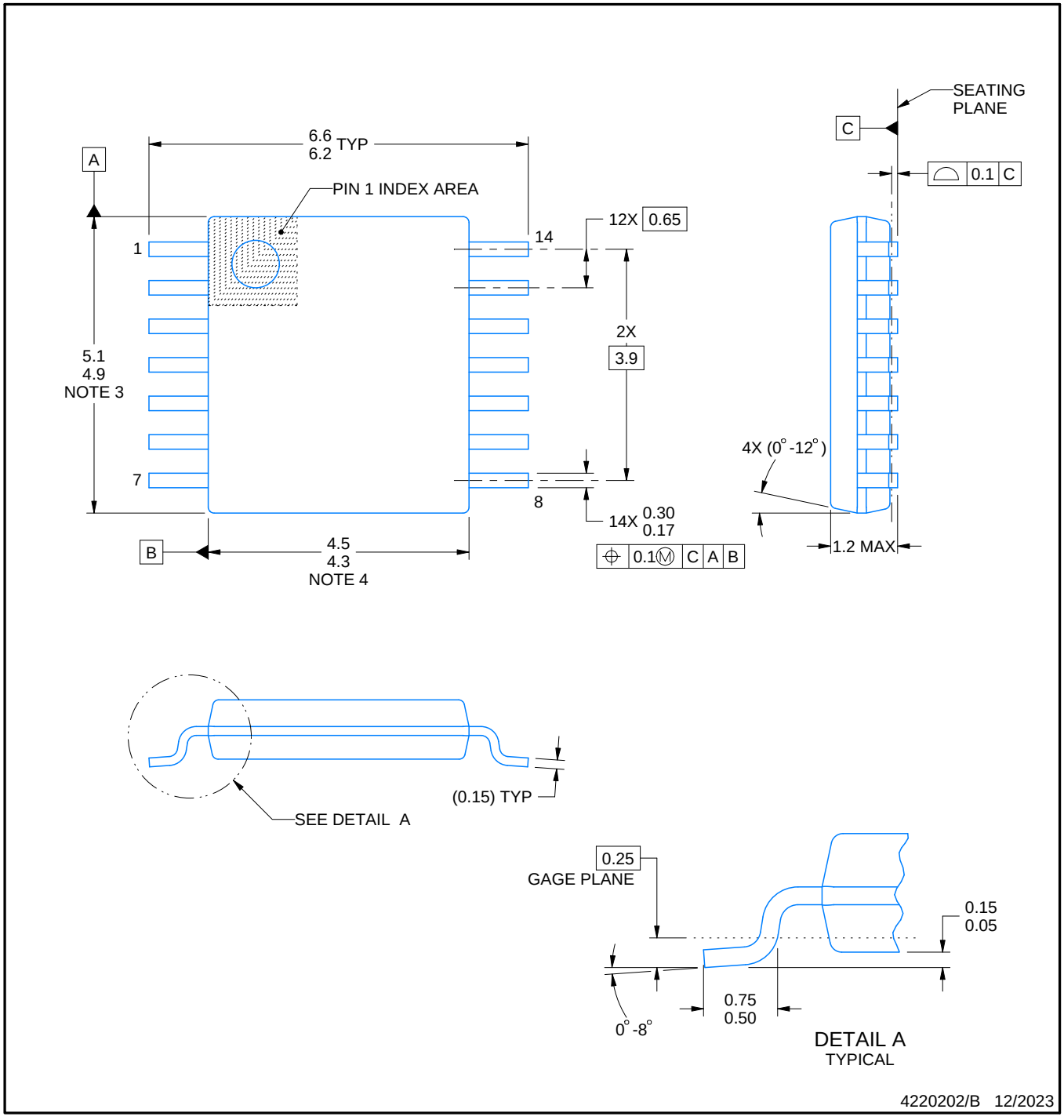
- Catalog - TI's standard catalog product

PACKAGE OUTLINE

PW0014A

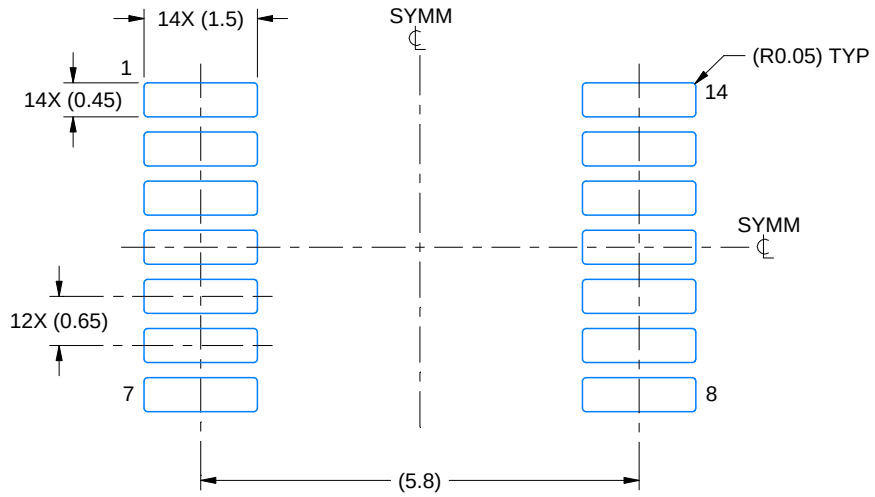
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

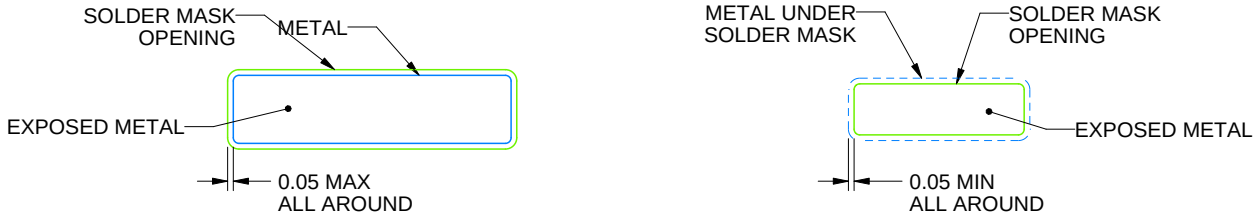


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

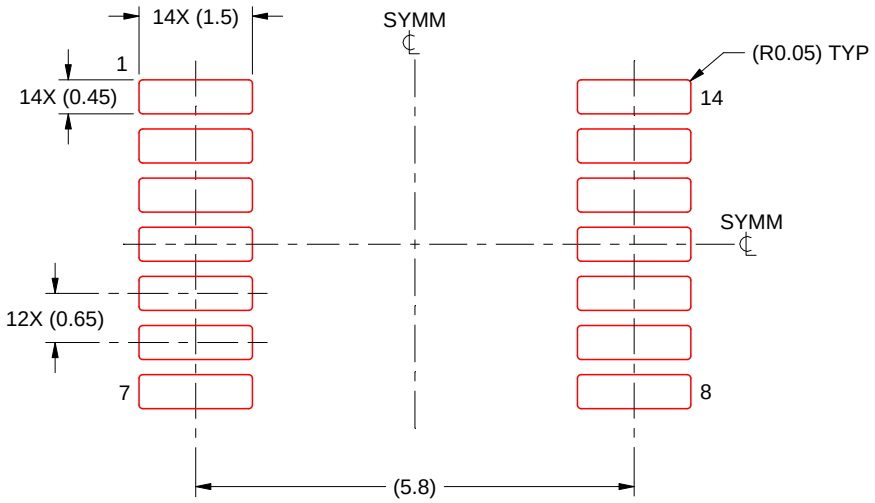


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、 テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、 テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。 テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、 テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、 テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、 テキサス・インスツルメンツの販売条件、または ti.com やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。 テキサス・インスツルメンツがこれらのリソースを提供することは、適用される テキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、 テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265