

TLV916x-Q1 車載用 16V、11MHz、レール ツー レール I/O、低オフセット電圧、低ノイズ車載オペアンプ

1 特長

- 車載アプリケーション向けに AEC-Q100 認証済み
 - 温度グレード 1: -40°C ~ +125°C, T_A
 - デバイス HBM ESD 分類レベル 3A (≥2500V)
 - デバイス CDM ESD 分類レベル C3 (≥1500V)
- 低いオフセット電圧: ±210μV
- 低いオフセット電圧ドリフト: ±0.25μV/°C
- 低ノイズ: 1kHz で 6.8nV/√Hz、広帯域で 4.2nV/√Hz
- 大きい同相除去: 110dB
- 低いバイアス電流: ±10pA
- レール ツー レール 入出力
- 広い帯域幅: 11MHz GBW、ユニティ ゲイン で安定
- 高いスルーレート: 33V/μs
- 低い静止電流: アンプ 1 個あたり 2.4mA
- 広い電源範囲: ±1.35V ~ ±8V、2.7V ~ 16V
- 堅牢な EMIRR 性能

2 アプリケーション

- AEC-Q100 グレード 1 アプリケーションに最適化
- インフォテインメントおよびクラスタ
- パッシブ型安全運転支援システム
- 車体エレクトロニクスおよび照明
- HEV/EV のインバータおよびモータ制御
- オンボード充電器 (OBC) およびワイヤレス充電器
- パワートレイン電流センサ
- 先進運転支援システム (ADAS)
- ハイサイドおよびローサイド電流検出

3 概要

TLV916x-Q1 ファミリー (TLV9161-Q1、TLV9162-Q1、TLV9164-Q1) は、車載用 16V 汎用オペアンプ ファミリーです。これらのデバイスは、レール ツー レール入出力、低オフセット (±210μV、標準値)、低オフセット ドリフト (±0.25μV/°C、標準値)、低ノイズ (1kHz 時に 6.8nV/√Hz、10kHz 時に 4.2nV/√Hz) など、卓越した DC 精度と AC 性能を備えています。

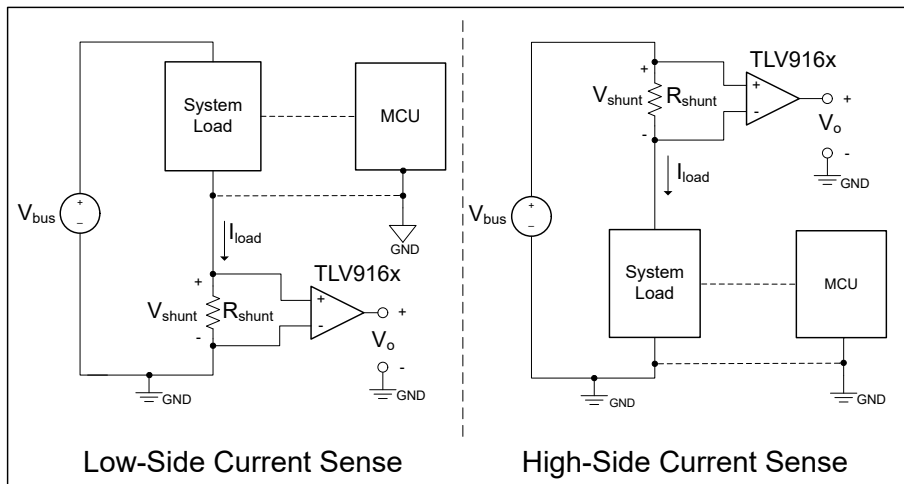
広い差動入力電圧範囲、大きい短絡電流 (±73mA)、大きいスルーレート (33V/μs) などの特長を備えた TLV916x-Q1 は、車載アプリケーションに適した柔軟で堅牢な高性能オペアンプです。

TLV916x-Q1 ファミリーのオペアンプは標準パッケージで供給され、-40°C ~ 125°C で動作が規定されています。

パッケージ情報

部品番号 ⁽¹⁾	チャネル数	パッケージ	パッケージサイズ ⁽²⁾
TLV9161-Q1	シングル	DBV (SOT-23, 5)	2.9mm × 2.8mm
		DCK (SC70, 5)	2mm × 2.1mm
TLV9162-Q1	デュアル	D (SOIC, 8)	4.9mm × 6mm
		DGK (VSSOP, 8)	3mm × 4.9mm
		PW (TSSOP, 8)	3mm × 6.4mm
TLV9164-Q1	クワッド	D (SOIC, 14)	8.65mm × 6mm
		PW (TSSOP, 14)	5mm × 6.4mm

- 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
- パッケージサイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



TLV916x-Q1 を使用した電流検出アプリケーション



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4 Pin Configuration and Functions

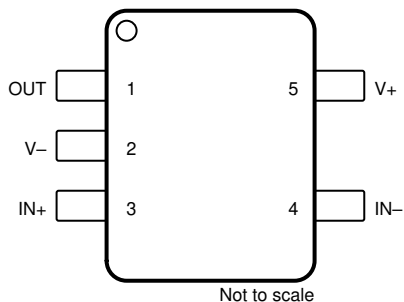


図 4-1. TLV9161-Q1 DBV Package,
5-Pin SOT-23
(Top View)

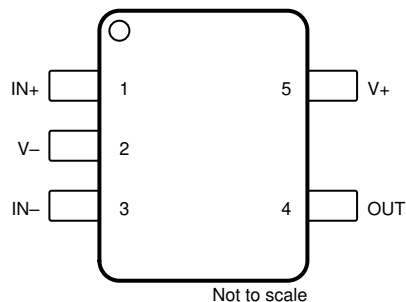


図 4-2. TLV9161-Q1 DCK Package,
5-Pin SC70
(Top View)

表 4-1. Pin Functions: TLV9161-Q1

NAME	PIN		TYPE ⁽¹⁾	DESCRIPTION
	SOT-23 (DBV)	SC70 (DCK)		
IN+	3	1	I	Noninverting input
IN–	4	3	I	Inverting input
OUT	1	4	O	Output
V+	5	5	—	Positive (highest) power supply
V–	2	2	—	Negative (lowest) power supply

(1) I = input, O = output

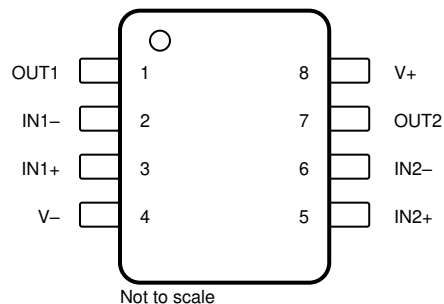
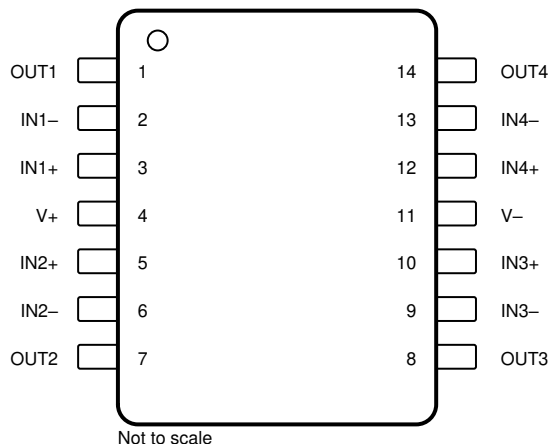


図 4-3. TLV9162-Q1 D, PW, and DGK Package,
8-Pin SOIC, TSSOP, and VSSOP
(Top View)

表 4-2. Pin Functions: TLV9162-Q1

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
IN1+	3	I	Noninverting input, channel 1
IN1–	2	I	Inverting input, channel 1
IN2+	5	I	Noninverting input, channel 2
IN2–	6	I	Inverting input, channel 2
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
V+	8	—	Positive (highest) power supply
V–	4	—	Negative (lowest) power supply

(1) I = input, O = output



**図 4-4. TLV9164-Q1 D and PW Package,
14-Pin SOIC and TSSOP
(Top View)**

表 4-3. Pin Functions: TLV9164-Q1

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
IN1+	3	I	Noninverting input, channel 1
IN1–	2	I	Inverting input, channel 1
IN2+	5	I	Noninverting input, channel 2
IN2–	6	I	Inverting input, channel 2
IN3+	10	I	Noninverting input, channel 3
IN3–	9	I	Inverting input, channel 3
IN4+	12	I	Noninverting input, channel 4
IN4–	13	I	Inverting input, channel 4
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
OUT3	8	O	Output, channel 3
OUT4	14	O	Output, channel 4
V+	4	—	Positive (highest) power supply
V–	11	—	Negative (lowest) power supply

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Supply voltage, $V_S = (V+) - (V-)$		0	20	V
Signal input pins	Common-mode voltage ⁽³⁾	$(V-) - 0.5$	$(V+) + 0.5$	V
	Differential voltage ⁽³⁾		$V_S + 0.2$	V
	Current ⁽³⁾	-10	10	mA
Shutdown pin voltage		$V-$	$V+$	
Output short-circuit ⁽²⁾		Continuous		
Operating ambient temperature, T_A		-55	150	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		-65	150	°C

- (1) Operating the device beyond the ratings listed under *Absolute Maximum Ratings* will cause permanent damage to the device. These are stress ratings only, based on process and design limitations, and this device has not been designed to function outside the conditions indicated under *Recommended Operating Conditions*. Exposure to any condition outside *Recommended Operating Conditions* for extended periods, including absolute-maximum-rated conditions, may affect device reliability and performance.
- (2) Short-circuit to ground, one amplifier per package. Extended short-circuit current, especially with higher supply voltage, can cause excessive heating and eventual destruction.
- (3) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5V beyond the supply rails must be current limited to 10mA or less.

5.2 ESD Ratings

			VALUE	UNIT
TLV9161-Q1				
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	±1500	
TLV9162-Q1 and TLV9164-Q1				
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2500	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	±1500	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage, $(V+) - (V-)$	2.7	16	V
V_I	Common mode voltage range	$V-$	$V+$	V
T_A	Specified temperature	-40	125	°C

5.4 Thermal Information for Single Channel

THERMAL METRIC ⁽¹⁾		TLV9161-Q1		UNIT
		DBV (SOT-23)	DCK (SC70)	
		5 PINS	5 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	189.3	202.4	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	86.8	111.6	°C/W
R _{θJB}	Junction-to-board thermal resistance	55.9	51.6	°C/W
ψ _{JT}	Junction-to-top characterization parameter	23.6	25.8	°C/W
ψ _{JB}	Junction-to-board characterization parameter	55.5	51.4	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

5.5 Thermal Information for Dual Channel

THERMAL METRIC ⁽¹⁾		TLV9162-Q1			Unit
		D (SOIC)	PW (TSSOP)	DGK (VSSOP)	
		8 PINS	8 PINS	8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	130.8	159.1	173.9	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	74.0	67.9	65.7	°C/W
R _{θJB}	Junction-to-board thermal resistance	74.3	98.1	95.6	°C/W
ψ _{JT}	Junction-to-top characterization parameter	25.8	9.1	10.9	°C/W
ψ _{JB}	Junction-to-board characterization parameter	73.5	96.7	94.1	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

5.6 Thermal Information for Quad Channel

THERMAL METRIC ⁽¹⁾		TLV9164-Q1		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	94.9	120.0	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	51.1	50.4	°C/W
R _{θJB}	Junction-to-board thermal resistance	51.4	63.1	°C/W
ψ _{JT}	Junction-to-top characterization parameter	15.3	8.1	°C/W
ψ _{JB}	Junction-to-board characterization parameter	51.0	62.5	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

5.7 Electrical Characteristics

For $V_S = (V+) - (V-) = 2.7V$ to $16V$ ($\pm 1.35V$ to $\pm 8V$) at $T_A = 25^\circ C$, $R_L = 10k\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V _{OS}	Input offset voltage	V _{CM} = V–		±0.21	±1.03	mV	
			T _A = –40°C to 125°C	±1.2			
dV _{OS} /dT	Input offset voltage drift	V _{CM} = V–	T _A = –40°C to 125°C	±0.25		μV/°C	
PSRR	Input offset voltage versus power supply	TLV9161-Q1, TLV9162-Q1, V _{CM} = V–, V _S = 5V to 16V		±0.45	±2	μV/V	
		TLV9161-Q1, TLV9162-Q1 D and DGK packages V _{CM} = V–, V _S = 5V to 16V	T _A = –40°C to 125°C	±0.45	±3		
		TLV9162-Q1 PW package V _{CM} = V–, V _S = 5V to 16V	T _A = –40°C to 125°C	±0.45	±3.8		
		TLV9164-Q1, V _{CM} = V–, V _S = 5V to 16V		±0.45	±2.2		
			T _A = –40°C to 125°C	±0.45	±3.8		
		TLV9161-Q1, TLV9162-Q1, TLV9164-Q1, V _{CM} = V–, V _S = 2.7V to 16V ⁽¹⁾	T _A = –40°C to 125°C	±2	±12		
	DC channel separation			0.4		μV/V	
INPUT BIAS CURRENT							
I _B	Input bias current			±10		pA	
I _{OS}	Input offset current			±10		pA	
NOISE							
E _N	Input voltage noise	f = 0.1Hz to 10Hz		2.7		μV _{PP}	
				0.49		μV _{RMS}	
e _N	Input voltage noise density	f = 1kHz		6.8		nV/√Hz	
		f = 10kHz		4.2			
i _N	Input current noise density	f = 1kHz		55		fA/√Hz	
INPUT VOLTAGE RANGE							
V _{CM}	Common-mode voltage range			(V–)	(V+)	V	
CMRR	Common-mode rejection ratio	V _S = 16V, V– < V _{CM} < (V+) – 2V (PMOS pair)	T _A = –40°C to 125°C	85	110	dB	
		V _S = 5V, V– < V _{CM} < (V+) – 2V (PMOS pair) ⁽¹⁾		75	98		
		V _S = 2.7V, V– < V _{CM} < (V+) – 2V (PMOS pair)		90			
		V _S = 2.7 – 16V, (V+) – 1V < V _{CM} < V+ (NMOS pair)		78			
		(V+) – 2V < V _{CM} < (V+) – 1V		See 5-6			
INPUT IMPEDANCE							
Z _{ID}	Differential			100 9		MΩ pF	
Z _{ICM}	Common-mode			6 1		TΩ pF	
OPEN-LOOP GAIN							
A _{OL}	Open-loop voltage gain	V _S = 16V, V _{CM} = V _S / 2, (V–) + 0.1V < V _O < (V+) – 0.1V		120	136	dB	
			T _A = –40°C to 125°C	136			
		V _S = 5V, V _{CM} = V _S / 2, (V–) + 0.1V < V _O < (V+) – 0.1V ⁽¹⁾		104	125		
			T _A = –40°C to 125°C	125			
		V _S = 2.7V, V _{CM} = V _S / 2, (V–) + 0.1V < V _O < (V+) – 0.1V ⁽¹⁾		90	105		
	T _A = –40°C to 125°C	105					

5.7 Electrical Characteristics (続き)

For $V_S = (V_+) - (V_-) = 2.7V$ to $16V$ ($\pm 1.35V$ to $\pm 8V$) at $T_A = 25^\circ C$, $R_L = 10k\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$, unless otherwise noted.

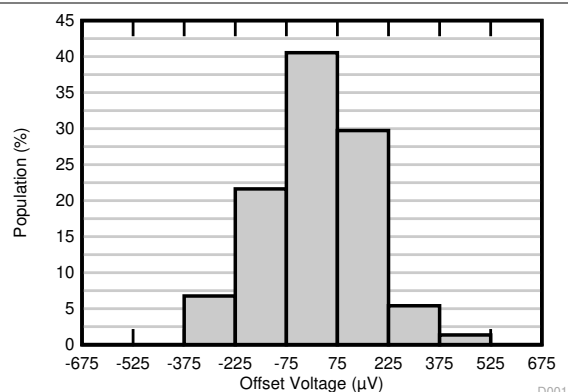
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product			11		MHz
SR	Slew rate	$V_S = 16V$, $G = +1$, $V_{STEP} = 10V$, $C_L = 20pF^{(2)}$		33		V/ μs
t_s	Settling time	To 0.1%, $V_S = 16V$, $V_{STEP} = 10V$, $G = +1$, $C_L = 20pF$		0.70		μs
		To 0.1%, $V_S = 16V$, $V_{STEP} = 2V$, $G = +1$, $C_L = 20pF$		0.22		
		To 0.01%, $V_S = 16V$, $V_{STEP} = 10V$, $G = +1$, $C_L = 20pF$		0.89		
		To 0.01%, $V_S = 16V$, $V_{STEP} = 2V$, $G = +1$, $C_L = 20pF$		0.42		
	Phase margin	$G = +1$, $R_L = 10k\Omega$, $C_L = 20pF$		64		°
	Overload recovery time	$V_{IN} \times \text{gain} > V_S$		120		ns
THD+N	Total harmonic distortion + noise	$V_S = 16V$, $V_O = 3V_{RMS}$, $G = 1$, $f = 1kHz$		0.00005%		
				126		dB
		$V_S = 10V$, $V_O = 3V_{RMS}$, $G = 1$, $f = 1kHz$, $R_L = 128\Omega$		0.0032%		
				90		dB
		$V_S = 10V$, $V_O = 0.4V_{RMS}$, $G = 1$, $f = 1kHz$, $R_L = 32\Omega$		0.00032%		
				110		dB
OUTPUT						
	Voltage output swing from rail	Positive and negative rail headroom	$V_S = 16V$, $R_L = \text{no load}$	6		mV
			$V_S = 16V$, $R_L = 10k\Omega$	25	60	
			$V_S = 16V$, $R_L = 2k\Omega$	85	300	
			$V_S = 2.7V$, $R_L = \text{no load}$	0.5		
			$V_S = 2.7V$, $R_L = 10k\Omega$	5	20	
			$V_S = 2.7V$, $R_L = 2k\Omega$	20	50	
I_{SC}	Short-circuit current			± 73		mA
C_{LOAD}	Capacitive load drive			See 5-33		pF
Z_O	Open-loop output impedance	$I_O = 0A$		See 5-30		Ω
POWER SUPPLY						
I_Q	Quiescent current per amplifier	TLV9162-Q1, TLV9164-Q1, $I_O = 0A$		2.4	2.8	mA
			$T_A = -40^\circ C$ to $125^\circ C$		2.84	
		TLV9161-Q1, $I_O = 0A$		2.48	2.92	
			$T_A = -40^\circ C$ to $125^\circ C$		2.98	

(1) Specified by characterization only.

(2) See [5-15](#) for more information.

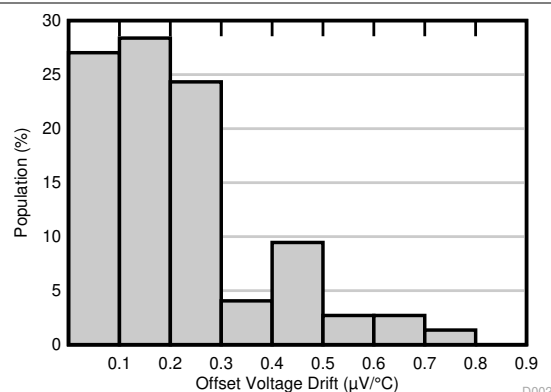
5.8 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $V_S = \pm 8\text{V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{k}\Omega$ (unless otherwise noted)



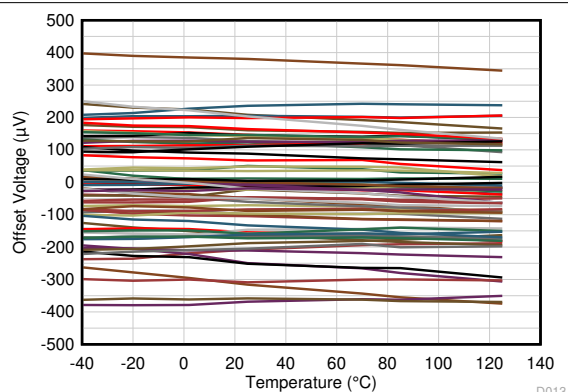
Distribution from 74 amplifiers, $T_A = 25^\circ\text{C}$

図 5-1. Offset Voltage Production Distribution



Distribution from 74 amplifiers

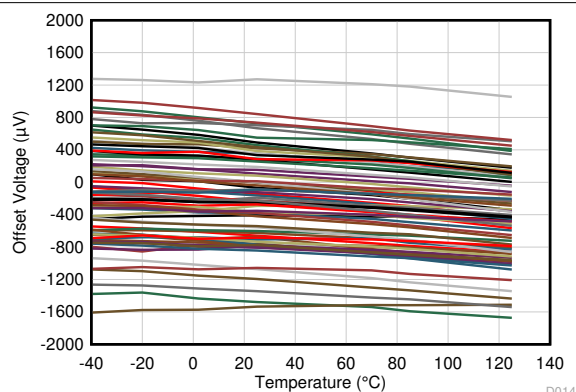
図 5-2. Offset Voltage Drift Distribution



$V_{CM} = V_-$

Data from 74 amplifiers

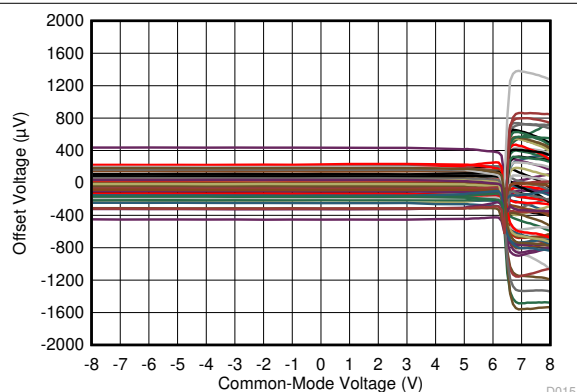
図 5-3. Offset Voltage vs Temperature



$V_{CM} = V_+$

Data from 74 amplifiers

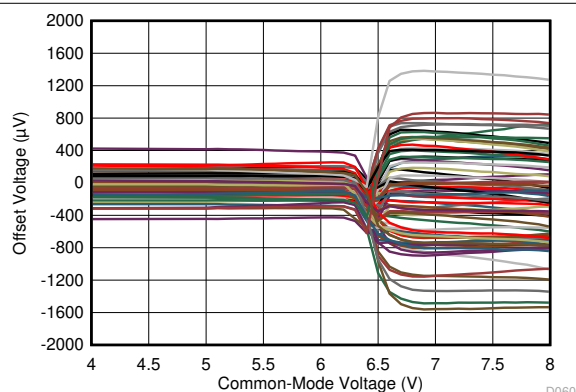
図 5-4. Offset Voltage vs Temperature



$T_A = 25^\circ\text{C}$

Data from 74 amplifiers

図 5-5. Offset Voltage vs Common-Mode Voltage



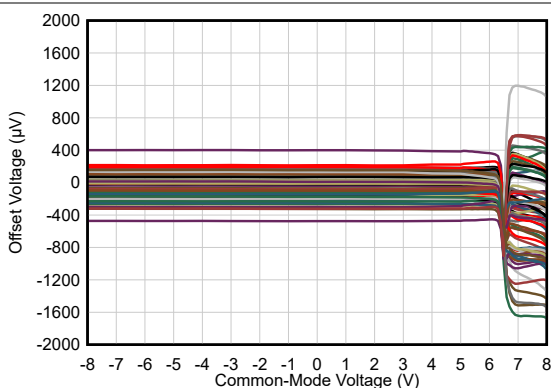
$T_A = 25^\circ\text{C}$

Data from 74 amplifiers

図 5-6. Offset Voltage vs Common-Mode Voltage (Transition Region)

5.8 Typical Characteristics (continued)

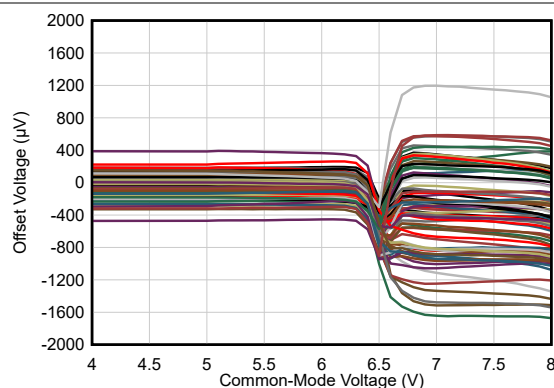
at $T_A = 25^\circ\text{C}$, $V_S = \pm 8\text{V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{k}\Omega$ (unless otherwise noted)



$T_A = 125^\circ\text{C}$

Data from 74 amplifiers

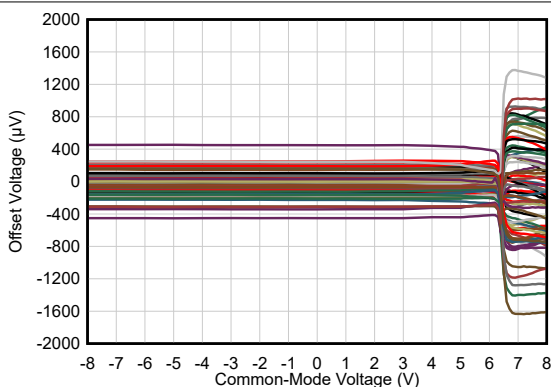
Figure 5-7. Offset Voltage vs Common-Mode Voltage



$T_A = 125^\circ\text{C}$

Data from 74 amplifiers

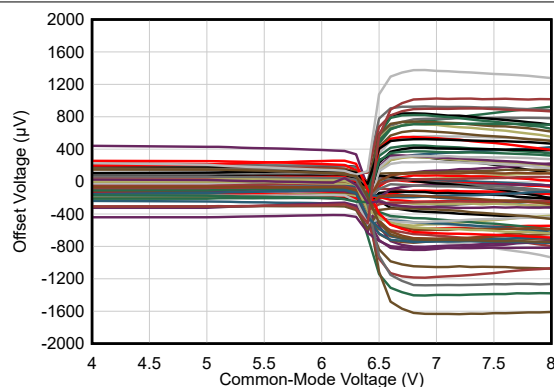
Figure 5-8. Offset Voltage vs Common-Mode Voltage (Transition Region)



$T_A = -40^\circ\text{C}$

Data from 74 amplifiers

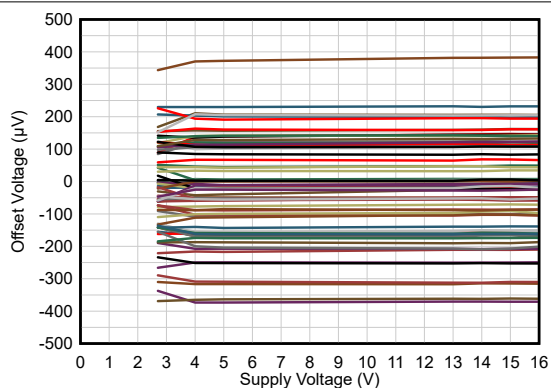
Figure 5-9. Offset Voltage vs Common-Mode Voltage



$T_A = -40^\circ\text{C}$

Data from 74 amplifiers

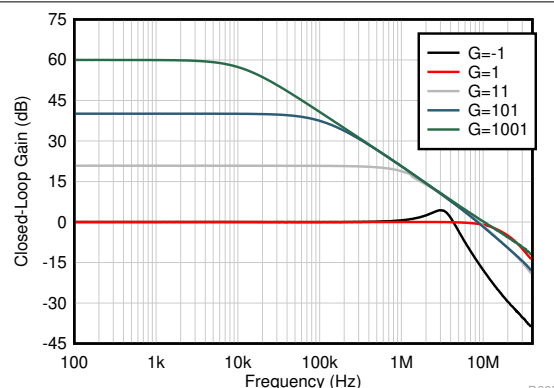
Figure 5-10. Offset Voltage vs Common-Mode Voltage (Transition Region)



$V_{CM} = V_-$

Data from 74 amplifiers

Figure 5-11. Offset Voltage vs Power Supply



D005

Figure 5-12. Closed-Loop Gain vs Frequency

5.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 8\text{V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{k}\Omega$ (unless otherwise noted)

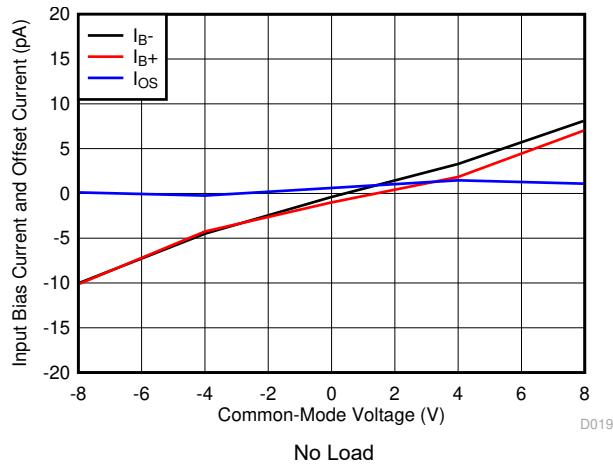


Figure 5-13. Input Bias Current and Offset Current vs Common-Mode Voltage

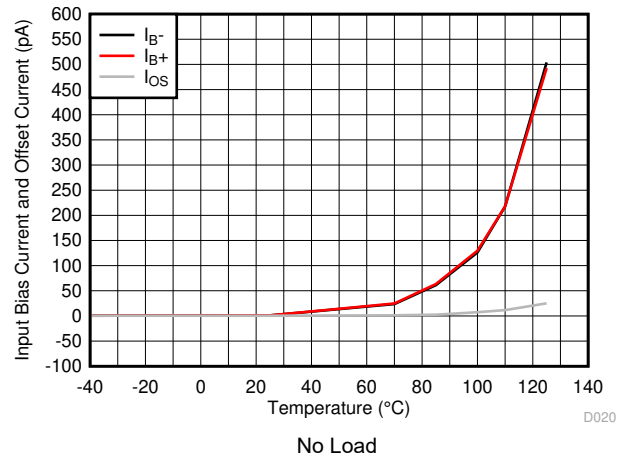


Figure 5-14. Input Bias Current and Offset Current vs Temperature

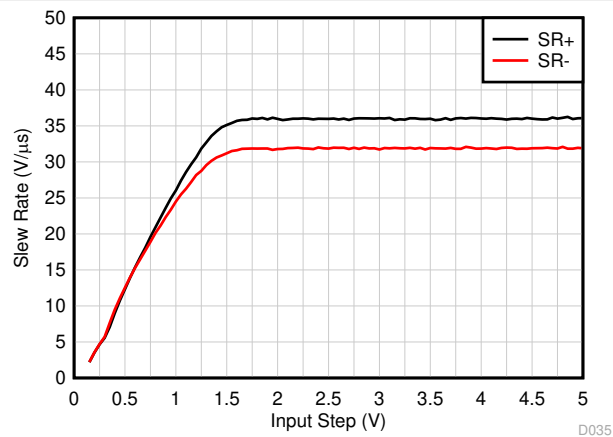


Figure 5-15. Slew Rate vs Input Step Voltage

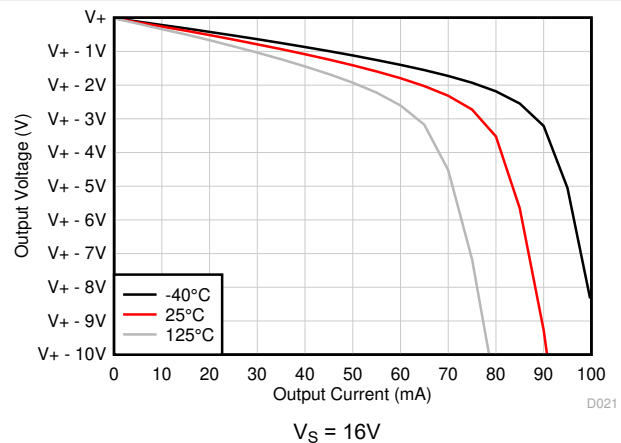


Figure 5-16. Output Voltage Swing vs Output Current (Sourcing)

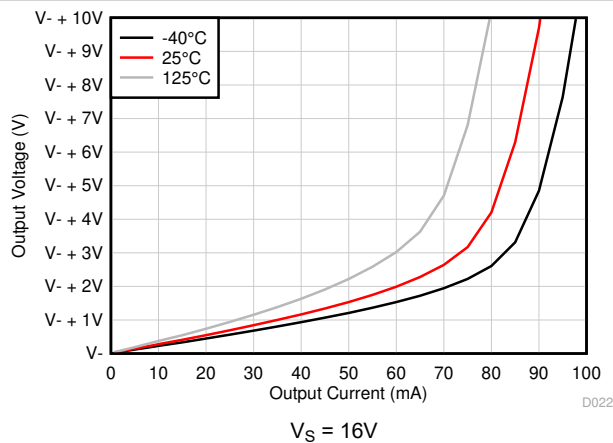


Figure 5-17. Output Voltage Swing vs Output Current (Sinking)

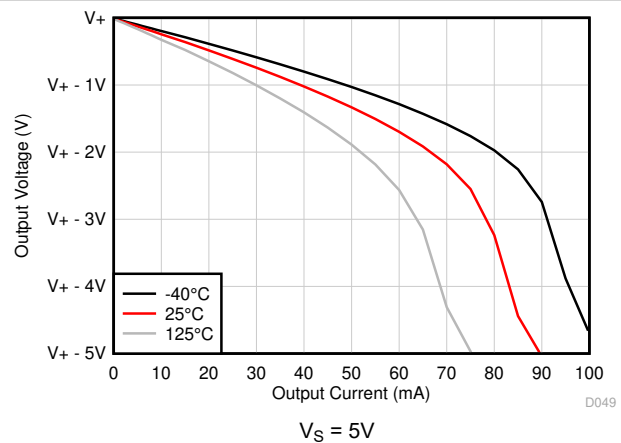


Figure 5-18. Output Voltage Swing vs Output Current (Sourcing)

5.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 8\text{V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{k}\Omega$ (unless otherwise noted)

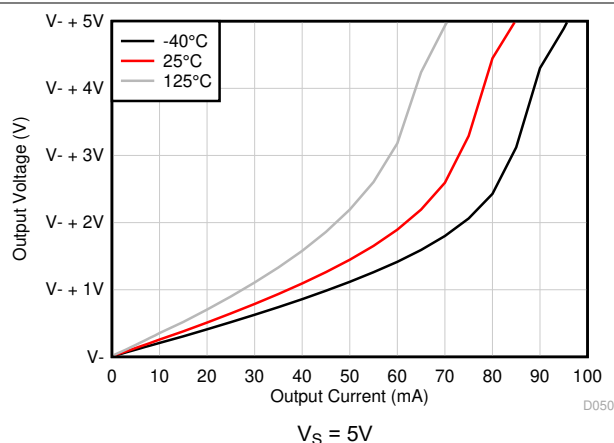


Figure 5-19. Output Voltage Swing vs Output Current (Sinking)

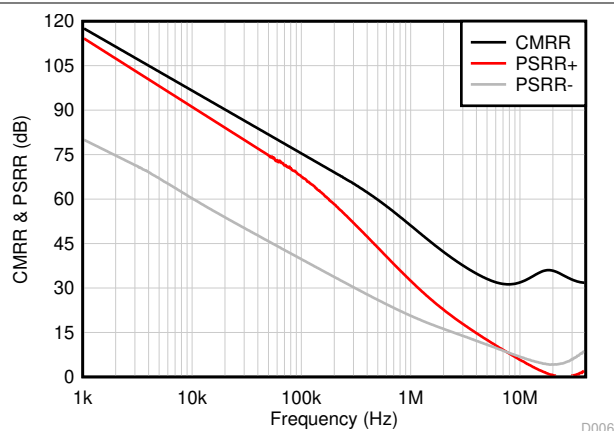


Figure 5-20. CMRR and PSRR vs Frequency

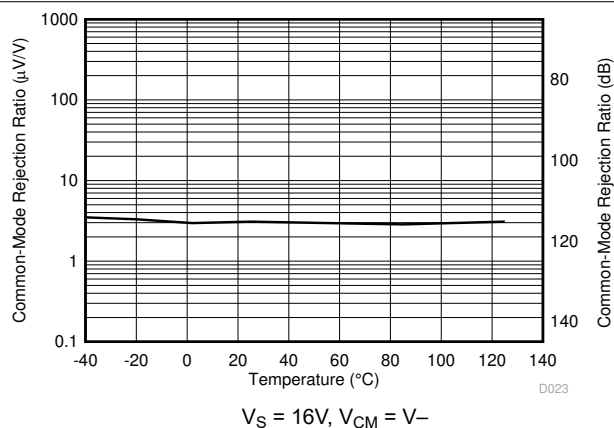


Figure 5-21. CMRR vs Temperature

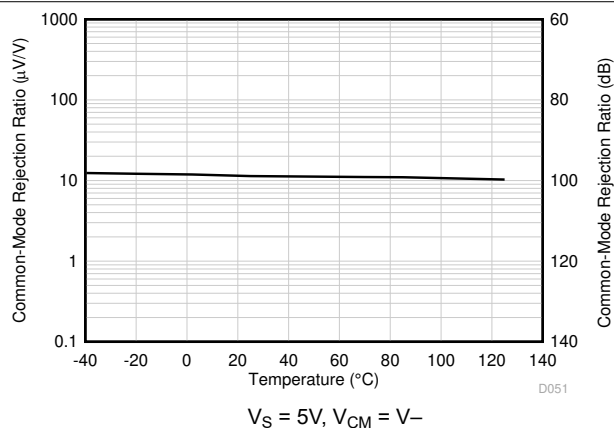


Figure 5-22. CMRR vs Temperature

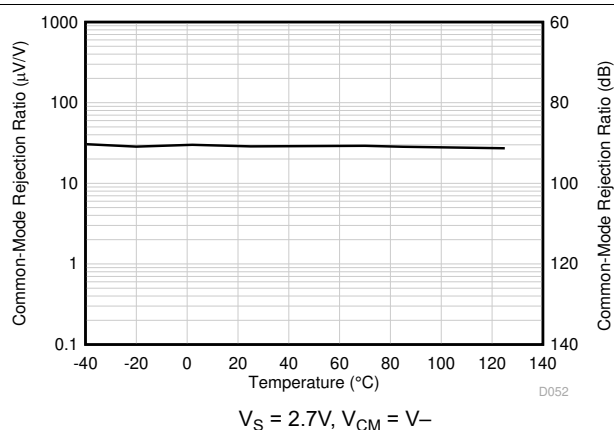


Figure 5-23. CMRR vs Temperature

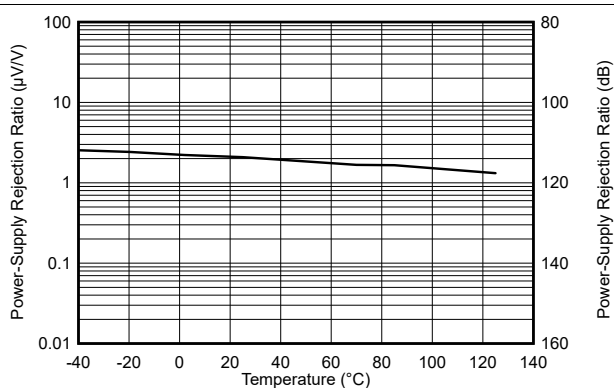


Figure 5-24. PSRR vs Temperature

5.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 8\text{V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{k}\Omega$ (unless otherwise noted)

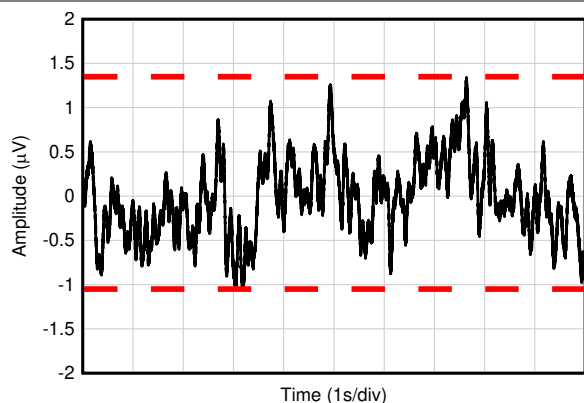


图 5-25. 0.1Hz to 10Hz Noise

D025

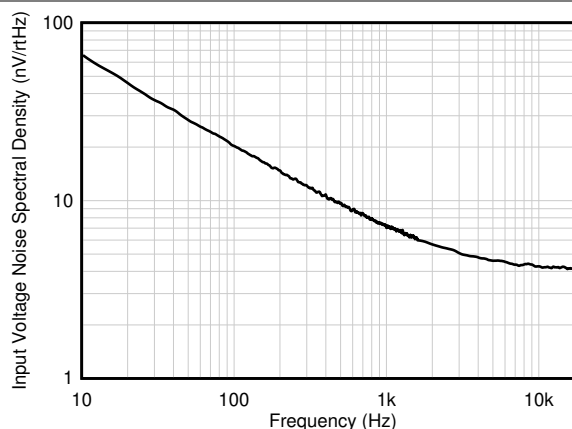


图 5-26. Input Voltage Noise Spectral Density vs Frequency

D007

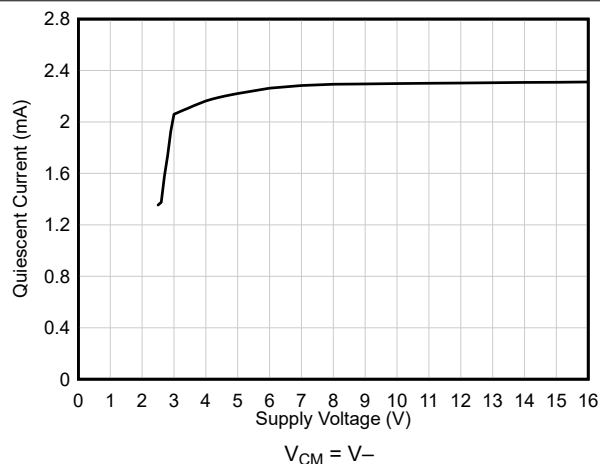


图 5-27. Quiescent Current vs Supply Voltage

$V_{CM} = V_-$

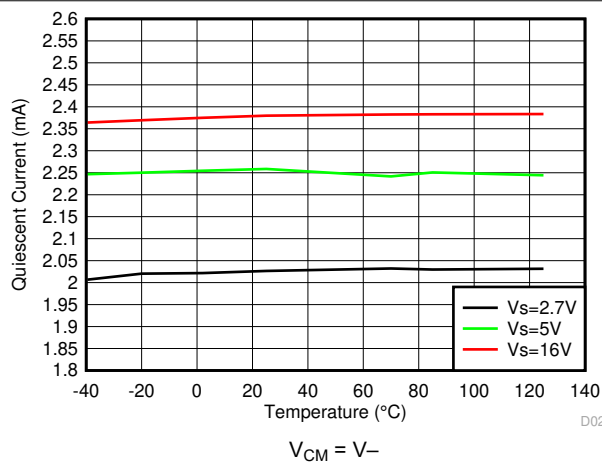


图 5-28. Quiescent Current vs Temperature

$V_{CM} = V_-$

D027

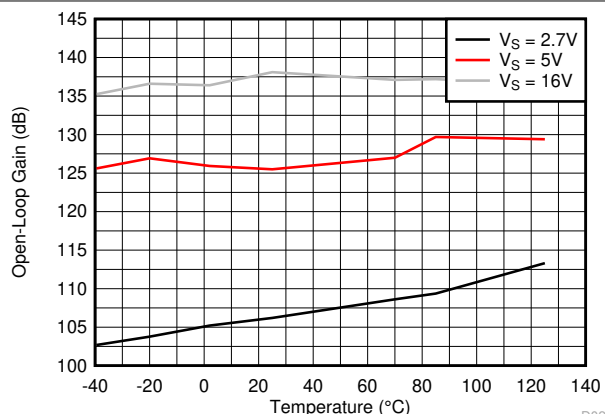


图 5-29. Open-Loop Voltage Gain vs Temperature (dB)

D028

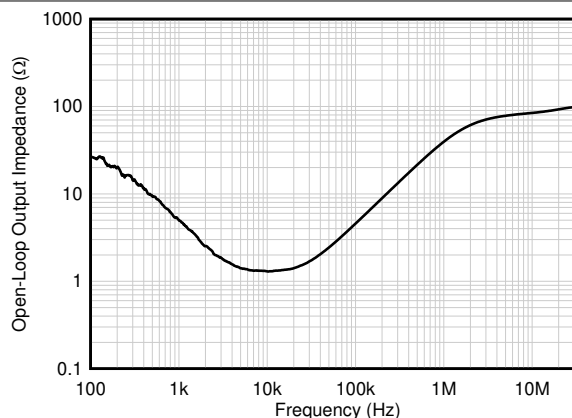


图 5-30. Open-Loop Output Impedance vs Frequency

D099

5.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 8\text{V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{k}\Omega$ (unless otherwise noted)

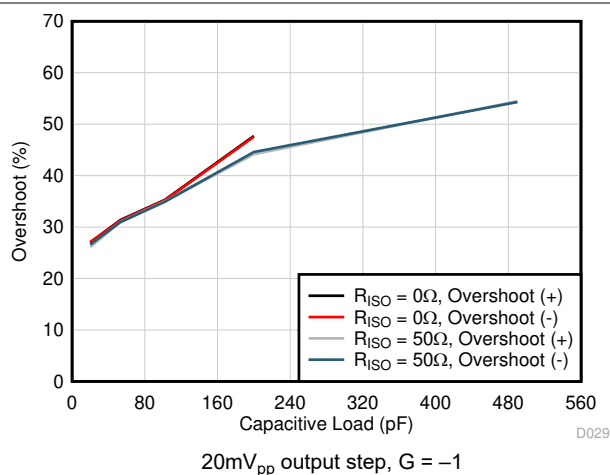


Figure 5-31. Small-Signal Overshoot vs Capacitive Load

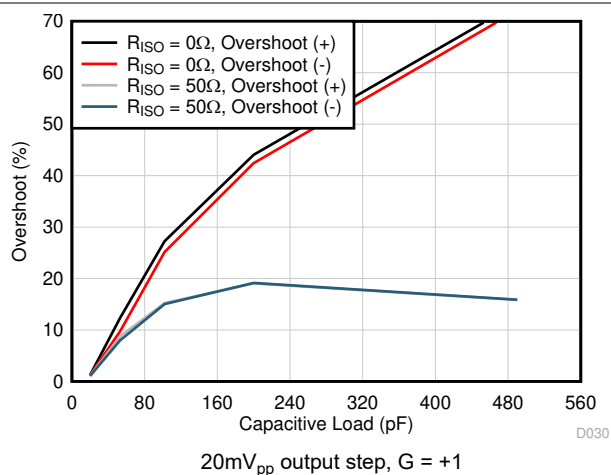


Figure 5-32. Small-Signal Overshoot vs Capacitive Load

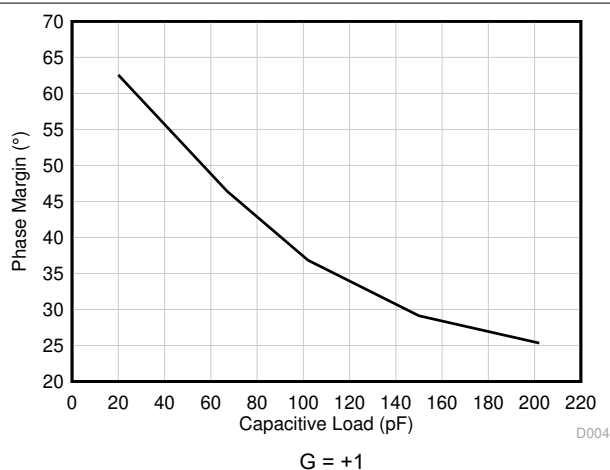


Figure 5-33. Phase Margin vs Capacitive Load

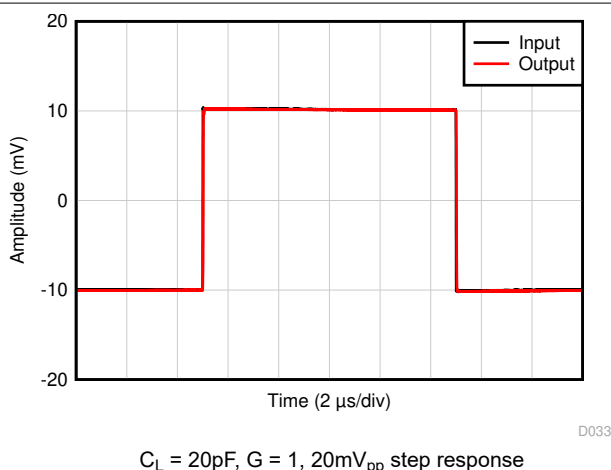


Figure 5-34. Small-Signal Step Response

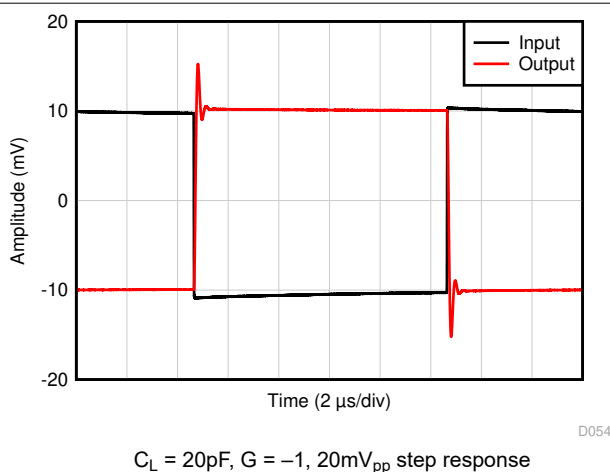


Figure 5-35. Small-Signal Step Response

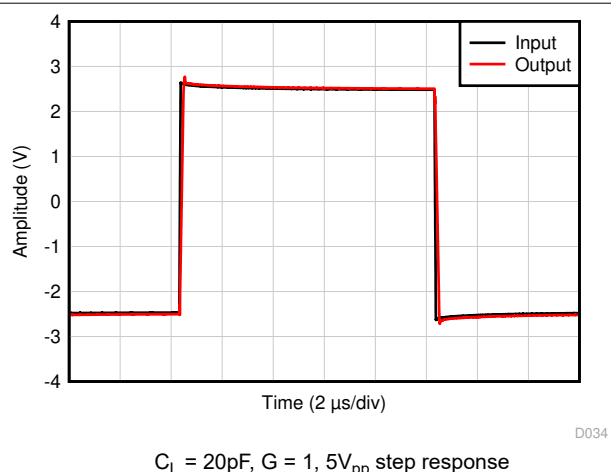
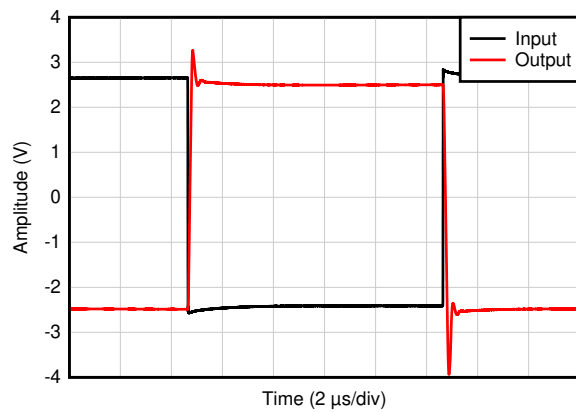


Figure 5-36. Large-Signal Step Response

5.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 8\text{V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{k}\Omega$ (unless otherwise noted)



$C_L = 20\text{pF}$, $G = -1$, $5V_{pp}$ step response

図 5-37. Large-Signal Step Response

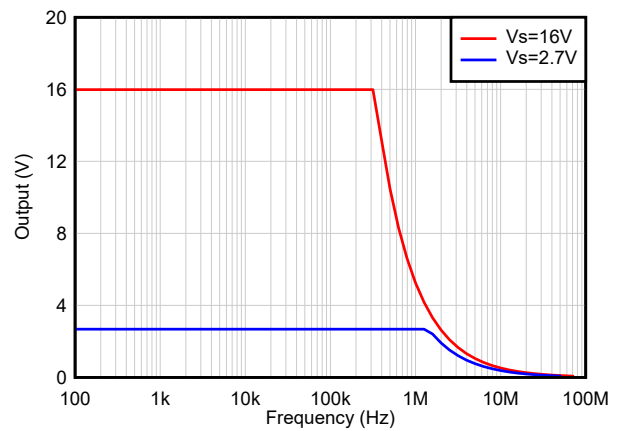


図 5-38. Maximum Output Voltage vs Frequency

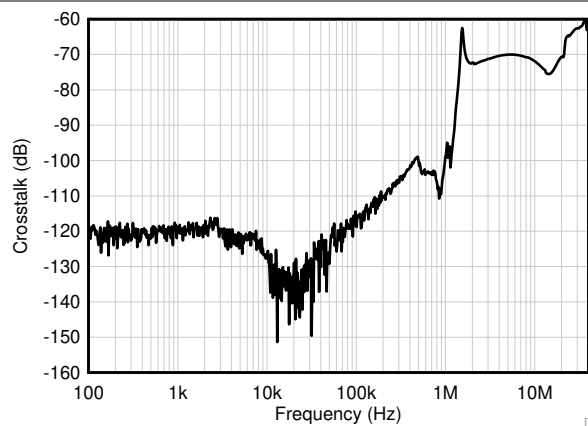


図 5-39. Channel Separation vs Frequency

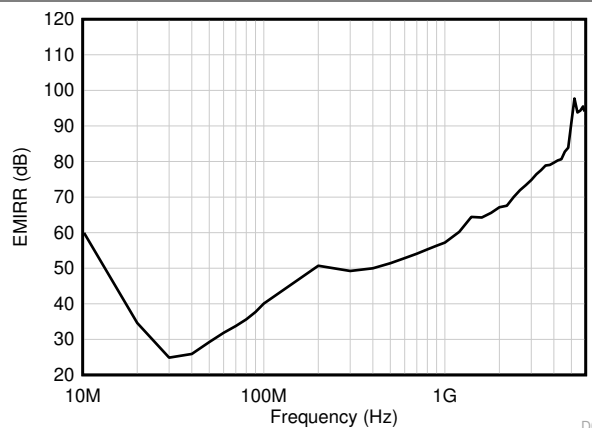


図 5-40. EMIRR (Electromagnetic Interference Rejection Ratio) vs Frequency

6 Detailed Description

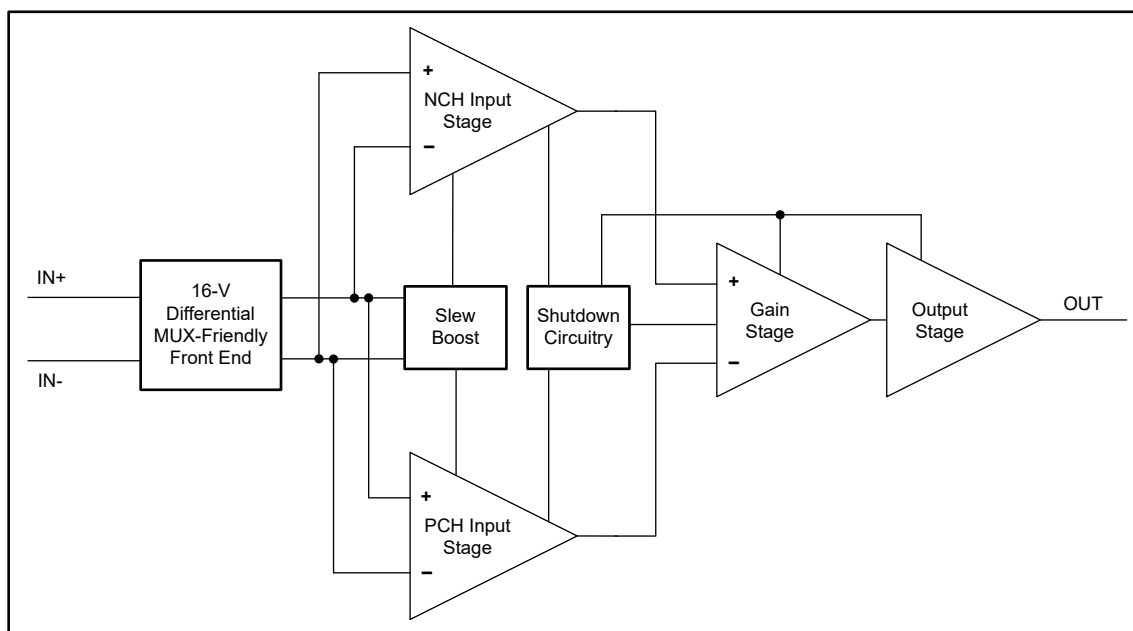
6.1 Overview

The TLV916x-Q1 family (TLV9161-Q1, TLV9162-Q1, and TLV9164-Q1) is a family of 16V, general-purpose, automotive operational amplifiers.

These devices offer excellent DC precision and AC performance, including rail-to-rail input or output, low offset ($\pm 210\mu\text{V}$, typical), low offset drift ($\pm 0.25\mu\text{V}/^\circ\text{C}$, typical), and 11MHz bandwidth.

Features such as wide differential input range, high short-circuit current ($\pm 73\text{mA}$), and high slew rate ($33\text{V}/\mu\text{s}$) make the TLV916x-Q1 a flexible, robust, and high-performance operational amplifier for 16V automotive applications.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Input Protection Circuitry

The TLV916x-Q1 uses a special input architecture to eliminate the requirement for input protection diodes but still provides robust input protection under transient conditions. [Figure 6-1](#) shows conventional input diode protection schemes that are activated by fast transient step responses and introduce signal distortion and settling time delays because of alternate current paths, as shown in [Figure 6-2](#). For low-gain circuits, these fast-ramping input signals forward-bias back-to-back diodes, causing an increase in input current and resulting in extended settling time.

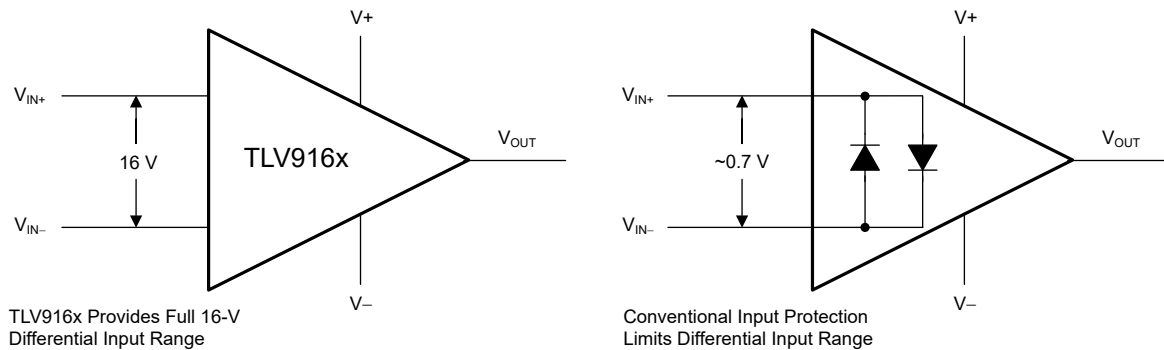


Figure 6-1. TLV916x-Q1 Input Protection Does Not Limit Differential Input Capability

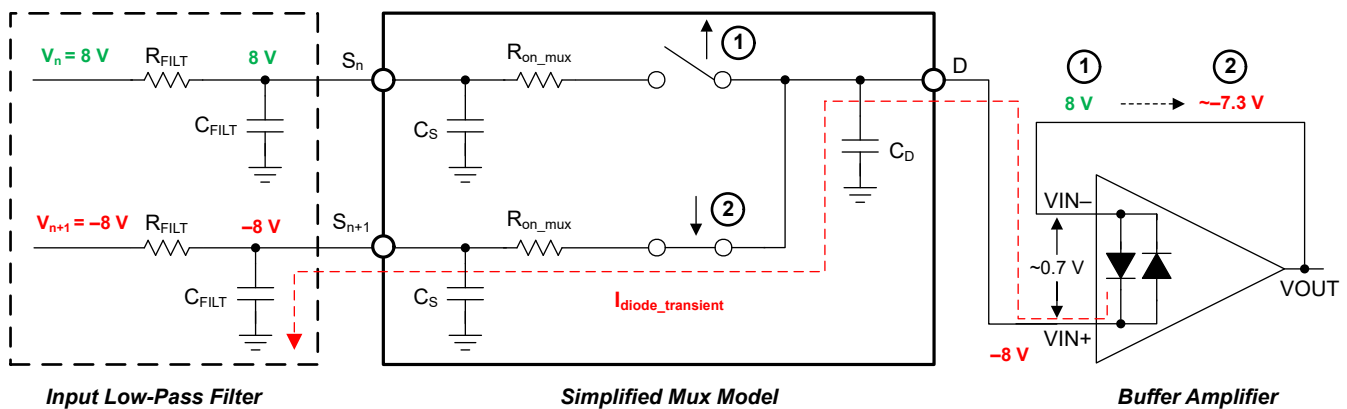


Figure 6-2. Back-to-Back Diodes Create Settling Issues

The TLV916x-Q1 family of operational amplifiers provides a true high-impedance differential input capability using a patented input protection architecture that does not introduce additional signal distortion or delayed settling time, making the device an optimal op amp for multichannel, high-switched, input applications. The TLV916x-Q1 tolerates a maximum differential swing (voltage between inverting and non-inverting pins of the op amp) of up to 16V, making the device suitable for use as a comparator or in applications with fast-ramping input signals such as data-acquisition systems; see the TI TechNote [MUX-Friendly Precision Operational Amplifiers](#) for more information.

6.3.2 EMI Rejection

The TLV916x-Q1 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the TLV916x-Q1 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10MHz to 6GHz. 図 6-3 shows the results of this testing on the TLV916x-Q1. 表 6-1 provides the EMIRR IN+ values for the TLV916x-Q1 at particular frequencies commonly encountered in real-world applications. The *EMI Rejection Ratio of Operational Amplifiers* application report contains detailed information on the topic of EMIRR performance as it relates to op amps and is available for download from www.ti.com.

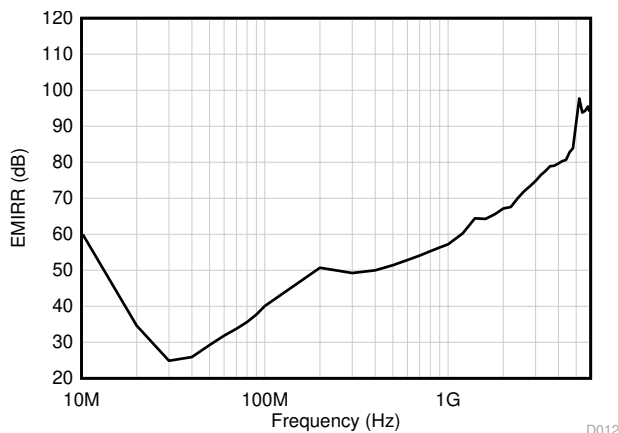


図 6-3. EMIRR Testing

表 6-1. TLV9161-Q1 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	50.0dB
900MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6GHz), GSM, aeronautical mobile, UHF applications	56.3dB
1.8GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1GHz to 2GHz)	65.6dB
2.4GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2GHz to 4GHz)	70.0dB
3.6GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	78.9dB
5GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4GHz to 8GHz)	91.0dB

6.3.3 Thermal Protection

The internal power dissipation of any amplifier causes its internal (junction) temperature to rise. This phenomenon is called *self heating*. The absolute maximum junction temperature of the TLV916x-Q1 is 150°C. Exceeding this temperature causes damage to the device. The TLV916x-Q1 has a thermal protection feature that reduces damage from self heating. The protection works by monitoring the temperature of the device and turning off the op amp output drive for temperatures above 170°C. Figure 6-4 shows an application example for the TLV9162-Q1 that has significant self heating because of its power dissipation (0.627W). In this example, both channels have a quiescent power dissipation while one of the channels has a significant load. Thermal calculations indicate that for an ambient temperature of 60°C, the device junction temperature reaches 175°C. The actual device, however, turns off the output drive to recover towards a safe junction temperature. Figure 6-4 shows how the circuit behaves during thermal protection. During normal operation, the device acts as a buffer so the output is 5V. When self heating causes the device junction temperature to increase above the internal limit, the thermal protection forces the output to a high-impedance state and the output is pulled to ground through resistor R_L . If the condition that caused excessive power dissipation is not removed, the amplifier will oscillate between a shutdown and enabled state until the output fault is corrected. Please note that thermal performance can vary greatly depending on the package selected and the PCB layout design. This example uses the thermal performance of the TSSOP (8) package.

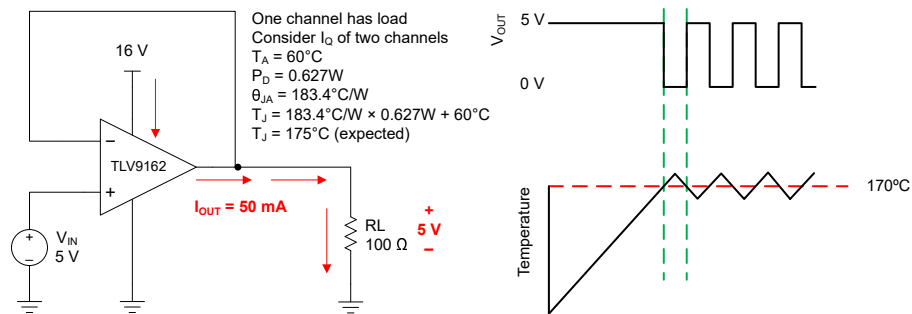


Figure 6-4. Thermal Protection

6.3.4 Capacitive Load and Stability

The TLV916x-Q1 features an output stage capable of driving moderate capacitive loads, and by leveraging an isolation resistor, the device can easily be configured to drive larger capacitive loads. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads; see Figure 6-5 and Figure 6-6. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier will be stable in operation.

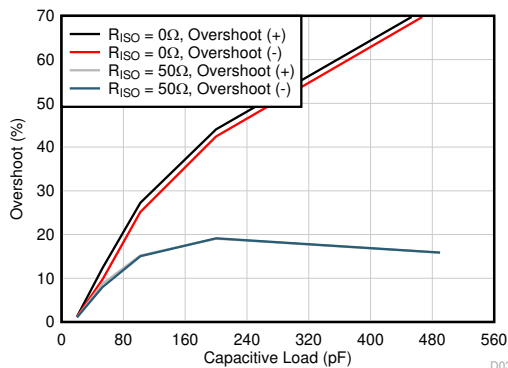


Figure 6-5. Small-Signal Overshoot vs Capacitive Load (20mV_{pp} Output Step, G = +1)

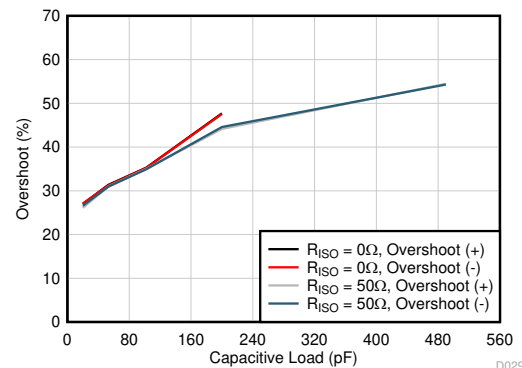


Figure 6-6. Small-Signal Overshoot vs Capacitive Load (20mV_{pp} Output Step, G = -1)

For additional drive capability in unity-gain configurations, improve capacitive load drive by inserting a small resistor, R_{ISO} , in series with the output, as shown in 図 6-7. This resistor significantly reduces ringing and maintains DC performance for purely capacitive loads. However, if a resistive load is in parallel with the capacitive load, then a voltage divider is created, thus introducing a gain error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio R_{ISO} / R_L , and is generally negligible at low output levels. A high capacitive load drive makes the TLV916x-Q1 well suited for applications such as reference buffers, MOSFET gate drives, and cable-shield drives. The circuit shown in 図 6-7 uses an isolation resistor, R_{ISO} , to stabilize the output of an op amp. R_{ISO} modifies the open-loop gain of the system for increased phase margin.

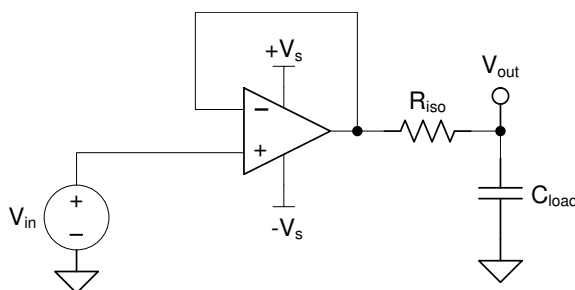


図 6-7. Extending Capacitive Load Drive With the TLV9161-Q1

6.3.5 Common-Mode Voltage Range

The TLV916x-Q1 is a 16V, rail-to-rail input operational amplifier with an input common-mode range that extends to both supply rails. This wide range is achieved with paralleled complementary N-channel and P-channel differential input pairs, as shown in [Figure 6-8](#). The N-channel pair is active for input voltages close to the positive rail, typically from $(V+) - 1V$ to the positive supply. The P-channel pair is active for inputs from the negative supply to approximately $(V+) - 2V$. There is a small transition region, typically $(V+) - 2V$ to $(V+) - 1V$ in which both input pairs are on. This transition region can vary modestly with process variation. Within this region PSRR, CMRR, offset voltage, offset drift, noise, and THD performance may be degraded compared to operation outside this region.

[Figure 5-5](#) shows this transition region for a typical device in terms of input voltage offset in more detail.

For more information on common-mode voltage range and PMOS/NMOS pair interaction, see [Op Amps With Complementary-Pair Input Stages](#) application note.

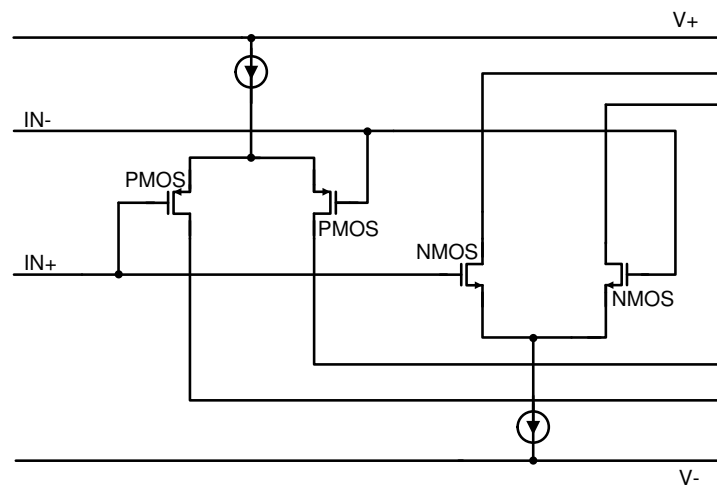


Figure 6-8. Rail-to-Rail Input Stage

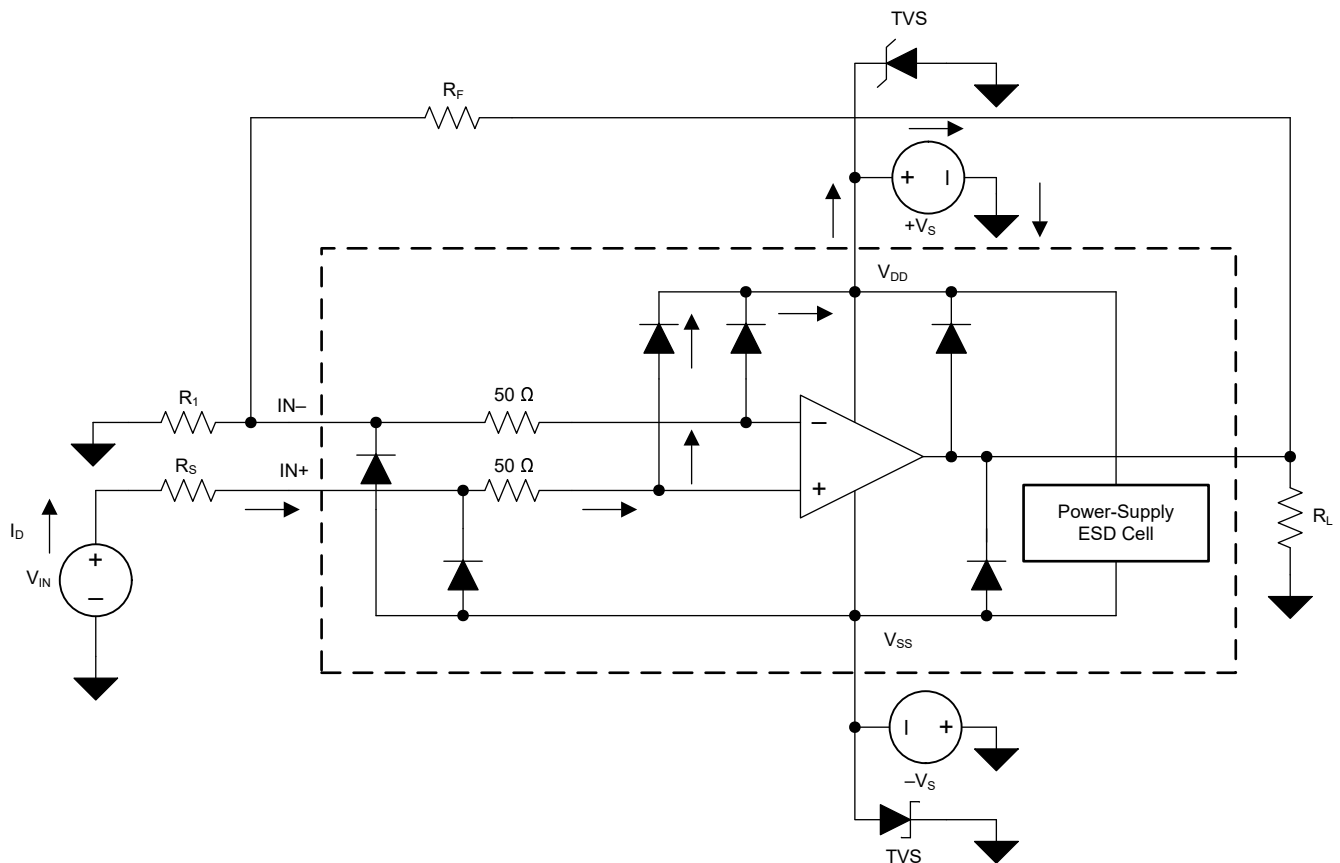
6.3.6 Phase Reversal Protection

The TLV916x-Q1 family has internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in non-inverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The TLV916x-Q1 is a rail-to-rail input op amp; therefore, the common-mode range can extend up to the rails. Input signals beyond the rails do not cause phase reversal; instead, the output limits into the appropriate rail. For more information on phase reversal, see [Op Amps With Complementary-Pair Input Stages](#) application note.

6.3.7 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress (EOS). These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. 6-9 shows an illustration of the ESD circuits contained in the TLV916x-Q1 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device or the power-supply ESD cell, internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.



6-9. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event is very short in duration and very high voltage (for example; 1kV, 100ns), whereas an EOS event is long duration and lower voltage (for example; 50V, 100ms). The ESD diodes are designed for out-of-circuit ESD protection (that is, during assembly, test, and storage of the device before being soldered to the PCB). During an ESD event, the ESD signal is passed through the ESD steering diodes to an absorption circuit (labeled ESD power-supply circuit). The ESD absorption circuit clamps the supplies to a safe level.

Although this behavior is necessary for out-of-circuit protection, excessive current and damage is caused if activated in-circuit. A transient voltage suppressors (TVS) can be used to prevent against damage caused by turning on the ESD absorption circuit during an in-circuit ESD event. Using the appropriate current limiting resistors and TVS diodes allows for the use of device ESD diodes to protect against EOS events.

6.3.8 Overload Recovery

Overload recovery is defined as the time required for the op amp output to recover from a saturated state to a linear state. The output devices of the op amp enter a saturation region when the output voltage exceeds the rated operating voltage, either due to the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the TLV916x-Q1 is approximately 120ns.

6.3.9 Typical Specifications and Distributions

Designers often have questions about a typical specification of an amplifier in order to design a more robust circuit. Due to natural variation in process technology and manufacturing procedures, every specification of an amplifier will exhibit some amount of deviation from the ideal value, like an amplifier's input offset voltage. These deviations often follow *Gaussian (bell curve)*, or *normal* distributions, and circuit designers can leverage this information to guardband their system, even when there is not a minimum or maximum specification in the [Electrical Characteristics](#) table.

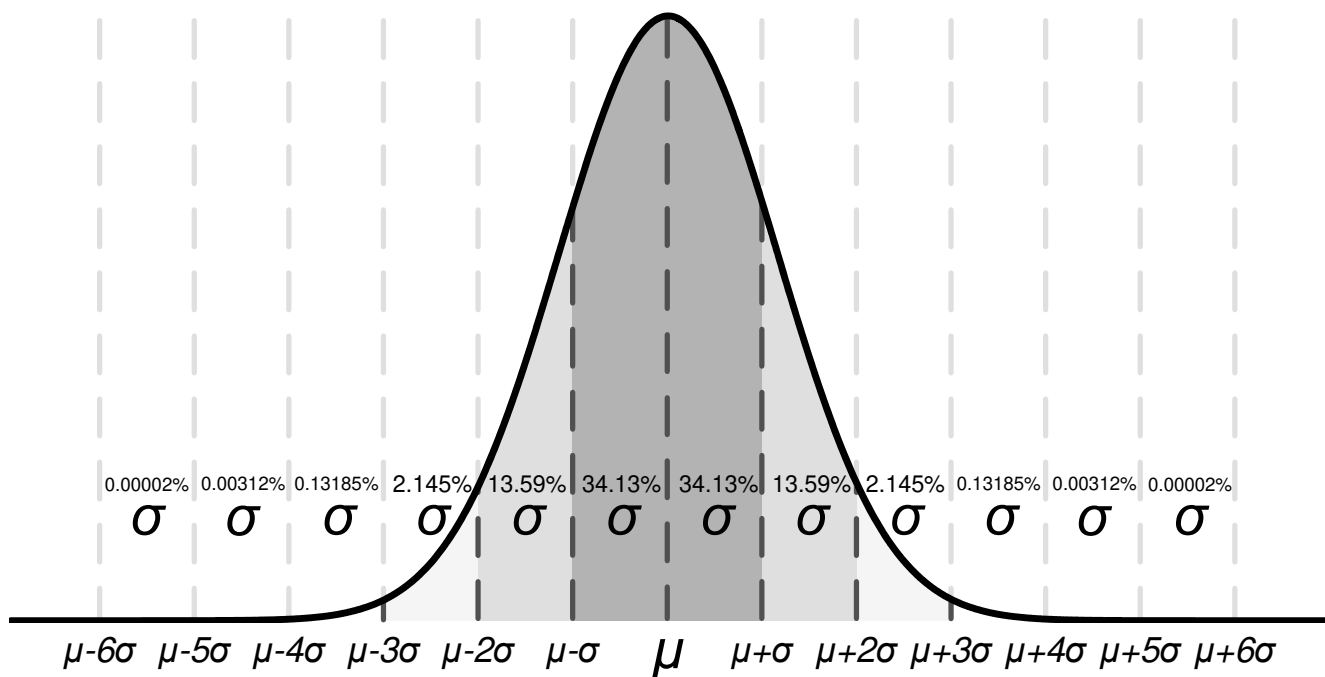


図 6-10. Ideal Gaussian Distribution

図 6-10 shows an example distribution, where μ , or μ , is the mean of the distribution, and where σ , or σ , is the standard deviation of a system. For a specification that exhibits this kind of distribution, approximately two-thirds (68.26%) of all units can be expected to have a value within one standard deviation, or one sigma, of the mean (from $\mu - \sigma$ to $\mu + \sigma$).

Depending on the specification, values listed in the *typical* column of the [Electrical Characteristics](#) table are represented in different ways. As a general rule of thumb, if a specification naturally has a nonzero mean (for example, like gain bandwidth), then the typical value is equal to the mean (μ). However, if a specification naturally has a mean near zero (like input offset voltage), then the typical value is equal to the mean plus one standard deviation ($\mu + \sigma$) in order to most accurately represent the typical value.

This chart can be used to calculate approximate probability of a specification in a unit; for example, for TLV916x-Q1, the typical input voltage offset is 210 μ V, so 68.2% of all TLV916x-Q1 devices are expected to have an offset from $-210\mu\text{V}$ to 210 μ V. At 4 σ ($\pm 840\mu\text{V}$), 99.9937% of the distribution has an offset voltage less than $\pm 840\mu\text{V}$, which means 0.0063% of the population is outside of these limits, which corresponds to about 1 in 15,873 units.

Specifications with a value in the minimum or maximum column are assured by TI, and units outside these limits will be removed from production material. For example, the TLV916x-Q1 family has a maximum offset voltage of 1mV at 25°C, and even though this corresponds to about 5 σ (≈ 1 in 1.7 million units), which is extremely unlikely, TI assures that any unit with larger offset than 1mV will be removed from production material.

For specifications with no value in the minimum or maximum column, consider selecting a sigma value of sufficient guardband for the application, and design worst-case conditions using this value. For example, the 6 σ value corresponds to about 1 in 500 million units, which is an extremely unlikely chance, and could be an option as a wide guardband to design a system around. In this case, the TLV916x-Q1 family does not have a maximum or minimum for offset voltage drift, but based on the typical value of 0.25 $\mu\text{V}/^\circ\text{C}$ in the [Electrical Characteristics](#) table, it can be calculated that the 6 σ value for offset voltage drift is about 1.5 $\mu\text{V}/^\circ\text{C}$. When designing for worst-case system conditions, this value can be used to estimate the worst possible offset across temperature without having an actual minimum or maximum value.

However, process variation and adjustments over time can shift typical means and standard deviations, and unless there is a value in the minimum or maximum specification column, TI cannot assure the performance of a device. This information should be used only to estimate the performance of a device.

6.4 Device Functional Modes

The TLV916x-Q1 has a single functional mode and is operational when the power-supply voltage is greater than 2.7V ($\pm 1.35\text{V}$). The maximum power supply voltage for the TLV916x-Q1 is 16V ($\pm 8\text{V}$).

7 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TLV916x-Q1 family offers excellent DC precision and AC performance. These devices operate up to 16V supply rails and offer true rail-to-rail input/output, low offset voltage and offset voltage drift, as well as 11MHz bandwidth and high output drive. These features make the TLV916x-Q1 a robust, high-performance operational amplifier for 16V industrial applications.

7.2 Typical Applications

7.2.1 Low-Side Current Measurement

Figure 7-1 shows the TLV9161-Q1 configured in a low-side current sensing application. For a full analysis of the circuit shown in Figure 7-1 including theory, calculations, simulations, and measured data, see TI Precision Design TIPD129, *0A to 1A Single-Supply Low-Side Current-Sensing Solution*.

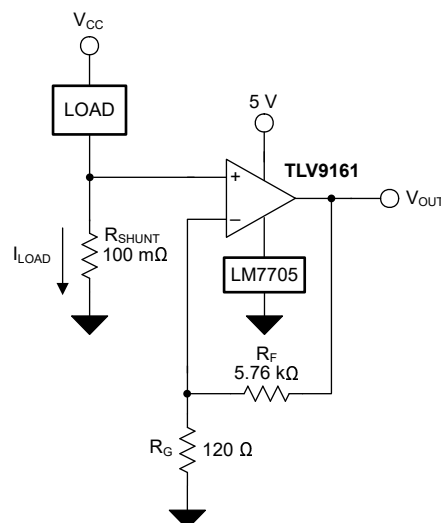


Figure 7-1. TLV9161-Q1 in a Low-Side, Current-Sensing Application

7.2.1.1 Design Requirements

The design requirements for this design are:

- Load current: 0A to 1A
- Output voltage: 4.9V
- Maximum shunt voltage: 100mV

7.2.1.2 Detailed Design Procedure

The transfer function of the circuit in 図 7-1 is given in 式 1:

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times \text{Gain} \quad (1)$$

The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0A to 1A. To keep the shunt voltage below 100mV at maximum load current, the largest shunt resistor is defined using 式 2:

$$R_{SHUNT} = \frac{V_{SHUNT_MAX}}{I_{LOAD_MAX}} = \frac{100 \text{ mV}}{1 \text{ A}} = 100 \text{ m}\Omega \quad (2)$$

Using 式 2, R_{SHUNT} is calculated to be 100mΩ. The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the TLV916x-Q1 to produce an output voltage of 0V to 4.9V. The gain needed by the TLV916x-Q1 to produce the necessary output voltage is calculated using 式 3:

$$\text{Gain} = \frac{(V_{OUT_MAX} - V_{OUT_MIN})}{(V_{IN_MAX} - V_{IN_MIN})} \quad (3)$$

Using 式 3, the required gain is calculated to be 49V/V, which is set with resistors R_F and R_G . 式 4 is used to size the resistors, R_F and R_G , to set the gain of the TLV916x-Q1 to 49V/V.

$$\text{Gain} = 1 + \frac{(R_F)}{(R_G)} \quad (4)$$

Choosing R_F as 5.76kΩ, R_G is calculated to be 120Ω. R_F and R_G were chosen as 5.76kΩ and 120Ω because the values are standard value resistors that create a 49:1 ratio. Other resistors that create a 49:1 ratio can also be used. However, excessively large resistors generate thermal noise that exceeds the intrinsic noise of the op amp. 図 7-2 shows the measured transfer function of the circuit shown in 図 7-1.

7.2.1.3 Application Curves

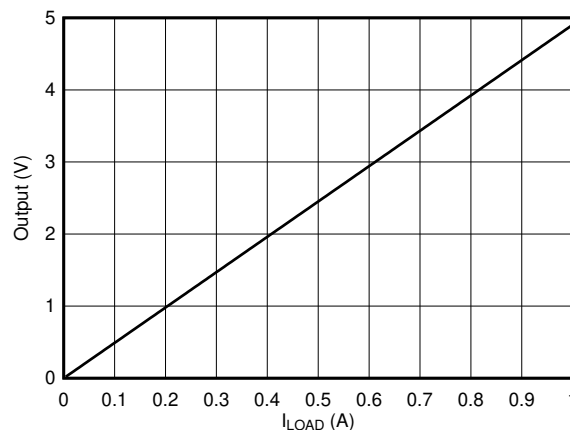


図 7-2. Low-Side, Current-Sense, Transfer Function

7.3 Power Supply Recommendations

The TLV916x-Q1 is specified for operation from 2.7V to 16V ($\pm 1.35\text{V}$ to $\pm 8\text{V}$); many specifications apply from -40°C to 125°C or with specific supply voltage and test conditions.

注意

Supply voltages larger than 20V can permanently damage the device; see the [Absolute Maximum Ratings](#) section.

Place 0.1µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to the [Layout](#) section.

7.4 Layout

7.4.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
 - Connect low-ESR, 0.1µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in [Figure 7-4](#), keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

7.4.2 Layout Example

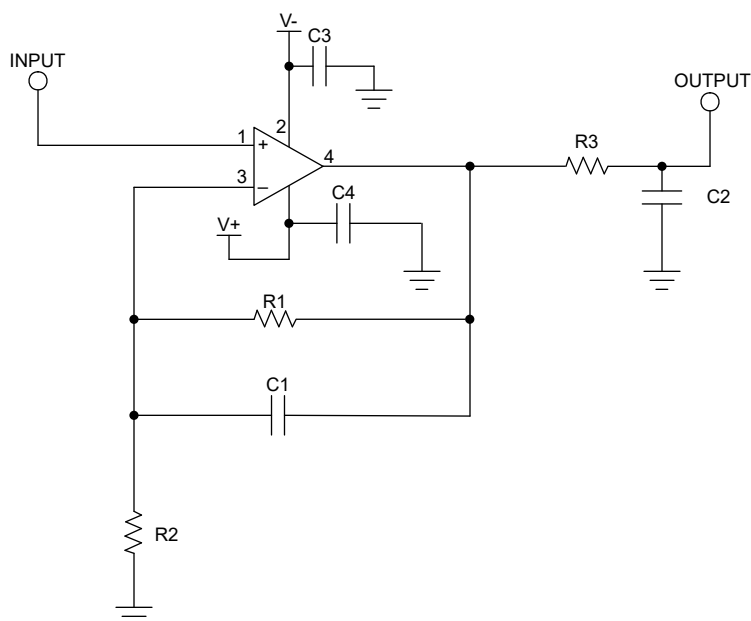


図 7-3. Schematic for Non-inverting Configuration Layout Example

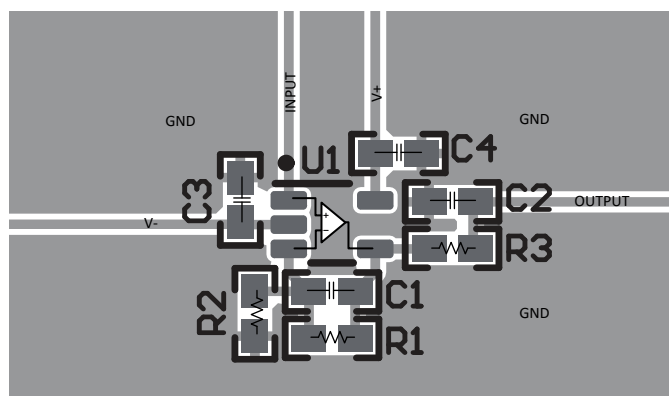


図 7-4. Operational Amplifier Board Layout for Non-inverting Configuration - SC70 (DCK) Package

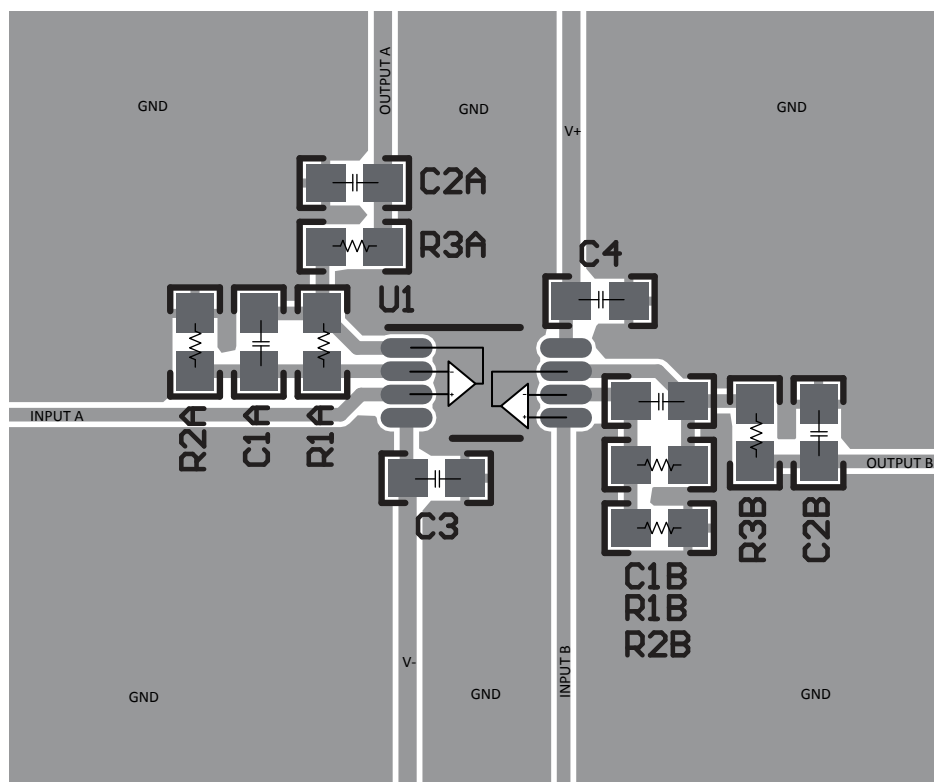


図 7-5. Example Layout for VSSOP-8 (DGK) Package

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a [free download](#) from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

注

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the [TINA-TI folder](#).

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following:

1. Texas Instruments, [Analog Engineer's Circuit Cookbook: Amplifiers](#)
2. Texas Instruments, [AN31 amplifier circuit collection](#) application note
3. Texas Instruments, [MUX-Friendly, Precision Operational Amplifiers](#) application brief
4. Texas Instruments, [EMI Rejection Ratio of Operational Amplifiers](#) application note
5. Texas Instruments, [Op Amps With Complementary-Pair Input Stages](#) application note

8.3 ドキュメントの更新通知を受け取る方法

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8.7 用語集

[テキサス・インスツルメンツ用語集](#)

この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

Changes from Revision * (April 2023) to Revision A (August 2024)	Page
• 「製品情報」表を「パッケージ情報」に変更.....	1
• パッケージ情報の表に PW パッケージを追加。.....	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV9161QDBVRQ1	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2W2H
TLV9161QDBVRQ1.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2W2H
TLV9161QDCKRQ1	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1NJ
TLV9161QDCKRQ1.A	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1NJ
TLV9162QDGKRQ1	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2S5T
TLV9162QDGKRQ1.A	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2S5T
TLV9162QDRQ1	Active	Production	SOIC (D) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9162Q
TLV9162QDRQ1.A	Active	Production	SOIC (D) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9162Q
TLV9162QPWRQ1	Active	Production	TSSOP (PW) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	9162PW
TLV9162QPWRQ1.A	Active	Production	TSSOP (PW) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	9162PW
TLV9164QDRQ1	Active	Production	SOIC (D) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV9164QD
TLV9164QDRQ1.A	Active	Production	SOIC (D) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV9164QD
TLV9164QPWRQ1	Active	Production	TSSOP (PW) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9164PW
TLV9164QPWRQ1.A	Active	Production	TSSOP (PW) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9164PW

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

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⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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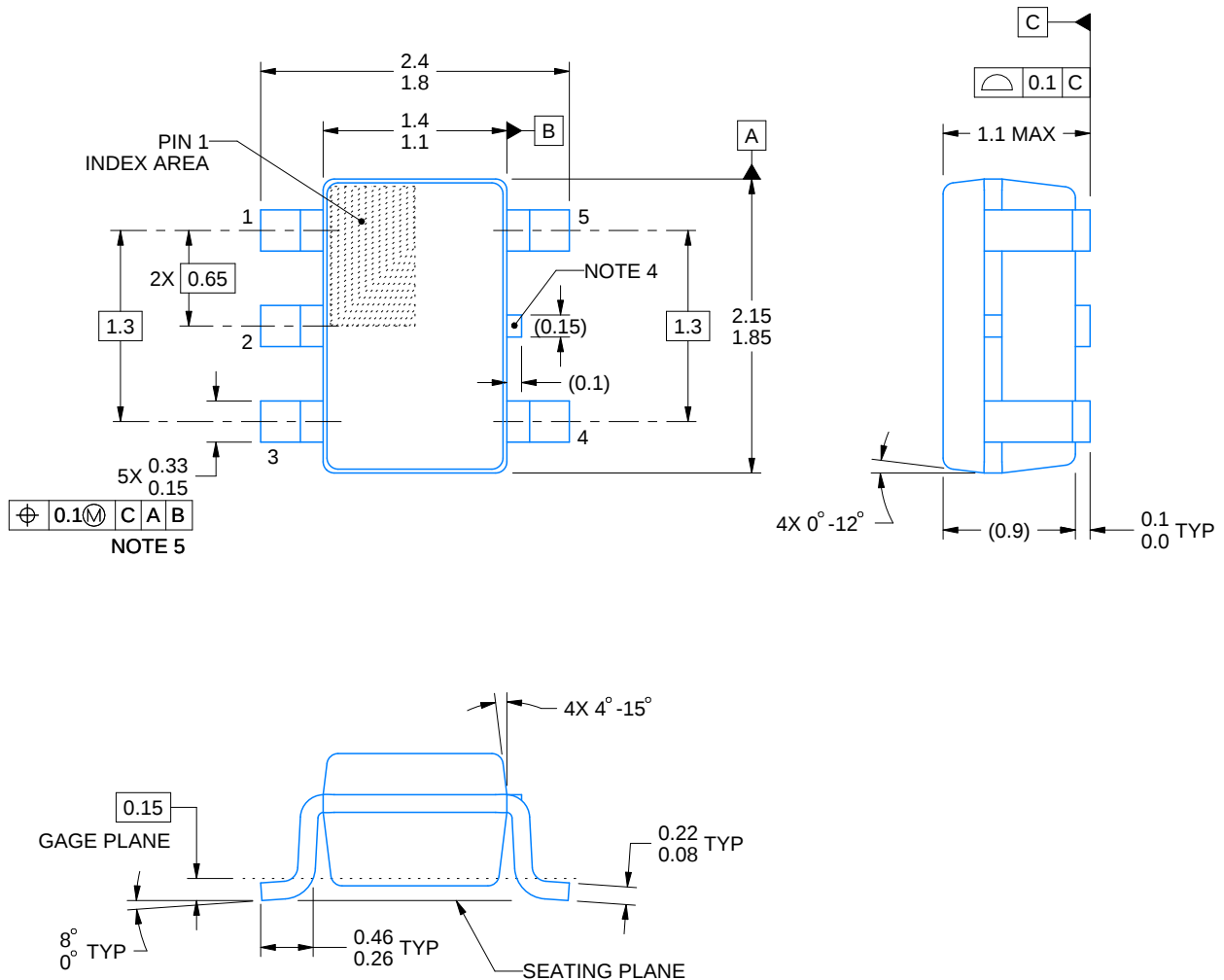
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV9161-Q1, TLV9162-Q1, TLV9164-Q1 :

- Catalog : [TLV9161](#), [TLV9162](#), [TLV9164](#)

NOTE: Qualified Version Definitions:

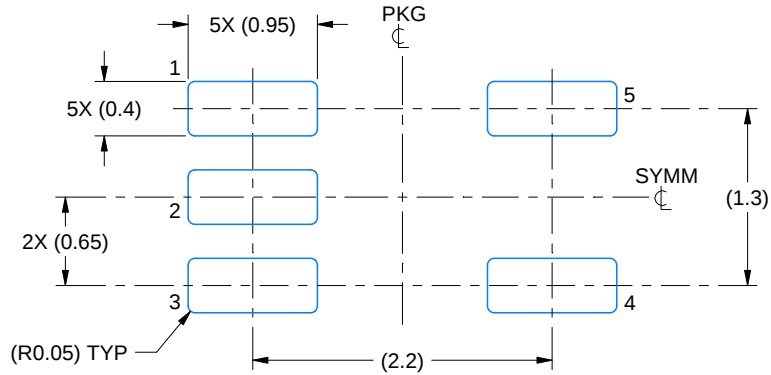
- Catalog - TI's standard catalog product



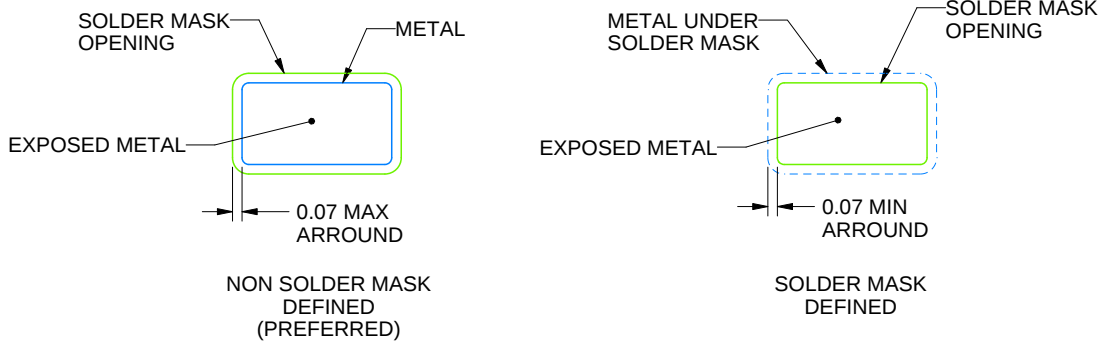
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

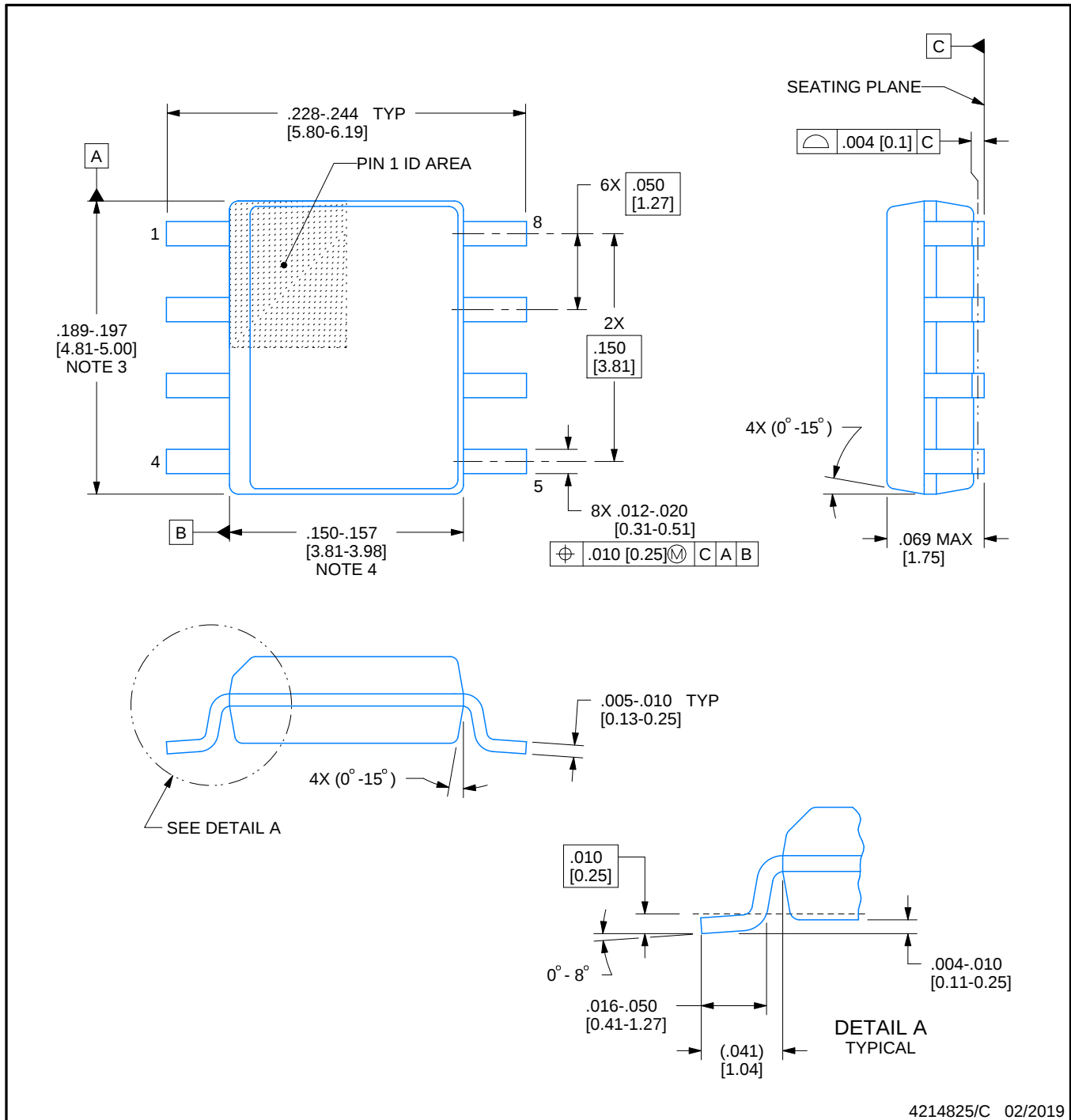


D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

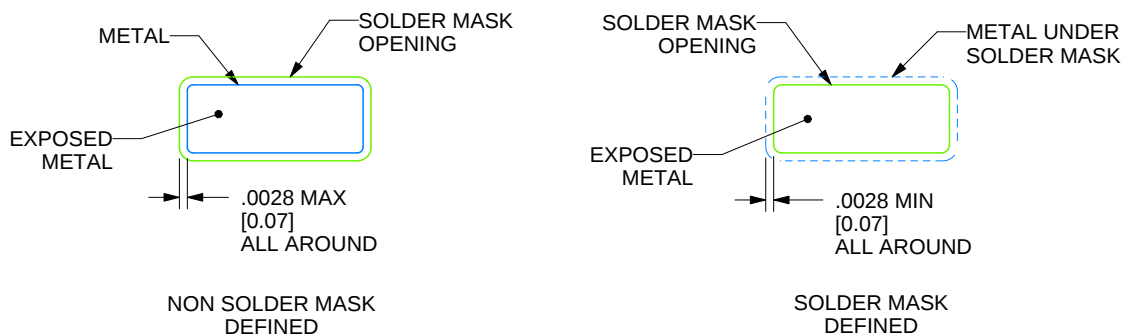
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

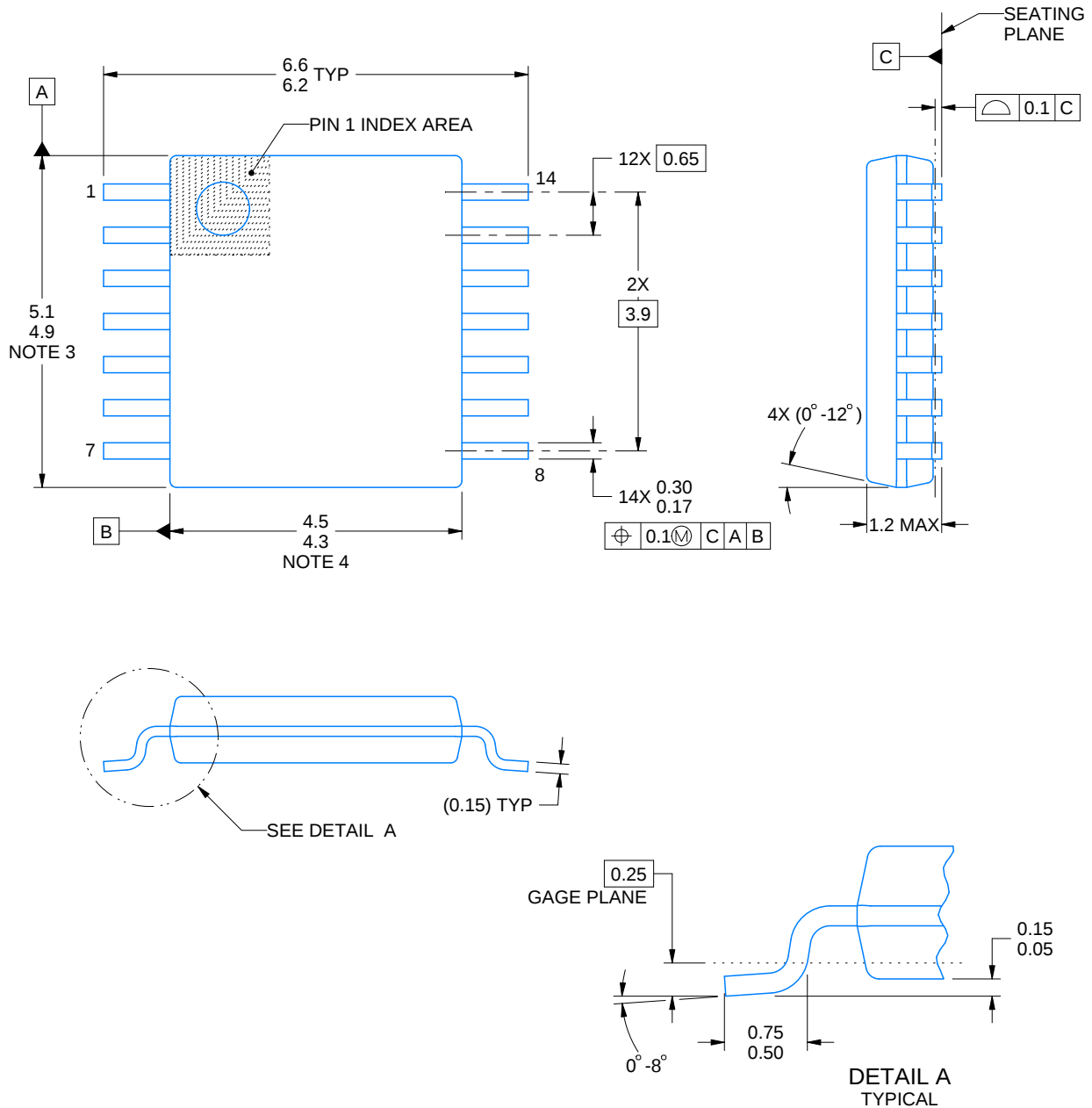
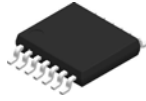


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

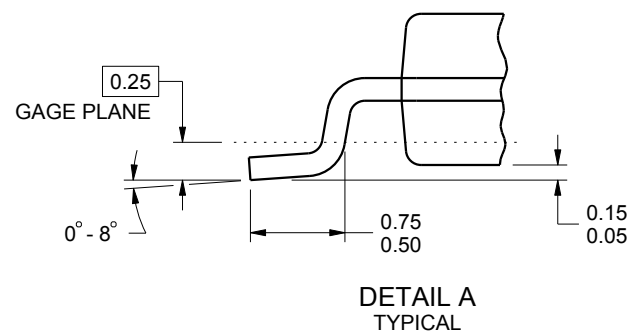
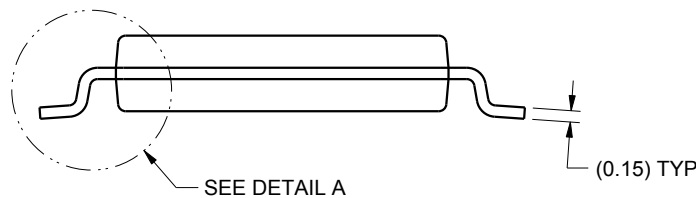
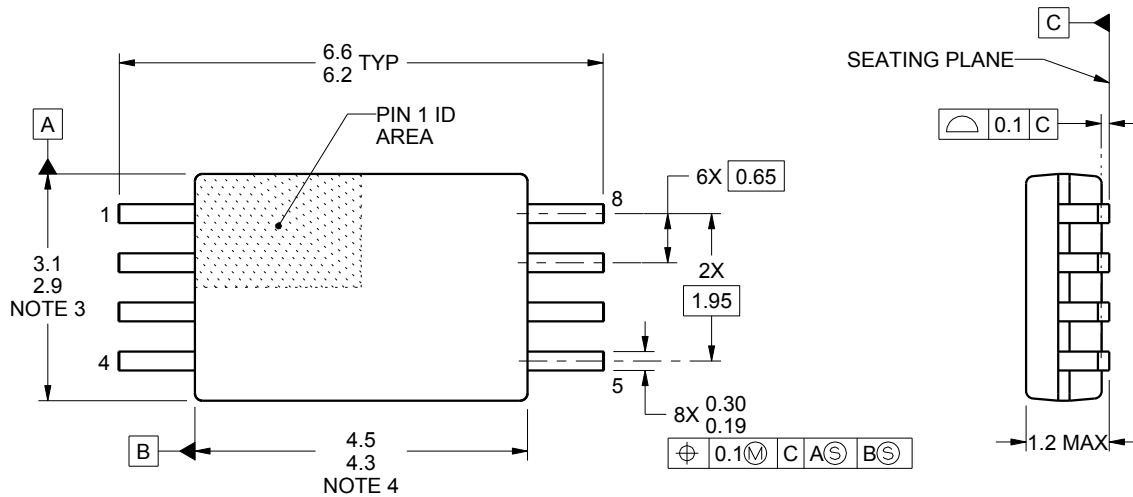
PW0008A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4221848/A 02/2015

NOTES:

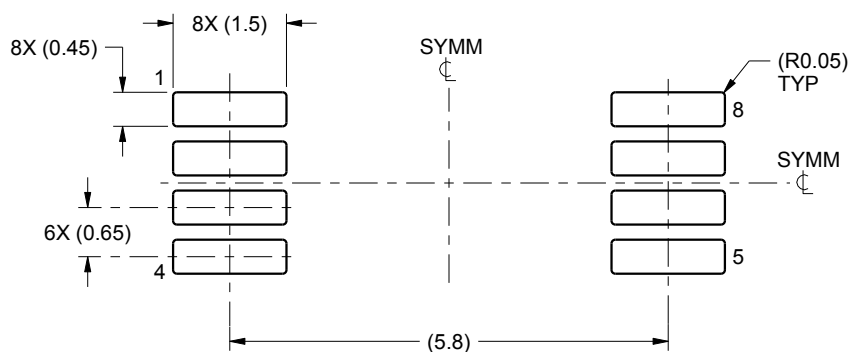
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

EXAMPLE BOARD LAYOUT

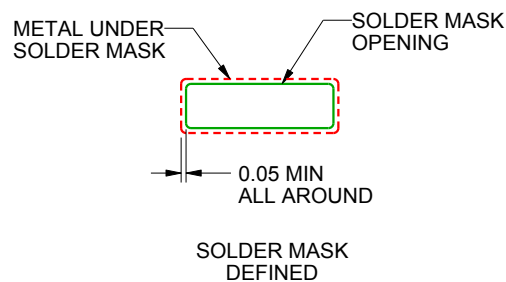
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

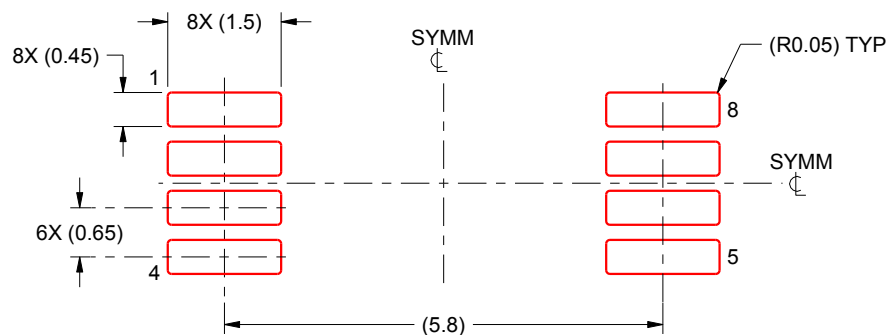
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



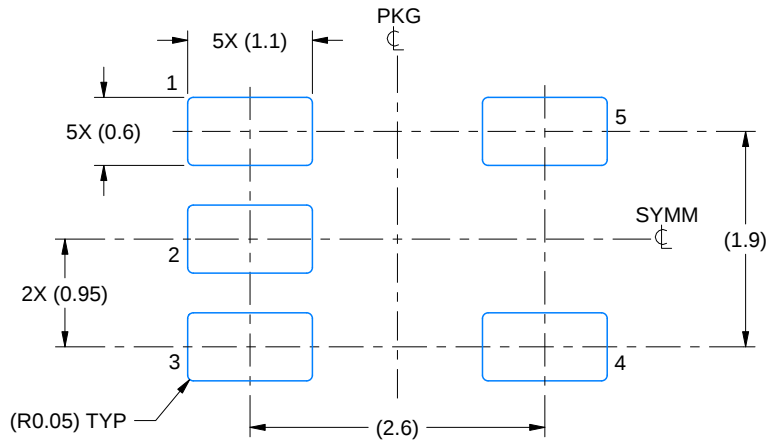
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

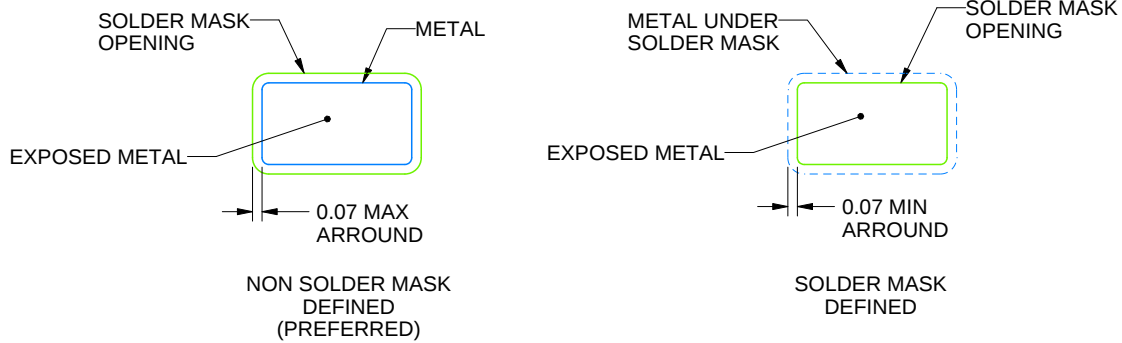
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



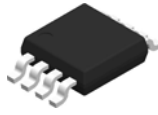
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

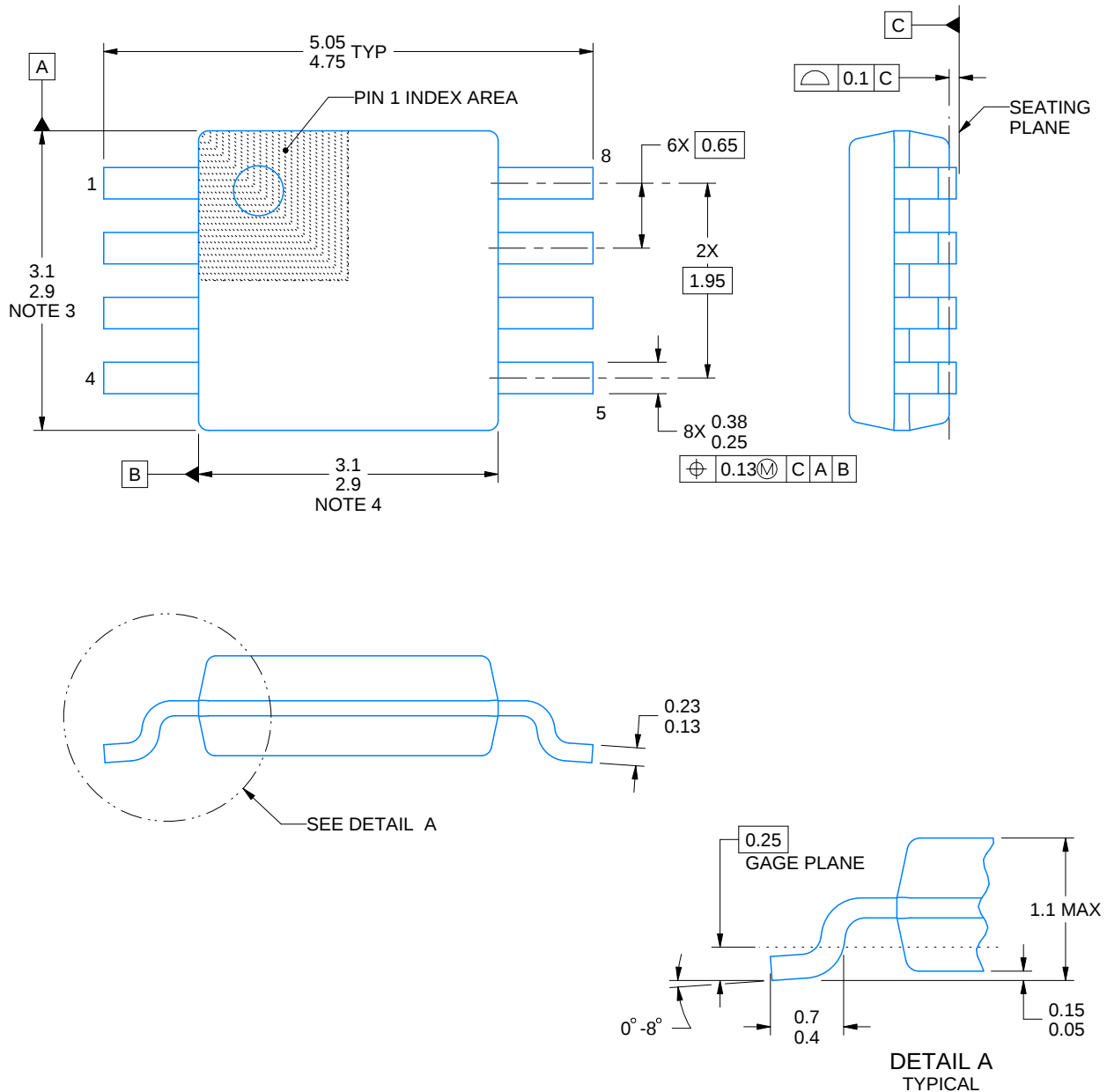
DGK0008A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

NOTES:

PowerPAD is a trademark of Texas Instruments.

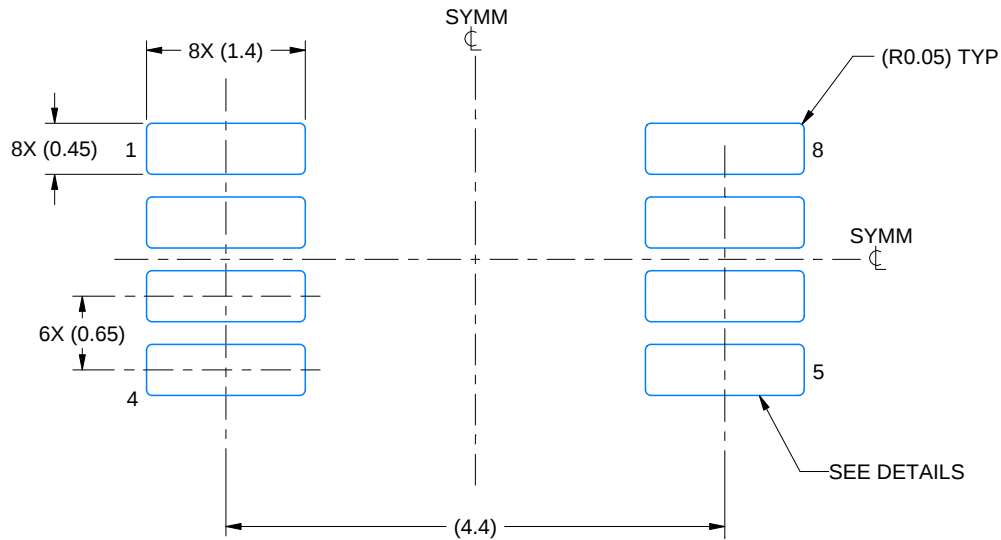
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

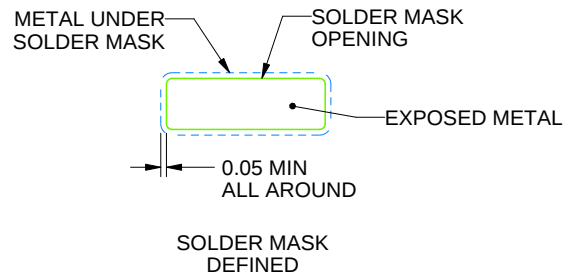
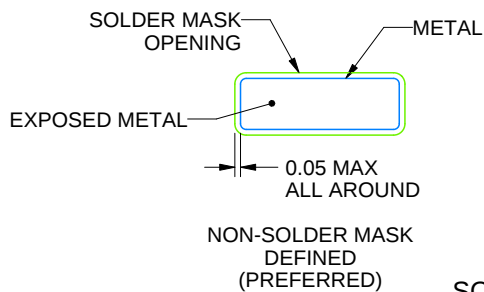
DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

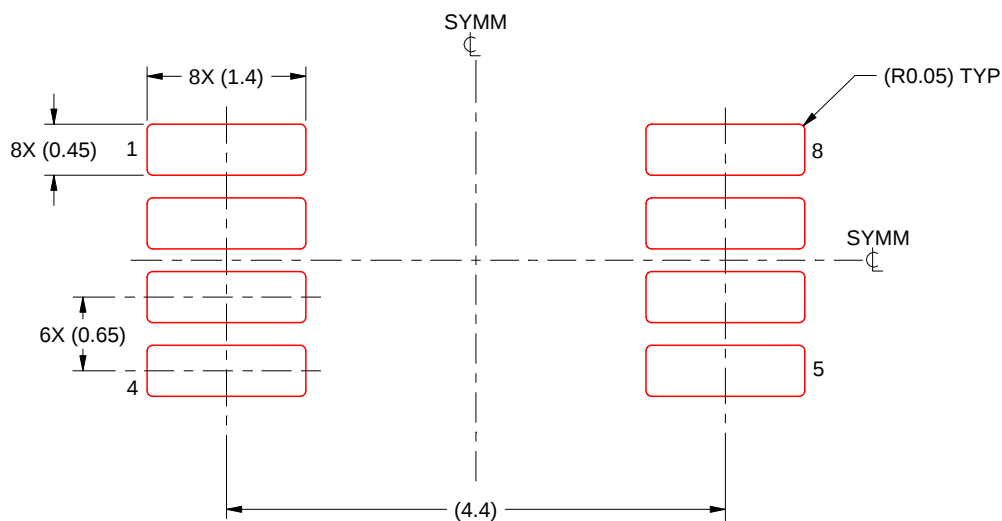
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

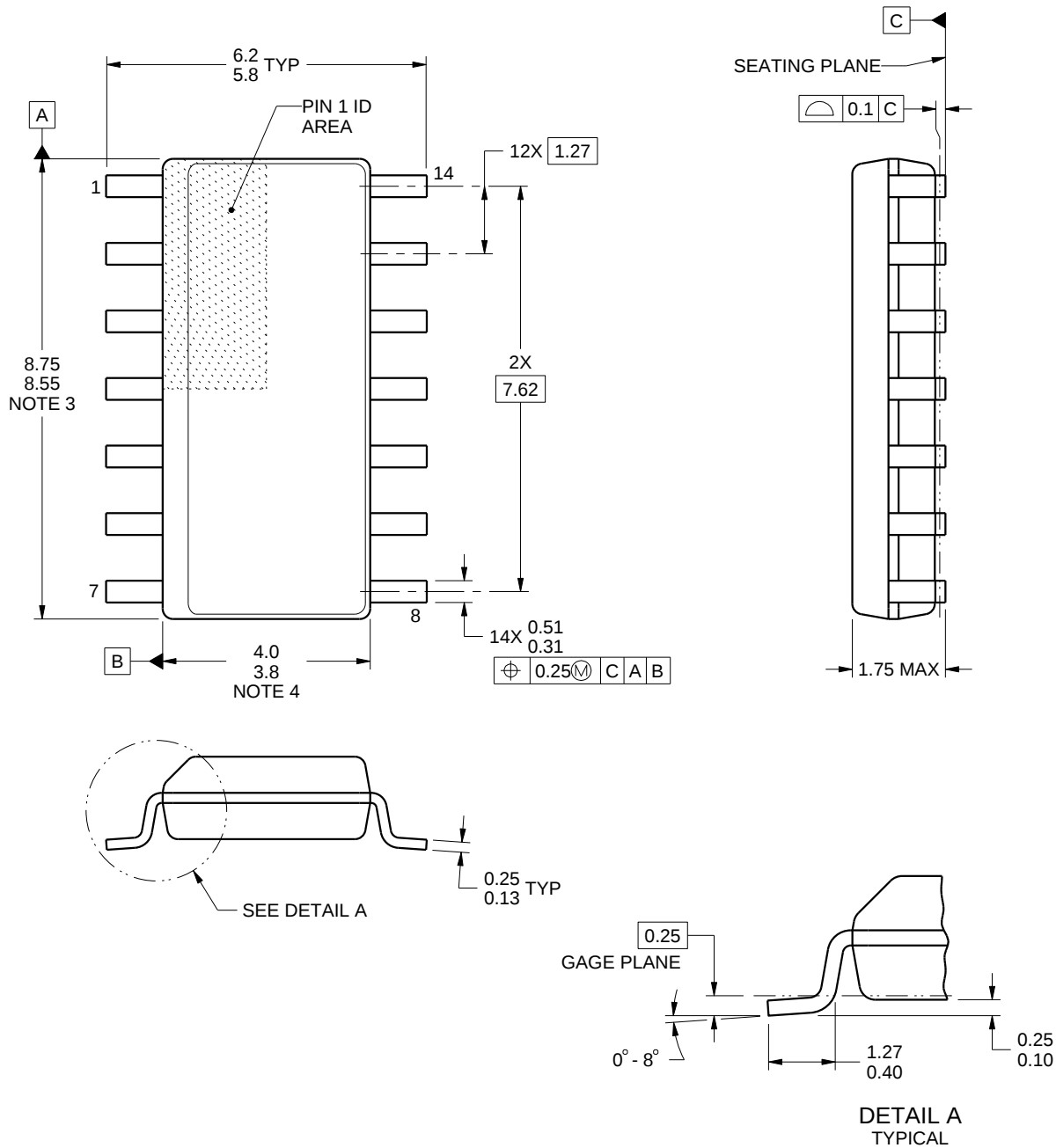
4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

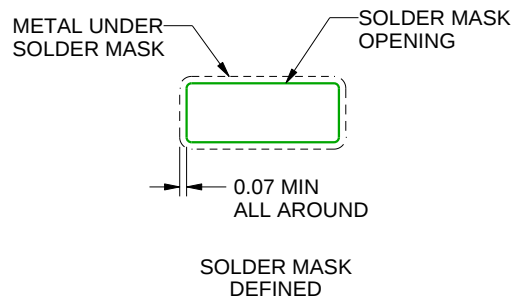
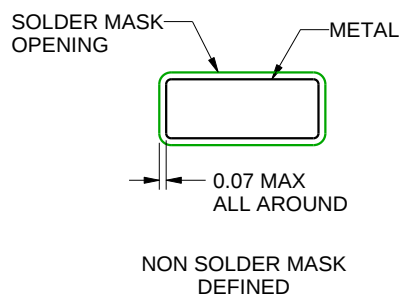
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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