参考資料

TLV9051 / TLV9052 / TLV9054 5MHz、 15V/µs 高スルー レートの RRIO オペアンプ

1 特長

- 高いスルーレート：15V/µs
- 低い静止電流：330µA
- レール ツー レール入出力
- 低い入力オフセット電圧：±0.33mV
- ユニティ ゲイン帯域幅：5MHz
- 低い広帯域ノイズ：15nV/√Hz
- 低い入力バイアス電流：2pA
- ユニティ ゲイン安定
- 内部 RFI および EMI フィルタ
- 低コストのアプリケーション向けのスケーラブルな CMOS オペアンプ ファミリ
- 最低 1.8V の電源電圧で動作
- 拡張温度範囲：-40℃～125℃

2 アプリケーション

- HVAC：暖房、換気、空調
- フォトダイオード・アンプ
- 電流シャント・モニタリングによる DC モータの制御
- 白物家電 (冷蔵庫、洗濯機など)
- センサ・シグナル・コンディショニング
- アクティブ・フィルタ
- ローサイド電流センシング

3 概要

TLV9051、TLV9052、TLV9054 デバイスは、それぞれシングル、デュアル、クワッドのオペアンプです。これらのデバイスは、1.8V～6.0V の低電圧で動作するよう設計されています。入力と出力は、非常に高いスルーレートでレール ツー レールで動作できます。これらのデバイスは、コストが制限され、低電圧動作、高いスルー レート、小さい静止電流が要求されるアプリケーションに理想的です。TLV905x ファミリの容量性負荷の駆動能力は 150pF であり、抵抗性のオープン ループ出力インピーダンスにより、非常に大きな容量性負荷でも簡単に安定化できます。

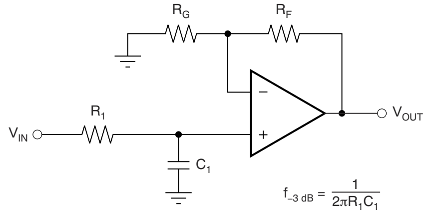
TLV905xS デバイスにはシャットダウン モードがあり、アンプの電源をオフにしてスタンバイ モードに移行すると、標準消費電流は 1µA 未満になります。

TLV905x ファミリのデバイスはユニティ ゲイン安定で、RFI および EMI フィルタが内蔵され、オーバードライブ状況でも位相反転が発生しないため、簡単に使用できます。

製品情報

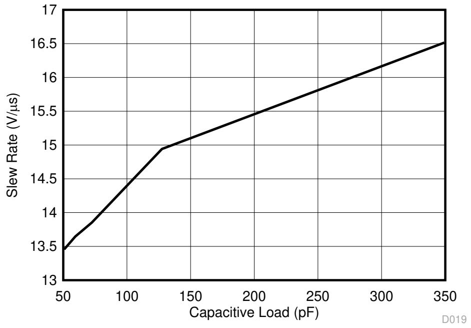
部品番号 (1)	チャネル数	パッケージ (2)	パッケージ サイズ(4)
TLV9051	シングル	DBV (SOT-23、5)	2.9mm × 2.8mm
		DCK (SC70、5)	2mm × 2.1mm
		DRL (SOT553、5)(3)	1.6mm × 1.6mm
		DPW (X2SON、5)	0.8mm × 0.8mm
TLV9051S	シングル、シャットダウン	DBV (SOT-23、6)	2.9mm × 2.8mm
TLV9052	デュアル	D (SOIC、8)	4.9mm × 6mm
		PW (TSSOP、8)	3.mm × 6.4mm
		DGK (VSSOP、8)	3mm × 4.9mm
		DDF (SOT-23、8)	2.9mm × 2.8mm
		DSG (WSON、8)	2mm × 2mm
TLV9052S	デュアル、シャットダウン	DGS (VSSOP、10)	3mm × 4.9mm
		RUG (X2QFN、10)	1.5mm × 2mm
TLV9054	クワッド	D (SOIC、14)	8.65mm × 6mm
		PW (TSSOP、14)	5mm × 6.4mm
		RUC (WQFN、14)	2mm × 2mm
		RTE (WQFN、16)	3mm × 3mm
TLV9054S	クワッド、シャットダウン	RTE (WQFN、16)	3mm × 3mm

(1) 製品比較表を参照してください。
(2) 詳細については、セクション 11 を参照してください。
(3) パッケージはプレビュー専用です。
(4) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR_1C_1}\right)$$

シングル ポールのローパス フィルタ



スルー レートと負荷容量との関係

English Data Sheet: SBOS942

Table of Contents

---

4 Device Comparison Table

DEVICE	NO. OF CH.	PACKAGE LEADS												
		SC70 DCK	SOT-23 DBV	SOT-553 (1) DRL	X2SON DPW	SOIC D	WSON DSG	VSSOP DGK	TSSOP PW	SOT-23 DDF	VSSOP DGS	X2QFN RUG	X2QFN RUC	WQFN RTE
TLV9051	1	5	5	5	5	—	—	—	—	—	—	—	—	—
TLV9051S		—	6	—	—	—	—	—	—	—	—	—	—	—
TLV9052	2	—	—	—	—	8	8	8	8	8	—	—	—	—
TLV9052S		—	—	—	—	—	—	—	—	—	10	10	—	—
TLV9054	4	—	—	—	—	14	—	—	14	—	—	—	14	16
TLV9054S		—	—	—	—	—	—	—	—	—	—	—	—	16

(1) Package is for preview only.

5 Pin Configuration and Functions

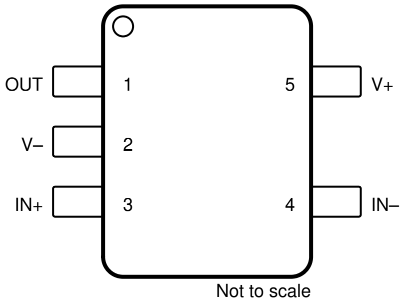


図 5-1. TLV9051 DBV, DRL Packages 5-Pin SOT-23, SOT-553 Top View

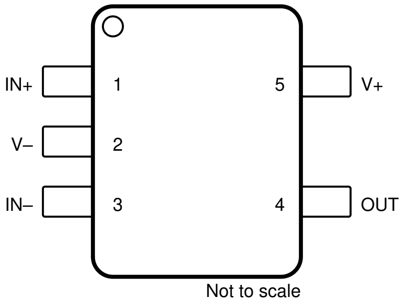


図 5-2. TLV9051 DCK Package 5-Pin SC70 Top View

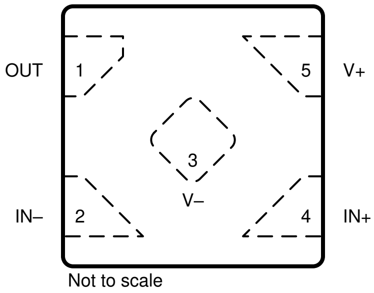


図 5-3. TLV9051 DPW Package 5-Pin X2SON Top View

表 5-1. Pin Functions: TLV9051

PIN				I/O	DESCRIPTION
NAME	SOT-23, SOT-553	SC-70	X2SON		
IN–	4	3	2	I	Inverting input
IN+	3	1	4	I	Noninverting input
OUT	1	4	1	O	Output
V–	2	2	3	—	Negative (low) supply or ground (for single-supply operation)
V+	5	5	5	—	Positive (high) supply

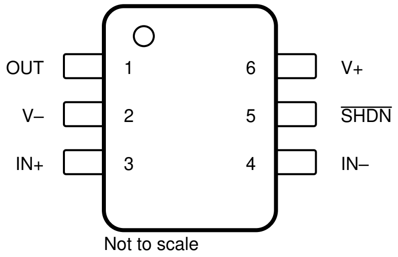


図 5-4. TLV9051S DBV Package 6-Pin SOT-23 Top View

表 5-2. Pin Functions: TLV9051S

PIN		I/O	DESCRIPTION
NAME	**NO.**		
–IN	4	I	Inverting input
+IN	3	I	Noninverting input
OUT	1	O	Output
$\overline{\text{SHDN}}$	5	I	Shutdown: low = amp disabled, high = amp enabled. See *セクション 7.3.9* for more information.
V–	2	—	Negative (lowest) supply or ground (for single-supply operation).
V+	6	—	Positive (highest) supply

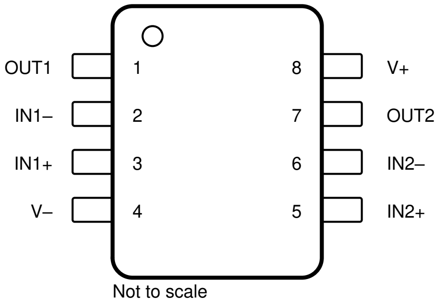
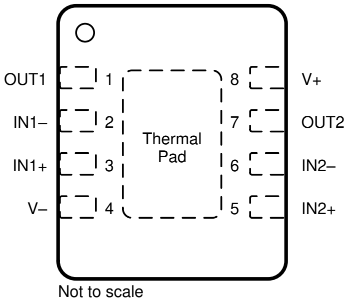


図 5-5. TLV9052 D, DGK, PW, DDF Packages 8-Pin SOIC, VSSOP, TSSOP, SOT-23 Top View



Connect exposed thermal pad to V–. See *セクション 7.3.6* for more information.

図 5-6. TLV9052 DSG Package 8-Pin WSON With Exposed Thermal Pad Top View

表 5-3. Pin Functions: TLV9052

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1–	2	I	Inverting input, channel 1
IN1+	3	I	Noninverting input, channel 1
IN2–	6	I	Inverting input, channel 2
IN2+	5	I	Noninverting input, channel 2
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
V–	4	—	Negative (low) supply or ground (for single-supply operation)
V+	8	—	Positive (high) supply

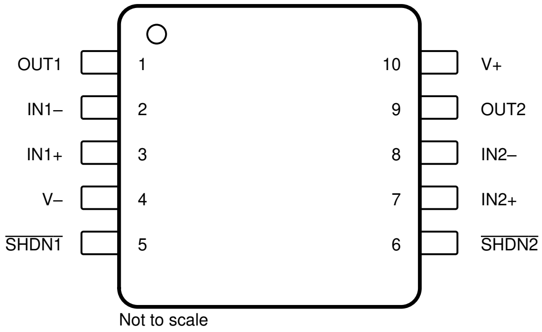


図 5-7. TLV9052S DGS Package 10-Pin VSSOP Top View

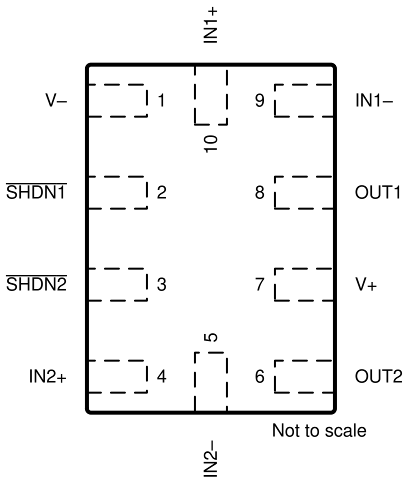


図 5-8. TLV9052S RUG Package 10-Pin X2QFN Top View

表 5-4. Pin Functions: TLV9052S

PIN			I/O	DESCRIPTION
NAME	VSSOP	X2QFN		
IN1–	2	9	I	Inverting input, channel 1
IN1+	3	10	I	Noninverting input, channel 1
IN2–	8	5	I	Inverting input, channel 2
IN2+	7	4	I	Noninverting input, channel 2
OUT1	1	8	O	Output, channel 1
OUT2	9	6	O	Output, channel 2
$\overline{\text{SHDN1}}$	5	2	I	Shutdown: low = amp disabled, high = amp enabled, channel 1. See *セクション 7.3.9* for more information.
$\overline{\text{SHDN2}}$	6	3	I	Shutdown: low = amp disabled, high = amp enabled, channel 2. See *セクション 7.3.9* for more information.
V–	4	1	—	Negative (low) supply or ground (for single-supply operation)
V+	10	7	—	Positive (high) supply

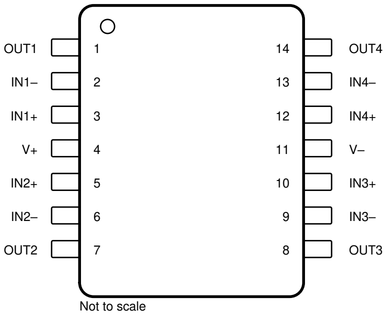


図 5-9. TLV9054 D, PW Packages 14-Pin SOIC, TSSOP Top View

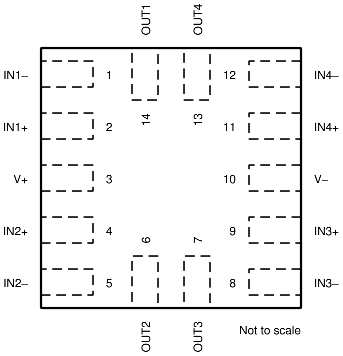
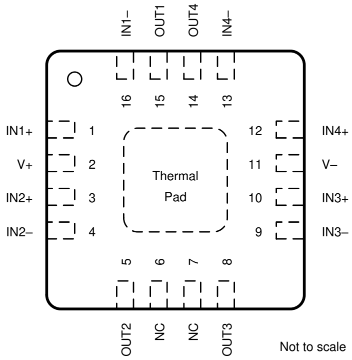


図 5-10. TLV9054 RUC Package 14-Pin X2QFN Top View

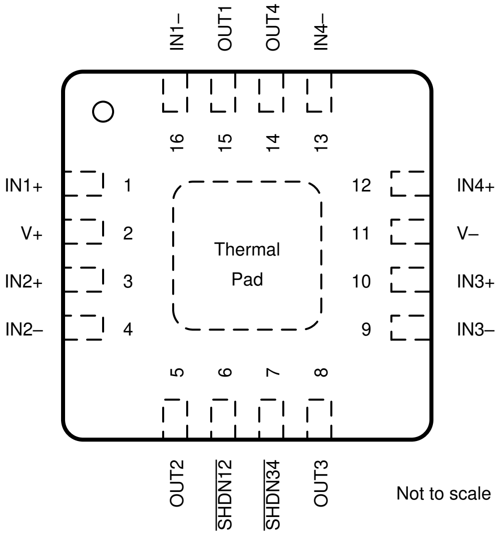


Connect exposed thermal pad to V–. See *セクション 7.3.6* for more information.

図 5-11. TLV9054 RTE Package 16-Pin WQFN With Exposed Thermal Pad Top View

表 5-5. Pin Functions: TLV9054

PIN				I/O	DESCRIPTION
NAME	SOIC, TSSOP	WQFN	X2QFN		
IN1–	2	16	1	I	Inverting input, channel 1
IN1+	3	1	2	I	Noninverting input, channel 1
IN2–	6	4	5	I	Inverting input, channel 2
IN2+	5	3	4	I	Noninverting input, channel 2
IN3–	9	9	8	I	Inverting input, channel 3
IN3+	10	10	9	I	Noninverting input, channel 3
IN4–	13	13	12	I	Inverting input, channel 4
IN4+	12	12	11	I	Noninverting input, channel 4
NC	—	6, 7	—	—	No internal connection
OUT1	1	15	14	O	Output, channel 1
OUT2	7	5	6	O	Output, channel 2
OUT3	8	8	7	O	Output, channel 3
OUT4	14	14	13	O	Output, channel 4
V–	11	11	10	—	Negative (low) supply or ground (for single-supply operation)
V+	4	2	3	—	Positive (high) supply



Connect exposed thermal pad to V–. See *セクション 7.3.6* for more information.

図 5-12. TLV9054S RTE Package 16-Pin WQFN With Exposed Thermal Pad Top View

表 5-6. Pin Functions: TLV9054S

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1+	1	I	Noninverting input, channel 1
IN1–	16	I	Inverting input, channel 1
IN2+	3	I	Noninverting input, channel 2
IN2–	4	I	Inverting input, channel 2
IN3+	10	I	Noninverting input, channel 3
IN3–	9	I	Inverting input, channel 3
IN4+	12	I	Noninverting input, channel 4
IN4–	13	I	Inverting input, channel 4
$\overline{\text{SHDN12}}$	6	I	Shutdown: low = amp disabled, high = amp enabled, channel 1 and 2. See *セクション 7.3.9* for more information.
$\overline{\text{SHDN34}}$	7	I	Shutdown: low = amp disabled, high = amp enabled, channel 3 and 4. See *セクション 7.3.9* for more information.
OUT1	15	O	Output, channel 1
OUT2	5	O	Output, channel 2
OUT3	8	O	Output, channel 3
OUT4	14	O	Output, channel 4
V–	11	—	Negative (low) supply or ground (for single-supply operation)
V+	2	—	Positive (high) supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)[1]

			MIN	MAX	UNIT
Supply voltage				7	V
Signal input pins	Voltage[2]	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential		(V+) – (V–) + 0.2	
	Current[2]		–10	10	mA
Output short-circuit[3]			Continuous		mA
Temperature	Specified, T_A		–40	125	°C
	Junction, T_J			150	
	Storage, T_{stg}		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Current limit input signals that can swing more than 0.5 V beyond the supply rails to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
TLV9051 X2SON PACKAGE				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1500	
ALL OTHER PACKAGES				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)	1.8	6.0	V
V_{IN}	Input pin voltage	(V–) – 0.1	(V+) + 0.1	V
	Specified temperature	–40	125	°C

6.4 Thermal Information for Single Channel

THERMAL METRIC[1]		TLV9051, TLV9051S					UNIT
		DPW (X2SON)	DBV (SOT-23)		DCK (SC70)	DRL (SOT553)[2]	
		5 PINS	5 PINS	6 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	470.0	228.1	210.8	231.2	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	211.9	152.1	152.1	144.4	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	334.8	97.7	92.3	78.6	TBD	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	29.8	74.1	76.2	51.3	TBD	°C/W

6.4 Thermal Information for Single Channel (続き)

THERMAL METRIC(1)		TLV9051, TLV9051S					UNIT
		DPW (X2SON)	DBV (SOT-23)		DCK (SC70)	DRL (SOT553) (2)	
		5 PINS	5 PINS	6 PINS	5 PINS	5 PINS	
Ψ_{JB}	Junction-to-board characterization parameter	333.2	97.3	92.1	78.3	TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	N/A	N/A	TBD	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) This package option is for preview only.

6.5 Thermal Information for Dual Channel

THERMAL METRIC(1)		TLV9052, TLV9052S							UNIT
		D (SOIC)	DGK (VSSOP)	DSG (WSON)	PW (TSSOP)	DDF (SOT-23)	DGS (VSSOP)	RUG (X2QFN)	
		8 PINS	8 PINS	8 PINS	8 PINS	8 PINS	10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	155.4	208.8	102.3	205.1	184.4	170.4	197.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	95.5	93.3	120.0	93.7	112.8	84.9	93.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	98.9	130.7	68.2	135.7	99.9	113.5	123.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	41.9	26.1	15.1	25.0	18.7	16.4	3.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	98.1	128.9	68.2	134.0	99.3	112.3	120.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	43.6	N/A	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Thermal Information for Quad Channel

THERMAL METRIC(1)		TLV9054, TLV9054S					UNIT
		D (SOIC)	PW (TSSOP)	RTE (WQFN)		RUC (X2SQFN)	
		14 PINS	14 PINS	14 PINS	16 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	115.0	147.2	65.5	65.6	209.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	71.1	67.2	70.6	70.6	68.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	71.0	91.6	40.5	40.5	153.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	29.7	16.6	5.8	5.8	3.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	70.6	90.7	40.5	40.5	152.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	24.5	24.5	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.7 Electrical Characteristics: V_S (Total Supply Voltage) = (V+) – (V–) = 1.8 V to 5.5 V

at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted);

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = 5 V		±0.33	±1.6	mV
		V_S = 5 V, T_A = –40°C to +125°C			±2	
dV_{OS}/dT	Drift	V_S = 5 V, T_A = –40°C to +125°C		±0.5		μV/°C
PSRR	Power-supply rejection ratio	V_S = 1.8 V – 5.5 V, V_{CM} = (V–)		±13	±80	μV/V
	Channel separation, dc	At dc		115		dB
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage	V_S = 1.8 V to 5.5 V	(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	V_S = 5.5 V, (V–) – 0.1 V < V_{CM} < (V+) – 1.4 V, T_A = –40°C to +125°C	80	96		dB
		V_S = 5.5 V, V_{CM} = –0.1 V to 5.6 V, T_A = –40°C to +125°C	62	79		
		V_S = 1.8 V, (V–) – 0.1 V < V_{CM} < (V+) – 1.4 V, T_A = –40°C to +125°C		88		
		V_S = 1.8 V, V_{CM} = –0.1 V to 1.9 V, T_A = –40°C to +125°C		72		
INPUT BIAS CURRENT						
I_B	Input bias current			±2	±18(2)	pA
		T_A = –40°C to +125°C			±525(2)	pA
I_{OS}	Input offset current			±1	±15(2)	pA
		T_A = –40°C to +125°C			±440(2)	pA
NOISE						
E_n	Input voltage noise (peak-to-peak)	V_S = 5 V, f = 0.1 Hz to 10 Hz		6		μV_{PP}
e_n	Input voltage noise density	V_S = 5 V, f = 10 kHz		15		nV/√Hz
		V_S = 5 V, f = 1 kHz		20		nV/√Hz
i_n	Input current noise density	f = 1 kHz		18		fA/√Hz
INPUT CAPACITANCE						
C_{ID}	Differential			2		pF
C_{IC}	Common-mode			4		pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	V_S = 1.8 V, (V–) + 0.04 V < V_O < (V+) – 0.04 V, R_L = 10 kΩ		106		dB
		V_S = 5.5 V, (V–) + 0.05 V < V_O < (V+) – 0.05 V, R_L = 10 kΩ	104	128		
		V_S = 1.8 V, (V–) + 0.06 V < V_O < (V+) – 0.06 V, R_L = 2 kΩ		108		
		V_S = 5.5 V, (V–) + 0.15 V < V_O < (V+) – 0.15 V, R_L = 2 kΩ		130		
FREQUENCY RESPONSE						
GBP	Gain bandwidth product	V_S = 5.5 V, G = +1		5		MHz
φ_m	Phase margin	V_S = 5.5 V, G = +1		60		Degrees
SR	Slew rate	V_S = 5.5 V, G = +1, C_L = 130pF		15		V/μs
t_S	Settling time	To 0.1%, V_S = 5.5 V, 2-V step , G = +1, C_L = 100 pF		0.75		μs
		To 0.01%, V_S = 5.5 V, 2-V step , G = +1, C_L = 100 pF		1		
t_{OR}	Overload recovery time	V_S = 5.5 V, V_{IN} × gain > V_S		0.3		μs
THD + N	Total harmonic distortion + noise(1)	V_S = 5.5 V, V_{CM} = 2.5 V, V_O = 1 V_{RMS}, G = +1, f = 1 kHz		0.0006%		
OUTPUT						

6.7 Electrical Characteristics: V_S (Total Supply Voltage) = (V+) – (V–) = 1.8 V to 5.5 V (続き)

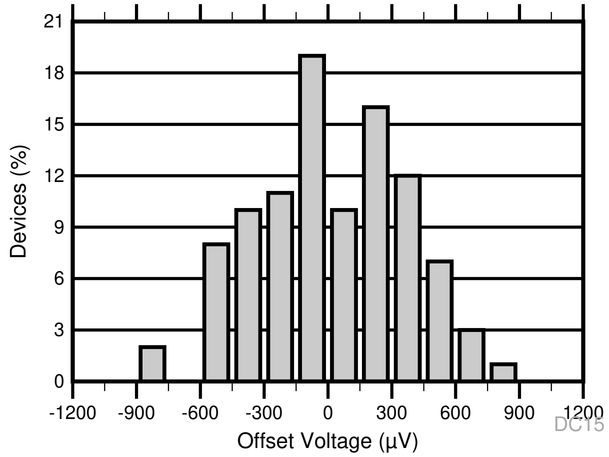
at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted);

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Voltage output swing from supply rails	V_S = 5.5 V, R_L = 10 kΩ,			16	mV
		V_S = 5.5 V, R_L = 2 kΩ,			40	
I_{SC}	Short-circuit current	V_S = 5 V		±50		mA
Z_O	Open-loop output impedance	V_S = 5 V, f = 5 MHz		250		Ω
POWER SUPPLY						
I_Q	Quiescent current per amplifier	V_S = 5.5 V, I_O = 0 mA,		330	450	µA
		V_S = 5.5 V, I_O = 0 mA, T_A = –40°C to +125°C			475	
SHUTDOWN						
I_{QSD}	Quiescent current per amplifier	V_S = 1.8 to 5.5 V, all amplifiers disabled, SHDN = V-		0.35	1	µA
Z_{SHDN}	Output impedance	V_S = 1.8 to 5.5 V, amplifier disabled		10 || 2		GΩ || pF
	High-level voltage shutdown threshold (amplifier enabled)	V_S = 1.8 to 5.5 V		(V-) + 0.9	(V-) + 1.1	V
	Low-loevel voltage shutdown threshold (amplifeir disabled)	V_S = 1.8 to 5.5 V	(V-) + 0.2	(V-) + 0.7		V
t_{ON}	Amplifier enabled time (full shutdown [3] [4]			35		µS
t_{ON}	Amplifier enabled time (partial shutdown) [3] [4]			10		µS
t_{OFF}	Amplifier diabled time [3]			6		µS
	SHDN pin input bias current (per pin)	V_S = 1.8 V to 5.5 V, V+ ≥ (V+) - 0.8 V		6.5		nA
	SHDN pin input bias current (per pin)	V_S = 1.8 V to 5.5 V, V+ ≤ (V-) + 0.8 V		155		nA

(1) Third-order filter; bandwidth = 80 kHz at –3 dB.
(2) Specified by design and characterization; not production tested.
(3) Disable time (t_{OFF}) and enable time (t_{ON}) are defined as the time interval between the 50% point of the signal applied to the SHDN pin and the point at which the output voltage reaches the 10% (disable) or 90% (enable) level.
(4) Full shutdown refers to the dual TLV9052S having both channels 1 and 2 disabled (SHDN1 = SHDN2 = V–) and the quad TLV9054S having all channels 1 to 4 disabled (SHDN12 = SHDN34 = V–). For partial shutdown, only one SHDN pin is exercised; in this mode, the internal biasing circuitry remains operational and the enable time is shorter.

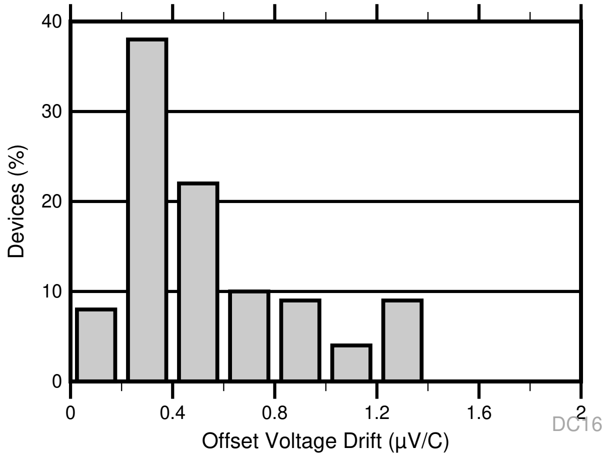
6.8 Typical Characteristics

at T_A = 25°C, V_S = 5.5V, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



V_S = 5.5V

図 6-1. Offset Voltage Production Distribution



V_S = 5.5V, T_A = –40°C to 125°C

図 6-2. Offset Voltage Drift Distribution

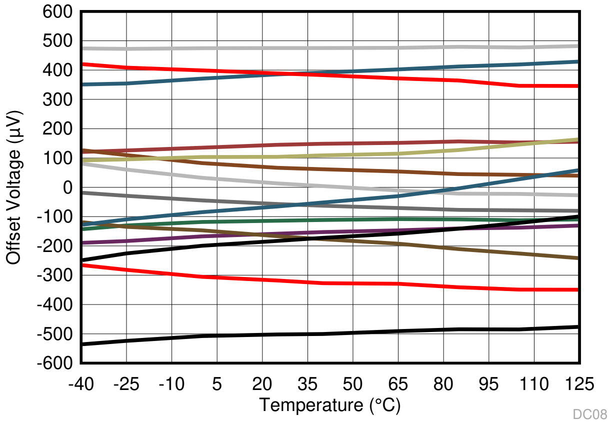


図 6-3. Offset Voltage vs Temperature

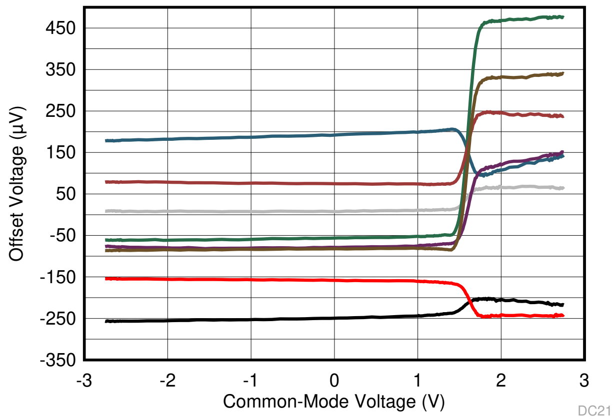


図 6-4. Offset Voltage vs Common-Mode Voltage

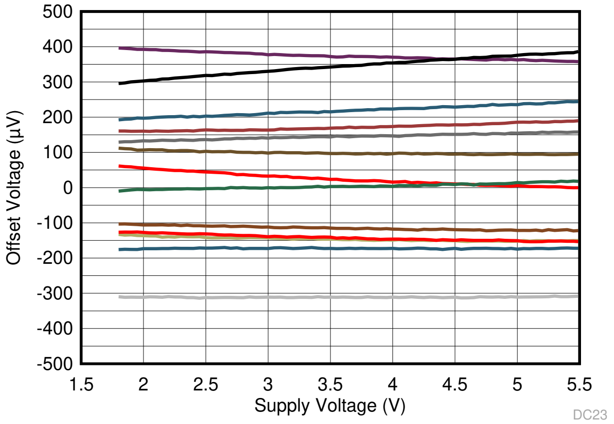


図 6-5. Offset Voltage vs Power Supply

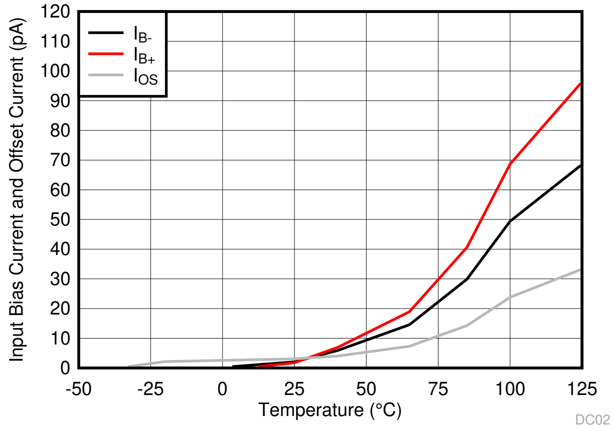


図 6-6. Input Bias Current vs Temperature

6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5V, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

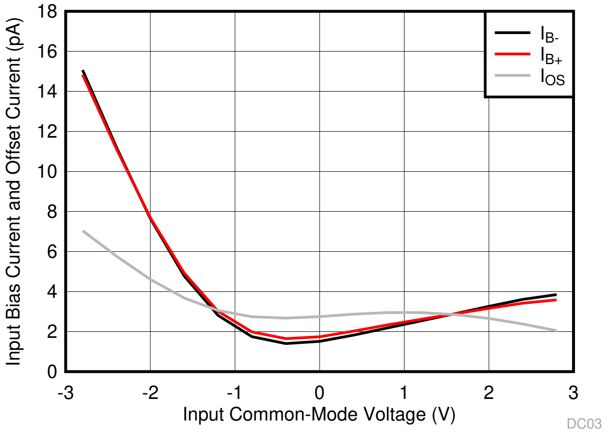


図 6-7. Input Bias Current and Offset Current vs Common-Mode Voltage

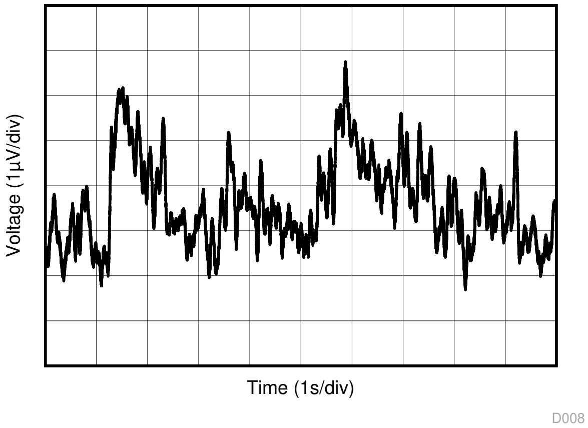


図 6-8. 0.1-Hz to 10-Hz Input Voltage Noise

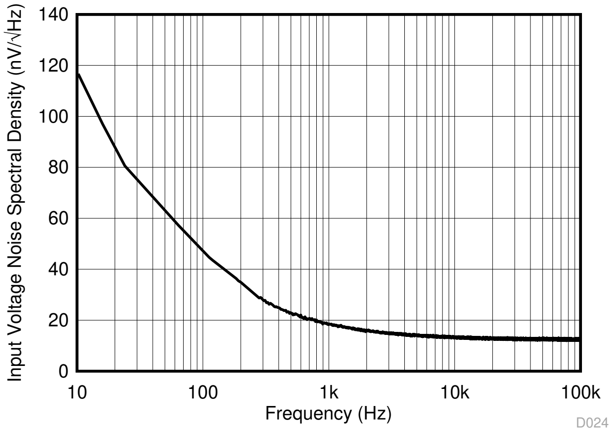


図 6-9. Input Voltage Noise Spectral Density vs Frequency

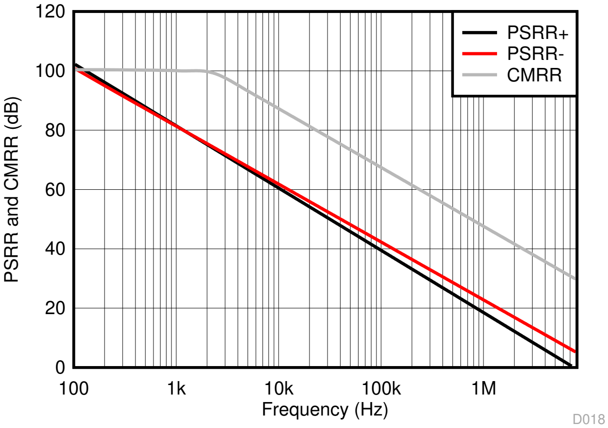


図 6-10. CMRR and PSRR vs Frequency (Referred to Input)

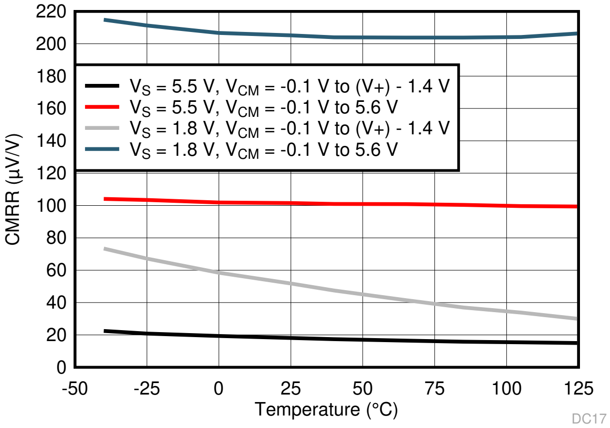
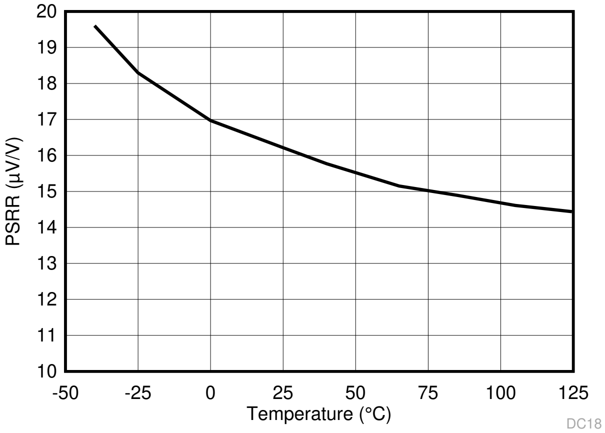


図 6-11. CMRR vs Temperature



V_S = 1.8V to 5.5V

図 6-12. PSRR vs Temperature

6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5V, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

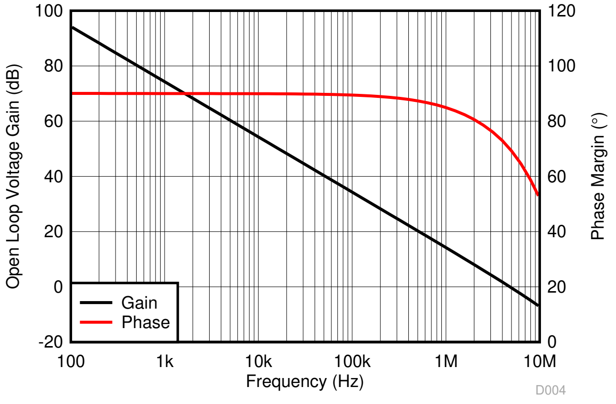


図 6-13. Open Loop Voltage Gain and Phase vs Frequency

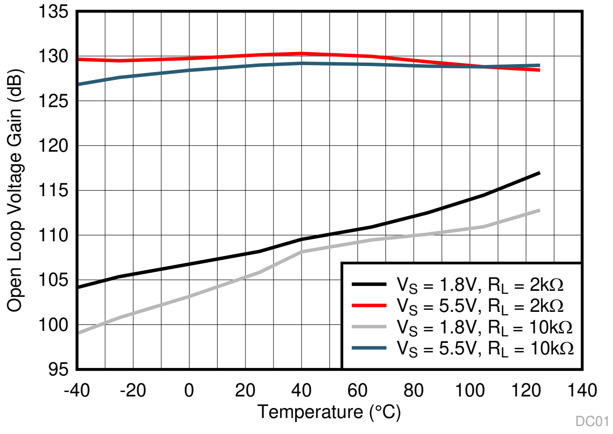


図 6-14. Open Loop Voltage Gain vs Temperature

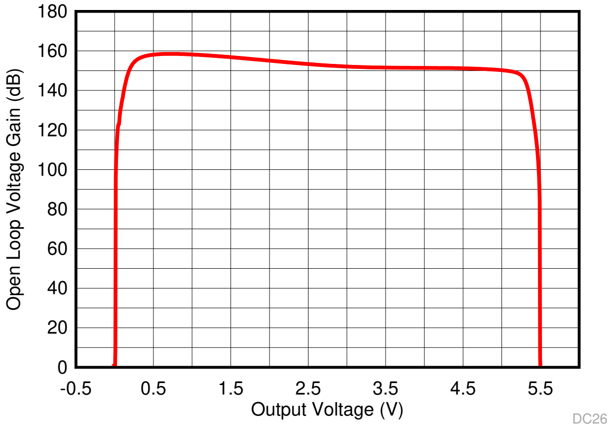


図 6-15. Open Loop Voltage Gain vs Output Voltage

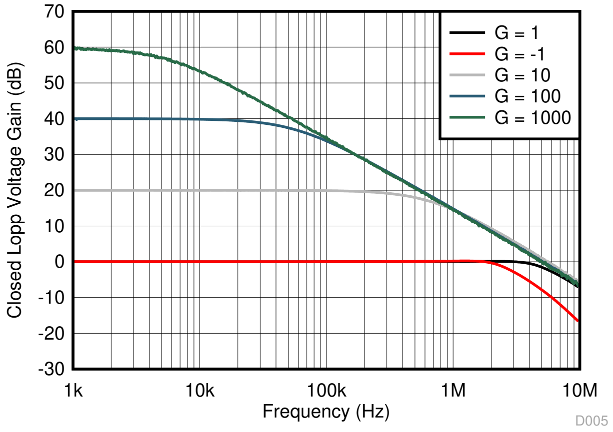


図 6-16. Closed Loop Voltage Gain vs Frequency

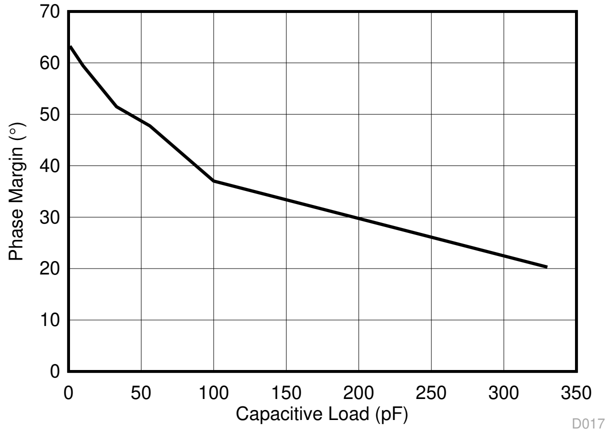


図 6-17. Phase Margin vs Capacitive Load

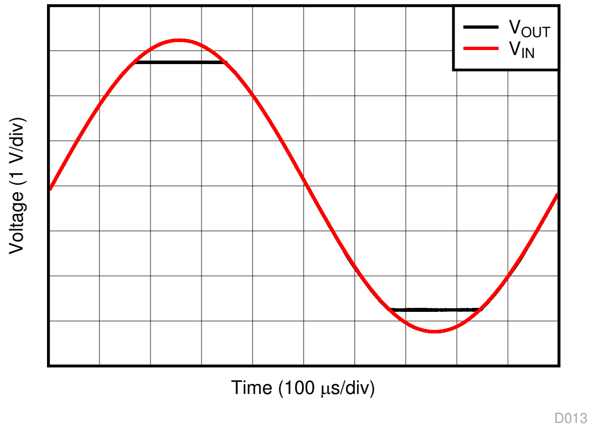
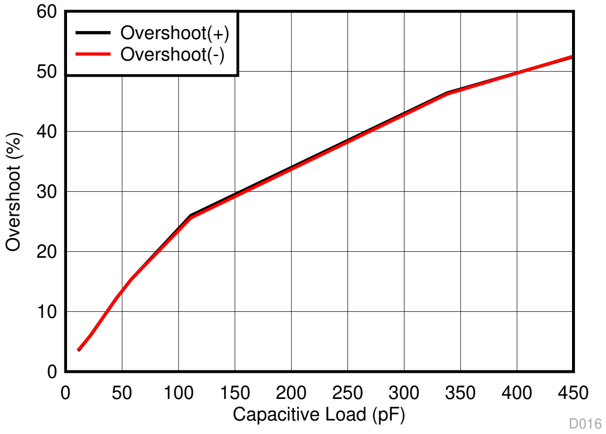


図 6-18. No Phase Reversal

6.8 Typical Characteristics (continued)

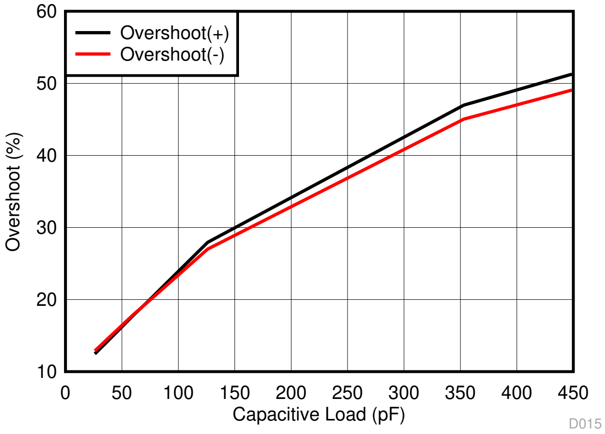
at T_A = 25°C, V_S = 5.5V, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



G = +1V/V

V_{OUT} step = 100mV_{p-p}

図 6-19. Small-Signal Overshoot vs Load Capacitance



G = –1V/V

V_{OUT} step = 100mV_{p-p}

図 6-20. Small-Signal Overshoot vs Load Capacitance

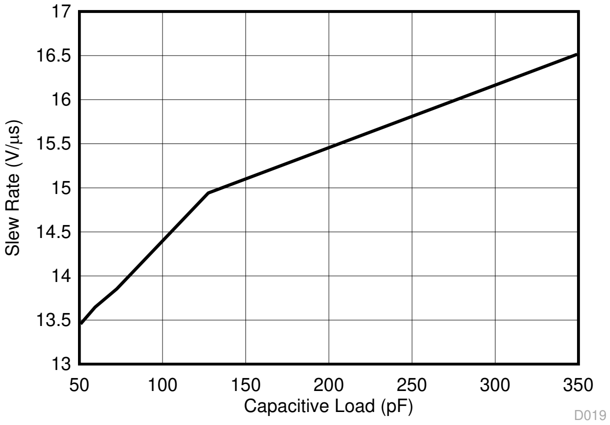
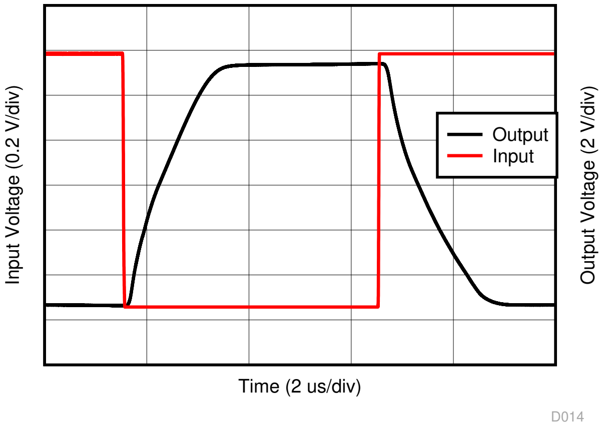


図 6-21. Slew Rate vs Capacitive Load

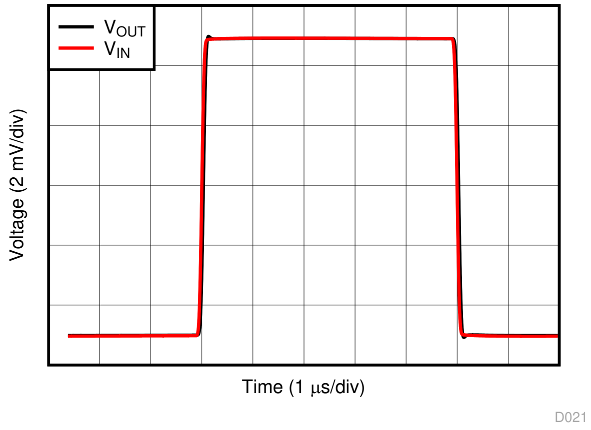


G = –10V/V

図 6-22. Overload Recovery

6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5V, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

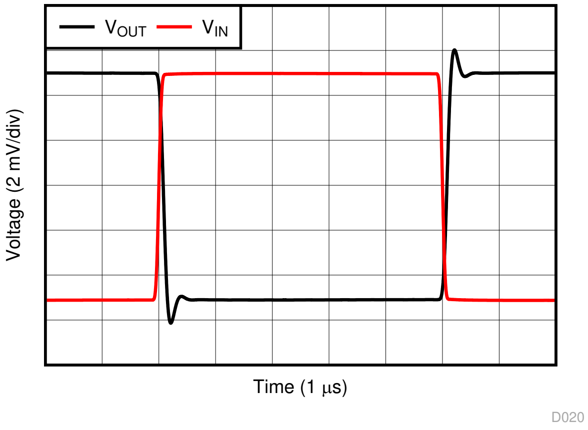


G = +1V/V

V_{OUT} step = 10mV$_{p-}$

p

図 6-23. Small-Signal Step Response

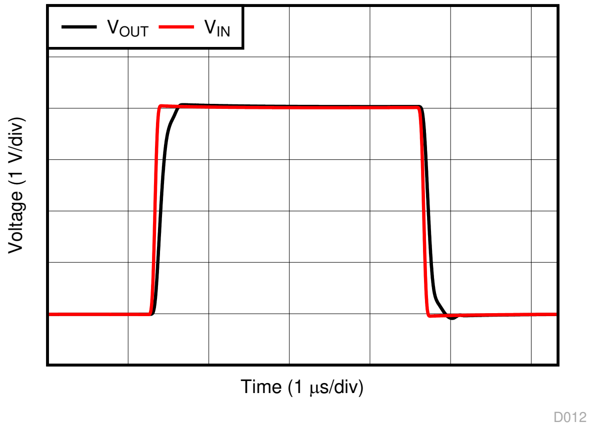


G = –1V/V

V_{OUT} step = 10mV$_{p-}$

p

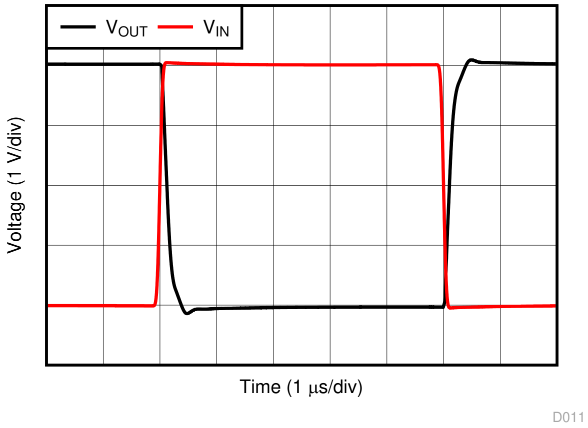
図 6-24. Small-Signal Step Response



G = +1V/V

V_{OUT} step = 4$V_{p\text{-}p}$

図 6-25. Large-Signal Step Response



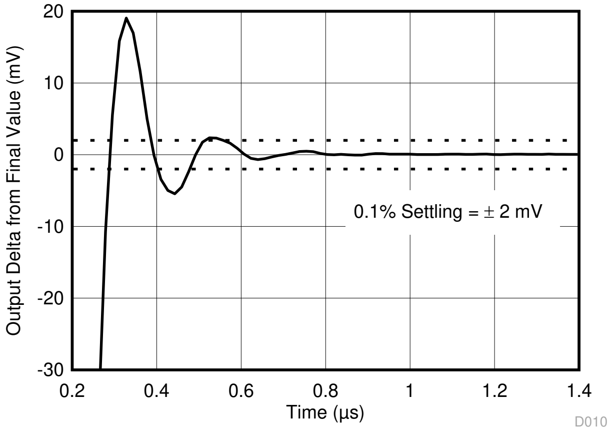
G = –1V/V

V_{OUT} step = 4$V_{p\text{-}p}$

図 6-26. Large-Signal Step Response

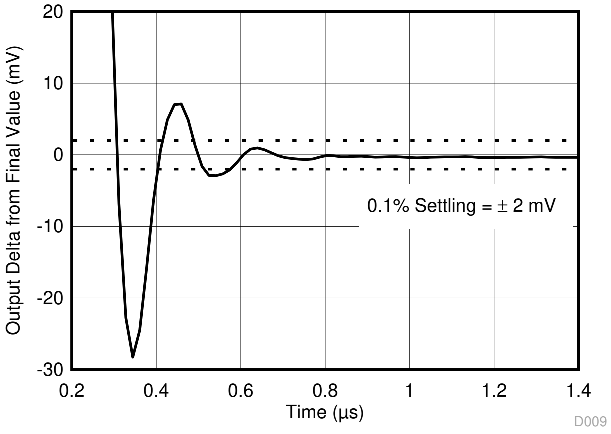
6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5V, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



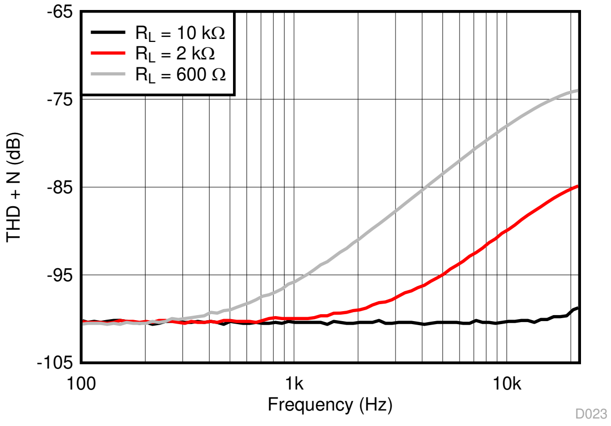
C_L = 100pF G = +1V/V

図 6-27. Positive Large-Signal Settling Time



C_L = 100pF G = +1V/V

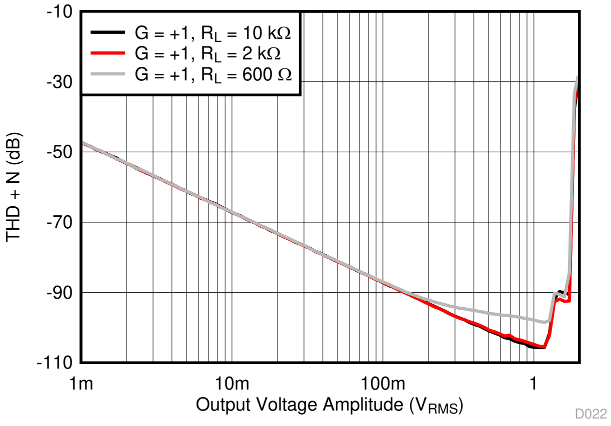
図 6-28. Negative Large-Signal Settling Time



V_{OUT} = 0.5V_{RMS} G = +1 V_{CM} = 2.5V

BW = 80kHz

図 6-29. THD + N vs Frequency



f = 1kHz G = +1 V_{CM} = 2.5V

BW = 80kHz

図 6-30. THD + N vs Amplitude

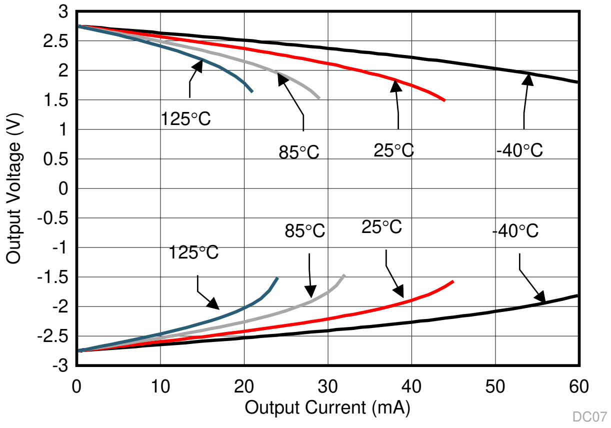


図 6-31. Output Voltage Swing vs Output Current

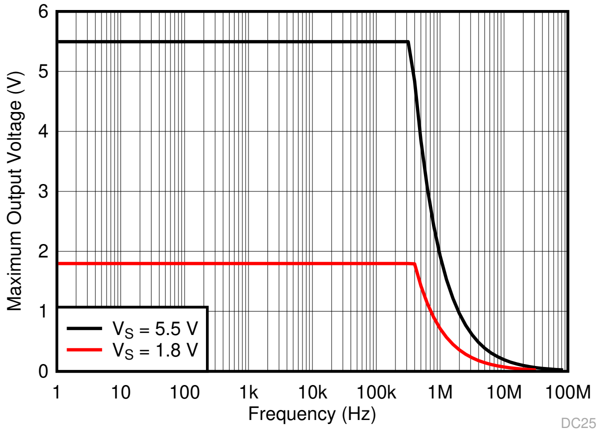


図 6-32. Maximum Output Voltage vs Frequency and Supply Voltage

6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5V, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

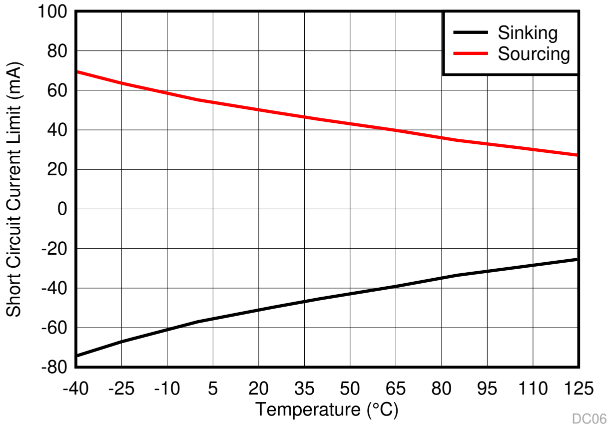


図 6-33. Short-Circuit Current vs Temperature

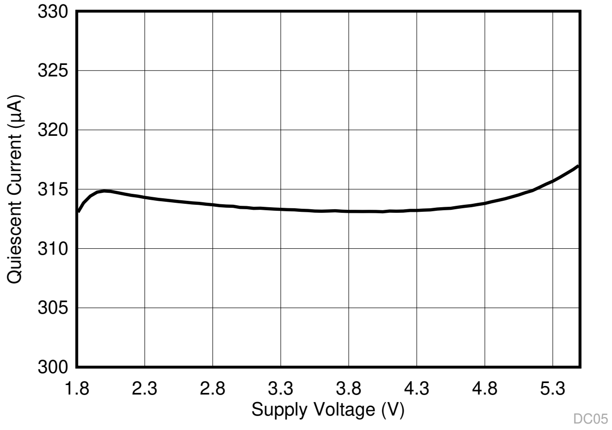


図 6-34. Quiescent Current vs Supply Voltage

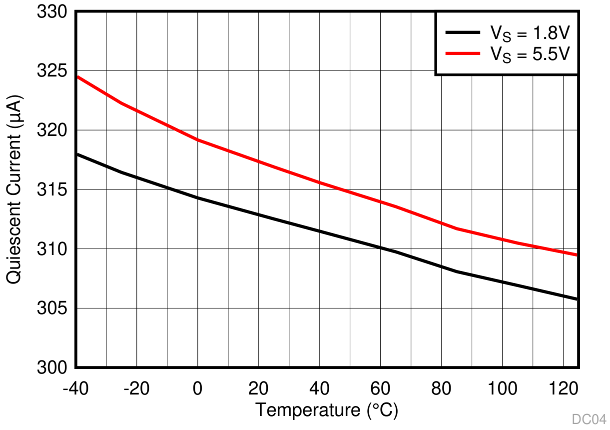


図 6-35. Quiescent Current vs Temperature

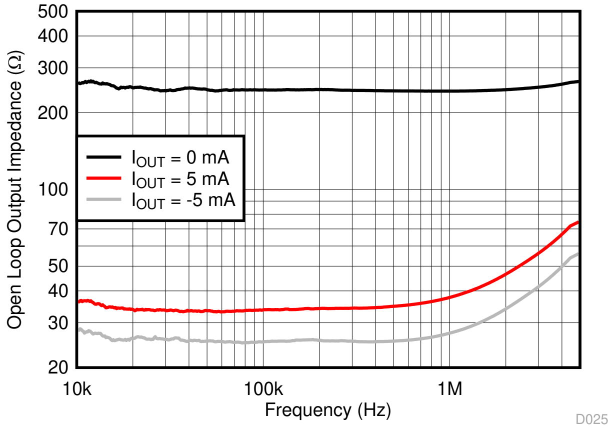
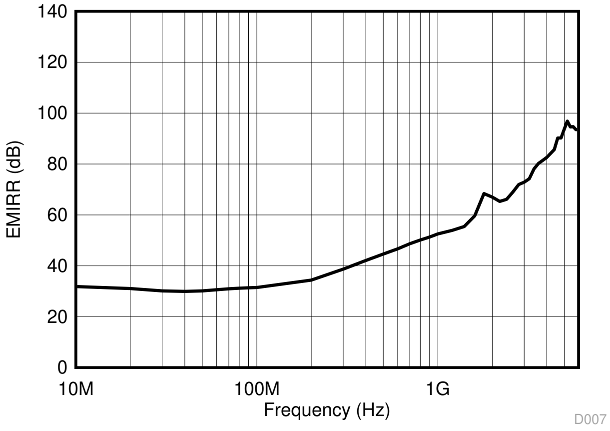
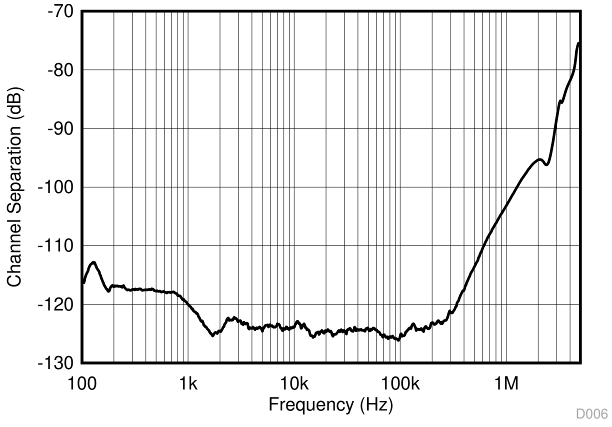


図 6-36. Open-Loop Output Impedance vs Frequency



P_{RF} = –10dBm

図 6-37. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR+) vs Frequency



P_{RF} = –10dBm

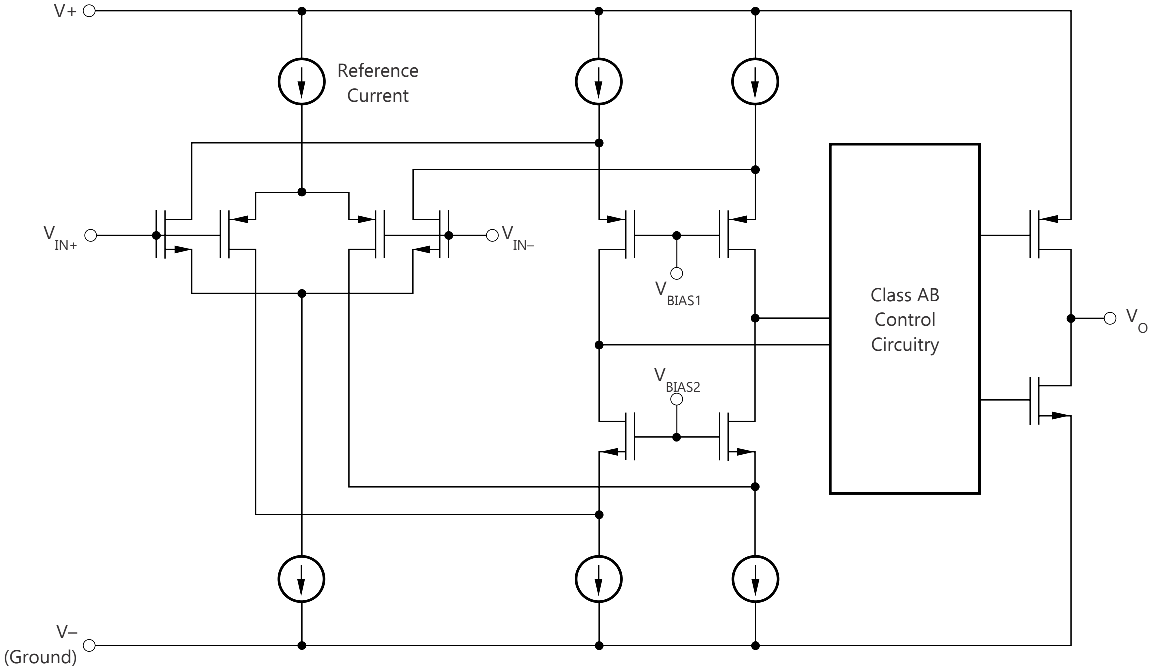
図 6-38. Channel Separation vs Frequency

7 Detailed Description

7.1 Overview

The TLV905x devices are a 5MHz family of low-power, rail-to-rail input and output op amps. These devices operate from 1.8V to 5.5V, are unity-gain stable, and are designed for a wide range of general-purpose applications. The input common-mode voltage range includes both rails and allows the TLV905x family to be used in virtually any single-supply application. The unique combination of a high slew rate and low quiescent current makes this family a potential choice for battery-powered motor-drive applications. Rail-to-rail input and output swing significantly increase dynamic range, especially in low-supply applications.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Voltage

The TLV905x family of op amps is specified for operation from 1.8V to 6.0V. In addition, many specifications apply from –40°C to 125°C. Parameters that vary significantly with operating voltages or temperature are illustrated in the *セクション 6.8*.

7.3.2 Rail-to-Rail Input

The input common-mode voltage range of the TLV905x family extends 100mV beyond the supply rails for the full supply voltage range of 1.8V to 6.0V. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair, as shown in the *セクション 7.2*. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1.4V to 200mV above the positive supply, whereas the P-channel pair is active for inputs from 200mV below the negative supply to approximately (V+) – 1.4V. There is a small transition region, typically (V+) – 1.2V to (V+) – 1V, in which both pairs are on. This 200-mV transition region can vary up to 200mV with process variation. Thus, the transition region (with both stages on) can range from (V+) – 1.4V to (V+) – 1.2V on the low end, and up to (V+) – 1V to (V+) – 0.8V on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can degrade compared to device operation outside this region.

7.3.3 Rail-to-Rail Output

Designed as low-power, low-voltage operational amplifiers, the TLV905x family delivers a robust output drive capability. A class AB output stage with common-source transistors achieves full rail-to-rail output swing capability. For resistive loads of 10kΩ, the output swings to within 16mV of either supply rail, regardless of the applied power-supply voltage. Different load conditions change the ability of the amplifier to swing close to the rails.

7.3.4 EMI Rejection

The TLV905x uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the TLV905x benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10MHz to 6GHz. 図 7-1 shows the results of this testing on the TLV905x. 表 7-1 shows the EMIRR IN+ values for the TLV905x at particular frequencies commonly encountered in real-world applications. The *EMI Rejection Ratio of Operational Amplifiers* application report contains detailed information on the topic of EMIRR performance as it relates to op amps and is available for download from www.ti.com.

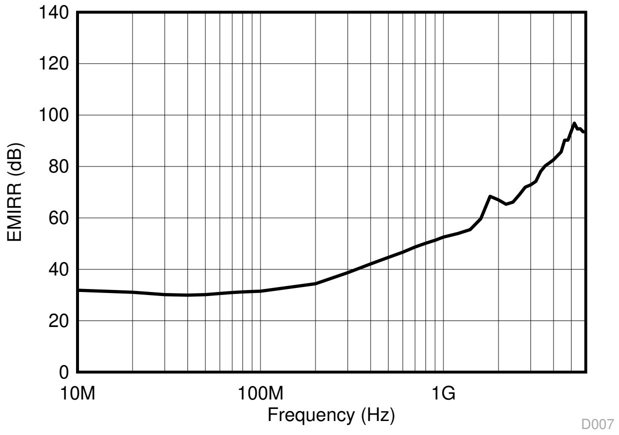


図 7-1. EMIRR Testing

表 7-1. TLV905x EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	41.8dB
900MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6GHz), GSM, aeronautical mobile, UHF applications	53.1dB
1.8GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1GHz to 2GHz)	71.8dB
2.4GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2GHz to 4GHz)	70.0dB
3.6GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	81.2dB
5GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4GHz to 8GHz)	92.5dB

7.3.5 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the rated operating voltage, because of the high input voltage or high gain. After the device enters the saturation region, the output devices require time to return to the linear operating state. After the output devices return to their linear operating state, the device begins to slew at the specified slew rate. Therefore, the propagation delay (in case of an overload condition) is the sum of the overload recovery time and the slew time. The overload recovery time for the TLV905x family is approximately 300 ns.

7.3.6 Packages With an Exposed Thermal Pad

The TLV905x family is available in packages such as the WSON-8 (DSG) and WQFN-16 (RTE) which feature an exposed thermal pad. Inside the package, the die is attached to this thermal pad using an electrically conductive compound. For this reason, when using a package with an exposed thermal pad, the thermal pad must either be connected to V– or left floating. Attaching the thermal pad to a potential other then V– is not allowed, and the performance of the device is not verified when doing so.

7.3.7 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. 図 7-2 shows the ESD circuits contained in the TLV905x devices. The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power supply lines, where they meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

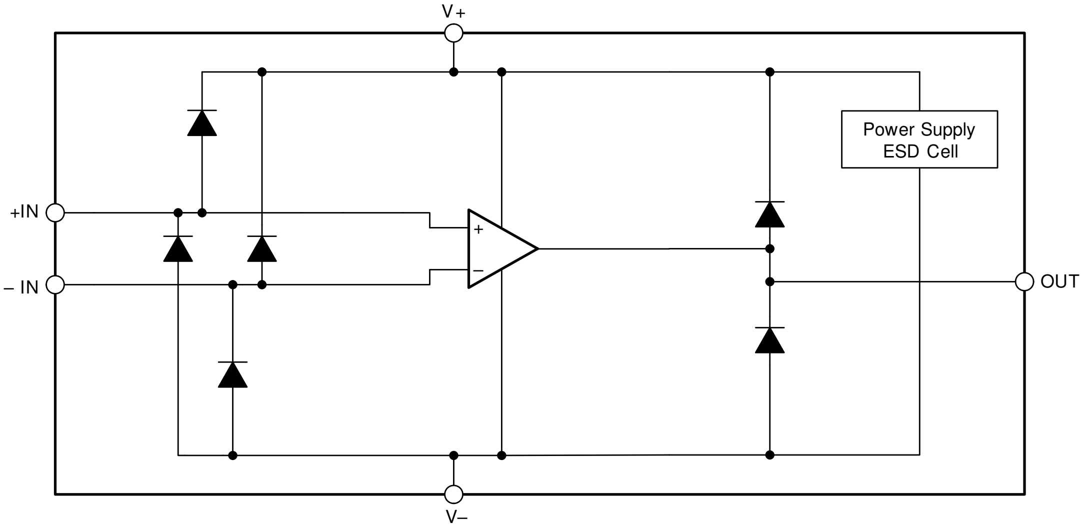


図 7-2. Equivalent Internal ESD Circuitry

7.3.8 Input Protection

The TLV905x family incorporates internal ESD protection circuits on all pins. For input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes provide in-circuit, input overdrive protection, as long as the current is limited to 10mA, as shown in the *セクション 6.1*. 図 7-3 shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value must be kept to a minimum in noise-sensitive applications.

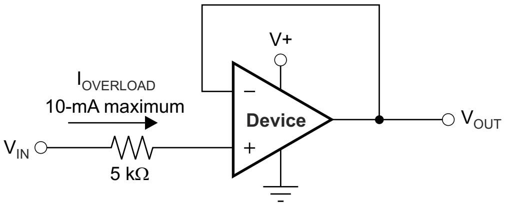


図 7-3. Input Current Protection

7.3.9 Shutdown Function

The TLV905xS devices feature $\overline{\text{SHDN}}$ pins that disable the op amp, placing the device into a low-power standby mode. In this mode, the op amp consumes 1µA of maximum quiescent current, referred to as I_{QSD}. The $\overline{\text{SHDN}}$ pins are active low, meaning that shutdown mode is enabled when the input to the $\overline{\text{SHDN}}$ pin is a valid logic low.

The $\overline{\text{SHDN}}$ pins are referenced to the negative supply voltage of the op amp. The threshold of the shutdown feature lies around 800mV (typical) and does not change with respect to the supply voltage. Hysteresis has been included in the switching threshold for smooth switching characteristics. For shutdown behavior, the $\overline{\text{SHDN}}$ pins should be driven with valid logic signals. A valid logic low is defined as a voltage between V– and V– + 0.4V. A valid logic high is defined as a voltage between V– + 1.2V and V+. The shutdown pin circuitry includes a pull-up resistor, which will inherently pull the voltage of the pin to the positive supply rail if not driven. Thus, to enable the amplifier, the $\overline{\text{SHDN}}$ pins must either be left floating or driven to a valid logic high. To disable the amplifier, the $\overline{\text{SHDN}}$ pins must be driven to a valid logic low .While TI highly recommends that the shutdown pin be connected to a valid high or a low voltage or driven, TI has included a pull-up resistor connected to VCC. The maximum voltage allowed at the $\overline{\text{SHDN}}$ pins is (V+) + 0.5V. Exceeding this voltage level will damage the device.

The $\overline{\text{SHDN}}$ pins are high-impedance CMOS inputs. Dual op amp versions are independently controlled and quad op amp versions are controlled in pairs with logic inputs. For battery-operated applications, this feature may be used to greatly reduce the average current and extend battery life. The enable time is 35 µs for full shutdown of all channels; disable time is 6 µs. When disabled, the output assumes a high-impedance state. This architecture allows the TLV905xS to be operated as a gated amplifier (or to have the device output multiplexed onto a common analog output bus). Shutdown time (t_{OFF}) depends on loading conditions and increases as load resistance increases. For shutdown (disable) within a specific shutdown time, the specified 10kΩ load to midsupply (V_S / 2) is required. If using the TLV905xS without a load, the resulting turnoff time is significantly increased.

7.4 Device Functional Modes

The TLV905x family is operational when the power-supply voltage is between 1.8V (±0.9V) and 6.0V (±3.0V).

The TLV905xS devices feature a shutdown mode and are shutdown when a valid logic low is applied to the shutdown pin.

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The TLV905x family features 5MHz bandwidth and very high slew rate of 15V/µs with only 330µA of supply current per channel, providing excellent AC performance at very low-power consumption. DC applications are well served with a very low input noise voltage of $15nV/\sqrt{Hz}$ at 10kHz, low input bias current, and a typical input offset voltage of 0.33mV.

8.2 Typical Low-Side Current Sense Application

図 8-1 shows the TLV905x configured in a low-side current sensing application.

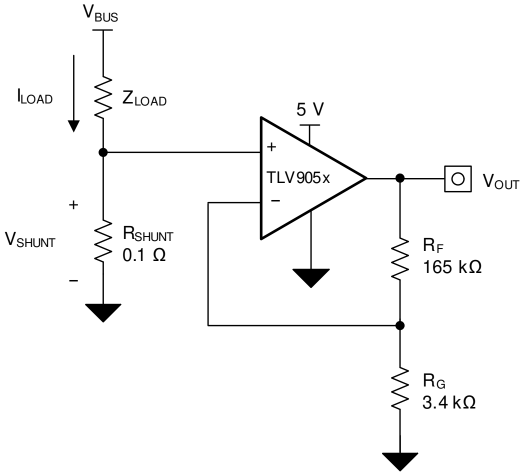


図 8-1. TLV905x in a Low-Side, Current-Sensing Application

8.2.1 Design Requirements

The design requirements for this design are:

- Load current: 0A to 1A
- Output voltage: 4.95V
- Maximum shunt voltage: 100mV

8.2.2 Detailed Design Procedure

The transfer function of the circuit in 図 8-1 is given in 式 1.

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times Gain \tag{1}$$

The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0A to 1A. To keep the shunt voltage below 100mV at maximum load current, the largest shunt resistor is defined using 式 2.

$$R_{SHUNT} = \frac{V_{SHUNT\_MAX}}{I_{LOAD\_MAX}} = \frac{100\ mV}{1\ A} = 100\ m\Omega \tag{2}$$

Using 式 2, R_{SHUNT} equals 100 mΩ. The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the TLV905x device to produce an output voltage of approximately 0V to 4.95V. 式 3 calculates the gain required for the TLV905x device to produce the required output voltage.

$$Gain = \frac{(V_{OUT\_MAX} - V_{OUT_{MIN}})}{(V_{IN\_MAX} - V_{IN\_MIN})} \tag{3}$$

Using 式 3, the required gain equals 49.5V/V, which is set with the R_F and R_G resistors. 式 4 sizes the R_F and R_G, resistors to set the gain of the TLV905x device to 49.5V/V.

$$Gain = 1 + \frac{(R_F)}{(R_G)} \tag{4}$$

Selecting R_F to equal 165kΩ and R_G to equal 3.4kΩ provides a combination that equals approximately 49.5V/V. 図 8-2 shows the measured transfer function of the circuit shown in 図 8-1.

8.2.3 Application Curve

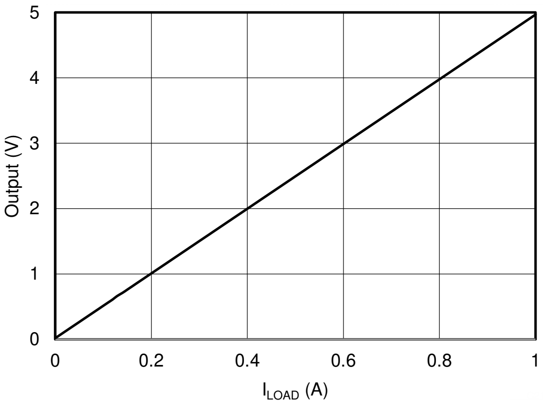


図 8-2. Low-Side, Current-Sense Transfer Function

8.3 Power Supply Recommendations

The TLV905x family is specified for operation from 1.8V to 6.0V (±0.9V to ±3.0V); many specifications apply from –40°C to 125°C. The *セクション 6.8* section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

> 注意
>
> Supply voltages larger than 7V can permanently damage the device; see the *セクション 6.1* table.

Place 0.1µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more-detailed information on bypass capacitor placement, see the *セクション 8.4.2* section.

8.4 Layout

8.4.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and of the op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see *Circuit Board Layout Techniques*.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in 図 8-4, keeping R_F and R_G close to the inverting input minimizes parasitic capacitance on the inverting input.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

8.4.2 Layout Example

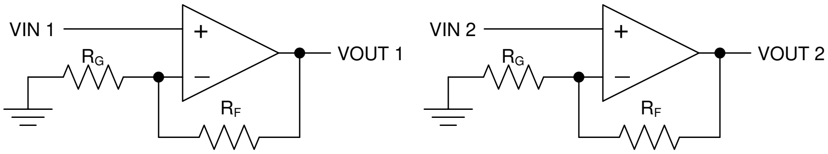


図 8-3. Schematic Representation for *Figure 8-4*

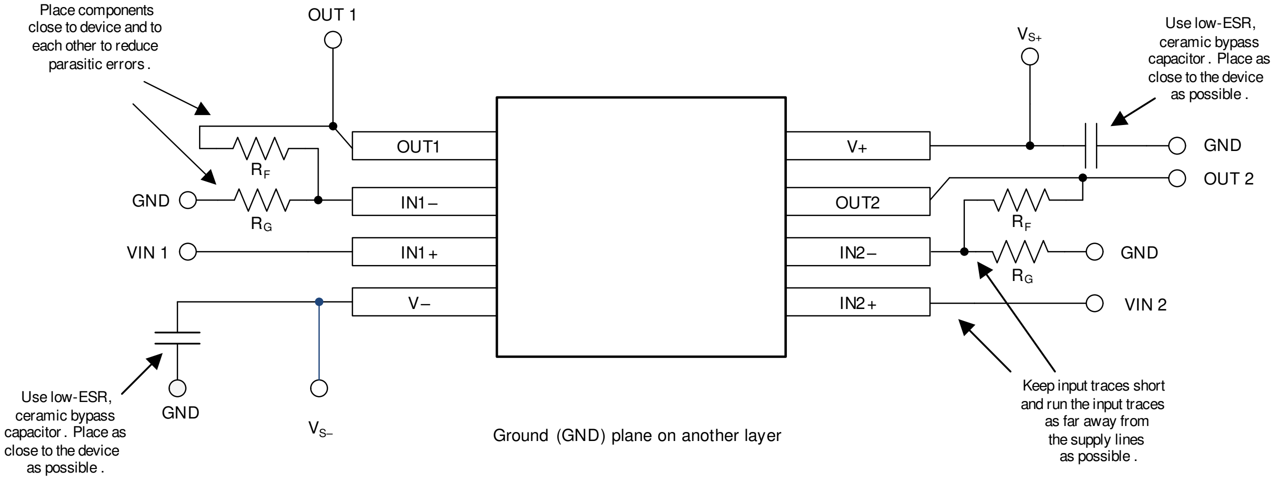


図 8-4. Layout Example

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *TLVx313 Low-Power, Rail-to-Rail In/Out, 500-μV Typical Offset, 1MHz Operational Amplifier for Cost-Sensitive Systems*
- Texas Instruments, *TLVx314 3MHz, Low-Power, Internal EMI Filter, RRIO, Operational Amplifier*
- Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers*
- Texas Instruments, *QFN/SON PCB Attachment*
- Texas Instruments, *Quad Flatpack No-Lead Logic Packages*
- Texas Instruments, *Circuit Board Layout Techniques*
- Texas Instruments, *Single-Ended Input to Differential Output Conversion Circuit Reference Design*

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

9.4 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.
Bluetooth® is a registered trademark of Bluetooth SIG, Inc.
すべての商標は、それぞれの所有者に帰属します。

9.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.6 用語集

テキサス・インスツルメンツ用語集	この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision I (November 2022) to Revision J (February 2024) **Page**

- Changed pins 3 and 4 the TLV9051S DBV pin diagram.. 3
- Added shutdown section into the Electrical Characteristics table...11

Changes from Revision H (October 2019) to Revision I (November 2022)	Page
• Increased maximum supply voltage in *Absolute Maximum Ratings* from 6 V to 7 V	9
• Added maximum limits for input bias current and input offset current	11

Changes from Revision G (September 2019) to Revision H (October 2019)	Page
• Added new human-body model and charged-device model ratings for TLV9051 X2SON package to the *ESD Ratings*	9
• Added *Packages With an Exposed Thermal Pad* section to *Feature Description* section	22

Changes from Revision F (June 2019) to Revision G (September 2019)	Page
• すべての TLV9051 パッケージのプレビュー タグを削除	1
• TLV9052 SOT-23 (8) - DDF パッケージのプレビュー タグを削除	1
• Added link to *Shutdown Function* section in all of the $\overline{\text{SHDN}}$ pin function rows	3
• Added *EMI Rejection* section to *Feature Description* section	21
• Added clarification to the *Shutdown Function* section	23

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、テキサス・インスツルメンツの販売条件、または ti.com やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用されるテキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV9051IDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	T51D
TLV9051IDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T51D
TLV9051IDCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	T51
TLV9051IDCKR.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	T51
TLV9051IDPWR	Active	Production	X2SON (DPW) | 5	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	FH
TLV9051IDPWR.A	Active	Production	X2SON (DPW) | 5	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	FH
TLV9051SIDBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	T51S
TLV9051SIDBVR.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	T51S
TLV9051SIDBVRG4	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T51S
TLV9051SIDBVRG4.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T51S
TLV9052IDDFR	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T052
TLV9052IDDFR.A	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T052
TLV9052IDDFRG4	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T052
TLV9052IDDFRG4.A	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T052
TLV9052IDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1PWX
TLV9052IDGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1PWX
TLV9052IDGKRG4	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1PWX
TLV9052IDGKRG4.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1PWX
TLV9052IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL9052
TLV9052IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL9052
TLV9052IDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL9052
TLV9052IDRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL9052
TLV9052IDSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	9052
TLV9052IDSGR.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	9052
TLV9052IDSGRG4	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	9052
TLV9052IDSGRG4.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	9052
TLV9052IPWR	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL9052
TLV9052IPWR.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL9052

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV9052SIDGSR	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	T052
TLV9052SIDGSR.A	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	T052
TLV9052SIRUGR	Active	Production	X2QFN (RUG) | 10	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	FPF
TLV9052SIRUGR.A	Active	Production	X2QFN (RUG) | 10	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	FPF
TLV9054IDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV9054D
TLV9054IDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV9054D
TLV9054IDRG4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV9054D
TLV9054IDRG4.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV9054D
TLV9054IPWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	(T9054PW, TLV9054)
TLV9054IPWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	(T9054PW, TLV9054)
TLV9054IRTER	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	FULL NIPDAU	Level-1-260C-UNLIM	-40 to 125	T54RT
TLV9054IRTER.A	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	FULL NIPDAU	Level-1-260C-UNLIM	-40 to 125	T54RT
TLV9054IRUCR	Active	Production	QFN (RUC) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1FF
TLV9054IRUCR.A	Active	Production	QFN (RUC) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1FF
TLV9054SIRTER	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	FULL NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9054S
TLV9054SIRTER.A	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	FULL NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9054S

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV9051, TLV9052 :

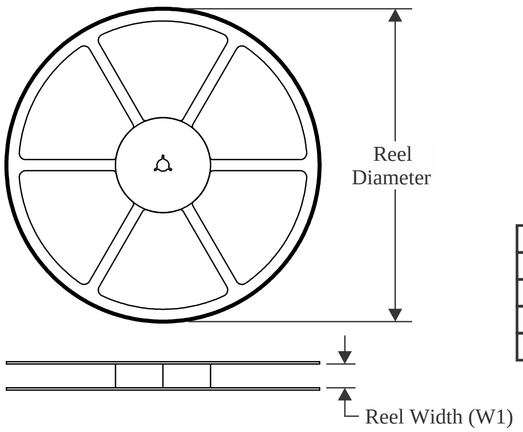
- Automotive : TLV9051-Q1, TLV9052-Q1

NOTE: Qualified Version Definitions:

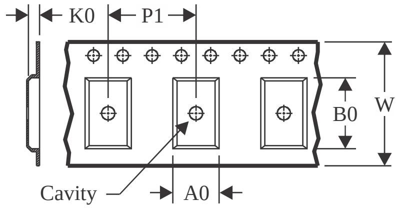
  - Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

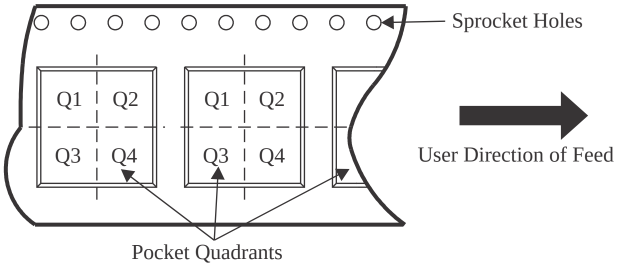


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

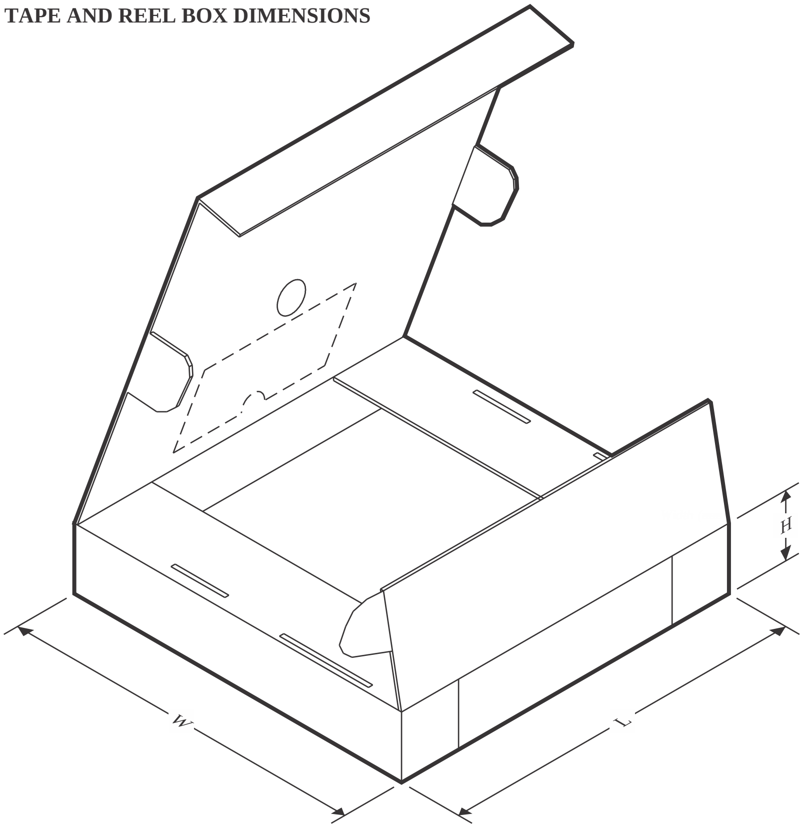


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV9051IDBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9051IDCKR	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
TLV9051IDCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
TLV9051IDPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q2
TLV9051SIDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9051SIDBVRG4	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9052IDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9052IDDFRG4	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9052IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV9052IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV9052IDGKRG4	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV9052IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV9052IDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV9052IDSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV9052IDSGRG4	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV9052IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV9052SIDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV9052SIRUGR	X2QFN	RUG	10	3000	178.0	8.4	1.75	2.25	0.56	4.0	8.0	Q1
TLV9054IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV9054IDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV9054IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV9054IRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TLV9054IRUCR	QFN	RUC	14	3000	180.0	9.5	2.16	2.16	0.5	4.0	8.0	Q2
TLV9054SIRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

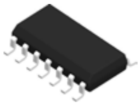
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV9051IDBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
TLV9051IDCKR	SC70	DCK	5	3000	208.0	191.0	35.0
TLV9051IDCKR	SC70	DCK	5	3000	210.0	185.0	35.0
TLV9051IDPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
TLV9051SIDBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TLV9051SIDBVRG4	SOT-23	DBV	6	3000	210.0	185.0	35.0
TLV9052IDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TLV9052IDDFRG4	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TLV9052IDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
TLV9052IDGKR	VSSOP	DGK	8	2500	356.0	356.0	36.0
TLV9052IDGKRG4	VSSOP	DGK	8	2500	353.0	353.0	32.0
TLV9052IDR	SOIC	D	8	2500	353.0	353.0	32.0
TLV9052IDRG4	SOIC	D	8	2500	353.0	353.0	32.0
TLV9052IDSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TLV9052IDSGRG4	WSON	DSG	8	3000	210.0	185.0	35.0
TLV9052IPWR	TSSOP	PW	8	2000	353.0	353.0	32.0
TLV9052SIDGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
TLV9052SIRUGR	X2QFN	RUG	10	3000	205.0	200.0	33.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV9054IDR	SOIC	D	14	2500	353.0	353.0	32.0
TLV9054IDRG4	SOIC	D	14	2500	353.0	353.0	32.0
TLV9054IPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
TLV9054IRTER	WQFN	RTE	16	3000	367.0	367.0	35.0
TLV9054IRUCR	QFN	RUC	14	3000	205.0	200.0	30.0
TLV9054SIRTER	WQFN	RTE	16	3000	367.0	367.0	35.0

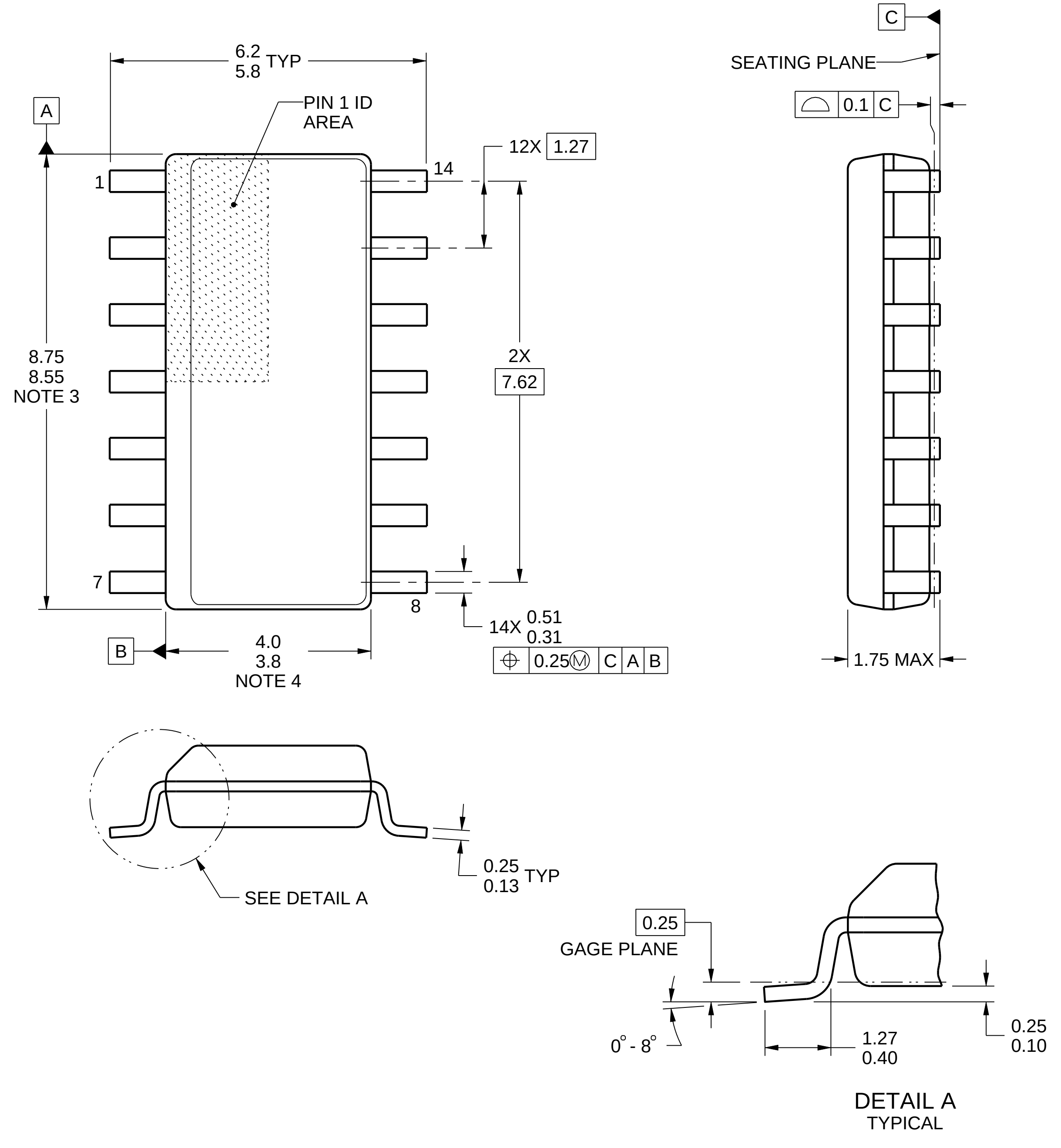


PACKAGE OUTLINE

D0014A

SOIC - 1.75 mm max height

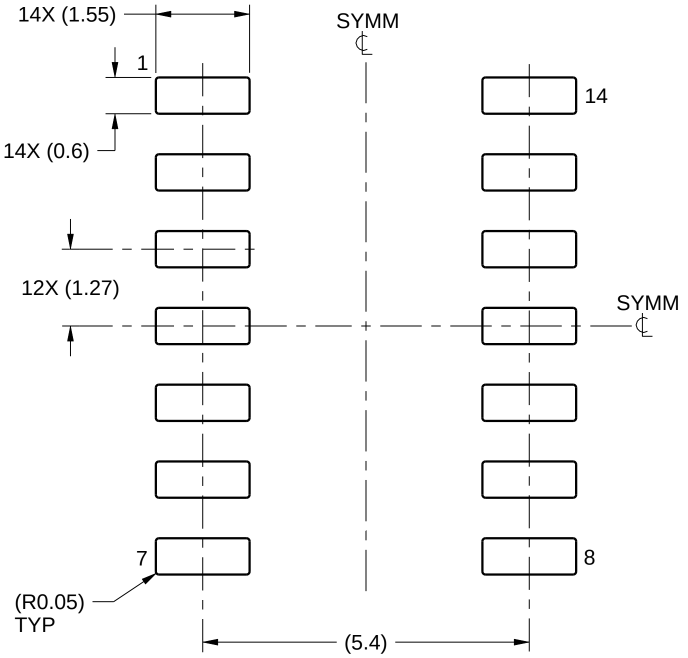
SMALL OUTLINE INTEGRATED CIRCUIT



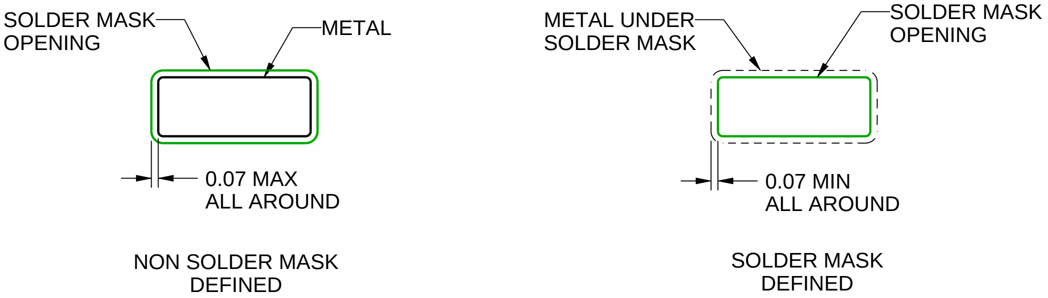
4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X

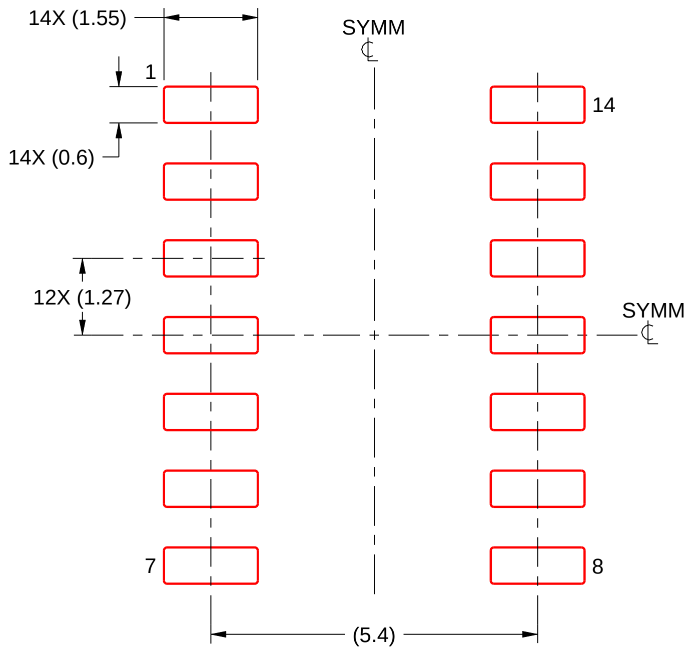


SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

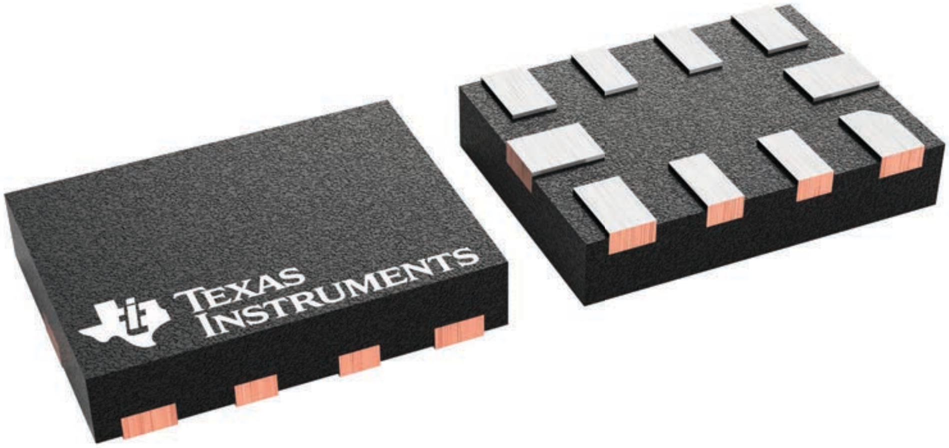
RUG 10

X2QFN - 0.4 mm max height

1.5 x 2, 0.5 mm pitch

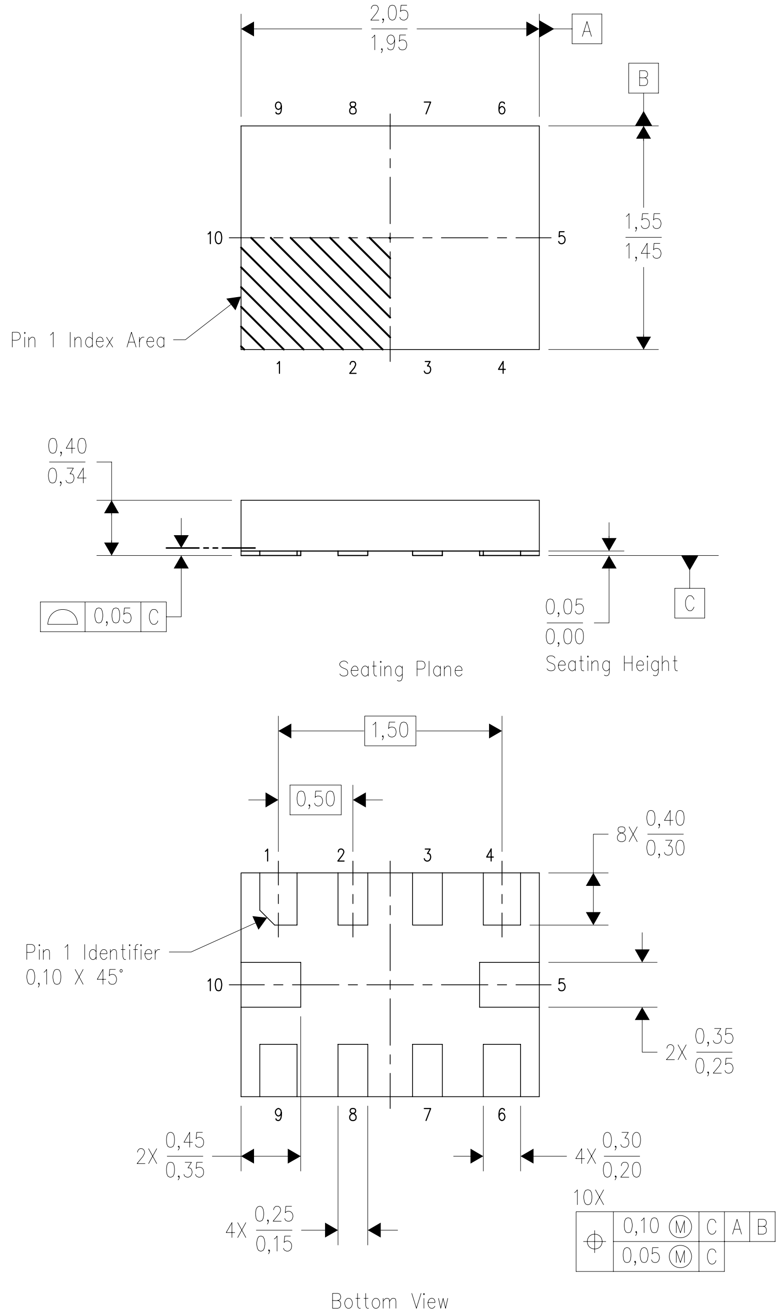
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4231768/A

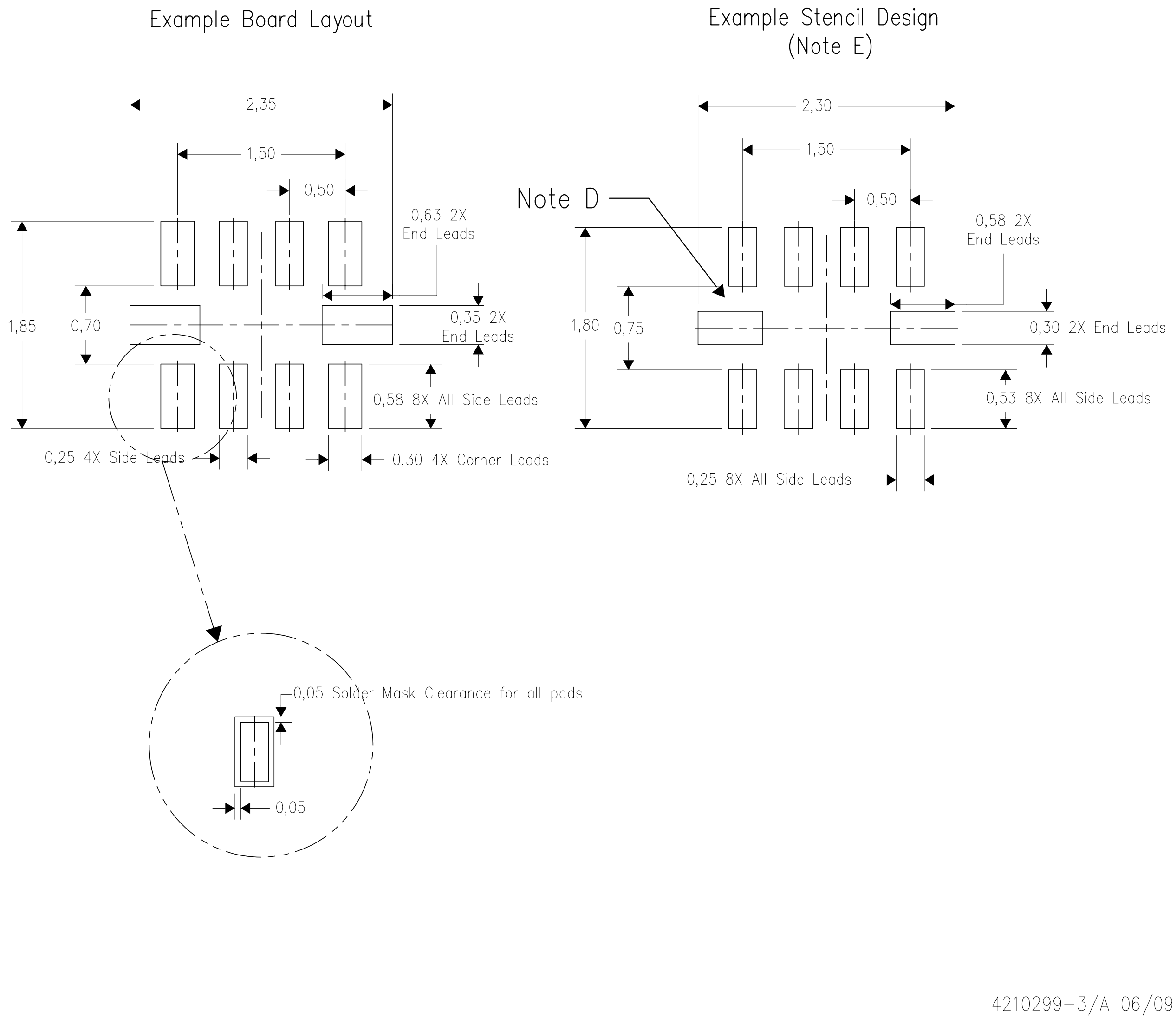
RUG (R-PQFP-N10) PLASTIC QUAD FLATPACK



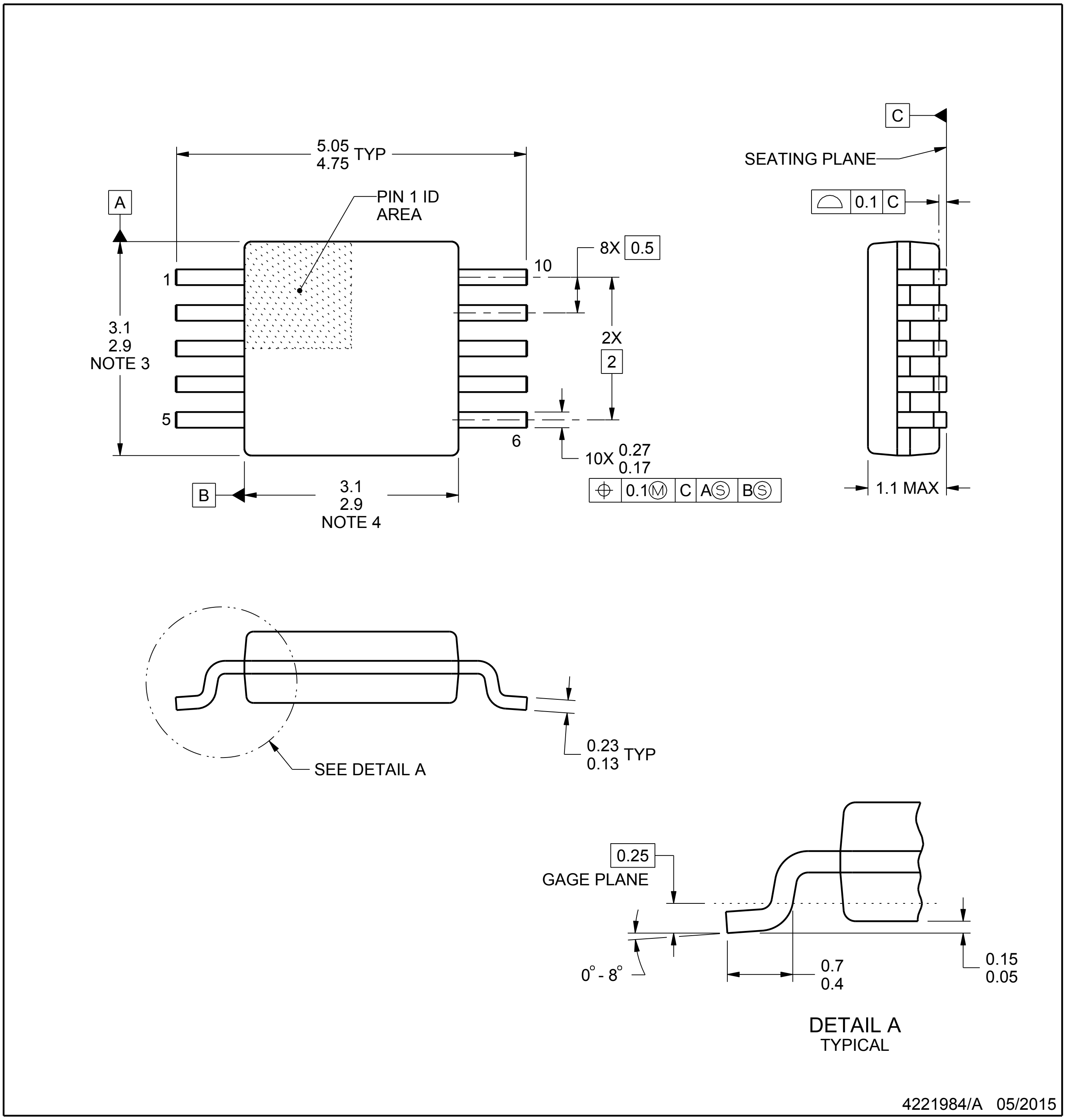
4208528-3/B 04/2008

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No-Lead) package configuration.
D. This package complies to JEDEC MO-288 variation X2EFD.

RUG (R–PQFP–N10)



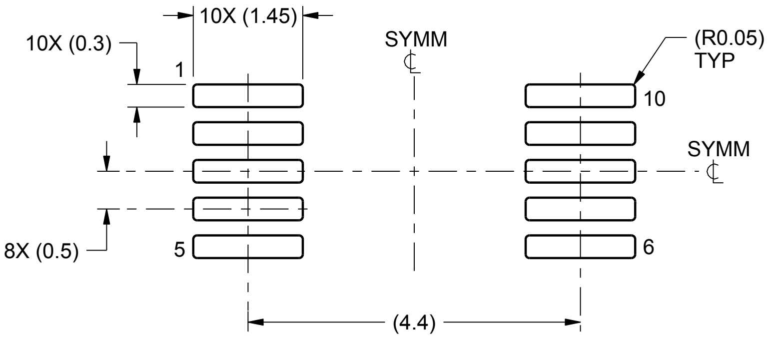
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
- E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
- F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.



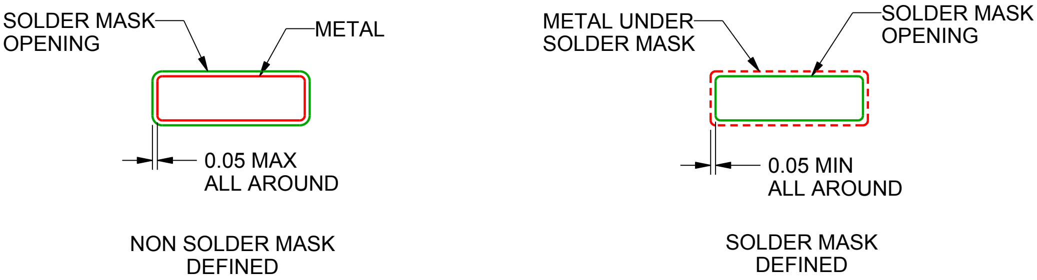
4221984/A 05/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

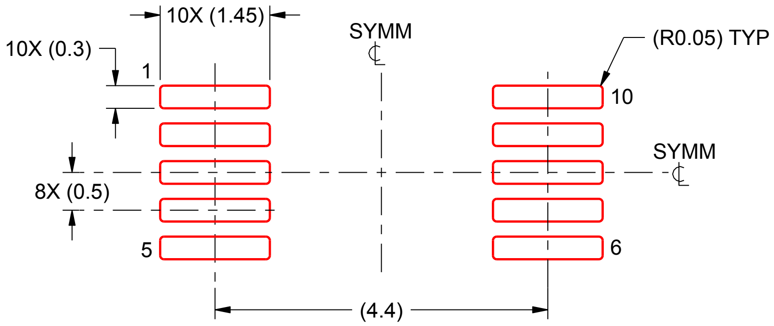


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DPW 5

X2SON - 0.4 mm max height

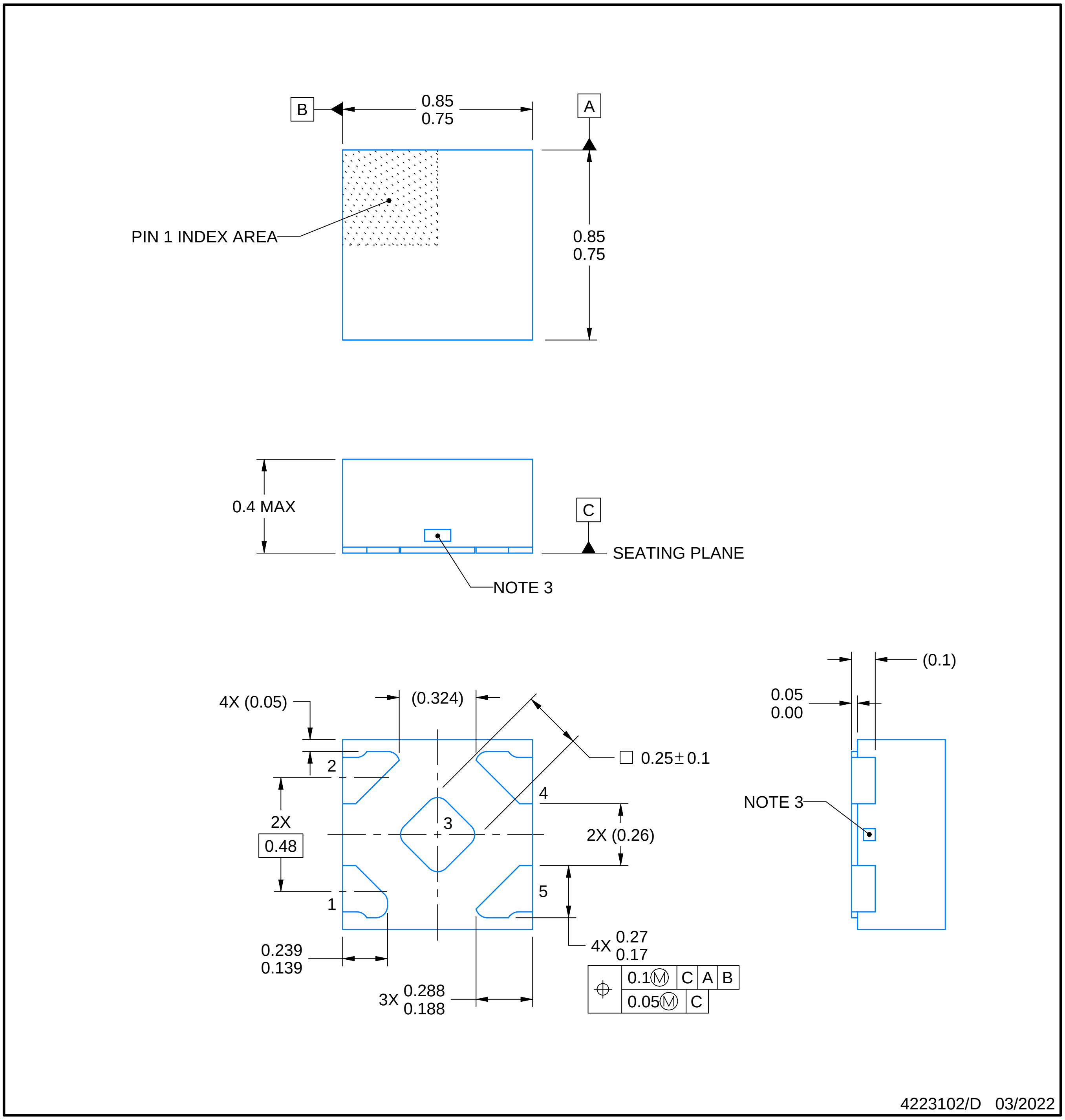
PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

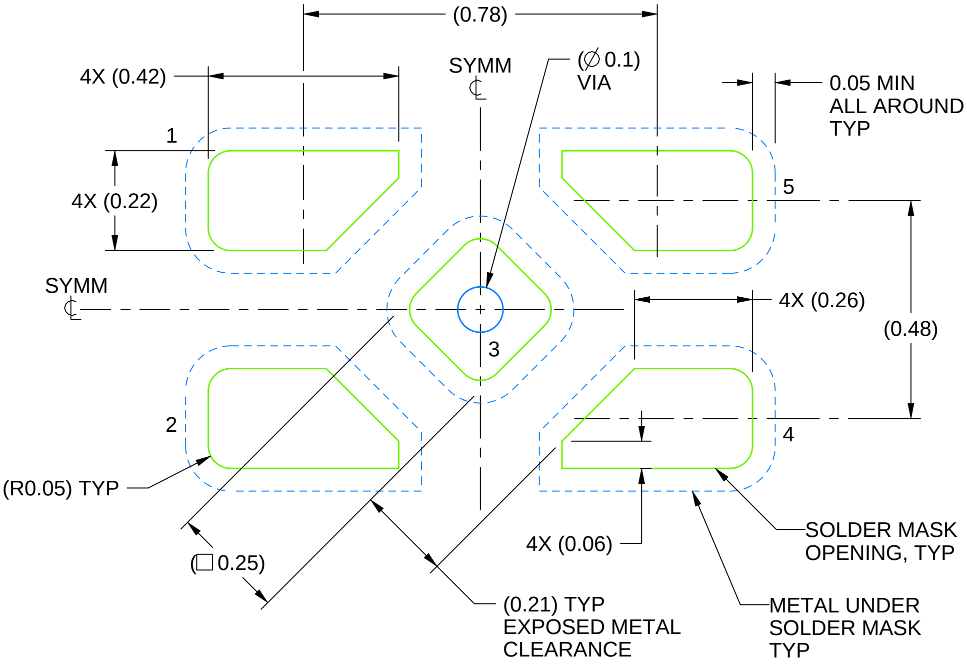
X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

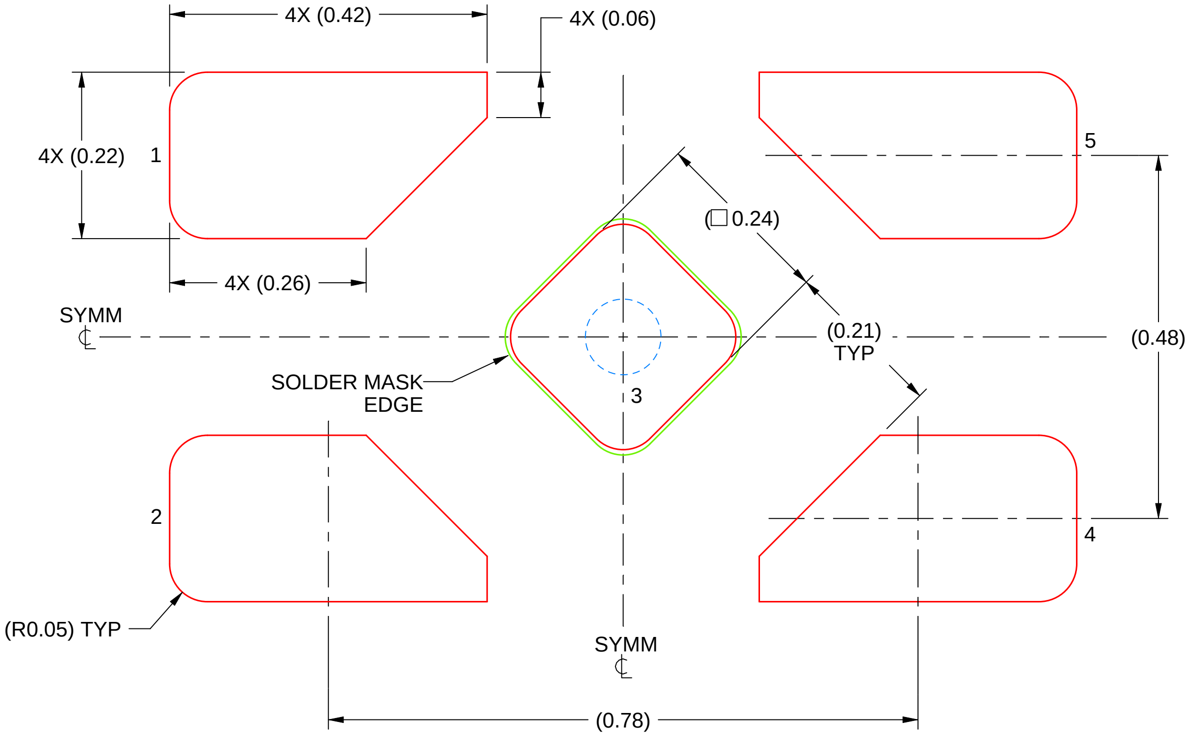
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).

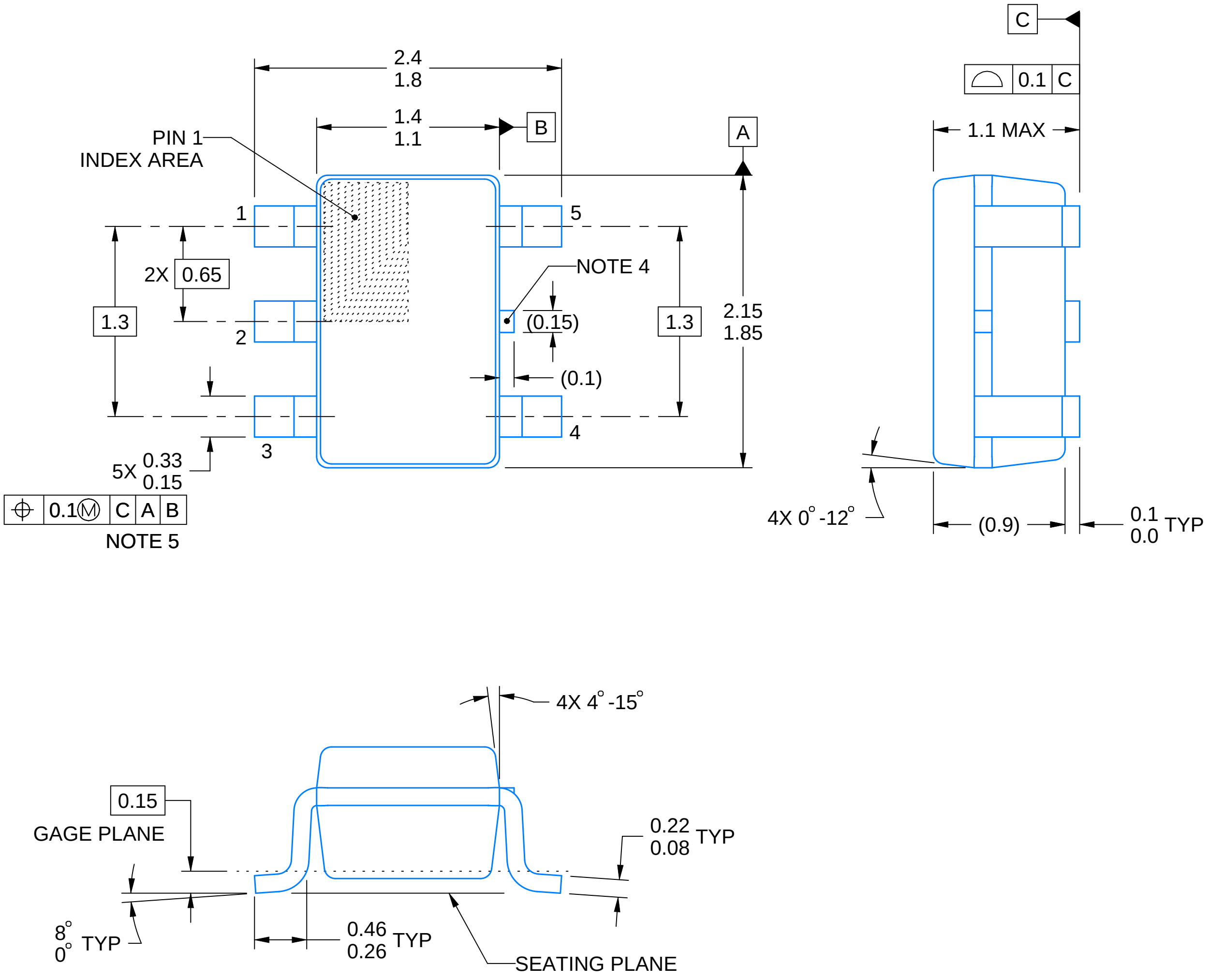


SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 3
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:100X

NOTES: (continued)

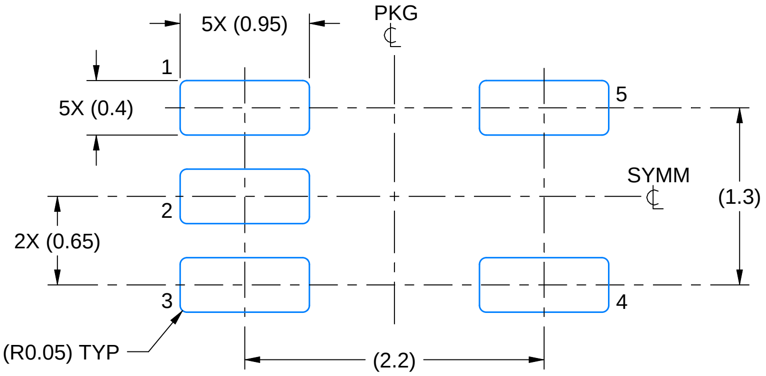
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



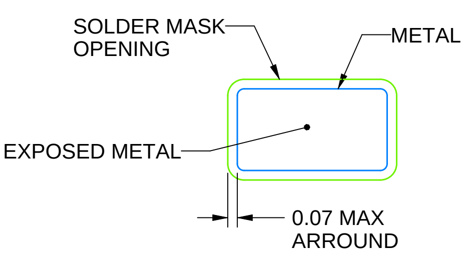
4214834/G 11/2024

NOTES:

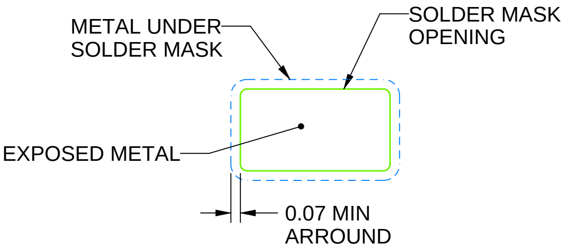
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



NON SOLDER MASK
DEFINED
(PREFERRED)

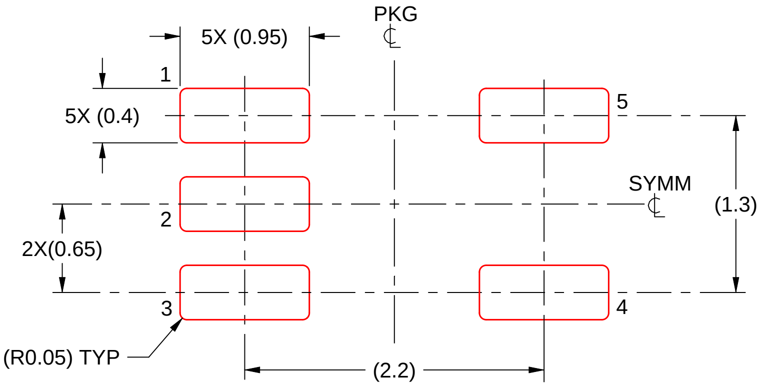


SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

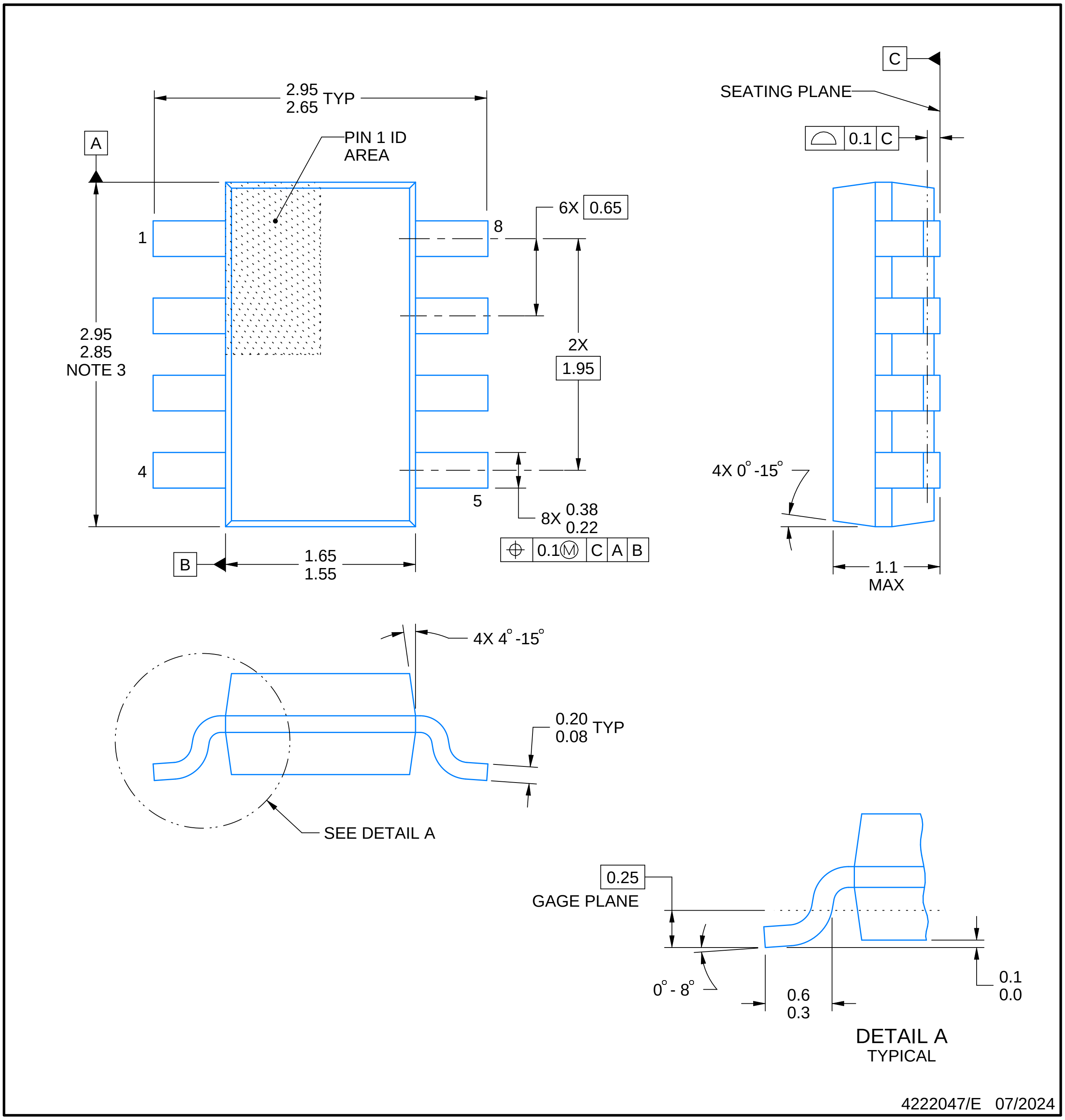
7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

NOTES: (continued)

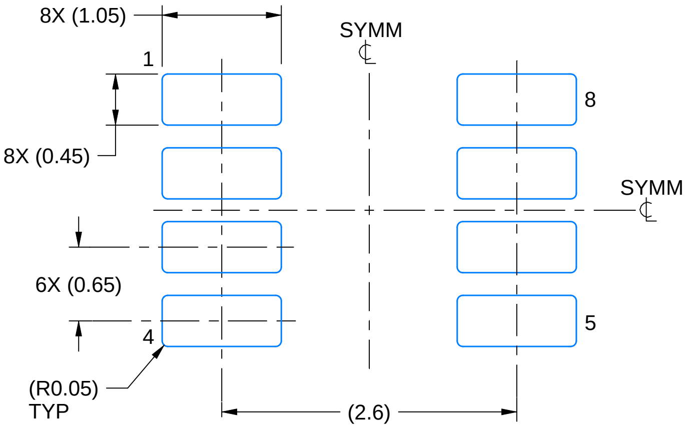
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.



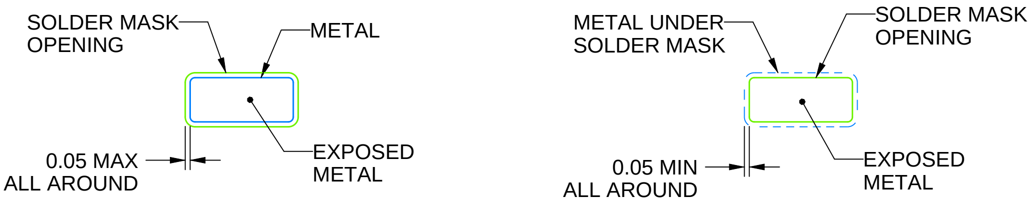
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

EXAMPLE BOARD LAYOUT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK
DEFINED

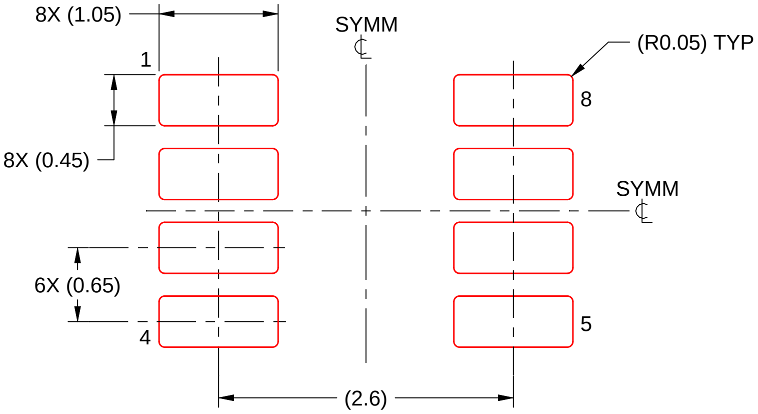
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4222047/E 07/2024

NOTES: (continued)

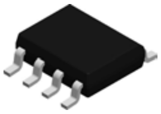
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

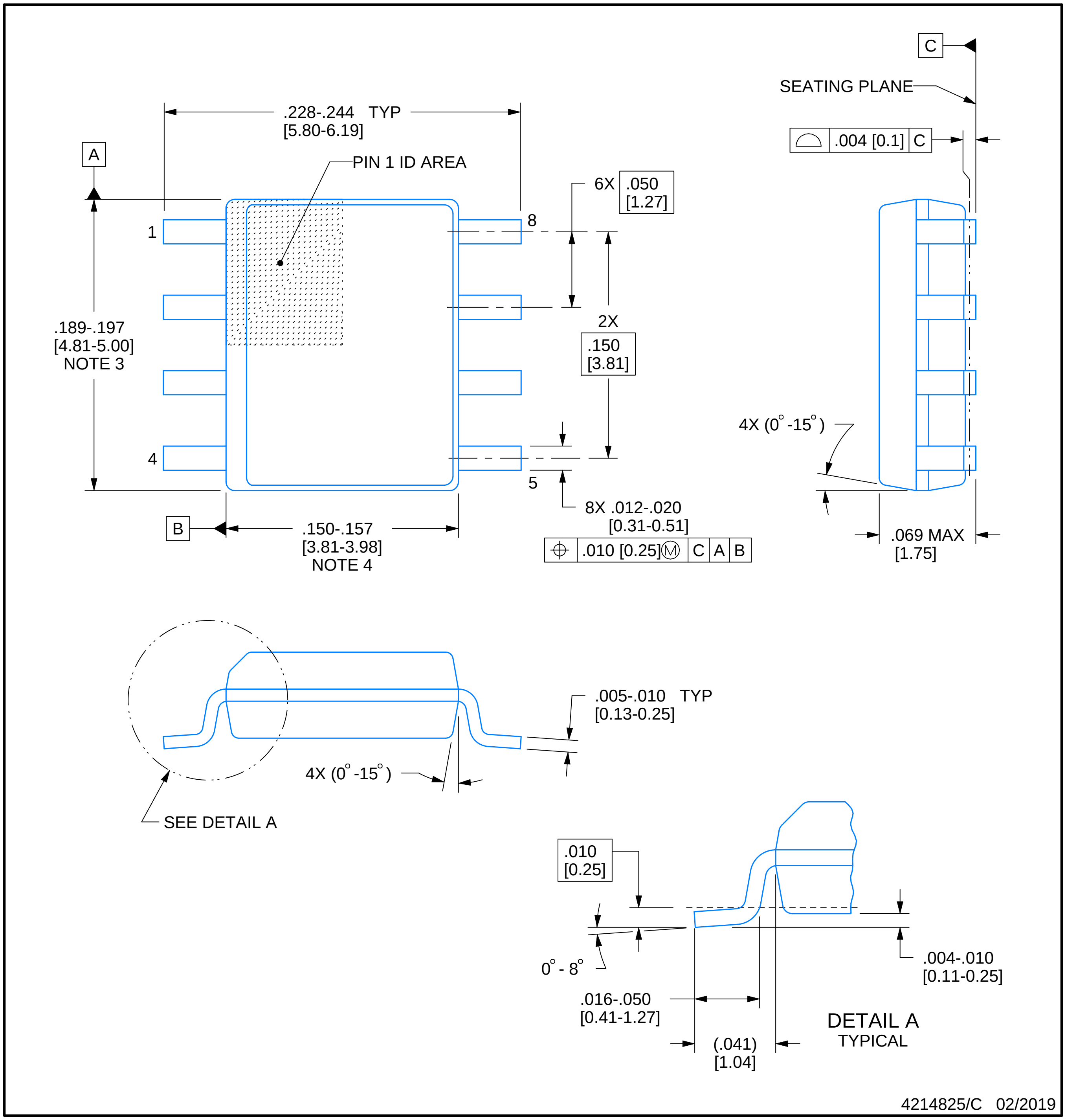


PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

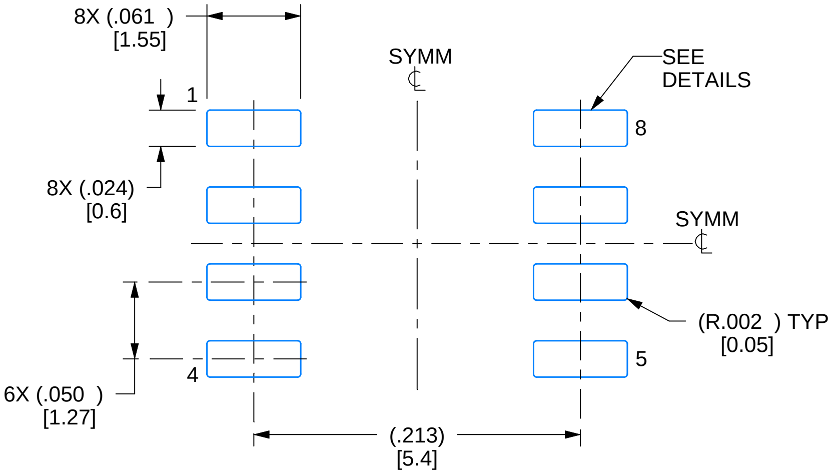
SMALL OUTLINE INTEGRATED CIRCUIT



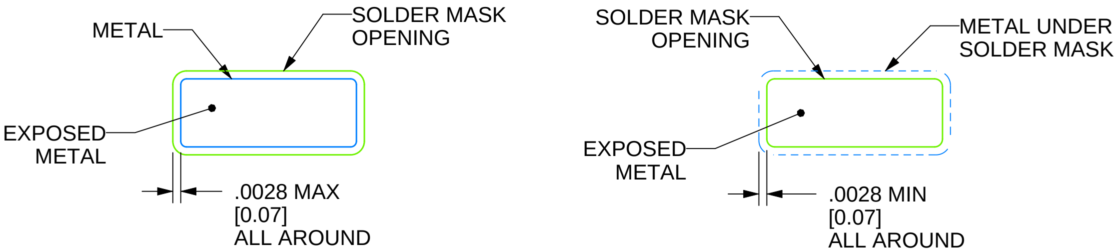
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



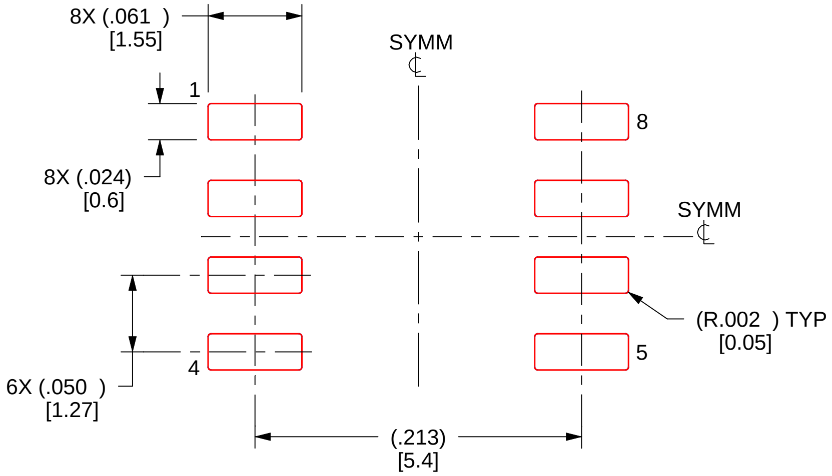
NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

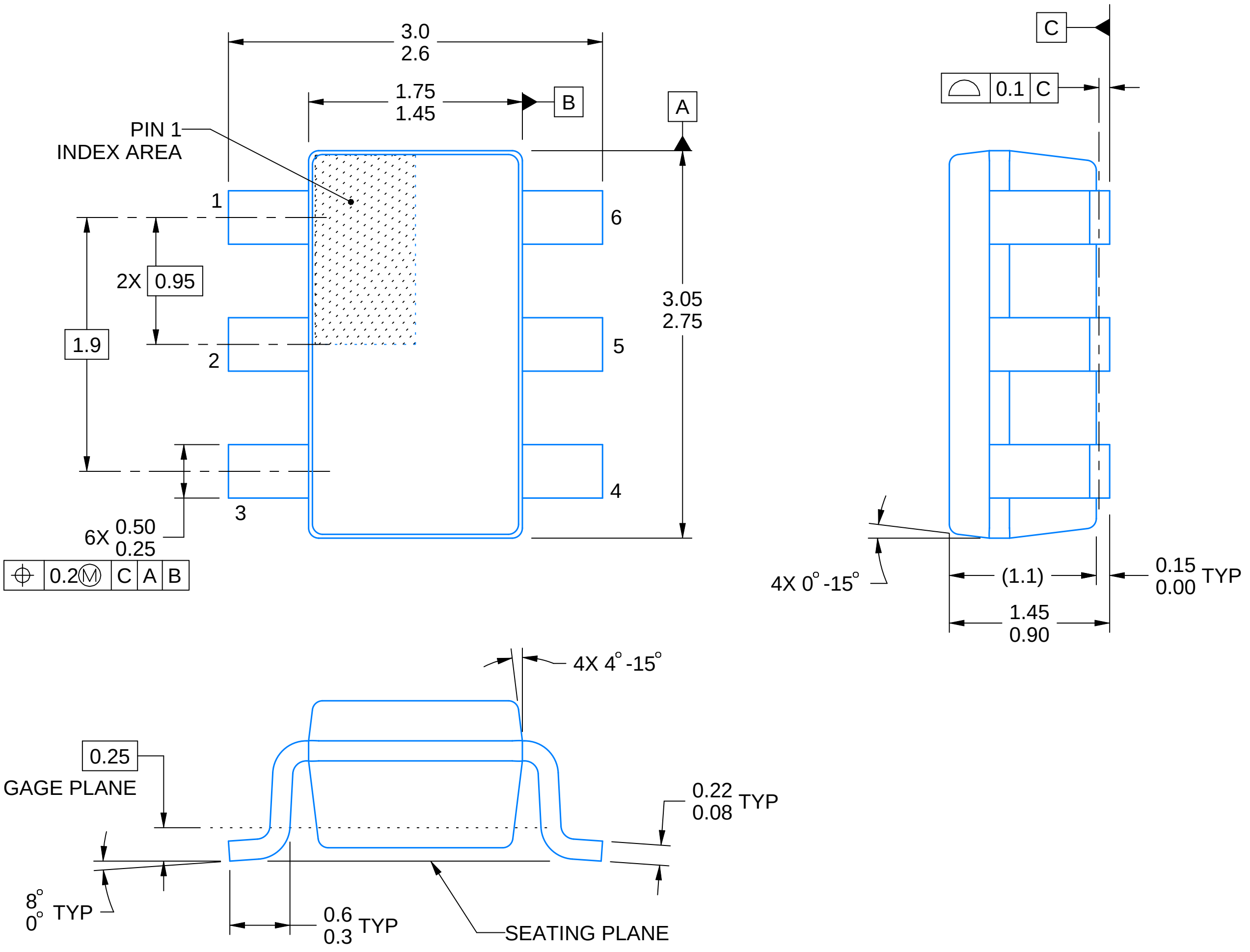
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

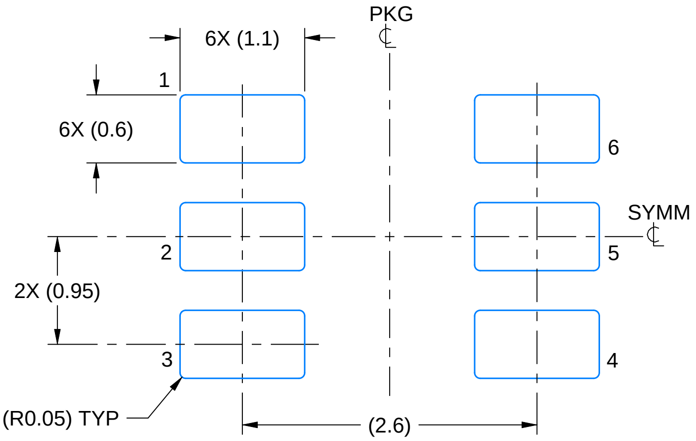
SMALL OUTLINE TRANSISTOR



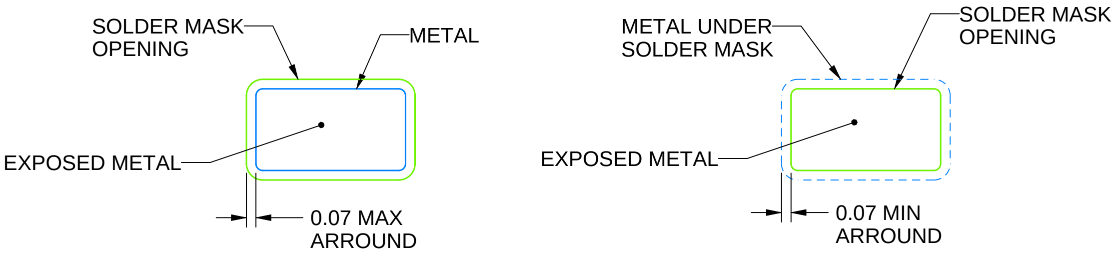
4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



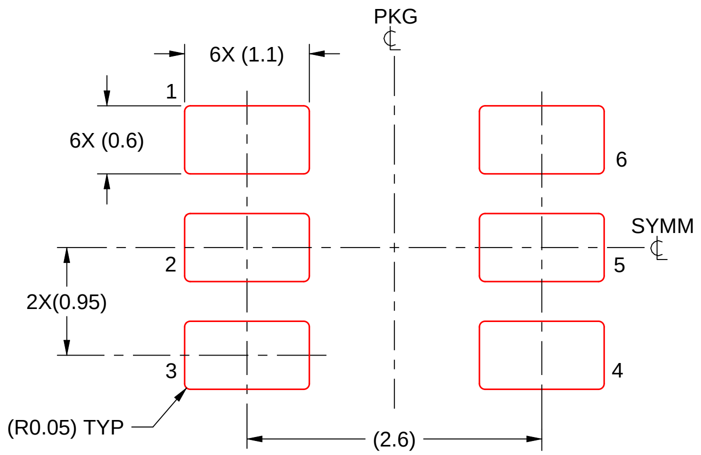
NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

NOTES: (continued)

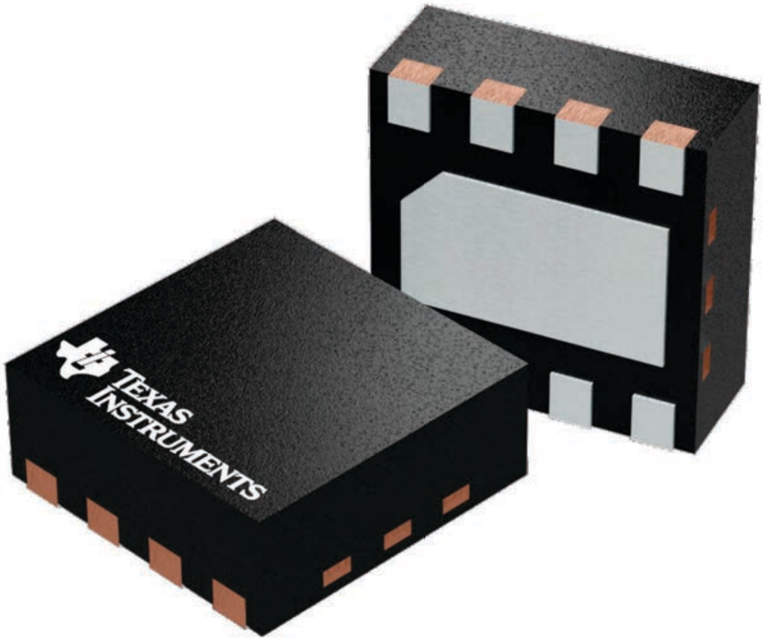
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

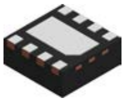
DSG 8 **WSON - 0.8 mm max height**

2 x 2, 0.5 mm pitch PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



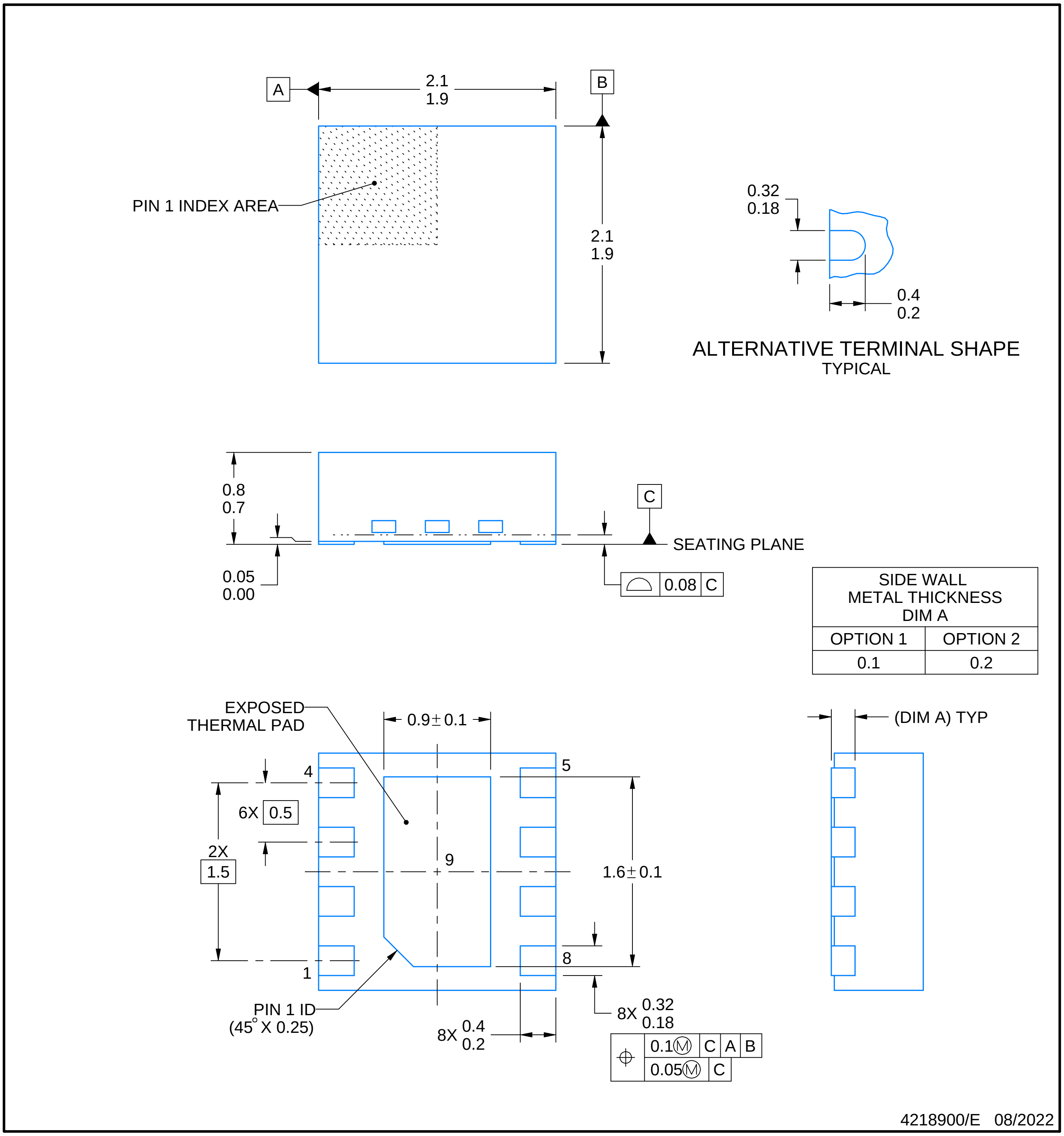
4224783/A



PACKAGE OUTLINE

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

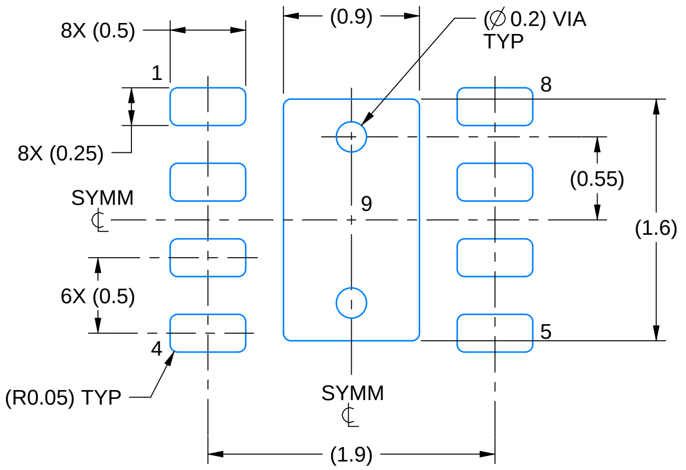


SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2

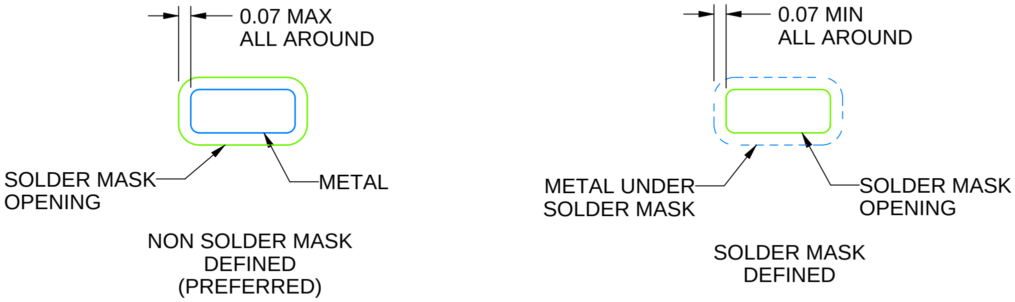
4218900/E 08/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



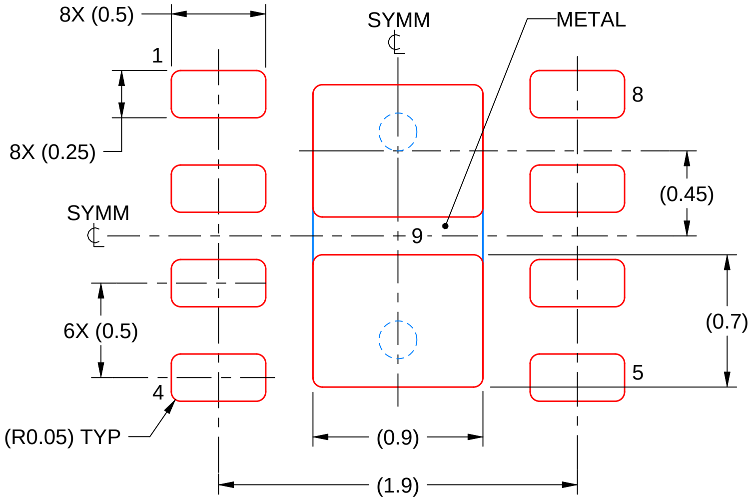
LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

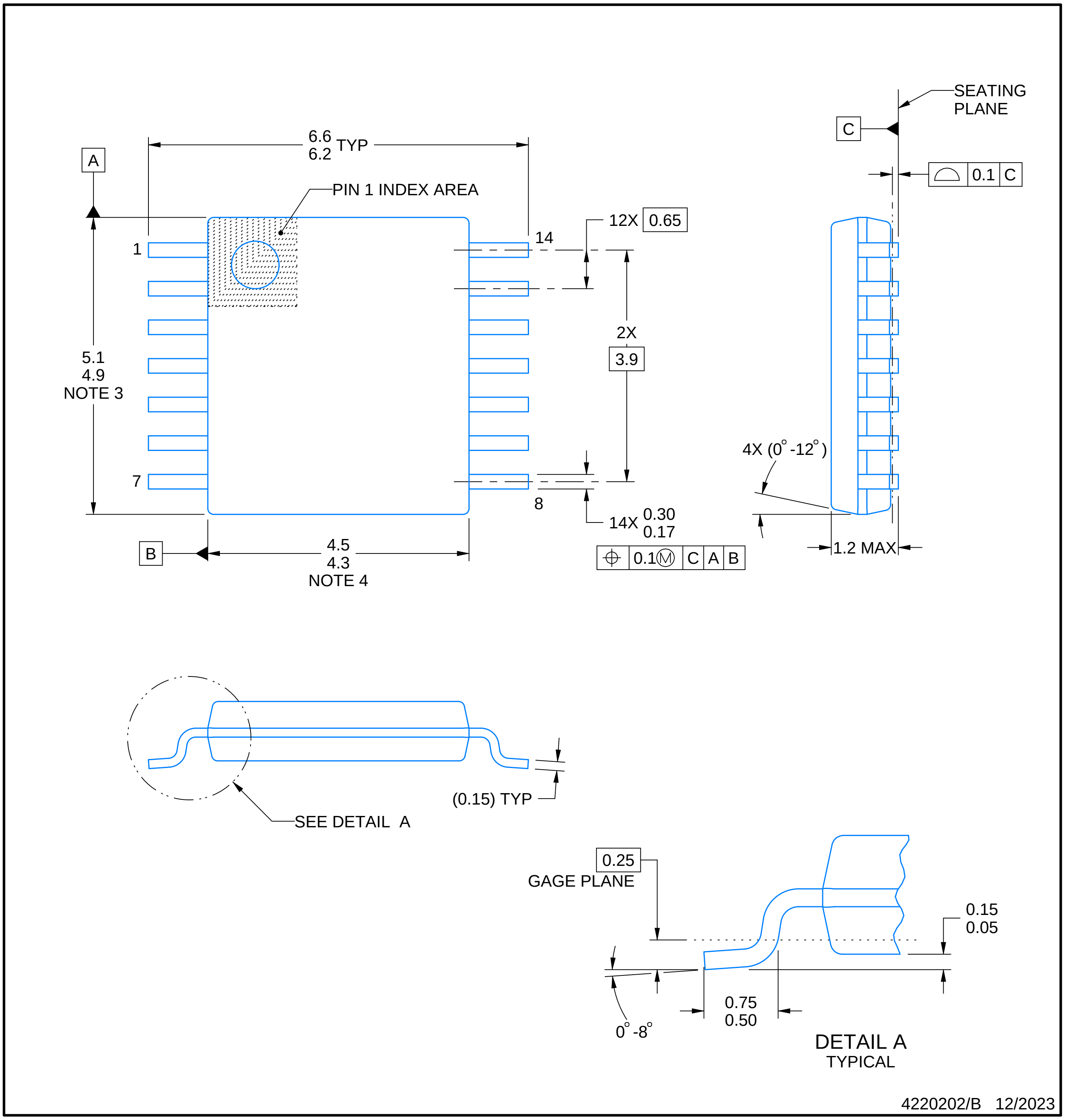


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

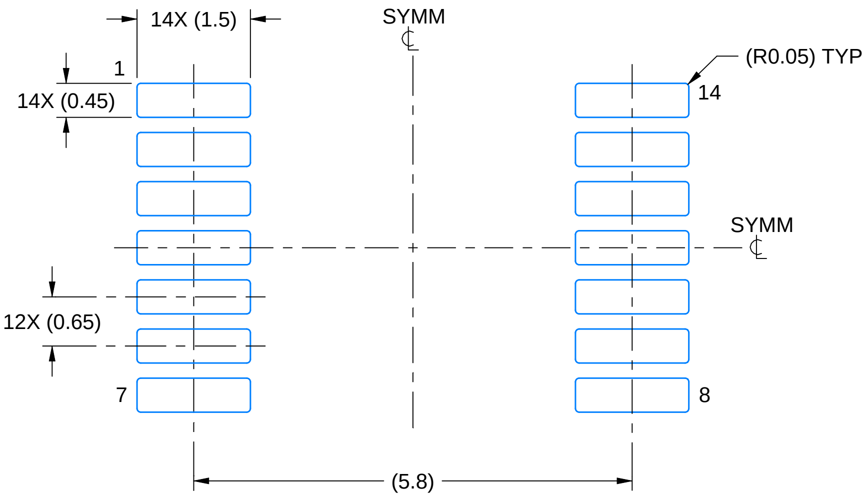
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

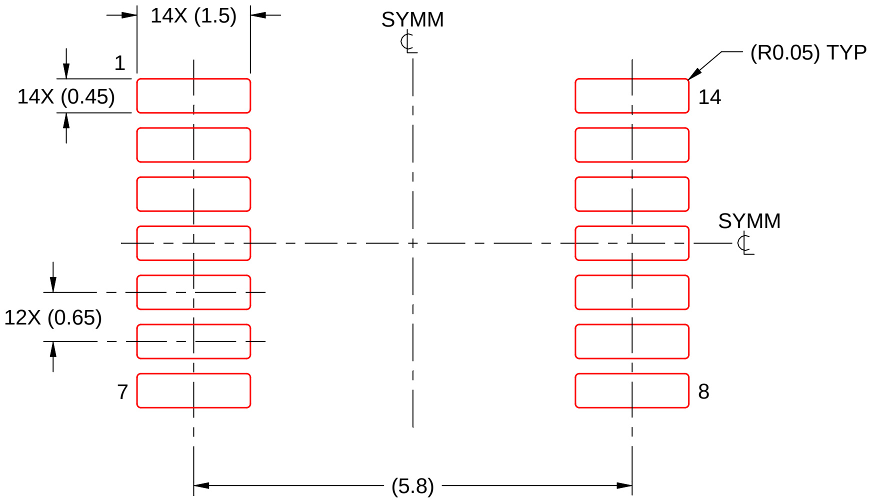
NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

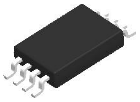


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

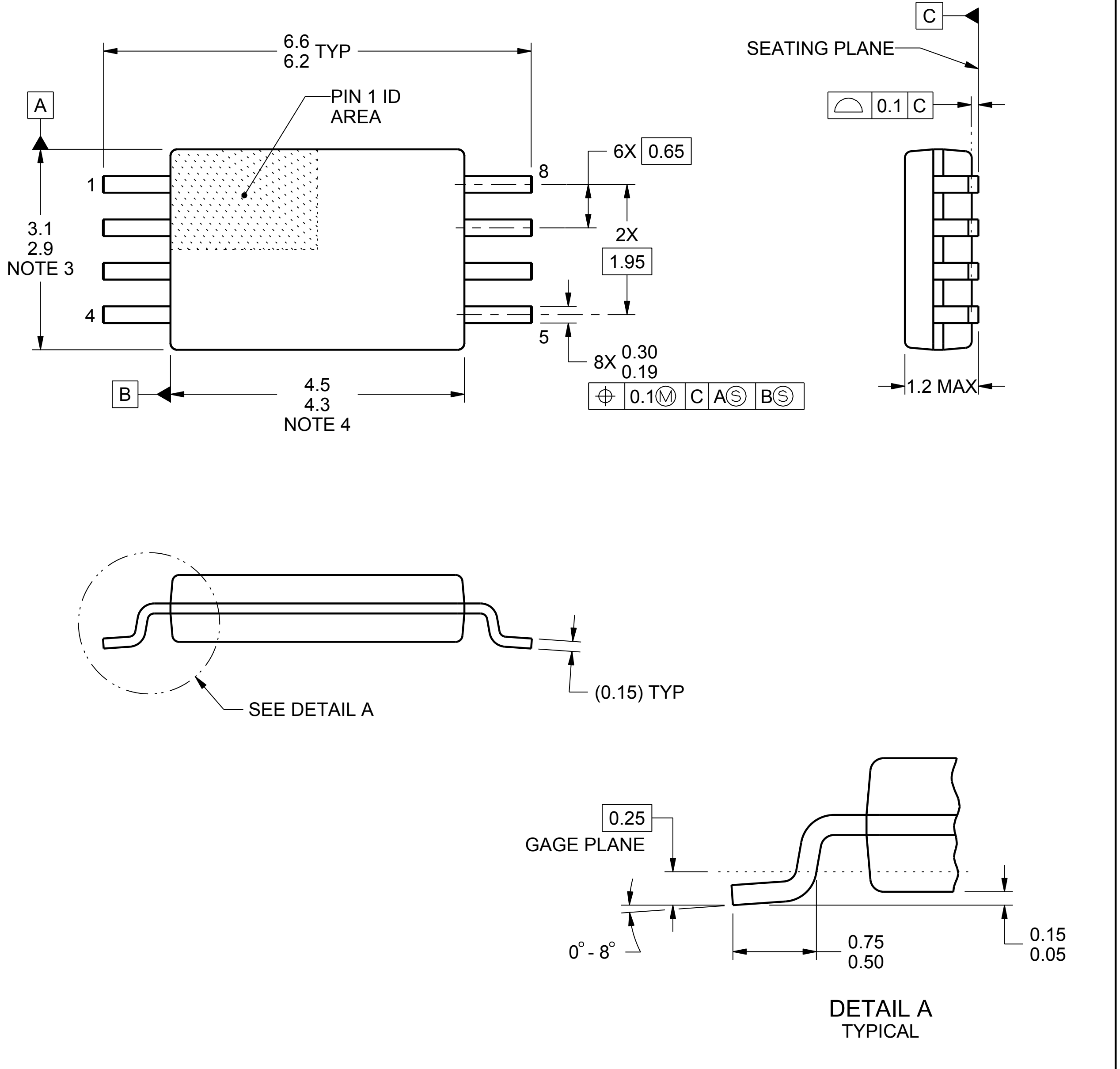
PACKAGE OUTLINE



PW0008A

TSSOP - 1.2 mm max height

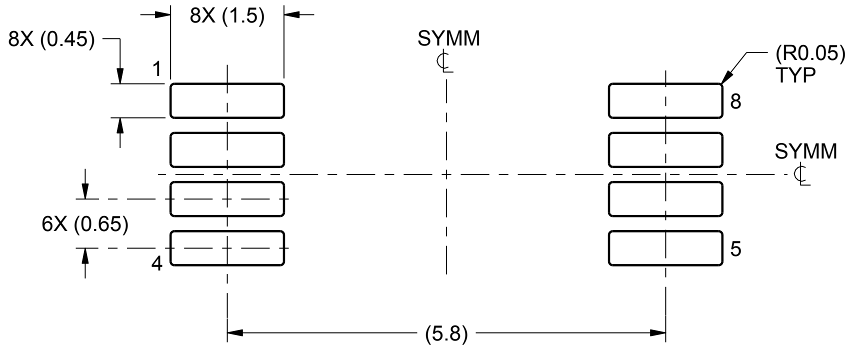
SMALL OUTLINE PACKAGE



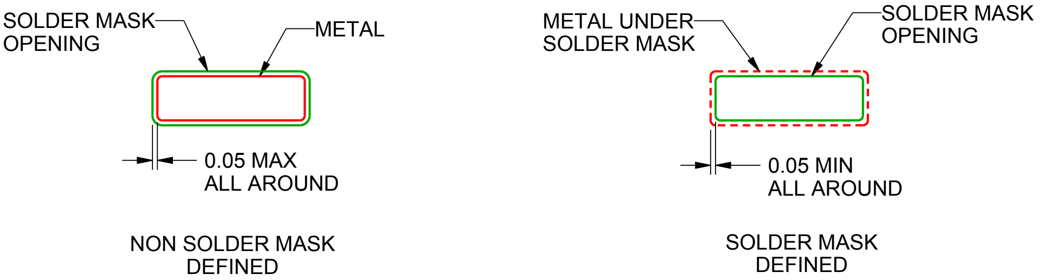
4221848/A 02/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

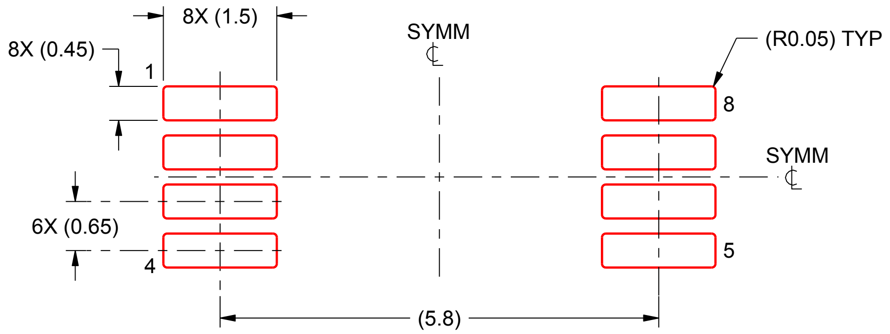


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

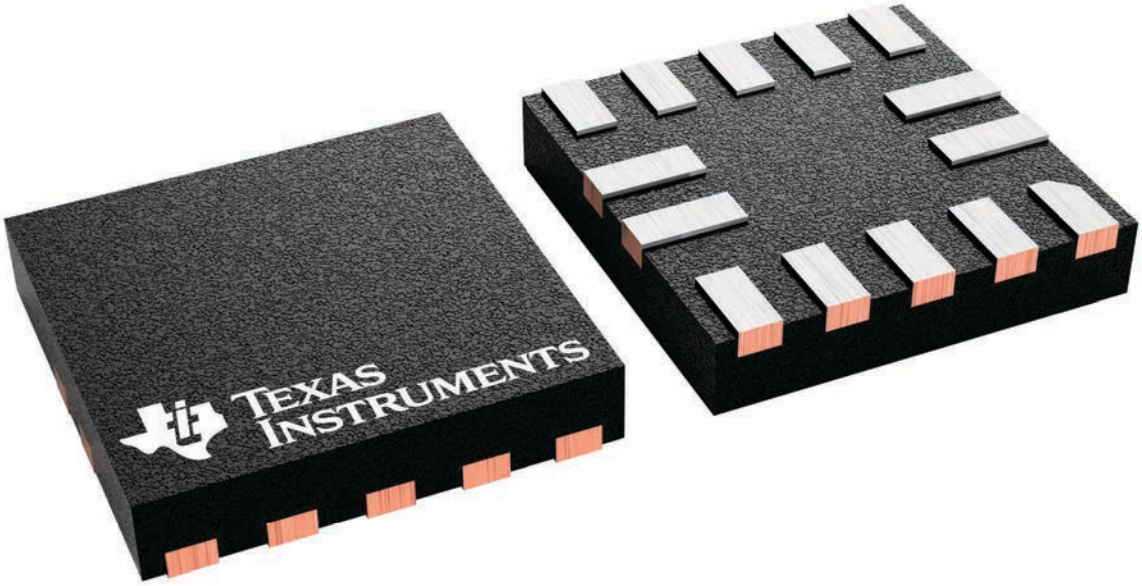
RUC 14

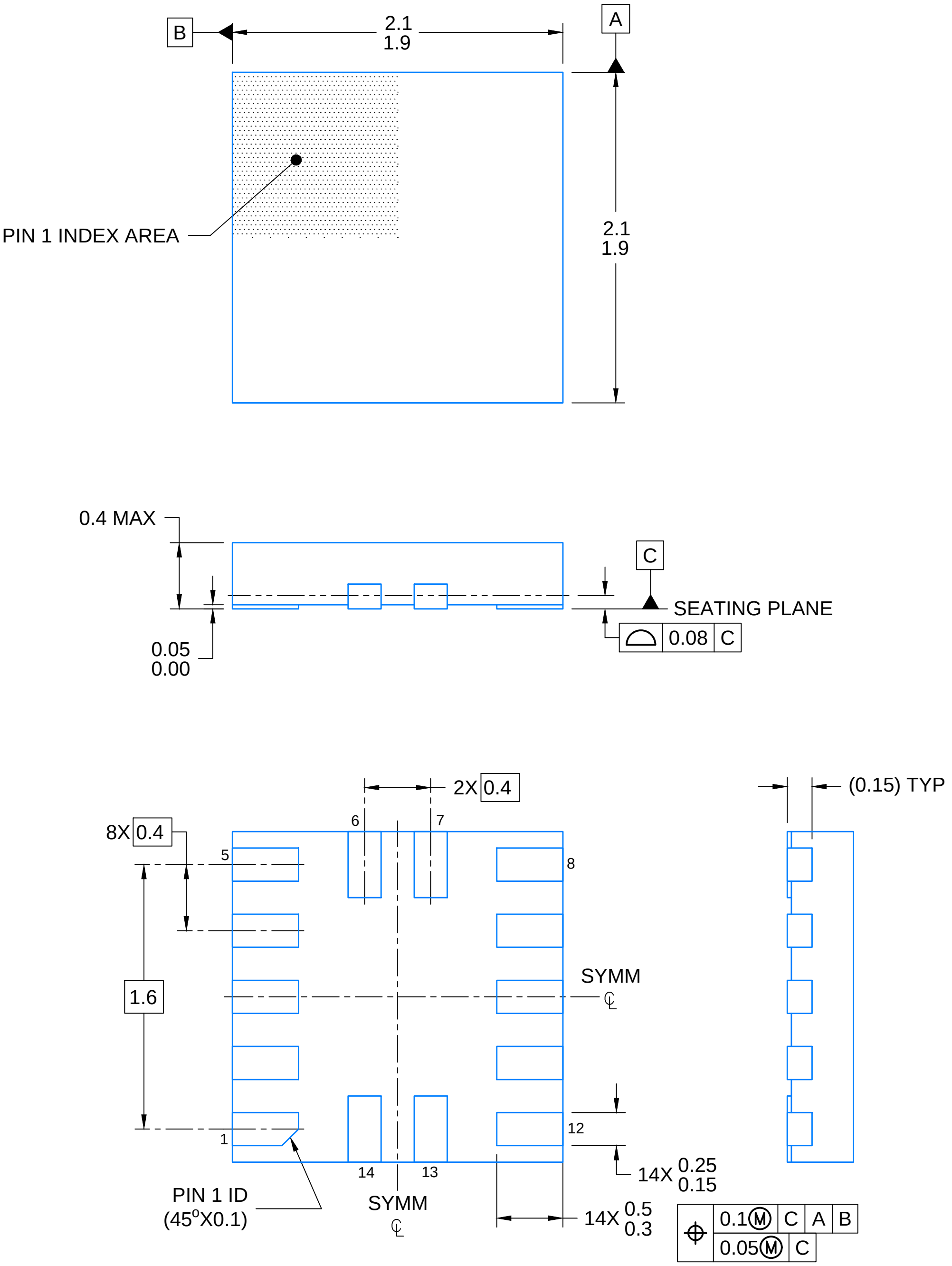
X2QFN - 0.4 mm max height

2 x 2, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

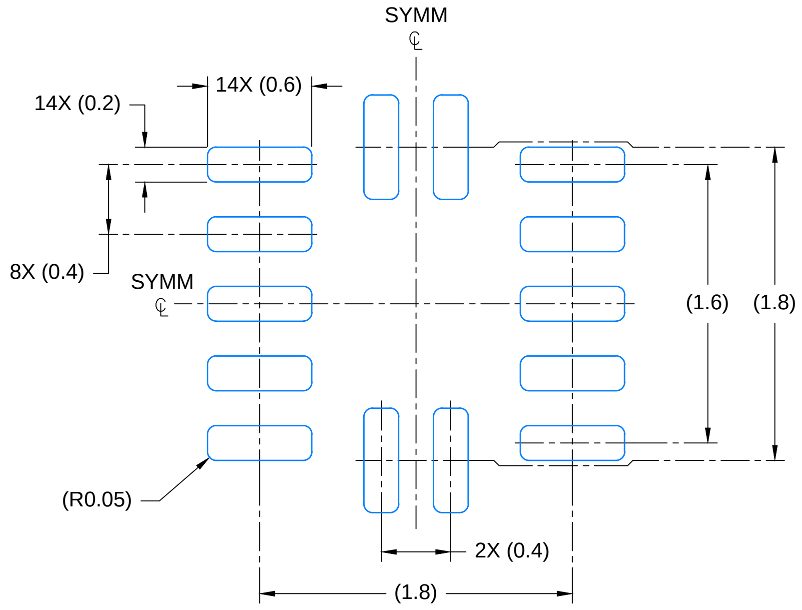




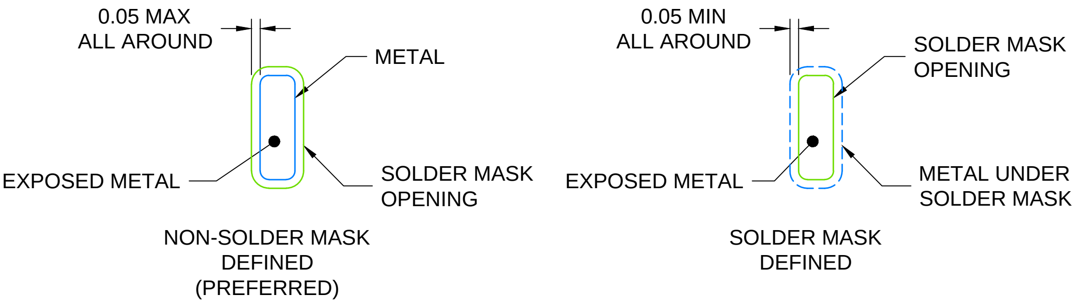
4220584/A 05/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 23X

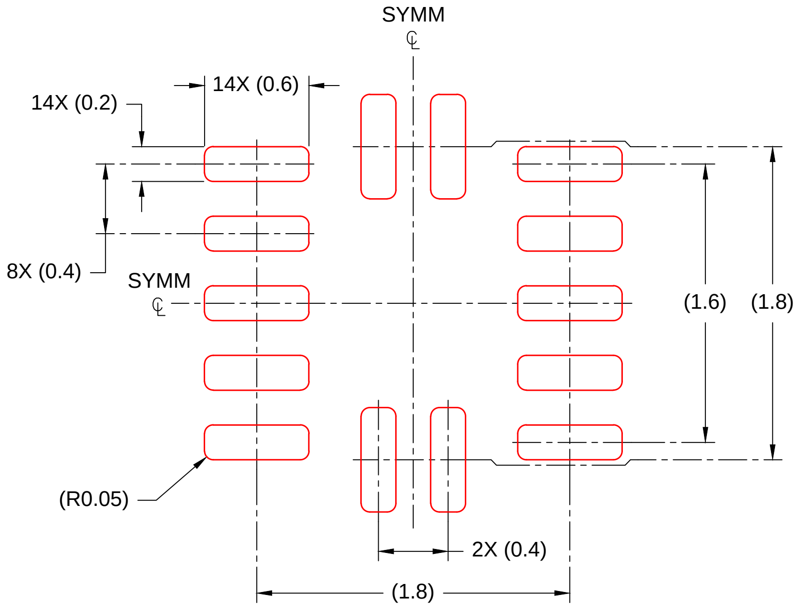


SOLDER MASK DETAILS

4220584/A 05/2019

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

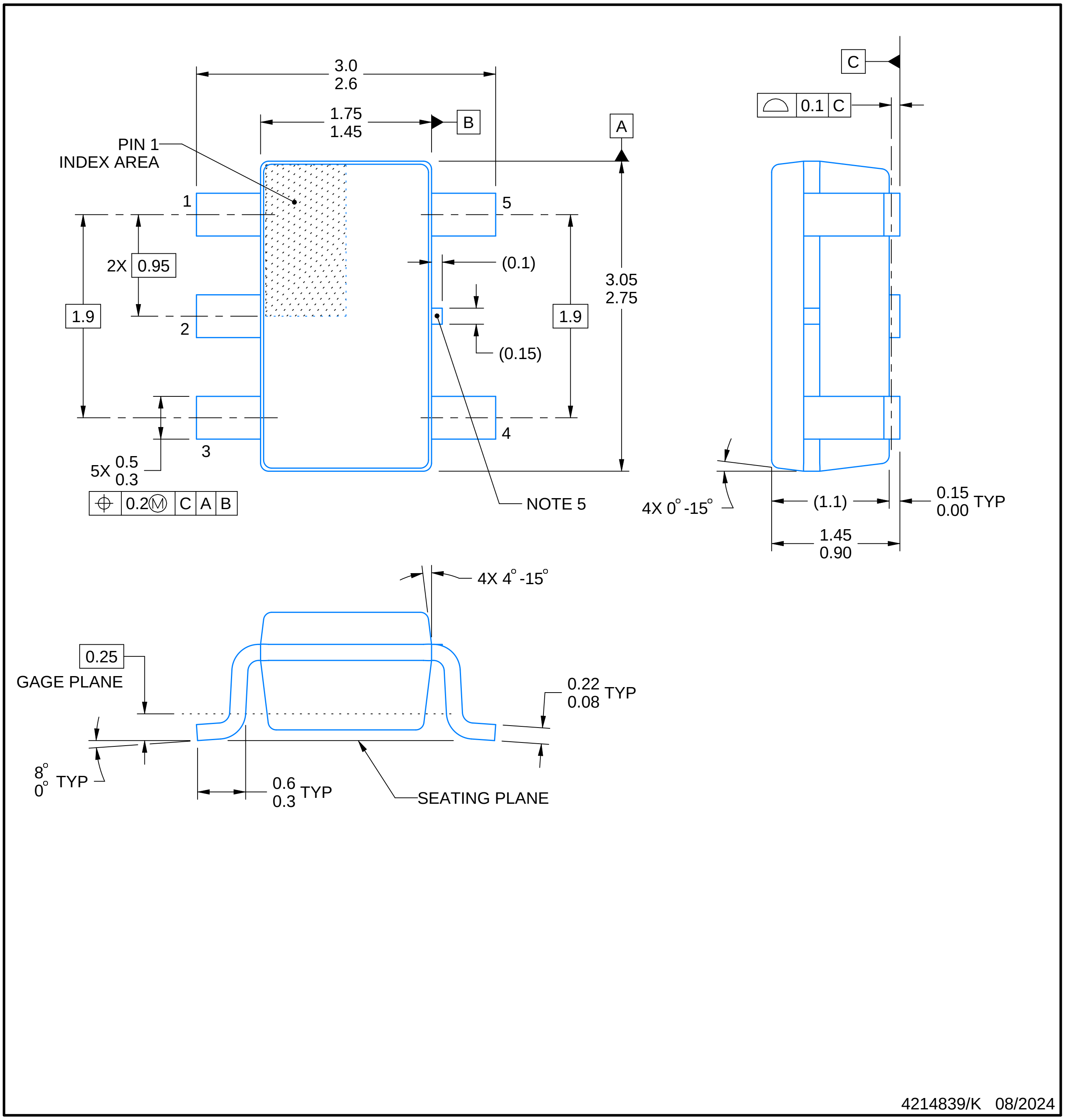


SOLDER PASTE EXAMPLE
BASED ON 0.100mm THICK STENCIL
SCALE: 23X

4220584/A 05/2019

NOTES: (continued)

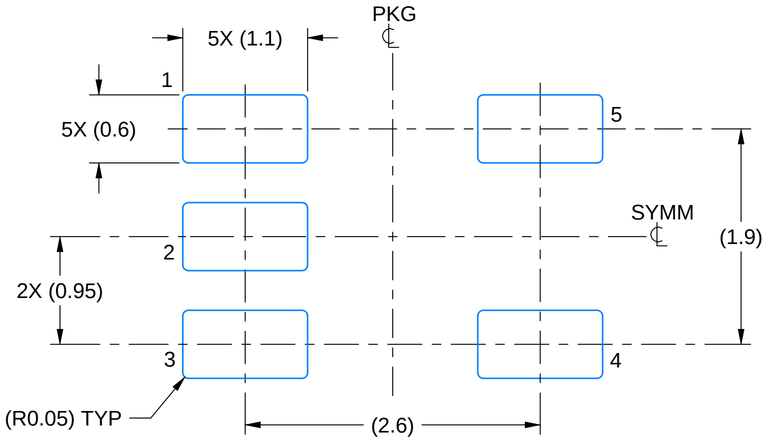
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



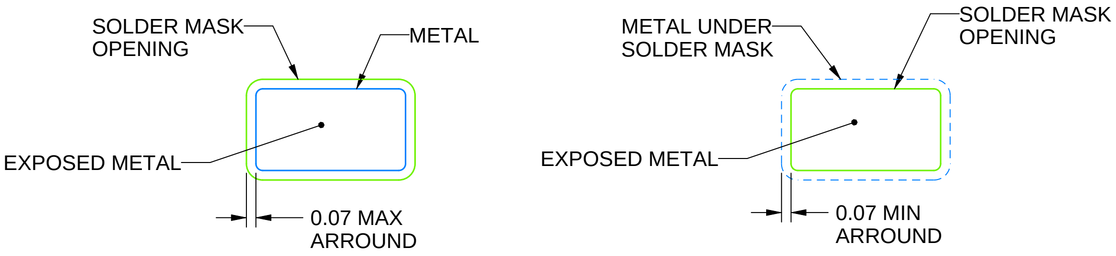
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



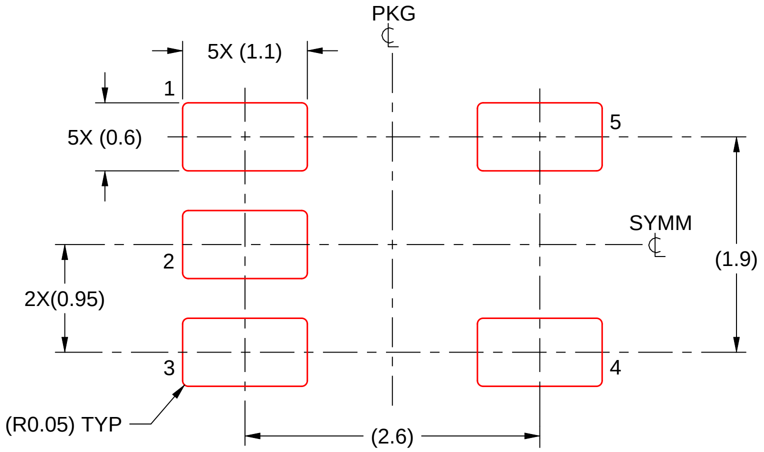
NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

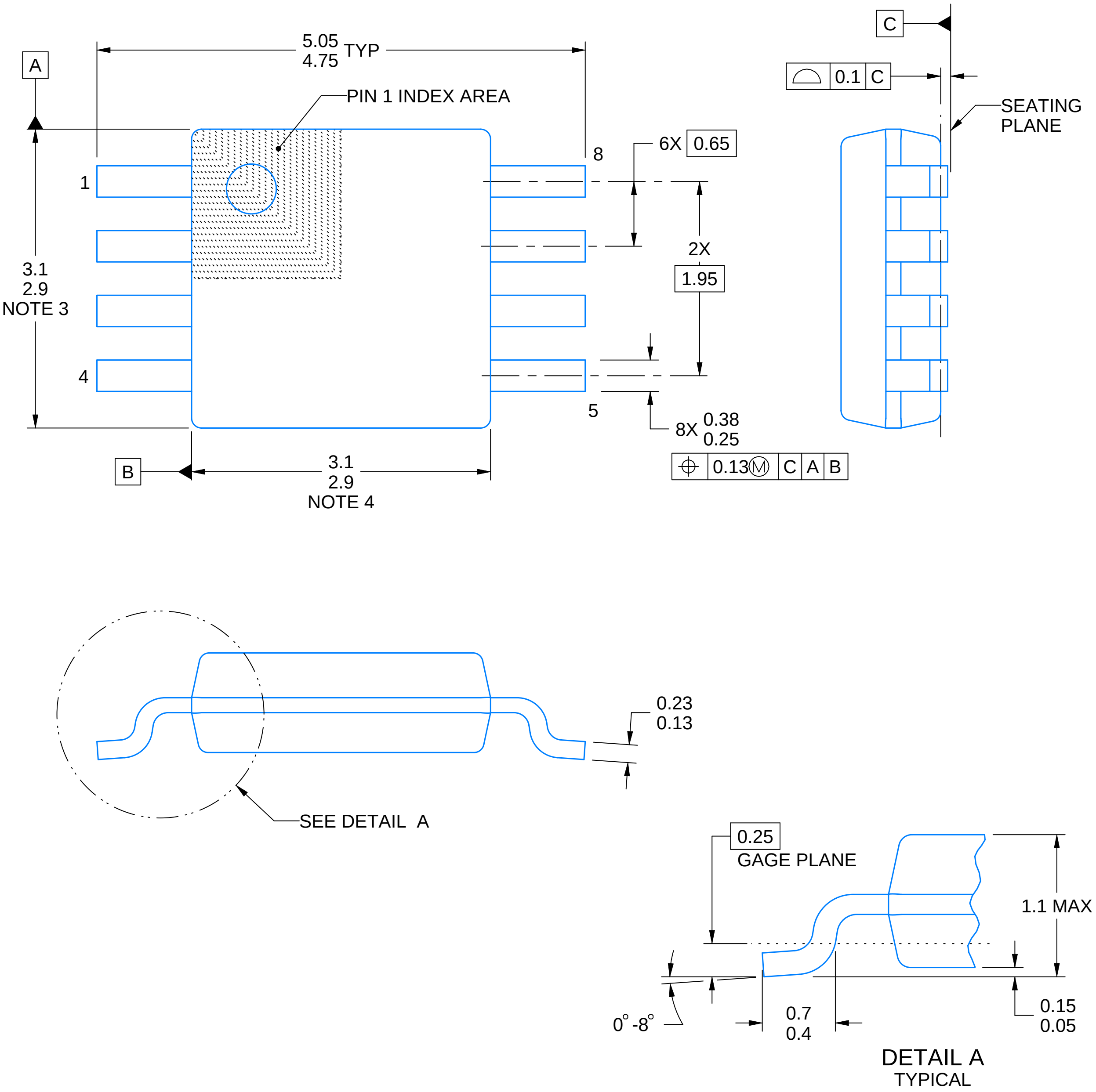
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

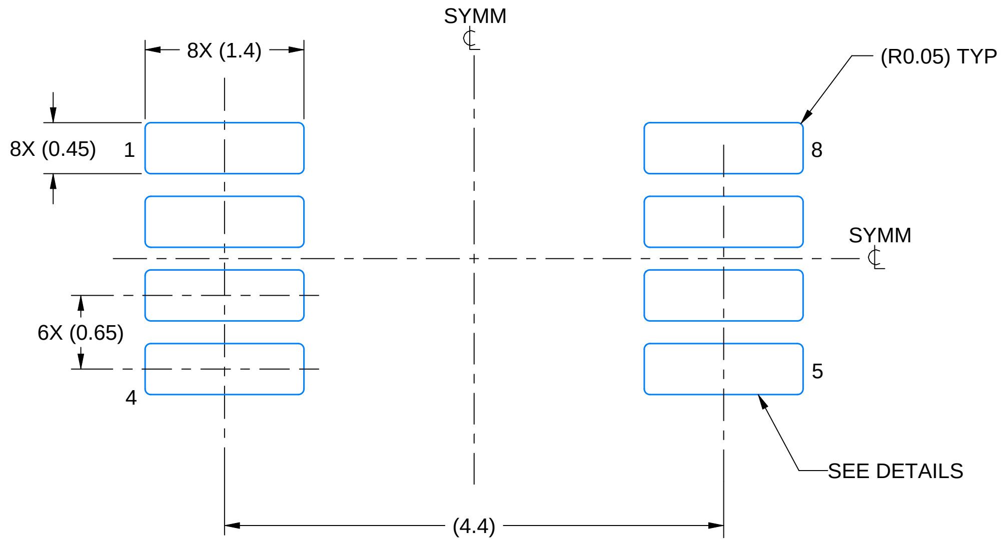


4214862/A 04/2023

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

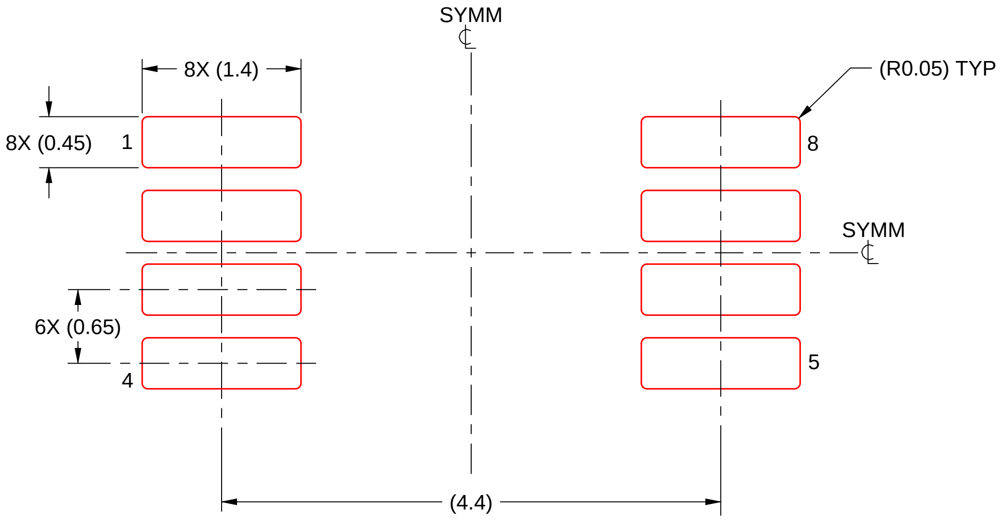
NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

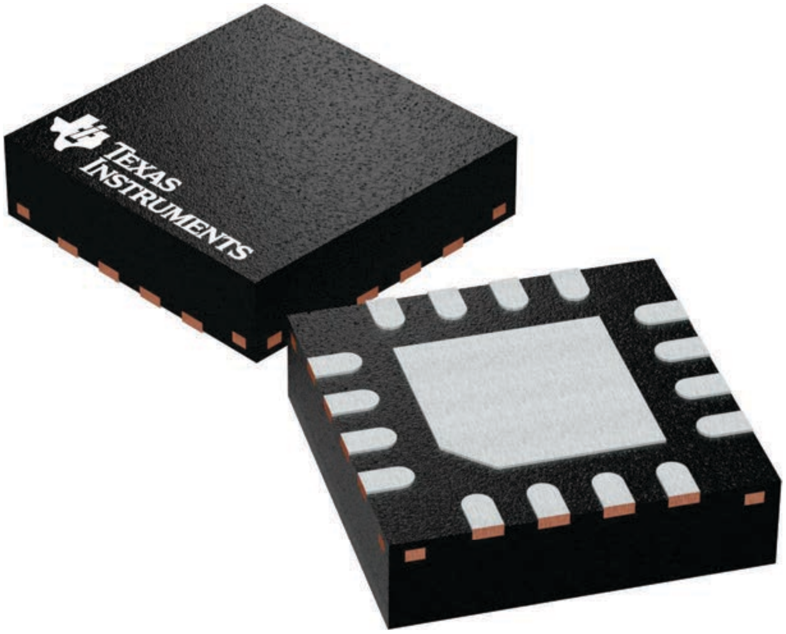
RTE 16

WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

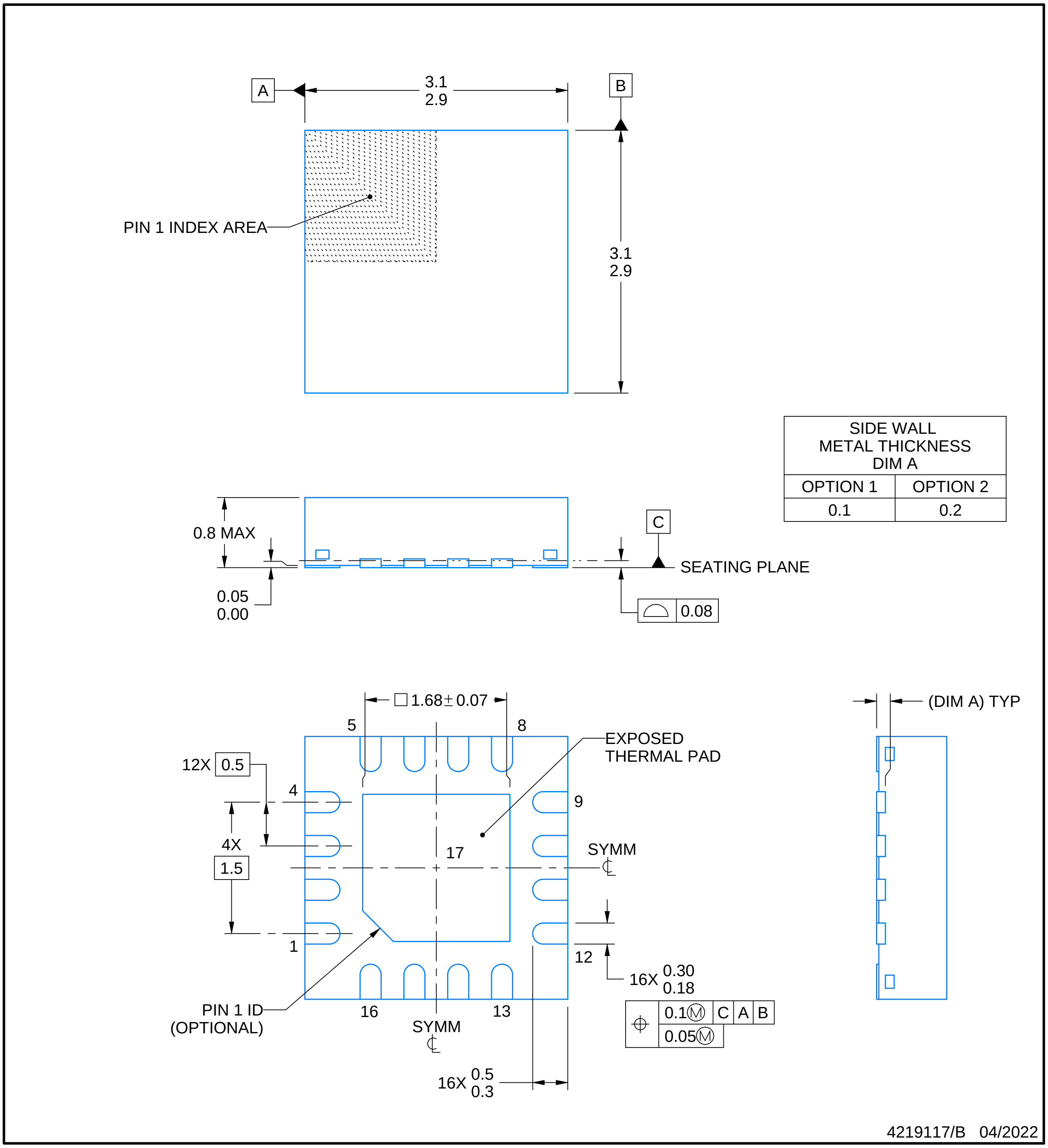
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



PACKAGE OUTLINE

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

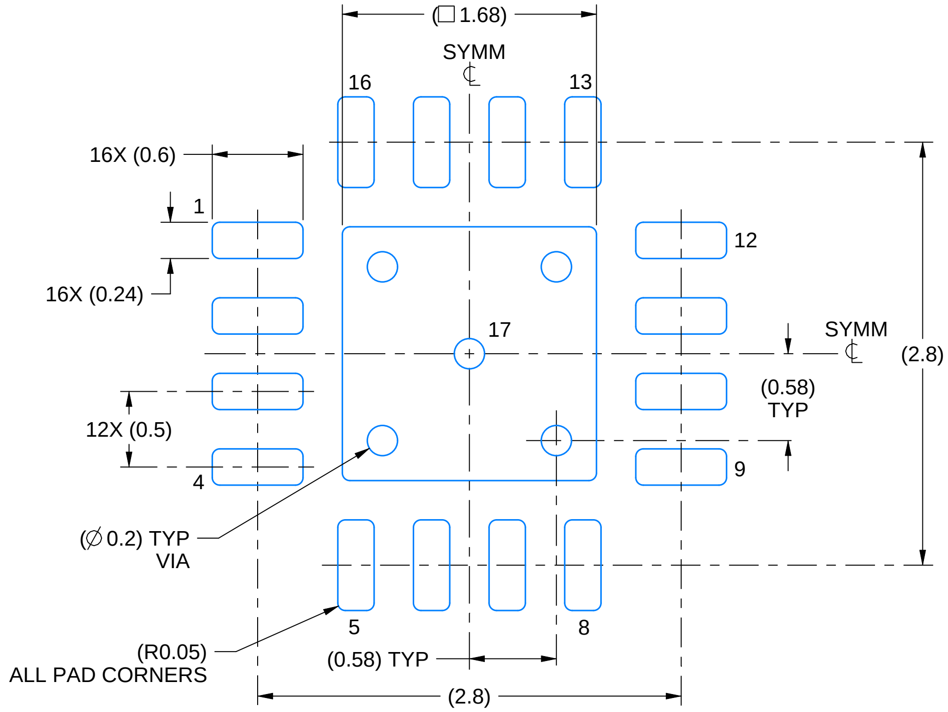


SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2

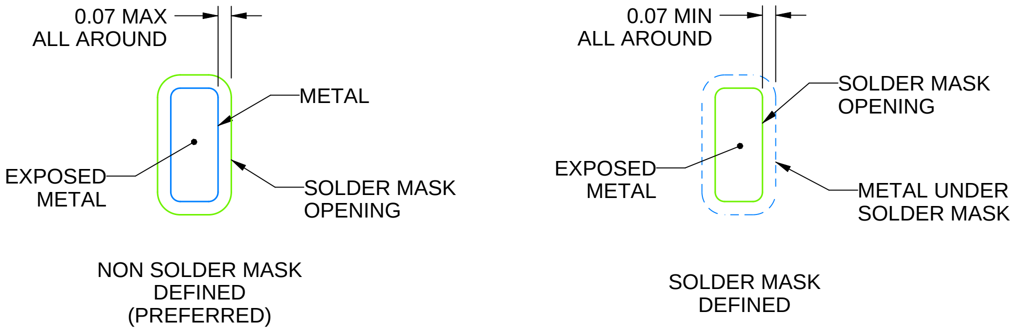
4219117/B 04/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

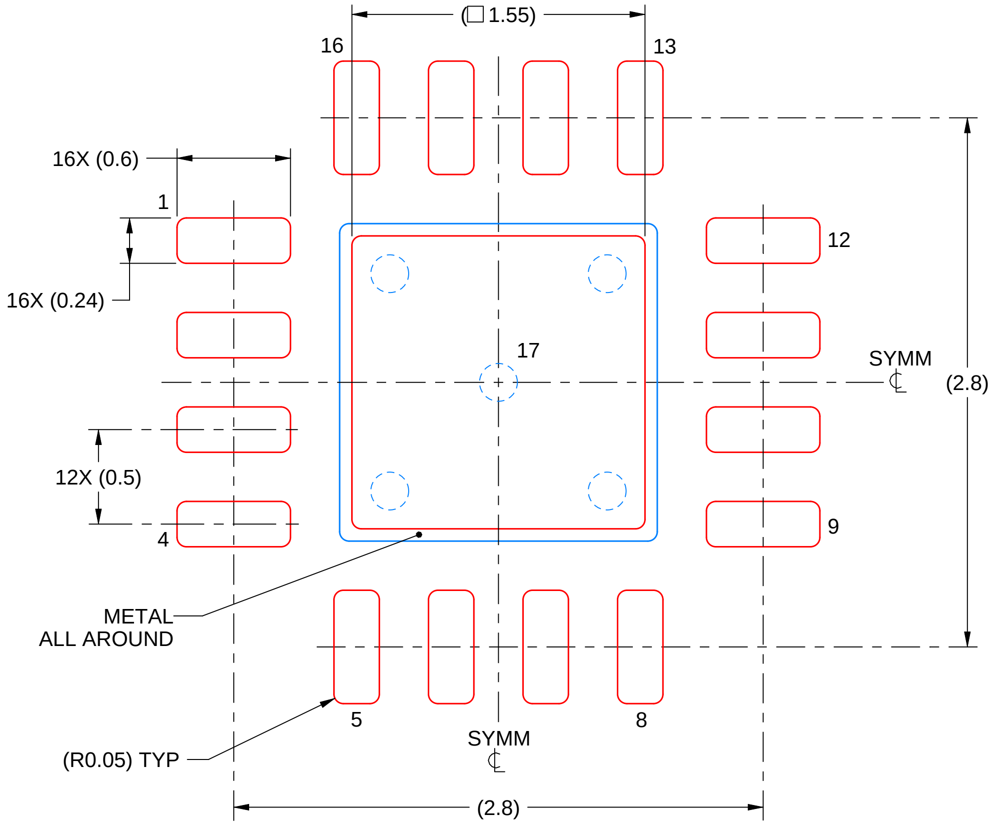


SOLDER MASK DETAILS

4219117/B 04/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

最終更新日：2025 年 10 月