TLV8801/TLV8802 コスト最適化システム向けの320nAナノパワー・オペアンプ

1 特長

- コスト最適化システム用
- ナノパワー消費電流: チャネルごとに320nA
- オフセット電圧: 4.5mV (最大値)
- 優れたTcVos: 1µV/℃
- ユニティ・ゲイン帯域幅: 6kHz
- ユニティ・ゲインで安定
- 低い入力バイアス電流: 0.1pA
- 広い電源電圧範囲: 1.7V～5.5V
- レール・ツー・レール出力
- 出力反転なし
- EMI保護
- 温度範囲: -40℃～+125℃
- 業界標準パッケージ:
  - シングル: 5ピンSOT-23
  - デュアル: 8ピンVSSOP

2 アプリケーション

- CO検出器やO_2検出器などの気体検出器
- PIRセンサを使用するモーション検出器
- イオン化煙アラーム
- サーモスタット
- リモート・センサ、IoT (Internet of Things)
- アクティブRFIDリーダーおよびタグ
- 携帯型医療機器
- 携帯型血糖値計

3 概要

TLV8801 (シングル)およびTLV8802 (デュアル)ファミリの超低消費電力オペアンプは、ワイヤレス機器および低消費電力の有線機器における、コスト最適化されたセンシング・アプリケーションに理想的です。TLV880xアンプを使用すると、CO検出器、煙検出器、モーション検出セキュリティ・システム(PIRモーション・センシングのような)など、バッテリ動作時間を重視する機器において、消費電力を最小化できます。また、注意深く設計されたCMOS入力段により、バイアス電流が非常に低い(フェムトアンペア単位)ため、メガオームのフィードバック抵抗を含むトランスインピーダンス・アンプ(TIA)構成や、ソース・インピーダンスの高いセンシング・アプリケーションなど、感度の高いアプリケーションに影響を及ぼすようなI_{BIAS}やI_{OS}の誤差が低減されます。さらに、EMI保護が組み込まれているため、携帯電話、WiFi、無線送信機、タグ・リーダーなどのソースから発生する不要なRF信号への感受性が低下しています。

TLV8801 (シングル)およびTLV8802 (デュアル)バージョンは、それぞれ業界標準の5ピンのSOT-23および8ピンのVSSOPパッケージで供給されます。

LPV80xおよびTLV880xナノパワー・アンプ

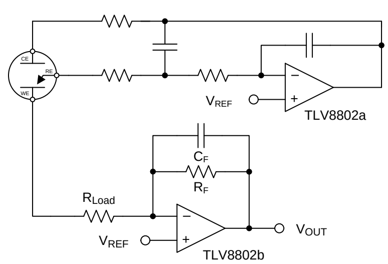
型番	チャネル	消費電流 (標準値/チャネル)	オフセット電圧 (最大値)
TLV8801	1	450nA	4.5mV
TLV8802	2	320nA	4.5mV
LPV801	1	450nA	3.5mV
LPV802	2	320nA	3.5mV

製品情報(1)

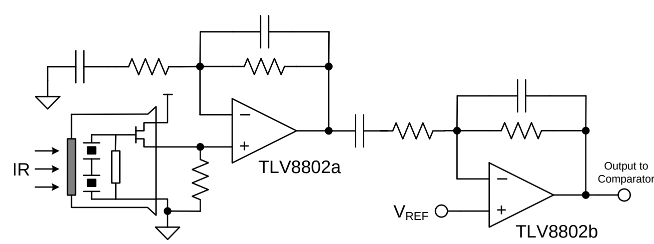
型番	パッケージ	本体サイズ
TLV8801	SOT-23 (5)	2.90mm×1.60mm
TLV8802	VSSOP (8)	3.00mm×3.00mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

ナノパワー電気化学センサ・アンプ



ナノパワーPIRモーション・センサ・アンプ



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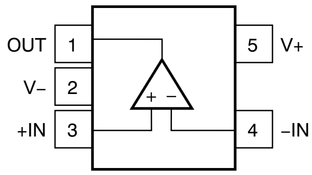
4 改訂履歴

2016年8月発行のものから更新 **Page**

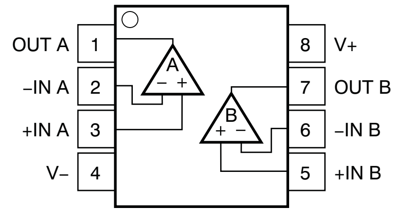
- LPVおよびTLVナノパワー・アンプの表のタイトルと、'01の消費電流を 変更 1
- Added seporate CMRR row for TLV8801 5
- Changed TLV8801 Typical supply current from 500nA to 450nA 5

5 Pin Configuration and Functions

TLV8801 5-Pin SOT-23
DBV Package
Top View



TLV8802 8-Pin VSSOP
DGK Package
Top View



Pin Functions: TLV8801 DBV

PIN		I/O	DESCRIPTION
NAME	NUMBER		
OUT	1	O	Output
-IN	4	I	Inverting Input
+IN	3	I	Non-Inverting Input
V-	2	P	Negative (lowest) power supply
V+	5	P	Positive (highest) power supply

Pin Functions: TLV8802 DGK

PIN		I/O	DESCRIPTION
NAME	NUMBER		
OUT A	1	O	Channel A Output
-IN A	2	I	Channel A Inverting Input
+IN A	3	I	Channel A Non-Inverting Input
V-	4	P	Negative (lowest) power supply
+IN B	5	I	Channel B Non-Inverting Input
-IN B	6	I	Channel B Inverting Input
OUT B	7	O	Channel B Output
V+	8	P	Positive (highest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
Supply voltage, V_s = (V+) - (V-)			–0.3	6	V
Input pins	Voltage (2) (3)	Common mode	(V-) - 0.3	(V+) + 0.3	V
		Differential	(V-) - 0.3	(V+) + 0.3	V
Input pins	Current		-10	10	mA
Output short current (4)			Continuous	Continuous	
Storage temperature, T_{stg}			–65	150	°C
Junction temperature				150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Not to exceed -0.3V or +6.0V on ANY pin, referred to V-
(3) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails should be current-limited to 10 mA or less.
(4) Short-circuit to Vs/2, one amplifer per package. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±750 V may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage (V+ – V–)	1.7		5.5	V
Specified temperature	-40		125	°C

6.4 Thermal Information

THERMAL METRIC (1)		TLV8801 DBV 5 PINS	TLV8802 DGK 8 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	177.4	177.6	ºC/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	133.9	68.8	
θ_{JB}	Junction-to-board thermal resistance	36.3	98.2	
ψ_{JT}	Junction-to-top characterization parameter	23.6	12.3	
ψ_{JB}	Junction-to-board characterization parameter	35.7	96.7	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

T_A = 25°C, V_S = 1.8V to 5 V, $V_{CM} = V_{OUT} = V_S/2$, and $R_L \geq 10\ M\Omega$ to V_S / 2, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE					

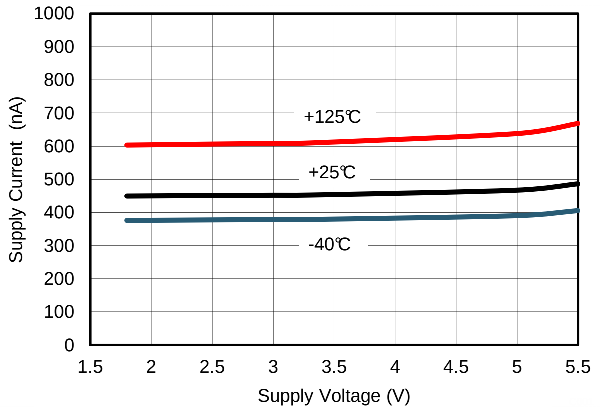
Electrical Characteristics (continued)

T_A = 25°C, V_S = 1.8V to 5 V, V_{CM} = V_{OUT} = V_S/2, and R_L≥ 10 MΩ to V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OS}	Input offset voltage	V_S = 1.8V, 3.3V, and 5V, V_{CM} = V-			0.55	±4.5	mV
		V_S = 1.8V, 3.3V, and 5V, V_{CM} = (V+) – 0.9 V			0.55	±4.5	
$\Delta V_{OS}/\Delta T$	Input offset drift	V_{CM} = V-	T_A = –40°C to 125°C		1		µV/°C
PSRR	Power-supply rejection ratio	V_S = 1.8V to 5V, V_{CM} = V-			1.6	60	µV/V
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range	V_S = 5 V		0		4.1	V
CMRR	Common-mode rejection ratio, TLV8801	(V–) ≤ V_{CM} ≤ (V+) – 0.9 V, V_S= 5V		77	87		dB
	Common-mode rejection ratio, TLV8802	(V–) ≤ V_{CM} ≤ (V+) – 0.9 V, V_S= 5V		80	90		dB
INPUT BIAS CURRENT							
I_B	Input bias current	V_S = 1.8V			±100		fA
I_{OS}	Input offset current	V_S = 1.8V			±100		
INPUT IMPEDANCE							
	Differential				7		pF
	Common mode				3		
NOISE							
E_n	Input voltage noise	f = 0.1 Hz to 10 Hz			12		µVp-p
e_n	Input voltage noise density	f = 100 Hz			340		nV/√Hz
		f = 1 kHz			450		
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 0.3 V ≤ V_O ≤ (V+) – 0.3 V, R_L = 100 kΩ			120		dB
OUTPUT							
V_{OH}	Voltage output swing from positive rail	V_S = 1.8V, R_L = 100 kΩ to V^+/2		10	3.5		mV
V_{OL}	Voltage output swing from negative rail	V_S = 1.8V, R_L = 100 kΩ to V^+/2			2.5	10	
I_{SC}	Short-circuit current	V_S = 3.3V, Short to V_S/2			4.7		mA
Z_O	Open loop output impedance	f = 1 kHz, I_O = 0 A			90		kΩ
FREQUENCY RESPONSE							
GBP	Gain-bandwidth product	C_L = 20 pF, R_L = 10 MΩ, V_S = 5V			6		kHz
SR	Slew rate (10% to 90%)	G = 1, Rising Edge, C_L = 20 pF, V_S = 5V			1.4		V/ms
		G = 1, Falling Edge, C_L = 20 pF, V_S = 5V			1.5		
POWER SUPPLY							
$I_{Q-TLV8801}$	Quiescent Current	V_{CM} = V-, I_O = 0, V_S = 3.3 V			450	700	nA
$I_{Q-TLV8802}$	Quiescent Current, Per Channel	V_{CM} = V-, I_O = 0, V_S = 3.3 V			320	650	nA

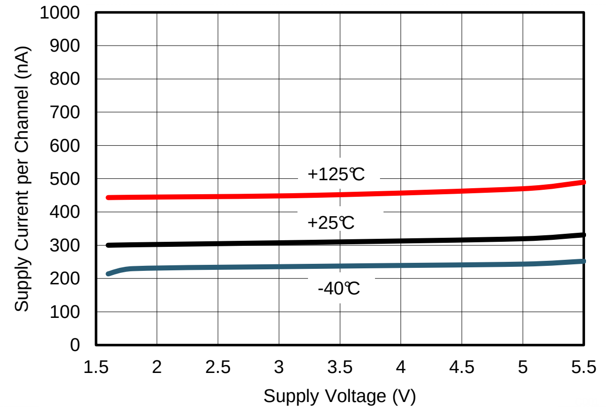
6.6 Typical Characteristics

at T_A = 25°C, R_L = 10MΩ to V_S/2 ,C_L = 20pF, V_{CM} = V_S / 2V unless otherwise specified.



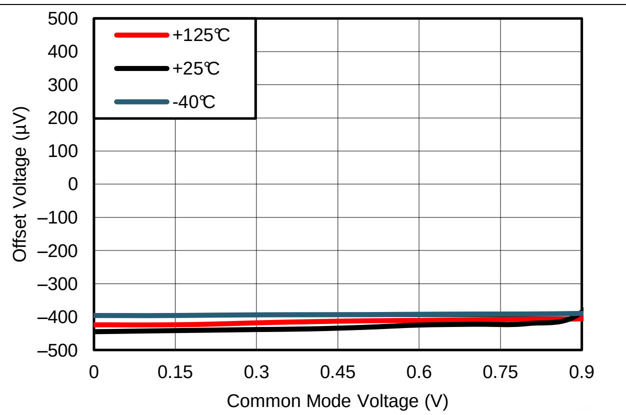
V_{CM} = V-　TLV8801　R_L=No Load

Figure 1. Supply Current vs. Supply Voltage, TLV8801



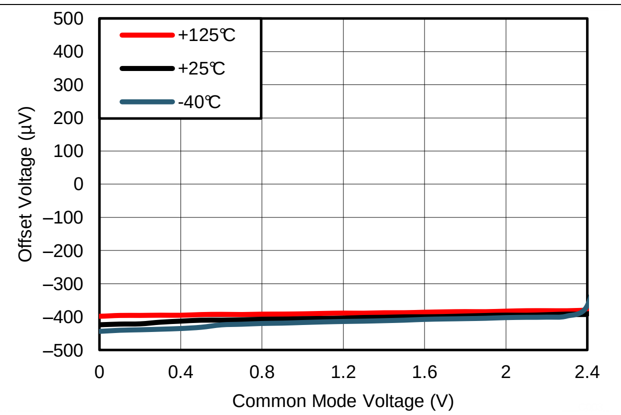
V_{CM} = V-　TLV8802　R_L=No Load

Figure 2. Supply Current vs. Supply Voltage, TLV8802



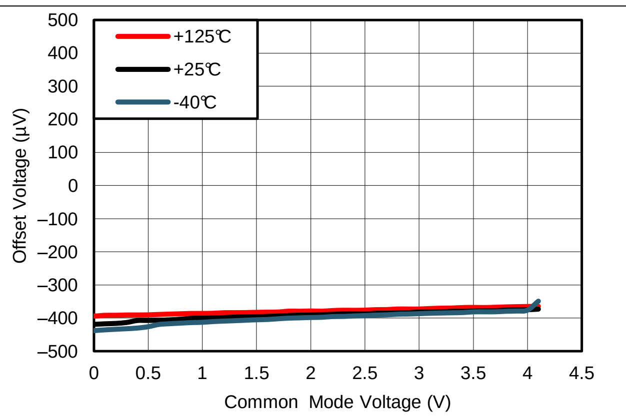
V_S= 1.8V　R_L= 10MΩ

Figure 3. Typical Offset Voltage vs. Common Mode Voltage



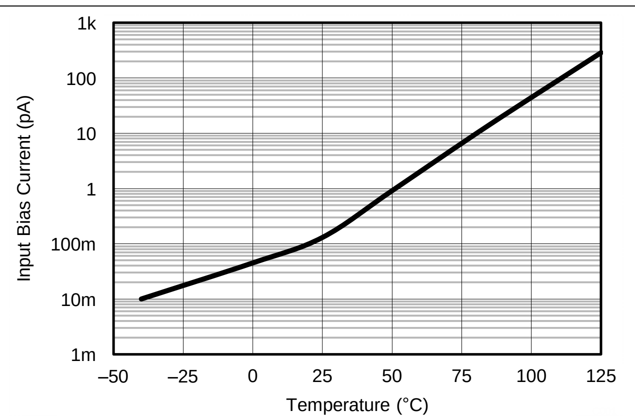
V_S= 3.3V　R_L= 10MΩ

Figure 4. Typical Offset Voltage vs. Common Mode Voltage



V_S= 5V　R_L= 10MΩ

Figure 5. Typical Offset Voltage vs. Common Mode Voltage



V_S= 5V　T_A = -40 to 125　V_{CM} = Vs/2

Figure 6. Input Bias Current vs. Temperature

Typical Characteristics (continued)

at T_A = 25°C, R_L = 10MΩ to V_S/2 ,C_L = 20pF, V_{CM} = V_S / 2V unless otherwise specified.

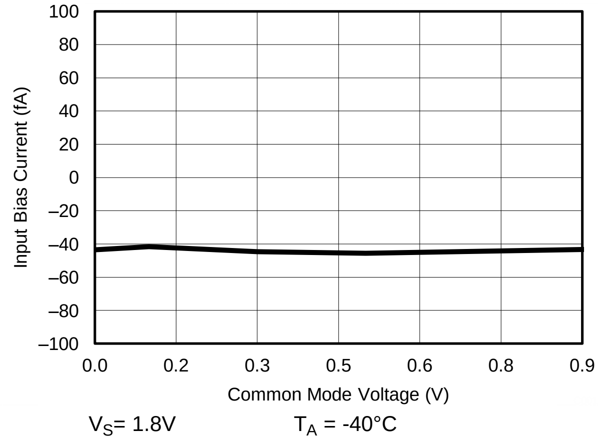


Figure 7. Input Bias Current vs. Common Mode Voltage

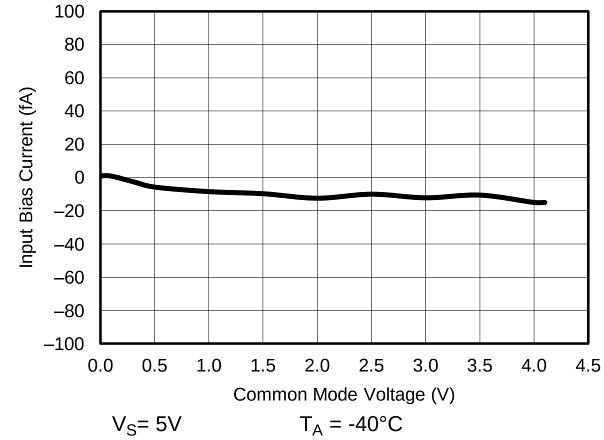


Figure 8. Input Bias Current vs. Common Mode Voltage

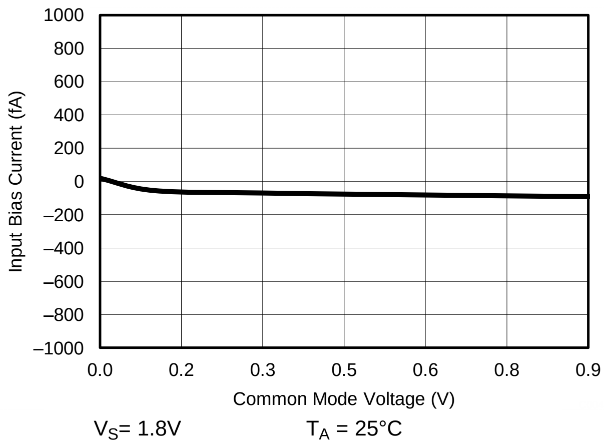


Figure 9. Input Bias Current vs. Common Mode Voltage

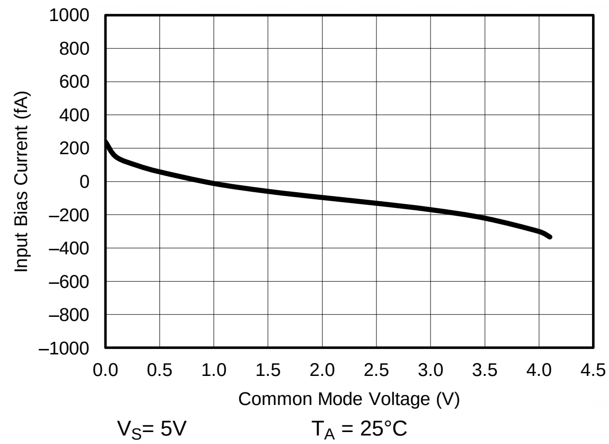


Figure 10. Input Bias Current vs. Common Mode Voltage

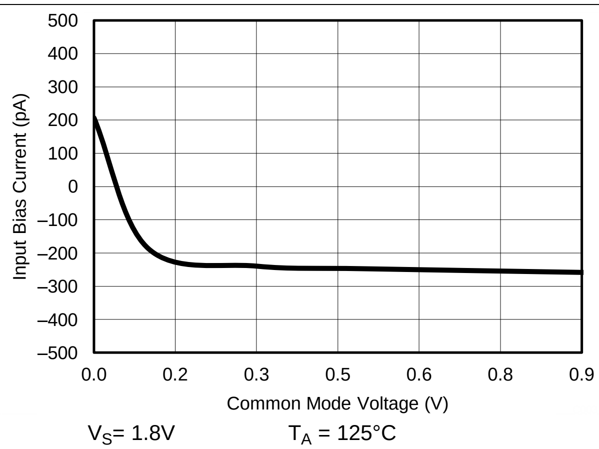


Figure 11. Input Bias Current vs. Common Mode Voltage

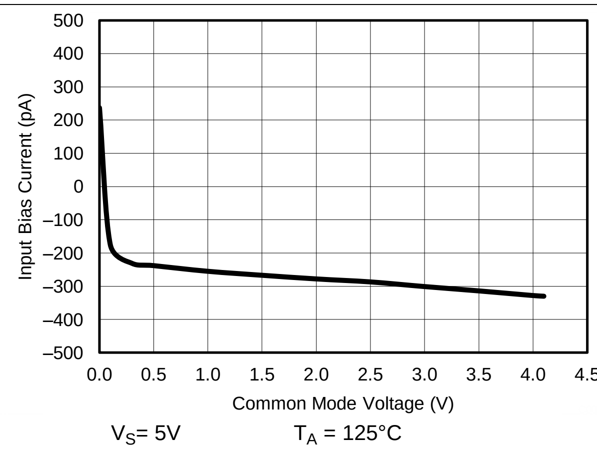


Figure 12. Input Bias Current vs. Common Mode Voltage

Typical Characteristics (continued)

at T_A = 25°C, R_L = 10MΩ to V_S/2 ,C_L = 20pF, V_{CM} = V_S / 2V unless otherwise specified.

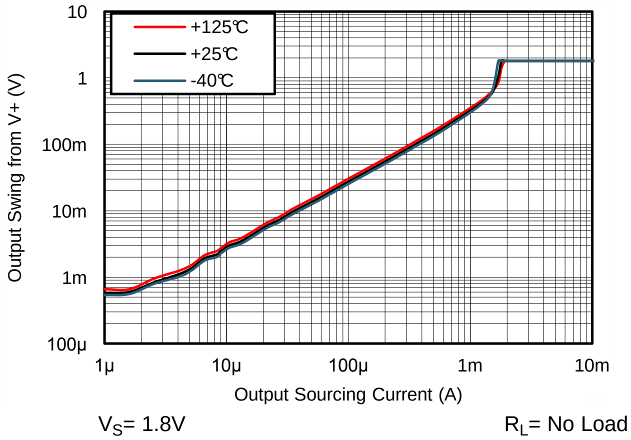


Figure 13. Output Swing vs. Sourcing Current, 1.8V

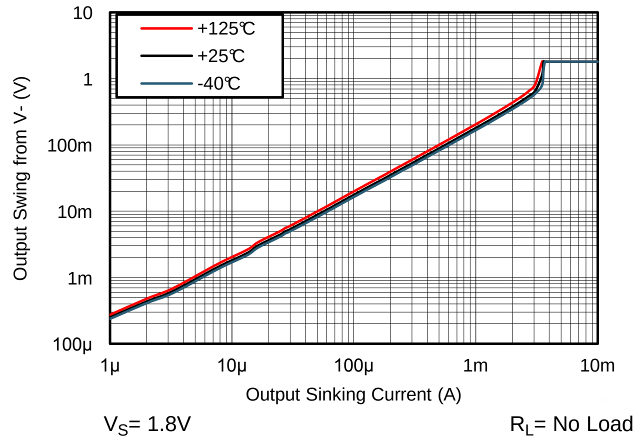


Figure 14. Output Swing vs. Sinking Current, 1.8V

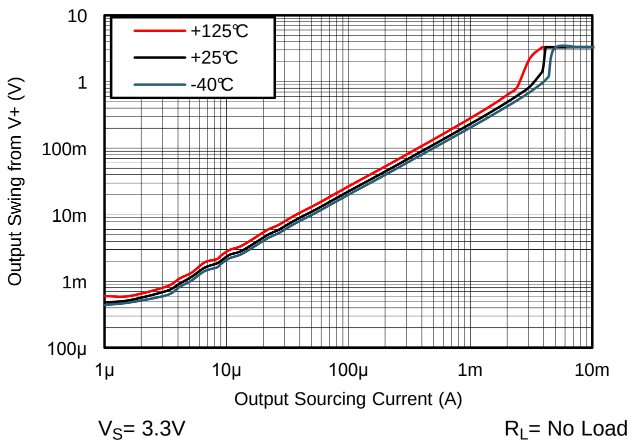


Figure 15. Output Swing vs. Sourcing Current, 3.3V

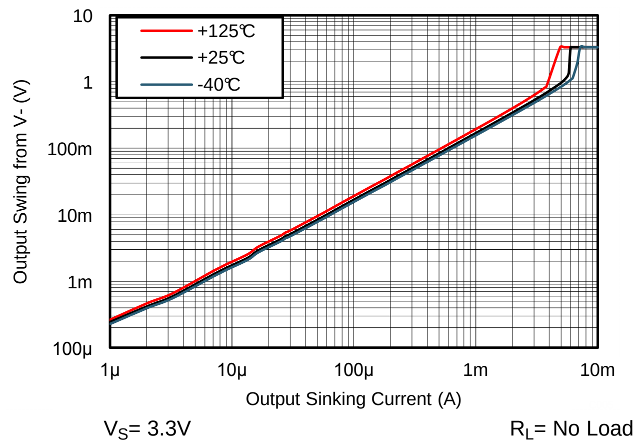


Figure 16. Output Swing vs. Sinking Current, 3.3V

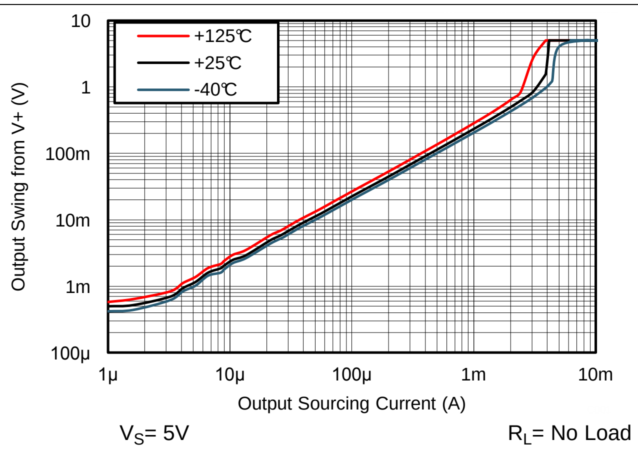


Figure 17. Output Swing vs. Sourcing Current, 5V

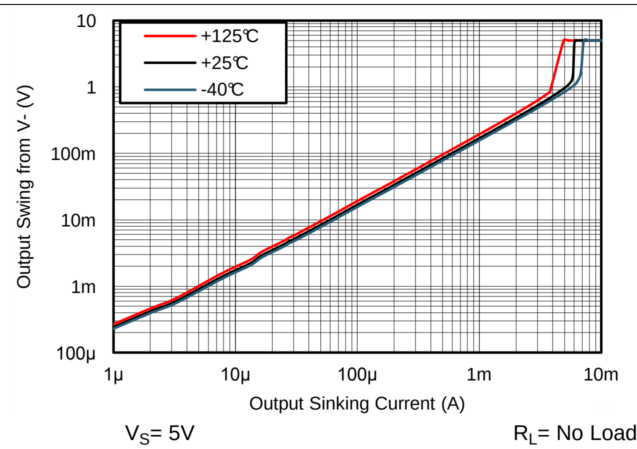
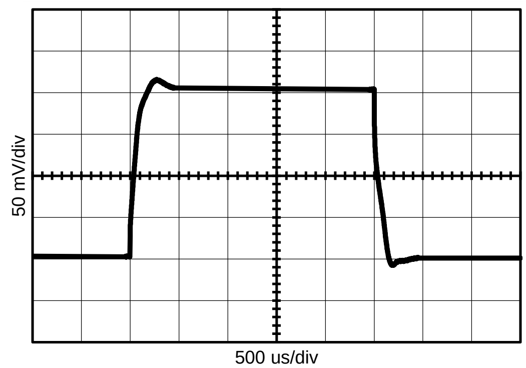


Figure 18. Output Swing vs. Sinking Current, 5V

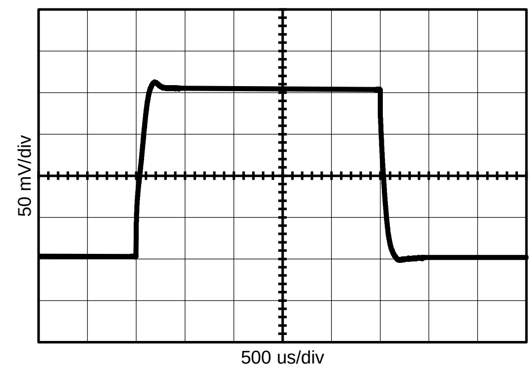
Typical Characteristics (continued)

at T_A = 25°C, R_L = 10MΩ to V_S/2 ,C_L = 20pF, V_{CM} = V_S / 2V unless otherwise specified.



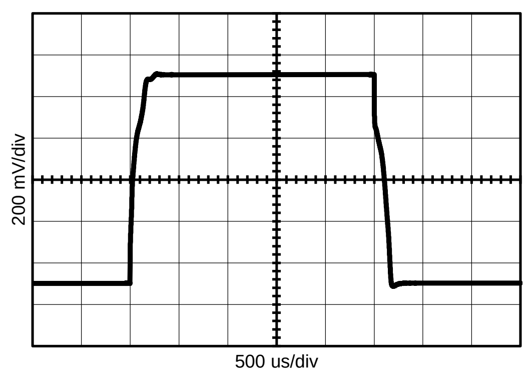
T_A = 25 | R_L= 10MΩ | Vout = 200mVpp
V_S= ±0.9V | C_L= 20pF | A_V = +1

Figure 19. Small Signal Pulse Response, 1.8V



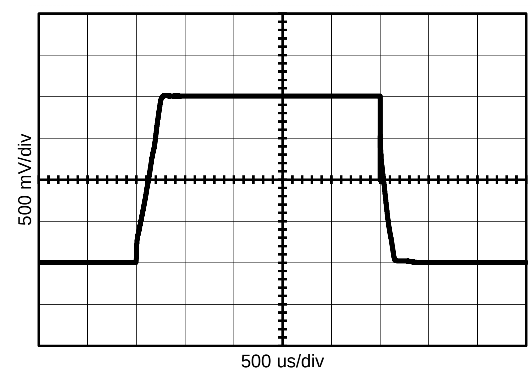
T_A = 25 | R_L= 10MΩ | Vout = 200mVpp
V_S= ±2.5V | C_L= 20pF | A_V = +1

Figure 20. Small Signal Pulse Response, 5V



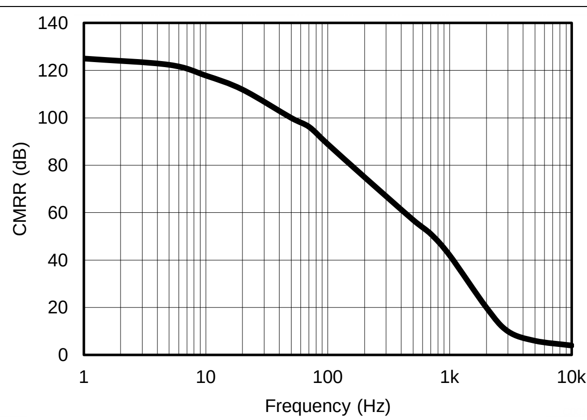
T_A = 25 | R_L= 10MΩ | Vout = 1Vpp
V_S= ±0.9V | C_L= 20pF | A_V = +1

Figure 21. Large Signal Pulse Response, 1.8V



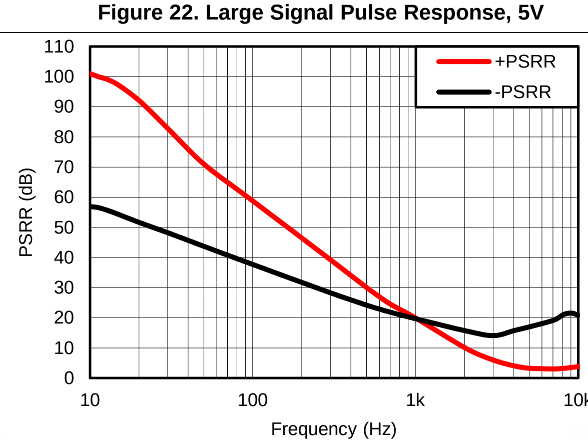
T_A = 25 | R_L= 10MΩ | Vout = 2Vpp
V_S= ±2.5V | C_L= 20pF | A_V = +1

Figure 22. Large Signal Pulse Response, 5V



T_A = 25 | R_L= 10MΩ | ΔV_{CM} = 0.5Vpp
V_S= 5V | C_L= 20p
V_{CM} = Vs/2 | A_V = +1

Figure 23. CMRR vs Frequency

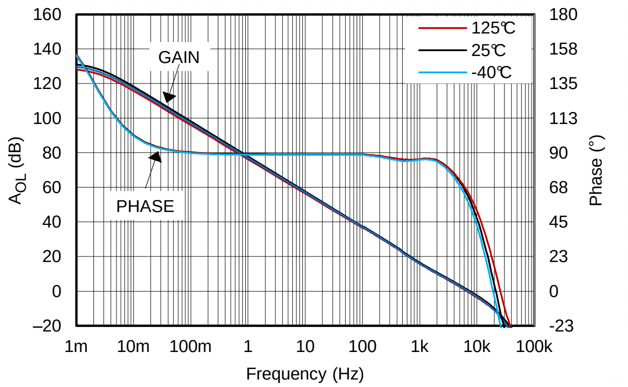


T_A = 25 | R_L= 10MΩ | ΔV_S = 0.5Vpp
V_S= 3.3V | C_L= 20p
V_{CM} = Vs/2 | A_V = +1

Figure 24. ±PSRR vs Frequency

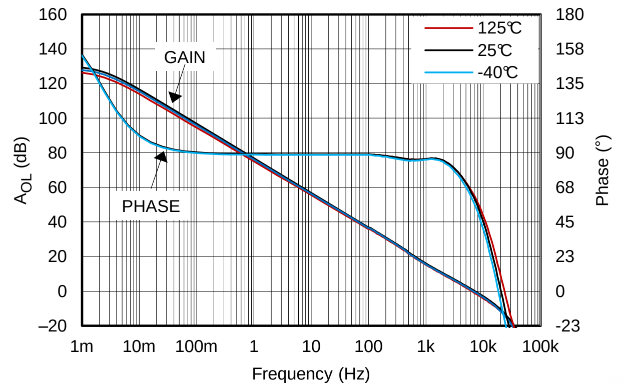
Typical Characteristics (continued)

at T_A = 25°C, R_L = 10MΩ to V_S/2 ,C_L = 20pF, V_{CM} = V_S / 2V unless otherwise specified.



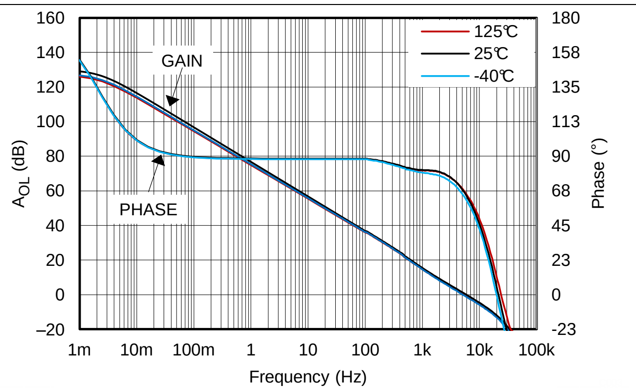
T_A = -40, 25, 125°C　R_L= 10MΩ　V_{OUT} = 200mV_{PP}
V_S= 5V　C_L= 20pF　V_{CM} = Vs/2

Figure 25. Open Loop Gain and Phase, 5V, 10 MΩ Load



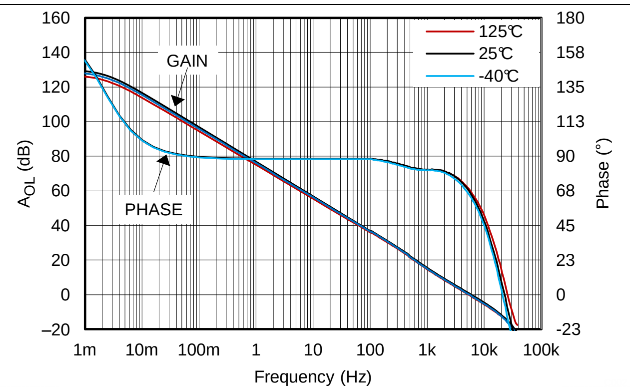
T_A = -40, 25, 125°C　R_L= 10MΩ　V_{OUT} = 200mV_{PP}
V_S= 3.3V　C_L= 20pF　V_{CM} = Vs/2

Figure 26. Open Loop Gain and Phase, 3.3V, 10 MΩ Load



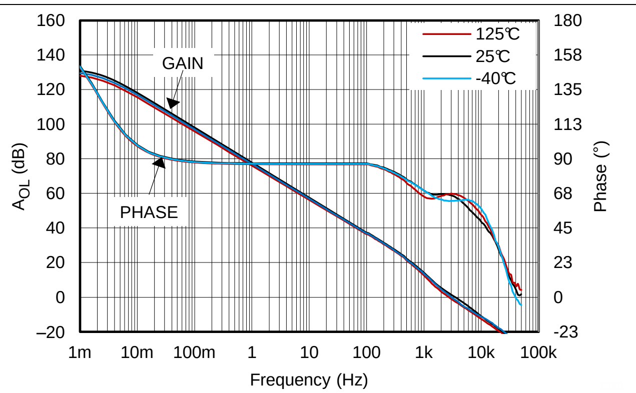
T_A = -40, 25, 125°C　R_L= 1MΩ　V_{OUT} = 200mV_{PP}
V_S= 5V　C_L= 20pF　V_{CM} = Vs/2

Figure 27. Open Loop Gain and Phase, 5V, 1 MΩ Load



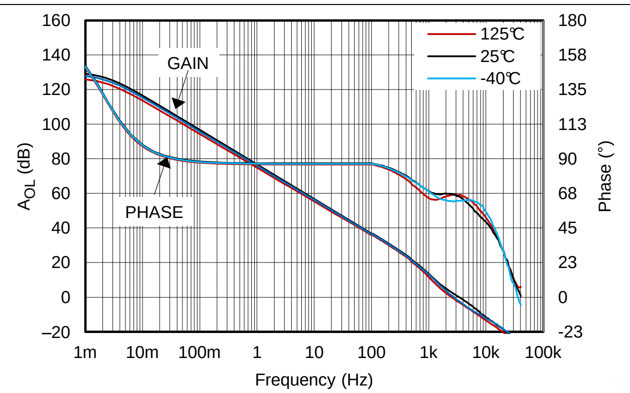
T_A = -40, 25, 125°C　R_L= 1MΩ　V_{OUT} = 200mV_{PP}
V_S= 3.3V　C_L= 20pF　V_{CM} = Vs/2

Figure 28. Open Loop Gain and Phase, 3.3V, 1 MΩ Load



T_A = -40, 25, 125°C　R_L= 100kΩ　V_{OUT} = 200mV_{PP}
V_S= 5V　C_L= 20pF　V_{CM} = Vs/2

Figure 29. Open Loop Gain and Phase, 5V, 100kΩ Load

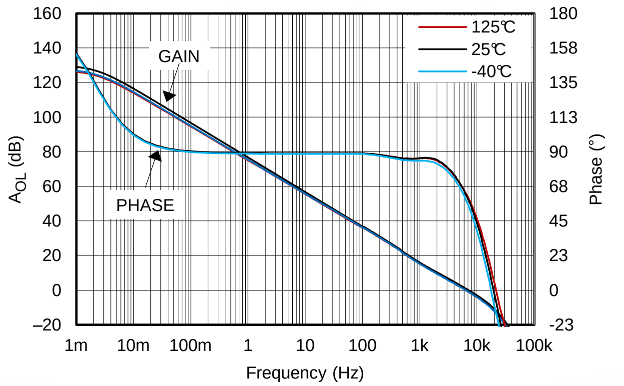


T_A = -40, 25, 125°C　R_L= 100kΩ　V_{OUT} = 200mV_{PP}
V_S= 3.3V　C_L= 20pF　V_{CM} = Vs/2

Figure 30. Open Loop Gain and Phase, 3.3V, 100kΩ Load

Typical Characteristics (continued)

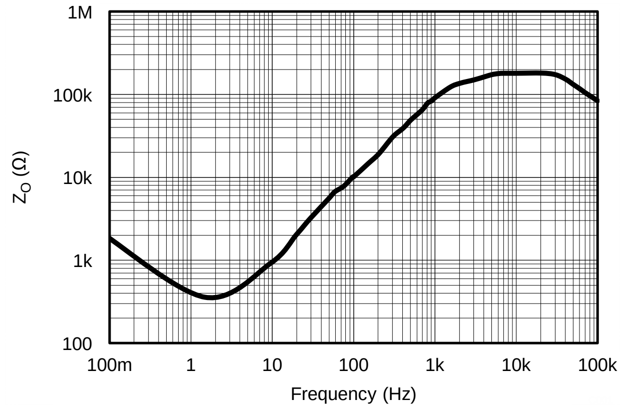
at T_A = 25°C, R_L = 10MΩ to V_S/2 ,C_L = 20pF, V_{CM} = V_S / 2V unless otherwise specified.



T_A = -40, 25, 125°C R_L= 10MΩ V_{OUT} = 200mV$_{PP}$

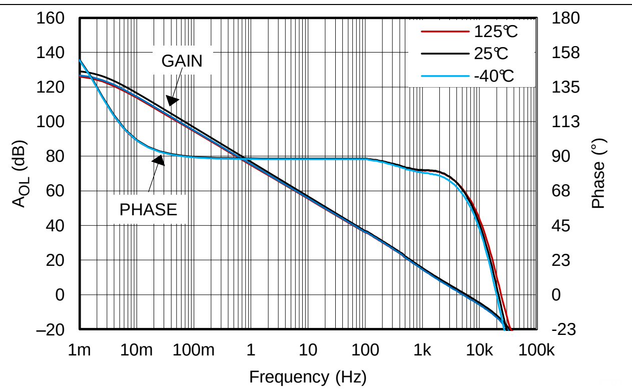
V_S= 1.8V C_L= 20pF V_{CM} = Vs/2

Figure 31. Open Loop Gain and Phase, 1.8V, 10 MΩ Load



T_A = 25°C V_S= 5 V R_L= 10MΩ

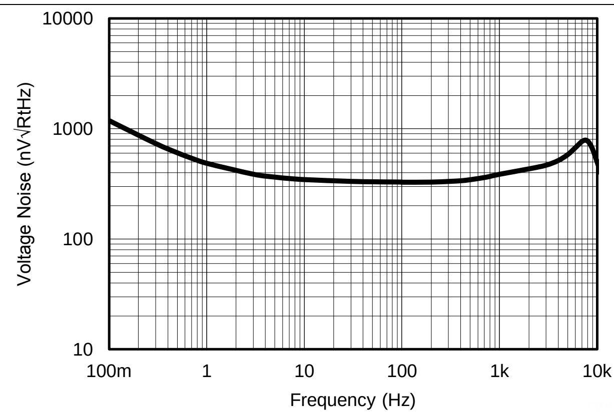
Figure 32. Open Loop Output Impedance



T_A = -40, 25, 125°C R_L= 1MΩ V_{OUT} = 200mV$_{PP}$

V_S= 1.8V C_L= 20pF V_{CM} = Vs/2

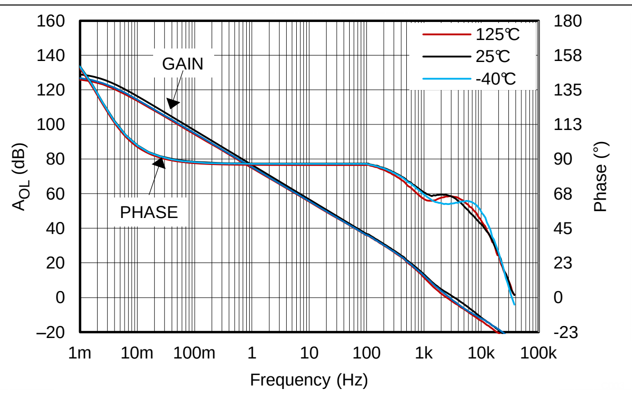
Figure 33. Open Loop Gain and Phase, 1.8V, 1 MΩ Load



T_A = 25 R_L= 1MΩ V_{CM} = Vs/2

V_S= 5V C_L= 20pF A_V = +1

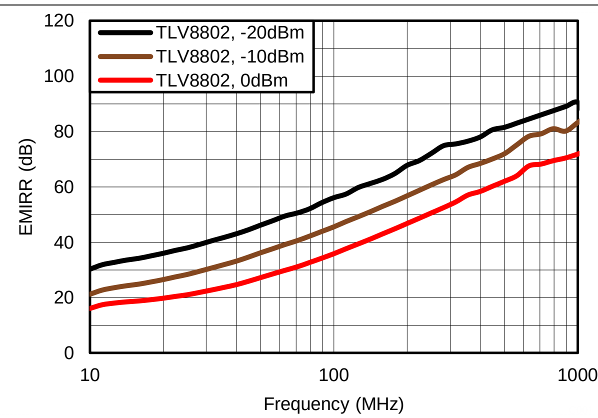
Figure 34. Input Voltage Noise vs Frequency



T_A = -40, 25, 125°C R_L= 100kΩ V_{OUT} = 200mV$_{PP}$

V_S= 1.8V C_L= 20pF V_{CM} = Vs/2

Figure 35. Open Loop Gain and Phase, 1.8V, 100kΩ Load



T_A = 25 R_L= 1MΩ V_{CM} = Vs/2

V_S= 3.3V C_L= 20pF A_V = +1

Figure 36. EMIRR Performance

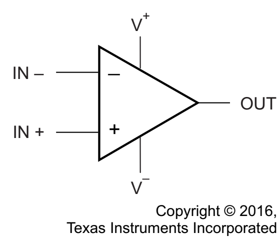
7 Detailed Description

7.1 Overview

The TLV8801 (single) and TLV8802 (dual) series nanoPower CMOS operational amplifiers are designed for long-life battery-powered and energy harvested applications. They operate on a single supply with operation as low as 1.7 V. The output is rail-to-rail and swings to within 3.5mV of the supplies with a 100kΩ load. The common-mode range extends to the negative supply making it ideal for single-supply applications. EMI protection has been employed internally to reduce the effects of EMI.

Parameters that vary significantly with operating voltages or temperature are shown in the *Typical Characteristics* curves.

7.2 Functional Block Diagram



7.3 Feature Description

The amplifier's differential inputs consist of a non-inverting input (+IN) and an inverting input (–IN). The amplifer amplifies only the difference in voltage between the two inputs, which is called the differential input voltage. The output voltage of the op-amp V_{OUT} is given by Equation 1:

$$V_{OUT} = A_{OL} \, (IN^+ - IN^-) \tag{1}$$

where

- A_{OL} is the open-loop gain of the amplifier, typically around 120 dB (1,000,000x, or 1,000,000 Volts per microvolt).

7.4 Device Functional Modes

7.4.1 Negative-Rail Sensing Input

The input common-mode voltage range of the TLV880x extends from (V-) to (V+) – 0.9 V. In this range, low offset can be expected with a minimum of 80dB CMRR. The TLV880x is protected from output "inversions" or "reversals".

7.4.2 Rail to Rail Output Stage

The TLV880x output voltage swings 3.5 mV from rails at 1.8 V supply, which provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

The TLV880x Maximum Output Voltage Swing graph defines the maximum swing possible under a particular output load.

7.4.3 Design Optimization for Nanopower Operation

When designing for ultralow power, choose system feedback components carefully. To minimize quiecent current consumption, select large-value feedback resistors. Any large resistors will react with stray capacitance in the circuit and the input capacitance of the operational amplifier. These parasitic RC combinations can affect the stability of the overall system. A feedback capacitor may be required to assure stability and limit overshoot or gain peaking.

When possible, use AC coupling and AC feedback to reduce static current draw through the feedback elements. Use film or ceramic capacitors since large electolytics may have large static leakage currents in the nanoamps.

Device Functional Modes (continued)

7.4.4 Driving Capacitive Load

The TLV880x is internally compensated for stable unity gain operation, with a 6 kHz typical gain bandwidth. However, the unity gain follower is the most sensitive configuration to capacitive load. The combination of a capacitive load placed directly on the output of an amplifier along with the amplifier's output impedance creates a phase lag, which reduces the phase margin of the amplifier. If the phase margin is significantly reduced, the response will be under damped which causes peaking in the transfer and, when there is too much peaking, the op amp might start oscillating.

In order to drive heavy (>50pF) capacitive loads, an isolation resistor, R_{ISO}, should be used, as shown in Figure 37. By using this isolation resistor, the capacitive load is isolated from the amplifier's output. The larger the value of R_{ISO}, the more stable the amplifier will be. If the value of R_{ISO} is sufficiently large, the feedback loop will be stable, independent of the value of C_L. However, larger values of R_{ISO} result in reduced output swing and reduced output current drive. The recommended value for R_{ISO} is 30-50kΩ.

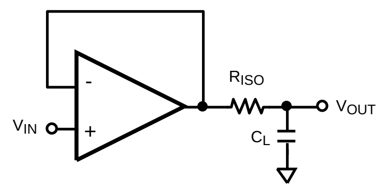


Figure 37. Resistive Isolation Of Capacitive Load

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLV880x is a ultra-low power operational amplifier that provides 6 kHz bandwidth with only 320nA typical quiescent current, and near precision drift specifications. These rail-to-rail output amplifiers are specifically designed for battery-powered applications. The input common-mode voltage range extends to the negative supply rail and the output swings to within millivolts of the rails, maintaining a wide dynamic range.

8.2 Typical Application: Three Terminal CO Gas Sensor Amplifier

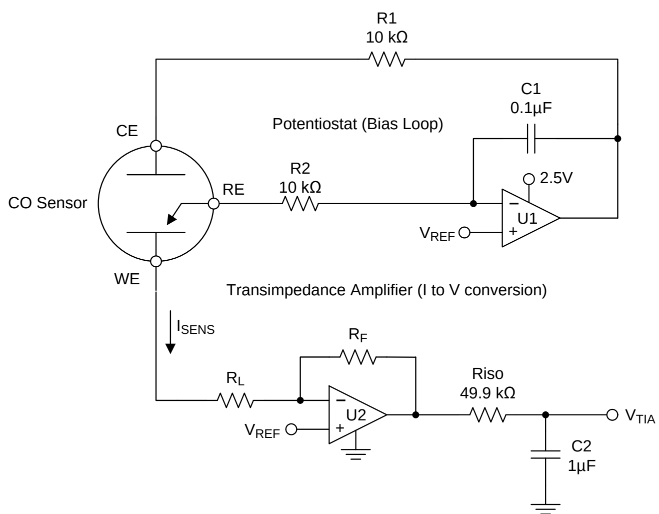


Figure 38. Three Terminal Gas Sensor Amplifer Schematic

8.2.1 Design Requirements

Figure 38 shows a simple micropower potentiostat circuit for use with three terminal unbiased CO sensors, though it is applicable to many other type of three terminal gas sensors or electrochemical cells.

The basic sensor has three electrodes; The Sense or Working Electrode ("WE"), Counter Electrode ("CE") and Reference Electrode ("RE"). A current flows between the CE and WE proportional to the detected concentration.

The RE monitors the potential of the internal reference point. For an unbiased sensor, the WE and RE electrodes must be maintained at the same potential by adjusting the bias on CE. Through the Potentiostat circuit formed by U1, the servo feedback action will maintain the RE pin at a potential set by V_{REF}.

R1 is to maintain stability due to the large capacitance of the sensor. C1 and R2 form the Potentiostat integrator and set the feedback time constant.

U2 forms a transimpedance amplifier ("TIA") to convert the resulting sensor current into a proportional voltage. The transimpedance gain, and resulting sensitivity, is set by R_F according to Equation 2.

$$V_{TIA} = (-I * R_F) + V_{REF} \quad (2)$$

R_L is a load resistor of which the value is normally specified by the sensor manufacturer (typically 10 ohms). The potential at WE is set by the applied $V_{REF.}$ Riso provides capacitive isolation and, combined with C2, form the output filter and ADC reservoir capacitor to drive the ADC.

Typical Application: Three Terminal CO Gas Sensor Amplifier (continued)

8.2.2 Detailed Design Procedure

For this example, we will be using a CO sensor with a sensitivity of 69nA/ppm. The supply votlage and maximum ADC input voltage is 2.5V, and the maximum concentration is 300ppm.

First the V_{REF} voltage must be determined. This voltage is a compromise between maximum headroom and resolution, as well as allowance for "footroom" for the minimum swing on the CE terminal, since the CE terminal generally goes negative in relation to the RE potential as the concentration (sensor current) increases. Bench measurements found the difference between CE and RE to be 180mV at 300ppm for this particular sensor.

To allow for negative CE swing "footroom" and voltage drop across the 10k resistor, 300mV was chosen for V_{REF}.

Therefore +300mV will be used as the minimum V_{ZERO} to add some headroom.

$V_{ZERO} = V_{REF} = +300mV$

where

- V_{ZERO} is the zero concentration voltage
- V_{REF} is the reference voltage (300mV) (3)

Next we calculate the maximum sensor current at highest expected concentration:

$I_{SENSMAX} = I_{PERPPM}$ * ppmMAX = 69nA * 300ppm = 20.7uA

where

- $I_{SENSMAX}$ is the maximum expected sensor current
- I_{PERPPM} is the manufacturer specified sensor current in Amps per ppm
- ppmMAX is the maximum required ppm reading (4)

Now find the available output swing range above the reference voltage available for the measurement:

$V_{SWING} = V_{OUTMAX} – V_{ZERO}$ = 2.5V – 0.3V = 2.2V

where

- V_{SWING} is the expected change in output voltage
- V_{OUTMAX} is the maximum amplifer output swing (usually near V+) (5)

Now we calculate the transimpedance resistor (R_F) value using the maximum swing and the maximum sensor current:

$R_F = V_{SWING} / I_{SENSMAX}$ = 2.2V / 20.7µA = 106.28 kΩ (we will use 110 kΩ for a common value) (6)

Typical Application: Three Terminal CO Gas Sensor Amplifier (continued)

8.2.3 Application Curve

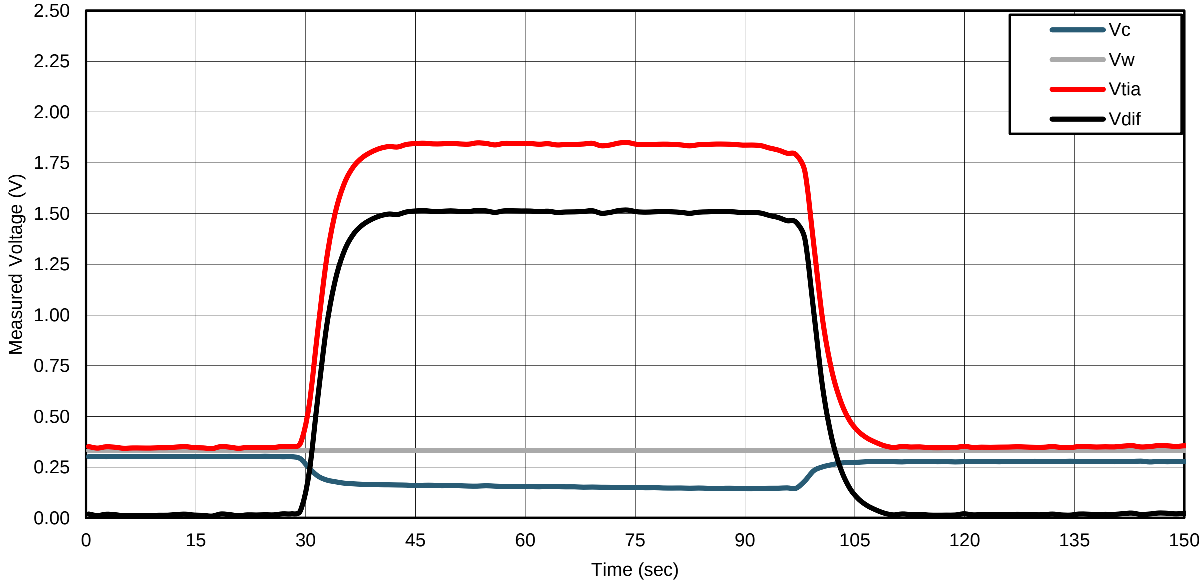


Figure 39. Monitored Voltages when exposed to 200ppm CO

Figure 39 shows the resulting circuit voltages when the sensor was exposed to 200ppm step of carbon monoxide gas. V_C is the monitored CE pin voltage and clearly shows the expected CE voltage dropping below the WE voltage, V_W, as the concentration increases.

V_{TIA} is the output of the transimpedance amplifer U2. V_{DIFF} is the calculated difference between V_{REF} and V_{TIA}, which will be used for the ppm calculation.

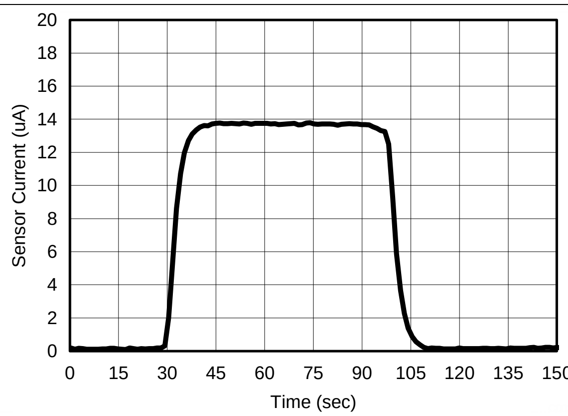


Figure 40. Calculated Sensor Current

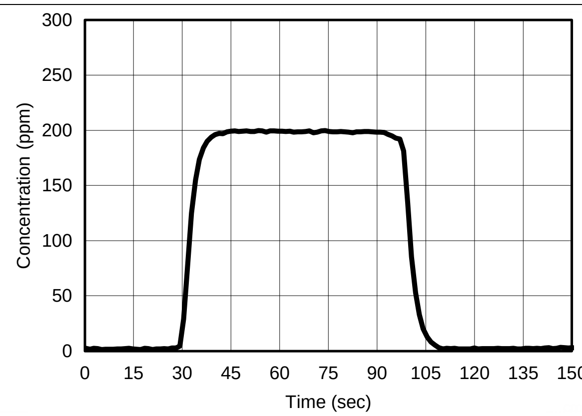


Figure 41. Calculated ppm

Figure 40 shows the calculated sensor current using the formula in Equation 7 :

$$I_{SENSOR} = V_{DIFF} / R_F = 1.52V / 110\ k\Omega = 13.8uA \quad (7)$$

Equation 8 shows the resulting conversion of the sensor current into ppm.

$$ppm = I_{SENSOR} / I_{PERPPM} = 13.8\mu A / 69nA = 200 \quad (8)$$

Total supply current for the amplifier section is less than 700 nA, minus sensor current. Note that the sensor current is sourced from the amplifier output, which in turn comes from the amplifier supply voltage. Therefore, any continuous sensor current must also be included in supply current budget calculations.

8.3 Do's and Don'ts

Do properly bypass the power supplies.

Do add series resistance to the output when driving capacitive loads, particularly cables, Muxes and ADC inputs.

Do add series current limiting resistors and external schottky clamp diodes if input voltage is expected to exceed the supplies. Limit the current to 1mA or less (1KΩ per volt).

9 Power Supply Recommendations

The TLV880x is specified for operation from 1.7 V to 5.5 V (±0.75 V to ±2.75 V) over a –40°C to 125°C temperature range. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

CAUTION

Supply voltages larger than 6 V can permanently damage the device.

For proper operation, the power supplies must be properly decoupled. For decoupling the supply lines it is suggested that 100 nF capacitors be placed as close as possible to the operational amplifier power supply pins. For single supply, place a capacitor between V^+ and V^- supply leads. For dual supplies, place one capacitor between V^+ and ground, and one capacitor between V^- and ground.

Low bandwidth nanopower devices do not have good high frequency (> 1 kHz) AC PSRR rejection against high-frequency switching supplies and other 1 kHz and above noise sources, so extra supply filtering is recommended if kilohertz or above noise is expected on the power supply lines.

10 Layout

10.1 Layout Guidelines

The V+ pin should be bypassed to ground with a low ESR capacitor.

The optimum placement is closest to the V+ and ground pins.

Care should be taken to minimize the loop area formed by the bypass capacitor connection between V+ and ground.

The ground pin should be connected to the PCB ground plane at the pin of the device.

The feedback components should be placed as close to the device as possible to minimize strays.

10.2 Layout Example

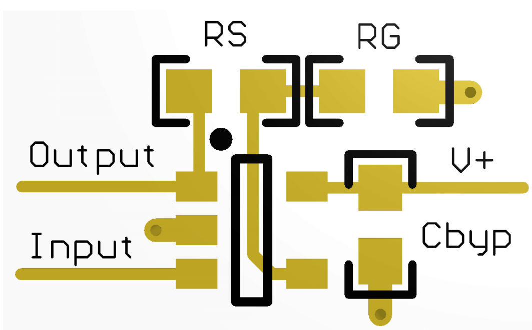


Figure 42. SOT-23 Layout Example (Top View)

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 開発サポート

TINA-TI SPICEベース・アナログ・シミュレータ・プログラム、http://www.ti.com/tool/tina-ti

DIPアダプタ評価モジュール、http://www.ti.com/tool/dip-adapter-evm

TIユニバーサル・オペアンプ評価モジュール、http://www.ti.com/tool/opampevm

TI FilterProフィルタ設計ソフトウェア、http://www.ti.com/tool/filterpro

11.2 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 1. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
TLV8801	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TLV8802	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

11.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV8801DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	16DM
TLV8801DBVR.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	16DM
TLV8801DBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	16DM
TLV8801DBVT.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	16DM
TLV8802DGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(8802, TLV)
TLV8802DGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(8802, TLV)
TLV8802DGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(8802, TLV)
TLV8802DGKT.B	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(8802, TLV)

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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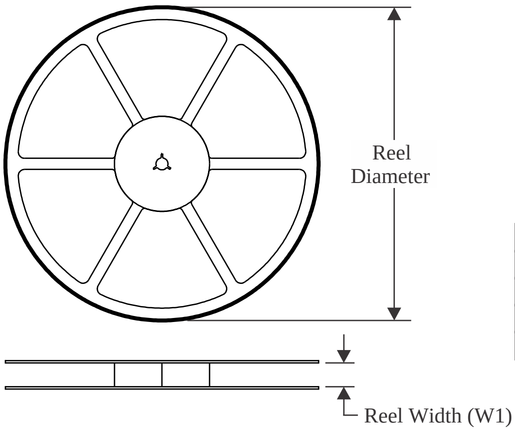
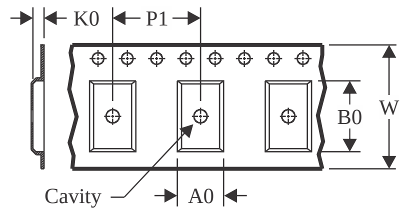
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

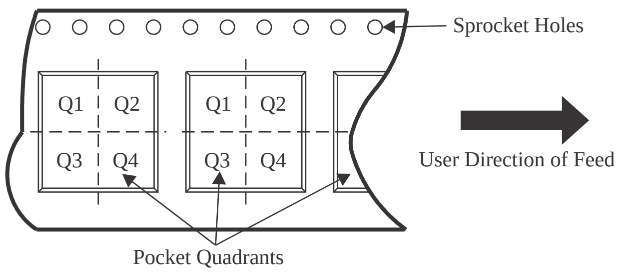


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

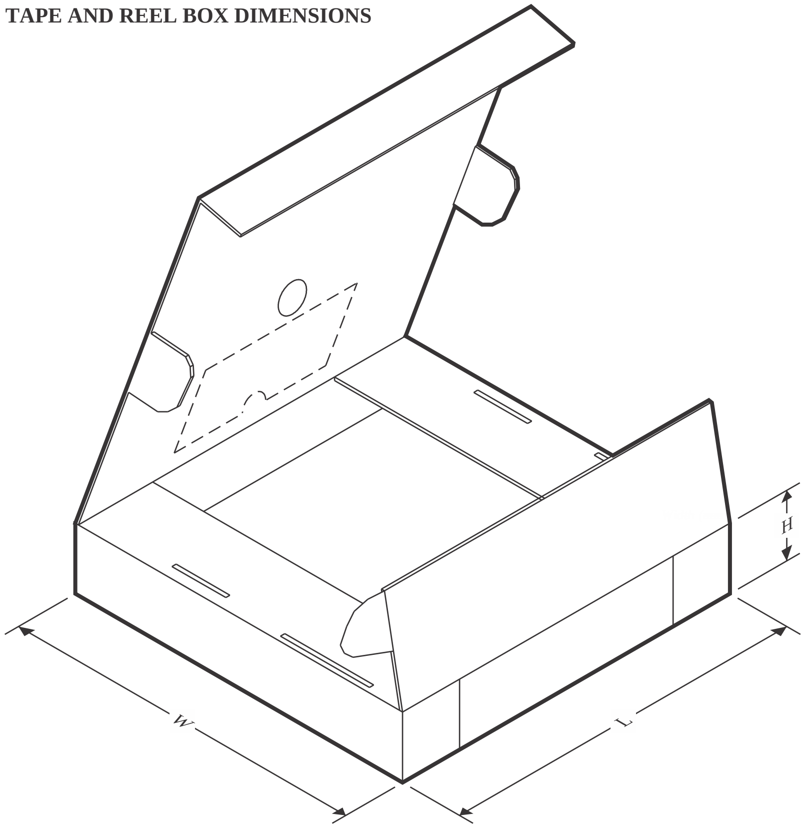
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

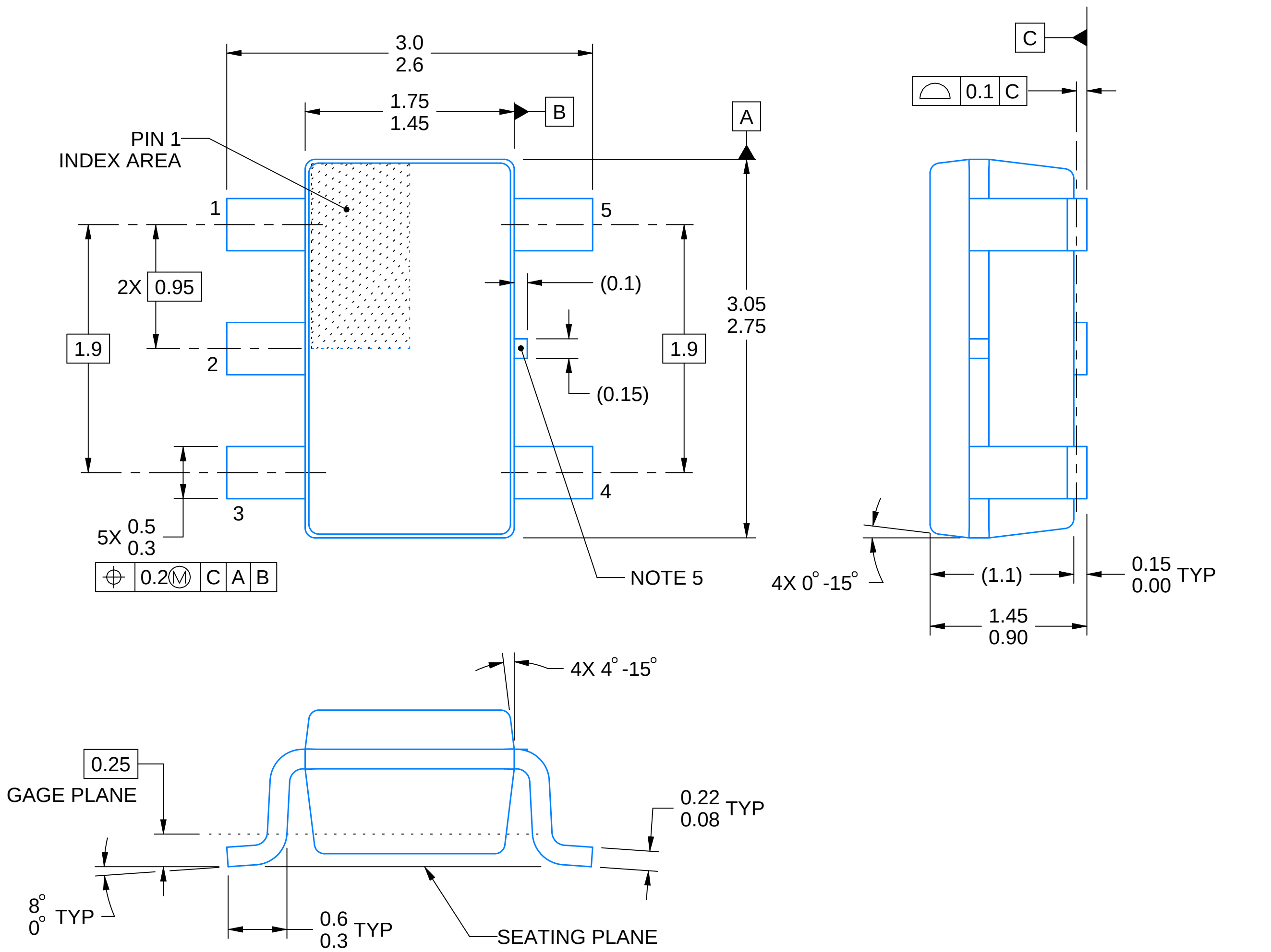
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV8801DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV8801DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV8801DBVT	SOT-23	DBV	5	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV8801DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV8802DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV8802DGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV8802DGKT	VSSOP	DGK	8	250	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV8801DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
TLV8801DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV8801DBVT	SOT-23	DBV	5	250	208.0	191.0	35.0
TLV8801DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TLV8802DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
TLV8802DGKT	VSSOP	DGK	8	250	353.0	353.0	32.0
TLV8802DGKT	VSSOP	DGK	8	250	366.0	364.0	50.0



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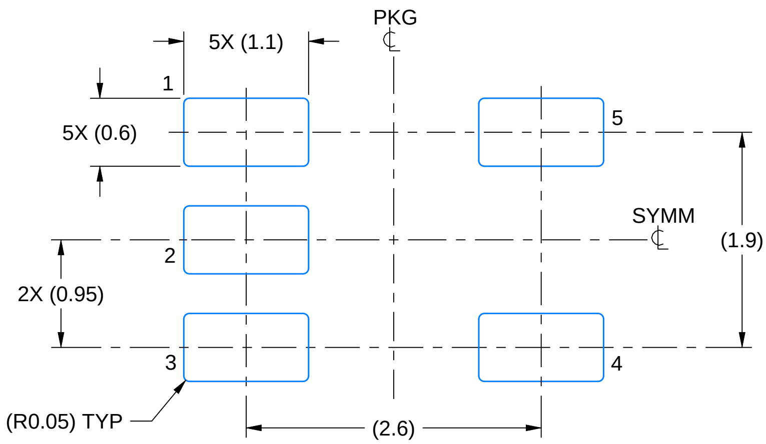
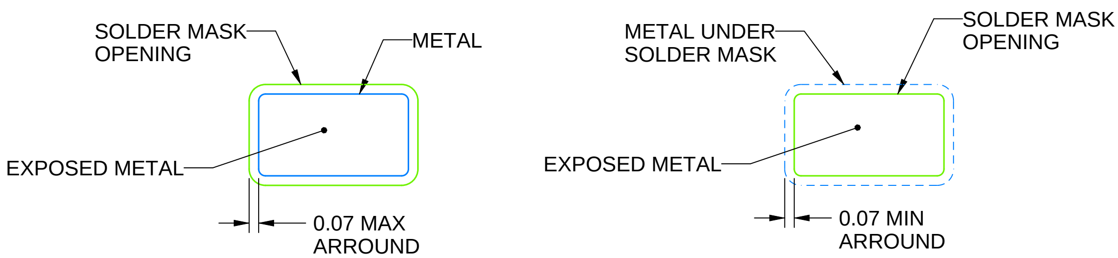
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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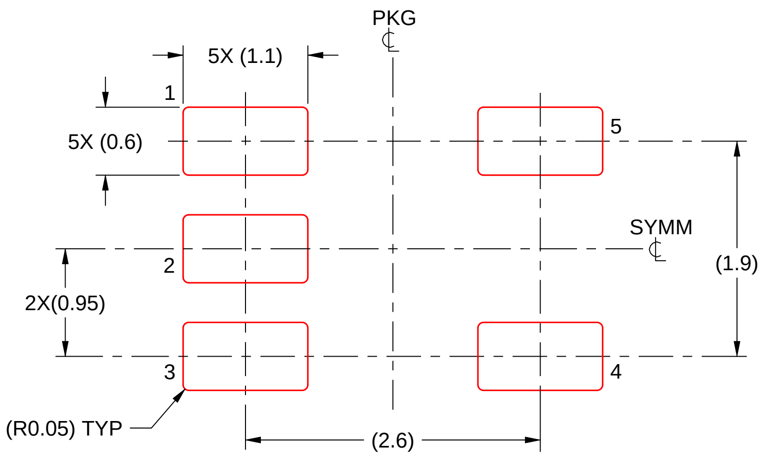
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

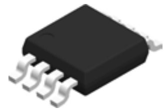


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

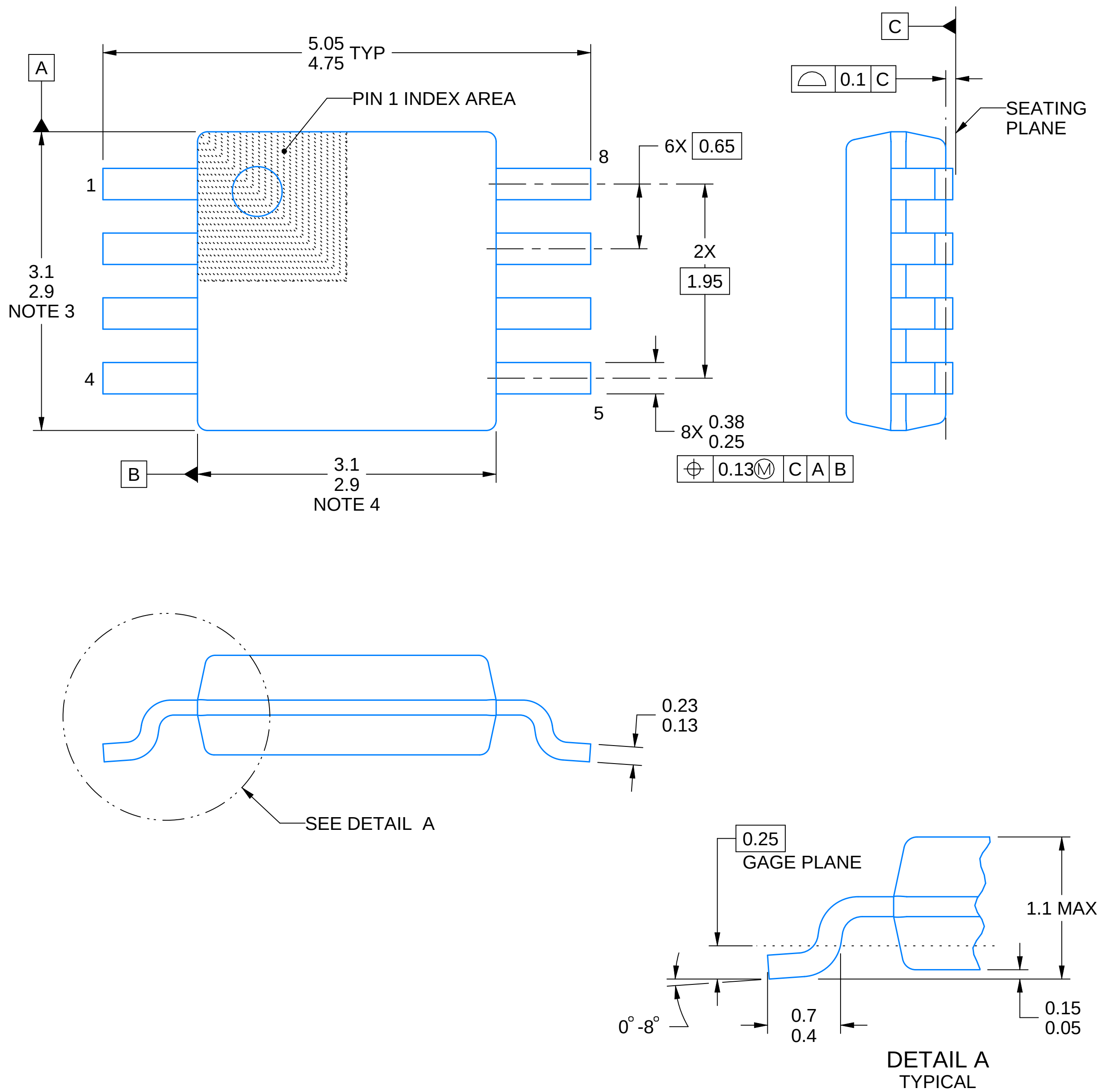


DGK0008A

PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

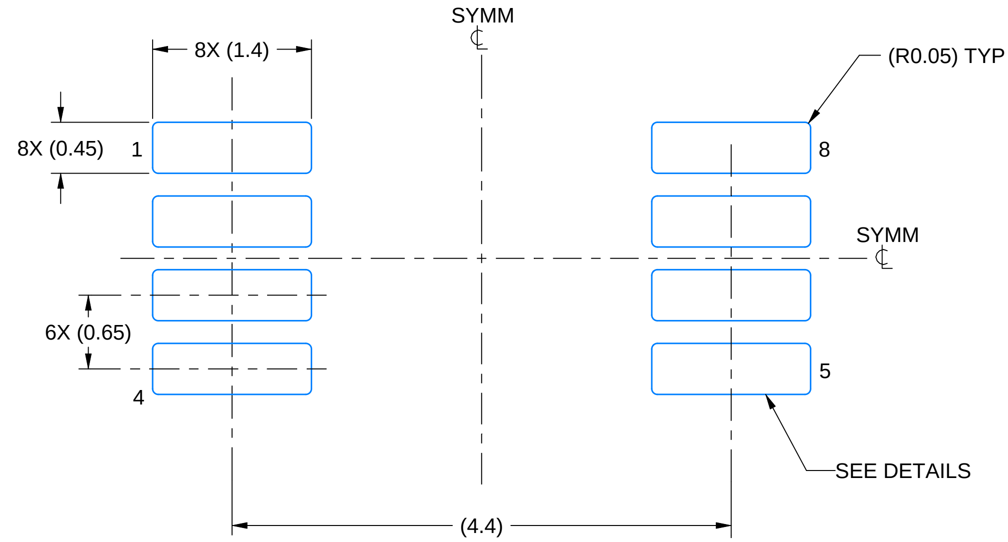


4214862/A 04/2023

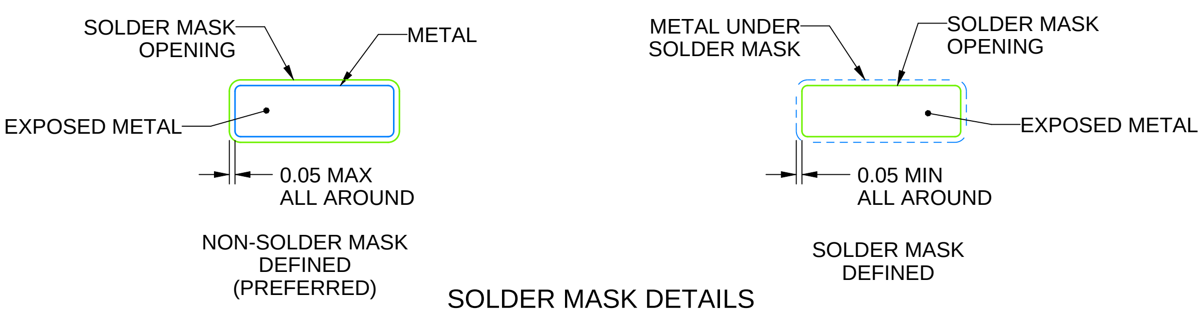
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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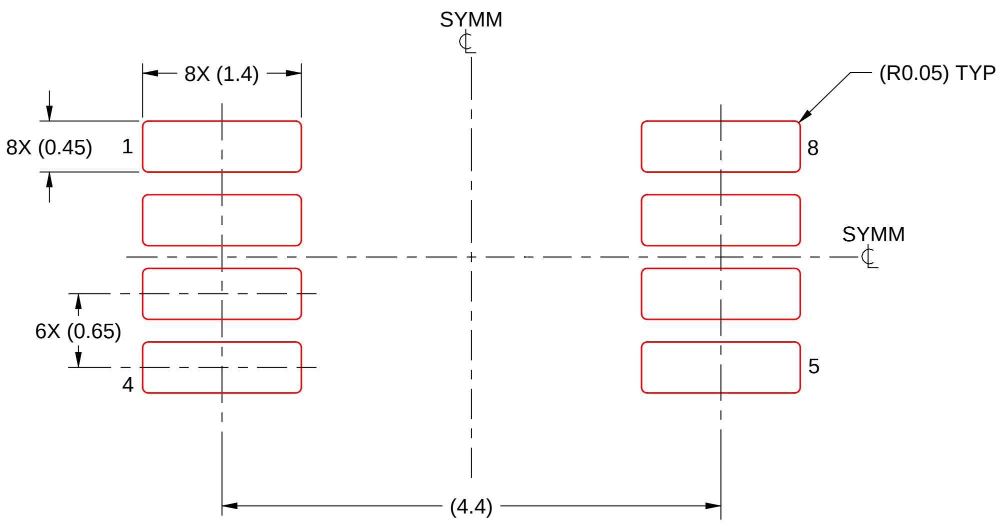
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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