TLV841 小型 nanoPower 電圧監視 IC、WCSP パッケージ

1 特長

高性能設計:

- わずかな静止電流:125nA (標準値)
- 高いスレッショルド精度:±0.5% (標準値)
- 高精度ヒステリシス (V_{HYS}) を内蔵:5% (標準値)

多様なアプリケーションに対応する設計:

- 動作電圧範囲:0.7V～5.5V
- 調整可能なスレッショルド電圧:0.505V (標準値)
- 固定 (V_{IT-}) 電圧:0.8V～4.9V (0.1V 刻み)
- 独立した SENSE ピン (TLV841S)
- アクティブ LOW のマニュアル・リセット ($\overline{MR}$) (TLV841M)
- TLV841 のプッシュ・ボタン監視 (S/M バリアント)
- リセット遅延時間をプログラム可能 (t_D):コンデンサ・ベースのプログラマブル (TLV841C)
  - 最小遅延時間:40µs (標準値)、コンデンサなしの場合
- リセット遅延時間をプログラム可能 (t_D):固定時間遅延オプション (TLV841M および TLV841S)
  - 40µs、2ms、10ms、30ms、50ms、80ms、100ms、150ms、200ms
- 温度範囲:–40℃～+125℃

複数の出力トポロジ、パッケージ・タイプ:

- TLV841xxDL:オープン・ドレイン、アクティブ LOW ($\overline{RESET}$)
- TLV841xxPL:プッシュプル、アクティブ LOW ($\overline{RESET}$)
- TLV841xxDH:オープン・ドレイン、アクティブ HIGH (RESET)
- TLV841xxPH:プッシュプル、アクティブ HIGH (RESET)
- パッケージ:0.73mm x 0.73mm DSBGA

2 アプリケーション

- ウェアラブルや補聴器などのパーソナル・エレクトロニクス
- ホーム・シアターおよびエンターテインメント
- POS システム
- グリッド・インフラストラクチャ
- データ・センターおよびエンタープライズ・コンピューティング

3 概要

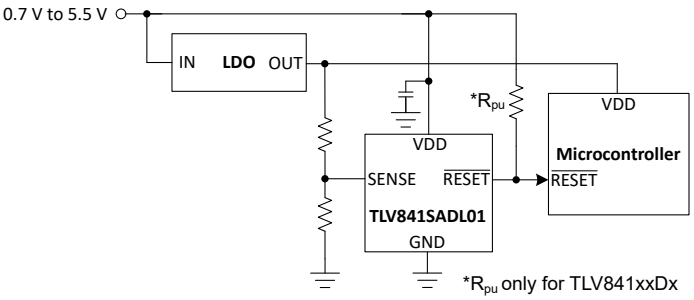
TLV841 は、超小型の DSBGA パッケージに ±0.5% のスレッショルド精度を備えたナノパワー高精度電圧監視 IC です。TLV841 には 3 つのピン配置バリエーション (S、M、C) があり、クラス最小のソリューション・サイズで多くの独自オプションを提供します。ヒステリシスに加えてプログラム可能な遅延が内蔵されているので、電圧レールやプッシュ・ボタン信号を監視するときに誤リセット信号が発生することを防止できます。TLV841S のアクティブ LOW 出力では、SENSE ピンと $\overline{RESET}$ ピンの間に外付け抵抗を追加することで、電圧スレッショルドのヒステリシスを増やすことができます。TLV841 は、高精度、低消費電力、クラス最高の機能を最小のコンパクトなフォーム・ファクタで実現しており、パーソナル製品やコンシューマ製品など、幅広いバッテリ駆動アプリケーションに最適なソリューションを提供します。

VDD ピンと SENSE ピンが別になっているので (TLV841S) 、高信頼性システムで求められる冗長性を実現できます。SENSE が VDD から分離されており、VDD 以外のレール電圧を監視することも、プッシュボタン入力として使用することもできます。SENSE ピンは高インピーダンス入力なので外付け抵抗を使うこともできます。TLV841S は、外付けコンデンサなしで固定リセット遅延タイミング・オプションを提供します。TLV841C を使用すると、CT ピンがフローティングのままになっているときの最小遅延を含め、リセット時間遅延をプログラム可能です。TLV841M には独立したマニュアル・リセット ($\overline{MR}$) ピンがあり、外部信号で強制的にリセット状態にすることも、プッシュ・ボタン入力として使用することも可能です。TLV841M は、VDD および $\overline{MR}$ ピン監視用に設定できるので、シンプルな 2 チャネル監視回路ソリューションを作成できます。TLV841 は、-40℃～+125℃ (T_A) の温度範囲で動作します。

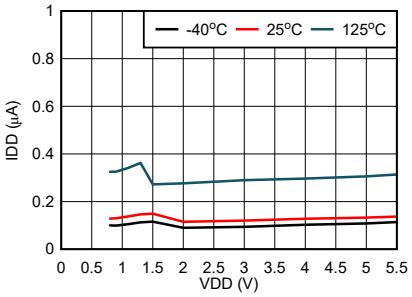
製品情報

部品番号	パッケージ (1)	本体サイズ (公称)
TLV841	DSBGA (4)	0.73mm×0.73mm

(1) パッケージの詳細については、このデータシートの末尾の外形図を参照してください。



代表的なアプリケーション回路



標準消費電流

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (June 2021) to Revision D (January 2023)	Page
• Removed Table 12-2	26

Changes from Revision B (May 2021) to Revision C (June 2021)	Page
• デバイスの RTM	1

5 Device Comparison

図 5-1 shows the device naming nomenclature to compare the different device variants. See 表 12-1 for a more detailed explanation. Please contact Texas Instruments for availability of variant options.

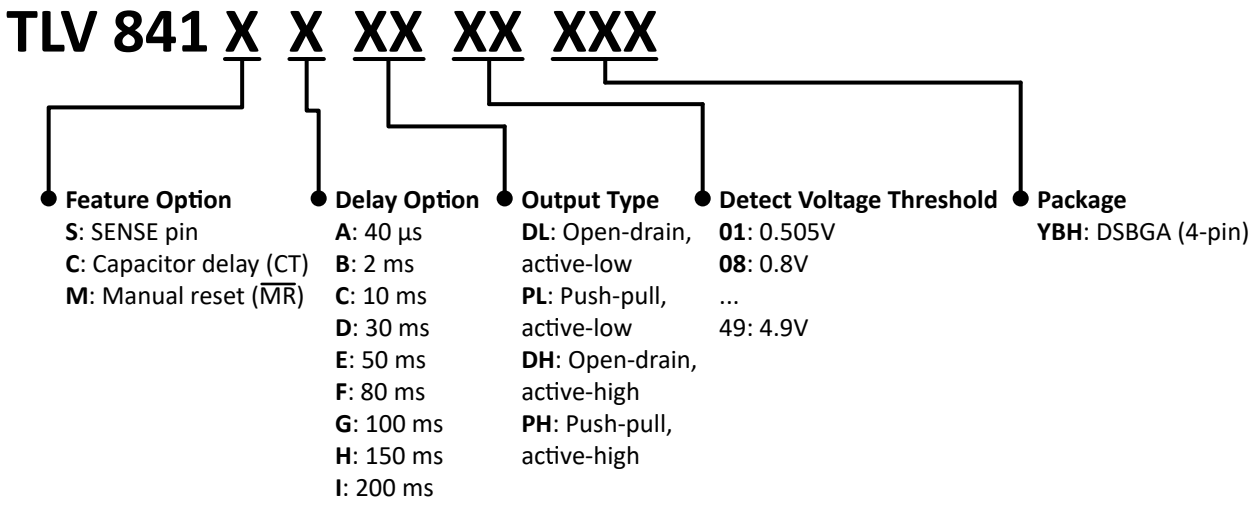


図 5-1. Device Naming Nomenclature

6 Pin Configuration and Functions

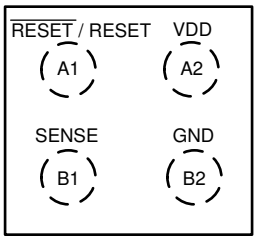


図 6-1. YBH 4-Pin DSBGA Package (TLV841S) Top View

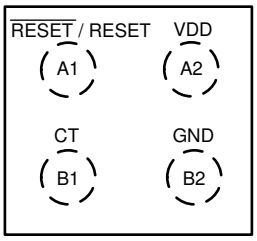


図 6-2. YBH 4-Pin DSBGA Package (TLV841C) Top View

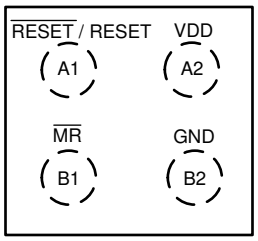


図 6-3. YBH 4-Pin DSBGA Package (TLV841M) Top View

表 6-1. Pin Functions

PIN				I/O	DESCRIPTION
PIN NO.	TLV841S	TLV841C	TLV841M		
A1	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	O	**Active-Low Output Reset Signal for TLV841xxxL**: This pin is driven logic low when VDD and SENSE voltage falls below the negative voltage threshold (V_{IT-}) or when the $\overline{\text{MR}}$ voltage falls below the logic low threshold. $\overline{\text{RESET}}$ remains logic low (asserted) until $\overline{\text{MR}}$ is above the logic high threshold or for the duration of the delay time period (t_D) after VDD or SENSE voltage rises above $V_{IT-} + V_{HYS}$
A1	RESET	RESET	RESET	O	**Active-High Output Reset Signal for TLV841xxxH**: This pin is driven logic high when VDD or SENSE voltage falls below the negative voltage threshold (V_{IT-}) or when the $\overline{\text{MR}}$ voltage falls below the logic low threshold. RESET remains logic high (asserted) until $\overline{\text{MR}}$ is above the logic high threshold or for the duration of the delay time period (t_D) after VDD or SENSE voltage rises above $V_{IT-} + V_{HYS}$
A2	VDD	VDD	VDD	I	**Input Supply Voltage**: The VDD pin connects to the power supply to power the device. TLV841C and TLV841M monitor VDD voltage. TLV841S monitors SENSE only. Good analog design practice recommends placing a minimum 0.1 µF ceramic capacitor as near as possible to the VDD pin.
B1	SENSE	_	_	I	**SENSE pin**: This pin is connected to the voltage to be monitored. When the voltage on SENSE falls below the negative threshold voltage V_{IT-}, reset asserts. When the voltage on SENSE rises above the positive threshold voltage ($V_{IT-} + V_{HYS}$), reset deasserts. For noisy applications, placing a 10 nF to 100 nF ceramic capacitor close to this pin may be needed for optimum performance.
B1	_	CT	_	I	**Capacitor Time Delay Pin**: The CT pin offers a user-programmable reset deassert delay time. Connect an external capacitor on this pin to adjust time delay. When not in use leave pin floating for the smallest fixed time delay.
B1	_	_	$\overline{\text{MR}}$	I	**Manual Reset**: Pull this pin to a logic low to assert a reset signal in the $\overline{\text{RESET}}$ output pin ($\overline{\text{RESET}}$ signal for DL and PL option). After $\overline{\text{MR}}$ pin is left floating or pulls to logic high, the $\overline{\text{RESET}}$ output deasserts to the nominal state after the reset delay time (t_D)expires. **If unused, the pin can be left floating or connected to VDD.**
B2	GND	GND	GND	_	**Ground**

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range, unless otherwise noted(1)

		MIN	MAX	UNIT
Voltage	VDD, SENSE (TLV841S)	–0.3	6	V
Voltage	CT (TLV841C), $\overline{MR}$ (TLV841M), $\overline{RESET}$ (TLV841xxPx), RESET (TLV841xxPx)	–0.3	V_{DD}+0.3 (3)	V
	$\overline{RESET}$ (TLV841xxDx), RESET (TLV841xxDx)	–0.3	6	
Current	$\overline{RESET}$, RESET		±20	mA
Temperature(2)	Operating ambient temperature, T_A	–40	125	°C
Temperature	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) As a result of the low dissipated power in this device, it is assumed that $T_J = T_A$.
(3) The absolute maximum rating is (VDD + 0.3) V or 6 V, whichever is smaller

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	± 2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	± 750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Voltage	VDD (TLV841C, TLV841M)	0.7		5.5	V
	VDD (TLV841S)	0.85		5.5	
	VDD (TLV841xxPH)	1		5.5	
	SENSE	0		5.5	
	$\overline{MR}$ (1), CT	0		V_{DD}	
	$\overline{RESET}$(TLV841xxPL), RESET (TLV841xxPH)	0		V_{DD}	
	$\overline{RESET}$(TLV841xxDL), RESET (TLV841xxDH)	0		5.5	
Current	$\overline{RESET}$, RESET	–5		5	mA
T_A	Operating free air temperature	–40		125	°C
C_{CT}	CT pin capacitor range	0		10	µF

(1) If the logic signal driving $\overline{MR}$ is less than V_{DD}, then additional current flows into VDD and out of $\overline{MR}$. $\overline{MR}$ pin voltage should not be higher than V_{DD}.

7.4 Thermal Information

THERMAL METRIC(1)		TLV841 YBH (WCSP) 4 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	180.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	58.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	58.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

At $V_{DDMIN} \le V_{DD} \le 5.5$ V, CT = $\overline{MR}$ = Open, $\overline{RESET}$/RESET pull-up resistor $R_{pull-up}$ (3) = 100 kΩ to VDD, output reset load C_{LOAD} = 10 pF and over the operating free-air temperature range –40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
COMMON PARAMETERS								
$V_{ADJ-VIT-}$	Negative-going input threshold for TLV841Sxxx01 ADJ version					0.505		V
V_{IT-}	Negative-going input threshold range Fixed threshold version (1)				0.8		4.9	V
V_{IT-_ACC}	Negative-going input threshold accuracy		V_{IT-} = 0.505 V (TLV841Sxx01) or 0.8 V to 1.7 V (Fixed threshold)		-2.5	±0.5	2.5	%
			V_{IT-} = 1.8 V to 4.9 V (Fixed threshold)		-2	±0.5	2	
V_{HYS}	Hysteresis on V_{IT-} pin		V_{IT-} = 0.505 V and 0.8 V		3	5	8	%
			V_{IT-} = 0.9 V to 4.9 V		3	5	7	
V_{POR}	Power on reset voltage (2)		TLV841xxxLxx	$V_{OL(MAX)}$ = 300 mV $I_{\overline{RESET}(Sink)}$ = 15 µA			700	mV
			TLV841xxxHxx	$V_{OH(MIN)}$ = 0.8VDD $I_{RESET(Source)}$ = 15 µA			900	
V_{OL}	Low level output voltage			V_{DD} = 0.85 V $I_{\overline{RESET}(Sink)}$ = 15 µA $I_{RESET(Sink)}$ = 15 µA			300	mV
				V_{DD} = 3.3 V $I_{\overline{RESET}(Sink)}$ = 2 mA $I_{RESET(Sink)}$ = 2 mA			300	mV
				V_{DD} = 5.5 V $I_{\overline{RESET}(Sink)}$ = 2 mA $I_{RESET(Sink)}$ = 2 mA			300	mV
V_{OH}	High level output voltage			V_{DD} = 1 V $I_{\overline{RESET}(Source)}$ = 15 µA $I_{RESET(Source)}$ = 15 µA	0.8V_{DD}			V
				V_{DD} = 1.8 V $I_{\overline{RESET}(Source)}$ = 500 µA $I_{RESET(Source)}$ = 500 µA	0.8V_{DD}			V
				$V_{DD} \ge$ 3.3 V $I_{\overline{RESET}(Source)}$ = 2 mA $I_{RESET(Source)}$ = 2 mA	0.8V_{DD}			V
$I_{lkg(OD)}$	Open-Drain output leakage current		$V_{DD} = V_{PULLUP}$ = 5.5 V	T_A = –40°C to 85°C		10	100	nA
						10	350	
I_{DD}	Supply current into VDD pin	Supply current into VDD pin	V_{DD} = 5.5 V V_{IT-} = 1.9 V to 4.9 V			0.125	1	µA

7.5 Electrical Characteristics (continued)

At $V_{DDMIN} \le V_{DD} \le 5.5$ V, CT = $\overline{MR}$ = Open, $\overline{RESET}$/RESET pull-up resistor $R_{pull-up}$ (3) = 100 kΩ to VDD, output reset load C_{LOAD} = 10 pF and over the operating free-air temperature range –40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
TLV841S							
I_{SENSE}	Current into SENSE pin, fixed threshold variant	$V_{DD} = V_{SENSE}$ = 5.5 V V_{IT-} = 0.8 V to 4.9 V			0.025	0.1	µA
	Current into SENSE pin, ADJ variant	$V_{DD} = V_{SENSE}$ = 5.5 V V_{IT-} = 0.505 V			0.025	0.05	
TLV841M							
$V_{\overline{MR}\_L}$	Manual reset logic low input					$0.3V_{DD}$	V
$V_{\overline{MR}\_H}$	Manual reset logic high input			$0.7V_{DD}$			V
$R_{\overline{MR}}$	Manual reset internal pull-up resistance				100		kΩ
TLV841C							
R_{CT}	CT pin internal resistance			410	500	590	kΩ

(1) V_{IT-} threshold voltage range from 0.8 V to 4.9 V (for DL, PL, DH) and 1 V to 4.9 V (for PH) in 100 mV steps, for released versions see Device Voltage Thresholds table.
(2) V_{POR} is the minimum V_{DD} voltage level for a controlled output state.
(3) Pull up resistance applicable for open drain variants

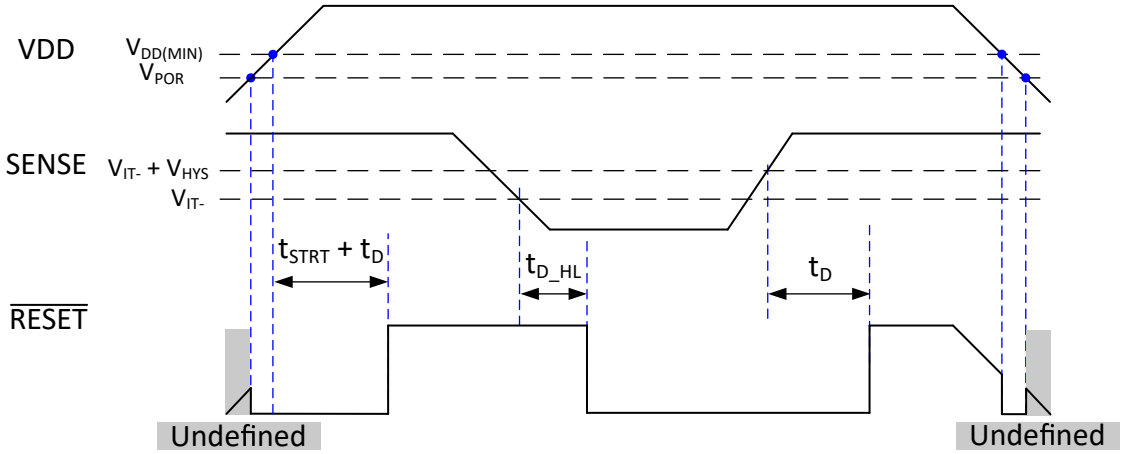
7.6 Timing Requirements

At $V_{DDMIN} \le V_{DD} \le 5.5$ V, CT = $\overline{MR}$ = Open, $\overline{RESET}$ pull-up resistor $R_{pull-up}$ = 100 kΩ to VDD, output load is C_{LOAD} = 10 pF and over the operating free-air temperature range –40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{P_HL}	Propagation detect delay for V_{DD} falling below V_{IT-}	V_{DD} = (V_{IT+} + 10%) to (V_{IT-} – 10%) (2)		30	50	µs
t_D	Reset time delay (TLV841C variant)	CT pin = Open or NC		40	80	µs
		CT pin = 10 nF		6.2		ms
		CT pin = 1 µF		619		ms
t_D	Reset time delay (TLV841S and TLV841M variant) (5)	Variant A (3)		40	80	µs
		Variant B (3)		2		ms
		Variant C (3)		10		ms
		Variant D (3)		30		ms
		Variant E (3)		50		ms
		Variant F (3)		80		ms
		Variant G (3)		100		ms
		Variant H (3)		150		ms
		Variant I (3)		200		ms
t_{GI_VIT-}	Glitch immunity V_{IT-}	5% V_{IT-} overdrive (4)		10		µs
t_{STRT}	Startup Delay (1)				300	µs
$t_{\overline{MR}\_RES}$	Propagation delay from $\overline{MR}$ low to reset	V_{DD} = 3.3 V, $\overline{MR}$ < $V_{\overline{MR}\_L}$		t_{P_HL}		µs
$t_{\overline{MR}\_tD}$	Delay from release $\overline{MR}$ to deassert reset	V_{DD} = 3.3 V, $\overline{MR}$ = $V_{\overline{MR}\_L}$ to $V_{\overline{MR}\_H}$		t_D		ms
$t_{\overline{MR}\_PW}$	Glitch immunity $\overline{MR}$ pin			10		µs

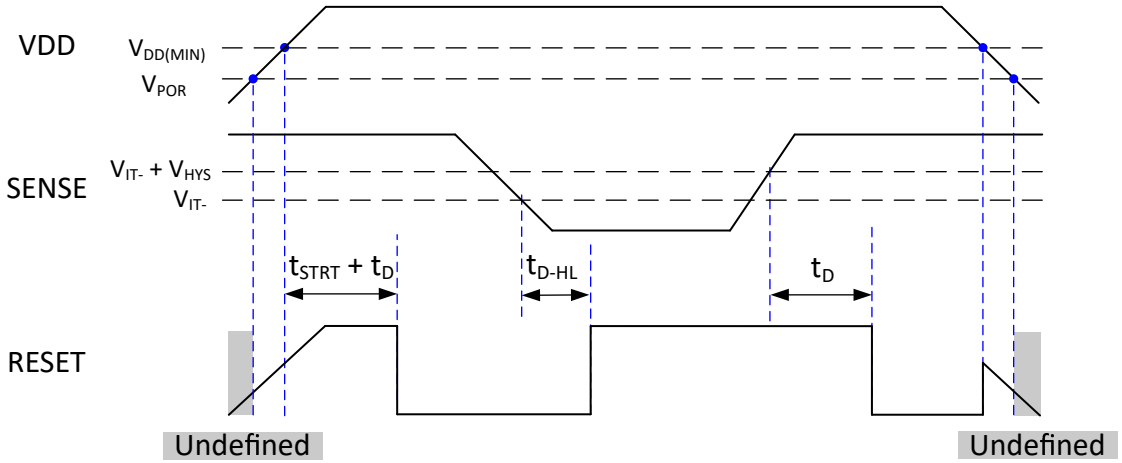
(1) When VDD starts from less than the specified minimum V_{DD} and then exceeds V_{POR}, reset is release after the startup delay (t_{STRT}). For TLV841C variants a capacitor at CT pin will add t_D delay to t_{STRT} time
(2) t_{P_HL} measured from threhold trip point (V_{IT-}) to V_{OL} for active low variants and V_{OH} for active high variants.
(3) Refer device nomenclature table for variant description. V_{DD} transition from V_{IT-} – 10% to V_{IT+} + 10% for TLV841M and TLV841C; V_{SENSE} transition from V_{IT-} – 10% to V_{IT+} + 10% for TLV841S
(4) Overdrive % = [(V_{DD}/ V_{IT-}) – 1] × 100% for TLV841M and TLV841C; Overdrive % = [(V_{SENSE}/ V_{IT-}) – 1] × 100% for TLV841S
(5) Specified by design and characterization

7.7 Timing Diagrams



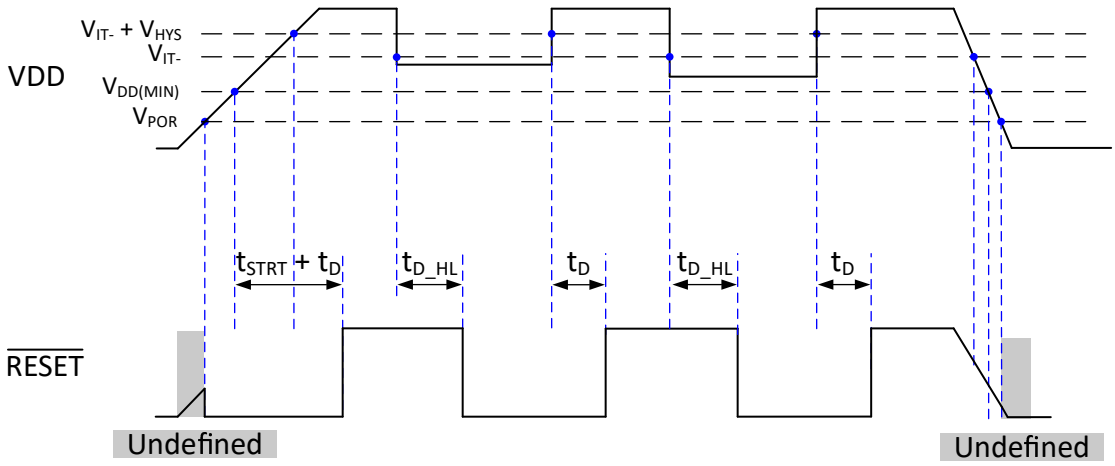
A. Open-Drain timing diagram assumes the $\overline{\text{RESET}}$ pin is connected via an external pull-up resistor to VDD.

図 7-1. Timing Diagram for TLV841SxxL (SENSE) Active Low Output [Open-Drain and Push-Pull Output Topology]



A. Open-Drain timing diagram assumes the RESET pin is connected via an external pull-up resistor to VDD.

図 7-2. Timing Diagram for TLV841SxxH (SENSE) Active High Output [Open-Drain and Push-Pull Output Topology]

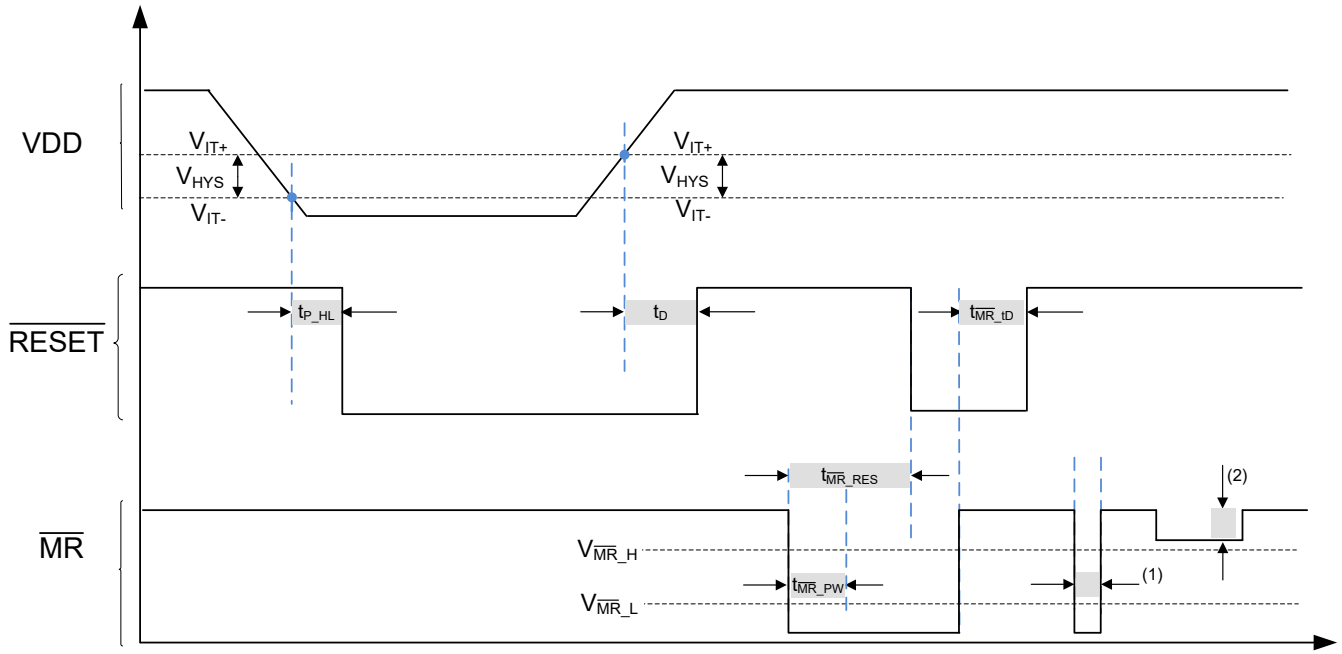


A. Open-Drain timing diagram assumes the $\overline{\text{RESET}}$ / RESET pin is connected via an external pull-up resistor to VDD.

B. $t_{D\ (no\ cap)}$ is included in t_{STRT} time delay. If t_D delay is programmed by an external capacitor connected to CT pin then t_D programmed time will be added to the startup time, VDD slew rate = 1 V / µs.

C. Be advised that the VDD falling slew rate is (slew rate > 1 V / µs) and resulting $\overline{\text{RESET}}$in what is shown above figure. The $\overline{\text{RESET}}$ behavior would be similar to 図 7-1 if the slew rate was much slower or if VDD decay time is larger than the prop delay (t_{D_HL}).

図 7-3. Timing Diagram for TLV841CxxL (CT) Active Low Output [Open-Drain and Push-Pull Output Topology]



A. Open-Drain timing diagram assumes the $\overline{\text{RESET}}$ / RESET pin is connected via an external pull-up resistor to VDD.

図 7-4. Timing Diagram for TLV841MxxL Active Low Output ($\overline{\text{MR}}$) [Open-Drain and Push-Pull Output Topology]

7.8 Typical Characteristics

Typical characteristics show the typical performance of the TLV841 device. Test conditions are T_A = 25°C, V_{DD} = 3.3 V, $R_{pull-up}$ = 100 kΩ, C_{Load} = 50 pF, unless otherwise noted.

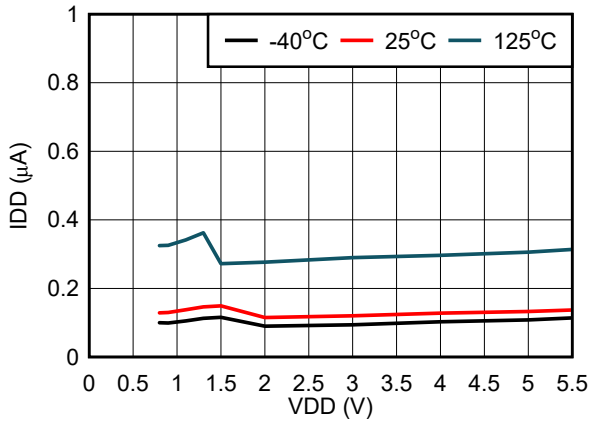


図 7-5. Supply Current vs Supply Voltage for TLV841S

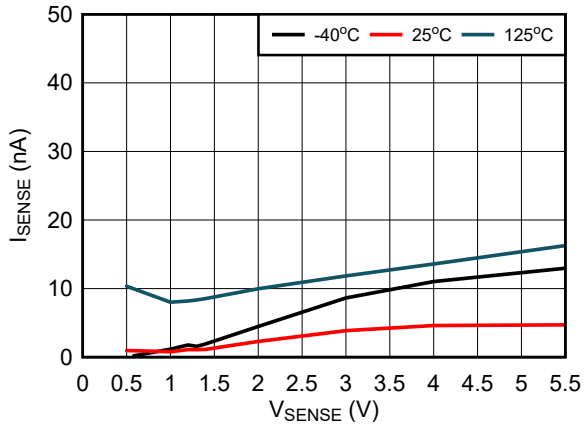


図 7-6. SENSE Current vs V_{SENSE}

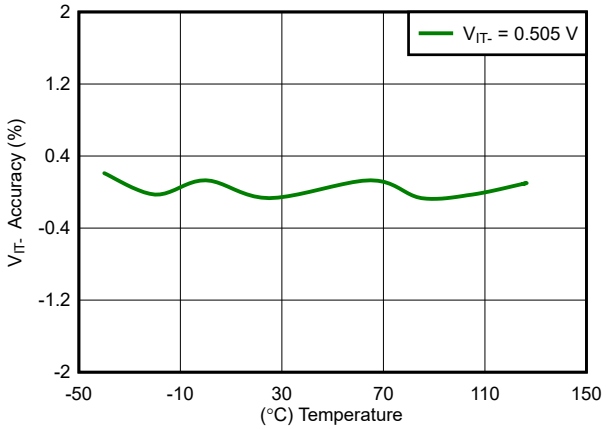


図 7-7. V_{IT-} Accuracy vs Temperature

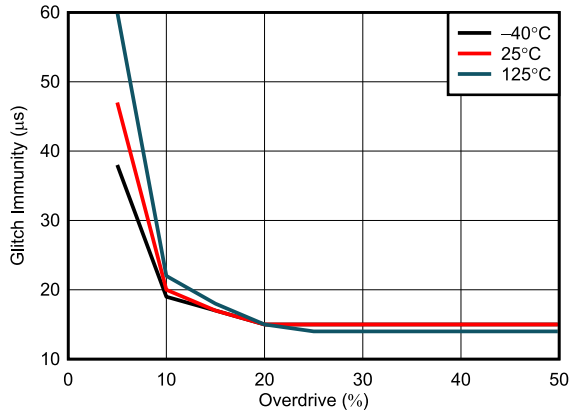


図 7-8. SENSE Glitch Immunity (V_{IT-}) vs Overdrive

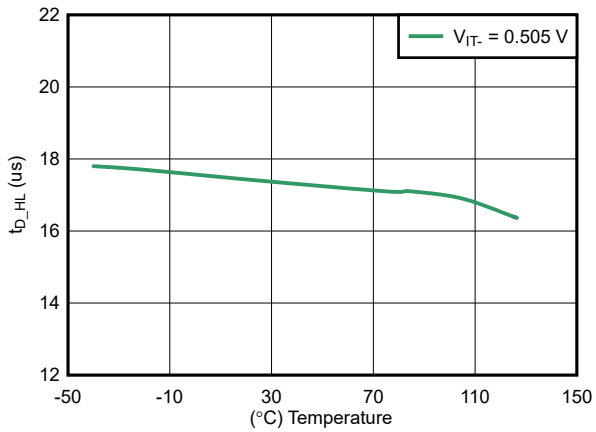


図 7-9. SENSE Delay (t_{D_HL}) vs Temperature

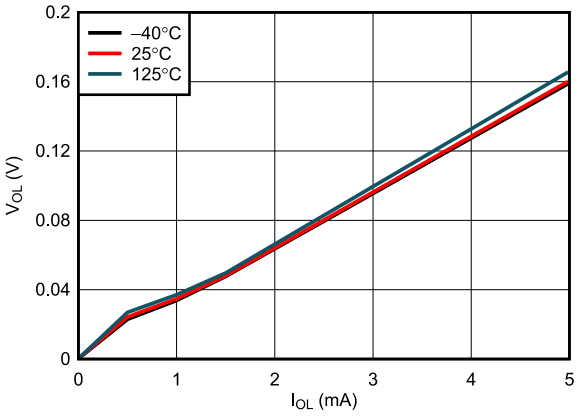


図 7-10. V_{OL} vs I_{OL}

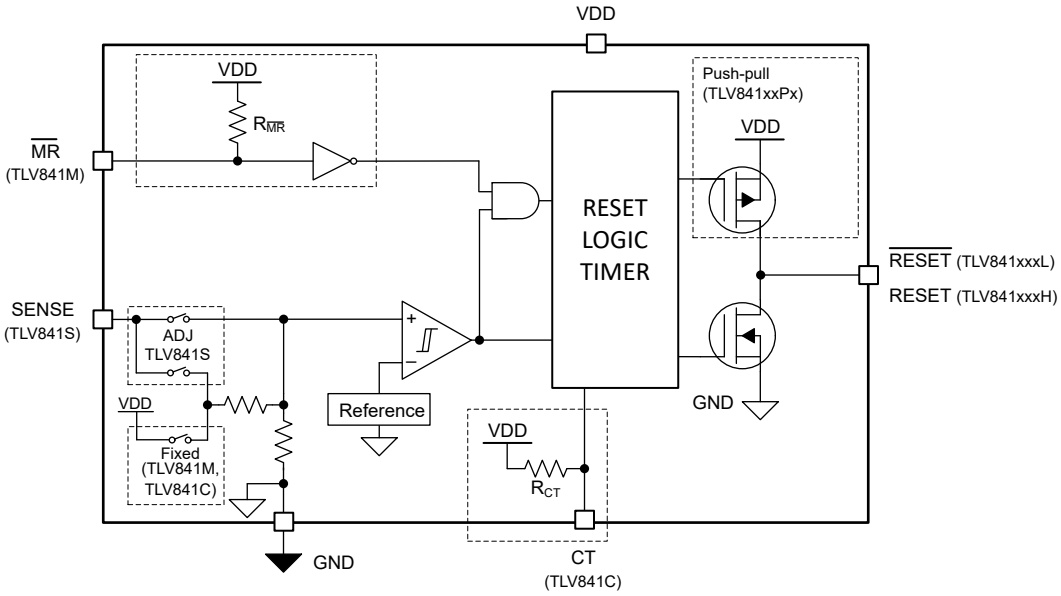
8 Detailed Description

8.1 Overview

The TLV841 is a family of very small, accurate, nano-quiescent current voltage supervisors with fixed threshold voltages. TLV841S features a separate SENSE pin for adjustable voltage threshold without losing accuracy, TLV841C features a programable reset time delay using external capacitor, and TLV841M features an active-low manual reset ($\overline{MR}$). The TLV841 family provide ±0.5% typical monitor threshold accuracy with hysteresis and glitch immunity.

The adjustable variant of TLV841S has an internal reference voltage of 0.505 V and can be used to accurately monitor any voltage above 0.505 V within the recommended operating conditions. In addition to the adjustable threshold variant, fixed negative threshold voltages (V_{IT-}) can be factory set from 0.8 V to 4.9 V in 100 mV steps. TLV841 is available in a very small (0.73 mm x 0.73 mm) 4-pin BGA package.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Input Voltage (VDD)

For TLV841C and TLV841M, the VDD pin is monitored by the internal comparator to indicate when VDD falls below the fixed threshold voltage. For TLV841S, the SENSE pin is monitored by the internal comparator. VDD also functions as the supply for the internal bandgap, internal regulator, state machine, buffers and other control logic blocks. Good design practice involve placing a 0.1 µF to 1 µF bypass capacitor at VDD input for noisy applications to ensure enough charge is available for the device to power up correctly.

8.3.1.1 VDD Hysteresis

The internal comparator has built-in hysteresis to avoid erroneous output reset release. If the voltage at the VDD (TLV841C, TLV841M) pin falls below V_{IT-} the output reset is asserted. When the monitored voltage goes above V_{IT-} plus hysteresis (V_{HYS}) the output reset is deasserted after t_D delay.

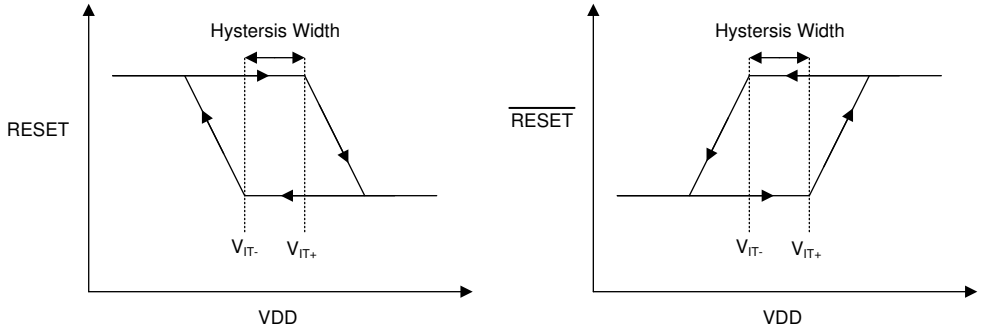


図 8-1. Hysteresis Diagram

8.3.1.2 VDD Transient Immunity

The TLV841 is immune to quick voltage transients or excursion on VDD. Sensitivity to transients depends on both pulse duration (t_{GI_VIT-}), specified in セクション 7.6, and overdrive. Overdrive is defined by how much VDD deviates from the specified threshold. Threshold overdrive is calculated as a percent of the threshold in question, as shown in 式 1.

$$\text{Overdrive} = | ((V_{DD} / V_{IT-}) - 1) \times 100\% | \quad (1)$$

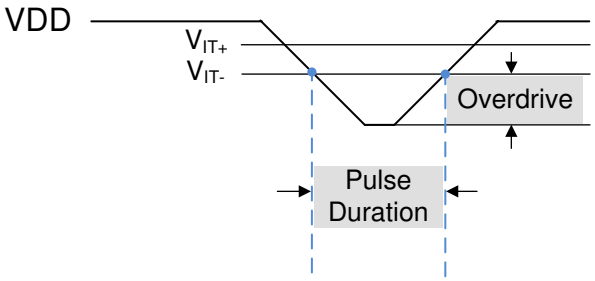


図 8-2. Overdrive vs Pulse Duration

8.3.2 SENSE Input (TLV841S)

The SENSE input can vary from 0 V to 5.5 V, regardless of the device supply voltage used. The SENSE pin is used to monitor a critical voltage rail or push-button input. If the voltage on this pin drops below V_{IT-}, then $\overline{\text{RESET}}$/RESET is asserted. When the voltage on the SENSE pin rises above the positive threshold voltage $V_{IT-} + V_{HYS}$, $\overline{\text{RESET}}$/RESET deasserts after the user-defined $\overline{\text{RESET}}$/RESET delay time. The internal comparator has built-in hysteresis to ensure well-defined $\overline{\text{RESET}}$/RESET assertions and deassertions even when there are small changes on the voltage rail being monitored.

The TLV841 device is relatively immune to short transients on the SENSE pin. Glitch immunity ($t_{GI\_V_{IT-}}$), specified in セクション 7.6, is dependent on threshold overdrive, as illustrated in 図 7-8. Although not required in most cases, for noisy applications, good analog design practice is to place a 10 nF to 100 nF bypass capacitor at the SENSE input to reduce sensitivity to transient voltages on the monitored signal.

8.3.2.1 SENSE Hysteresis

The internal comparator has built-in hysteresis to avoid erroneous output reset release. If the voltage at the SENSE (TLV841S) pin falls below V_{IT-} the output reset is asserted. When the monitored voltage goes above V_{IT-} plus hysteresis (V_{HYS}) the output reset is deasserted after t_D delay.

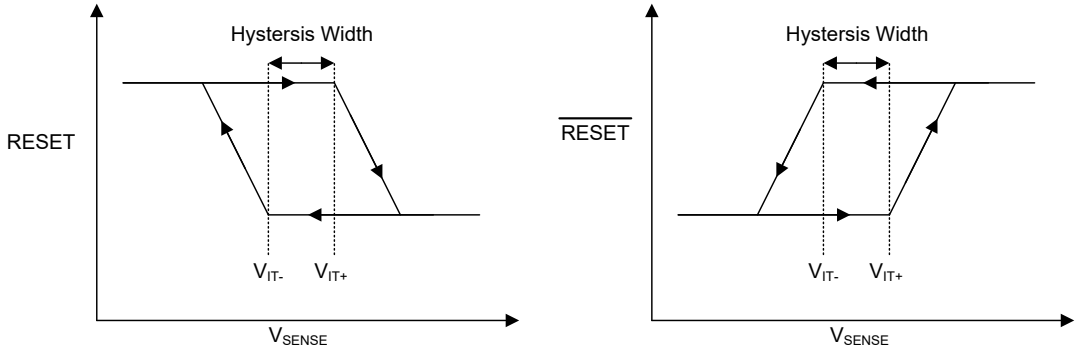


図 8-3. Hysteresis Diagram

8.3.2.2 Immunity to SENSE Pin Voltage Transients

The TLV841S is immune to short voltage transient spikes or excursion on the SENSE pin. To further improve the noise immunity on the SENSE pin, placing a 10 nF to 100 nF capacitor between the SENSE pin and GND can reduce the sensitivity to sensitivity to transient voltages on the monitored signal.

Sensitivity to transients depends on both transient duration and overdrive (amplitude) on the transient voltage. Overdrive is defined by how much V_{SENSE} exceeds the specified threshold and is important to know because the smaller the overdrive, the slower the resonse of the output. Threshold overdrive is calculated as a percent of the threshold in question, as shown in 式 2.

$$\text{Overdrive} = | ((V_{SENSE} / V_{IT-}) - 1) \times 100\% | \quad (2)$$

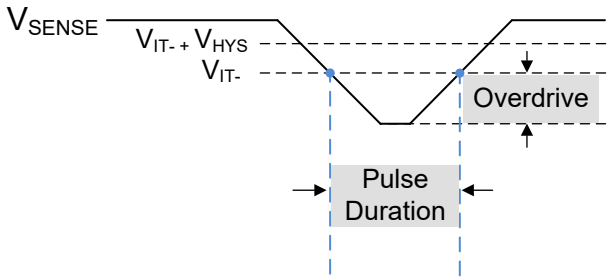


図 8-4. Overdrive vs Pulse Duration

8.3.3 User-Programmable Reset Time Delay for TLV841C only

The reset time delay can be set to a typical value of 40 µs by leaving the CT pin floating, or a maximum value of approximately 6.2 seconds by connecting 10 µF delay capacitor. The reset time delay (t_D) can be programmed by connecting a capacitor no larger than 10 µF between the CT pin and GND.

The relationship between external capacitor ($C_{CT\_EXT\ (typ)}$) in µF at CT pin and the time delay ($t_{D\ (typ)}$) in seconds is given by 式 3.

$$t_{D\ (typ)} = -\ln (0.29) \times R_{CT\ (typ)} \times C_{CT\_EXT\ (typ)} + t_{D\ (no\ cap,\ typ)} \quad (3)$$

式 3 is simplified to 式 4 by plugging $R_{CT\ (typ)}$ and $t_{D\ (no\ cap,\ typ)}$ given in *セクション 7.5* and *セクション 7.6*:

$$t_{D\ (typ)} = 618937 \times C_{CT\_EXT\ (typ)} + 40\ \mu s \quad (4)$$

式 5 solves for external capacitor value C_{CT_EXT} in units of µF where $t_{D\ (typ)}$ is in units of seconds

$$C_{CT\_EXT} = (t_{D\ (typ)} - 40\ \mu s) \div 618937 \quad (5)$$

The reset delay varies according to three variables: the external capacitor C_{CT_EXT}, CT pin internal resistance R_{CT} provided in セクション 7.5, and a constant. The maximum variance due to the constant is show in 式 6:

$$t_{D\ (max)} = -\ln (0.25) \times R_{CT\ (max)} \times C_{CT\_EXT\ (max)} + t_{D\ (no\ cap,\ max)} \quad (6)$$

The recommended maximum delay capacitor for the TLV841C is limited to 10 µF as this ensures enough time for the capacitor to fully discharge when a voltage fault occurs. Also, having a too large of a capacitor value can cause very slow charge up (rise times) and system noise can cause the the internal circuit to trip earlier or later near the threshold. This leads to variation in time delay where it can make the delay accuracy worse in the presence of system noise.

When a voltage fault occurs, the previously charged up capacitor discharges and if the monitored voltage returns from the fault condition before the delay capacitor discharges completely, the delay will be shorter than expected. The capacitor will begin charging from a voltage above zero and resulting in shorter than expected time delay. A larger delay capacitor can be used so long as the capacitor has enough time to fully discharge during the duration of the voltage fault. The amount of time required to discharge the delay capacitor relative to the reset delay rises as VDD fault undervoltage increases as shown in 図 8-5. From the graph below, to ensure the C_{CT_EXT} capacitor is fully discharged, the time period or duration of the voltage fault needs to be greater than 10% of the programmed reset time delay.

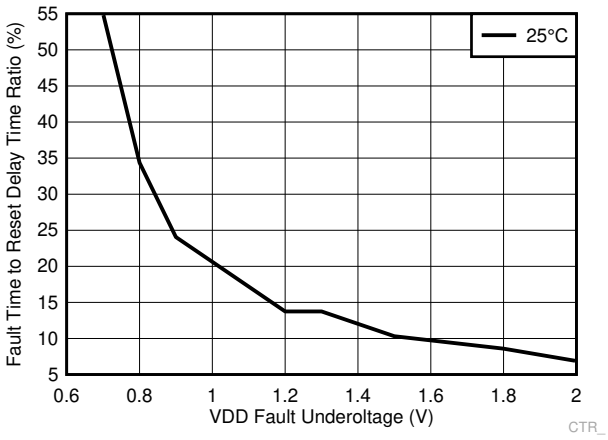


図 8-5. C_{CT_EXT} Discharge Time During Fault Condition (C_{CT_EXT} = 1 µF)

8.3.4 Manual Reset ($\overline{MR}$) Input for TLV841M only

The manual reset ($\overline{MR}$) input allows a processor GPIO or other logic circuits to initiate a reset. A logic low on $\overline{MR}$ with pulse duration longer than $t_{\overline{MR}\_RES}$ will causes reset output to assert. After $\overline{MR}$ returns to a logic high ($V_{\overline{MR}\_H}$) and VDD is above V_{IT+}, reset is deasserted after the user programmed reset time delay (t_D) expires.

If $\overline{MR}$ is not controlled externally, then $\overline{MR}$ can be left disconnected. If the logic signal controlling $\overline{MR}$ is less than VDD, then additional current flows from VDD into $\overline{MR}$ internally. For minimum current consumption, drive $\overline{MR}$ to either VDD or GND. $V_{\overline{MR}}$ should not be higher than VDD voltage.

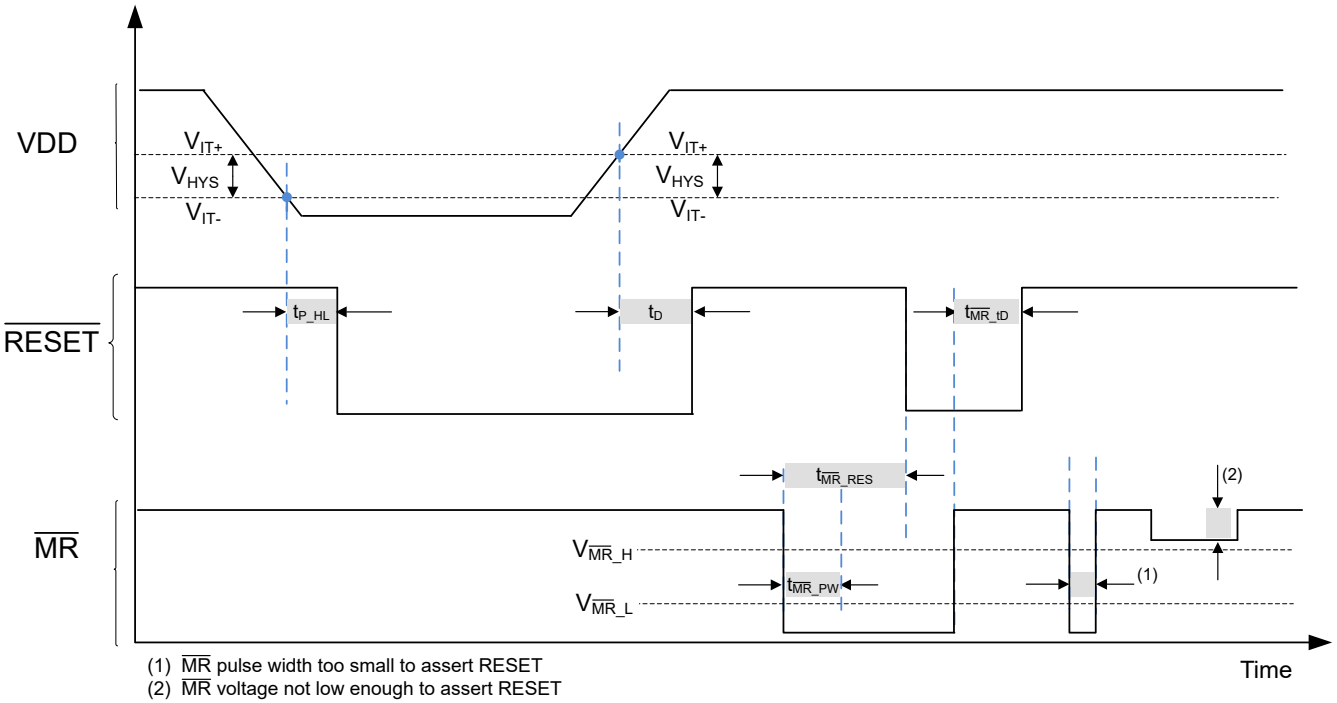


図 8-6. Timing Diagram $\overline{MR}$ and $\overline{RESET}$ (TLV841M)

8.3.5 Output Logic

8.3.5.1 $\overline{\text{RESET}}$ Output, Active-Low

$\overline{\text{RESET}}$ (Active-Low) applies to TLV841xxD**L** (Open-Drain) and TLV841xxP**L** (Push-Pull) hence the "**L**" in the device name. $\overline{\text{RESET}}$ remains high (deasserted) as long as VDD/SENSE is above the negative threshold (V_{IT-}) and the $\overline{\text{MR}}$ pin is floating or above $V_{\overline{MR}\_H}$. If VDD/SENSE falls below the negative threshold (V_{IT-}) or if $\overline{\text{MR}}$ is driven low, then $\overline{\text{RESET}}$ is asserted.

When $\overline{\text{MR}}$ is again logic high or floating and VDD/SENSE rise above V_{IT+} (V_{IT-} + V_{HYS}), the delay circuit will hold $\overline{\text{RESET}}$ low for the specified reset time delay (t_D). When the reset time delay has elapsed, the $\overline{\text{RESET}}$ pin goes back to logic high voltage V_{OH}.

The TLV841xx**D**L (Open-Drain) version, denoted with "**D**" in the device name, requires an external pull-up resistor to hold $\overline{\text{RESET}}$ pin high. Connect the external pull-up resistor to the desired pull-up voltage source and $\overline{\text{RESET}}$ can be pulled up to any voltage up to 5.5 V independent of the VDD voltage. To ensure proper voltage levels, give some consideration when choosing the external pull-up resistor values. The external pull-up resistor value determines the actual V_{OL}, the output capacitive loading, and the output leakage current ($I_{lkg(OD)}$).

The Push-Pull variant (TLV841xx**P**L), denoted with "**P**" in the device name, does not require an external pull-up resistor

8.3.5.2 RESET Output, Active-High

RESET (active-high), denoted with no bar above the pin label, applies only to TLV841xxD**H** (open-drain) and TLV841xxP**H** (push-pull) active-high version, hence the **"H"** in the device name. RESET remains low (deasserted) as long as VDD/SENSE is above the threshold (V_{IT-}) and the manual reset signal ($\overline{\text{MR}}$) is floating or above $V_{\overline{MR}\_H}$. If VDD/SENSE falls below the negative threshold (V_{IT-}) or if $\overline{\text{MR}}$ is driven low, then RESET is asserted driving the RESET pin to high voltage V_{OH}.

When $\overline{\text{MR}}$ is again logic high or floating and VDD/SENSE is above V_{IT+} (V_{IT-} + V_{HYS}) the delay circuit will hold RESET high for the specified reset time delay (t_D). When the reset time delay has elapsed, the RESET pin goes back to low voltage V_{OL}

The TLV841xx**D**H (Open-Drain) version, denoted with "**D**" in the device name, requires an external pull-up resistor to hold $\overline{\text{RESET}}$ pin high. Connect the external pull-up resistor to the desired pull-up voltage source and $\overline{\text{RESET}}$ can be pulled up to any voltage up to 5.5 V independent of the VDD voltage. To ensure proper voltage levels, give some consideration when choosing the external pull-up resistor values. The external pull-up resistor value determines the actual V_{OL}, the output capacitive loading, and the output leakage current ($I_{lkg(OD)}$).

The Push-Pull variant (TLV841xx**P**H), denoted with "**P**" in the device name, does not require an external pull-up resistor

8.4 Device Functional Modes

表 8-1 and 表 8-2 summarizes the various functional modes of the device. Logic high is represented by "H" and logic low is represented by "L".

表 8-1. Truth Table for TLV841S

VDD	SENSE	RESET (ACTIVE-HIGH)	$\overline{\text{RESET}}$ (ACTIVE-LOW)
VDD < V_{POR}	—	Undefined	Undefined
V_{POR} < V_{DD} < $V_{DD(MIN)}$ (1)	—	H	L
VDD ≥ $V_{DD(MIN)}$	V_{SENSE}< V_{IT-}	H	L
VDD ≥ $V_{DD(MIN)}$	V_{SENSE} > V_{IT-} + V_{HYS}	L	H

(1) When V_{DD} falls below $V_{DD(MIN)}$, undervoltage-lockout (UVLO) takes effect and $\overline{\text{RESET}}$ is held logic low (RESET is held logic high) until V_{DD} falls below V_{POR} at which the $\overline{\text{RESET}}$/RESET output is undefined.

表 8-2. Truth Table for TLV841M

VDD	$\overline{\text{MR}}$	RESET (ACTIVE-HIGH)	$\overline{\text{RESET}}$ (ACTIVE-LOW)
VDD < V_{POR}	—	Undefined	Undefined
V_{POR} < V_{DD} < V_{IT-}	—	H	L
VDD ≥ V_{IT-}	L	H	L
VDD ≥ V_{IT-}	H	L	H
VDD ≥ V_{IT-}	Floating	L	H

8.4.1 Normal Operation (V_{DD} > V_{POR})

When VDD is greater than V_{POR}, the reset signal is determined by the voltage on the VDD pin with respect to the trip point (V_{IT-})

- $\overline{\text{MR}}$ high: The reset signal corresponds to VDD with respect to the threshold voltage.
- $\overline{\text{MR}}$ low: In this mode, the reset is asserted regardless of the threshold voltage.

8.4.2 Below Power-On-Reset (V_{DD} < V_{POR})

When the voltage on VDD is lower than V_{POR}, the device does not have enough bias voltage to internally pull the asserted output low or high and reset voltage level is undefined.

9 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

The following sections describe in detail how to properly use this device, depending on the requirements of the final application.

9.2 Typical Application

Design 1: Adjustable Voltage Supervisor with Push-Button Functionality

A typical application for the TLV841S is voltage rail monitoring with push-button functionality. In this design application, the TLV841SADL01 is being used to monitor a 3.3 V power rail and will trigger a reset when the voltage drops below 2.90 V or when the push-button is pressed. The reset output connects to an MCU for system resetting or servicing the push-button.

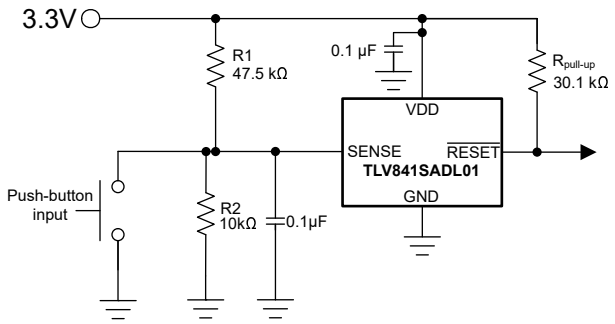


図 9-1. Design 1 - Adjustable Voltage Supervisor with Push-Button Functionality Circuit

9.2.1 Design Requirements

The design requirements, described in 表 9-1, for this design has a defined reset threshold voltage of 2.90 V, a reset delay of 40 µs and an output current no larger than 150 µA.

表 9-1. Design Requirements

PARAMETER	DESIGN REQUIREMENTS	DESIGN RESULTS
Reset Asserting	Reset needs to assert when under the reset condition of a button press or VDD ≤ 2.90 V.	Reset asserted when under the reset condition of a button pressed or VDD ≤ 2.90 V.
Reset Asserting Timing	Reset output needs to assert when the reset conditions are met for 20 µs, and needs to de-assert after 40 µs of no reset conditions.	Reset output asserted when the reset conditions were met for 26.4 µs and deasserted after 46.8 µs of no reset conditions.
Output Current	The output current must not exceed 150 µA.	The output current was 110 µA under the reset condition.

9.2.2 Detailed Design Procedure

The TLV841SADL01 can monitor any voltage above 0.505 V using an external voltage divider. This device has a negative going input threshold voltage of 0.505 V; however, the design needs to assert a reset when VDD drops below 2.90 V. By using a resistor divider (R1 = 47.5 kΩ, R2 = 10 kΩ) the negative going threshold voltage becomes 2.90 V. The device's positive going voltage threshold is V_{IT-} + V_{HYS}. The typical V_{HYS} is 25 mV. This in combination with the resistor divider makes the design's positive going threshold voltage equal to 3.05 V. If VDD falls below 2.90 V, $\overline{\text{RESET}}$ will assert. If VDD rises above 3.05 V, $\overline{\text{RESET}}$ will deassert. See 図 9-2 for a timing diagram detailing the voltage levels and reset assertion/deassertion conditions.

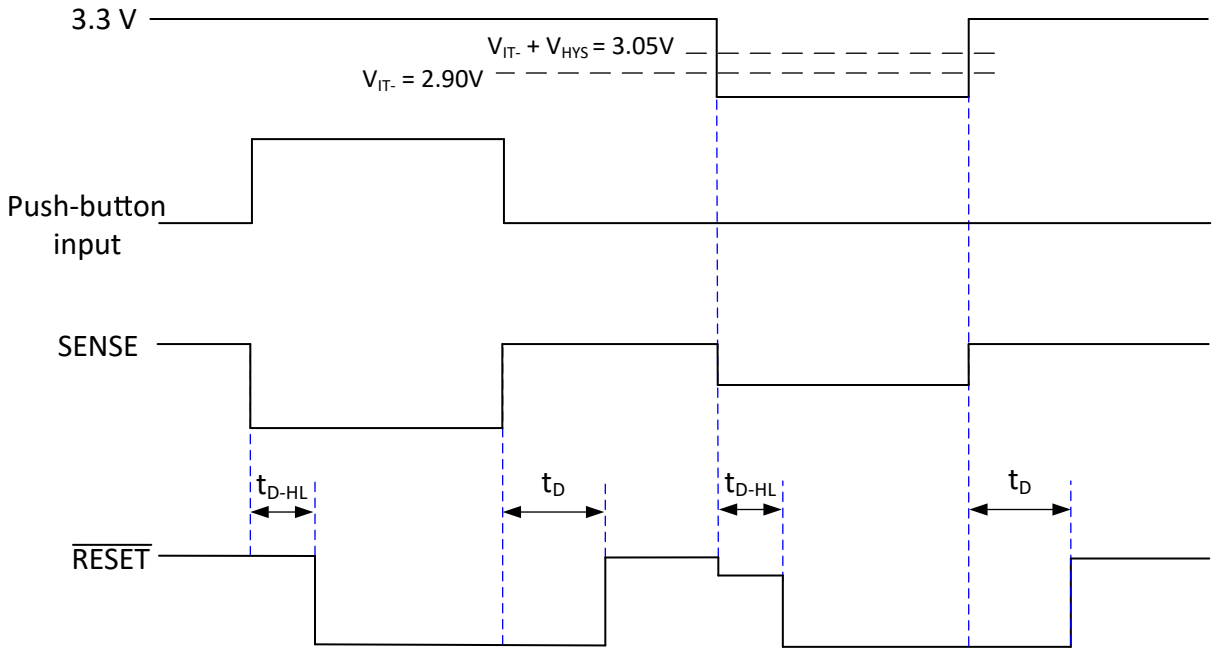


図 9-2. Design 1 Timing Diagram

This design will also enter a reset condition when the "push-button input" is asserted. The push-button is tied to ground and when pressed will drop the SENSE voltage to 0 V, making the device assert a reset. As a good analog practice, a 0.1 µF capacitor was also placed on VDD.

The desired reset timing conditions are sense propagation delay time (t_{P_HL} of 25 µs (how long it takes to assert $\overline{\text{RESET}}$) and a reset delay time of 40 µs (how long it takes to deassert $\overline{\text{RESET}}$). 図 9-3 and 図 9-4 are the results of the described application where the measured propagation delay and reset delay time are shown respectively.

For the requirement of a maximum output current, an external pull-up resistor needs to be selected so that the current through the external pull-up resistor exceeds no more than 150 µA. When the reset output is low, the voltage drop across the external pull-up resistor is equal to VDD. Ohm’s law is used to calculate the minimum resistor value. The resistor needs to be greater than 22 kΩ in order to pull less than 150 µA in the reset asserted low condition. A resistor value of 30.1 kΩ was selected to accomplish this.

Note that this design does not account for tolerances.

9.2.3 Application Curves: TLV841EVM

These application curves are taken with the TLV841SADL01 part on the TLV841EVM. Please see the TLV841 User Guide for more information.

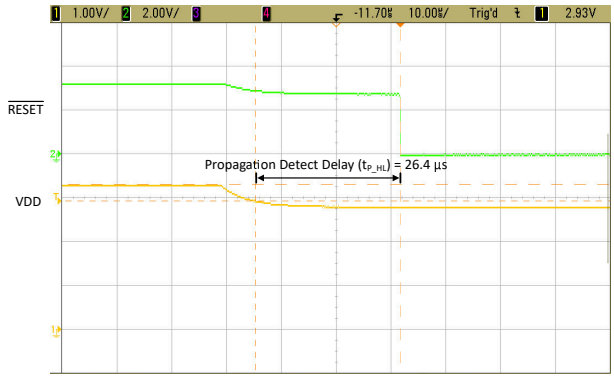


図 9-3. TLV841EVM Propagation Delay Time Delay (t_{D_HL})

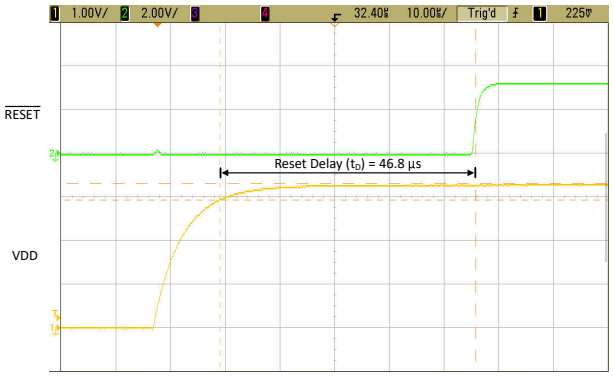


図 9-4. TLV841EVM $\overline{\text{RESET}}$ Time Delay (t_D)

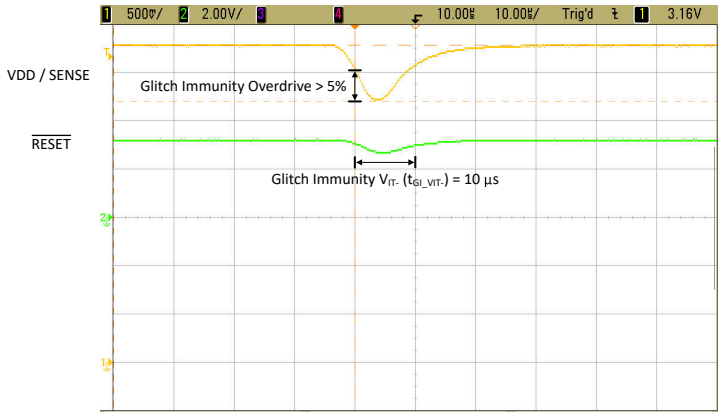


図 9-5. TLV841EVM SENSE Pin Glitch Immunity (t_{GI_VIT-})

10 Power Supply Recommendations

These devices are designed to operate from an input supply with a voltage range between 0.7 V and 5.5 V. TI recommends an input supply capacitor of 0.1 µF between the VDD pin and GND pin. This device has a 6 V absolute maximum rating on the VDD pin. If the voltage supply providing power to VDD is susceptible to any large voltage transient that can exceed 6 V, additional precautions must be taken.

11 Layout

11.1 Layout Guidelines

Make sure that the connection to the VDD pin is low impedance. Good analog design practice recommends placing a minimum 0.1 µF ceramic capacitor as near as possible to the VDD pin. If a capacitor is not connected to the CT pin (TLV841C), then minimize parasitic capacitance on this pin so the rest time delay is not adversely affected.

- Make sure that the connection to the VDD pin is low impedance. Good analog design practice is to place a greater than 0.1 µF ceramic capacitor as near as possible to the VDD pin.
- If a C_{CT_EXT} capacitor is used (TLV841C), place the capacitor as close as possible to the CT pin. If the CT pin is left unconnected, make sure to minimize the amount of parasitic capacitance on the pin to less than 5 pF.
- If a SENSE capacitor (C_{SENSE}) is used (TLV841S), place the capacitor as close as possible to the SENSE pin to further improve the noise immunity on the SENSE pin. Placing a 10 nF to 100 nF capacitor between the SENSE pin and GND can reduce the sensitivity to sensitivity to transient voltages on the monitored signal.
- Place the pull-up resistors on $\overline{\text{RESET}}$ pin as close to the pin as possible.

11.2 Layout Example

The layout example in 図 11-1 shows how the TLV841S is laid out on a printed circuit board (PCB) for every device variant.

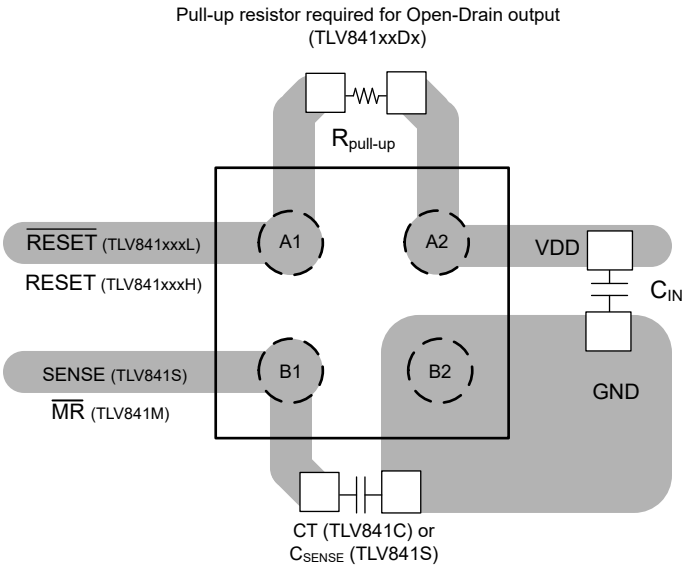


図 11-1. TLV841 Recommended Layout

12 Device and Documentation Support

12.1 Device Nomenclature

図 5-1 in セクション 5 and 表 12-1 shows how to decode the function of the device based on its part number.

表 12-1. Device Naming Convention

DESCRIPTION	NOMENCLATURE	VALUE
Generic Part number	TLV841	TLV841
Feature Option	S	SENSE pin option
	C	CT pin for programmable delay using external capacitor
	M	Manual Reset ($\overline{MR}$) pin option
Delay Option	A	40 µs (No internal reset time delay)
	B	2 ms reset time delay
	C	10 ms reset time delay
	D	30 ms reset time delay
	E	50 ms reset time delay
	F	80 ms reset time delay
	G	100 ms reset time delay
	H	150 ms reset time delay
	I	200 ms reset time delay
Variant code (Output Topology)	DL	Open-Drain, Active-Low
	PL	Push-Pull, Active-Low
	DH	Open-Drain, Active-High
	PH	Push-Pull, Active-High
Detect Voltage Option	## (two characters)	Example: 12 stands for 1.2 V threshold
Package	YBH	DSBGA (4)
Reel	R	Large Reel

12.2 Documentation Support

12.2.1 Related Documentation

The following related documents are available for download at www.ti.com:

- *Optimizing Resistor Dividers at a Comparator Input*, SLVA450
- *Sensitivity Analysis for Power Supply Design*, SLVA481
- *Getting Started With TMS320C28x Digital Signal Controllers*, SPRAAM0
- TLV841EVM-775 Evaluation Module User Guide, SBVU030
- C2000 Delfino Family of Microprocessors
- TMS320F2833x microcontroller, SPRS439

12.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.4 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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12.6 静電気放電に関する注意事項

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

12.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV841SADL01YBHR	Active	Production	DSBGA (YBH) | 4	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	9
TLV841SADL01YBHR.A	Active	Production	DSBGA (YBH) | 4	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	9
TLV841SADL41YBHR	Active	Production	DSBGA (YBH) | 4	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	T
TLV841SADL41YBHR.A	Active	Production	DSBGA (YBH) | 4	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	T

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

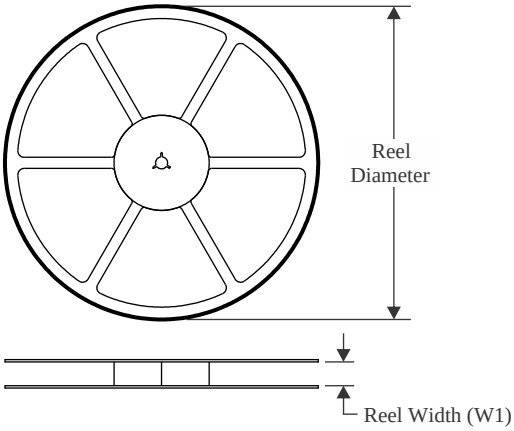
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

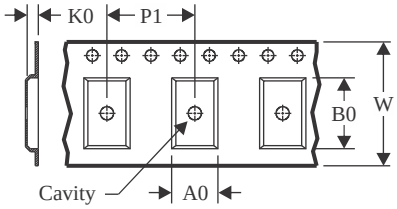
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

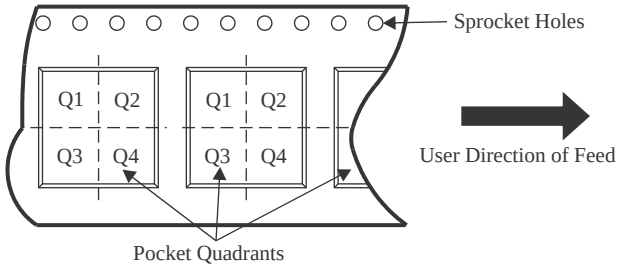


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

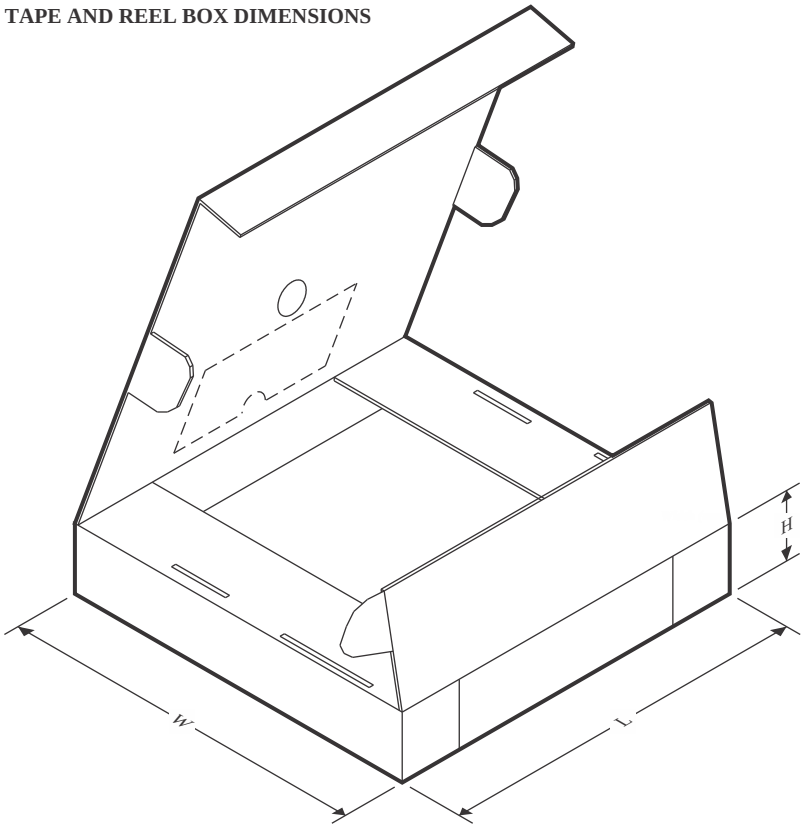
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV841SADL01YBHR	DSBGA	YBH	4	3000	180.0	8.4	0.84	0.84	0.48	4.0	8.0	Q1
TLV841SADL41YBHR	DSBGA	YBH	4	3000	180.0	8.4	0.84	0.84	0.48	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

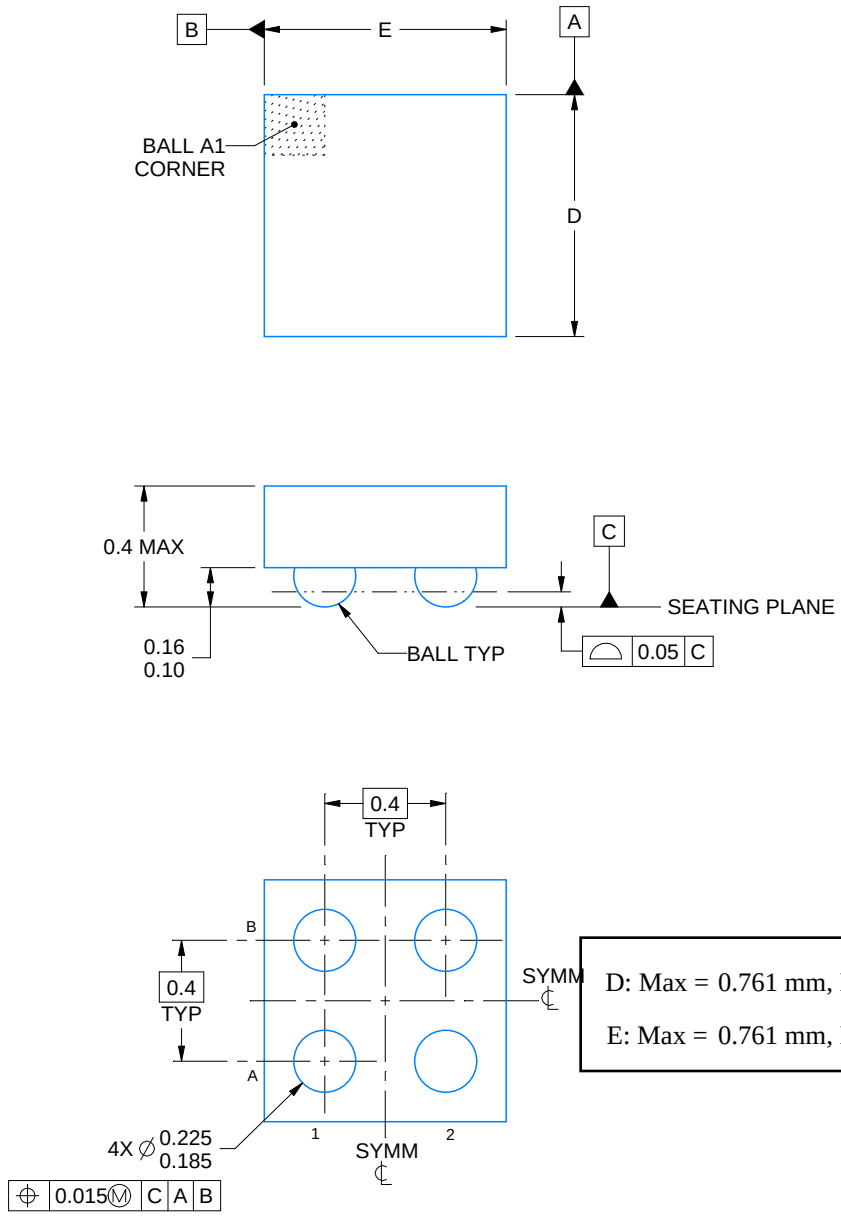
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV841SADL01YBHR	DSBGA	YBH	4	3000	182.0	182.0	20.0
TLV841SADL41YBHR	DSBGA	YBH	4	3000	182.0	182.0	20.0

PACKAGE OUTLINE

YBH0004

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



4224051/A 11/2017

NOTES:

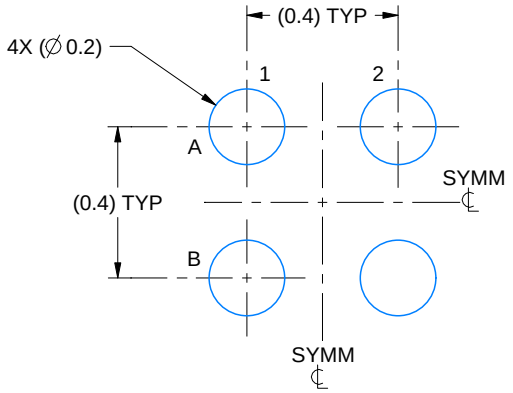
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

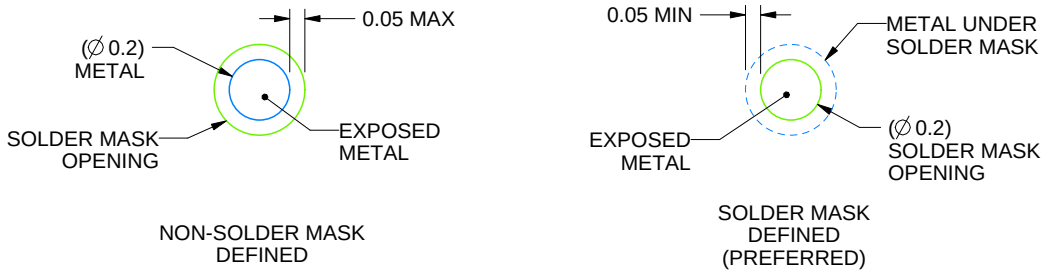
YBH0004

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

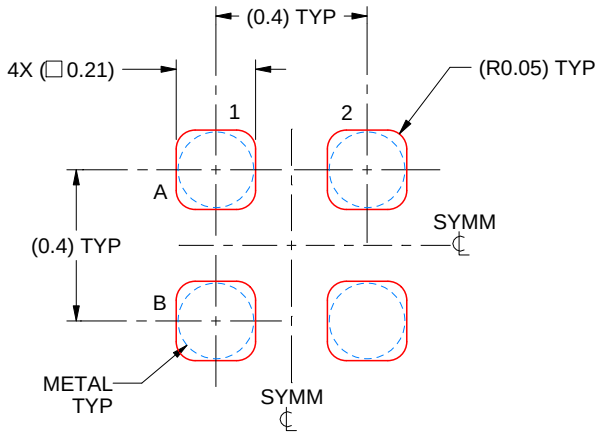
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YBH0004

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 50X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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最終更新日：2025 年 10 月