

FEATURES

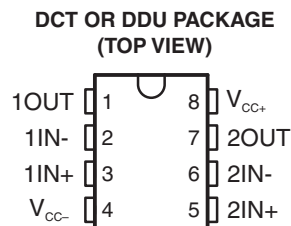
- Low Supply Current...20 μ A Typ
- Single Power Supply
- Rail-to-Rail Common-Mode Input Voltage Range
- Push-Pull Output Circuit
- Low Input-Bias Current

APPLICATIONS

- Battery Packs for Sensing Battery Voltage
- MP3 Players, Digital Cameras, PMPs
- Cellular Phones, PDAs, Notebook Computers
- Test Equipment
- General-Purpose Low-Voltage Applications

DESCRIPTION/ORDERING INFORMATION

The TLV7256 is a CMOS-type general-purpose dual comparator capable of single power-supply operation and using lower supply currents than the conventional bipolar comparators. Its push-pull output can connect directly to local ICs such as TTL and CMOS circuits.



ORDERING INFORMATION⁽¹⁾

T_A	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SSOP – DCT	Reel of 3000	TLV7256IDCTR	PREVIEW
		Reel of 250	TLV7256IDCTT	
	VSSOP – DDU	Reel of 3000	TLV7256IDDUR	YAUA

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
 (2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Typical Application Circuit

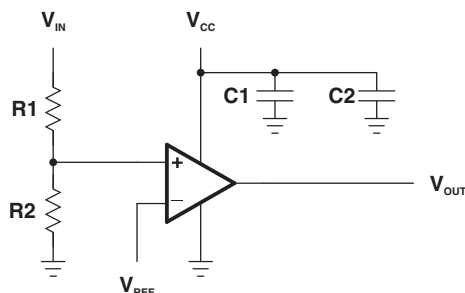


Figure 1. Threshold Detector



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TLV7256

DUAL COMPARATOR

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Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	1.5	7	V
V _{ID}	Differential input voltage			V
V _I	Input voltage	V _{CC-}	V _{CC+}	V
I _O	Output current		±35	mA
θ _{JA}	Thermal resistance, junction to ambient ⁽²⁾	DCT package	220	°C/W
		DDU package	227	
P _D	Power dissipation	DCT package	250	mW
		DDU package	200	
T _A	Operating free-air temperature range	–40	85	°C
T _{stg}	Storage temperature range	–55	125	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Package thermal impedance is calculated according to JESD 51-7.

Recommended Operating Conditions

		MIN	MAX	UNIT
V _{CC}	Supply voltage	1.8	5	V
T _A	Operating free-air temperature	–40	85	°C

Electrical Characteristics

$V_{CC+} = 5\text{ V}$, $V_{CC-} = \text{GND}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage		25°C		±2	±7	mV
			–40°C to 85°C			±8	
I_{IO}	Input offset current		25°C		2		pA
I_I	Input bias current		25°C		4		pA
V_{CM}	Common-mode input voltage		25°C	0		V_{CC}	V
CMRR	Common-mode rejection ratio	$\Delta V_{CM} = 5\text{ V}$	25°C	48	65		dB
		$0 \leq V_{CM} \leq 5\text{ V}$	–40°C to 85°C	48			
I_{CC}	Supply current	Output = High, $V_{IN} = 5\text{ V}$	25°C		37	51	μA
		Output = Low, $V_{IN} = 5\text{ V}$			40	60	
		Output = High, $V_{IN} = 5\text{ V}$	–40°C to 85°C			61	
		Output = Low, $V_{IN} = 5\text{ V}$				70	
		Output = High, $V_{IN} = 2.5\text{ V}$	25°C		20	32	
		Output = Low, $V_{IN} = 2.5\text{ V}$			26	42	
		Output = High, $V_{IN} = 2.5\text{ V}$	–40°C to 85°C			40	
		Output = Low, $V_{IN} = 2.5\text{ V}$				53	
A_{VD}	Voltage gain	$V_D = 3\text{ V}$, $1\text{ V} \leq V_{OUT} \leq 4\text{ V}$	25°C		88		dB
I_{sink}	Sink current	$V_{OL} = 0.5\text{ V}$	25°C	25	33		mA
			–40°C to 85°C	20			
I_{source}	Source current	$V_{OH} = 4.5\text{ V}$	25°C	30	35		mA
			–40°C to 85°C	25			
V_{OL}	Low-level output voltage	$I_{sink} = 5\text{ mA}$	25°C		0.07	0.12	V
			–40°C to 85°C			0.20	
V_{OH}	High-level output voltage	$I_{source} = 5\text{ mA}$	25°C	4.9	4.93		V
			–40°C to 85°C	4.85			

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Electrical Characteristics

$V_{CC+} = 2.7\text{ V}$, $V_{CC-} = \text{GND}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage		25°C		±2	±8	mV
			–40°C to 85°C			±9	
I_{IO}	Input offset current		25°C		2		pA
I_I	Input bias current		25°C		4		pA
V_{CM}	Common-mode input voltage		25°C	0		V_{CC}	V
CMRR	Common-mode rejection ratio	$\Delta V_{CM} = 2.7\text{ V}$	25°C	42	57		dB
		$0 \leq V_{CM} \leq 2.7\text{ V}$	–40°C to 85°C	42			
I_{CC}	Supply current	Output = High, $V_{IN} = 2.7\text{ V}$	25°C		30	55	μA
		Output = Low, $V_{IN} = 2.7\text{ V}$			36	55	
		Output = High, $V_{IN} = 2.7\text{ V}$	–40°C to 85°C			65	
		Output = Low, $V_{IN} = 2.7\text{ V}$				65	
		Output = High, $V_{IN} = 1.35\text{ V}$	25°C		30	48	
		Output = Low, $V_{IN} = 1.35\text{ V}$			35	55	
		Output = High, $V_{IN} = 1.35\text{ V}$	–40°C to 85°C			55	
		Output = Low, $V_{IN} = 1.35\text{ V}$				65	
A_{VD}	Voltage gain	$V_D = 1.7\text{ V}$, $0.5\text{ V} \leq V_{OUT} \leq 2.2\text{ V}$	25°C		88		dB
I_{sink}	Sink current	$V_{OL} = 0.5\text{ V}$	25°C	13	18		mA
			–40°C to 85°C	11			
I_{source}	Source current	$V_{OH} = 2.2\text{ V}$	25°C	15	20		mA
			–40°C to 85°C	13			
V_{OL}	Low-level output voltage	$I_{sink} = 5\text{ mA}$	25°C		0.11	0.16	V
			–40°C to 85°C			0.19	
V_{OH}	High-level output voltage	$I_{source} = 5\text{ mA}$	25°C	2.54	2.60		V
			–40°C to 85°C	2.45			

Electrical Characteristics

$V_{CC+} = 1.8\text{ V}$, $V_{CC-} = \text{GND}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage		25°C		±2	±8	mV
			–40°C to 85°C			±9	
I_{IO}	Input offset current		25°C		2		pA
I_I	Input bias current		25°C		4		pA
V_{CM}	Common-mode input voltage		25°C	0		$V_{CC} - 0.3$	V
CMRR	Common-mode rejection ratio	$\Delta V_{CM} = 5\text{ V}$	25°C	40	55		dB
		$0 \leq V_{CM} \leq 5\text{ V}$	–40°C to 85°C	40			
I_{CC}	Supply current	Output = High, $V_{IN} = 1.8\text{ V}$	25°C		30	55	μA
		Output = Low, $V_{IN} = 1.8\text{ V}$			33	47	
		Output = High, $V_{IN} = 1.8\text{ V}$	–40°C to 85°C			60	
		Output = Low, $V_{IN} = 1.8\text{ V}$				51	
		Output = High, $V_{IN} = 0.9\text{ V}$	25°C		20	32	
		Output = Low, $V_{IN} = 0.9\text{ V}$			25	37	
		Output = High, $V_{IN} = 0.9\text{ V}$	–40°C to 85°C			34	
		Output = Low, $V_{IN} = 0.9\text{ V}$				40	
A_{VD}	Voltage gain	$V_D = 1.1\text{ V}$, $0.4\text{ V} \leq V_{OUT} \leq 1.5\text{ V}$	25°C		88		dB
I_{sink}	Sink current	$V_{OL} = 0.5\text{ V}$	25°C	6	9		mA
			–40°C to 85°C	5			
I_{source}	Source current	$V_{OH} = 2.2\text{ V}$	25°C	5	9		mA
			–40°C to 85°C	4			
V_{OL}	Low-level output voltage	$I_{sink} = 5\text{ mA}$	25°C		0.2	0.34	V
			–40°C to 85°C			0.39	
V_{OH}	High-level output voltage	$I_{source} = 5\text{ mA}$	25°C	1.3	1.6		V
			–40°C to 85°C	1.2			

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Switching Characteristics

$V_{CC+} = 5\text{ V}$, $V_{CC-} = \text{GND}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP	UNIT
t_{PLH}	Propagation delay time (turn on)	Overdrive = 100 mV	680	ns
		TTL step input	500	
t_{PHL}	Propagation delay time (turn off)	Overdrive = 100 mV	250	ns
		TTL step input	380	
t_{TLH}	Response time	Overdrive = 100 mV	60	ns
t_{THL}			8	

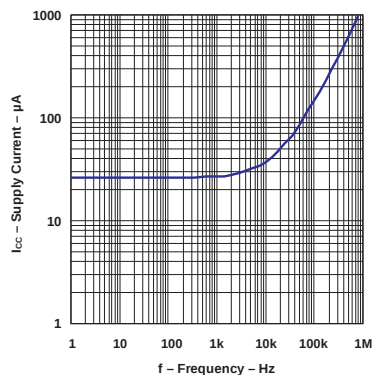
Switching Characteristics

$V_{CC+} = 3\text{ V}$, $V_{CC-} = \text{GND}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

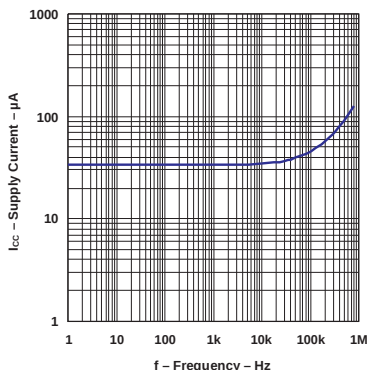
PARAMETER		TEST CONDITIONS	TYP	UNIT
t_{PLH}	Propagation delay time (turn on)	Overdrive = 100 mV	550	ns
t_{PHL}	Propagation delay time (turn off)	Overdrive = 100 mV	250	ns
t_{TLH}	Response time	Overdrive = 100 mV	30	ns
t_{THL}			8	

TYPICAL CHARACTERISTICS

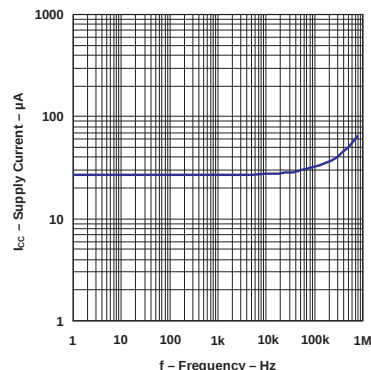
SUPPLY CURRENT
VS
FREQUENCY
 $V_{CC} = 5\text{ V}$



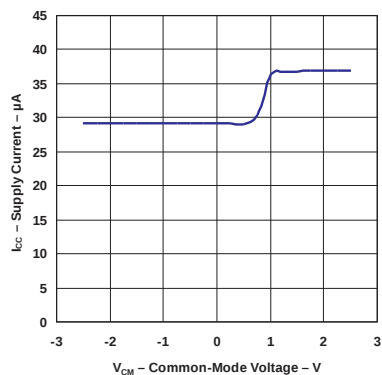
SUPPLY CURRENT
VS
FREQUENCY
 $V_{CC} = 2.7\text{ V}$



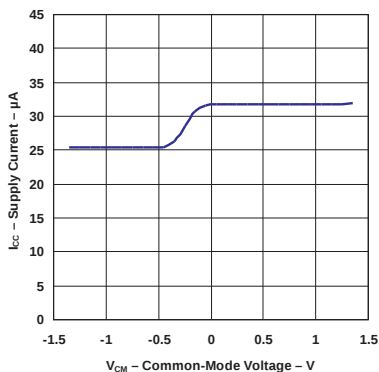
SUPPLY CURRENT
VS
FREQUENCY
 $V_{CC} = 1.8\text{ V}$



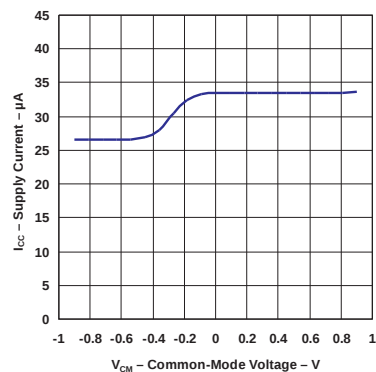
SUPPLY CURRENT
VS
COMMON-MODE VOLTAGE
 $V_{CC} = \pm 2.5\text{ V}$



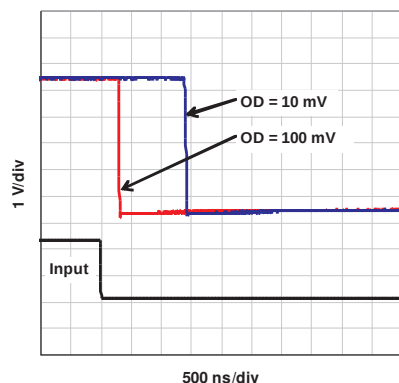
SUPPLY CURRENT
VS
COMMON-MODE VOLTAGE
 $V_{CC} = \pm 1.35\text{ V}$



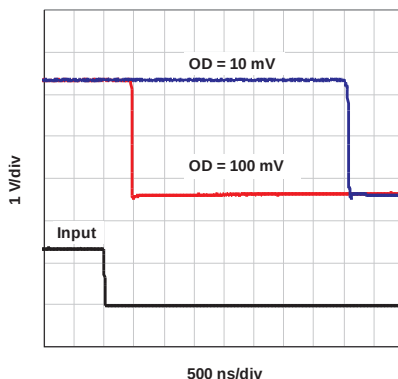
SUPPLY CURRENT
VS
COMMON-MODE VOLTAGE
 $V_{CC} = \pm 0.9\text{ V}$



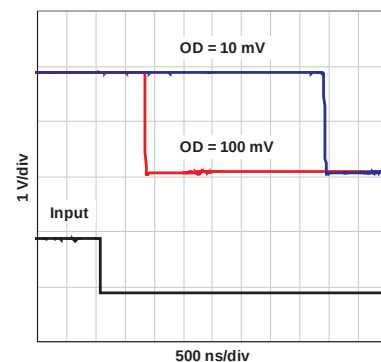
PROPAGATION DELAY TIME,
HIGH TO LOW
 $V_{CC} = 5\text{ V}$



PROPAGATION DELAY TIME,
HIGH TO LOW
 $V_{CC} = 2.7\text{ V}$

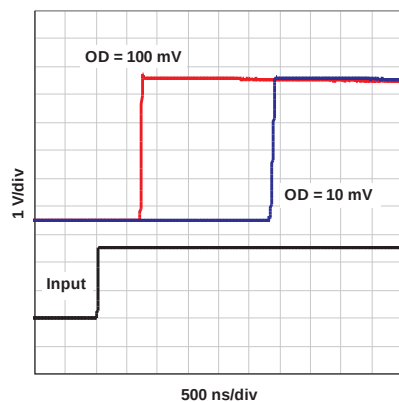


PROPAGATION DELAY TIME,
HIGH TO LOW
 $V_{CC} = 1.8\text{ V}$

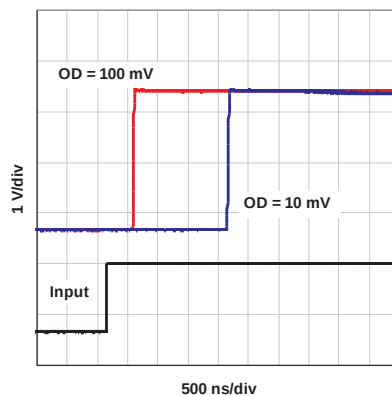


TYPICAL CHARACTERISTICS (continued)

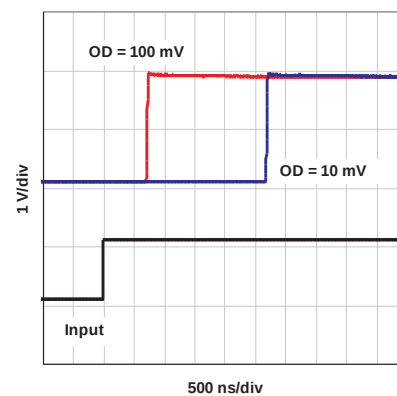
PROPAGATION DELAY TIME,
LOW TO HIGH
 $V_{CC} = 5\text{ V}$



PROPAGATION DELAY TIME,
LOW TO HIGH
 $V_{CC} = 2.7\text{ V}$



PROPAGATION DELAY TIME,
LOW TO HIGH
 $V_{CC} = 1.8\text{ V}$



PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV7256IDDUR	Active	Production	VSSOP (DDU) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YAUUA
TLV7256IDDUR.A	Active	Production	VSSOP (DDU) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YAUUA
TLV7256IDDURG4	Active	Production	VSSOP (DDU) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YAUUA
TLV7256IDDURG4.A	Active	Production	VSSOP (DDU) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YAUUA

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV7256IDDUR	VSSOP	DDU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
TLV7256IDDURG4	VSSOP	DDU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

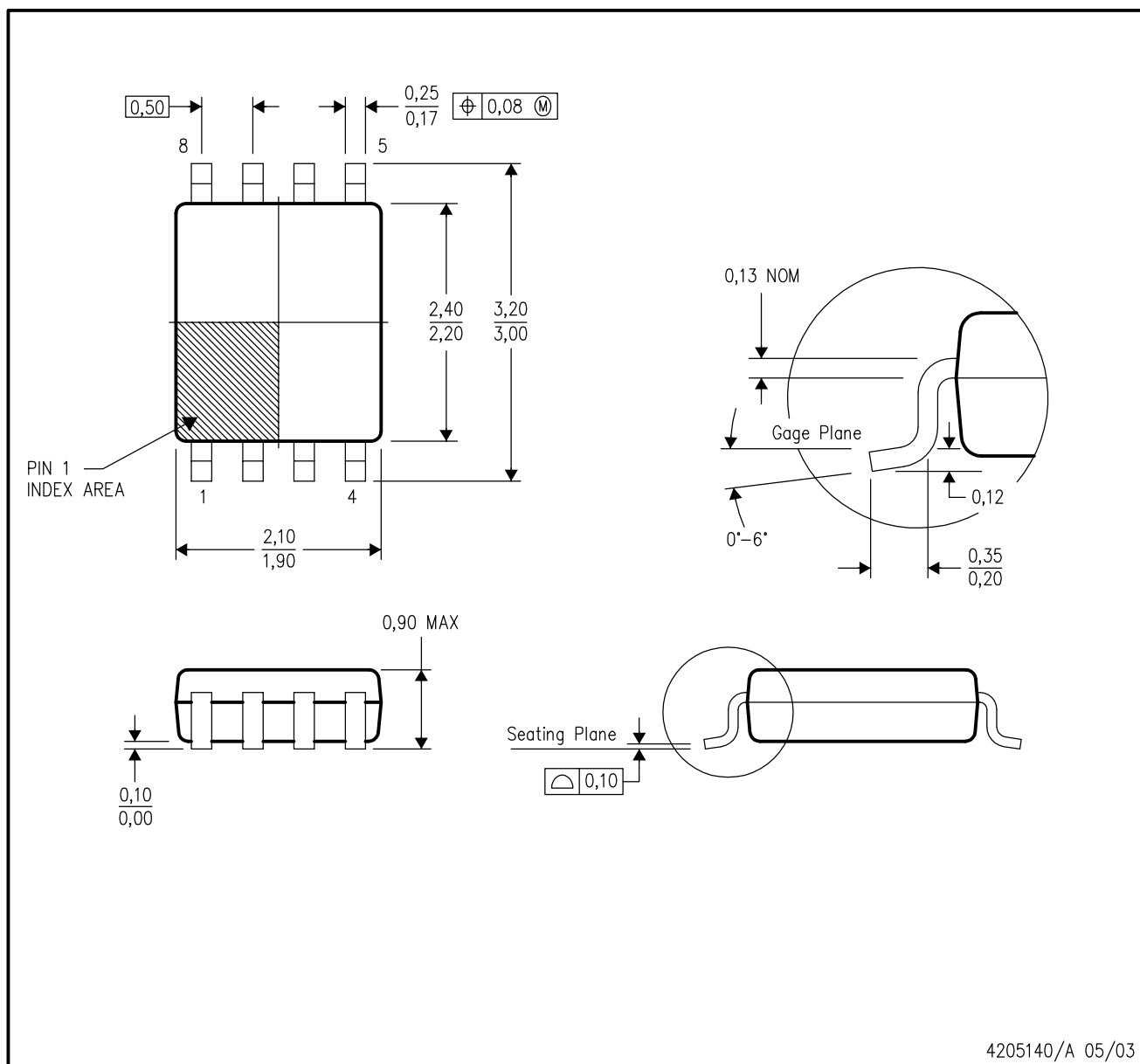


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV7256IDDUR	VSSOP	DDU	8	3000	202.0	201.0	28.0
TLV7256IDDURG4	VSSOP	DDU	8	3000	202.0	201.0	28.0

DDU (R-PDSO-G8)

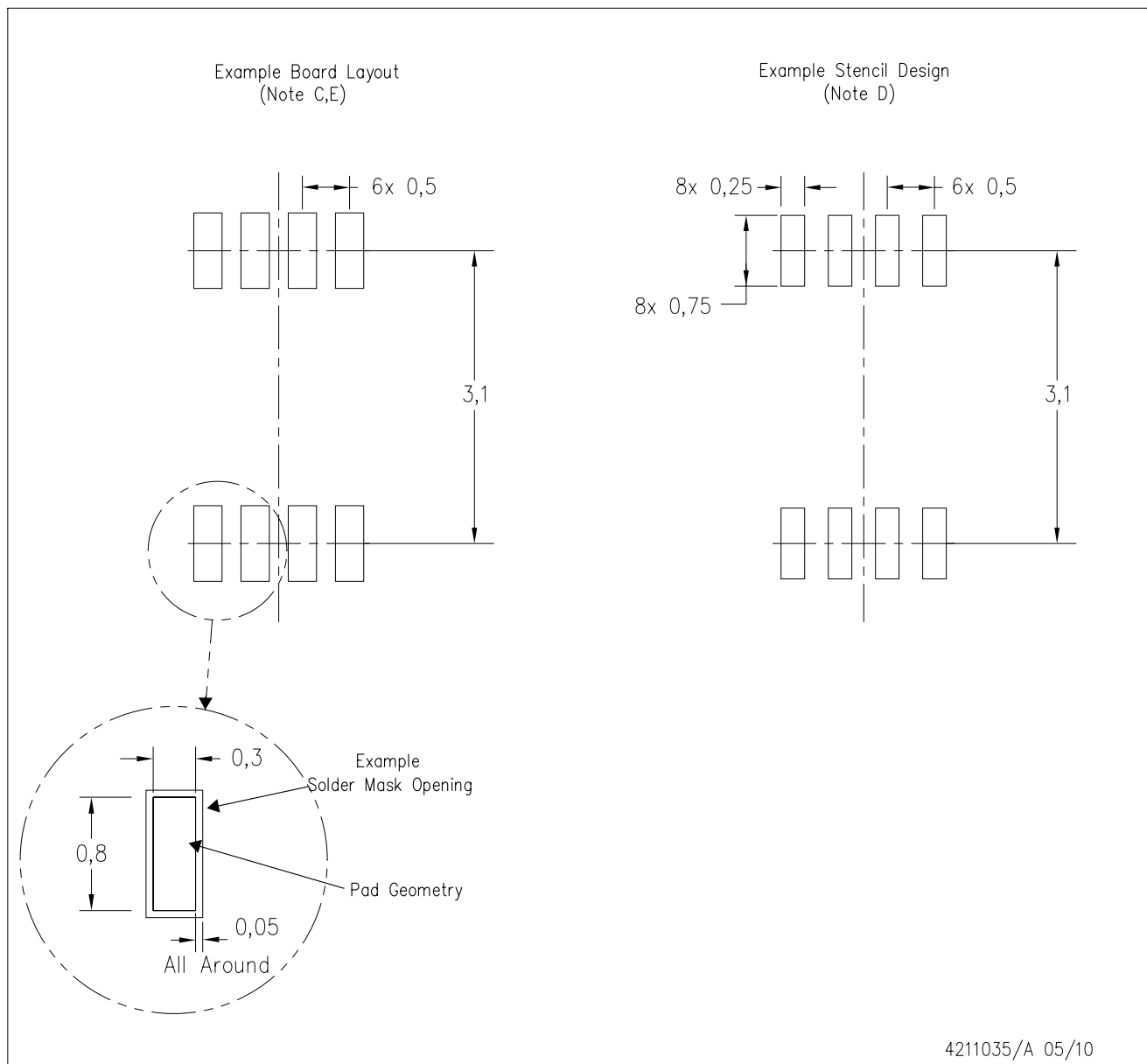
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion.
 - Falls within JEDEC MO-187 variation CA.

DDU (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE (DIE UP)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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