

TLV701x および TLV702x 小型、低消費電力、低電圧コンパレータ

1 特長

- 超小型パッケージ: X2SON (0.8 × 0.8mm²)
- 標準パッケージ: SOT23、SC70、VSSOP
- 広い電源電圧範囲: 1.6V~6.5V
- 静止電流: 5μA
- 短い伝搬遅延: 260ns
- レール・ツー・レールの同相入力電圧
- 内部ヒステリシス
- プッシュプルおよびオープンドレインの出力オプション
- 入力オーバードライブでの位相反転なし
- 動作時周囲温度: -40°C~125°C

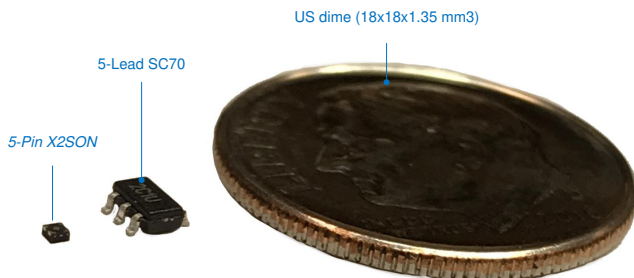
2 アプリケーション

- 携帯電話およびタブレット
- 携帯用およびバッテリー駆動の機器
- IR 受信機
- レベル変換器
- スレッショルド検出器および弁別装置
- ウィンドウ・コンパレータ
- ゼロクロス検出器

3 概要

TLV7011/7021 (シングル・チャネル) および TLV7012/7022 (デュアル・チャネル) は、低電圧で動作し、レール・ツー・レール入力をサポートするマイクロパワー・コンパレータです。これらのコンパレータは 0.8mm × 0.8mm の超小型リードレス・パッケージと標準のリード・パッケージで供給され、スマートフォンや他の携帯用またはバッテリー駆動アプリケーションなど、スペースに制約のある設計に適しています。

X2SONパッケージと、SC70および米10セント硬貨との比較



TLV701x および TLV702x は、速度と消費電力の組み合わせが非常に優れており、伝搬遅延は 260ns、静止消費電流は 5μA です。この高速な応答時間と Micro-Power との組み合わせから、電力の限られたシステムでも、フォルト状況を監視して迅速に応答できます。これらのコンパレータの動作電圧範囲は 1.6V~6.5V で、3V および 5V のシステムと互換性があります。

また、これらコンパレータはオーバードライブ入力について出力の位相反転がなく、内部的なヒステリシスを備えています。これらの特長から、このファミリのコンパレータは過酷でノイズの大きな環境において、ゆっくりと変化する入力信号をクリーンなデジタル出力へ変換する必要がある場合に、正確な電圧を監視するため最適です。

製品情報⁽¹⁾

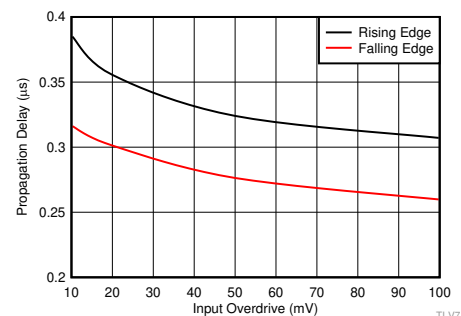
型番	パッケージ (ピン数)	本体サイズ(公称)
TLV7011、 TLV7021	X2SON (5)	0.80mm×0.80mm
	SC70 (5)	2.00mm×1.25mm
	SOT-23 (5)	2.90mm×1.60mm
TLV7012、TLV7022	VSSOP (8)	3mm×3mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

TLV70x1ファミリの低消費電力コンパレータ

型番	出力	I _Q (標準値)	t _{PD} (標準値)
TLV701x	プッシュプル	5μA	260ns
TLV702x	オープンドレイン	5μA	260ns
TLV703x	プッシュプル	335nA	3μs
TLV704x	オープンドレイン	335nA	3μs

伝搬遅延とオーバードライブとの関係



T_A = 25°C, V_{CC} = 5V, C_L = 15pF

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4 改訂履歴

Revision D (February 2019) から Revision E に変更	Page
• デュアル・チャネル・オプションを 追加	1

Revision C (March 2018) から Revision D に変更	Page
• 「特長」にリード・パッケージ・オプションを 追加	1
• SOT23 パッケージのプレビュー・ステータス 削除	1
• Deleted preview status of SOT23 package	4

Revision B (November 2017) から Revision C に変更	Page
• プレビューのSC70パッケージを量産データに変更	1

Revision A (July 2017) から Revision B に変更	Page
• 伝播遅延を200nsから260nsに変更	1
• データシートにプレビューのSC70およびSOT-23パッケージを追加	1
• マーケティングの要求に対応して「TLV70x1 ファミリの Micropower コンパレータ」表を追加	1
• 主要な図のタイトルを「伝播遅延とオーバードライブとの関係(TLV7011)」から「伝播遅延とオーバードライブとの関係」に変更	1
• Removed (TLV7011 only) text from several <i>Typical Characteristics</i> graphs	11
• Removed some <i>Typical Characteristics</i> graphs	11
• Added 図 14	11
• Added 図 21	13
• Added content to the <i>Inputs</i> section	17
• Added the <i>IR Receiver Analog Front End</i> section	22

2017年5月発行のものから更新

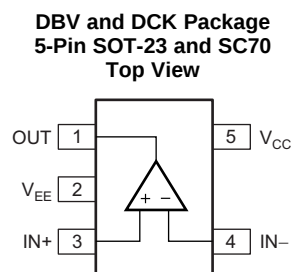
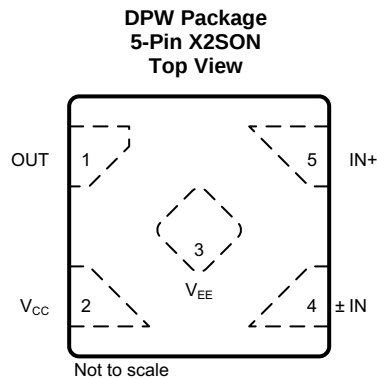
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• デバイスのステータスを「事前情報」から「量産データ」に変更	1
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5 概要 (続き)

TLV701x は、LED の制御または容量性負荷の駆動を行う際に数ミリアンペアの電流をシンクおよびソースできるプッシュプル出力段を備えています。TLV702x にはオープンドレインの出力段があり、 V_{CC} を超える出力レベルが可能であるため、レベル変換器やバイポーラからシングルエンドへのコンバータに適しています。

6 Pin Configuration and Functions

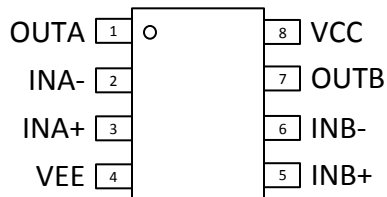


Pin Functions

PIN			I/O/P ⁽¹⁾	DESCRIPTION
NAME	X2SON	SOT-23, SC70		
OUT	1	1	O	Output
V_{CC}	2	5	P	Positive (highest) power supply
V_{EE}	3	2	P	Negative (lowest) power supply
IN–	4	4	I	Inverting input
IN+	5	3	I	Noninverting input

(1) I = Input, O = Output, P = Power

**TLV7012/22 DGG Packages
8-Pin VSSOP
Top View**



Pin Functions: TLV7012/22

PIN		I/O	DESCRIPTION
NAME	NO.		
INA–	2	I	Inverting input, channel A
INA+	3	I	Noninverting input, channel A
INB–	6	I	Inverting input, channel B
INB+	5	I	Noninverting input, channel B
OUTA	1	O	Output, channel A
OUTB	7	O	Output, channel B
VEE	4	—	Negative (lowest) supply or ground (for single-supply operation)
VCC	8	—	Positive (highest) supply

7 Specifications

7.1 Absolute Maximum Ratings (Single)

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Supply voltage ($V_S = V_{CC} - V_{EE}$)			6	V
Input pins (IN+, IN-) ⁽²⁾		$V_{EE} - 0.3$	6	V
Current into Input pins (IN+, IN-) ⁽²⁾			±10	mA
Output (OUT)	TLV7011/7012 ⁽³⁾	$V_{EE} - 0.3$	$V_{CC} + 0.3$	V
	TLV7021/7022	$V_{EE} - 0.3$	6	
Output short-circuit duration ⁽⁴⁾			10	s
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Input terminals are diode-clamped to V_{EE} . Input signals that can swing 0.3V below V_{EE} must be current-limited to 10mA or less.
- (3) Output maximum is ($V_{CC} + 0.3V$) or 6V, whichever is less.
- (4) Short-circuit to ground, one comparator per package.

7.2 Absolute Maximum Ratings (Dual)

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Supply voltage $V_S = V_{CC} - V_{EE}$		-0.3	7	V
Input pins (IN+, IN-) ⁽²⁾		$V_{EE} - 0.3$	7	V
Current into Input pins (IN+, IN-)			±10	mA
Output (OUT) (TLV7012) ⁽³⁾		$V_{EE} - 0.3$	$V_{CC} + 0.3$	V
Output (OUT) (TLV7022)		$V_{EE} - 0.3$	7	V
Output short-circuit duration ⁽⁴⁾			10	s
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Input terminals are diode-clamped to V_{EE} . Input signals that can swing 0.3V below V_{EE} must be current-limited to 10mA or less.
- (3) Output maximum is ($V_{CC} + 0.3V$) or 7 V, whichever is less.
- (4) Short-circuit to ground, one comparator per package.

7.3 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.4 Recommended Operating Conditions (Single)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage ($V_S = V_{CC} - V_{EE}$)		1.6		5.5	V
Input Voltage Range		$V_{EE} - 0.1$		$V_{CC} + 0.2$	V
Ambient temperature, T_A		-40		125	°C

7.5 Recommended Operating Conditions (Dual)

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage $V_S = V_{CC} - V_{EE}$	1.6	6.5	V
Input voltage range	$V_{CC} - 0.1$	$V_{EE} + 0.2$	V
Ambient temperature, T_A	-40	125	°C

7.6 Thermal Information (Single)

THERMAL METRIC ⁽¹⁾		TLV7011/TLV7021			UNIT
		DPW (X2SON)	DBV (SOT23)	DCK (SC70)	
		5 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	497.5	306.3	278.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	275.5	228.4	188.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	372.2	166.5	113.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	55.5	138.5	82.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	370.3	165.3	112.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	165.1	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.7 Thermal Information (Dual)

THERMAL METRIC ⁽¹⁾		TLV7012/TLV7022	UNIT
		DGK (VSSOP)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	211.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	96.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	133.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	28.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	131.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.8 Electrical Characteristics (Single)

$V_S = 1.8\text{ V}$ to 5 V , $V_{CM} = V_S / 2$; minimum and maximum values are at $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ (unless otherwise noted). Typical values are at $T_A = 25^\circ\text{C}$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage		± 0.5	± 8	mV
V_{HYS}	Hysteresis	1.2	4.2	14	mV
V_{CM}	Common-mode voltage range	V_{EE}		$V_{CC} + 0.1$	V
		$V_{EE} + 0.1$		$V_{CC} + 0.1$	
I_B	Input bias current		5		pA
I_{OS}	Input offset current		1		pA
V_{OH}	Output voltage high (for TLV7011 only)	4.7	4.8		V
V_{OL}	Output voltage low		120	220	mV
I_{LKG}	Open-drain output leakage current (TLV7021 only)		100		pA
CMRR	Common-mode rejection ratio		78		dB
PSRR	Power supply rejection ratio		78		dB
I_{SC}	Short-circuit current	$V_S = 5\text{ V}$, sourcing	65		mA
		$V_S = 5\text{ V}$, sinking	44		
I_{CC}	Supply current	$V_S = 1.8\text{ V}$, no load, $V_{ID} = -0.1\text{ V}$ (Output Low)	5	10	μA

7.9 Switching Characteristics (Single)

Typical values are at $T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$, $V_{CM} = 2.5\text{ V}$; $C_L = 15\text{ pF}$, input overdrive = 100 mV (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low ($R_P = 2.5\text{ k}\Omega$ TLV7021 only)		260		ns
t_{PLH}	Propagation delay time, low-to-high ($R_P = 2.5\text{ k}\Omega$ TLV7021 only)		310		ns
t_R	Rise time (for TLV7011 only)	20% to 80%	5		ns
t_F	Fall time	80% to 20%	5		ns
t_{ON}	Power-up time ⁽¹⁾		20		μs

(1) During power on, V_S must exceed 1.6 V for t_{ON} before the output tracks the input.

7.10 Electrical Characteristics (Dual)

$V_S = 1.8\text{ V}$ to 5 V , $V_{CM} = V_S / 2$; minimum and maximum values are at $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ (unless otherwise noted). Typical values are at $T_A = 25^\circ\text{C}$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input Offset Voltage		± 0.1	± 8	mV
V_{HYS}	Hysteresis		9	15	mV
V_{CM}	Common-mode voltage range	V_{EE}		$V_{CC} + 0.1$	V
I_B	Input bias current		2		pA
I_{OS}	Input offset current		1		pA
V_{OH}	Output voltage high (for TLV7012 only)	$V_S = 5\text{ V}$, $V_{EE} = 0\text{ V}$, $I_O = 3\text{ mA}$	4.65	4.8	V
V_{OL}	Output voltage low	$V_S = 5\text{ V}$, $V_{EE} = 0\text{ V}$, $I_O = 3\text{ mA}$	250	350	mV
I_{LKG}	Open-drain output leakage current (TLV7022 only)	$V_S = 5\text{ V}$, $V_{ID} = +0.1\text{ V}$ (output high), $V_{PULLUP} = V_{CC}$	100		pA
CMRR	Common-mode rejection ratio	$V_{EE} < V_{CM} < V_{CC}$, $V_S = 5\text{ V}$	73		dB
PSRR	Power supply rejection ratio	$V_S = 1.8\text{ V}$ to 5 V , $V_{CM} = V_S / 2$	77		dB
I_{SC}	Short-circuit current	$V_S = 5\text{ V}$, sourcing (for TLV7012 only)	29		mA
		$V_S = 5\text{ V}$, sinking	33		
I_{CC}	Supply current / Channel	$V_S = 1.8\text{ V}$, no load, $V_{ID} = -0.1\text{ V}$ (Output Low)	4.7	9	μA

7.11 Switching Characteristics (Dual)

Typical values are at $T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $V_{CM} = V_S / 2$; $C_L = 15\text{ pF}$, input overdrive = 100 mV (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high to low (RP = $4.99\text{ k}\Omega$ TLV7022 only) ⁽¹⁾		310		ns
t_{PLH}	Propagation delay time, low to high (RP = $4.99\text{ k}\Omega$ TLV7022 only) ⁽¹⁾		260		ns
t_R	Rise time (TLV7012 only)		5		ns
t_F	Fall time		5		ns
t_{ON}	Power-up time		20		μs

(1) The lower limit for RP is $650\text{ }\Omega$

7.12 Timing Diagrams

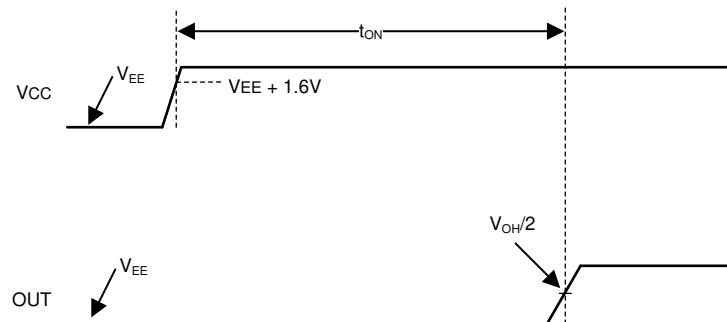


图 1. Start-Up Time Timing Diagram (IN+ > IN-)

Timing Diagrams (continued)

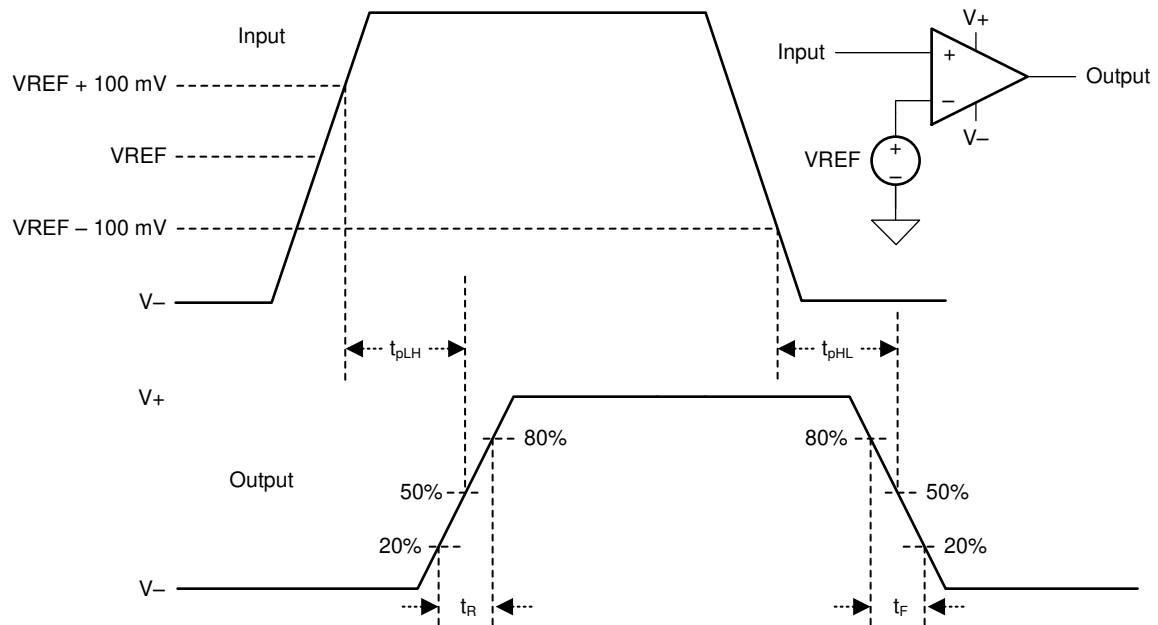
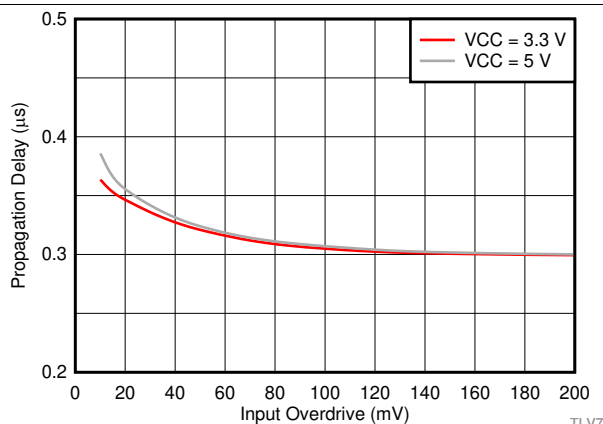


图 2. Propagation Delay Timing Diagram

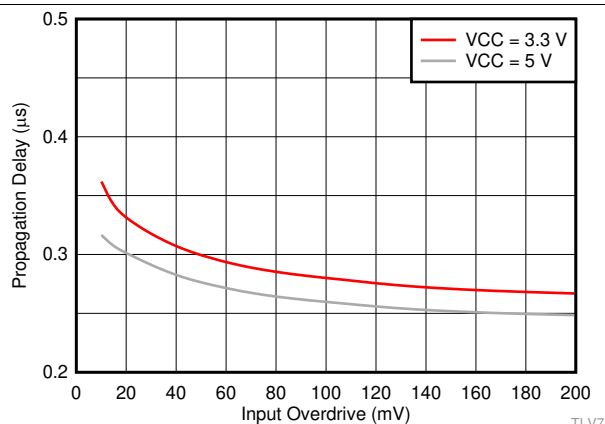
7.13 Typical Characteristics

$T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$, $V_{EE} = 0\text{ V}$, $V_{CM} = V_{CC}/2$, $C_L = 15\text{ pF}$



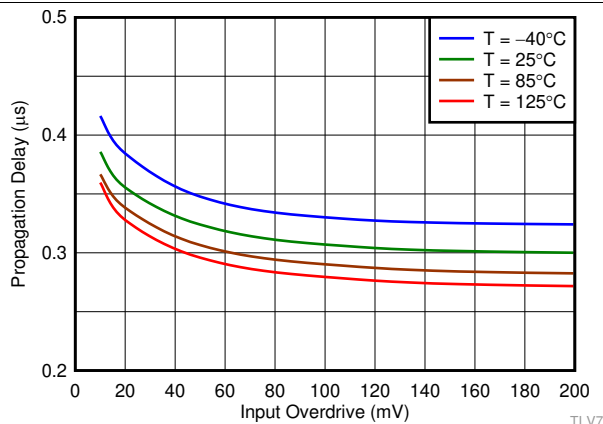
$T_A = 25^\circ\text{C}$,

图 3. TLV7011 Propagation Delay (L-H) vs. Input Overdrive



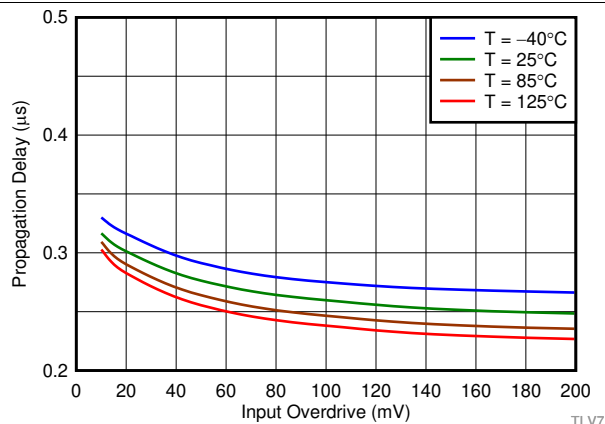
$T_A = 25^\circ\text{C}$

图 4. Propagation Delay (H-L) vs. Input Overdrive



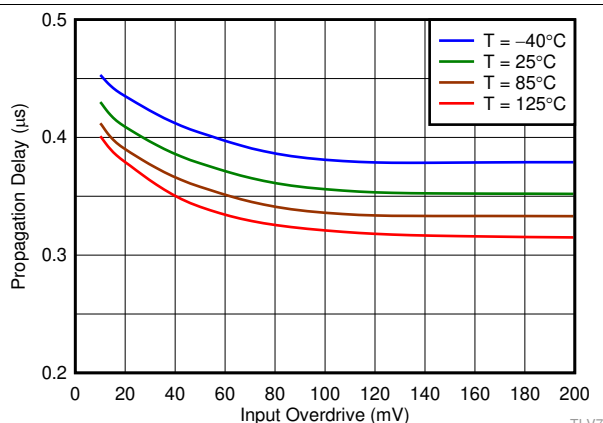
$V_{CC} = 5\text{ V}$

图 5. TLV7011 Propagation Delay (L-H) vs. Input Overdrive



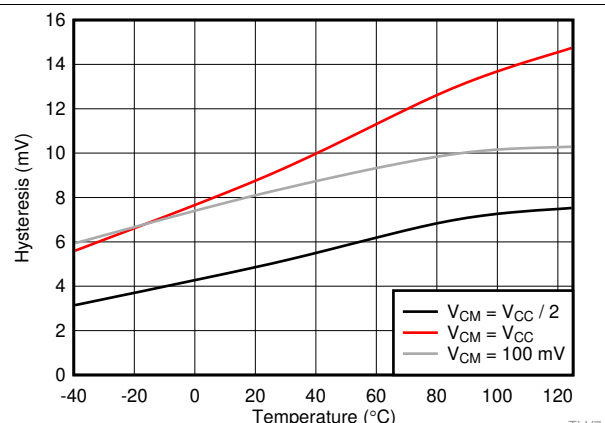
$V_{CC} = 5\text{ V}$

图 6. Propagation Delay (H-L) vs. Input Overdrive



$R_{\text{pull-up}} = 2.5\text{k}$

图 7. TLV7021 Propagation Delay (L-H) vs. Input Overdrive

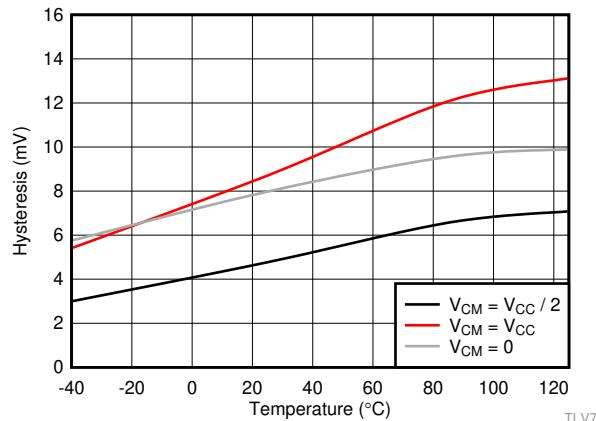


$V_{CC} = 1.8\text{ V}$

图 8. Hysteresis vs. Temperature

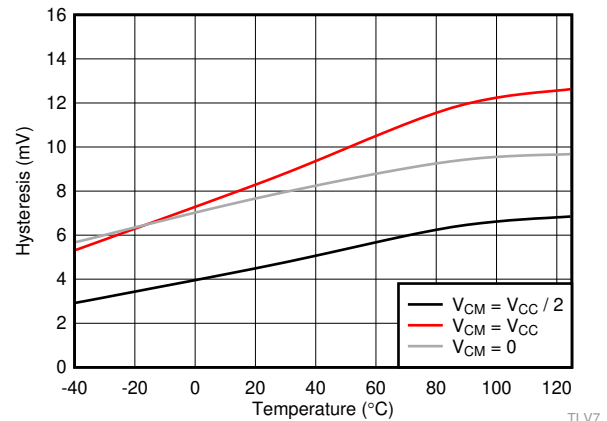
Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$, $V_{EE} = 0\text{ V}$, $V_{CM} = V_{CC}/2$, $C_L = 15\text{ pF}$



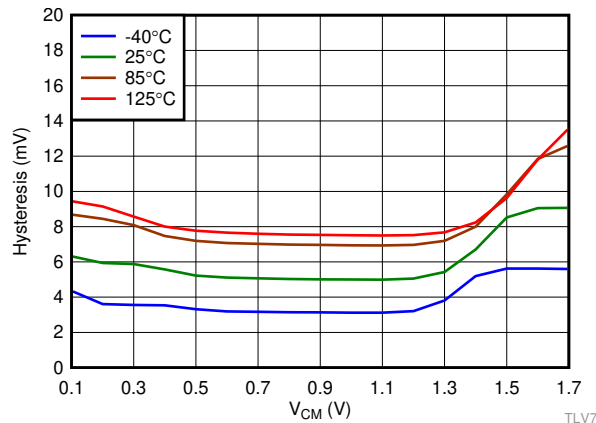
$V_{CC} = 3.3\text{ V}$

Figure 9. Hysteresis vs. Temperature



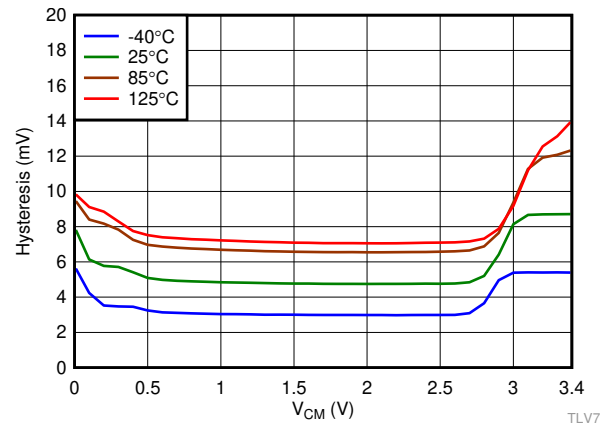
$V_{CC} = 5\text{ V}$

Figure 10. Hysteresis vs. Temperature



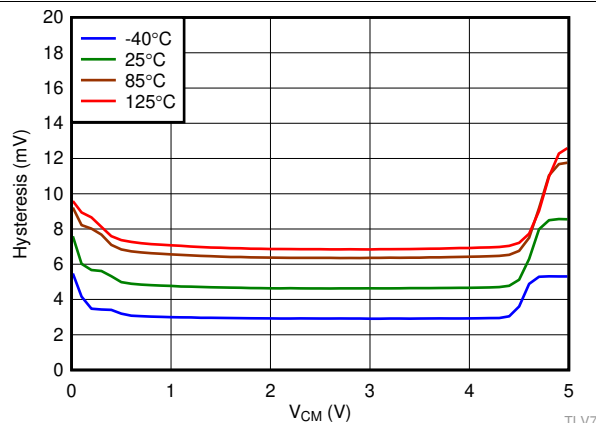
$V_{CC} = 1.8\text{ V}$

Figure 11. Hysteresis vs. V_{CM}



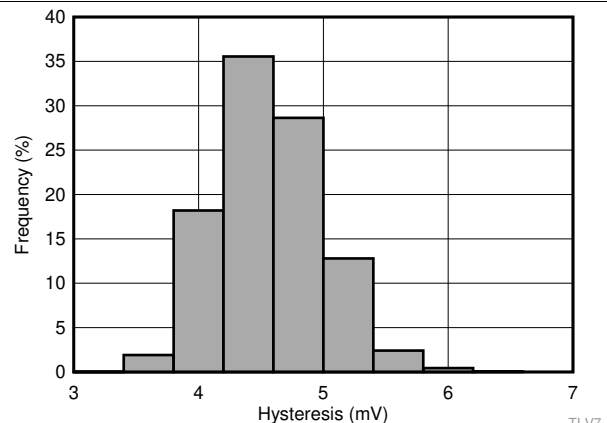
$V_{CC} = 3.3\text{ V}$

Figure 12. Hysteresis vs. V_{CM}



$V_{CC} = 5\text{ V}$

Figure 13. Hysteresis vs. V_{CM}

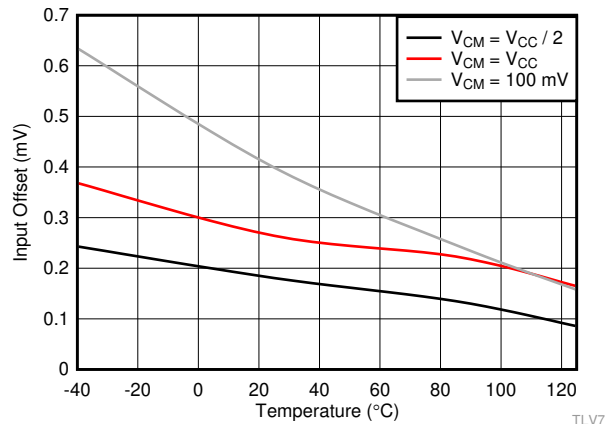


Distribution Taken From 10,777 Comparators

Figure 14. Hysteresis Histogram

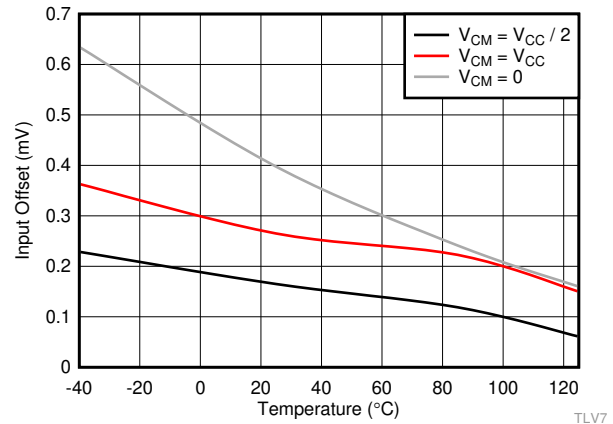
Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$, $V_{EE} = 0\text{ V}$, $V_{CM} = V_{CC}/2$, $C_L = 15\text{ pF}$



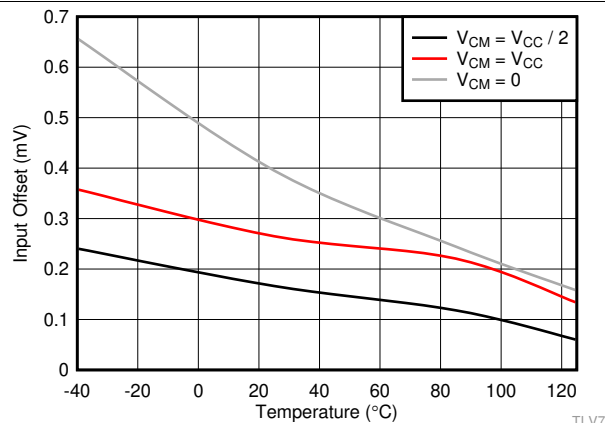
$V_{CC} = 1.8\text{ V}$

FIG 15. Input Offset vs. Temperature



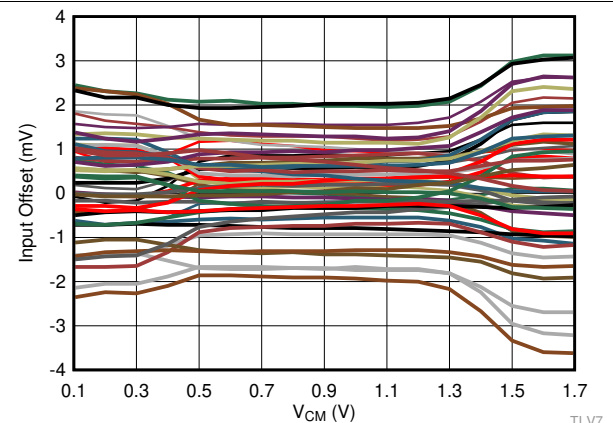
$V_{CC} = 3.3\text{ V}$

FIG 16. Input Offset vs. Temperature



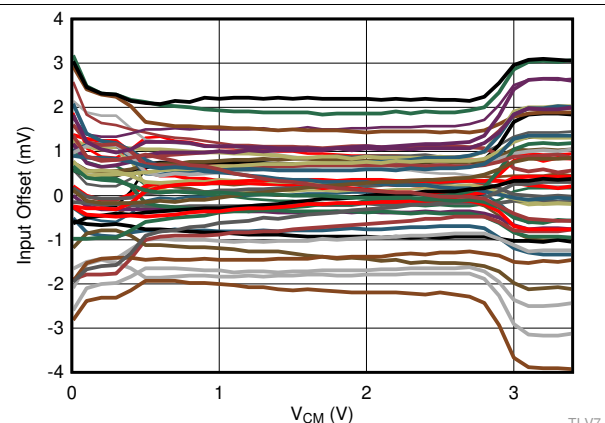
$V_{CC} = 5\text{ V}$

FIG 17. Input Offset vs. Temperature



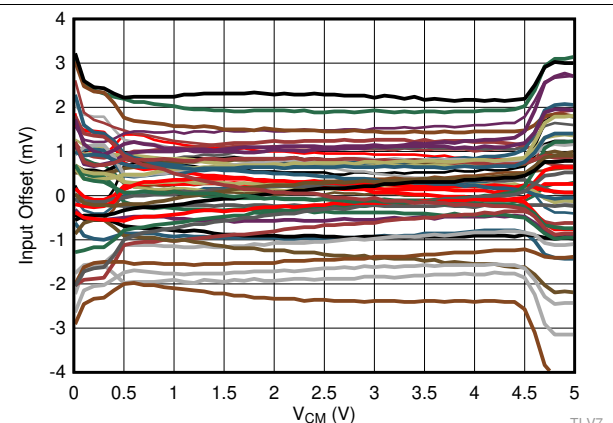
$V_{CC} = 1.8\text{ V}$, 50 devices

FIG 18. Input Offset Voltage vs. V_{CM}



$V_{CC} = 3.3\text{ V}$, 50 devices

FIG 19. Input Offset Voltage vs. V_{CM}

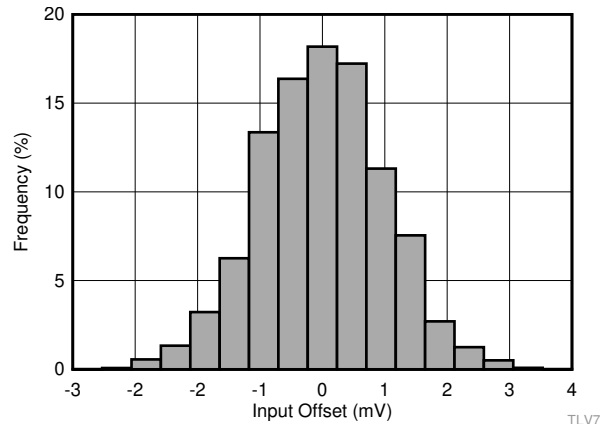


$V_{CC} = 5\text{ V}$, 50 devices

FIG 20. Input Offset Voltage vs. V_{CM}

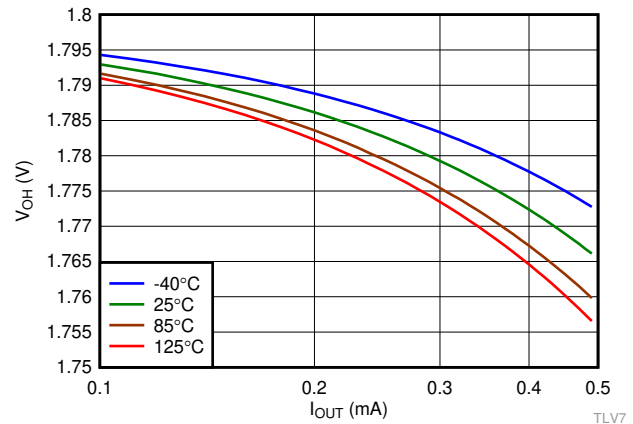
Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$, $V_{EE} = 0\text{ V}$, $V_{CM} = V_{CC}/2$, $C_L = 15\text{ pF}$



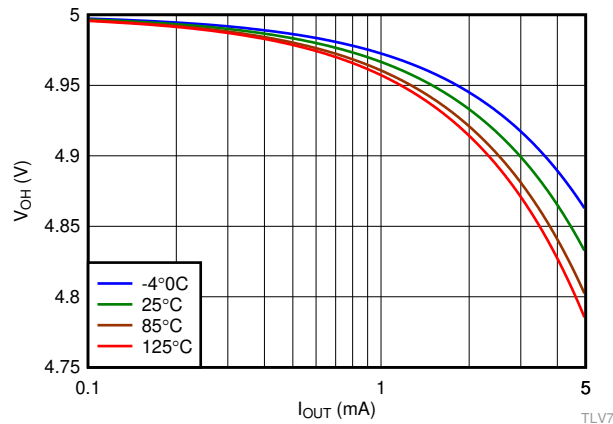
Distribution Taken From 10,777 Comparators

FIG 21. Input Offset Voltage Histogram



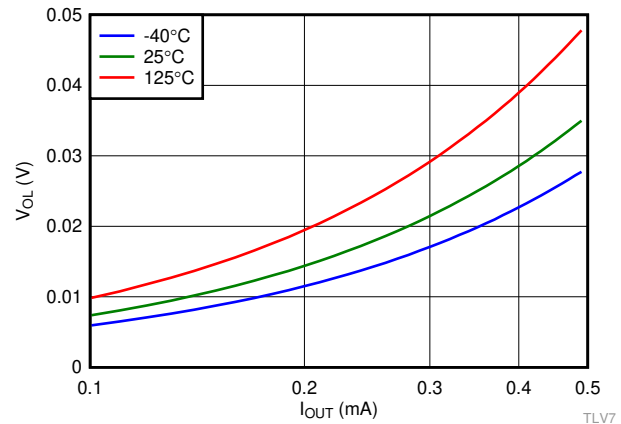
$V_{CC} = 1.8\text{ V}$

FIG 22. TLV7011 Output Voltage High vs. Output Source Current



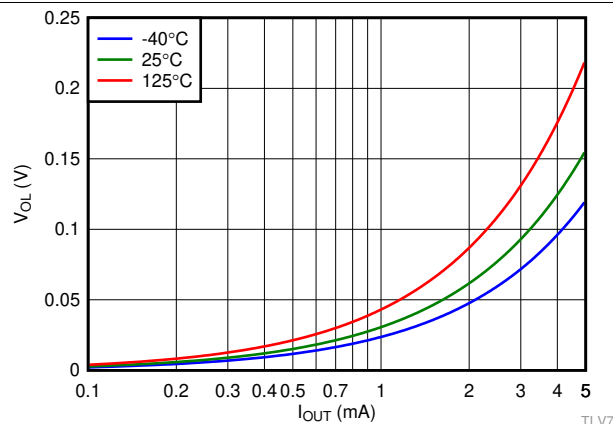
$V_{CC} = 5\text{ V}$

FIG 23. TLV7011 Output Voltage High vs. Output Source Current



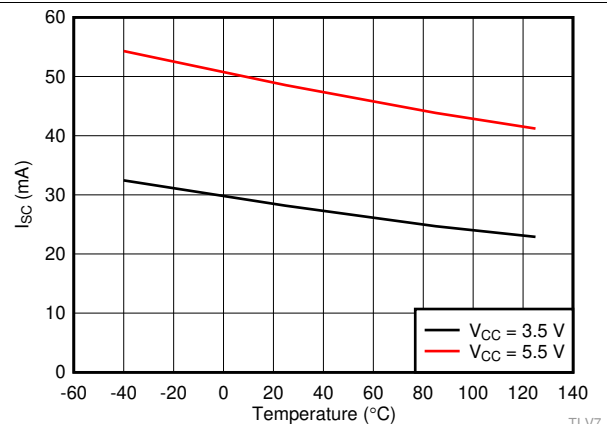
$V_{CC} = 1.8\text{ V}$

FIG 24. Output Voltage Low vs. Output Sink Current



$V_{CC} = 5\text{ V}$

FIG 25. Output Voltage Low vs. Output Sink Current

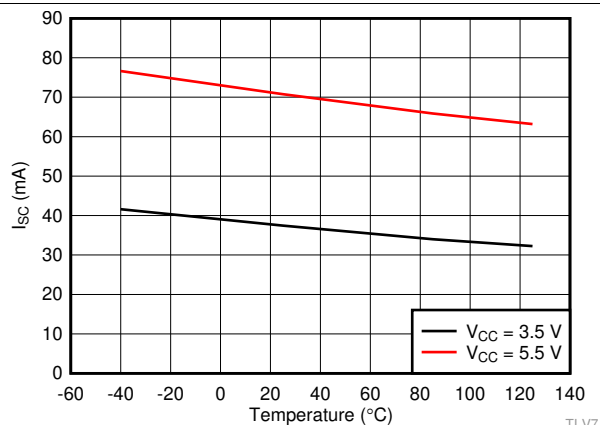


$V_{CM} = V_{CC}/2$

FIG 26. Output Short-Circuit (Sink) Current vs. Temperature

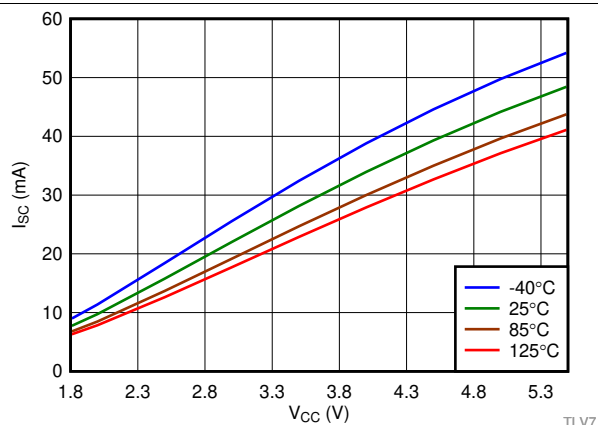
Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$, $V_{EE} = 0\text{ V}$, $V_{CM} = V_{CC}/2$, $C_L = 15\text{ pF}$



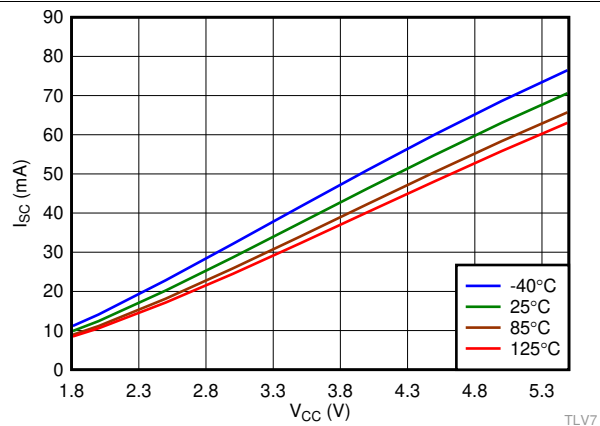
$V_{CM} = V_{CC}/2$

FIG 27. TLV7011 Output Short-Circuit (Source) Current vs. Temperature



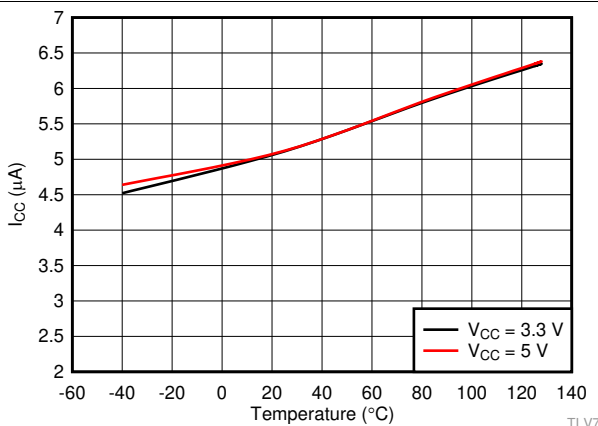
$V_{CM} = V_{CC}/2$

FIG 28. Output Short Circuit (Sink) vs. V_{CC}



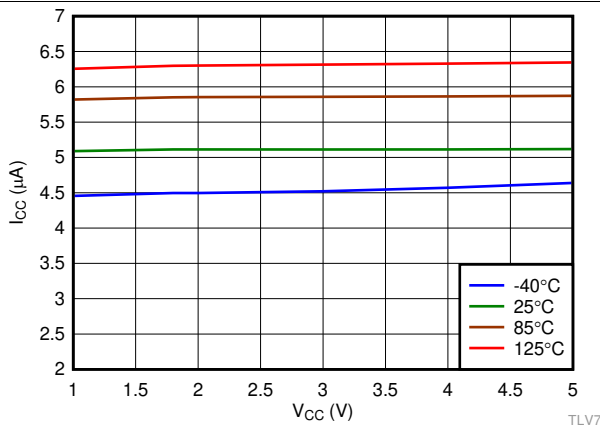
$V_{CM} = V_{CC}/2$

FIG 29. TLV7011 Output Short Circuit (Source) vs. V_{CC}



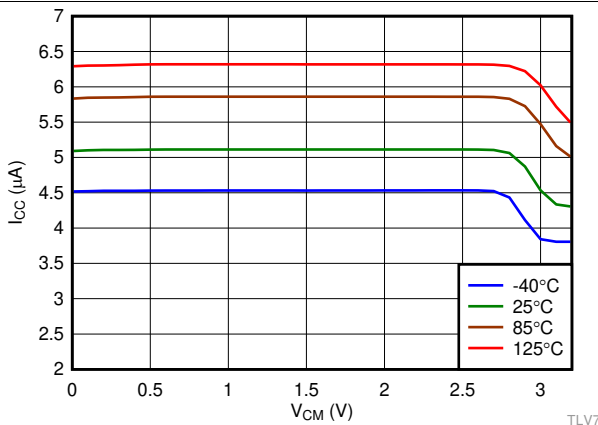
$V_{CM} = V_{CC}/2$

FIG 30. I_{CC} vs. Temperature



$V_{CM} = V_{CC}/2$

FIG 31. I_{CC} vs. V_{CC}

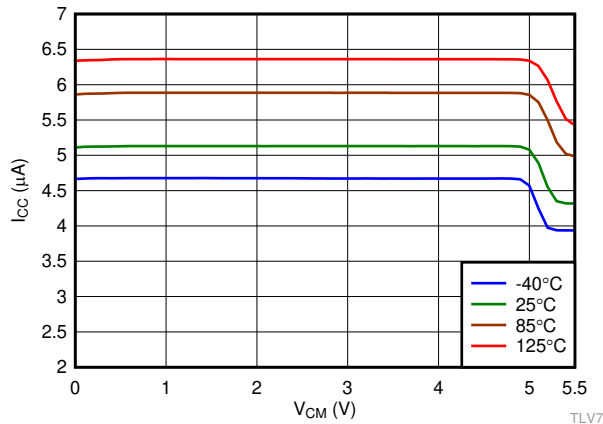


$V_{CC} = 3.3\text{ V}$

FIG 32. I_{CC} vs. V_{CM}

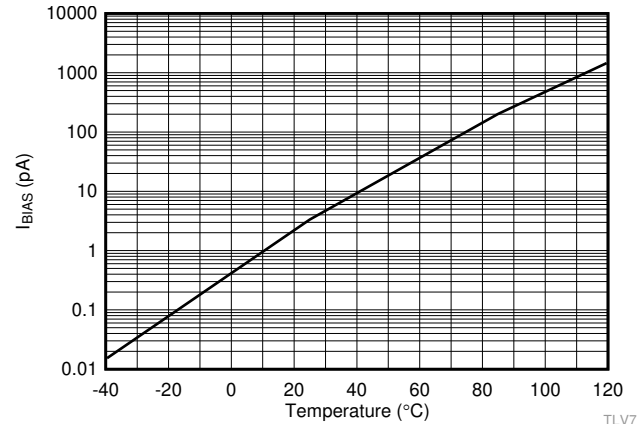
Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$, $V_{EE} = 0\text{ V}$, $V_{CM} = V_{CC}/2$, $C_L = 15\text{ pF}$



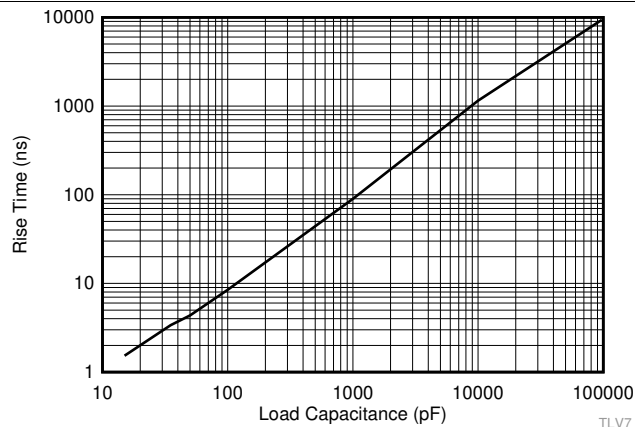
$V_{CC} = 5\text{ V}$

FIG 33. I_{CC} vs. V_{CM}



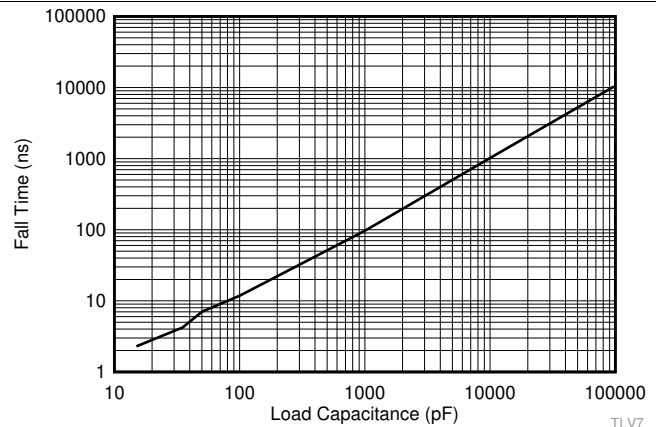
$V_{CC} = 3.3\text{ V}$

FIG 34. Input Bias Current vs. Temperature



$V_{OD} = 100\text{ mV}$

FIG 35. TLV7011 Output Rise Time vs. Load Capacitance



$V_{OD} = 100\text{ mV}$

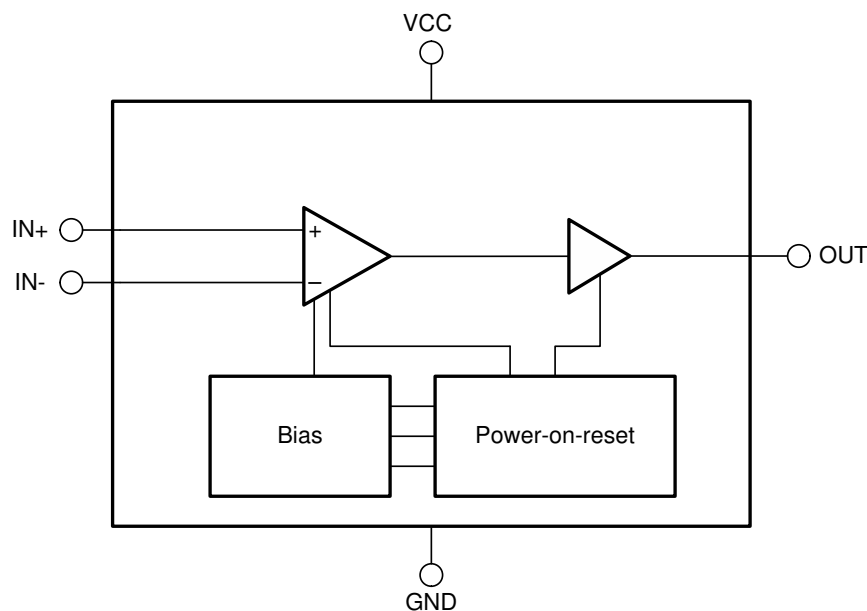
FIG 36. Output Fall Time vs. Load Capacitance

8 Detailed Description

8.1 Overview

The TLV701x and TLV702x devices are single-channel, micro-power comparators with push-pull and open-drain outputs. Operating down to 1.6 V and consuming only 5 μ A, the TLV701x and TLV702x are ideally suited for portable and industrial applications. The comparators are available in leadless and leaded packages to offer significant board space saving in space-challenged designs.

8.2 Functional Block Diagram



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8.3 Feature Description

The TLV701x (push-pull) and TLV702x (open-drain) devices are micro-power comparators that are capable of operating at low voltages. The TLV701x and TLV702x feature a rail-to-rail input stage capable of operating up to 100 mV beyond the VCC power supply rail. The comparators also feature a push-pull and open-drain output stage with internal hysteresis.

8.4 Device Functional Modes

The TLV701x and TLV702x have a Power-on-Reset (POR) circuit. While the power supply (V_S) is ramping up or ramping down, the POR circuitry will be activated.

For the TLV701x, the POR circuit will hold the output low (at V_{EE}) while activated.

For the TLV702x, the POR circuit will keep the output high impedance (logical high) while activated.

When the supply voltage is greater than, or equal to, the minimum supply voltage, the comparator output reflects the state of the differential input (V_{ID}).

8.4.1 Inputs

The TLV701x and TLV702x input common-mode extends from V_{EE} to 100 mV above V_{CC} . The differential input voltage (V_{ID}) can be any voltage within these limits. No phase-inversion of the comparator output will occur when the input pins exceed V_{CC} and V_{EE} .

Device Functional Modes (continued)

While TI recommends operating the TLV701x and TLV702x within the specified common-mode range, the inputs are fault tolerant to voltages up to 5.5 V independent of the applied V_{CC} value. Fault tolerant is defined as maintaining the same high input impedance when V_{CC} is unpowered or within the recommended operating range. Because the inputs of the TLV701x and TLV702x are fault tolerant, the inputs to the comparator can be any value between 0 V and 5.5 V while V_{CC} is ramping up. This feature allows any supply and input driven sequence as long as the input value and supply are within the specified ranges. In this case, no current limiting resistor is required. This is possible since the V_{CC} is isolated from the inputs such that it maintains its value even when a higher voltage is applied to the input.

The input bias current is typically 1 pA for input voltages between V_{CC} and V_{EE} . The comparator inputs are protected from undervoltage by internal diodes connected to V_{EE} . As the input voltage goes under V_{EE} , the protection diodes become forward biased and begin to conduct causing the input bias current to increase exponentially. Input bias current typically doubles for 10°C temperature increases.

8.4.2 Internal Hysteresis

The device hysteresis transfer curve is shown in [Figure 37](#). This curve is a function of three components: V_{TH} , V_{OS} , and V_{HYST} :

- V_{TH} is the actual set voltage or threshold trip voltage.
- V_{OS} is the internal offset voltage between V_{IN+} and V_{IN-} . This voltage is added to V_{TH} to form the actual trip point at which the comparator must respond to change output states.
- V_{HYST} is the internal hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise (4.2 mV for the TLV7011).

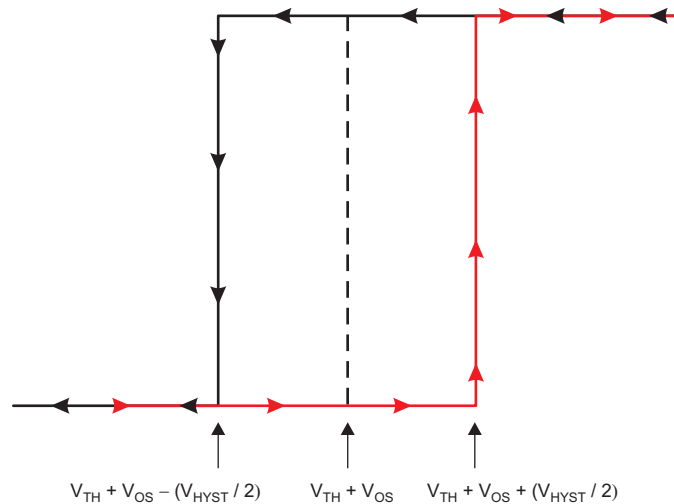


Figure 37. Hysteresis Transfer Curve

8.4.3 Output

The TLV701x feature a push-pull output stage eliminating the need for an external pull-up resistor. On the other hand, the TLV702x feature an open-drain output stage enabling the output logic levels to be pulled up to an external source independent of the supply voltage.

9 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TLV701x and TLV702x are micro-power comparators with reasonable response time. The comparators have a rail-to-rail input stage that can monitor signals beyond the positive supply rail with integrated hysteresis. When higher levels of hysteresis are required, positive feedback can be externally added. The push-pull output stage of the TLV701x is optimal for reduced power budget applications and features no shoot-through current. When level shifting or wire-ORing of the comparator outputs is needed, the TLV702x with its open-drain output stage is well suited to meet the system needs. In either case, the wide operating voltage range, low quiescent current, and micro-package of the TLV701x and TLV702x make these comparators excellent candidates for battery-operated and portable, handheld designs.

9.1.1 Inverting Comparator With Hysteresis for TLV701x

The inverting comparator with hysteresis requires a three-resistor network that is referenced to the comparator supply voltage (V_{CC}), as shown in 図 38. When V_{IN} at the inverting input is less than V_A , the output voltage is high (for simplicity, assume V_O switches as high as V_{CC}). The three network resistors can be represented as $R1 \parallel R3$ in series with $R2$. 式 1 defines the high-to-low trip voltage (V_{A1}).

$$V_{A1} = V_{CC} \times \frac{R2}{(R1 \parallel R3) + R2} \quad (1)$$

When V_{IN} is greater than V_A , the output voltage is low, very close to ground. In this case, the three network resistors can be presented as $R2 \parallel R3$ in series with $R1$. Use 式 2 to define the low to high trip voltage (V_{A2}).

$$V_{A2} = V_{CC} \times \frac{R2 \parallel R3}{R1 + (R2 \parallel R3)} \quad (2)$$

式 3 defines the total hysteresis provided by the network.

$$\Delta V_A = V_{A1} - V_{A2} \quad (3)$$

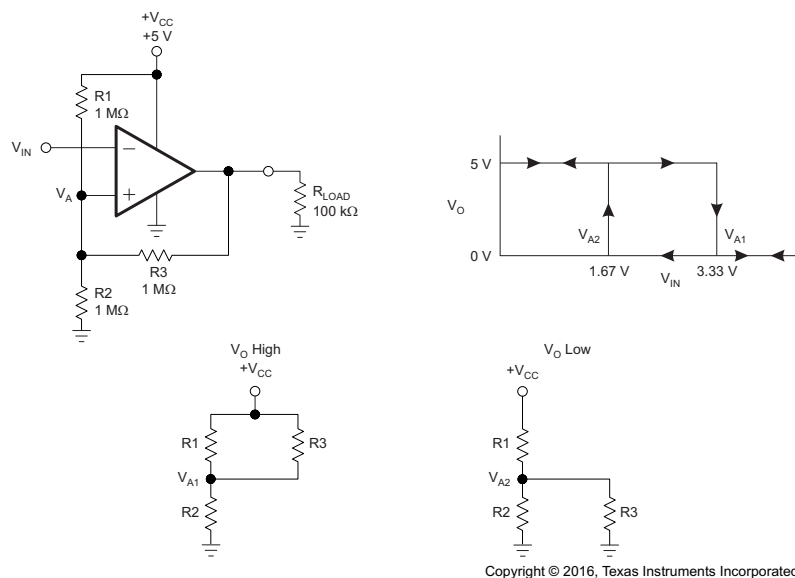


図 38. TLV701x in an Inverting Configuration With Hysteresis

Application Information (continued)

9.1.2 Noninverting Comparator With Hysteresis for TLV701x

A noninverting comparator with hysteresis requires a two-resistor network, as shown in [Figure 39](#), and a voltage reference (V_{REF}) at the inverting input. When V_{IN} is low, the output is also low. For the output to switch from low to high, V_{IN} must rise to V_{IN1} . Use [Equation 4](#) to calculate V_{IN1} .

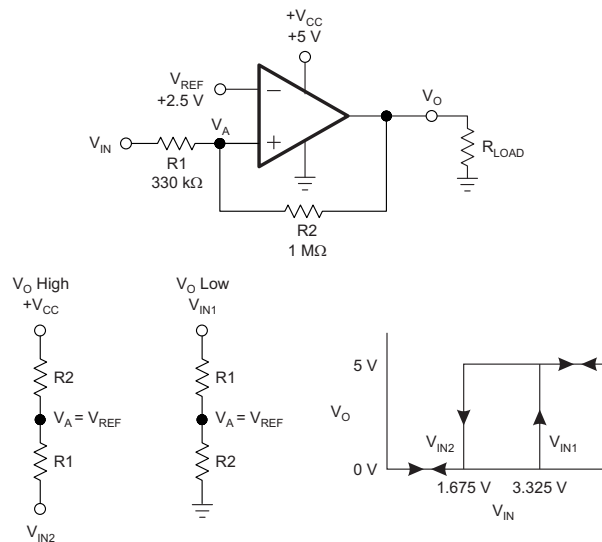
$$V_{IN1} = R1 \times \frac{V_{REF}}{R2} + V_{REF} \quad (4)$$

When V_{IN} is high, the output is also high. For the comparator to switch back to a low state, V_{IN} must drop to V_{IN2} such that V_A is equal to V_{REF} . Use [Equation 5](#) to calculate V_{IN2} .

$$V_{IN2} = \frac{V_{REF} (R1 + R2) - V_{CC} \times R1}{R2} \quad (5)$$

The hysteresis of this circuit is the difference between V_{IN1} and V_{IN2} , as shown in [Equation 6](#).

$$\Delta V_{IN} = V_{CC} \times \frac{R1}{R2} \quad (6)$$



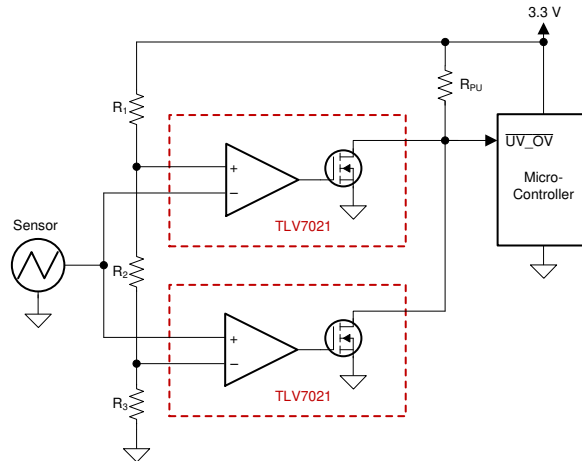
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Figure 39. TLV701x in a Noninverting Configuration With Hysteresis

9.2 Typical Applications

9.2.1 Window Comparator

Window comparators are commonly used to detect undervoltage and overvoltage conditions. [Figure 40](#) shows a simple window comparator circuit.



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Figure 40. Window Comparator

9.2.1.1 Design Requirements

For this design, follow these design requirements:

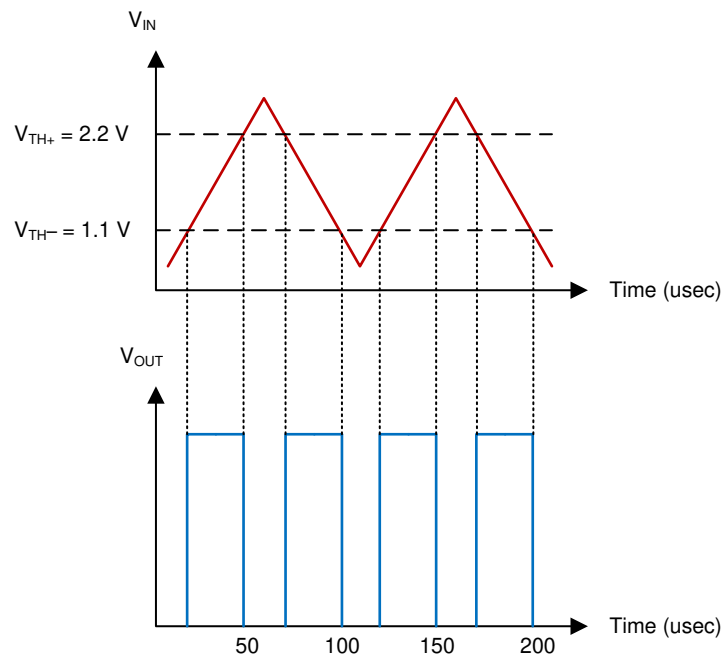
- Alert (logic low output) when an input signal is less than 1.1 V
- Alert (logic low output) when an input signal is greater than 2.2 V
- Alert signal is active low
- Operate from a 3.3-V power supply

9.2.1.2 Detailed Design Procedure

Configure the circuit as shown in [Figure 40](#). Connect V_{CC} to a 3.3-V power supply and V_{EE} to ground. Make R_1 , R_2 and R_3 each 10-M Ω resistors. These three resistors are used to create the positive and negative thresholds for the window comparator (V_{TH+} and V_{TH-}). With each resistor being equal, V_{TH+} is 2.2 V and V_{TH-} is 1.1 V. Large resistor values such as 10-M Ω are used to minimize power consumption. The sensor output voltage is applied to the inverting and noninverting inputs of the two TLV702x's. The TLV7021 is used for its open-drain output configuration. Using the TLV702x allows the two comparator outputs to be Wire-Or'd together. The respective comparator outputs will be low when the sensor is less than 1.1 V or greater than 2.2 V. V_{OUT} will be high when the sensor is in the range of 1.1 V to 2.2 V.

Typical Applications (continued)

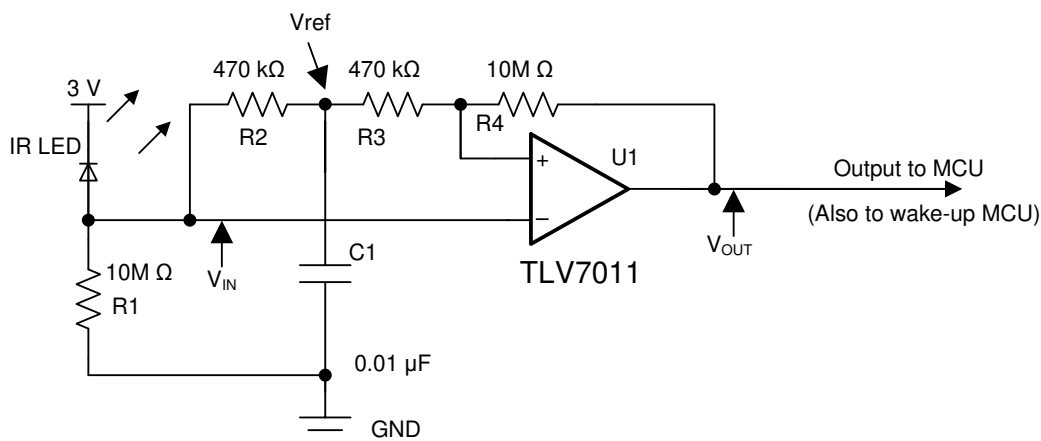
9.2.1.3 Application Curve



✎ 41. Window Comparator Results

9.2.2 IR Receiver Analog Front End

A single TLV7011 device can be used to build a complete IR receiver analog front end (AFE). The nanoamp quiescent current and low input bias current make it possible to be powered with a coin cell battery, which could last for years.



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✎ 42. IR Receiver Analog Front End Using TLV7011

9.2.2.1 Design Requirements

For this design, follow these design requirements:

- Use a proper resistor (R_1) value to generate an adequate signal amplitude applied to the inverting input of the comparator.
- The low input bias current I_B (2 pA typical) ensures that a greater value of R_1 to be used.

Typical Applications (continued)

- The RC constant value (R_2 and C_1) must support the targeted data rate (that is, 9,600 bauds) to maintain a valid tripping threshold.
- The hysteresis introduced with R_3 and R_4 helps to avoid spurious output toggles.

9.2.2.2 Detailed Design Procedure

The IR receiver AFE design is highly streamlined and optimized. R_1 converts the IR light energy induced current into voltage and applies to the inverting input of the comparator. Because a reverse biased IR LED is used as the IR receiver, a higher I/V transimpedance gain is required to boost the amplitude of reduced current. A 10M resistor is used as R_1 to support a 1-V, 100-nA transimpedance gain. This is made possible with the picoamps Input bias current I_B (5pA typical). The RC network of R_2 and C_1 establishes a reference voltage V_{ref} which tracks the mean amplitude of the IR signal. The RC constant of R_2 and C_1 (about 4.7 ms) is chosen for V_{ref} to track the received IR current fluctuation but not the actual data bit stream. The noninverting input is connected to V_{ref} and the output over the R_3 and R_4 resistor network which provides additional hysteresis for improved guard against spurious toggles.

To reduce the current drain from the coin cell battery, data transmission must be short and infrequent.

9.2.2.3 Application Curve

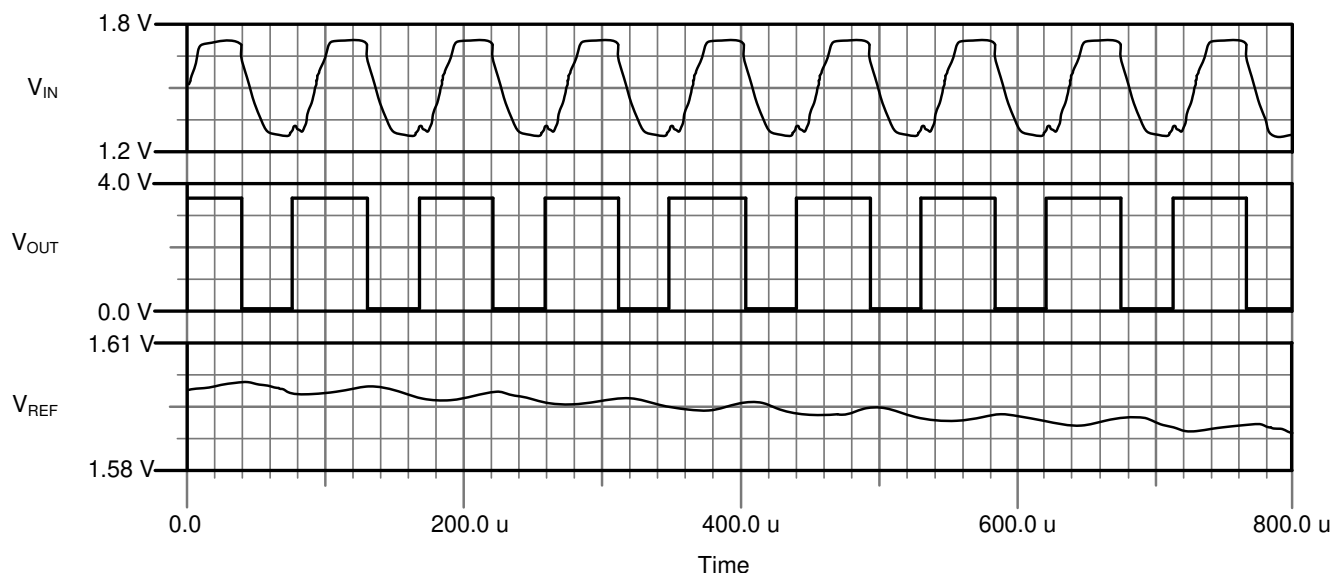


FIG 43. IR Receiver AFE Waveforms

Typical Applications (continued)

9.2.3 Square-Wave Oscillator

Square-wave oscillator can be used as low cost timing reference or system supervisory clock source.

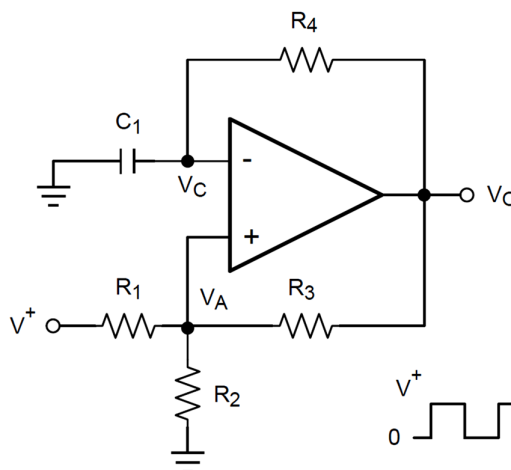


Figure 44. Square-Wave Oscillator

9.2.3.1 Design Requirements

The square-wave period is determined by the RC time constant of the capacitor and resistor. The maximum frequency is limited by propagation delay of the device and the capacitance load at the output. The low input bias current allows a lower capacitor value and larger resistor value combination for a given oscillator frequency, which may help to reduce BOM cost and board space.

9.2.3.2 Detailed Design Procedure

The oscillation frequency is determined by the resistor and capacitor values. The following calculation provides details of the steps.

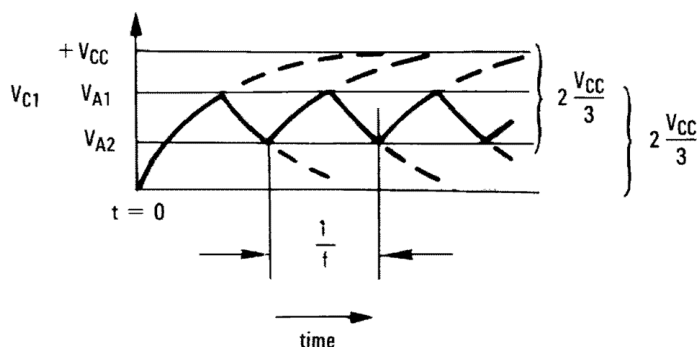


Figure 45. Square-Wave Oscillator Timing Thresholds

First consider the output of Figure 44 is high which indicates the inverted input V_C is lower than the noninverting input (V_A). This causes the C_1 to be charged through R_4 , and the voltage V_C increases until it is equal to the noninverting input. The value of V_A at the point is calculated by 式 7.

$$V_{A1} = \frac{V_{CC} \times R_2}{R_2 + R_1 + R_3} \quad (7)$$

if $R_1 = R_2 = R_3$, then $V_{A1} = 2 V_{CC} / 3$

Typical Applications (continued)

At this time the comparator output trips pulling down the output to the negative rail. The value of V_A at this point is calculated by 式 8.

$$V_{A2} = \frac{V_{CC}(R_2 \parallel R_3)}{R_1 + R_2 \parallel R_3} \quad (8)$$

if $R_1 = R_2 = R_3$, then $V_{A2} = V_{CC}/3$

The C_1 now discharges through the R_4 , and the voltage V_{CC} decreases until it reaches V_{A2} . At this point, the output switches back to the starting state. The oscillation period equals to the time duration from for C_1 from $2V_{CC}/3$ to $V_{CC}/3$ then back to $2V_{CC}/3$, which is given by $R_4 C_1 \times \ln 2$ for each trip. Therefore, the total time duration is calculated as $2 R_4 C_1 \times \ln 2$. The oscillation frequency can be obtained by 式 9:

$$f = 1 / (2 R_4 \times C_1 \times \ln 2) \quad (9)$$

9.2.3.3 Application Curve

Figure 46 shows the simulated results of tan oscillator using the following component values:

- $R_1 = R_2 = R_3 = R_4 = 100 \text{ k}\Omega$
- $C_1 = 100 \text{ pF}$, $C_L = 20 \text{ pF}$
- $V_+ = 5 \text{ V}$, $V_- = \text{GND}$
- C_{stray} (not shown) from V_A TO GND = 10 pF

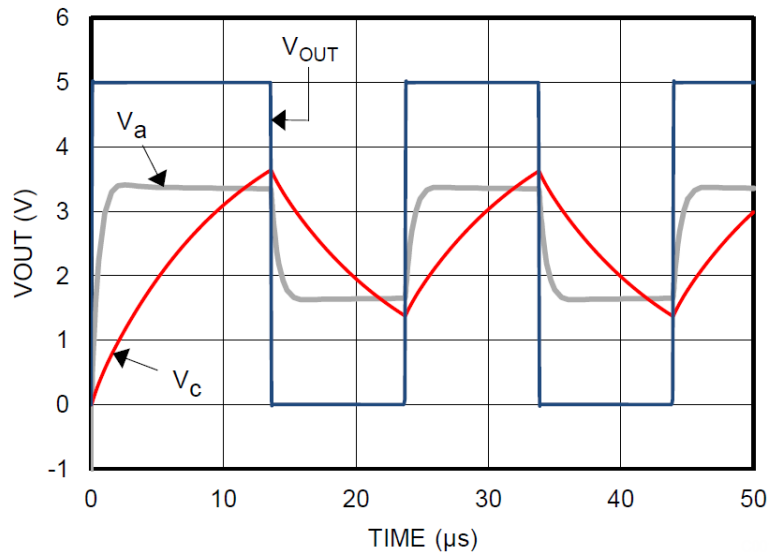


Figure 46. Square-Wave Oscillator Output Waveform

10 Power Supply Recommendations

The TLV701x and TLV702x have a recommended operating voltage range (V_S) of 1.6 V to 5.5 / 6.5 V. V_S is defined as $V_{CC} - V_{EE}$. Therefore, the supply voltages used to create V_S can be single-ended or bipolar. For example, single-ended supply voltages of 5 V and 0 V and bipolar supply voltages of +2.5 V and –2.5 V create comparable operating voltages for V_S . However, when bipolar supply voltages are used, it is important to realize that the logic low level of the comparator output is referenced to V_{EE} .

Output capacitive loading and output toggle rate will cause the average supply current to rise over the quiescent current.

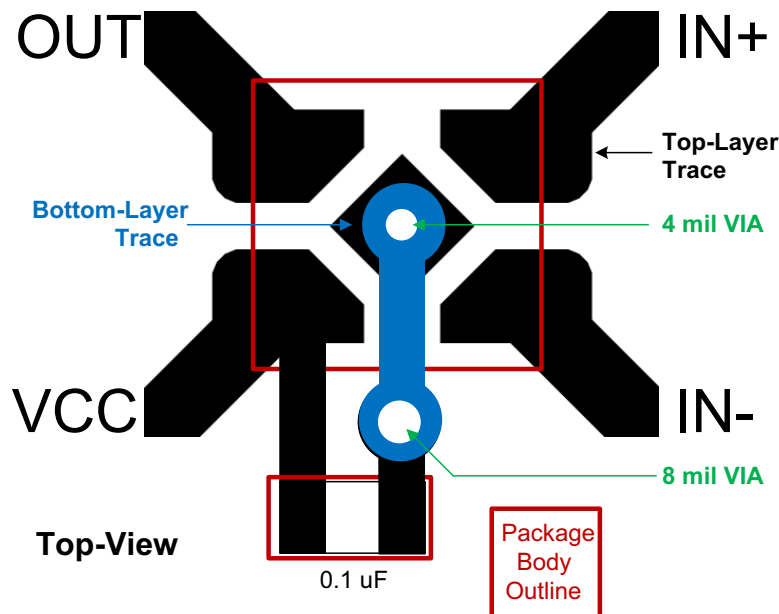
11 Layout

11.1 Layout Guidelines

To reduce PCB fabrication cost and improve reliability, TI recommends using a 4-mil via at the center pad connected to the ground trace or plane on the bottom layer.

A power-supply bypass capacitor of 100 nF is recommended when supply output impedance is high, supply traces are long, or when excessive noise is expected on the supply lines. Bypass capacitors are also recommended when the comparator output drives a long trace or is required to drive a capacitive load. Due to the fast rising and falling edge rates and high-output sink and source capability of the TLV7011 and TLV7021 output stages, higher than normal quiescent current can be drawn from the power supply. Under this circumstance, the system would benefit from a bypass capacitor across the supply pins.

11.2 Layout Example



✎ 47. Layout Example

12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 開発サポート

12.1.1.1 評価基板

TLV70x1デバイス・ファミリーを使用する回路の初期性能評価に役立てるため、評価基板(EVM)を利用可能です。[TLV7011 Micro-PowerコンパレータDIPアダプタ評価基板](#)は、テキサス・インスツルメンツWebサイトの製品フォルダで請求でき、TI eStoreから直接お求めにもなれます。

12.2 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 1. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
TLV7011	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TLV7021	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

12.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](#)のデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.4 コミュニティ・リソース

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

12.5 商標

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

12.6 静電気放電に関する注意事項



すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

12.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV7011DBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU SN NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	11C2
TLV7011DBVR.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	11C2
TLV7011DBVR.B	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	11C2
TLV7011DCKR	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19N
TLV7011DCKR.A	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19N
TLV7011DCKR.B	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19N
TLV7011DCKT	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19N
TLV7011DCKT.A	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19N
TLV7011DCKT.B	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19N
TLV7011DCKTG4	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19N
TLV7011DCKTG4.A	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19N
TLV7011DCKTG4.B	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19N
TLV7011DPWR	Active	Production	X2SON (DPW) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7N
TLV7011DPWR.A	Active	Production	X2SON (DPW) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7N
TLV7011DPWR.B	Active	Production	X2SON (DPW) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7N
TLV7012DDFR	Active	Production	SOT-23-THIN (DDF) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7012
TLV7012DDFR.A	Active	Production	SOT-23-THIN (DDF) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7012
TLV7012DGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU SN NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	7012
TLV7012DGKR.A	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7012
TLV7012DGKRG4	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7012
TLV7012DGKRG4.A	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7012
TLV7012DSGR	Active	Production	WSON (DSG) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7012
TLV7012DSGR.A	Active	Production	WSON (DSG) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7012
TLV7021DBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU SN NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	11D2
TLV7021DBVR.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	11D2
TLV7021DBVR.B	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	11D2
TLV7021DCKR	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-2-260C-1 YEAR	-40 to 125	19O

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV7021DCKR.A	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	19O
TLV7021DCKR.B	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	19O
TLV7021DCKT	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU SN	Level-2-260C-1 YEAR	-40 to 125	19O
TLV7021DCKT.A	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19O
TLV7021DCKT.B	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19O
TLV7021DPWR	Active	Production	X2SON (DPW) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7P
TLV7021DPWR.A	Active	Production	X2SON (DPW) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7P
TLV7021DPWR.B	Active	Production	X2SON (DPW) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7P
TLV7022DDFR	Active	Production	SOT-23-THIN (DDF) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7022
TLV7022DDFR.A	Active	Production	SOT-23-THIN (DDF) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7022
TLV7022DGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU SN NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	7022
TLV7022DGKR.A	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7022
TLV7022DSGR	Active	Production	WSON (DSG) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7022
TLV7022DSGR.A	Active	Production	WSON (DSG) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7022

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

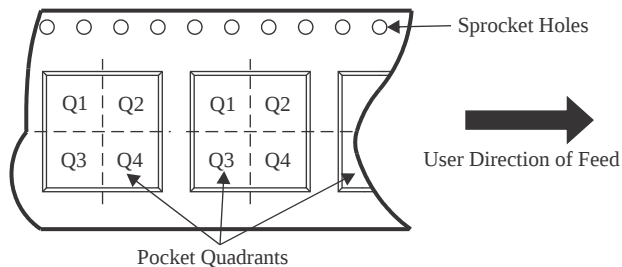
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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV7011DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV7011DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV7011DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV7011DCKTG4	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV7011DPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q2
TLV7012DDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV7012DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV7012DGKRG4	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV7012DSGR	WSO	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV7021DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV7021DCKR	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
TLV7021DCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
TLV7021DCKT	SC70	DCK	5	250	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
TLV7021DPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q2
TLV7022DDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV7022DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV7022DSGR	WSO8	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

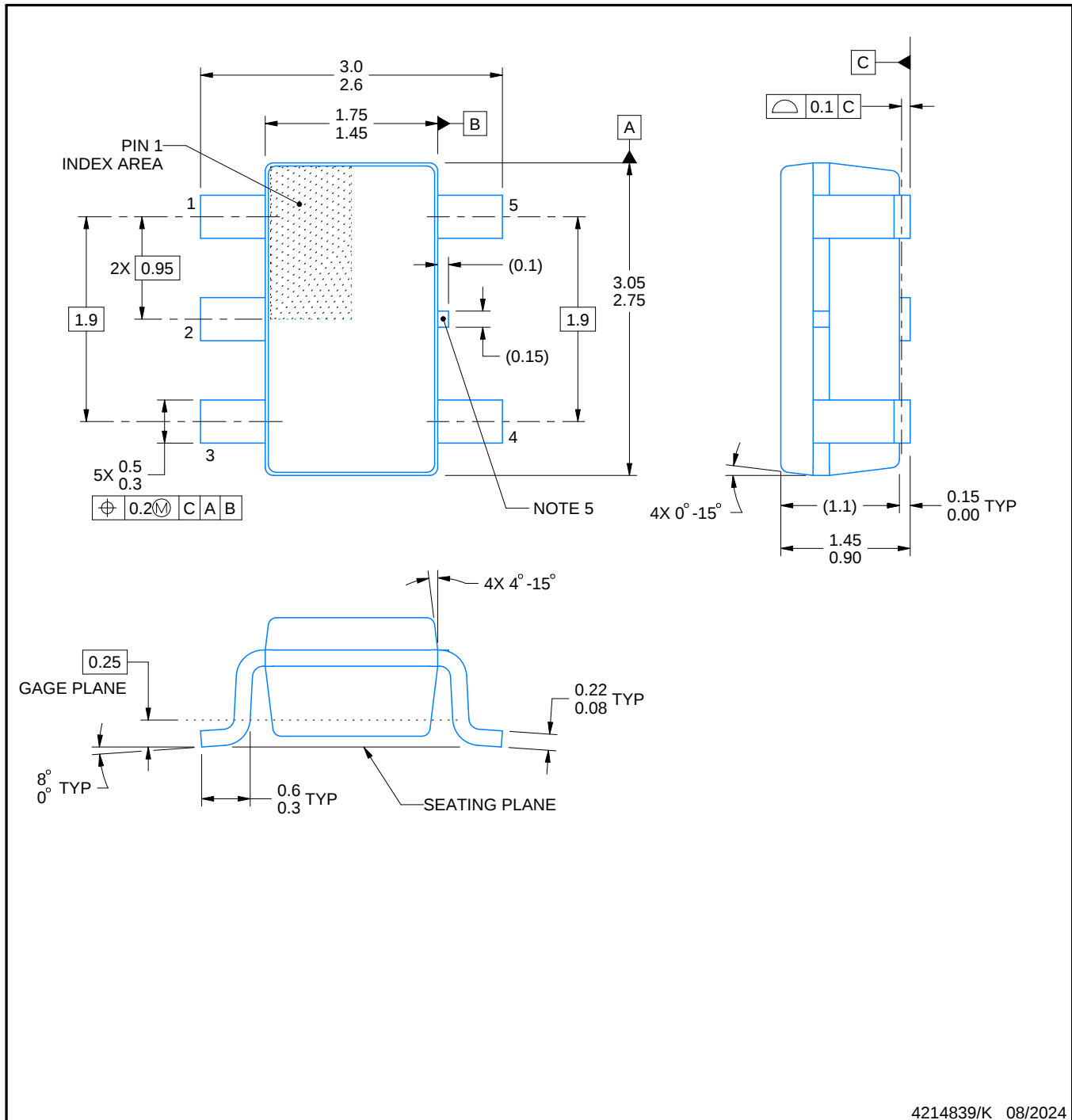


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV7011DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
TLV7011DCKR	SC70	DCK	5	3000	190.0	190.0	30.0
TLV7011DCKT	SC70	DCK	5	250	190.0	190.0	30.0
TLV7011DCKTG4	SC70	DCK	5	250	190.0	190.0	30.0
TLV7011DPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
TLV7012DDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TLV7012DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
TLV7012DGKRG4	VSSOP	DGK	8	2500	353.0	353.0	32.0
TLV7012DSGR	WSO	DSG	8	3000	210.0	185.0	35.0
TLV7021DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
TLV7021DCKR	SC70	DCK	5	3000	210.0	185.0	35.0
TLV7021DCKR	SC70	DCK	5	3000	210.0	185.0	35.0
TLV7021DCKT	SC70	DCK	5	250	210.0	185.0	35.0
TLV7021DPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
TLV7022DDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TLV7022DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
TLV7022DSGR	WSO	DSG	8	3000	210.0	185.0	35.0

DBV0005A**PACKAGE OUTLINE****SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR



4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



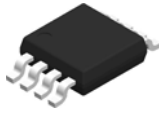
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK0008A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

NOTES:

PowerPAD is a trademark of Texas Instruments.

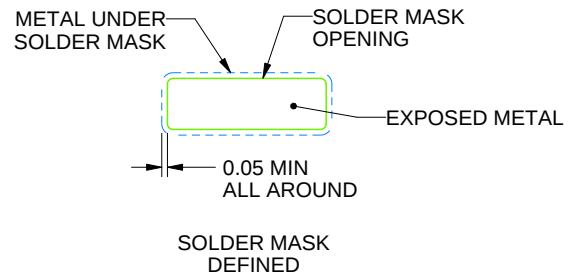
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DPW 5

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

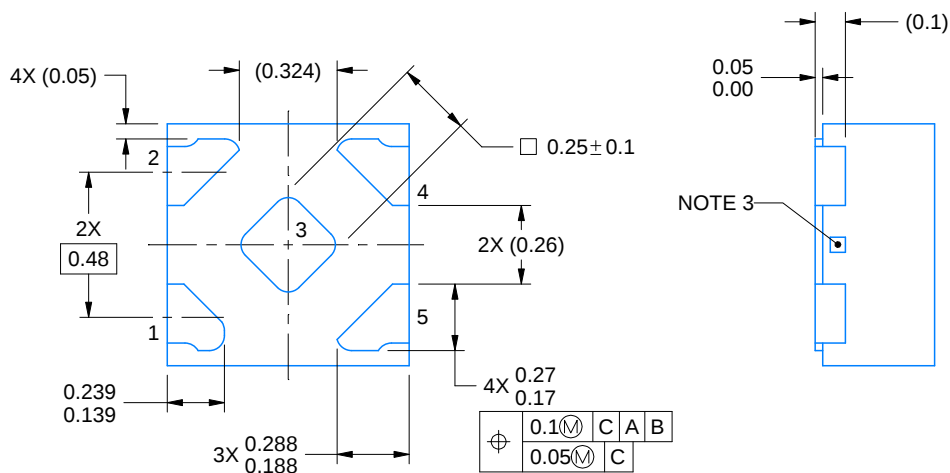
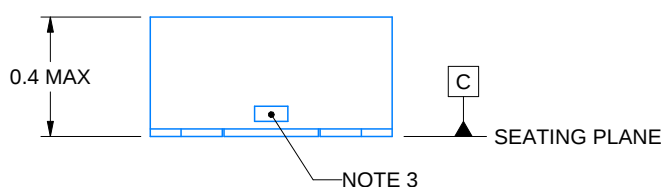
4211218-3/D



X2SON - 0.4 mm max height

Diagram illustrating the dimensions and pin index area of a component:

- The component is a rectangle with a width of 0.85 and a height of 0.75.
- A shaded rectangular area in the top-left corner is labeled "PIN 1 INDEX AREA".
- Dimension lines indicate the overall width (0.85) and height (0.75) of the component.
- Reference points A and B are marked at the top corners of the component.



NOTES:

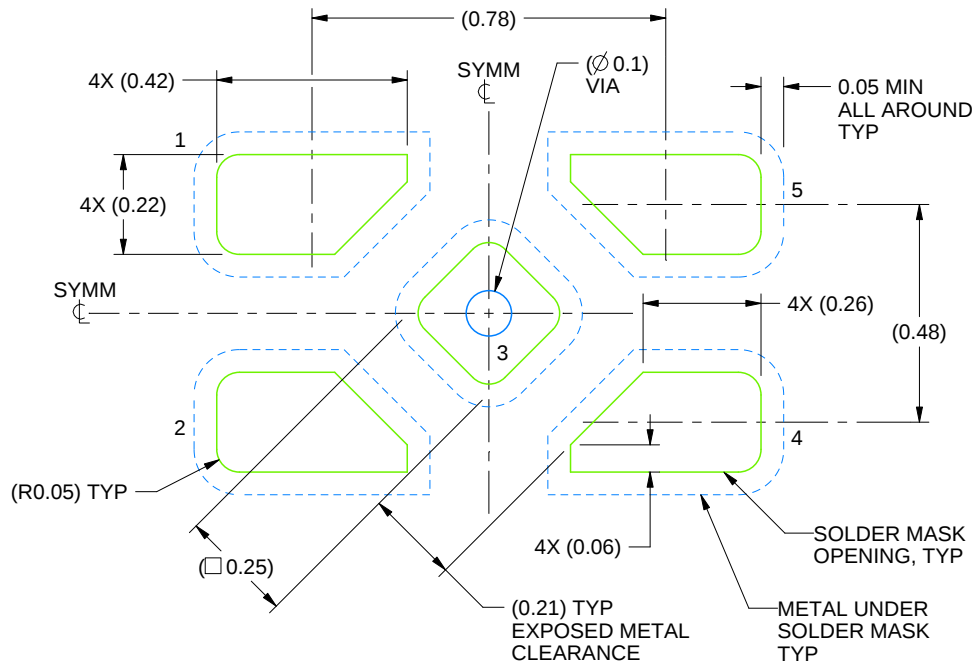
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.

EXAMPLE BOARD LAYOUT

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4223102/D 03/2022

NOTES: (continued)

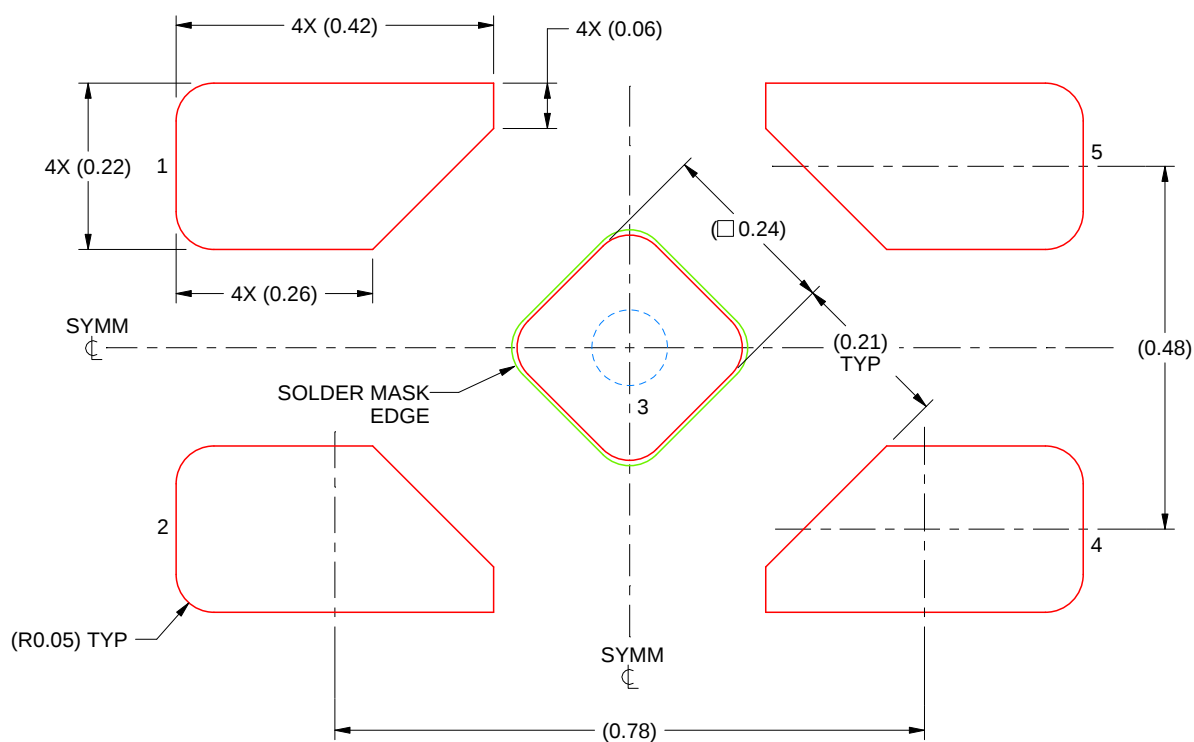
4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/sluea271).

EXAMPLE STENCIL DESIGN

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 3
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:100X

4223102/D 03/2022

NOTES: (continued)

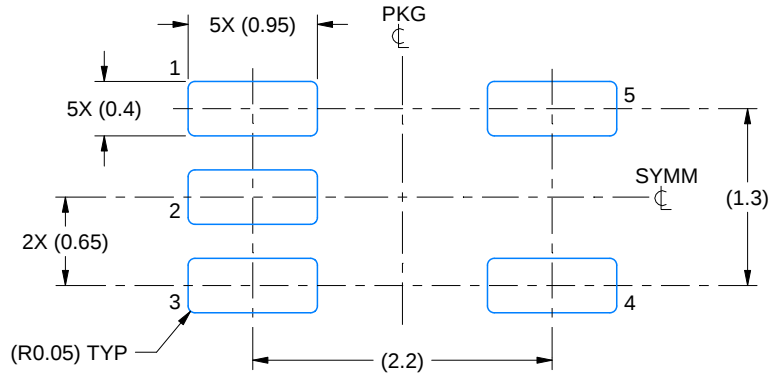
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



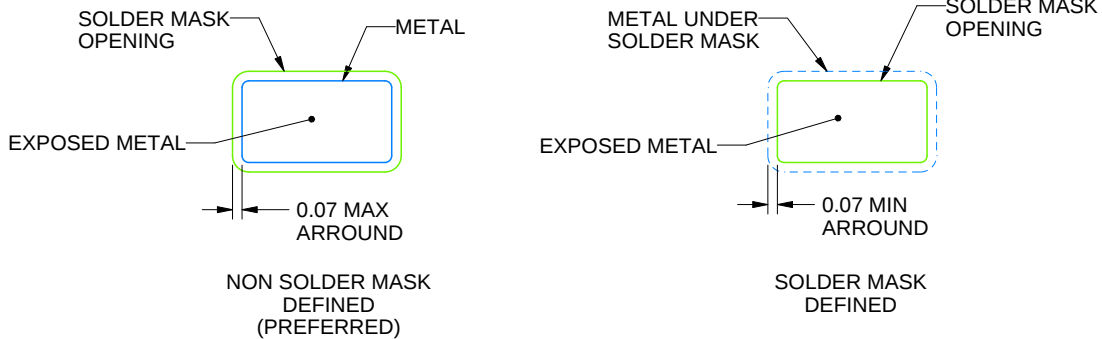
SOT - 1.1 max height

[illegible]

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4214834/G 11/2024

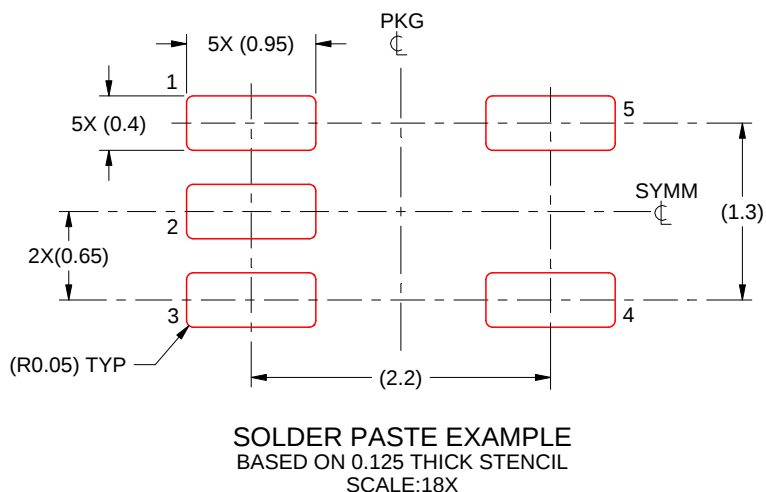
NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

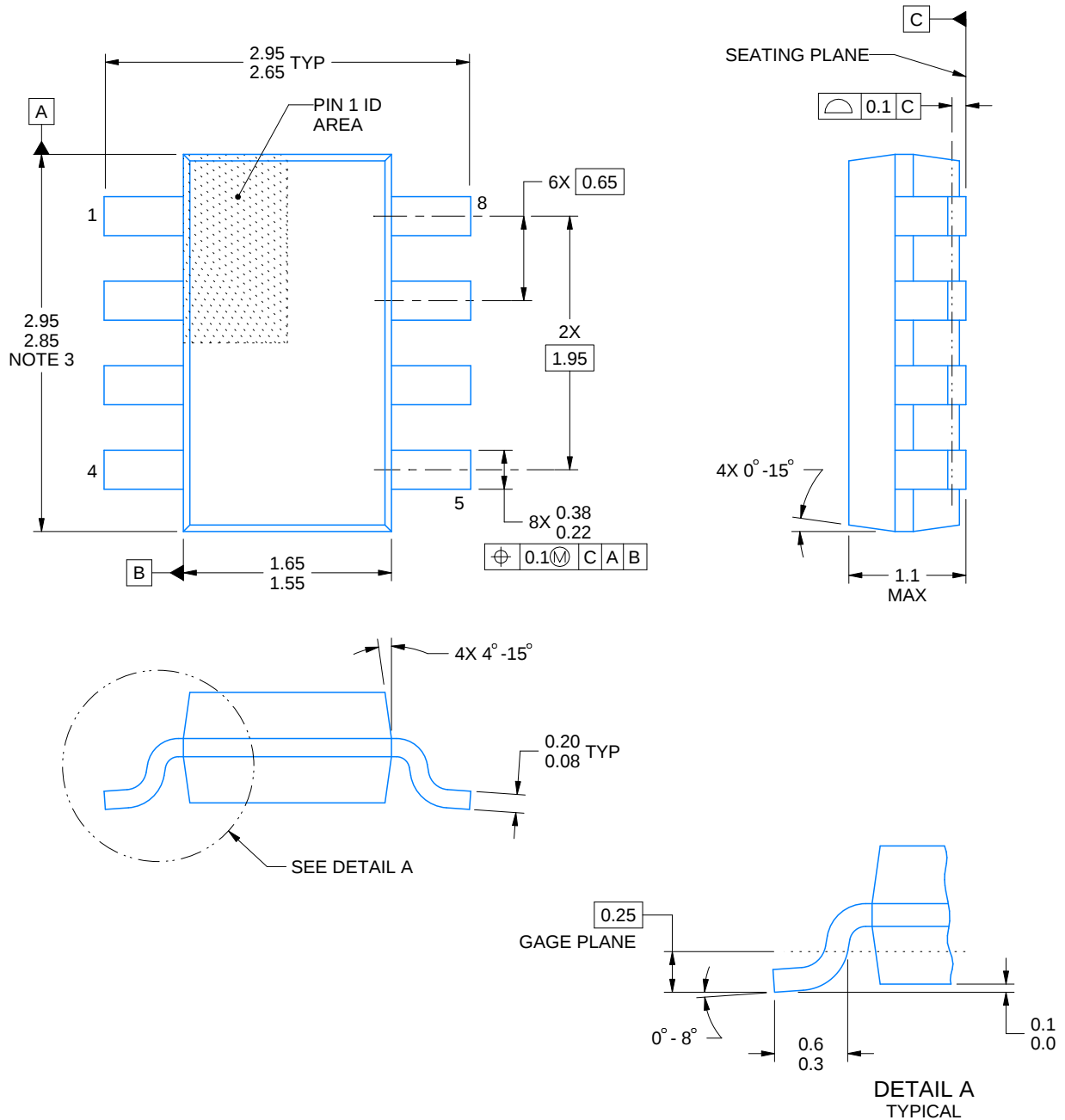
DDF0008A



PACKAGE OUTLINE

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



4222047/E 07/2024

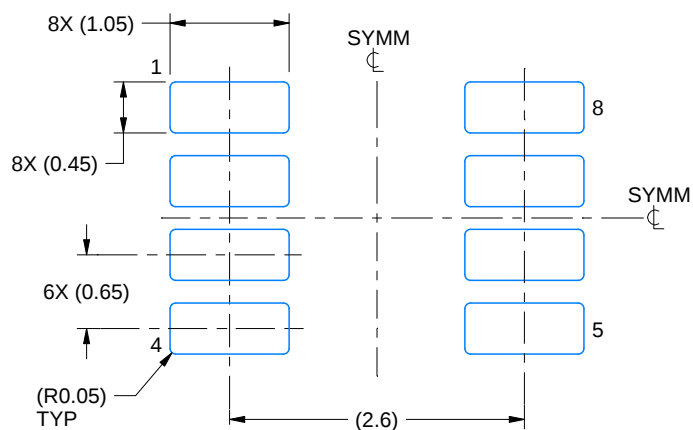
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

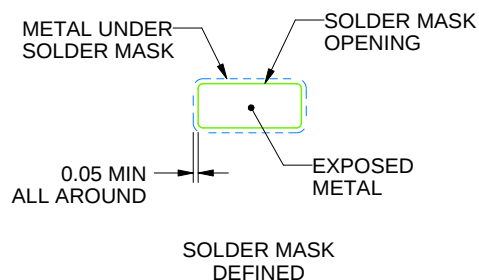
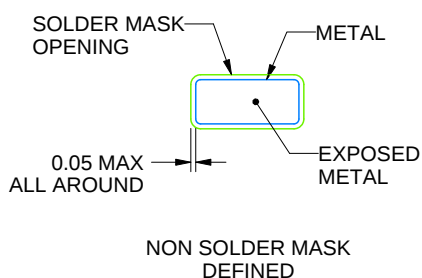
DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4222047/E 07/2024

NOTES: (continued)

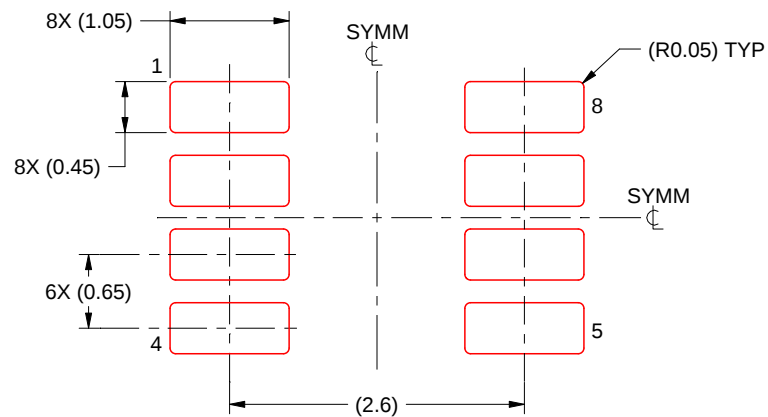
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

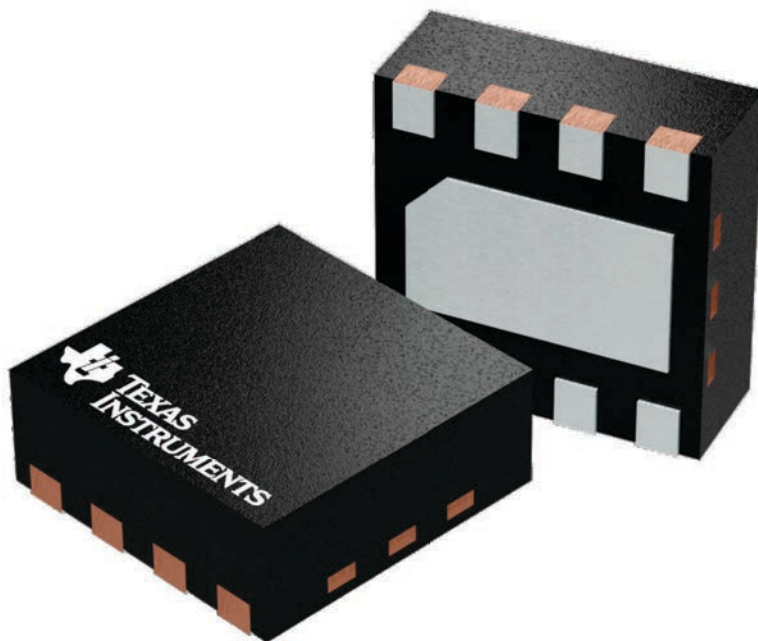
DSG 8

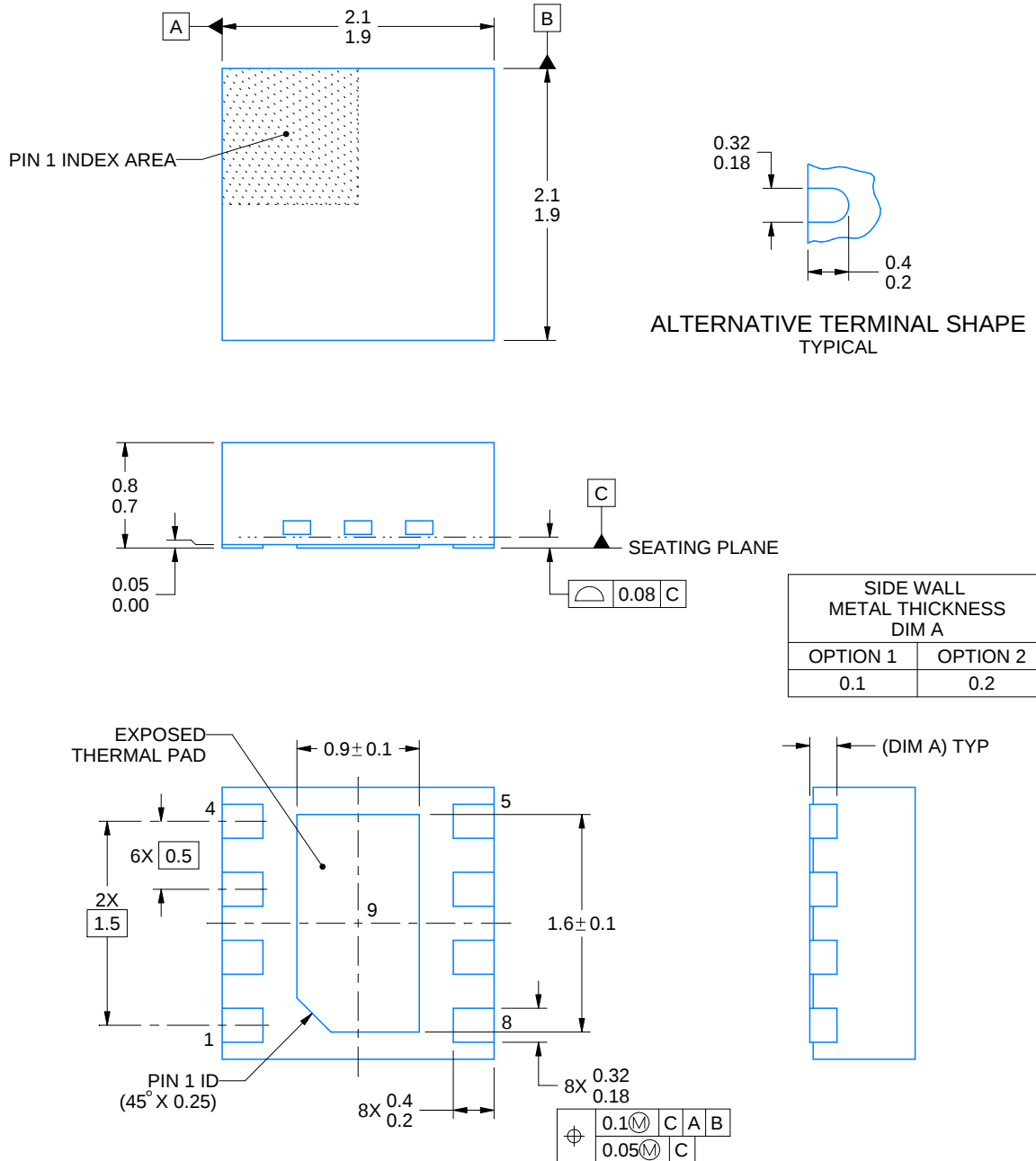
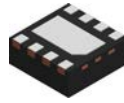
WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.





4218900/E 08/2022

NOTES:

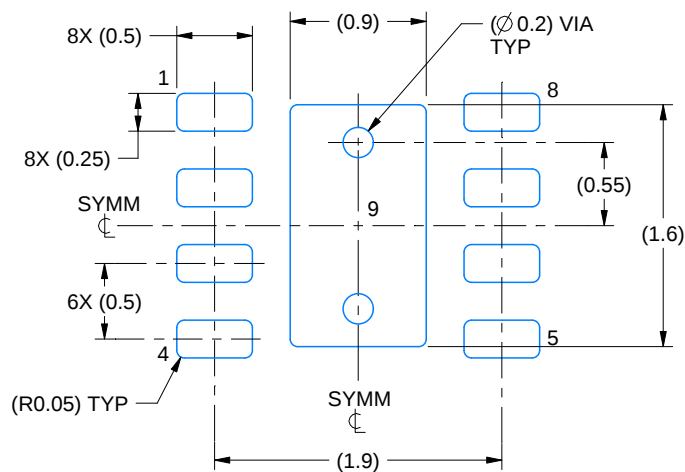
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

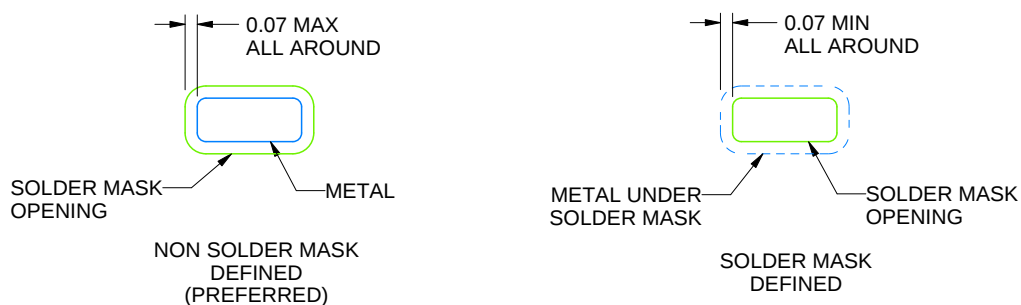
DSG0008A

WSN - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4218900/E 08/2022

NOTES: (continued)

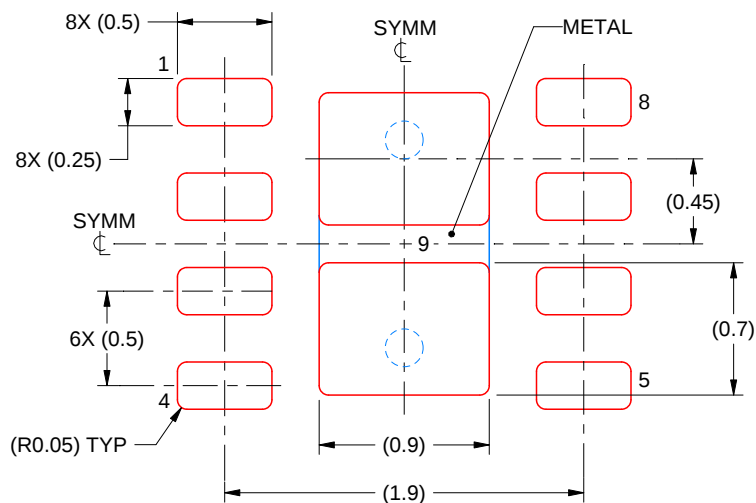
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slue271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DSG0008A

WSN - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/E 08/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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