TLV700xx-Q1 車載用 200mA、低 I_Q、ポータブル デバイス向け低ドロップアウト レギュレータ

1 特長

- 車載アプリケーション用に AEC-Q100 認定済み:
  - 温度グレード 1:-40℃～125℃、T_A
  - デバイス HBM ESD 分類レベル H2
  - デバイス CDM ESD 分類レベル C4B
- 2% 精度
- 低 I_Q:31µA
- 1.9V～4.8V の固定出力電圧の組み合わせが可能
- 高 PSRR:1kHz 時に 68dB
- 実効容量 0.1µF で安定
- サーマル シャットダウン機能と過電流保護機能
- AEC-Q100 レベル I に準拠した 100mA 超のラッチアップ性能
- SOT-23-5、SC70 の各パッケージで提供

2 アプリケーション

- 車載用カメラ モジュール
- イメージセンサ電源
- マイクロプロセッサ用レール
- 車載用インフォテイメントのヘッド ユニット
- 車載用ボディエレクトロニクス

3 概要

TLV700xx-Q1 ファミリの低ドロップアウト(LDO)リニア レギュレータは、低静止電流のデバイスで、ラインおよび負荷の過渡性能が非常に優れています。これらの LDO は、消費電力の制限が厳しいアプリケーション向けに設計されています。高精度のバンドギャップおよびエラー アンプにより、総合で 2%精度を実現しています。低出力ノイズ、非常に高い電源電圧変動除去比 (PSRR)、低ドロップアウト電圧を特長とする本シリーズのデバイスは、バッテリ駆動式の携帯機器向けに設計されています。どのバージョンのデバイスも、安全のためにサーマル シャットダウン機能と電流制限機能を搭載しています。

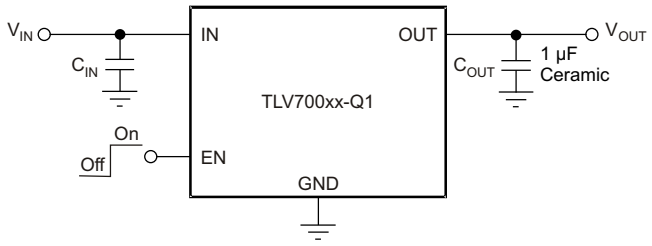
さらに、これらのデバイスはわずか 0.1µF の実効出力容量で安定します。この機能により、バイアス電圧および温度ディレーティングの高い、コスト効率の優れたコンデンサを使用できます。これらのデバイスは、出力負荷なしでも指定の精度へのレギュレーションを行います。

TLV700xx-Q1 LDO は、SOT-23-5 および SC70 パッケージで供給されます。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
TLV700xx-Q1	DCK (SC70、5)	2mm × 2.1mm
	DDC (SOT、5)	2.9mm × 2.8mm

(1) 詳細については、*メカニカル、パッケージ、および注文情報*を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



代表的なアプリケーションの回路 (固定電圧バージョン)

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4 Pin Configuration and Functions

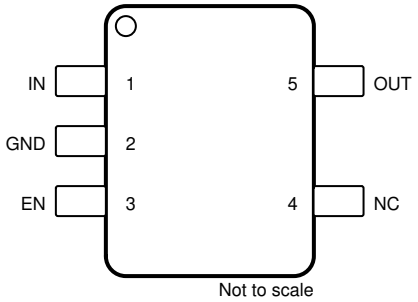


図 4-1. DDC and DCK Packages, 5-Pin SOT (Top View)

表 4-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	SC70	SOT		
EN	3	3	I	Enable pin. Driving EN over 0.9V turns on the regulator. Driving EN below 0.4V puts the regulator into shutdown mode and reduces operating current to 1µA, nominal.
GND	2	2	—	Ground pin
IN	1	1	I	Input pin. A small 1µF ceramic capacitor is recommended from this pin to ground to provide stability and good transient performance. See the *Input and Output Capacitor Requirements* section for more details.
NC	4	4	—	No connection. This pin can be tied to ground to improve thermal dissipation.
OUT	5	5	O	Regulated output voltage pin. A small 1µF ceramic capacitor is needed from this pin to ground to provide stability. See the *Input and Output Capacitor Requirements* section for more details.

5 Specifications

5.1 Absolute Maximum Ratings

at T_A = –40°C to +125°C (unless otherwise noted); all voltages are with respect to GND(1)

		MIN	MAX	UNIT
V_{IN}	Input voltage	–0.3	6	V
V_{EN}	Enable voltage	–0.3	V_{IN} + 0.3	V
V_{OUT}	Output voltage	–0.3	6	V
I_{OUT}	Maximum output current	Internally limited		
	Output short-circuit duration	Indefinite		
T_A	Operating ambient temperature	–40	150	°C
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2		5.5	V
V_{EN}	Enable voltage	0		5.5	V
I_{OUT}	Output current		200		mA
C_{IN}	Input capacitor	0	1		µF
C_{OUT}	Output capacitor	0.22	1		µF
T_A	Operating ambient temperature	–40		125	°C

5.4 Thermal Information

THERMAL METRIC(1)		TLV700xx-Q1 DDC (SOT) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	262.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	68.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	81.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	80.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

at T_A = –40°C to +125°C, V_{IN} = $V_{OUT(TYP)}$ + 0.3V or 2V (whichever is greater), I_{OUT} = 10mA, V_{EN} = V_{IN}, and C_{OUT} = 1µF (unless otherwise noted); typical values are at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		2		5.5	V
V_{OUT}	DC output accuracy	–40°C ≤ T_A ≤ +125°C, V_{OUT} ≥ 1V	–2%		2%	
$\Delta V_O/\Delta V_{IN}$	Line regulation	$V_{OUT(NOM)}$ + 0.5V ≤ V_{IN} ≤ 5.5V, I_{OUT} = 10mA		1	5	mV
$\Delta V_O/\Delta I_{OUT}$	Load regulation	0mA ≤ I_{OUT} ≤ 200mA			15	mV
V_{DO}	Dropout voltage(1)	V_{IN} = 0.98 × $V_{OUT(NOM)}$, I_{OUT} = 200mA		175	250	mV
I_{CL}	Output current limit	V_{OUT} = 0.9 × $V_{OUT(NOM)}$	220	350	860	mA
I_{GND}	Ground pin current	I_{OUT} = 0mA		31	55	µA
		I_{OUT} = 200mA, V_{IN} = V_{OUT} + 0.5V		270		
I_{SHDN}	Ground pin current (shutdown)	V_{EN} ≤ 0.4V, 2.0V ≤ V_{IN} ≤ 4.5V		1	2.5	µA
PSRR	Power-supply rejection ratio	V_{IN} = 2.3V, V_{OUT} = 1.8V, I_{OUT} = 10mA, f = 1kHz		68		dB
V_N	Output noise voltage	BW = 100Hz to 100kHz, V_{IN} = 2.3V, V_{OUT} = 1.8V, I_{OUT} = 10mA		48		μV_{RMS}
t_{STR}	Startup time(2)	C_{OUT} = 1µF, I_{OUT} = 200mA		100		µs
$V_{EN(HI)}$	Enable pin high (enabled)		0.9		V_{IN}	V
$V_{EN(LO)}$	Enable pin low (disabled)		0		0.4	V
I_{EN}	Enable pin current	V_{EN} = 5.5V , I_{OUT} = 10µA		0.04	0.5	µA
UVLO	Undervoltage lockout	V_{IN} rising		1.9		V
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		160		°C
		Reset, temperature decreasing		140		
T_A	Operating ambient temperature		–40		125	°C

(1) V_{DO} is measured for devices with $V_{OUT(NOM)}$ ≥ 2.35V.
(2) Startup time = time from EN assertion to 0.98 × $V_{OUT(NOM)}$.

5.6 Typical Characteristics

at T_J = –40°C to +125°C, V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2V (whichever is greater), I_{OUT} = 10mA, V_{EN} = V_{IN}, C_{IN} = 1µF, and C_{OUT} = 1µF (unless otherwise noted); typical values are at T_J = 25°C

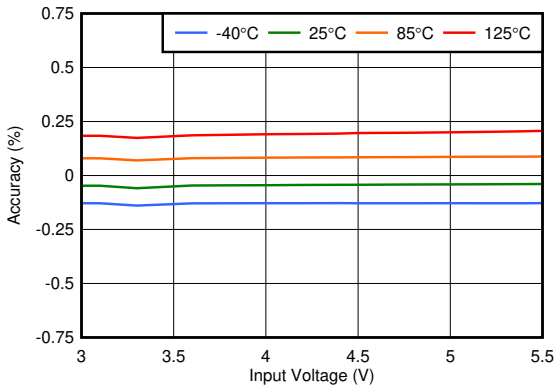


図 5-1. TLV70028-Q1 Line Regulation

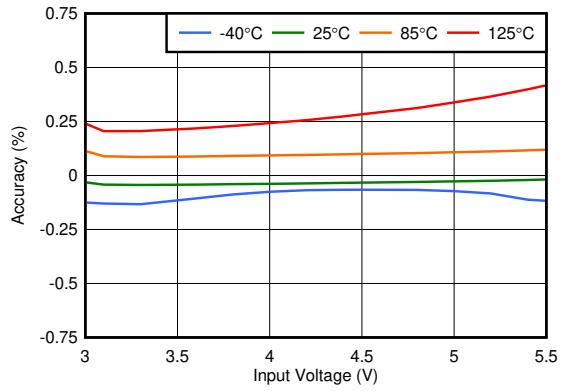


図 5-2. TLV70028-Q1 Line Regulation

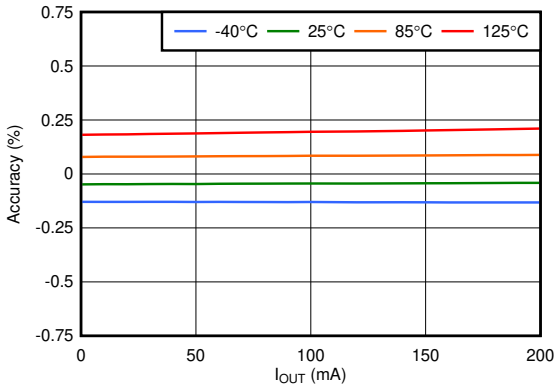


図 5-3. TLV70028-Q1 Load Regulation

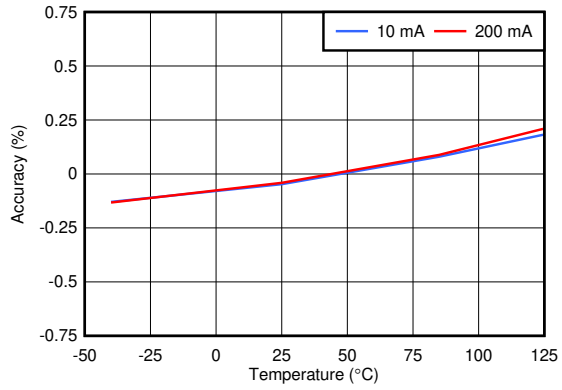


図 5-4. TLV70028-Q1 Accuracy vs Temperature

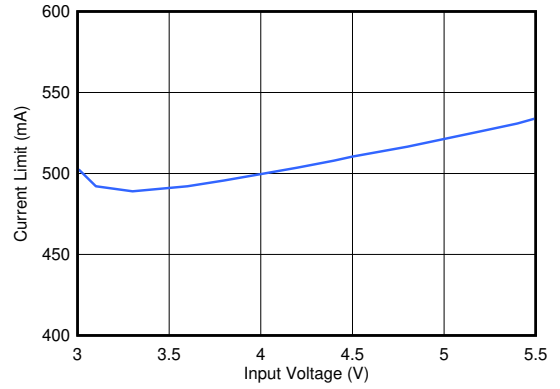


図 5-5. TLV70028-Q1 Current Limit vs Input Voltage

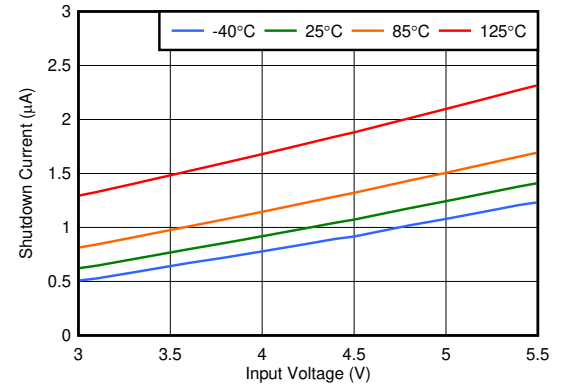


図 5-6. TLV70028-Q1 Shutdown Current vs Input Voltage

5.6 Typical Characteristics (continued)

at T_J = –40°C to +125°C, V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2V (whichever is greater), I_{OUT} = 10mA, V_{EN} = V_{IN}, C_{IN} = 1µF, and C_{OUT} = 1µF (unless otherwise noted); typical values are at T_J = 25°C

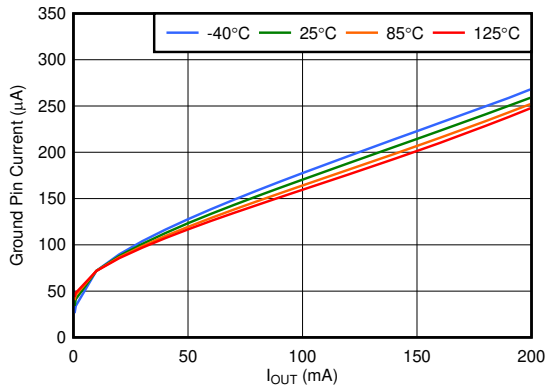


図 5-7. TLV70028-Q1 Ground Pin Current vs Output Current

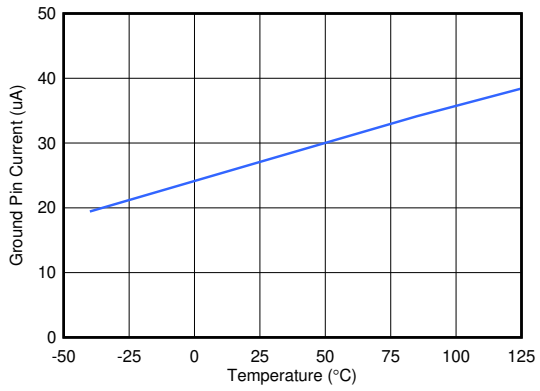
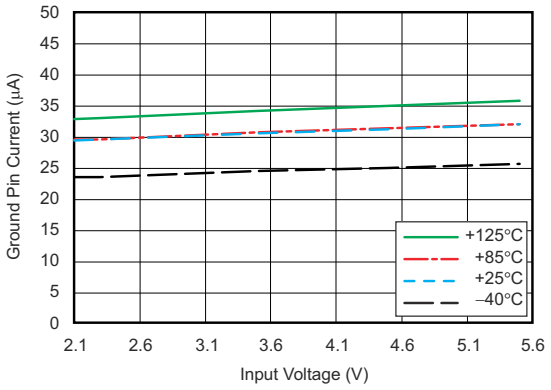
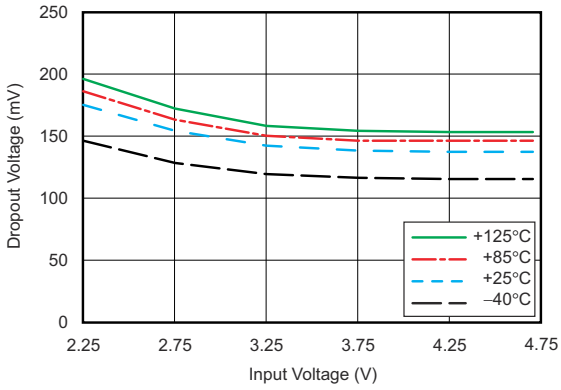


図 5-8. TLV70028-Q1 Ground Pin Current vs Temperature



IOUT = 0mA

図 5-9. TLV70048-Q1 Ground Pin Current vs Input Voltage



IOUT = 200mA

図 5-10. TLV70048-Q1 Dropout Voltage vs Input Voltage

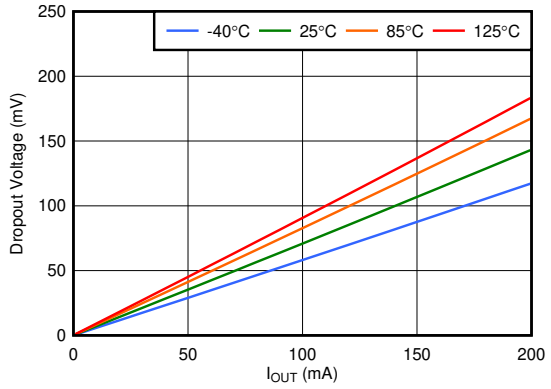


図 5-11. TLV70028-Q1 Dropout Voltage vs Output Current

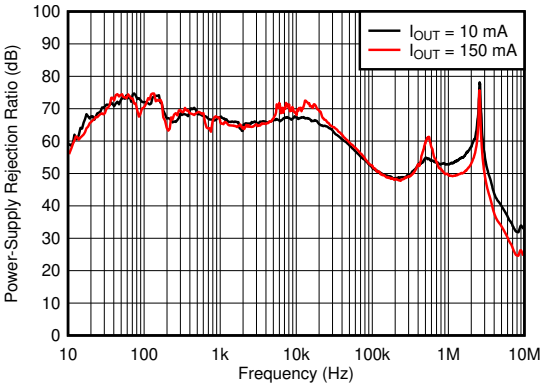


図 5-12. TLV70028-Q1 Power-Supply Rejection Ratio vs Frequency

5.6 Typical Characteristics (continued)

at T_J = –40°C to +125°C, V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2V (whichever is greater), I_{OUT} = 10mA, V_{EN} = V_{IN}, C_{IN} = 1µF, and C_{OUT} = 1µF (unless otherwise noted); typical values are at T_J = 25°C

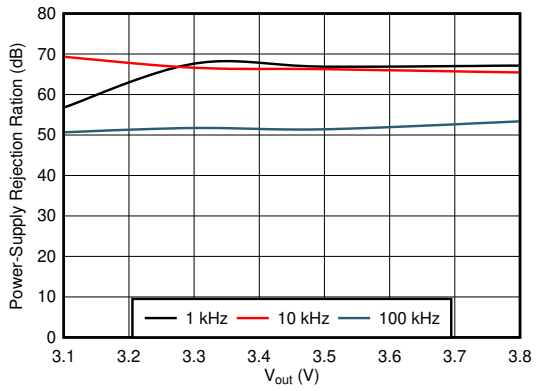


図 5-13. TLV70028-Q1 Power-Supply Rejection Ratio vs Output Voltage

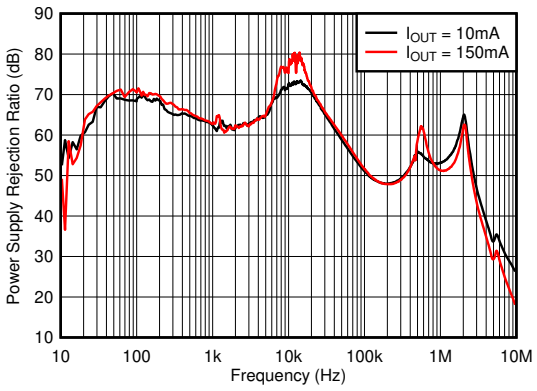


図 5-14. TLV70033-Q1 PSRR Ratio

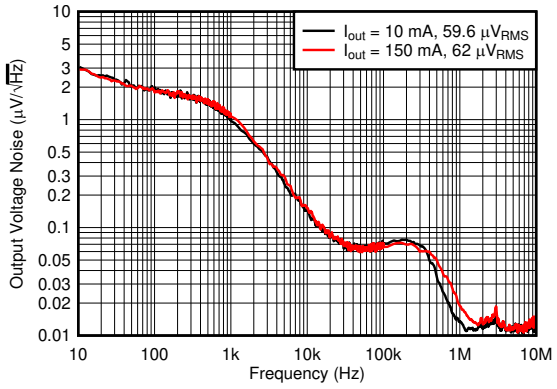
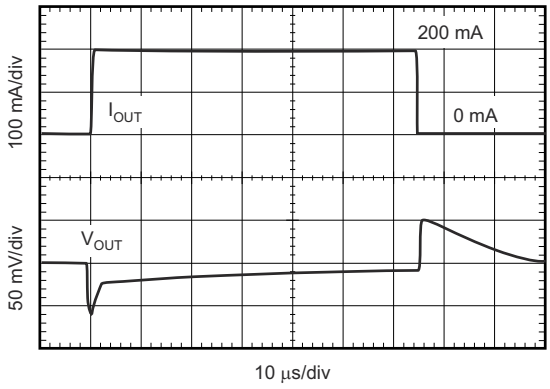
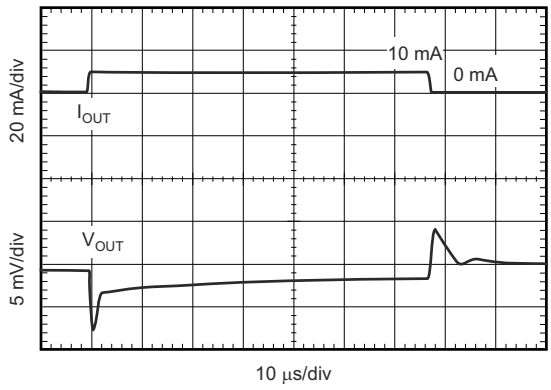


図 5-15. TLV70028-Q1 Output Spectral Noise Density vs Frequency



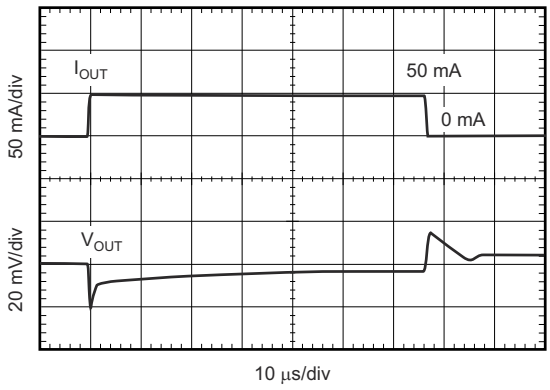
t_R = t_F = 1µs, V_{IN} = 2.1V

図 5-16. Load Transient Response



t_R = t_F = 1µs, V_{IN} = 2.3V

図 5-17. Load Transient Response

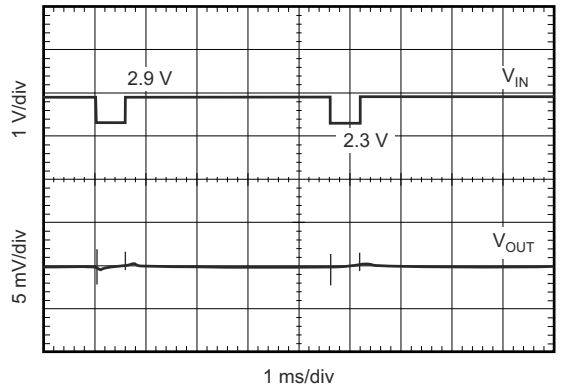


t_R = t_F = 1µs, V_{IN} = 2.3V

図 5-18. Load Transient Response

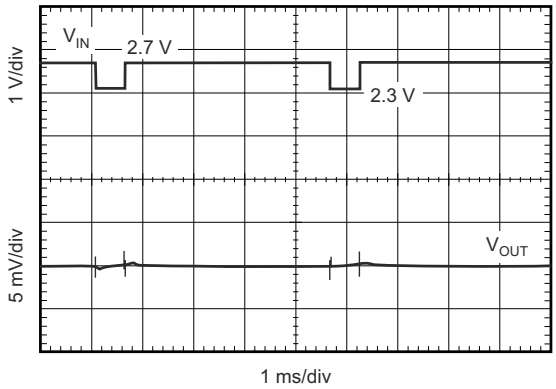
5.6 Typical Characteristics (continued)

at T_J = –40°C to +125°C, V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2V (whichever is greater), I_{OUT} = 10mA, V_{EN} = V_{IN}, C_{IN} = 1µF, and C_{OUT} = 1µF (unless otherwise noted); typical values are at T_J = 25°C



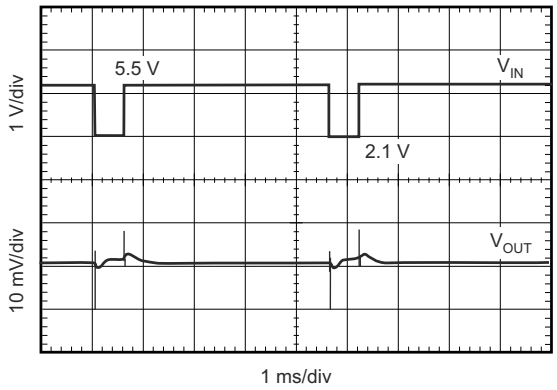
Slew rate = 1V/µs, I_{OUT} = 200mA

図 5-19. Line Transient Response



Slew rate = 1V/µs, I_{OUT} = 200mA

図 5-20. Line Transient Response



Slew rate = 1V/µs, I_{OUT} = 200mA

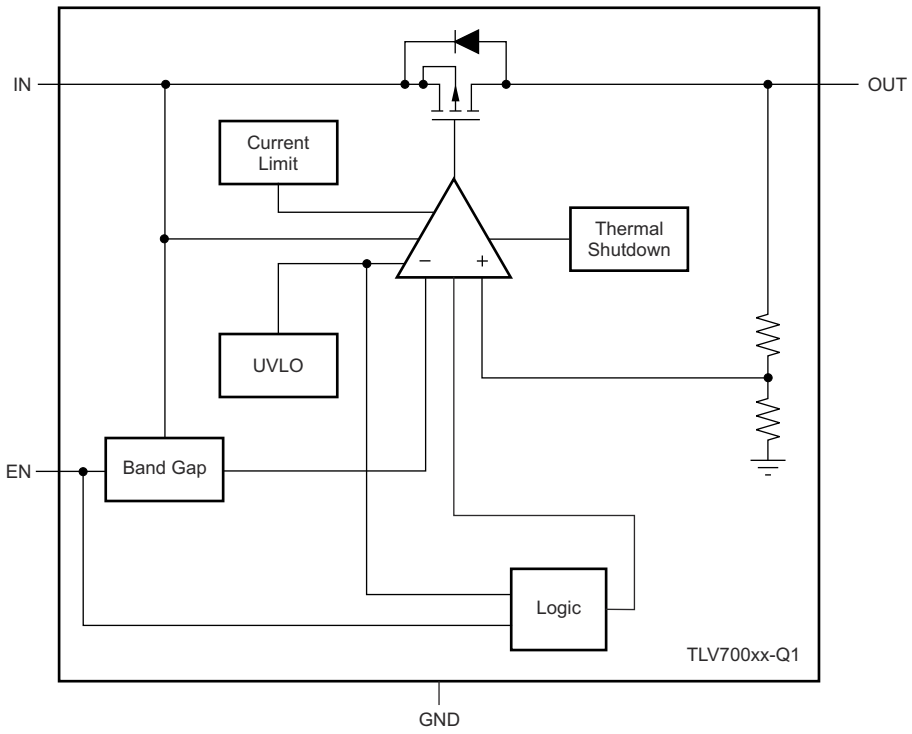
図 5-21. Line Transient Response

6 Detailed Description

6.1 Overview

The TLV700xx-Q1 low-dropout (LDO) linear regulators are low-quiescent-current devices with excellent line and load transient performance. These LDOs are designed for power-sensitive applications. A precision band-gap and error amplifier provides overall 2% accuracy together with low output noise, very high power-supply rejection ratio (PSRR), and low dropout voltage.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Internal Current Limit

The TLV700xx-Q1 internal current limit helps protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of the output voltage. In such a case, the output voltage is not regulated, and is $V_{OUT} = I_{LIMIT} \times R_{LOAD}$. The PMOS pass transistor dissipates $(V_{IN} – V_{OUT}) \times I_{LIMIT}$ until thermal shutdown is triggered and the device turns off. When the TLV700xx-Q1 cools down, the device is turned on by the internal thermal-shutdown circuit. If the fault condition continues, the device cycles between current limit and thermal shutdown; see the *Thermal Protection* section for more details.

The PMOS pass transistor in the TLV700xx-Q1 has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of the rated output current is recommended.

6.3.2 Shutdown

The enable pin (EN) is active high and is compatible with standard and low-voltage transistor-transistor logic, complementary metal oxide semiconductor (TTL-CMOS) levels. When shutdown capability is not required, EN can be connected to the IN pin.

6.3.3 Dropout Voltage

The TLV700xx-Q1 uses a PMOS pass transistor to achieve low dropout. When $(V_{IN} – V_{OUT})$ is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output

resistance is the $r_{DS(on)}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device behaves as a resistor in dropout.

As with any linear regulator, PSRR and transient response are degraded when (V_{IN} – V_{OUT}) approaches dropout. This effect is illustrated in 図 5-13 in the *Typical Characteristics* section.

6.3.4 Undervoltage Lockout (UVLO)

The TLV700xx-Q1 uses an undervoltage lockout circuit to keep the output shut off until the internal circuitry is operating properly.

6.4 Device Functional Modes

6.4.1 Operation with V_{IN} Less Than 2V

The TLV700xx-Q1 family of devices operates with input voltages above 2V. The typical UVLO voltage is 1.9V and the device operates at an input voltage above 2V. When the input voltage falls below the UVLO voltage, the device is shutdown.

6.4.2 Operation with V_{IN} Greater Than 2V

When V_{IN} is greater than 2V, if the input voltage is higher than the desired output voltage plus dropout voltage, the output voltage is equal to the desired value. Otherwise, the output voltage is V_{IN} minus the dropout voltage.

7 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

7.1 Application Information

The TLV700xx-Q1 devices belong to a family of next-generation-value LDO regulators. The devices consume low quiescent current and deliver excellent line and load transient performance. These characteristics, combined with low noise snd very good PSRR with little (V_{IN} – V_{OUT}) headroom, make this device family designed for for RF portable applications. This family of regulators offers sub-band-gap output voltages down to 0.7V, current limit, and thermal protection, and is specified from –40°C to +125°C.

7.1.1 Input and Output Capacitor Requirements

Ceramic, 1.0µF, X5R- and X7R-type capacitors are recommended because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature.

However, the TLV700xx-Q1 devices are designed to be stable with an effective capacitance of 0.1µF or larger at the output. Thus, these devices are stable with capacitors of other dielectric types as well, as long as the effective capacitance under operating bias voltage and temperature is greater than 0.1µF. This effective capacitance refers to the capacitance under the operating bias voltage and temperature conditions; that is, the capacitance after taking both bias voltage and temperature derating into consideration. In addition to allowing the use of cheaper dielectrics, this capability of being stable with 0.1µF effective capacitances also enables the use of smaller-footprint capacitors that have higher derating in size- and space-constrained applications.

Note that using a 0.1µF rated capacitor at the output of the LDO does not provide stability because the effective capacitance under the specified operating conditions is less than 0.1µF. Maximum ESR must be less than 200mΩ.

Although an input capacitor is not required for stability, good analog design practice is to connect a 0.1µF to 1µF, low-ESR capacitor across the IN pin and the GND pin of the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast, rise-time load transients are anticipated, or if the device is not located close to the power source. If source impedance is more than 2Ω, a 0.1µF input capacitor may be necessary to provide stability.

7.1.2 Transient Response

As with any regulator, increasing the size of the output capacitor reduces over- and undershoot magnitude but increases the duration of the transient response.

7.1.3 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit can cycle on and off. This cycling limits the dissipation of the regulator, protecting the regulator from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, limit junction temperature to 125°C (maximum). To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection must trigger at least 35°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of 125°C at the highest-expected ambient temperature and worst-case load.

The internal protection circuitry of the TLV700xx-Q1 is designed to protect against overload conditions. This circuitry is not intended to replace proper heatsinking. Continuously running the TLV700xx-Q1 into thermal shutdown degrades device reliability.

7.2 Typical Application

The TLV700xx-Q1 devices are 200mA, low quiescent current, low-noise, high-PSRR, fast start-up LDO linear regulators with excellent line and load transient response. The *TLV700xxEVM-503* user's guideevaluation module (EVM) helps designers evaluate the operation and performance of the TLV700xx-Q1 family.

図 7-1 shows a typical application for the TLV700xx-Q1 device.

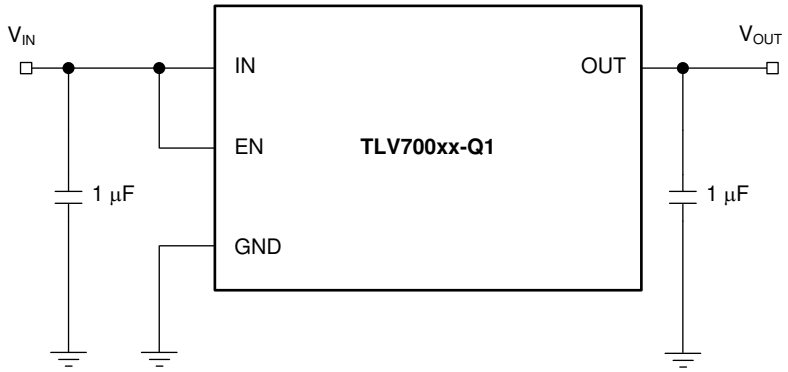


図 7-1. TLV700xx-Q1 Typical Application

7.2.1 Design Requirements

表 7-1 shows example design parameters and values for this typical application.

表 7-1. Design Parameters

PARAMETER	VALUE
Input voltage range	2V to 5.5V
Output voltage	2.2V, 2.8V, 3.2V
Output current rating	200mA
Effective output capacitor range	> 0.1µF
Maximum output capacitor ESR range	< 200mΩ

7.2.2 Detailed Design Procedure

7.2.2.1 Input Capacitance

Although not required for stability, connecting a 0.1µF to 1µF low-ESR capacitor across the IN pin and GND pin the regulator is good analog design practice.

7.2.2.2 Output Capacitance

Effect capacitance of 0.1µF or larger is required to provide stable operation. The maximum ESR must be less than 200mΩ.

7.2.2.3 Thermal Calculation

式 1 shows the thermal calculation.

$$P_D = I_{OUT} \times (V_{IN} - V_{OUT}) + I_Q \times V_{IN} \quad (1)$$

where:

- P_D = Continuous power dissipation
- I_{OUT} = Output current
- V_{IN} = Input voltage
- V_{OUT} = Output voltage
- Because I_Q << I_{OUT}, the term I_Q × V_{IN} is always ignored

For a device under operation at a given ambient air temperature (T_A), use 式 2 to calculate the junction temperature (T_J).

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (2)$$

where:

- $Z_{\theta JA}$ = Junction-to-ambient air thermal impedance

Use 式 3 to calculate the rise in junction temperature because of power dissipation.

$$\Delta T = T_J - T_A = (R_{\theta JA} \times P_D) \quad (3)$$

For a given maximum junction temperature (T_{Jmax}), use 式 4 to calculate the maximum ambient air temperature (T_{Amax}) at which the device can operate.

$$T_{Amax} = T_{Jmax} - (R_{\theta JA} \times P_D) \quad (4)$$

7.2.3 Application Curve

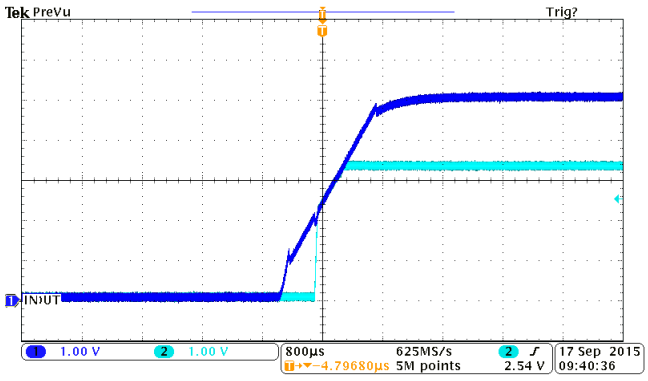


図 7-2. Power-Up

7.3 Power Supply Recommendations

The device is designed to operate from an input-voltage supply range between 2V and 5.5V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS7B69xx-Q1 device, a capacitor with a value of 0.1µF and a ceramic bypass capacitor are recommended to be added at the input.

7.4 Layout

7.4.1 Layout Guidelines

When laying out the board for the TLV700xx-Q1, the board is recommended to be designed with separate ground planes for V_{IN} and V_{OUT} that are only connected at the GND pin of the device, as shown in 図 7-3. Also, the ground connection for the bypass capacitor must be connected directly to the GND pin of the device. Improve the PSRR performance of the TLV700xx-Q1 by following these layout guidelines.

7.4.2 Board Layout Recommendations to Improve PSRR and Noise Performance

Place input and output capacitors as close to the device pins as possible. To improve ac performance (such as PSRR, output noise, and transient response), the board is recommended to be designed with separate ground planes for V_{IN} and V_{OUT}, with the ground plane connected only at the GND pin of the device. In addition, connect the ground connection for the output capacitor directly to the GND pin of the device. High-ESR capacitors can degrade PSRR performance.

7.4.3 Layout Example

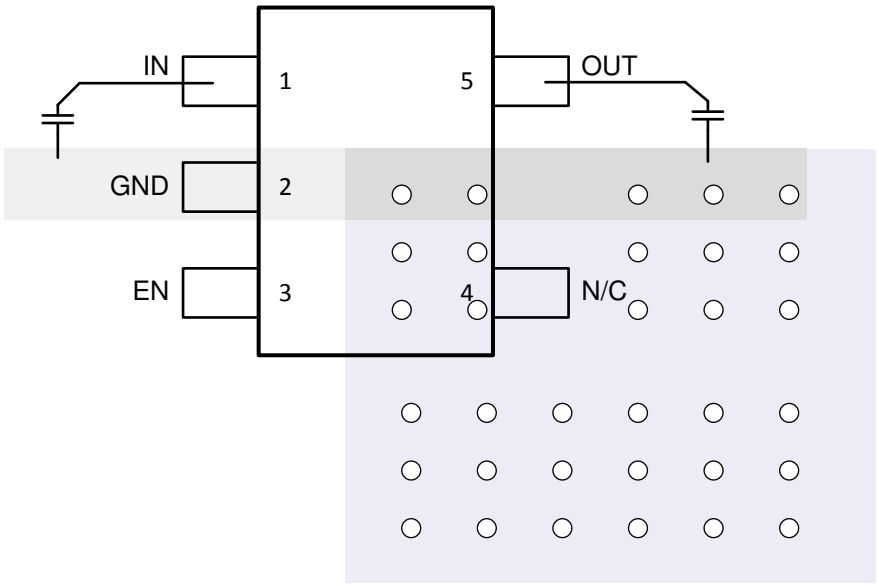


図 7-3. TLV700xx-Q1 Layout Example

8 Device and Documentation Support

8.1 Device Support

8.1.1 Device Nomenclature

表 8-1. Device Nomenclature

PRODUCT(1)	DESCRIPTION
TLV700**xxQyyyzQ1**	**xx** is the nominal output voltage (for example, 28 = 2.8V). **Q** indicates that this device is a grade-1 device in accordance with the AEC-Q100 standard. **yyy** is the package designator. **z** is the tape and reel quantity (R = 3000, T = 250). **Q1** indicates that this device is an automotive grade (AEC-Q100) device.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the device product folder at www.ti.com.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TLV700xxEVM-503* user's guide

8.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.4 サポート・リソース

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8.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

Changes from Revision C (June 2018) to Revision D (January 2025)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新	1

- Added *Device Nomenclature* table..... 16

Changes from Revision B (October 2016) to Revision C (June 2018) **Page**

- ドキュメントに DCK（SC70）パッケージを追加。TLV70025-Q1 および TLV70033-Q1 は従来は SLVSA61 に記載...1
- 「*特長*」セクションの「*固定出力電圧*」の箇条書き項目を、「*固定出力電圧の組み合わせ*」に変更.....1
- 「概要」セクションの最後の段落に SC70 パッケージを含めるよう変更..... 1
- 「*デバイス情報*」表に RGR の行を追加した..... 1
- Added T_J parameter to *Absolute Maximum Ratings* table.....4
- Changed T_J parameter to T_A in *Recommended Operating Conditions* table and changed *junction* to *ambient* in parameter name..... 4
- Added *TLV70033-Q1 PSRR Ratio* figure..... 6

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV70025QDDCRQ1	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QVC
TLV70025QDDCRQ1.A	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QVC
TLV70025QDDCRQ1.B	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QVC
TLV70028QDDCRQ1	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SJU
TLV70028QDDCRQ1.A	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SJU
TLV70028QDDCRQ1.B	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SJU
TLV70032QDDCRQ1	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SKA
TLV70032QDDCRQ1.A	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SKA
TLV70032QDDCRQ1.B	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SKA
TLV70033QDDCRQ1	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OFL
TLV70033QDDCRQ1.A	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OFL
TLV70033QDDCRQ1.B	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OFL

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

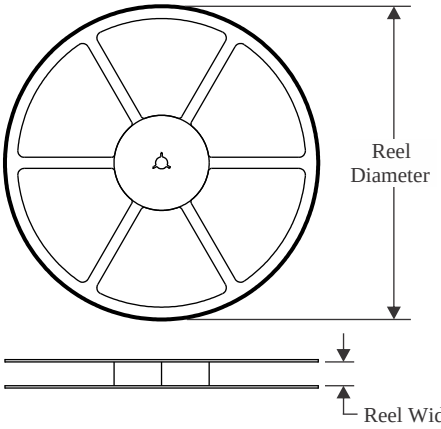
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

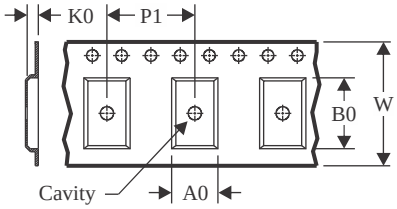
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

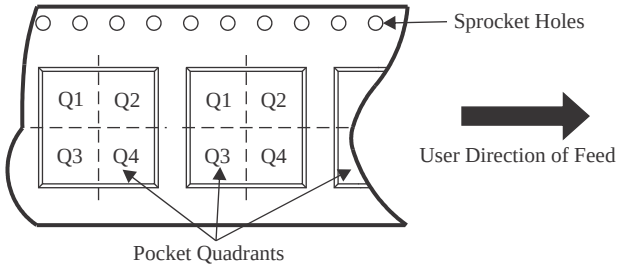


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

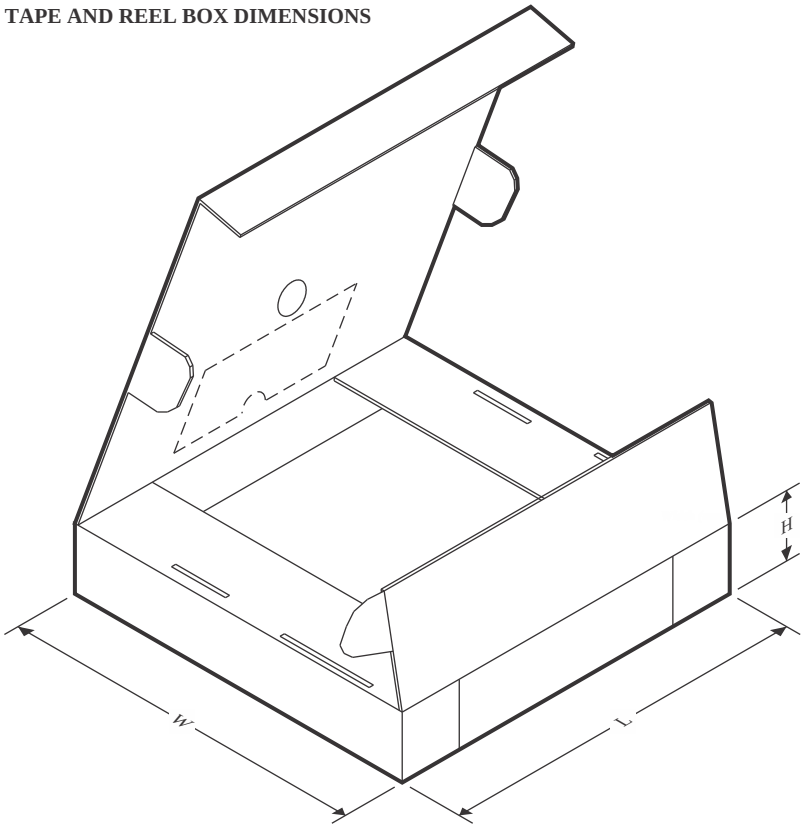
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV70025QDDCRQ1	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70028QDDCRQ1	SOT-23-THIN	DDC	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70032QDDCRQ1	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70033QDDCRQ1	SOT-23-THIN	DDC	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

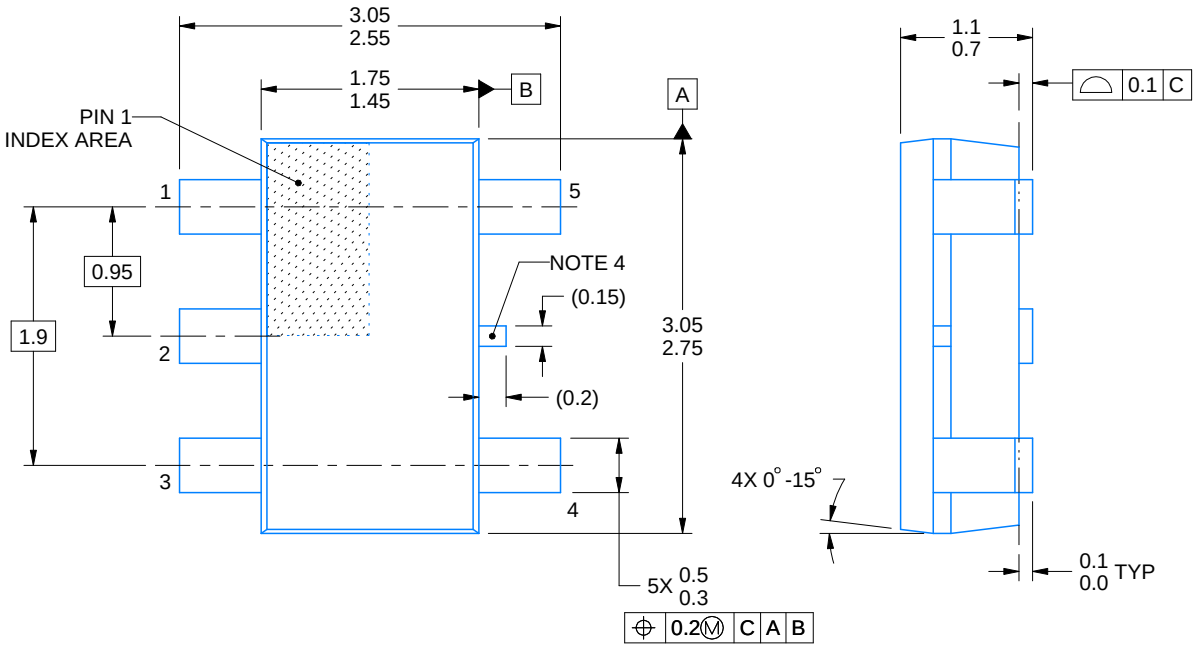
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV70025QDDCRQ1	SOT-23-THIN	DDC	5	3000	213.0	191.0	35.0
TLV70028QDDCRQ1	SOT-23-THIN	DDC	5	3000	213.0	191.0	35.0
TLV70032QDDCRQ1	SOT-23-THIN	DDC	5	3000	213.0	191.0	35.0
TLV70033QDDCRQ1	SOT-23-THIN	DDC	5	3000	213.0	191.0	35.0

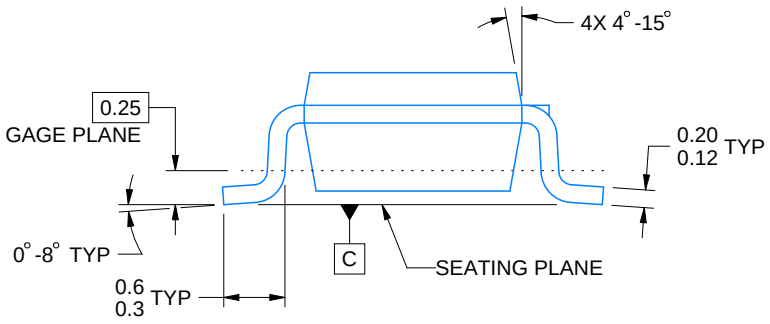
PACKAGE OUTLINE

DDC0005A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR





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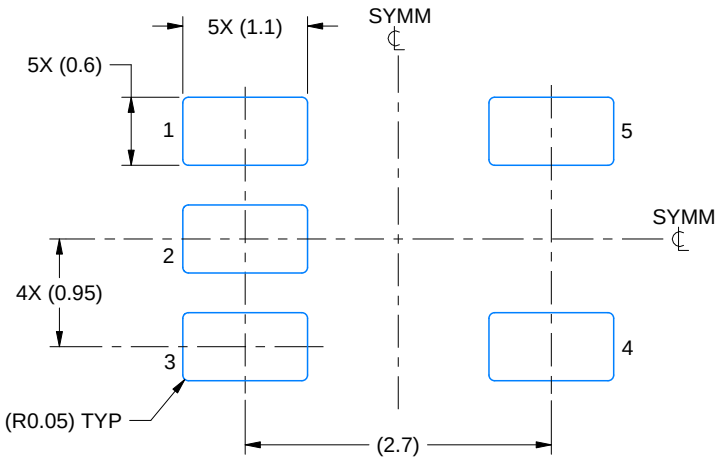
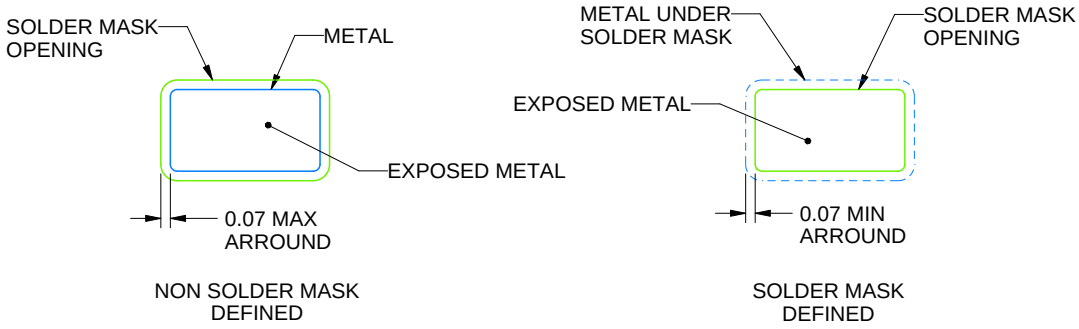
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.
4. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X



SOLDERMASK DETAILS

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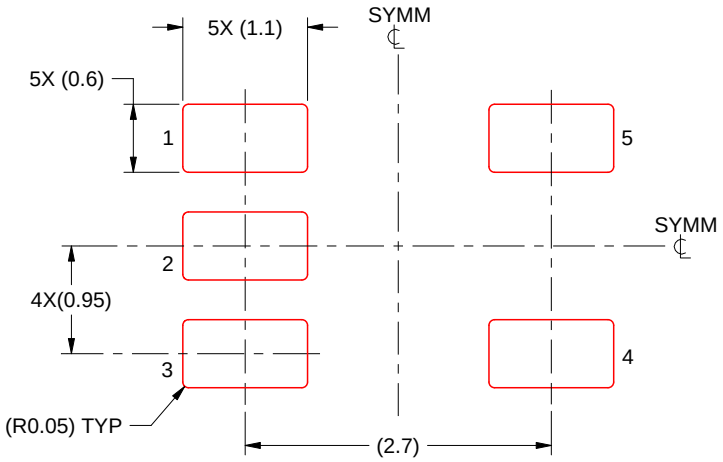
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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