

TLV6713 400mV基準電圧搭載マイクロパワー36Vコンパレータ

1 特長

- 広い電源電圧範囲: 1.8V~36V
- スレッシュホールドを変更可能: 最低400mV
- スレッシュホールドの高い精度
 - 0.25% (標準値)
 - 温度範囲全体で最大0.75%
- 低い静止電流: 7 μ A (標準値)
- オープン・ドレイン出力
- 内部ヒステリシス: 5.5mV (標準値)
- 温度範囲: -40°C~+125°C
- パッケージ: Thin SOT-23-6

2 アプリケーション

- ノートPCおよびタブレット
- スマートフォン
- デジタル・カメラ
- ビデオゲーム・コントローラ
- リレーおよびサーキット・ブレーカ
- ポータブル医療機器
- ドアまたは窓のセンサ
- 携帯用およびバッテリー駆動の製品

3 概要

TLV6713高電圧コンパレータは、1.8V~36Vの電源電圧範囲で動作します。高精度コンパレータと400mVの基準電圧に加え、低電圧検出用に定格25Vのオープン・ドレイン出力を内蔵しています。監視対象の電圧は外付け抵抗により設定できます。

SENSEピンの電圧が負のスレッシュホールドを下回るとOUTがLOWになり、正のスレッシュホールドを上回るとHIGHになります。TLV6713のコンパレータにはノイズ除去のヒステリシスが組み込まれているため、誤ったトリガが発生せず、安定した出力動作が確保されます。

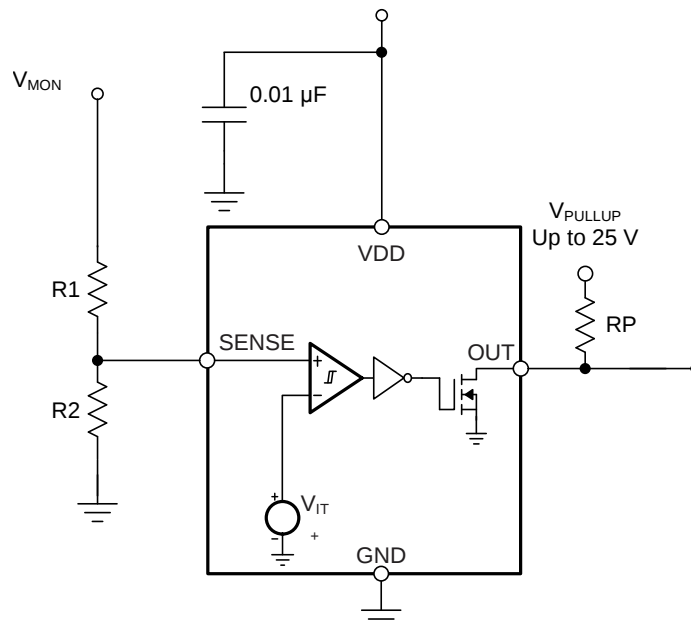
TLV6713はThin SOT-23-6パッケージで供給され、-40°C~+125°Cの接合部温度範囲で動作が規定されています。

製品情報 (1)

型番	パッケージ	本体サイズ(公称)
TLV6713	SOT-23 (6)	2.90mm×1.60mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にあるパッケージ・オプションについての付録を参照してください。

代表的なアプリケーション



目次

1	特長	1	8.3	Feature Description	9
2	アプリケーション	1	8.4	Device Functional Modes	9
3	概要	1	9	Application and Implementation	10
4	改訂履歴	2	9.1	Application Information	10
5	Device Comparison Table	2	9.2	Typical Application	11
6	Pin Configuration and Functions	3	10	Power Supply Recommendations	14
7	Specifications	4	11	Layout	15
7.1	Absolute Maximum Ratings	4	11.1	Layout Guidelines	15
7.2	ESD Ratings	4	11.2	Layout Example	15
7.3	Recommended Operating Conditions	4	12	デバイスおよびドキュメントのサポート	16
7.4	Thermal Information	4	12.1	デバイス・サポート	16
7.5	Electrical Characteristics	5	12.2	ドキュメントの更新通知を受け取る方法	16
7.6	Timing Requirements	5	12.3	コミュニティ・リソース	16
7.7	Typical Characteristics	6	12.4	商標	16
8	Detailed Description	8	12.5	静電気放電に関する注意事項	16
8.1	Overview	8	12.6	Glossary	16
8.2	Functional Block Diagram	8	13	メカニカル、パッケージ、および注文情報	16

4 改訂履歴

Revision A (April 2018) から Revision B に変更 Page

- 代表的なアプリケーションの図でプルアップ抵抗のテキストを36Vから25Vに変更 1

2018年1月発行のものから更新 Page

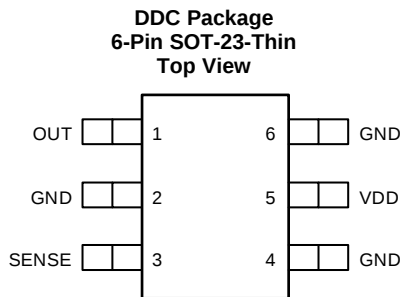
- 事前情報から量産データに変更 1

5 Device Comparison Table

Table 1. TLV67xx Integrated Comparator Family

PART NUMBER	CONFIGURATION	OPERATING VOLTAGE RANGE	THRESHOLD ACCURACY OVER TEMPERATURE
TLV6700	Window	1.8 V to 18 V	1%
TLV6703	Non-Inverting Single Channel	1.8 V to 18 V	1%
TLV6710	Window	1.8 V to 36 V	0.75%
TLV6713	Non-Inverting Single Channel	1.8 V to 36 V	0.75%

6 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	2, 4, 6	—	Ground. Connect all three pins to ground.
OUT	1	O	Comparator open-drain output. This pin is driven low when the voltage at this comparator is less than V_{IT-} . The output goes high when the sense voltage rises above V_{IT+} .
SENSE	3	I	Comparator input. This pin is connected to the voltage to be monitored with the use of an external resistor divider. When the voltage at this pin drops below the threshold voltage V_{IT-} , OUT is driven low.
VDD	5	I	Supply-voltage input. Connect a 1.8-V to 36-V supply to VDD to power the device. It is good analog design practice to place a 0.1- μ F ceramic capacitor close to this pin.

7 Specifications

7.1 Absolute Maximum Ratings⁽¹⁾

over operating junction temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Voltage ⁽²⁾	V _{DD}	−0.3	40	V
	V _{OUT}	−0.3	28	
	V _{SENSE}	−0.3	7	
Current	Output pin current		40	mA
Temperature	Operating junction, T _J	−40	125	°C
	Storage, T _{stg}	−40	125	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network ground terminal.

7.2 ESD Ratings

		VALUE	UNIT
V _(ESD) Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{DD}	Supply pin voltage	1.8		36	V
V _{SENSE}	Input pin voltage	0		1.7	V
V _{OUT}	Output pin voltage	0		25	V
V _{PULLUP}	Pullup voltage	0		25	V
I _{OUT}	Output pin current	0		10	mA
T _J	Junction temperature	−40	25	125	°C

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TLV6713	UNIT
		DDC (SOT-23)	
		6 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	201.6	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	47.8	°C/W
R _{θJB}	Junction-to-board thermal resistance	51.2	°C/W
ψ _{JT}	Junction-to-top characterization parameter	0.7	°C/W
ψ _{JB}	Junction-to-board characterization parameter	50.8	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.5 Electrical Characteristics

Over the operating temperature range of $T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $1.8\text{ V} \leq V_{DD} < 36\text{ V}$, and pullup resistor $R_P = 100\text{ k}\Omega$ (unless otherwise noted). Typical values are at $T_J = 25^{\circ}\text{C}$ and $V_{DD} = 12\text{ V}$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(POR)}$ Power-on reset voltage ⁽¹⁾	$V_{OL} \leq 0.2\text{ V}$			0.8	V
V_{IT-} SENSE pin negative input threshold voltage	$V_{DD} = 1.8\text{ V}$ to 36 V	397	400	403	mV
V_{IT+} SENSE pin positive input threshold voltage	$V_{DD} = 1.8\text{ V}$ to 36 V	400	405.5	413	mV
V_{HYS} SENSE pin hysteresis voltage ($HYS = V_{IT+} - V_{IT-}$)		2	5.5	12	mV
V_{OL} Low-level output voltage	$V_{DD} = 1.8\text{ V}$, $I_{OUT} = 3\text{ mA}$		130	250	mV
	$V_{DD} = 5\text{ V}$, $I_{OUT} = 5\text{ mA}$		150	250	
I_{IN} Input current (at SENSE pin)	$V_{DD} = 1.8\text{ V}$ and 36 V , $V_{SENSE} = 6.5\text{ V}$	-25	+1	+25	nA
	$V_{DD} = 1.8\text{ V}$ and 36 V , $V_{SENSE} = 0.1\text{ V}$	-15	+1	+15	
$I_{D(leak)}$ Open-drain leakage current	$V_{DD} = 1.8\text{ V}$ and 36 V , $V_{OUT} = 25\text{ V}$		10	300	nA
I_{DD} Supply current	$V_{DD} = 1.8\text{ V} - 36\text{ V}$		8	11	μA
UVLO Undervoltage lockout ⁽²⁾	V_{DD} falling	1.3	1.5	1.7	V

(1) The lowest supply voltage (V_{DD}) at which output is active; $t_{(VDD)} > 15\text{ }\mu\text{s/V}$. If less than $V_{(POR)}$, the output is undetermined.

(2) When V_{DD} falls below UVLO, OUT is driven low. The output cannot be determined if less than $V_{(POR)}$.

7.6 Timing Requirements

		MIN	NOM	MAX	UNIT
$t_{pd(HL)}$ High-to-low propagation delay ⁽¹⁾	$V_{DD} = 24\text{ V}$, $\pm 10\text{-mV}$ input overdrive, $R_L = 100\text{ k}\Omega$, $V_{OH} = 0.9 \times V_{DD}$, $V_{OL} = 250\text{ mV}$		9.9		μs
$t_{pd(LH)}$ Low-to-high propagation delay ⁽¹⁾	$V_{DD} = 24\text{ V}$, $\pm 10\text{-mV}$ input overdrive, $R_L = 100\text{ k}\Omega$, $V_{OH} = 0.9 \times V_{DD}$, $V_{OL} = 250\text{ mV}$		28.1		μs
$t_{d(start)}$ Startup delay ⁽²⁾	$V_{DD} = 5\text{ V}$		155		μs
t_r Output rise time	$V_{DD} = 12\text{ V}$, 10-mV input overdrive, $R_L = 100\text{ k}\Omega$, $C_L = 10\text{ pF}$, $V_O = (0.1\text{ to }0.9) \times V_{DD}$		2.7		μs
t_f Output fall time	$V_{DD} = 12\text{ V}$, 10-mV input overdrive, $R_L = 100\text{ k}\Omega$, $C_L = 10\text{ pF}$, $V_O = (0.9\text{ to }0.1) \times V_{DD}$		0.12		μs

(1) High-to-low and low-to-high refers to the transition at the input pin (SENSE).

(2) During power on, V_{DD} must exceed 1.8 V for at least $150\text{ }\mu\text{s}$ (typical) before the output state reflects the input condition.

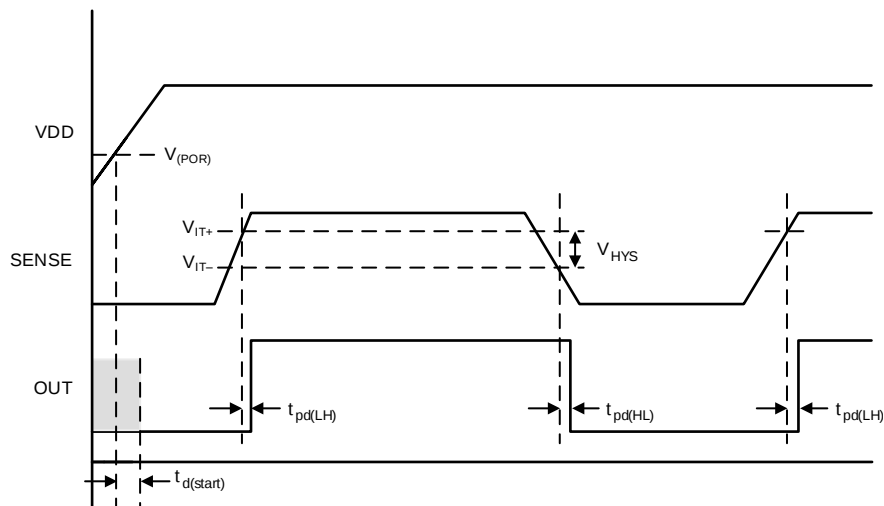


Figure 1. Timing Diagram

7.7 Typical Characteristics

at $T_J = 25^\circ\text{C}$ and $V_{DD} = 12\text{ V}$ (unless otherwise noted)

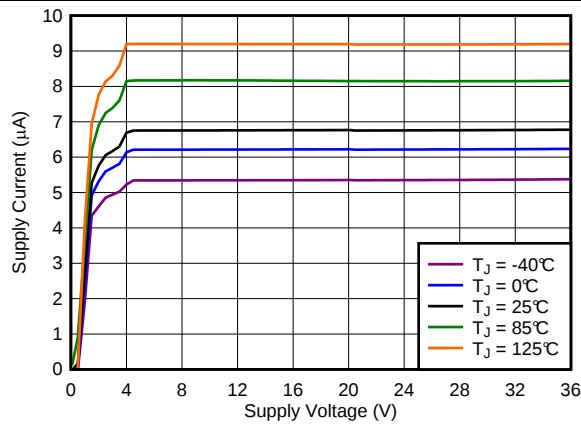
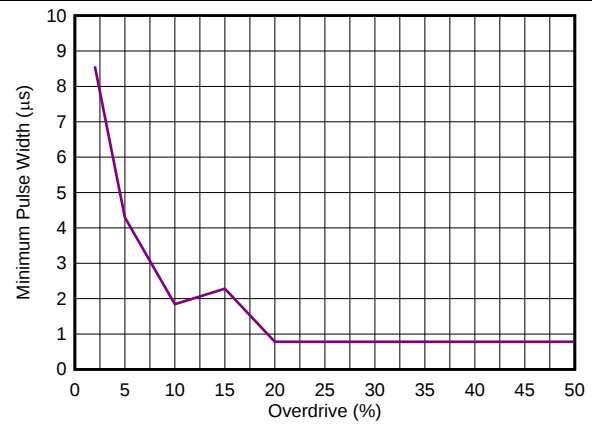


Figure 2. Supply Current vs Supply Voltage



$V_{DD} = 24\text{ V}$, minimum pulse duration required to trigger output high-to-low transition, SENSE = negative spike below V_{IT-}

Figure 3. Minimum Pulse Duration vs Threshold Overdrive Voltage

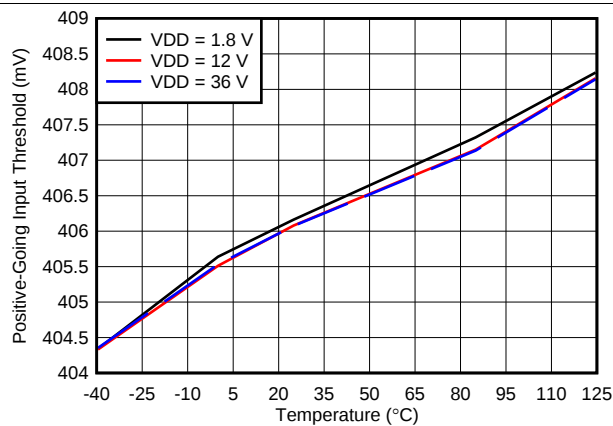


Figure 4. SENSE Positive Input Threshold Voltage (V_{IT+}) vs Temperature

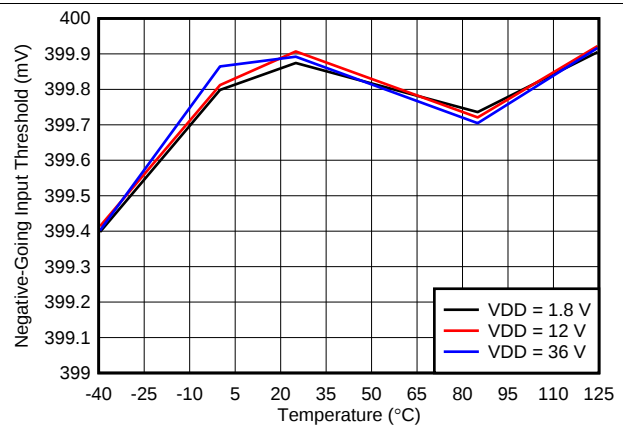


Figure 5. SENSE Negative Input Threshold Voltage (V_{IT-}) vs Temperature

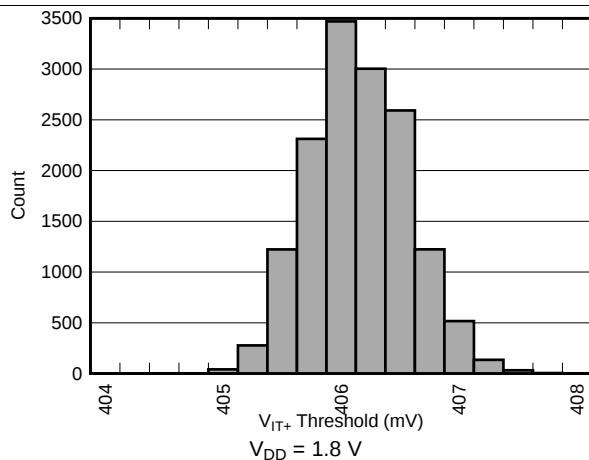


Figure 6. SENSE Positive Input Threshold Voltage (V_{IT+}) Distribution

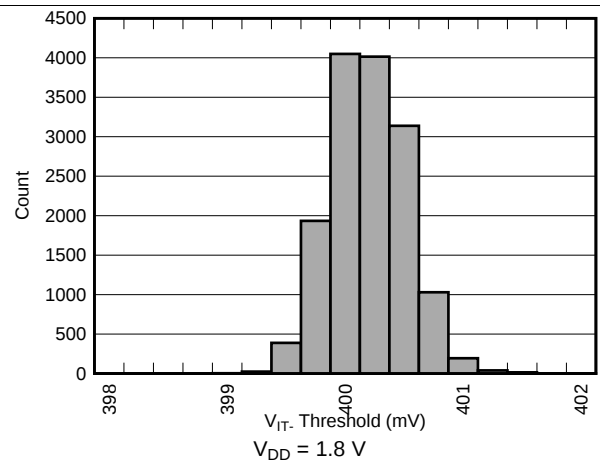
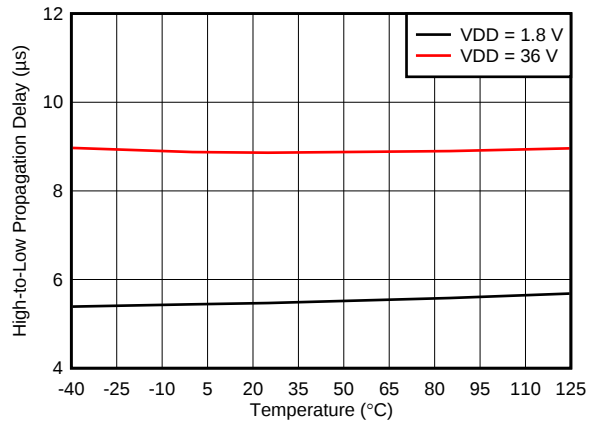


Figure 7. SENSE Negative Input Threshold Voltage (V_{IT-}) Distribution

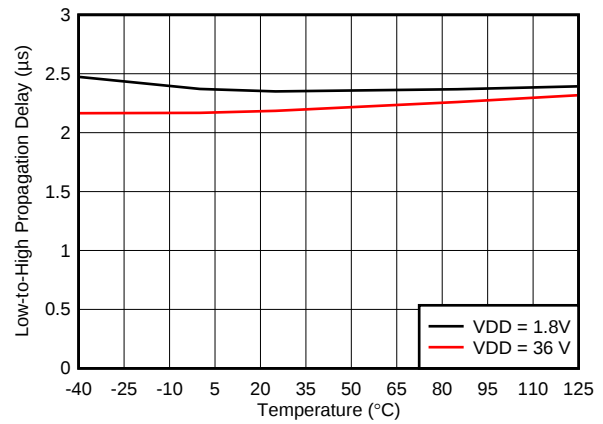
Typical Characteristics (continued)

at $T_J = 25^\circ\text{C}$ and $V_{DD} = 12\text{ V}$ (unless otherwise noted)



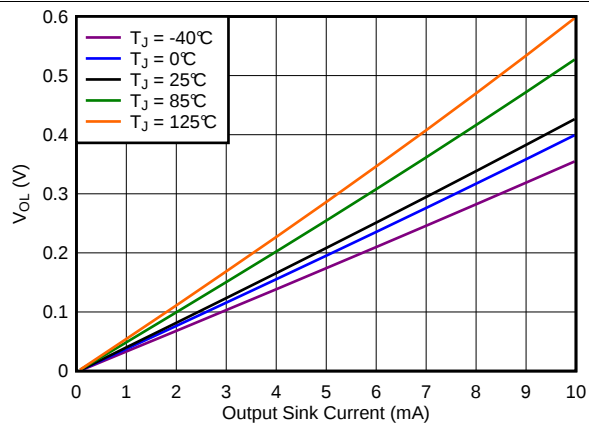
Input step $\pm 200\text{ mV}$

**Figure 8. Propagation Delay vs Temperature
(High-to-Low Transition at SENSE)**



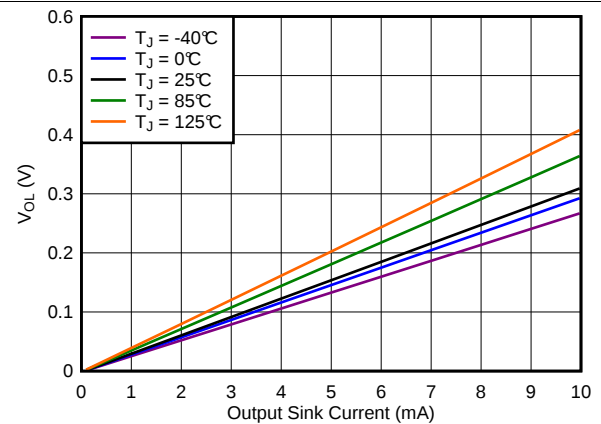
Input step $\pm 200\text{ mV}$

**Figure 9. Propagation Delay vs Temperature
(Low-to-High Transition at SENSE)**



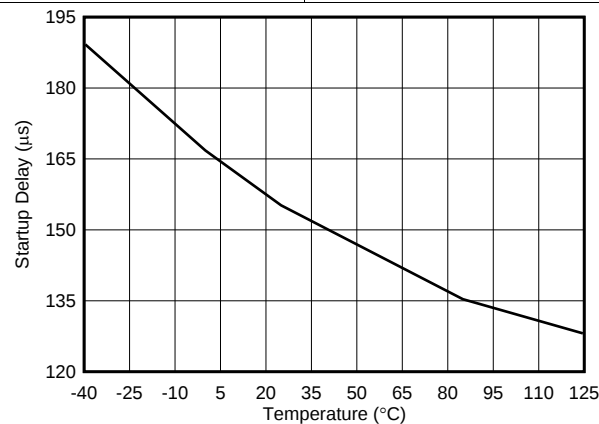
$V_{DD} = 1.8\text{ V}$

Figure 10. Output Voltage Low vs Output Sink Current



$V_{DD} = 12\text{ V}$

Figure 11. Output Voltage Low vs Output Sink Current



$V_{DD} = 5\text{ V}$

Figure 12. Start-up Delay vs Temperature

8 Detailed Description

8.1 Overview

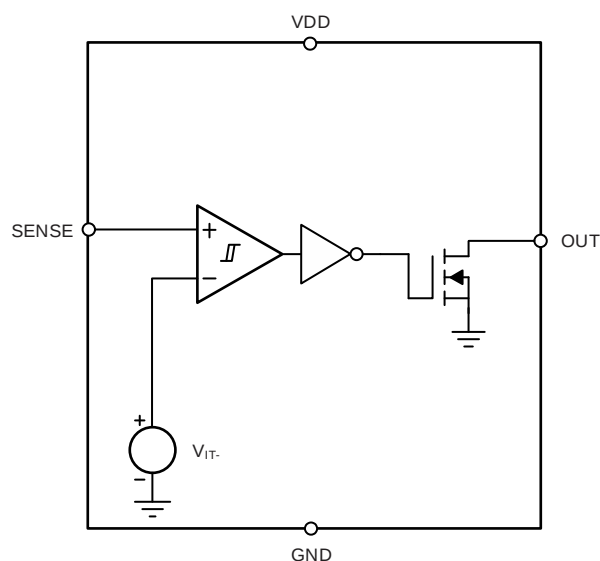
The TLV6713 combines a comparator and a precision reference for undervoltage detection. The TLV6713 features a wide supply voltage range (1.8 V to 36 V) and a high-accuracy threshold voltage of 400 mV (0.75% over temperature) with built-in hysteresis. The output is rated to 25 V and can sink up to 10 mA.

Set the input pin (SENSE) to monitor any voltage above 0.4 V by using an external resistor divider network. SENSE has very low input leakage current, allowing the use of a large resistor divider without sacrificing system accuracy. The relationship between the input and the output is shown in [Table 2](#). Broad voltage thresholds are supported that enable the device to be used in a wide array of applications.

Table 2. Truth Table

CONDITION	OUTPUT	OUTPUT STATE
$\text{SENSE} > V_{IT+}$	OUT high	Output high impedance
$\text{SENSE} < V_{IT-}$	OUT low	Output sinking

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Input Pin (SENSE)

The TLV6713 combines a comparator with a precision reference voltage. The comparator has one external input and one internal input connected to the internal reference. The falling threshold on SENSE is designed and trimmed to be equal to the reference voltage (400 mV). This configuration optimizes the device accuracy. The comparator also has built-in hysteresis that proves immunity to noise and ensures stable operation.

The comparator input swings from ground to 1.7 V (7 V absolute maximum), regardless of the device supply voltage used. Although not required in most cases, it is good analog design practice to place a 1-nF to 10-nF bypass capacitor at the comparator input for noisy applications to reduce sensitivity to transient voltage changes on the monitored signal.

For the comparator, the output (OUT) is driven to logic low when the input SENSE voltage drops below V_{IT-} . When the voltage exceeds V_{IT+} , OUT goes to a high-impedance state; see [Figure 1](#).

8.3.2 Output Pin (OUT)

In a typical TLV6713 application, the output is connected to a GPIO input of the processor (such as a digital signal processor [DSP], central processing unit [CPU], field-programmable gate array [FPGA], or application-specific integrated circuit [ASIC]).

The TLV6713 provides an open-drain output (OUT) rated to 25 V, independent of supply voltage, and can sink up to 40 mA. A pullup resistor is required to hold the line high when the output goes to a high-impedance state. Connect this pullup resistor to a voltage rail that meets the logic requirements of the downstream device. To ensure the proper voltage level, give some consideration when choosing the pullup resistor value. The pullup resistor value is determined by V_{OL} , output capacitive loading, and the open-drain leakage current ($I_{D(leak)}$). These values are specified in the [Electrical Characteristics](#) table.

[Table 2](#) and [Input Pin \(SENSE\)](#) describe how the output is asserted or high impedance. See [Figure 1](#) for a timing diagram that describes the relationship between threshold voltage and the respective output.

8.4 Device Functional Modes

8.4.1 Normal Operation ($V_{DD} > UVLO$)

When the voltage on VDD is greater than 1.8 V for at least 155 μ s, the OUT signal corresponds to the voltage on SENSE, as listed in [Table 2](#).

8.4.2 Undervoltage Lockout ($V_{(POR)} < V_{DD} < UVLO$)

When the voltage on VDD is less than the device UVLO voltage, and greater than the power-on reset voltage, $V_{(POR)}$, the OUT signal is asserted regardless of the voltage on SENSE.

8.4.3 Power On Reset ($V_{DD} < V_{(POR)}$)

When the voltage on VDD is lower than the required voltage to internally pull the asserted output to GND ($V_{(POR)}$), OUT is in a high-impedance state.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TLV6713 is used as a precision voltage supervisor in several different configurations. The monitored voltage (V_{MON}), VDD voltage, and output pullup voltage can be independent voltages or connected in any configuration. The following sections show the connection configurations and the voltage limitations for each configuration.

9.1.1 Input and Output Configurations

Figure 13 and Figure 14 show examples of the various input and output configurations.

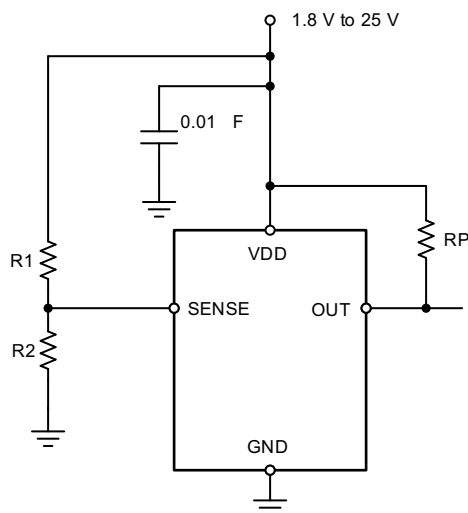
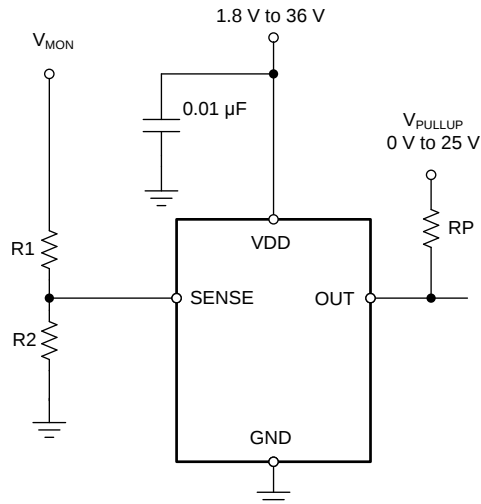


Figure 13. Monitoring the Same Voltage as V_{DD}

Application Information (continued)



NOTE: The input can monitor a voltage higher than V_{DD} (maximum) with the use of an external resistor divider network.

Figure 14. Monitoring a Voltage Other than V_{DD}

9.1.2 Immunity to Input Pin Voltage Transients

The TLV6713 is immune to short voltage transient spikes on the input pin. Sensitivity to transients depends on both transient duration and amplitude; see [Figure 3, Minimum Pulse Duration vs Threshold Overdrive Voltage](#).

9.2 Typical Application

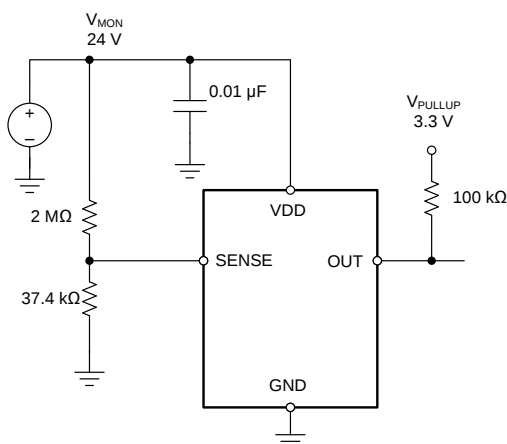


Figure 15. 24-V, 10% Comparator

Typical Application (continued)

9.2.1 Design Requirements

This typical voltage detector application is designed to meet the parameters listed in [Table 3](#):

Table 3. Design Parameters

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Monitored voltage	24-V nominal, falling ($V_{MON(UV)}$) threshold 10% nominal (21.6 V)	$V_{MON(UV)} = 21.8 \text{ V} \pm 2.7\%$
Output logic voltage	3.3-V CMOS	3.3-V CMOS
Maximum current consumption	30 μA	24 μA

9.2.2 Detailed Design Procedure

9.2.2.1 Resistor Divider Selection

The resistor divider values and target threshold voltage can be calculated by using [Equation 1](#) to determine $V_{MON(UV)}$.

$$V_{MON(UV)} = \left(1 + \frac{R1}{R2} \right) \times V_{IT}$$

where

- R1 and R2 are the resistor values for the resistor divider on the SENSE pin
 - $V_{MON(UV)}$ is the target voltage at which an undervoltage condition is detected
- (1)

Choose an R_{TOTAL} ($= R1 + R2$) so that the current through the divider is approximately 100 times higher than the input current at the SENSE pin. Use resistors with high values to minimize current consumption (as a result of low input bias current) without adding significant error to the resistive divider. For details on sizing input resistors, refer to [Optimizing Resistor Dividers at a Comparator Input](#), available for download from www.ti.com.

9.2.2.2 Pullup Resistor Selection

To ensure the proper logic-high voltage level (V_{HI}), select a pullup resistor value where the pullup voltage divided by the pullup resistor value does not exceed the sink-current capability of the device. Confirm this voltage level by verifying that the pullup voltage minus the open-drain leakage current ($I_{D(leak)}$) multiplied by the resistor is greater than the desired V_{HI} . These values are specified in the [Electrical Characteristics](#).

Use [Equation 2](#) to calculate the value of the pullup resistor.

$$\frac{V_{HI} - V_{pullup}}{I_{D(leak)}} \leq RP \leq \frac{V_{pullup}}{I_{OUT}}$$
(2)

9.2.2.3 Input Supply Capacitor

Although an input capacitor is not required for stability, for good analog design practice, connect a 0.1- μF low equivalent series resistance (ESR) capacitor across the VDD and GND pins. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is not located close to the power source.

9.2.3 Application Curve

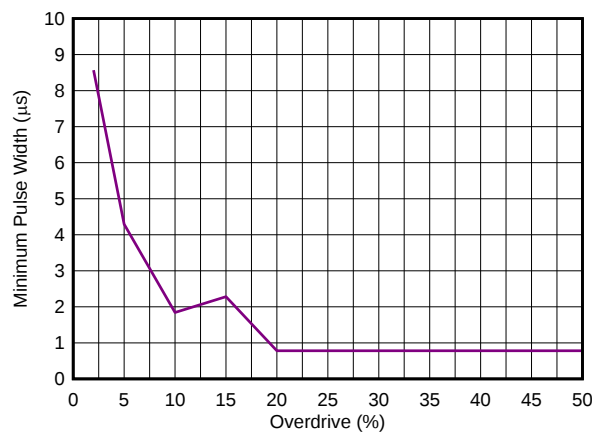


Figure 16. 24-V Window Monitor Output Response

10 Power Supply Recommendations

The TLV6713 has a 40-V absolute maximum rating on the VDD pin, with a recommended maximum operating condition of 36 V. If the voltage supply that provides power to VDD is susceptible to any large voltage transient that may exceed 40 V, or if the supply exhibits high voltage slew rates greater than 1 V/ μ s, then place an RC filter between the supply and VDD to filter any high-frequency transient surges on the VDD pin. In these cases, a 100- Ω resistor and 0.01- μ F capacitor are required, as shown in [Figure 17](#).

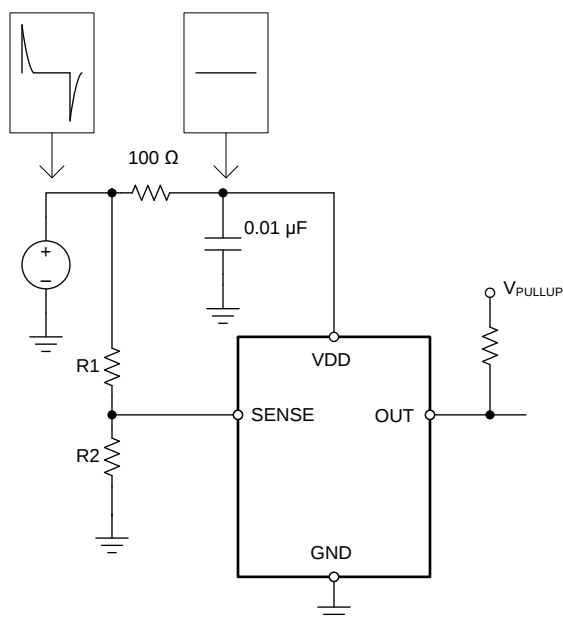


Figure 17. Using a RC Filter to Remove High-Frequency Disturbances on V_{DD}

11 Layout

11.1 Layout Guidelines

- Place R2 and R2 close to the device to minimize noise coupling into the SENSE node.
- Place the VDD decoupling capacitor close to the device.
- Avoid using long traces for the VDD supply node. The VDD capacitor (C_{VDD}), along with parasitic inductance from the supply to the capacitor, might form an LC tank and create ringing with peak voltages above the maximum VDD voltage. If long traces are unavoidable, see [Figure 17](#) for an example of filtering VDD.

11.2 Layout Example

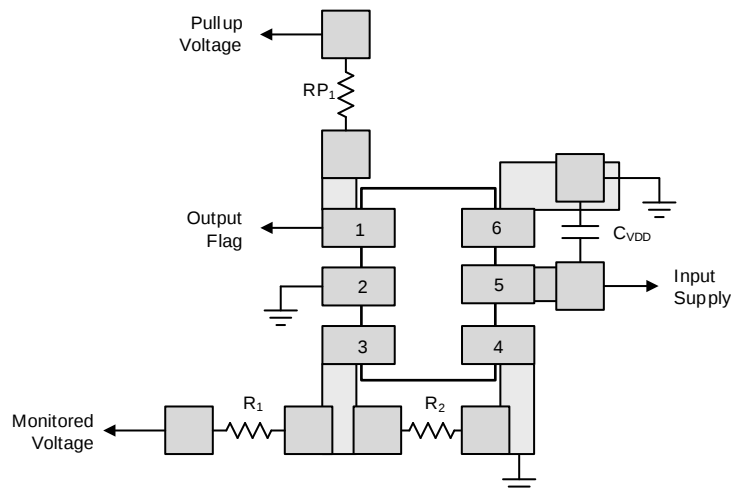


Figure 18. Recommended Layout

12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 開発サポート

[DIPアダプタ評価モジュール](#)では、SOT-23-6パッケージを標準のDIP-6ピン配置に変換して、プロトタイプ製作とベンチ評価を簡単に行うことができます。

12.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ オンライン・コミュニティ *TIのE2E (Engineer-to-Engineer) コミュニティ*。エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイデアを検討して、問題解決に役立てることができます。

設計サポート *TIの設計サポート 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。*

12.4 商標

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

12.5 静電気放電に関する注意事項



すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV6713DDCR	Active	Production	SOT-23-THIN (DDC) 6	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1II1
TLV6713DDCR.A	Active	Production	SOT-23-THIN (DDC) 6	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1II1
TLV6713DDCT	Active	Production	SOT-23-THIN (DDC) 6	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1II1
TLV6713DDCT.A	Active	Production	SOT-23-THIN (DDC) 6	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1II1
TLV6713DDCTG4	Active	Production	SOT-23-THIN (DDC) 6	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1II1
TLV6713DDCTG4.A	Active	Production	SOT-23-THIN (DDC) 6	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1II1

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

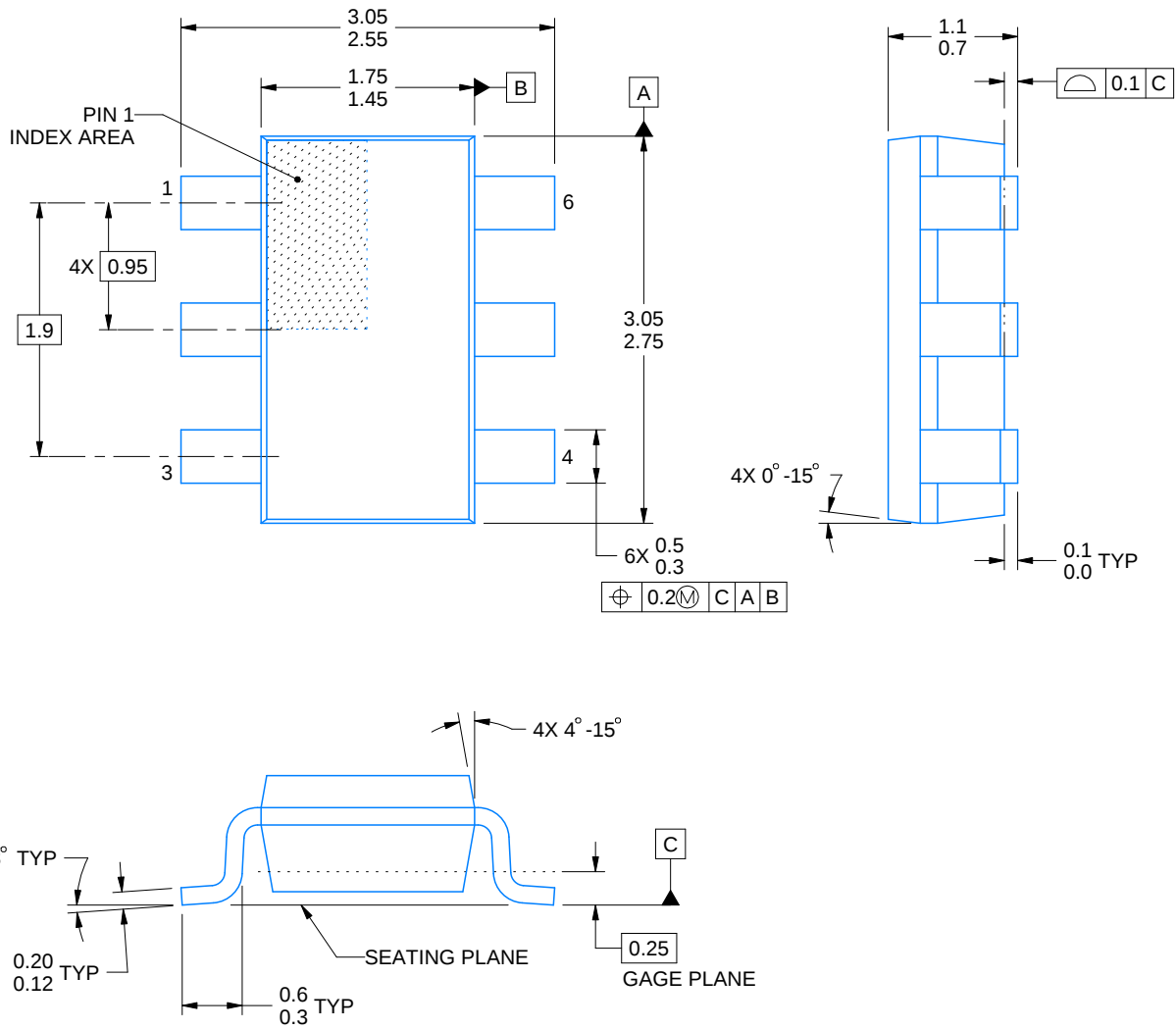
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV6713DDCR	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV6713DDCT	SOT-23-THIN	DDC	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV6713DDCTG4	SOT-23-THIN	DDC	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

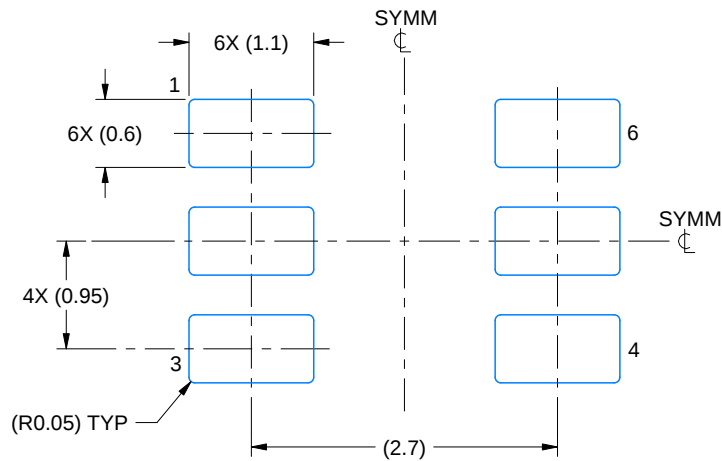
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV6713DDCR	SOT-23-THIN	DDC	6	3000	213.0	191.0	35.0
TLV6713DDCT	SOT-23-THIN	DDC	6	250	213.0	191.0	35.0
TLV6713DDCTG4	SOT-23-THIN	DDC	6	250	213.0	191.0	35.0



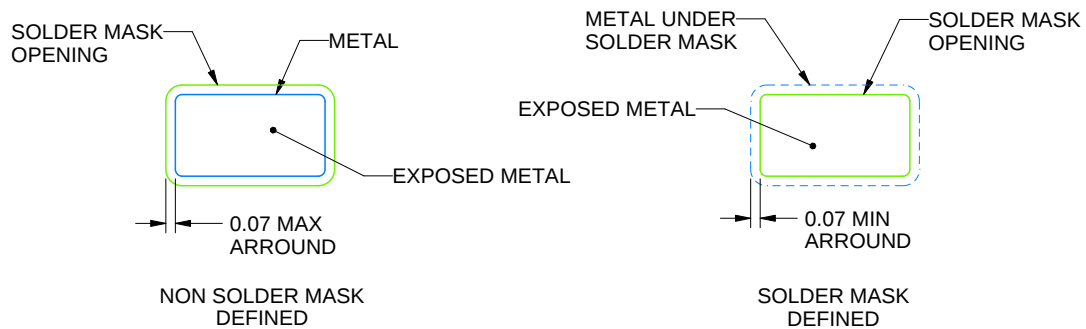
4214841/E 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE
EXPLODED METAL SHOWN
SCALE:15X

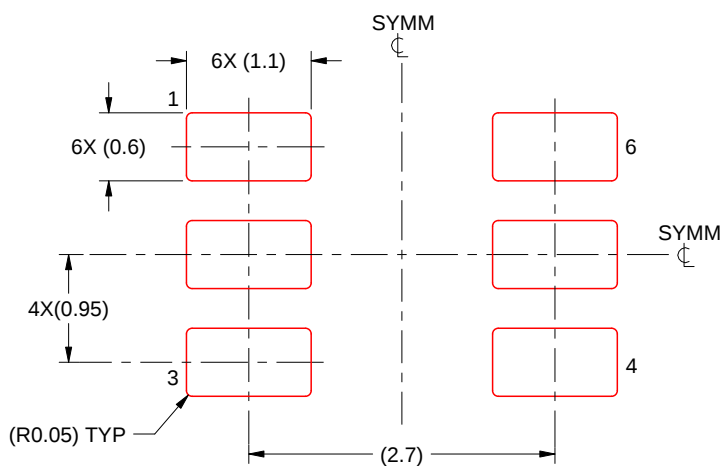


SOLDERMASK DETAILS

4214841/E 08/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
 BASED ON 0.125 THICK STENCIL
 SCALE:15X

4214841/E 08/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、[テキサス・インスツルメンツの販売条件](#)、または [ti.com](https://www.ti.com) やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用される テキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated