TLV62085 2mm×2mm VSONパッケージ、高効率の3A降圧コンバータ

1 特長

- DCS-Control™トポロジ
- 最大95%の効率
- 動作時静止電流: 17µA
- 31mΩおよび23mΩのパワーMOSFETスイッチ
- 入力電圧範囲: 2.5V～6.0V
- 出力電圧は0.8V～V_{IN}まで可変
- 省電力モードにより軽負荷時の効率を向上
- 100%デューティ·サイクル動作により低いドロップアウト電圧を実現
- ヒカップ短絡保護機能
- 出力放電
- パワー・グッド出力
- サーマル・シャットダウン保護機能
- 2mm×2mmのVSONパッケージで供給
- 改良された機能セットについては、TPS62085を参照
- WEBENCH® Power Designerにより、TLV62085を使用するカスタム設計を作成

2 アプリケーション

- バッテリ駆動のアプリケーション
- ポイント·オブ·ロード(POL)
- プロセッサ用電源
- ハードディスク・ドライブ(HDD)/ソリッドステート・ドライブ(SSD)

3 概要

TLV62085は、高効率な小型ソリューション向けに最適化された高周波同期整流降圧コンバータです。入力電圧範囲が2.5V～6.0Vで、一般的なバッテリ·テクノロジをサポートします。このデバイスは、広い出力電流範囲にわたって高い効率で降圧変換を行うことを主眼としています。中負荷から重負荷ではPWMモードで動作し、軽負荷時には自動的に省電力モードへ移行するため、負荷電流の全範囲にわたって高効率が維持されます。

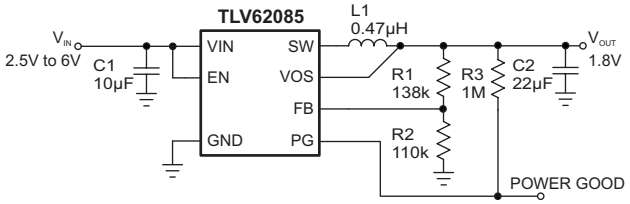
システム電源レールの要件に対処するため、内部補償回路は10µF～150µF、さらにそれを超えるものも含む、多くの外部出力コンデンサの値を選択できます。DCS-Control™アーキテクチャとともに、優れた負荷過渡性能と出力電圧レギュレーション精度を実現しています。このデバイスは、2mm×2mmのVSONパッケージで供給されます。

製品情報(1)

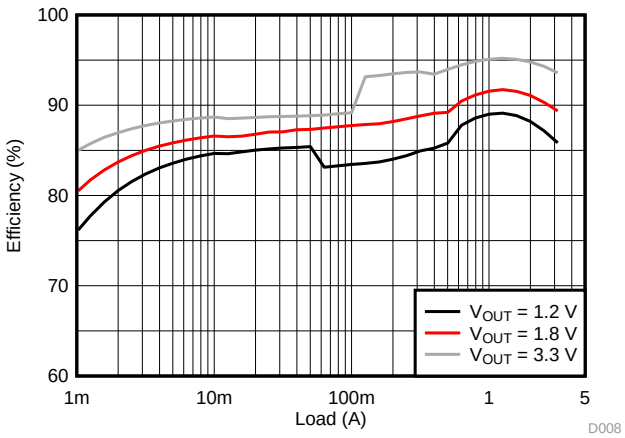
型番	パッケージ	本体サイズ(公称)
TLV62085	VSON (7)	2.00mm×2.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

代表的なアプリケーション回路図



V_{IN} = 5Vでの効率



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4 改訂履歴

Revision A (January 2017) to Revision B **Page**

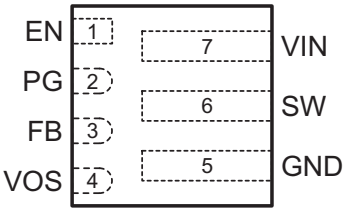
- Added 図 3 to power save mode section ... 7

201510 **Page**

- WEBENCH™の情報とハイパーリンクを「*特長*」、「*詳細な設計手順*」、「*デバイスのサポート*」セクションに Added ... 1
- Added SW (AC) to the *Absolute Maximum Rating* table ... 4
- Added 表 1, PG Pin Logic ... 8

5 Pin Configuration and Functions

RLT Package
7-Pin VSON
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	1	IN	Device enable pin. To enable the device, this pin needs to be pulled high. Pulling this pin low disables the device. This pin has a pulldown resistor of typically 400 kΩ when the device is disabled.
FB	3	IN	Feedback pin. Connect a resistor divider to set the output voltage.
GND	5		Ground pin.
PG	2	OUT	Power good open drain output pin. The pullup resistor can not be connected to any voltage higher than 6 V. If unused, leave it floating.
SW	6	PWR	Switch pin of the power stage.
VIN	7	PWR	Input voltage pin.
VOS	4	IN	Output voltage sense pin. This pin must be directly connected to the output capacitor.

6 Specifications

6.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Voltage at Pins(2)	VIN, FB, VOS, EN, PG	– 0.3	7	V
	SW (DC)	– 0.3	V_{IN} + 0.3	
	SW (AC, less than 100ns)(3)	– 3	11	
Temperature	Operating Junction, T_J	– 40	150	°C
	Storage, T_{stg}	– 65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) While switching.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions(1)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	2.5		6	V
V_{OUT}	Output voltage range	0.8		V_{IN}	V
I_{SINK_PG}	Sink current at PG pin			1	mA
V_{PG}	Pullup resistor voltage			6	V
T_J	Operating junction temperature	–40		125	°C

(1) Refer to *Application and Implementation* for further information.

6.4 Thermal Information

THERMAL METRIC(1)		TLV62085 RLT [VSON] 7 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	107.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	66.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	17.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

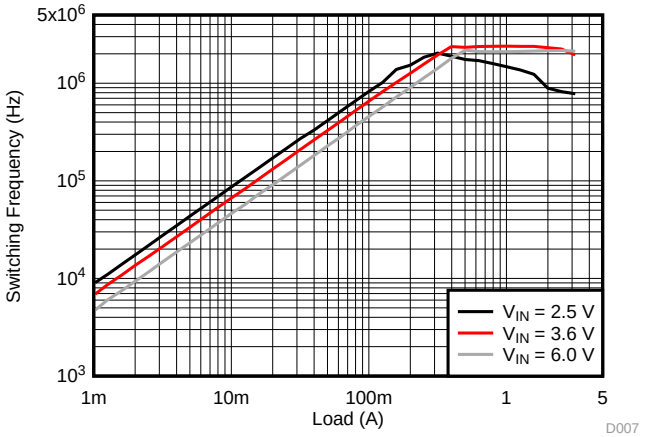
(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

T_J = 25 °C, and V_{IN} = 3.6 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_Q	Quiescent current into VIN	No load, device not switching		17		µA
I_{SD}	Shutdown current into VIN	EN = Low		0.7		µA
V_{UVLO}	Under voltage lock out threshold	V_{IN} falling	2.1	2.2	2.3	V
	Under voltage lock out hysteresis	V_{IN} rising		200		mV
T_{JSD}	Thermal shutdown threshold	T_J rising		150		°C
	Thermal shutdown hysteresis	T_J falling		20		°C
LOGIC INTERFACE EN						
V_{IH}	High-level input voltage	V_{IN} = 2.5 V to 6.0 V	1.0			V
V_{IL}	Low-level input voltage	V_{IN} = 2.5 V to 6.0 V			0.4	V
$I_{EN,LKG}$	Input leakage current into EN pin	EN = High		0.01		µA
R_{PD}	Pull-down resistance at EN pin	EN = Low		400		kΩ
SOFT START, POWER GOOD						
t_{SS}	Soft start time	Time from EN high to 95% of V_{OUT} nominal		0.8		ms
V_{PG}	Power good threshold	V_{OUT} rising, referenced to V_{OUT} nominal		95%		
		V_{OUT} falling, referenced to V_{OUT} nominal		90%		
$V_{PG,OL}$	Low-level output voltage	I_{sink} = 1 mA			0.4	V
$I_{PG,LKG}$	Input leakage current into PG pin	V_{PG} = 5.0 V		0.01		µA
OUTPUT						
V_{FB}	Feedback regulation voltage	PWM mode, 2.5 V ≤ VIN ≤ 6 V T_J = 0°C to 85 °C	792	800	808	mV
$I_{FB,LKG}$	Feedback input leakage current	V_{FB} = 1 V		0.01		µA
R_{DIS}	Output discharge resistor	EN = LOW, V_{OUT} = 1.8 V		260		Ω
POWER SWITCH						
$R_{DS(on)}$	High-side FET on-resistance	I_{SW} = 500 mA		31		mΩ
	Low-side FET on-resistance	I_{SW} = 500 mA		23		mΩ
I_{LIM}	High-side FET switch current limit		3.7	4.6	5.5	A
f_{SW}	PWM switching frequency	I_{OUT} = 1 A		2.4		MHz

6.6 Typical Characteristics



V_{OUT} = 1.2 V

図 1. Switching Frequency

7 Detailed Description

7.1 Overview

The TLV62085 synchronous step-down converter is based on the DCS-Control (Direct Control with Seamless transition into Power Save Mode) topology. This is an advanced regulation topology that combines the advantages of hysteretic, voltage, and current mode control schemes.

The DCS-Control topology operates in PWM (pulse width modulation) mode for medium to heavy load conditions and in Power Save Mode at light load currents. In PWM mode, the converter operates with its nominal switching frequency of 2.4 MHz, having a controlled frequency variation over the input voltage range. As the load current decreases, the converter enters Power Save Mode, reducing the switching frequency and minimizing the IC's current consumption to achieve high efficiency over the entire load current range. Because DCS-Control supports both operation modes (PWM and PFM) within a single building block, the transition from PWM mode to Power Save Mode is seamless and without effects on the output voltage. The device offers both excellent DC voltage and superior load transient regulation, combined with very low output voltage ripple, minimizing interference with RF circuits.

7.2 Functional Block Diagram

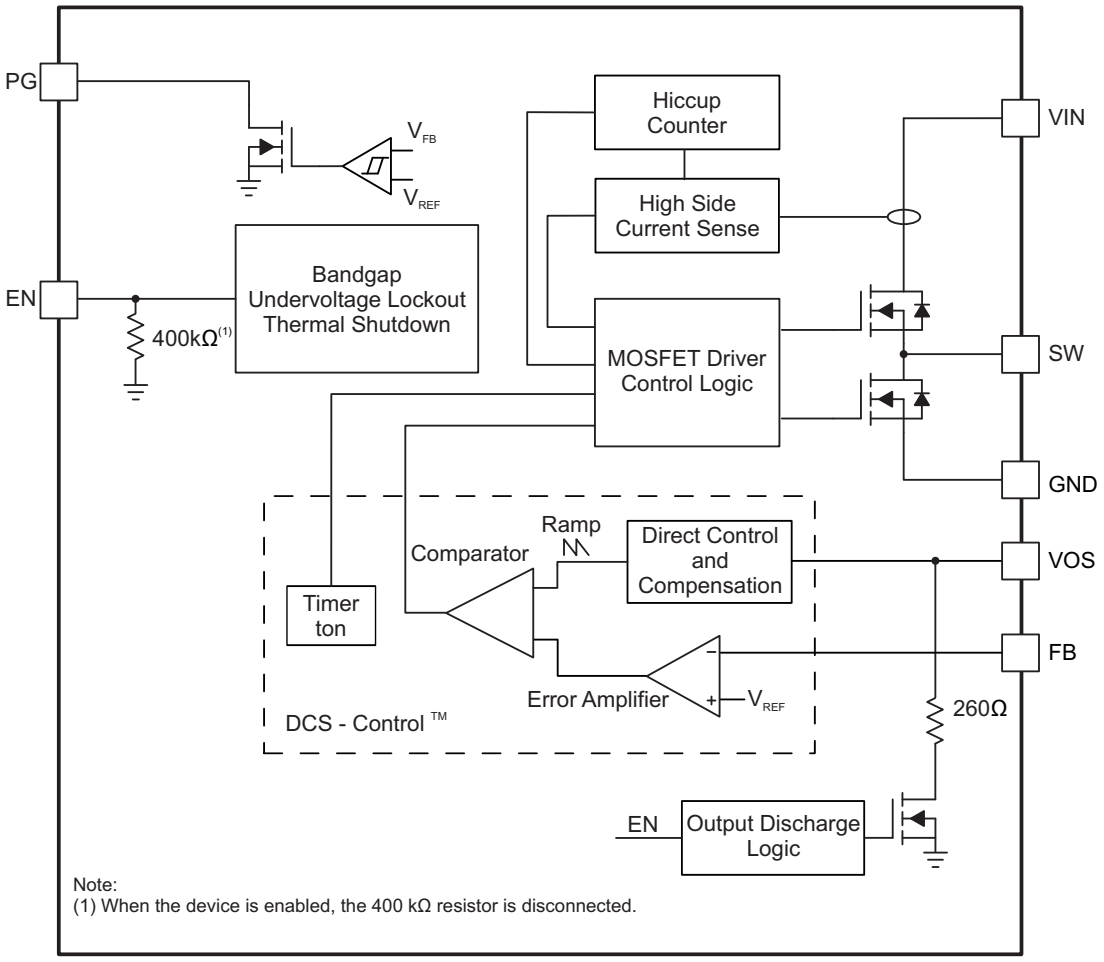


図 2. Functional Block Diagram

7.3 Feature Description

7.3.1 Power Save Mode

As the load current decreases, the TLV62085 enters Power Save Mode (PSM) operation. During Power Save Mode, the converter operates with reduced switching frequency and with a minimum quiescent current maintaining high efficiency. Power Save Mode occurs when the inductor current becomes discontinuous. Power Save Mode is based on a fixed on-time architecture, as related in Equation 1. The switching frequency over the whole load current range is also shown in 図 1 for a shown typical application.

$$t_{ON} = 420\ ns \times \frac{V_{OUT}}{V_{IN}}$$

$$f_{PFM} = \frac{2 \times I_{OUT}}{t_{ON}^2 \times \frac{V_{IN}}{V_{OUT}} \times \frac{V_{IN} - V_{OUT}}{L}} \quad (1)$$

In PSM, the output voltage rises slightly above the nominal output voltage, as shown in 図 10. This effect is minimized by increasing the output capacitor or inductor value.

During PAUSE period in PSM (shown in 図 3), the device does not change the PG pin state nor does it detect an UVLO event, in order to achieve a minimum quiescent current and maintain high efficiency at light loads.

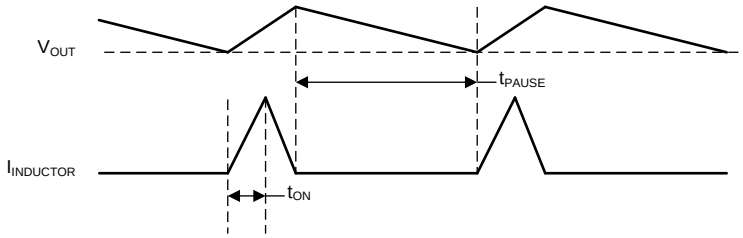


図 3. Power Save Mode Waveform Diagram

7.3.2 100% Duty Cycle Low Dropout Operation

The device offers low input-to-output voltage difference by entering 100% duty cycle mode. In this mode, the high-side MOSFET switch is constantly turned on and the low-side MOSFET is switched off. This is particularly useful in battery powered applications to achieve the longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage to maintain output regulation, depending on the load current and output voltage can be calculated as:

$$V_{IN,MIN} = V_{OUT} + I_{OUT,MAX} \times (R_{DS(on)} + R_L) \quad (2)$$

with

- $V_{IN,MIN}$ = Minimum input voltage to maintain an output voltage
- $I_{OUT,MAX}$ = Maximum output current
- $R_{DS(on)}$ = High-side FET ON-resistance
- R_L = Inductor ohmic resistance (DCR)

7.3.3 Soft Start

The TLV62085 has an internal soft-start circuitry which monotonically ramps up the output voltage and reaches the nominal output voltage during a soft-start time of typically 0.8 ms. This avoids excessive inrush current and creates a smooth output voltage slope. It also prevents excessive voltage drops of primary cells and rechargeable batteries with high internal impedance. The device is able to start into a prebiased output capacitor. The device starts with the applied bias voltage and ramps the output voltage to its nominal value.

Feature Description (continued)

7.3.4 Switch Current Limit and Hiccup Short-Circuit Protection

The switch current limit prevents the device from high inductor current and from drawing excessive current from the battery or input voltage rail. Excessive current might occur with a shorted or saturated inductor or a heavy load or shorted output circuit condition. If the inductor current reaches the threshold I_{LIM}, the high-side MOSFET is turned off and the low-side MOSFET is turned on to ramp down the inductor current. When this switch current limits is triggered 32 times, the device stops switching and enables the output discharge. The device then automatically starts a new start-up after a typical delay time of 66 µs has passed. This is named HICCUP short-circuit protection. The device repeats this mode until the high load condition disappears.

7.3.5 Undervoltage Lockout

To avoid misoperation of the device at low input voltages, an undervoltage lockout (UVLO) is implemented, which shuts down the device at voltages lower than V_{UVLO} with a hysteresis of 200 mV.

7.3.6 Thermal Shutdown

The device goes into thermal shutdown and stops switching when the junction temperature exceeds T_{JSD}. When the device temperature falls below the threshold by 20°C, the device returns to normal operation automatically.

7.4 Device Functional Modes

7.4.1 Enable and Disable

The device is enabled by setting the EN pin to a logic HIGH. Accordingly, shutdown mode is forced if the EN pin is pulled LOW with a shutdown current of typically 0.7 µA.

In shutdown mode, the internal power switches as well as the entire control circuitry are turned off. An internal resistor of 260 Ω discharges the output through the VOS pin smoothly. The output discharge function also works when thermal shutdown, UVLO, or short-circuit protection are triggered.

An internal pulldown resistor of 400 kΩ is connected to the EN pin when the EN pin is LOW. The pulldown resistor is disconnected when the EN pin is HIGH.

7.4.2 Power Good

The TLV62085 has a power good output. The power good goes high impedance once the output is above 95% of the nominal voltage, and is driven low once the output voltage falls below typically 90% of the nominal voltage. The PG pin is an open-drain output and is specified to sink up to 1 mA. The power good output requires a pull-up resistor connecting to any voltage rail less than 6 V. The PG signal can be used for sequencing of multiple rails by connecting it to the EN pin of other converters. Leave the PG pin unconnected when not used. 表 1 shows the PG pin logic.

表 1. PG Pin Logic

DEVICE CONDITIONS		LOGIC STATUS	
		HIGH Z	LOW
Enable	EN = High, $V_{FB} \geq V_{PG}$	√	
	EN = High, $V_{FB} \leq V_{PG}$		√
Shutdown	EN = Low		√
Thermal Shutdown	$T_J > T_{JSD}$		√
UVLO	$0.5\ V < V_{IN} < V_{UVLO}$		√
Power Supply Removal	$V_{IN} \leq 0.5\ V$	√	

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLV62085 is a synchronous step-down converter in which output voltage is adjusted by component selection. The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using the typical applications as a reference.

8.2 Typical Application

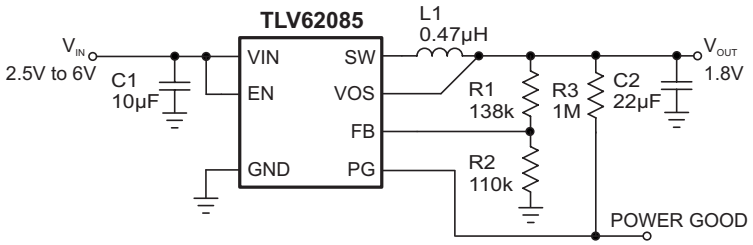


図 4. 1.8-V Output Voltage Application

8.2.1 Design Requirements

For this design example, use the parameters listed in 表 2 as the input parameters.

表 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	2.5 V to 6 V
Output voltage	1.8 V
Output current	≤ 3 A
Output ripple voltage	<30 mV

表 3 lists the components used for the example.

表 3. List of Components(1)

REFERENCE	DESCRIPTION	MANUFACTURER
C1	10 µF, Ceramic capacitor, 10 V, X7R, size 0805, GRM21BR71A106ME51L	Murata
C2	22 µF, Ceramic capacitor, 6.3 V, X5R, size 0805, GRM21BR60J226ME39L	Murata
L1	0.47 µH, Power Inductor, size 4 mm × 4 mm × 1.5 mm, XFL4015-471ME	Coilcraft
R1	Depending on the output voltage, 1%, size 0603;	Std
R2	110 kΩ, Chip resistor, 1/16 W, 1%, size 0603;	Std
R3	1 MΩ, Chip resistor, 1/16 W, 1%, size 0603	Std

(1) See Third-Party Products discalimer.

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design with WEBENCH® Tools

Click here to create a custom design using the TLV62085 device with the WEBENCH® Power Designer.

1. Start by entering your V_{IN}, V_{OUT}, and I_{OUT} requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. The WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   - Run electrical simulations to see important waveforms and circuit performance
   - Run thermal simulations to understand the thermal performance of your board
   - Export your customized schematic and layout into popular CAD formats
   - Print PDF reports for the design, and share your design with colleagues
5. Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Setting The Output Voltage

The output voltage is set by an external resistor divider according to Equation 3:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) = 0.8\ V \times \left(1 + \frac{R1}{R2}\right) \quad (3)$$

R2 must not be higher than 180 kΩ to achieve high efficiency at light load while providing acceptable noise sensitivity.

8.2.2.3 Output Filter Design

The inductor and the output capacitor together provide a low-pass filter. To simplify the selection process, 表 4 outlines possible inductor and capacitor value combinations for most applications.

表 4. Matrix of Output Capacitor and Inductor Combinations

NOMINAL L [µH](1)	NOMINAL C_{OUT} [µF](2)				
	10	22	47	100	150
0.47		+(3)	+	+	+
1	+	+	+	+	+
2.2					

(1) Inductor tolerance and current derating is anticipated. The effective inductance can vary by 20% and –30%.
(2) Capacitance tolerance and bias voltage derating is anticipated. The effective capacitance can vary by 20% and –50%.
(3) Typical application configuration. Other '+' mark indicates recommended filter combinations.

8.2.2.4 Inductor Selection

The main parameter for the inductor selection is the inductor value and then the saturation current of the inductor. To calculate the maximum inductor current under static load conditions, Equation 4 is given.

$$I_{L,MAX} = I_{OUT,MAX} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}}$$

where

- $I_{OUT,MAX}$ = Maximum output current
- ΔI_L = Inductor current ripple

- f_{SW} = Switching frequency
- L = Inductor value (4)

TI recommends choosing the saturation current for the inductor 20% to 30% higher than the $I_{L,MAX}$, out of Equation 4. A higher inductor value is also useful to lower ripple current but increases the transient response time as well. The following inductors are recommended to be used in designs.

表 5. List of Recommended Inductors(1)

INDUCTANCE [µH]	CURRENT RATING [A]	DIMENSIONS L × W × H [mm³]	DC RESISTANCE [mΩ typical]	PART NUMBER
0.47	6.6	4 × 4 × 1.5	7.6	Coilcraft XFL4015-471
0.47	4.7	3.2 × 2.5 × 1.2	21	TOKO DFE322512-R47N
1	5.1	4 × 4 × 2	10.8	Coilcraft XFL4020-102

(1) See Third-Party Products disclaimer.

8.2.2.5 Capacitor Selection

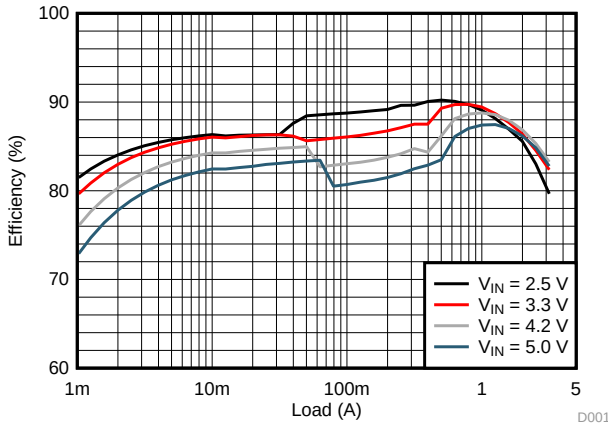
The input capacitor is the low-impedance energy source for the converter which helps to provide stable operation. A low ESR multilayer ceramic capacitor is recommended for best filtering and must be placed between VIN and GND as close as possible to those pins. For most applications, 10 µF is sufficient, though a larger value reduces input current ripple.

The architecture of the TLV62085 allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep its low resistance up to high frequencies and to get narrow capacitance variation with temperature, TI recommends using X7R or X5R dielectrics. The recommended typical output capacitor value is 22 µF; this capacitance can vary over a wide range as outline in the output filter selection table. Output capacitors above 150uF may be used with a reduced load current during startup to avoid triggering the short circuit protection.

A feed-forward capacitor is not required for device proper operation.

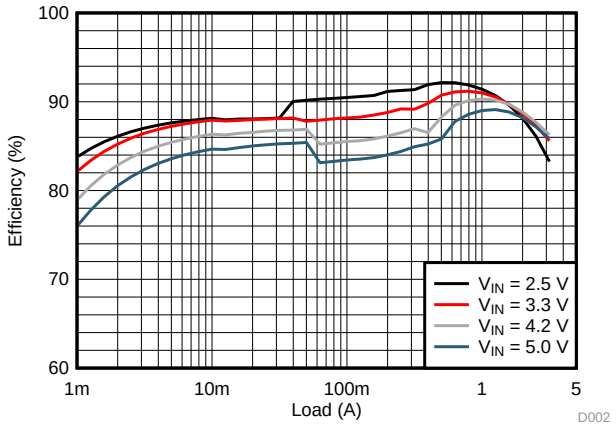
8.2.3 Application Curves

V_{IN} = 3.6 V, T_A = 25 ºC, unless otherwise noted



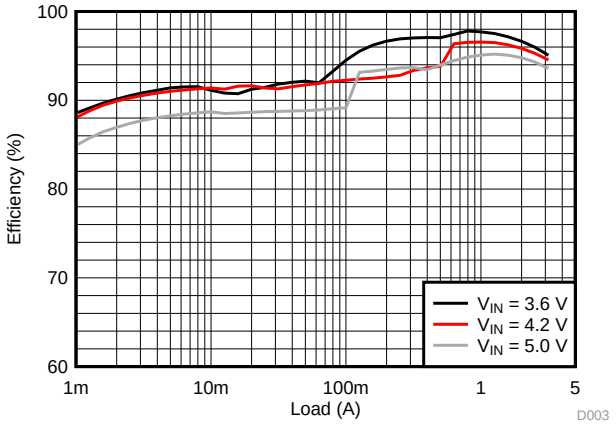
V_{OUT} = 0.95 V

図 5. Efficiency



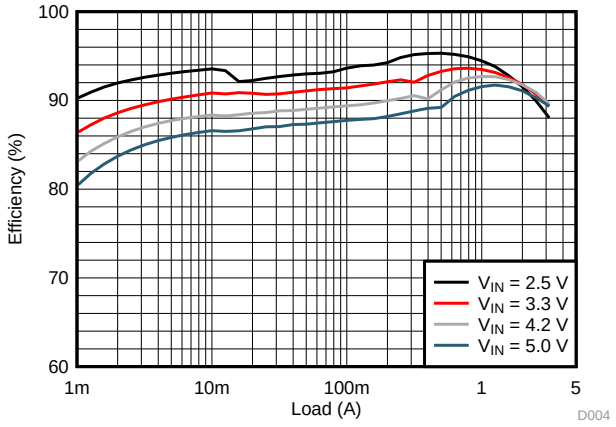
V_{OUT} = 1.2 V

図 6. Efficiency



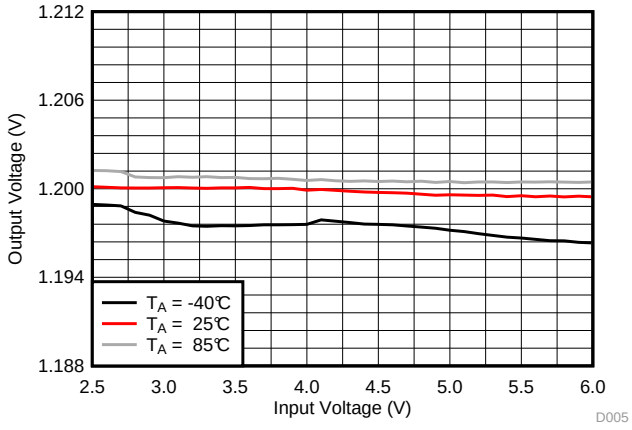
V_{OUT} = 3.3 V

図 7. Efficiency



V_{OUT} = 1.8 V

図 8. Efficiency



I_{OUT} = 1 A

図 9. Line Regulation

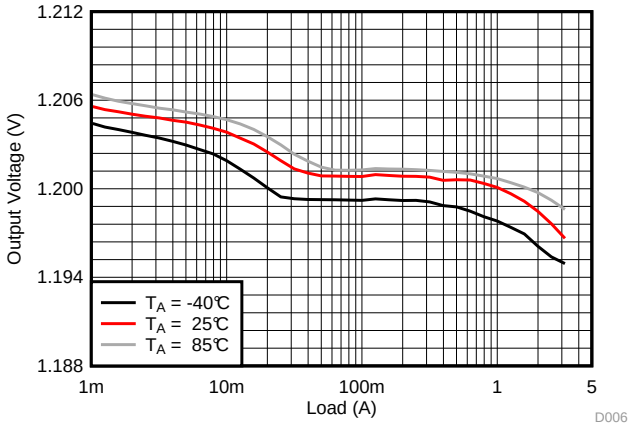
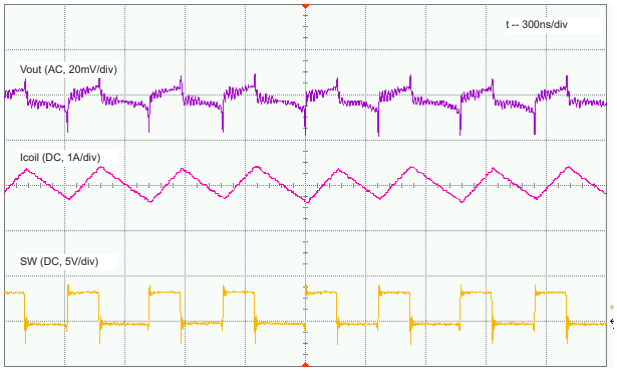
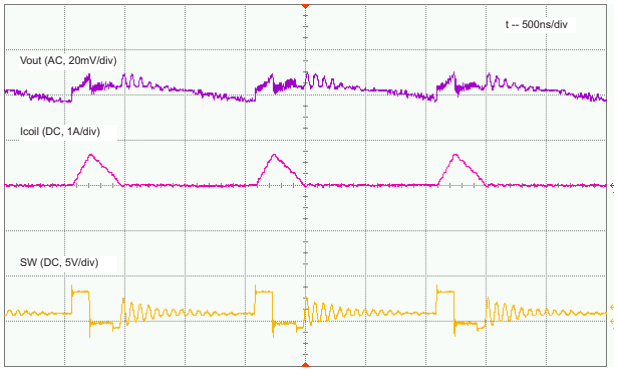


図 10. Load Regulation



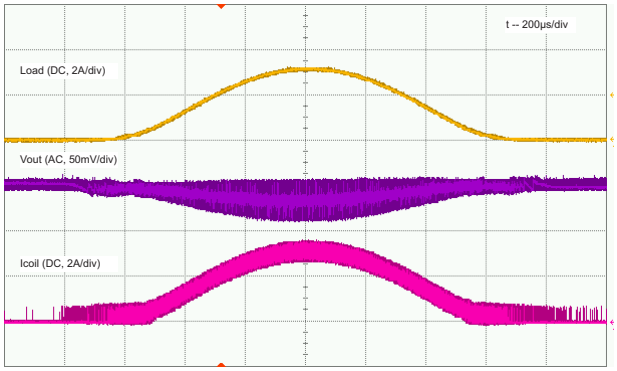
I_{OUT} = 3 A V_{OUT} = 1.2 V

図 11. PWM Operation



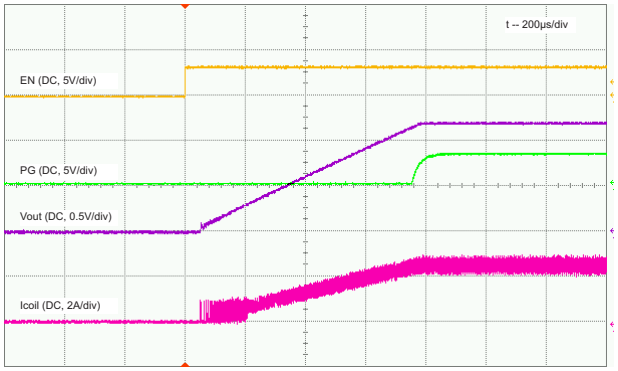
I_{OUT} = 0.1 A V_{OUT} = 1.2 V

図 12. PFM Operation



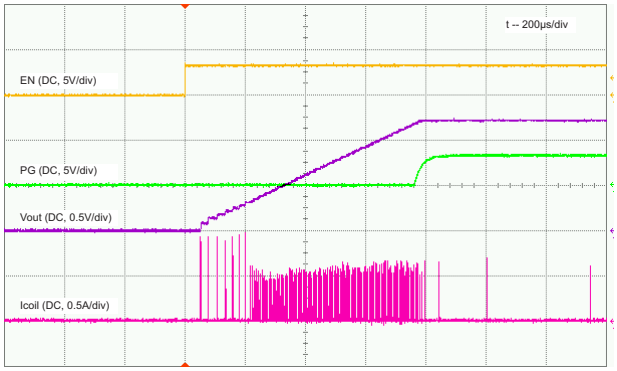
I_{OUT} = 0 A to 3 A V_{OUT} = 1.2 V

図 13. Load Sweep



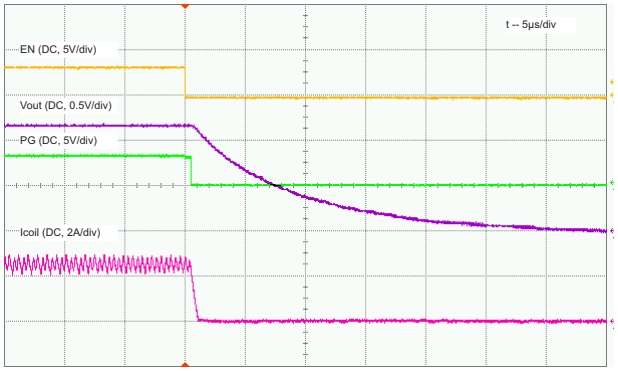
R_{OUT} = 0.47 Ω V_{OUT} = 1.2 V

図 14. Start-Up with Load



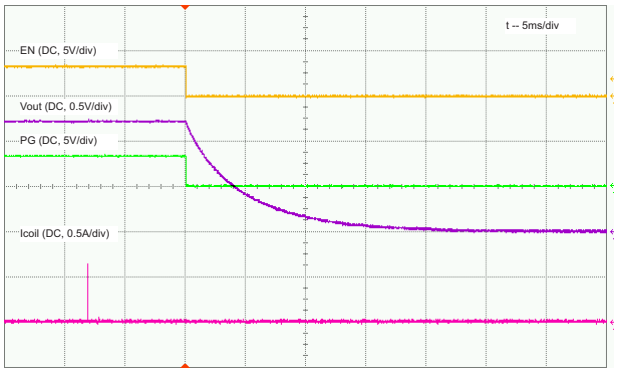
V_{OUT} = 1.2 V

図 15. Start-Up without Load



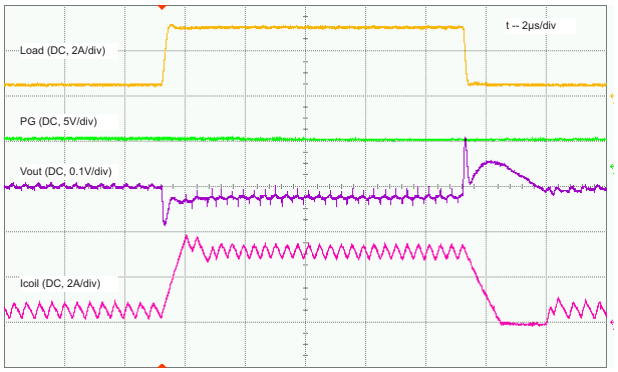
R_{OUT} = 0.47 Ω V_{OUT} = 1.2 V

図 16. Shutdown with Load



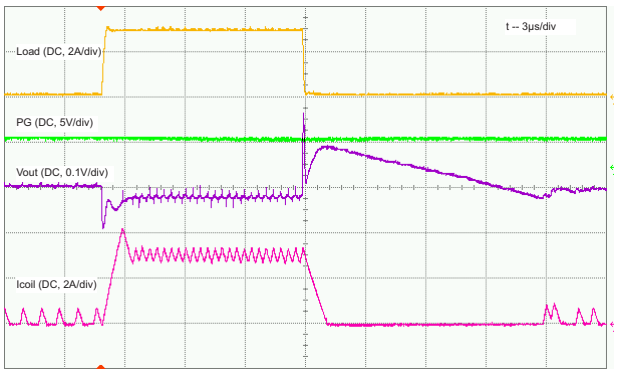
V_{OUT} = 1.2 V

図 17. Shutdown without Load



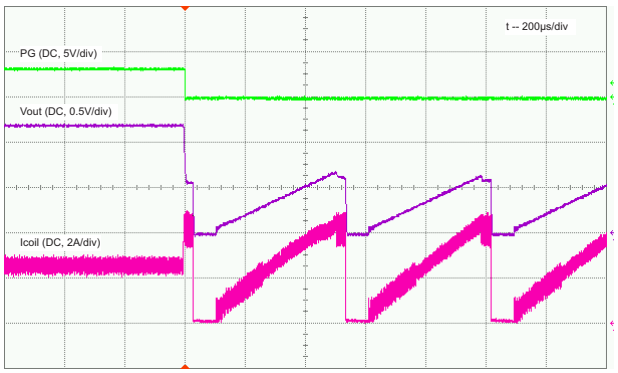
I_{OUT} = 0.5 A to 3 A V_{OUT} = 1.2 V

図 18. Load Transient



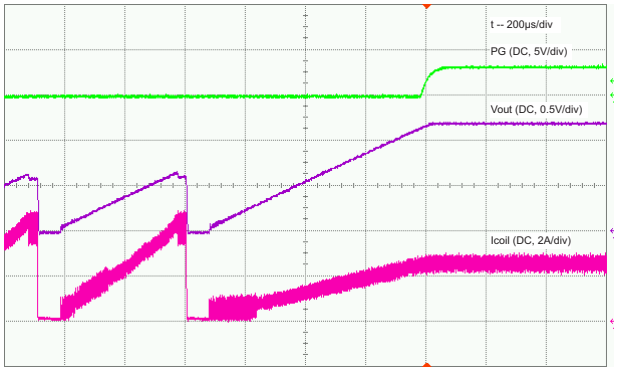
I_{OUT} = 50mA to 3A V_{OUT} = 1.2 V

図 19. Load Transient



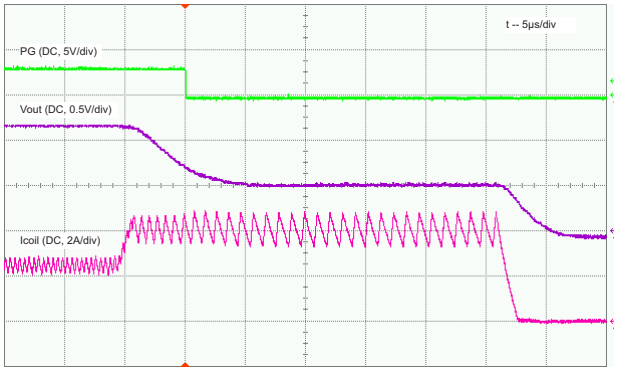
R_{OUT} = 0.47 Ω V_{OUT} = 1.2 V

図 20. Output Short-Circuit Protection, Entry



R_{OUT} = 0.47 Ω V_{OUT} = 1.2 V

図 21. Output Short-Circuit Protection, Recovery



R_{OUT} = 0.47 Ω V_{OUT} = 1.2 V

図 22. Output Short-Circuit Protection, HICCUP Zoom In

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 2.5 V to 6 V. Ensure that the input power supply has a sufficient current rating for the application.

10 Layout

10.1 Layout Guidelines

The printed-circuit-board (PCB) layout is an important step to maintain the high performance of the TLV62085 device.

The input and output capacitors and the inductor must be placed as close as possible to the IC. This keeps the traces short. Routing these traces direct and wide results in low trace resistance and low parasitic inductance. The low side of the input and output capacitors must be connected directly to the GND pin to avoid a ground potential shift. The sense traces connected to FB and VOS pins are signal traces. Special care must be taken to avoid noise being induced. By a direct routing, parasitic inductance can be kept small. GND layers might be used for shielding. Keep these traces away from SW nodes. See 図 23 for the recommended PCB layout.

10.2 Layout Example

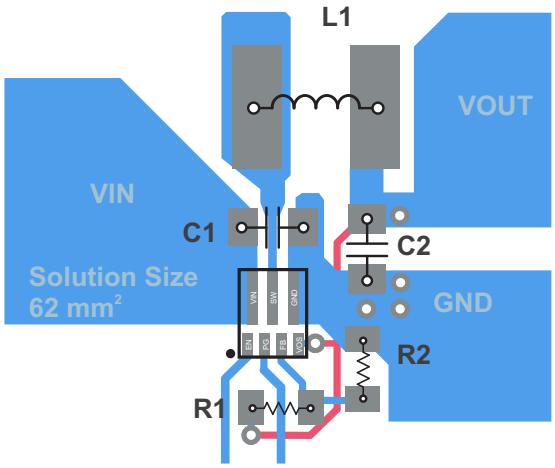


図 23. PCB Layout Recommendation

10.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power dissipation limits of a given component.

Two basic approaches for enhancing thermal performance are:

- Improving the power dissipation capability of the PCB design
- Introducing airflow in the system

The big copper planes connecting to the pads of the IC on the PCB improve the thermal performance of the device. For more details on how to use the thermal parameters, see the *Thermal Characteristics Application Notes*, SZZA017 and SPRA953.

11 デバイスおよびドキュメントのサポート

11.1 開発サポート

11.1.1 WEBENCH®ツールによるカスタム設計

ここをクリックすると、WEBENCH® Power Designerにより、TLV62085デバイスを使用するカスタム設計を作成できます。

1. 最初に、V_{IN}、V_{OUT}、I_{OUT}の要件を入力します。
2. 設計で効率、占有面積、コストなどの主要パラメータを最適化するため、オプティマイザのダイヤルを使用し、この設計と、テキサス・インスツルメンツによる他の可能なソリューションとを比較します。
3. WEBENCH Power Designerでは、カスタマイズされた回路図と部品リストを、リアルタイムの価格や部品の在庫情報と併せて参照できます。
4. ほとんどの場合、次の操作も実行できます。
   - 電気的なシミュレーションを実行し、重要な波形と回路の性能を確認する。
   - 熱的なシミュレーションを実行し、基板の熱特性を把握する。
   - カスタマイズされた回路図やレイアウトを、一般的なCADフォーマットでエクスポートする。
   - 設計のレポートをPDFで印刷し、同僚と設計を共有する。
5. WEBENCHツールの詳細は、www.ti.com/WEBENCHでご覧になれます。

11.1.2 デベロッパー・ネットワークの製品に関する免責事項

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11.2 ドキュメントのサポート

11.2.1 関連資料

関連資料については、以下を参照してください。

- 『熱特性についてのアプリケーション・ノート』、SZZA017
- 『熱特性についてのアプリケーション・ノート』、SPRA953

11.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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設計サポート ***TIの設計サポート*** **役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。**

11.5 Trademarks

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11.6 Electrostatic Discharge Caution

これらのデバイスは、限定的なESD（静電破壊）保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV62085RLTR	Active	Production	VSON-HR (RLT) | 7	3000 | LARGE T&R	Yes	Call TI | Sn | Matte Sn	Level-1-260C-UNLIM	-40 to 125	12Q5
TLV62085RLTR.A	Active	Production	VSON-HR (RLT) | 7	3000 | LARGE T&R	Yes	MATTE SN	Level-1-260C-UNLIM	-40 to 125	12Q5
TLV62085RLTR.B	Active	Production	VSON-HR (RLT) | 7	3000 | LARGE T&R	Yes	MATTE SN	Level-1-260C-UNLIM	-40 to 125	12Q5
TLV62085RLTT	Active	Production	VSON-HR (RLT) | 7	250 | SMALL T&R	Yes	Call TI | Sn | Matte Sn	Level-1-260C-UNLIM	-40 to 125	12Q5
TLV62085RLTT.A	Active	Production	VSON-HR (RLT) | 7	250 | SMALL T&R	Yes	MATTE SN	Level-1-260C-UNLIM	-40 to 125	12Q5
TLV62085RLTT.B	Active	Production	VSON-HR (RLT) | 7	250 | SMALL T&R	Yes	MATTE SN	Level-1-260C-UNLIM	-40 to 125	12Q5

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

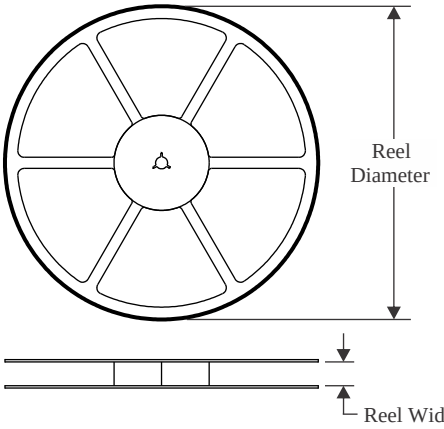
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

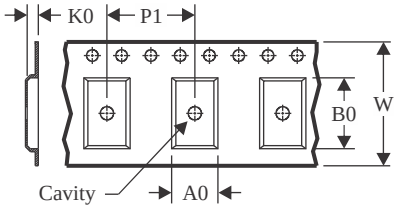
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

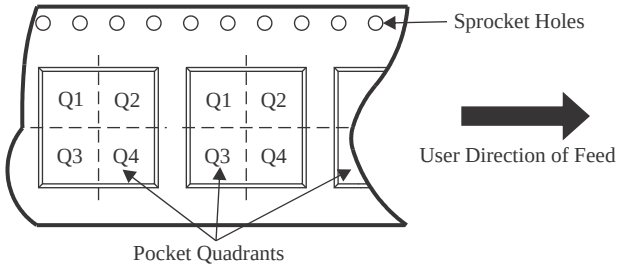


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

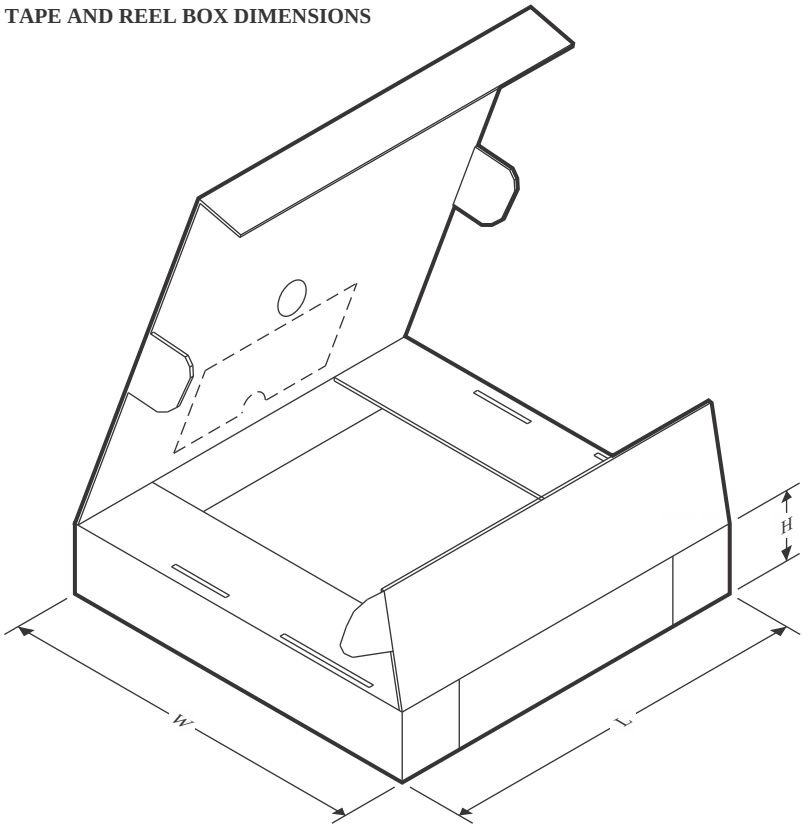
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV62085RLTR	VSON-HR	RLT	7	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV62085RLTT	VSON-HR	RLT	7	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

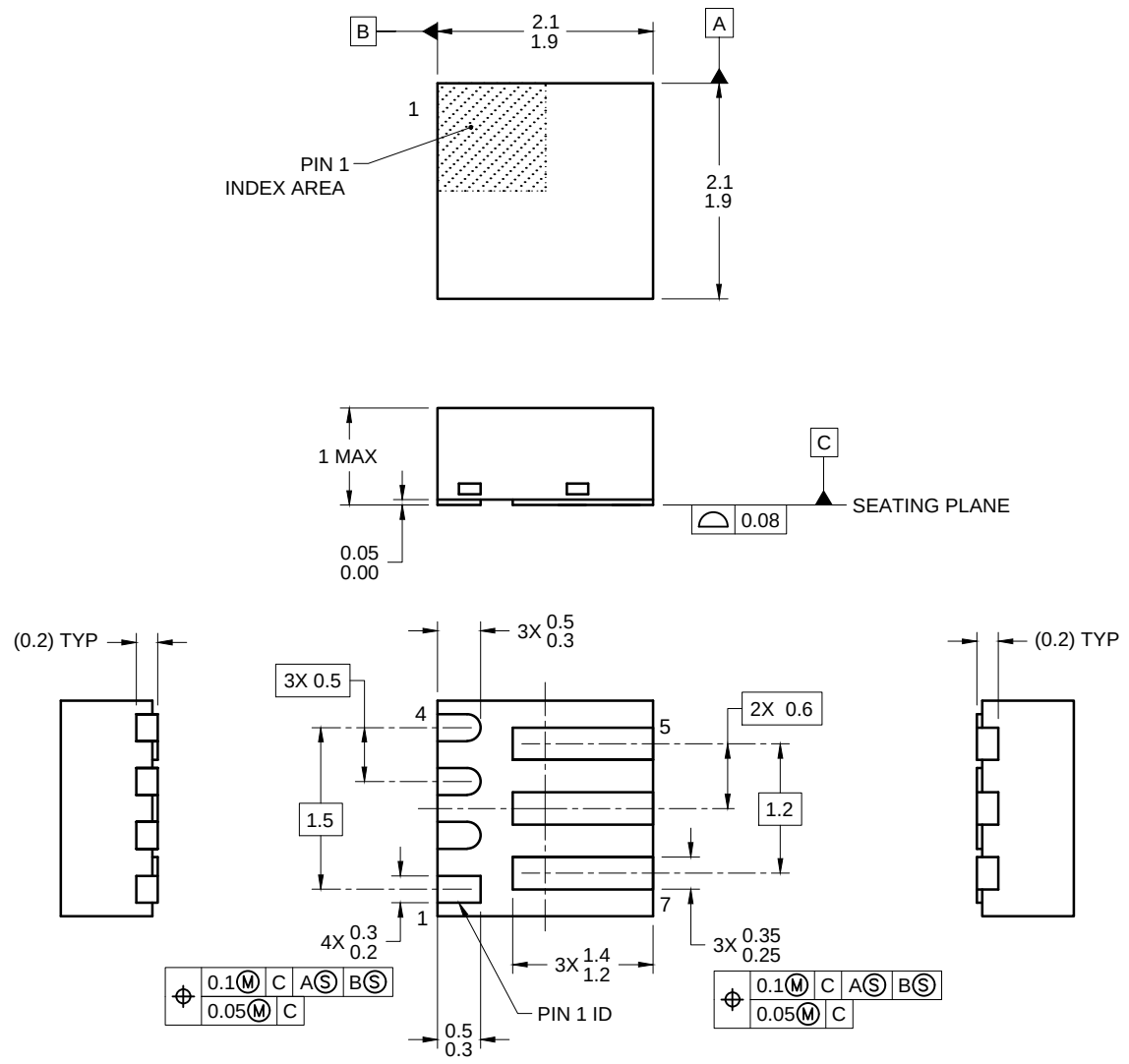
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV62085RLTR	VSON-HR	RLT	7	3000	210.0	185.0	35.0
TLV62085RLTT	VSON-HR	RLT	7	250	210.0	185.0	35.0

PACKAGE OUTLINE

RLT0007A

VSON - 1 mm max height

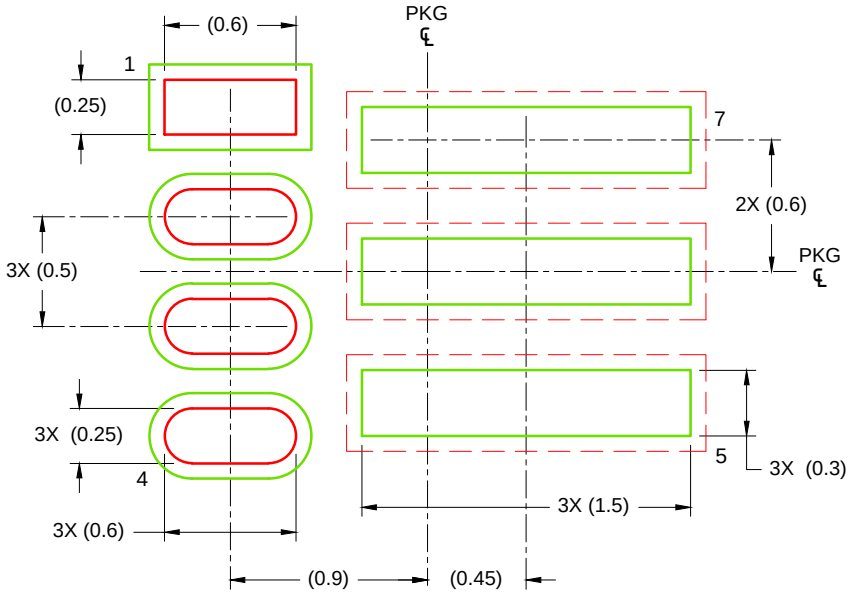
PLASTIC SMALL OUTLINE - NO LEAD



4220429/A 09/2014

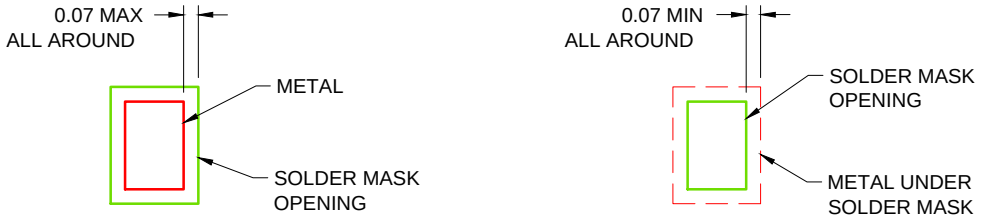
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE

SCALE: 30X



NON SOLDER MASK
DEFINED
PADS 1 - 4

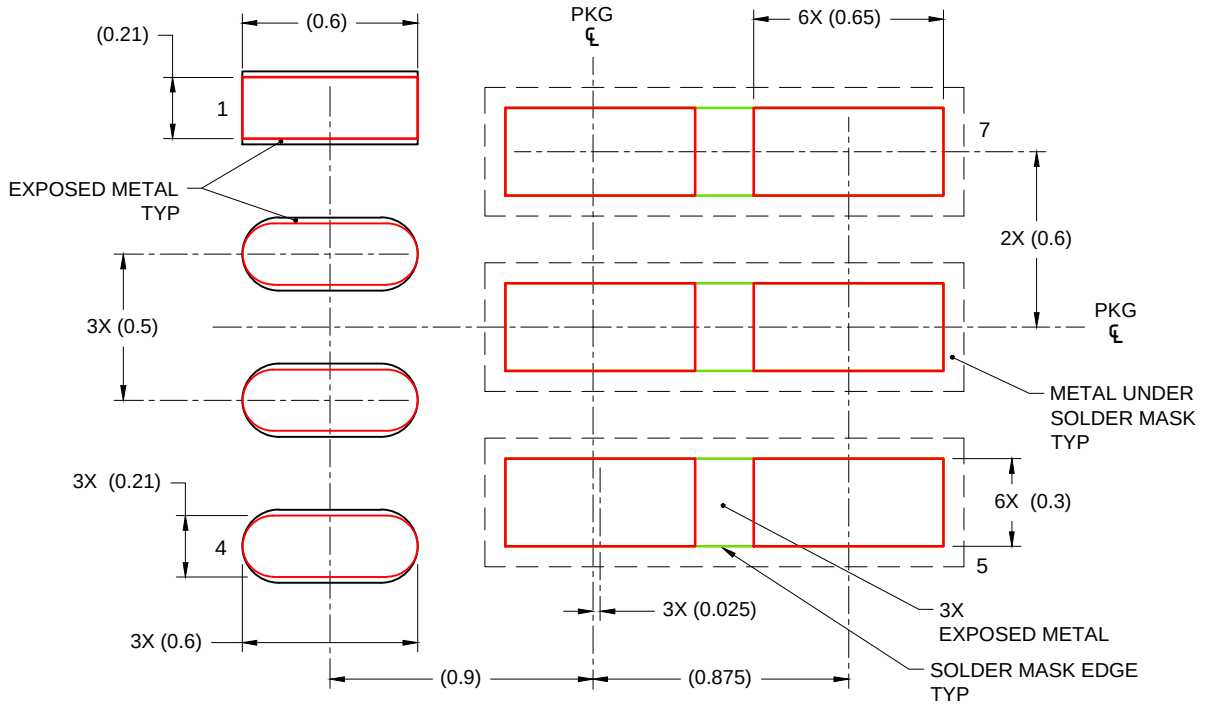
SOLDER MASK
DEFINED
PADS 5 - 7

SOLDER MASK DETAILS

4220429/A 09/2014

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
5. Vias should not be placed on soldering pads unless they are plugged or plated shut.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

FOR ALL EXPOSED PADS
85% PRINTED SOLDER COVERAGE BY AREA
SCALE: 40X

4220429/A 09/2014

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

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