TEXAS INSTRUMENTS
TLV61046A
JAJSD44B – APRIL 2017 – REVISED FEBRUARY 2021

# TLV61046A 昇圧型コンバータ、出力電圧 28V、パワー・ダイオード / 絶縁スイッチ内蔵

## 1 特長

- 入力電圧範囲:1.8V～5.5V、スタートアップ後は最低 1.6V
- 出力電圧:最大 28V
- パワー・ダイオードと絶縁スイッチを搭載
- 980mA (標準) のスイッチ電流
- 3.6V 入力 / 12V 出力での効率:最大 85%
- ±2.5% の出力電圧精度
- 軽負荷時のパワーセーブ動作モード
- 7ms の内部ソフトスタート時間
- シャットダウン時に入力と出力を完全に切り離し
- 出力短絡保護
- 出力過電圧保護
- サーマル・シャットダウン保護機能
- 3mm×3mm SOT23-6 パッケージ
- WEBENCH® Power Designer により TLV61046A を使用するカスタム設計を作成

## 2 アプリケーション

- PMOLED 電源
- LCD パネル
- ウェアラブル機器
- 携帯医療機器
- センサの電源

## 3 概要

TLV61046A は、PMOLED パネル、LCD バイアス電源、センサ・モジュールなどのアプリケーションのために設計された、高集積の昇圧コンバータです。TLV61046A には、30V パワー・スイッチ、入出力絶縁スイッチ、整流ダイオードが内蔵されています。1 つのリチウムイオン電池または直列接続された 2 つのアルカリ電池の入力から最大 28V の電圧を出力できます。

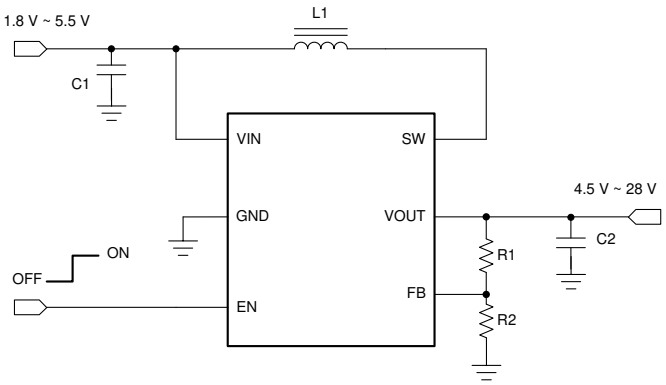
TLV61046A は 1.0MHz のスイッチング周波数で動作します。これにより、小さな外付け部品を使用できます。TLV61046A には、FB ピンを VIN ピンに接続することで、内部で出力電圧をデフォルトの 12V に設定できる機能があります。このように、12V の出力電圧を得るためにわずか 3 つの外部部品しか必要としません。TLV61046A には、標準 980mA のスイッチ電流制限があります。突入電流を低減させるため、7ms のソフトスタート時間が組み込まれています。TLV61046A がシャットダウン・モードのとき、絶縁スイッチは出力を入力から切り離して、リーク電流を最小限にします。また、TLV61046A には出力短絡保護、出力過電圧保護、サーマル・シャットダウンも実装されています。

TLV61046A は 6 ピン 3mm × 3mm SOT23-6 パッケージで供給されます。

**製品情報** (1)

| 部品番号 | パッケージ | 本体サイズ (公称) |
|---|---|---|
| TLV61046A | SOT23-6 (6) | 2.9mm×1.6mm |

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。




**概略回路図**

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**Changes from Revision A (April 2017) to Revision B (February 2021)** — **Page**

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- 文法と記数法を訂正 ... 1
- WEBENCH のリンクを追加 ... 1

**Changes from Revision * (April 2017) to Revision A (April 2017)** — **Page**

- ステータスを「量産データ」に変更 ... 1

# 5 Pin Configuration and Functions

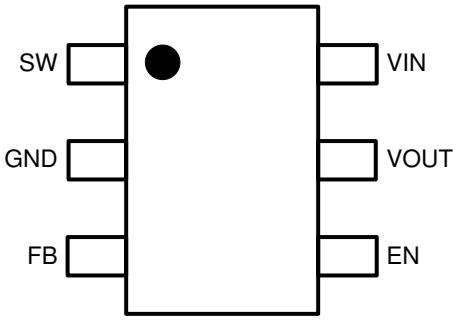



**図 5-1. DBV Package 6-Pin SOT23 Top View**

**表 5-1. Pin Functions**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NUMBER | | |
| SW | 1 | PWR | The switch pin of the converter. It is connected to the drain of the internal power MOSFET. |
| GND | 2 | PWR | Ground |
| FB | 3 | I | Voltage feedback of adjustable output voltage. Connected to the center tap of a resistor divider to program the output voltage. When it is connected to the VIN pin, the output voltage is set to 12 V by an internal feedback. |
| EN | 4 | I | Enable logic input. Logic high voltage enables the device. Logic low voltage disables the device and turns it into shutdown mode. |
| VOUT | 5 | PWR | Output of the boost converter |
| VIN | 6 | I | IC power supply input |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage range at terminals (2) | VIN, EN, FB | – 0.3 | 6 | V |
| | SW, VOUT | –0.3 | 32 | V |
| Operating junction temperature range, $T_J$ | | –40 | 150 | °C |
| Storage temperature range, $T_{stg}$ | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ (1) | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(2) | ±2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(3) | ±500 | V |

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage range | 1.8 | | 5.5 | V |
| $V_{OUT}$ | Output voltage range | 3.3 | | 28 | V |
| L | Effective inductance range | 2.2×0.7 | 10 | 22×1.3 | µH |
| $C_{IN}$ | Effective input capacitance range | 0.22 | 1.0 | | µF |
| $C_{OUT}$ | Effective output capacitance range | 0.22 | 1.0 | 10 | µF |
| $T_J$ | Operating junction temperature | –40 | | 125 | °C |

## 6.4 Thermal Information

| THERMAL METRIC(1) | | TLV61046A DBV (SOT23) 6 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 177.7 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 120.6 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 33.2 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 21.5 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 32.6 | |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | n/a | |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

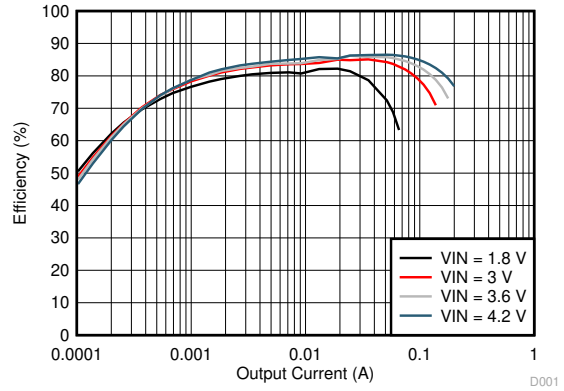
## 6.5 Electrical Characteristics

$T_A$ = –40°C to 85°C, $V_{IN}$ = 3.6 V and $V_{OUT}$ = 12 V. Typical values are at $T_A$ = 25°C, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| POWER SUPPLY | | | | | | |
| $V_{IN}$ | Input voltage range | | 1.8 | | 5.5 | V |
| $V_{IN\_UVLO}$ | Under voltage lockout threshold | $V_{IN}$ rising | | 1.75 | 1.8 | V |
| | | $V_{IN}$ falling | | 1.55 | 1.6 | |
| $V_{IN\_HYS}$ | VIN UVLO hysteresis | | | 200 | | mV |
| $I_{Q\_VIN}$ | Quiescent current into VIN pin | IC enabled, no load, no switching, $V_{IN}$ = 1.8 V to 5.5 V, $V_{OUT}$ = 12 V | | 110 | 200 | µA |
| $I_{SD}$ | Shutdown current into VIN pin | IC disabled, $V_{IN}$ = 1.8 V to 5.5 V, $T_A$ = 25°C | | 0.1 | 1.0 | µA |
| OUTPUT | | | | | | |
| $V_{OUT}$ | Output voltage range | | 3.3 | | 28 | V |
| $V_{OUT\_12V}$ | 12-V output voltage accuracy | FB pin connected to VIN pin, $T_J$=0°C to 125°C | 11.7 | 12.1 | 12.4 | V |
| $V_{REF}$ | Feedback voltage | PWM mode, $T_A$=25°C | 0.783 | 0.795 | 0.807 | V |
| | | PWM mode, $T_J$=-40°C to 125°C | 0.775 | 0.795 | 0.815 | V |
| | | PFM mode, $T_A$=25°C | | 0.803 | | V |
| $V_{OVP}$ | Output overvoltage protection threshold | | 28 | 29.2 | 30.4 | V |
| $V_{OVP\_HYS}$ | Over voltage protection hysteresis | | | 0.9 | | V |
| $I_{FB\_LKG}$ | Leakage current into FB pin | $T_A$ = 25°C | | | 200 | nA |
| $I_{SW\_LKG}$ | Leakage current into SW pin | IC disabled, $T_A$ = 25°C | | | 500 | nA |
| POWER SWITCH | | | | | | |
| $R_{DS(on)}$ | Isolation MOSFET on resistance | $V_{OUT}$ = 12 V | | 850 | | mΩ |
| | Low-side MOSFET on resistance | $V_{OUT}$ = 12 V | | 450 | | |
| $f_{SW}$ | Switching frequency | $V_{IN}$ = 3.6 V, $V_{OUT}$ = 12 V, PWM mode | 850 | 1050 | 1250 | kHz |
| $t_{ON\_min}$ | Minimal switch on time | | | 150 | 250 | ns |
| $I_{LIM\_SW}$ | Peak switch current limit | $V_{IN}$ = 3.6 V, $V_{OUT}$ = 12 V | 680 | 980 | 1250 | mA |
| | | $V_{IN}$ = 2.4 V, $V_{OUT}$ = 3.3 V | 20 | | | mA |
| $I_{LIM\_CHG}$ | Pre-charge current | $V_{IN}$ = 3.6 V, $V_{OUT}$ = 0 V | | 30 | 50 | mA |
| $t_{STARTUP}$ | Startup time | $V_{OUT}$ from $V_{IN}$ to 12 V, $C_{OUT\_effective}$ = 2.2 µF, $I_{OUT}$ = 0 A | 2 | 5 | | ms |
| LOGIC INTERFACE | | | | | | |
| $V_{EN\_H}$ | EN Logic high threshold | | | | 1.2 | V |
| $V_{EN\_L}$ | EN Logic Low threshold | | 0.4 | | | V |
| PROTECTION | | | | | | |
| $T_{SD}$ | Thermal shutdown threshold | $T_J$ rising | | 150 | | °C |
| $T_{SD\_HYS}$ | Thermal shutdown hysteresis | $T_J$ falling below $T_{SD}$ | | 20 | | °C |

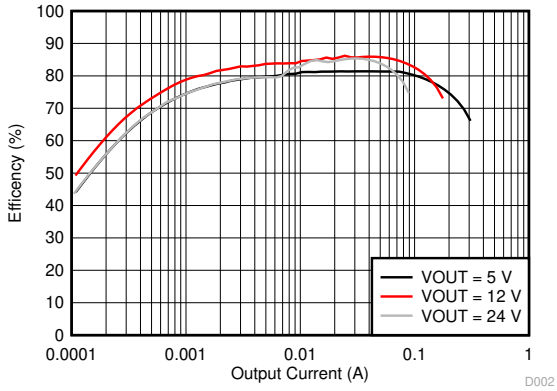
## 6.6 Typical Characteristics

$V_{IN}$ = 3.6 V, $V_{OUT}$ = 12 V, $T_A$ = 25°C, unless otherwise noted.



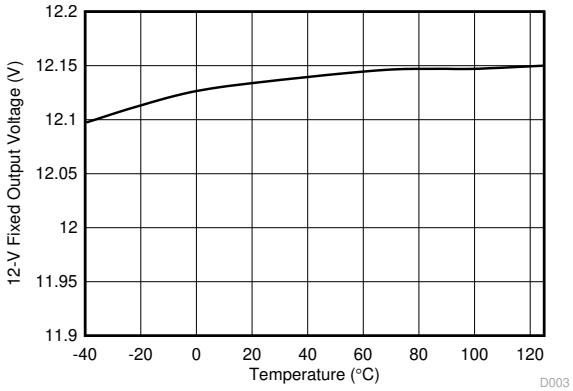

$V_{OUT}$ = 12 V

**図 6-1. Efficiency vs Output Current**



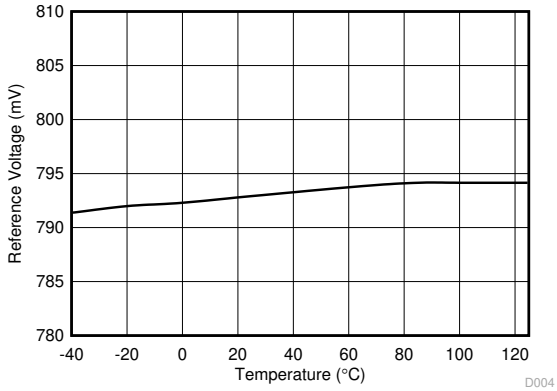

$V_{IN}$ = 3.6 V

**図 6-2. Efficiency vs Output Current**



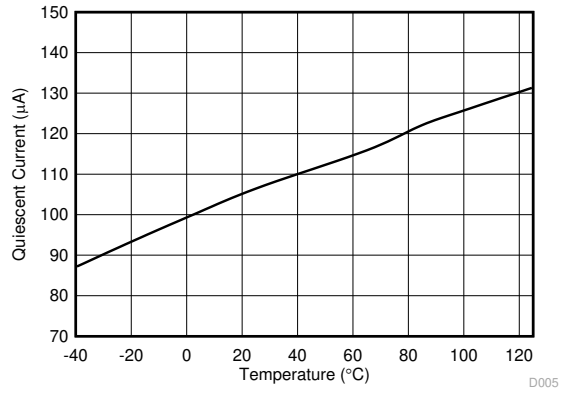

$V_{IN}$ = 3.6 V, $V_{OUT}$ = 12 V, FB pin connected to VIN pin, PWM mode

**図 6-3. 12-V Fixed Output Voltage vs Temperature**



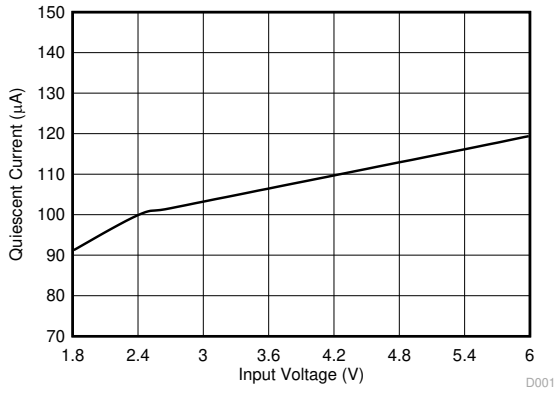

$V_{IN}$ = 3.6 V, $V_{OUT}$ = 12 V, PWM mode

**図 6-4. FB Reference Voltage vs Temperature**




$V_{IN}$ = 3.6 V, $V_{OUT}$ = 12 V, No switching

**図 6-5. Quiescent Current into VIN vs Temperature**

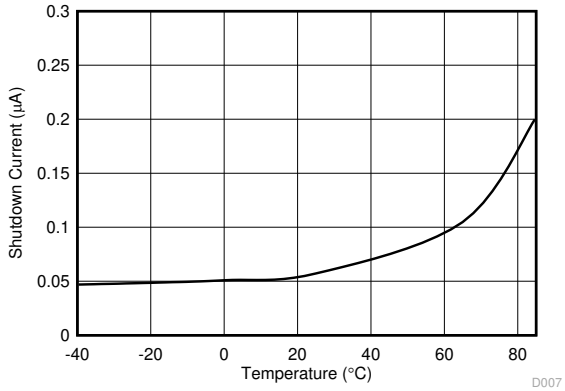



$V_{IN}$ = 1.8 V ~ 6 V, $V_{OUT}$ = 12 V, No switching

**図 6-6. Quiescent Current into VIN vs Input Voltage**

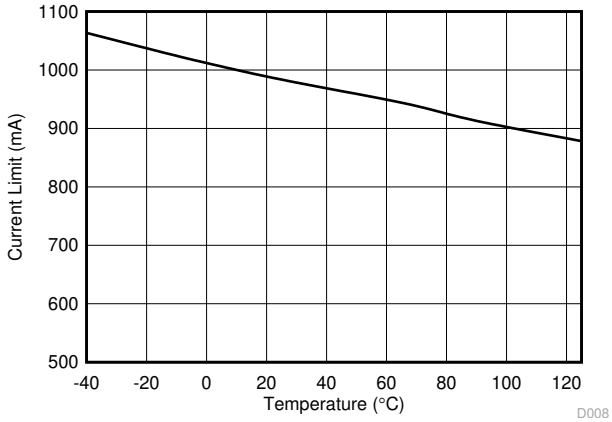
## 6.6 Typical Characteristics (continued)

$V_{IN}$ = 3.6 V, $V_{OUT}$ = 12 V, $T_A$ = 25°C, unless otherwise noted.



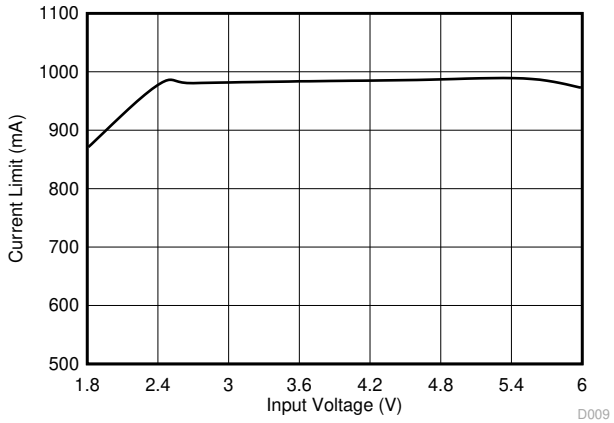

$V_{IN}$ = 3.6 V

**図 6-7. Shutdown Current vs Temperature**




$V_{IN}$ = 3.6 V, $V_{OUT}$ = 12 V

**図 6-8. Current Limit vs Temperature**




$V_{IN}$ = 1.8 V ~ 6 V, $V_{OUT}$ = 12 V

**図 6-9. Current Limit vs Input Voltage**

# 7 Detailed Description

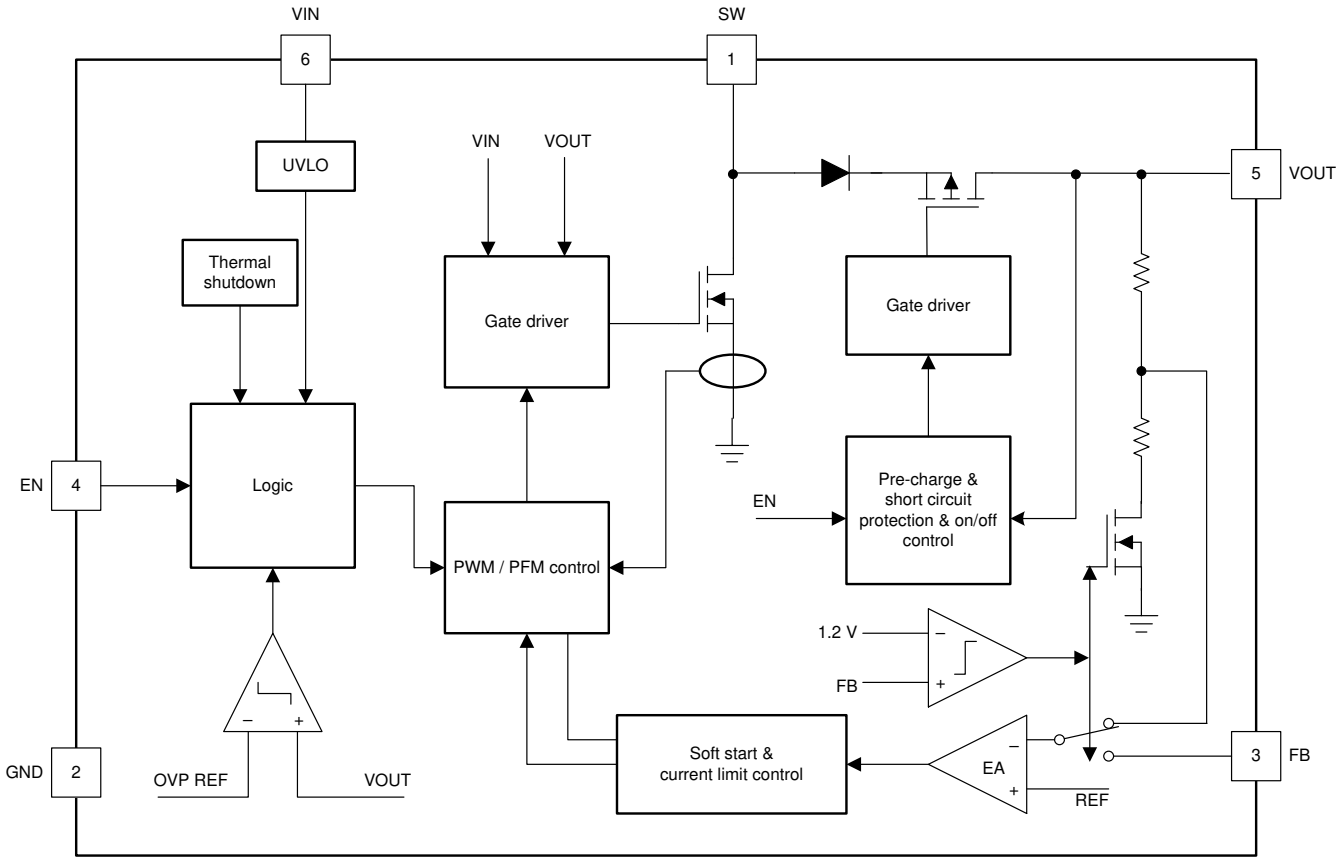
## 7.1 Overview

The TLV61046A is a highly-integrated boost converter designed for applications requiring high voltage and small solution size such as PMOLED panel power supply and sensor module. The TLV61046A integrates a 30-V power switch, an input to output isolation switch, and a rectifier diode. It can output up to 28 V from input of a Li+ battery or two-cell alkaline batteries in series.

One common issue with conventional boost regulators is the conduction path from input to output even when the power switch is turned off. It creates three problems, which are inrush current during start-up, output leakage current during shutdown, and excessive over load current. In the TLV61046A, the isolation switch is turned off under shutdown mode and over load conditions, thereby opening the current path. Thus, the TLV61046A can truely disconnect the load from the input voltage and minimize the leakage current during shutdown mode.

The TLV61046A operates with a switching frequency at 1.0 MHz. This allows the use of small external components. The TLV61046A has an internal default 12-V output voltage setting by connecting the FB pin to the VIN pin. Thus, it only needs three external components to get 12-V output voltage. The TLV61046A has typical 980-mA switch current limit. It has 7-ms built-in soft start time to minimize the inrush current. The TLV61046A also implements output short circuit protection, output overvoltage protection, and thermal shutdown.

## 7.2 Functional Block Diagram




## 7.3 Feature Description

### 7.3.1 Undervoltage Lockout

An undervoltage lockout (UVLO) circuit stops the operation of the converter when the input voltage drops below the typical UVLO threshold of 1.55 V. A hysteresis of 200 mV is added so that the device cannot be enabled again until the input voltage goes up to 1.75 V. This function is implemented in order to prevent malfunctioning of the device when the input voltage is between 1.55 V and 1.75 V.

### 7.3.2 Enable and Disable

When the input voltage is above the maximal UVLO rising threshold of 1.8 V and the EN pin is pulled high, the TLV61046A is enabled. When the EN pin is pulled low, the TLV61046A goes into shutdown mode. The device stops switching and the isolation switch is turned off, providing the isolation between input and output. In shutdown mode, less than 1-µA input current is consumed.

### 7.3.3 Soft Start

The TLV61046A begins soft start when the EN pin is pulled high. At the beginning of the soft start period, the isolation FET is turned on slowly to charge the output capacitor with 30-mA current for about 2 ms. This is called the pre-charge phase. After the pre-charge phase, the TLV61046A starts switching. This is called switching soft-start phase. An internal soft start circuit limits the peak inductor current according to the output voltage. When the output voltage is below 3 V, the peak inductor current is limited to 140 mA. Along with the output voltage going up from 3 V to 5 V, the peak current limit is gradually increased to the normal value of 980 mA. The switching soft start phase is about 5 ms typically. The soft start funciton reduces the inrush current during start-up.

### 7.3.4 Overvoltage Protection

The TLV61046A has internal output overvoltage protection (OVP) function. When the output voltage exceeds the OVP threshold of 29.2 V, the device stops switching. Once the output voltage falls 0.9 V below the OVP threshold, the device resumes operation again.

### 7.3.5 Output Short Circuit Protection

The TLV61046A starts to limit the output current whenever the output voltage drops below 4 V. The lower output voltage, the smaller output current limit. When the VOUT pin is shorted to ground, the output current is limited to less than 200 mA. This function protects the device from being damaged when the output is shorted to ground.

### 7.3.6 Thermal Shutdown

The TLV61046A goes into thermal shutdown once the junction temperature exceeds the thermal shutdown termperature threshold of 150°C typically. When the junction temperature drops below 130°C typically, the device starts operating again.

## 7.4 Device Functional Modes

The TLV61046A has two operation modes, PWM mode and power save mode.

### 7.4.1 PWM Mode

The TLV61046A uses a quasi-constant 1.0-MHz frequency pulse width modulation (PWM) at moderate to heavy load current. Based on the input voltage-to-output votlage ratio, a circuit predicts the required off-time. At the beginning of the switching cycle, the NMOS switching FET, shown in the functional block diagram, is turned on. The input voltage is applied across the inductor and the inductor current ramps up. In this phase, the output capacitor is discharged by the load current. When the inductor current hits the current threshold that is set by the output of the error amplifier, the PWM switch is turned off, and the power diode is forward-biased. The inductor transfers its stored energy to replenish the output capacitor and supply the load. When the off-time is expired, the next switching cycle starts again. The error amplifier compares the FB pin voltage with an internal reference votlage, and its output determines the inductor peak current.

The TLV61046A has a built-in compensation circuit that can accommodate a wide range of input voltage, output voltage, inductor value, and output capacitor value for stable operation.

### 7.4.2 Power Save Mode

The TLV61046A implements a power save mode with pulse frequency modulation (PFM) to improve efficiency at light load. When the load current decreases, the inductor peak current set by the output of the error amplifier declines to regulate the output voltage. When the inductor peak current hits the low limit of 200 mA, the output voltage will exceed the setting voltage as the load current decreases further. When the FB voltage hits the PFM reference voltage, the TLV61046A goes into power save mode. In power save mode, when the FB voltage rises and hits the PFM reference voltage, the device continues switching for several cycles because of the delay time

of the internal comparator, then it stops switching. The load is supplied by the output capacitor and the output voltage declines. When the FB voltage falls below the PFM reference voltage, after the delay time of the comparator, the device starts switching again to ramp up the output voltage.

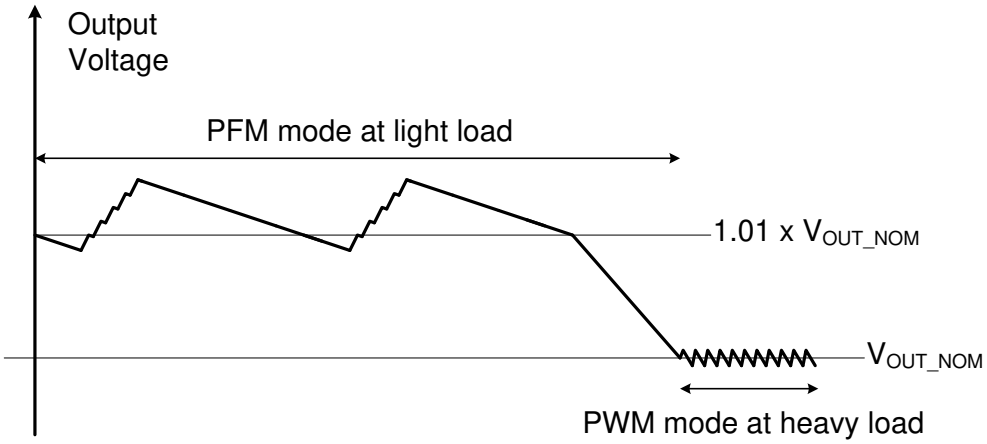



**図 7-1. Output Voltage in PWM Mode and PFM Mode**

# 8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。また、お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

## 8.1 Application Information

The TLV61046A is a boost DC-DC converter integrating a power switch, an input to output isolation switch, and a rectifier diode. The device supports up to 28-V output with the input voltage ranging from 1.8 V to 5.5 V. The TLV61046A adopts the current-mode control with adaptive constant off-time. The switching frequency is quasi-constant at 1.0 MHz. The isolation switch disconnects the output from the input during shutdown to minimize leakage current.

The following design procedure can be used to select component values for the TLV61046A.

## 8.2 Typical Application - 12-V Output Boost Converter

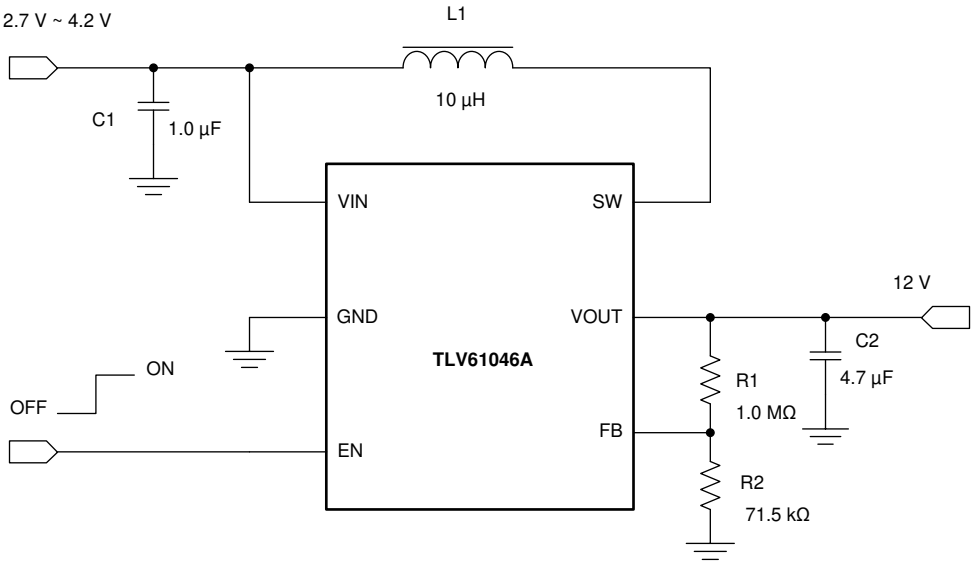



**図 8-1. 12-V Boost Converter**

### 8.2.1 Design Requirements

**表 8-1. Design Requirements**

| PARAMETERS | VALUES |
|---|---|
| Input Voltage | 2.7 V ~ 4.2 V |
| Output Voltage | 12 V |
| Output Current | 50 mA |
| Output Voltage Ripple | ±50 mV |

### 8.2.2 Detailed Design Procedure

#### *8.2.2.1 Custom Design With WEBENCH® Tools*

Click here to create a custom design using the TLV61046A device with the WEBENCH® Power Designer.

1. Start by entering the input voltage ($V_{IN}$), output voltage ($V_{OUT}$), and output current ($I_{OUT}$) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

#### *8.2.2.2 Programming the Output Voltage*

There are two ways to set the output voltage of the TLV61046A. When the FB pin is connected to the input voltage, the output voltage is fixed to 12 V. This function makes the TLV61046A only need three external components to minimize the solution size. The second way is to use an external resistor divider to set the desired output voltage.

By selecting the external resistor divider R1 and R2, as shown in 式 1, the output voltage is programmed to the desired value. When the output voltage is regulated, the typical voltage at the FB pin is $V_{REF}$ of 795 mV.

$$R1 = \left( \frac{V_{OUT}}{V_{REF}} - 1 \right) \times R2 \tag{1}$$

where

- $V_{OUT}$ is the desired output voltage
- $V_{REF}$ is the internal reference voltage at the FB pin

For best accuracy, R2 should be kept smaller than 80 kΩ to ensure the current flowing through R2 is at least 100 times larger than the FB pin leakage current. Changing R2 towards a lower value increases the immunity against noise injection. Changing the R2 towards a higher value reduces the quiescent current for achieving higher efficiency at low load currents.

#### *8.2.2.3 Inductor Selection*

Because the selection of the inductor affects steady state operation, transient behavior, and loop stability, the inductor is the most important component in power regulator design. There are three important inductor specifications, inductor value, saturation current, and dc resistance (DCR).

The TLV61046A is designed to work with inductor values between 2.2 µH and 22 µH. Follow 式 2 to 式 4 to calculate the peak current of the inductor for the application. To calculate the peak current in the worst case, use the minimum input voltage, maximum output voltage, and maximum load current of the application. To have enough design margin, choose the inductor value with -30% tolerance, and a low power-conversion efficiency for the calculation.

In a boost regulator, the inductor dc current can be calculated with 式 2.

$$I_{L(DC)} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \tag{2}$$

where

- $V_{OUT}$ is output voltage
- $I_{OUT}$ is output current
- $V_{IN}$ is input voltage

- η is power conversion efficiency, use 80% for most applications

The inductor ripple current is calculated with 式 3 for an asynchronous boost converter in continuous conduction mode (CCM).

$$\Delta I_{L(P-P)} = \frac{V_{IN} \times (V_{OUT} + 0.8V - V_{IN})}{L \times f_{SW} \times (V_{OUT} + 0.8V)} \quad (3)$$

where

- $\Delta I_{L(P-P)}$ is inductor ripple current
- L is inductor value
- $f_{SW}$ is switching frequency
- $V_{OUT}$ is output voltage
- $V_{IN}$ is input voltage

Therefore, the inductor peak current is calculated with 式 4.

$$I_{L(P)} = I_{L(DC)} + \frac{\Delta I_{L(P-P)}}{2} \quad (4)$$

Normally, it is advisable to work with an inductor peak-to-peak current of less than 40% of the average inductor current for maximum output current. A smaller ripple from a larger valued inductor reduces the magnetic hysteresis losses in the inductor and EMI. But in the same way, load transient response time is increased. Because the TLV61046A is for relatively small output current application, the inductor peak-to-peak current can be as high as 200% of the average current with a small inductor value, which means the TLV61046A always works in DCM mode. 表 8-2 lists the recommended inductors for the TLV61046A.

**表 8-2. Recommended Inductors for the TLV61046A**

| PART NUMBER | L(µH) | DCR MAX (mΩ) | SATURATION CURRENT (A) | SIZE (LxWxH) | VENDOR(1) |
|---|---|---|---|---|---|
| FDSD0420-H-100M | 10 | 200 | 2.5 | 4.2x4.2x2.0 | Toko |
| CDRH3D23/HP | 10 | 198 | 1.02 | 4.0x4.0x2.5 | Sumida |
| 74438336100 | 10 | 322 | 2.35 | 3.2x3.2x2.0 | Wurth |
| VLS4012-4R7M | 4.7 | 132 | 1.1 | 4.0x4.0x1.2 | TDK |

(1) See *Third-party Products Disclaimer*

#### *8.2.2.4 Input and Output Capacitor Selection*

The output capacitor is mainly selected to meet the requirements for output ripple and loop stability. This ripple voltage is related to the capacitance of the capacitor and its equivalent series resistance (ESR). Assuming a ceramic capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated by:

$$C_{OUT} = \frac{I_{OUT} \times D_{MAX}}{f_{SW} \times V_{RIPPLE}} \quad (5)$$

where

- $D_{MAX}$ is maximum switching duty cycle
- $V_{RIPPLE}$ is peak to peak output voltage ripple

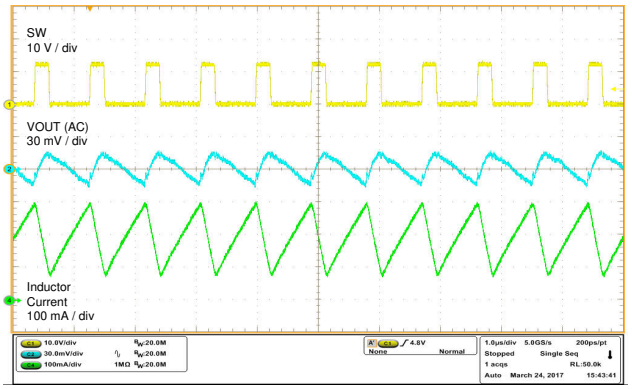
The ESR impact on the output ripple must be considered if tantalum or aluminum electrolytic capacitors are used.

Care must be taken when evaluating a ceramic capacitor's derating under dc bias, aging, and ac signal. For example, the dc bias can significantly reduce capacitance. A ceramic capacitor can lose more than 50% of its capacitance at its rated voltage. Therefore, always leave margin on the voltage rating to ensure adequate capacitance at the required output voltage.

It is recommended to use the output capacitor with effective capacitance in the range of 0.47 µF to 10 µF. The output capacitor affects loop stability of the boost regulator. If the output capacitor is below the range, the boost regulator can potentially become unstable. Increasing the output capacitor makes the output voltage ripple smaller in PWM mode.

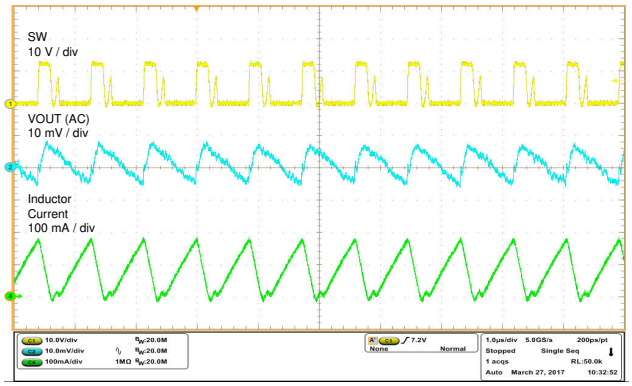
For input capacitor, a ceramic capacitor with more than 1.0 µF is enough for most applications.

### 8.2.3 Application Performance Curves



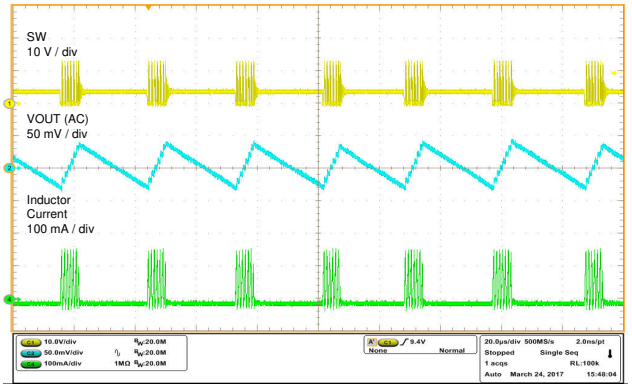

$V_{IN}$ = 3.6 V, $V_{OUT}$ = 12 V, $I_{OUT}$ = 50 mA

**図 8-2. Switching Waveforms in PWM CCM Mode**



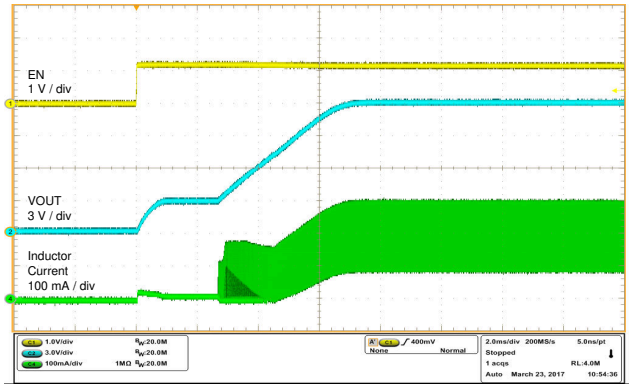

$V_{IN}$ = 3.6 V, $V_{OUT}$ = 12 V, $I_{OUT}$ = 18 mA

**図 8-3. Switching Waveforms in PWM DCM Mode**



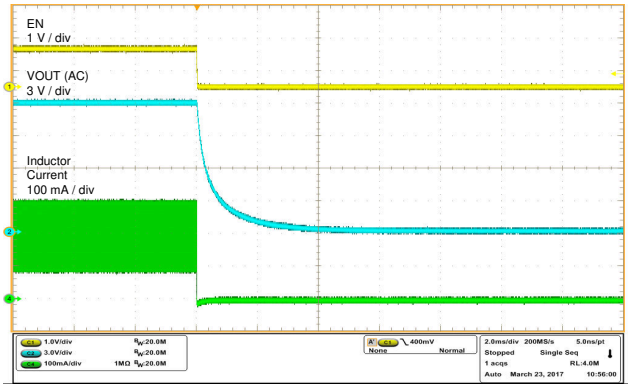

$V_{IN}$ = 3.6 V, $V_{OUT}$ = 12 V, $I_{OUT}$ = 3 mA

**図 8-4. Switching Waveforms in Power Save Mode**



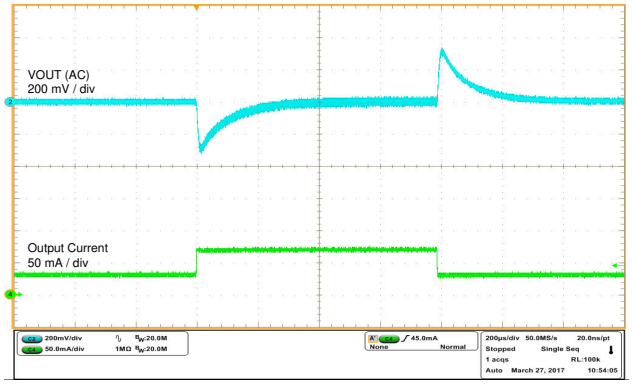

$V_{IN}$ = 3.6 V, $V_{OUT}$ = 12 V, $I_{OUT}$ = 50 mA

**図 8-5. Soft Start-up Waveforms**



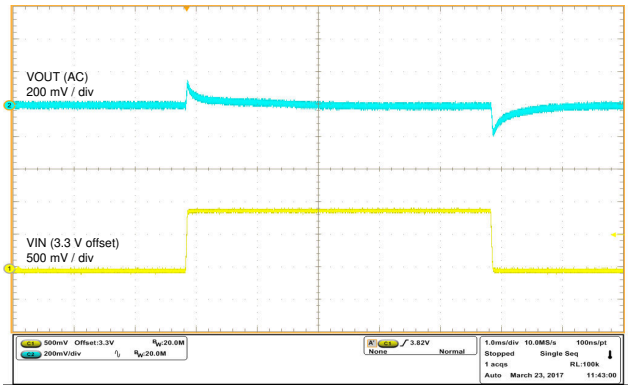

$V_{IN}$ = 3.6 V, $V_{OUT}$ = 12 V, $I_{OUT}$ = 50 mA

**図 8-6. Shutdown Waveforms**




$V_{IN}$ = 3.6 V, $V_{OUT}$ = 12 V

**図 8-7. 30-mA to 70-mA Load Transient Response**




$V_{OUT}$ = 12 V, $I_{OUT}$ = 50 mA

**図 8-8. Input Voltage from 3.3-V to 4.2-V Line Transient Response**

## 8.3 System Examples

### 8.3.1 Fixed 12-V Output Voltage with Three External Components

The TLV61046A can output fixed 12-V voltage by connecting the FB pin to the VIN pin to save the external resistor divider. The 図 8-9 shows the application circuit.

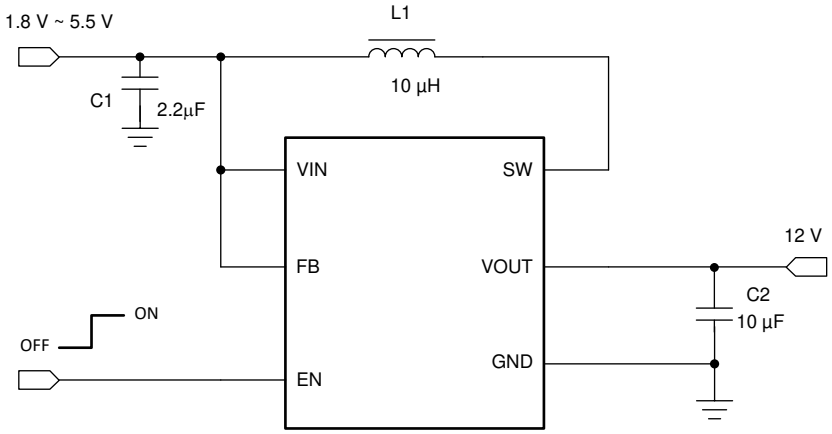



**図 8-9. Fixed 12-V Output Voltage by Connecting the FB Pin to VIN Pin**

## 9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 1.8 V to 5.5 V. This input supply must be well regulated. If the input supply is located more than a few inches from the converter, additional bulk capacitance can be required in addition to the ceramic bypass capacitors. A typical choice is an electrolytic or tantalum capacitor with a value of 47 µF. The output current of the input power supply needs to be rated according to the supply voltage, output voltage, and output current of the TLV61046A.

# 10 Layout

## 10.1 Layout Guidelines

As for all switching power supplies, especially those running at high switching frequency and high currents, layout is an important design step. If the layout is not carefully done, the regulator could suffer from instability and noise problems. To maximize efficiency, switch rise and fall time are very fast. To prevent radiation of high frequency noise (for example, EMI), proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize interplane coupling. The input capacitor needs not only to be close to the VIN pin, but also to the GND pin in order to reduce input supply ripple.

The most critical current path for all boost converters is from the switching FET, through the rectifier diode, then the output capacitors, and back to ground of the switching FET. This high current path contains nanosecond rise and fall time and should be kept as short as possible. Therefore, the output capacitors need not only to be close to the VOUT pin, but also to the GND pin to reduce the overshoot at the SW pin and VOUT pin.

## 10.2 Layout Example

A large ground plane on the bottom layer connects the ground pins of the components on the top layer through vias.

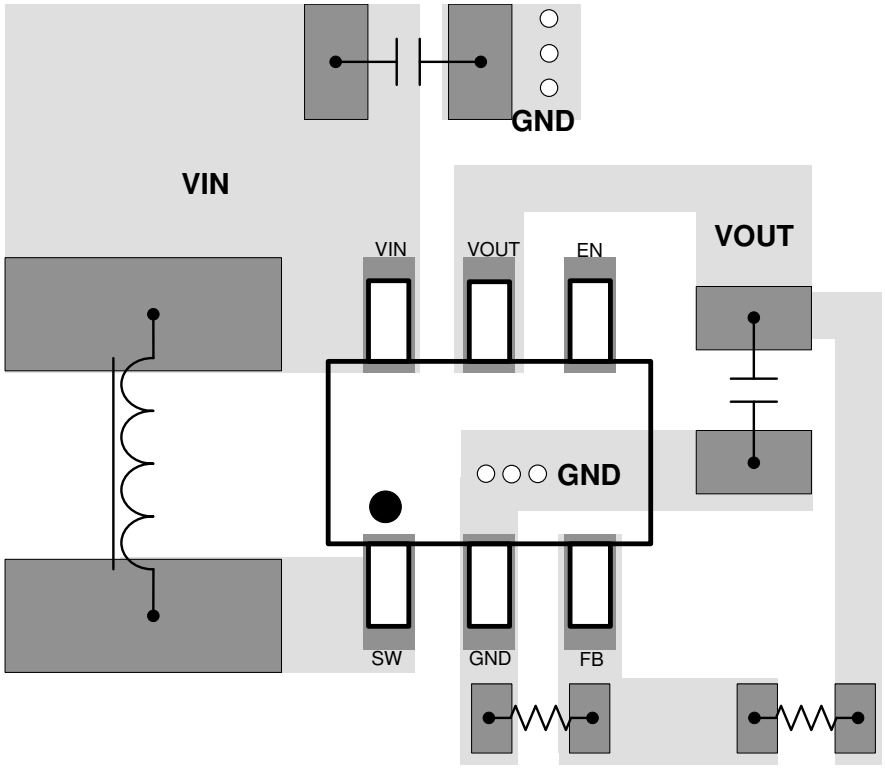



**図 10-1. PCB Layout Example**

# 11 Device and Documentation Support

## 11.1 Device Support

### 11.1.1 Third-Party Products Disclaimer

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### 11.1.2 Development Support

#### *11.1.2.1 Custom Design With WEBENCH® Tools*

Click here to create a custom design using the TLV61046A device with the WEBENCH® Power Designer.

1. Start by entering the input voltage ($V_{IN}$), output voltage ($V_{OUT}$), and output current ($I_{OUT}$) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

## 11.2 ドキュメントの更新通知を受け取る方法

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## 11.3 サポート・リソース

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

## 11.6 用語集

TI 用語集　この用語集には、用語や略語の一覧および定義が記載されています。

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TLV61046ADBVR | Active | Production | SOT-23 (DBV) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1C4F |
| TLV61046ADBVR.A | Active | Production | SOT-23 (DBV) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1C4F |
| TLV61046ADBVT | Active | Production | SOT-23 (DBV) \| 6 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1C4F |
| TLV61046ADBVT.A | Active | Production | SOT-23 (DBV) \| 6 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1C4F |
| TLV61046ADBVTG4 | Active | Production | SOT-23 (DBV) \| 6 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1C4F |
| TLV61046ADBVTG4.A | Active | Production | SOT-23 (DBV) \| 6 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1C4F |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

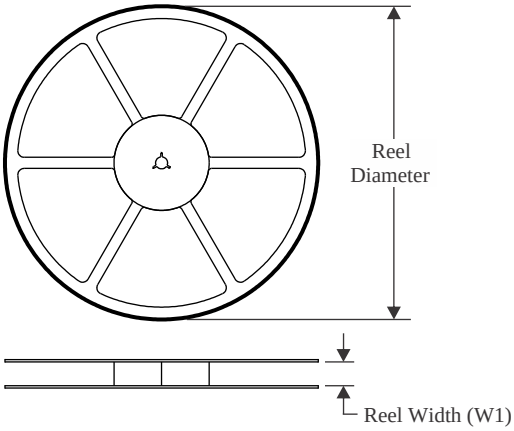
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

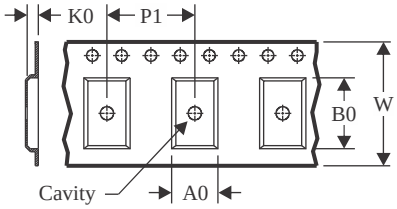
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

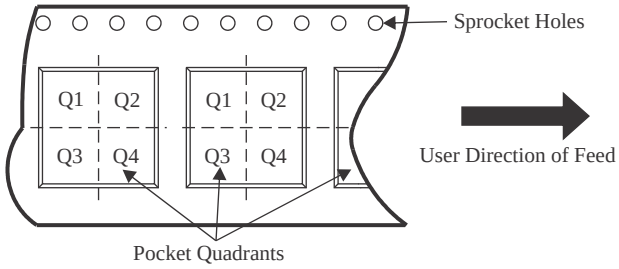



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

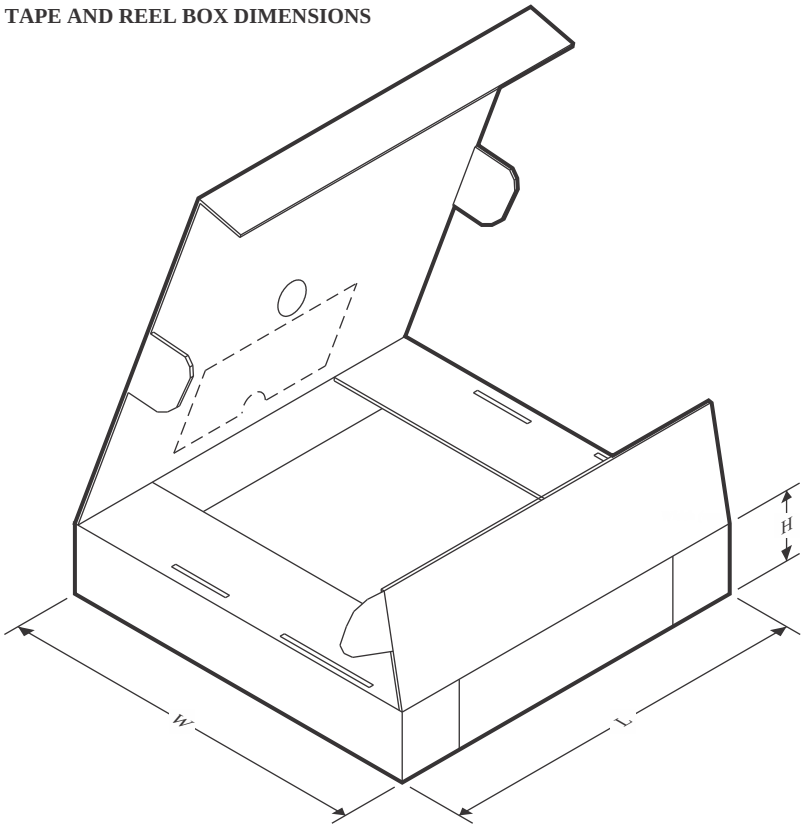
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV61046ADBVR | SOT-23 | DBV | 6 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV61046ADBVT | SOT-23 | DBV | 6 | 250 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV61046ADBVTG4 | SOT-23 | DBV | 6 | 250 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

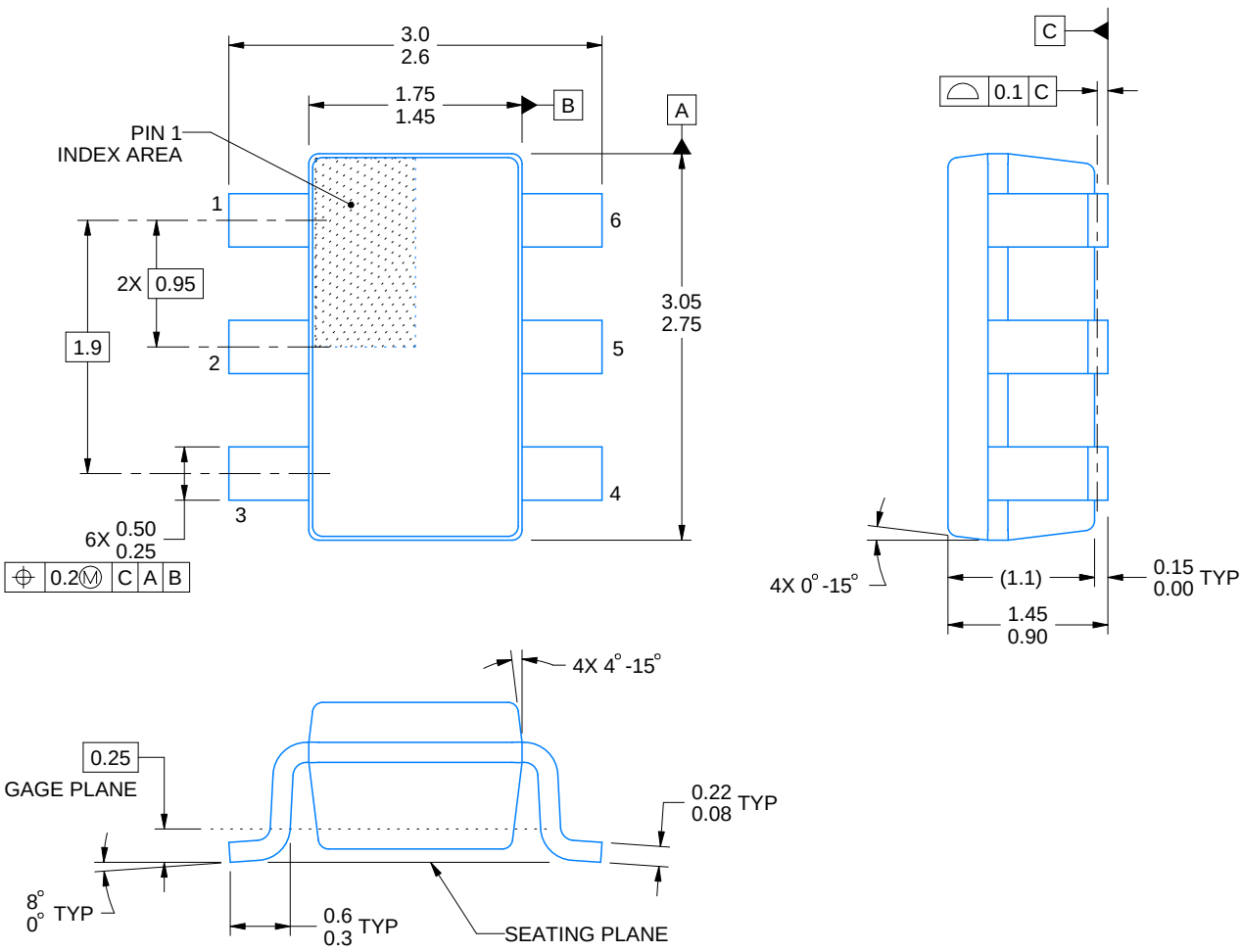
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TLV61046ADBVR | SOT-23 | DBV | 6 | 3000 | 210.0 | 185.0 | 35.0 |
| TLV61046ADBVT | SOT-23 | DBV | 6 | 250 | 210.0 | 185.0 | 35.0 |
| TLV61046ADBVTG4 | SOT-23 | DBV | 6 | 250 | 210.0 | 185.0 | 35.0 |

# PACKAGE OUTLINE

## DBV0006A

## SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

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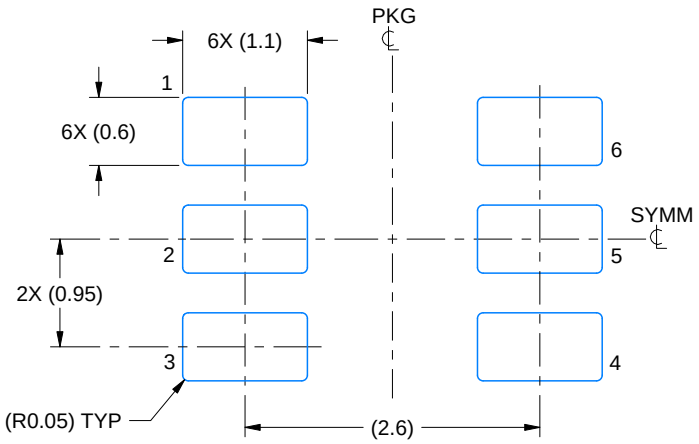
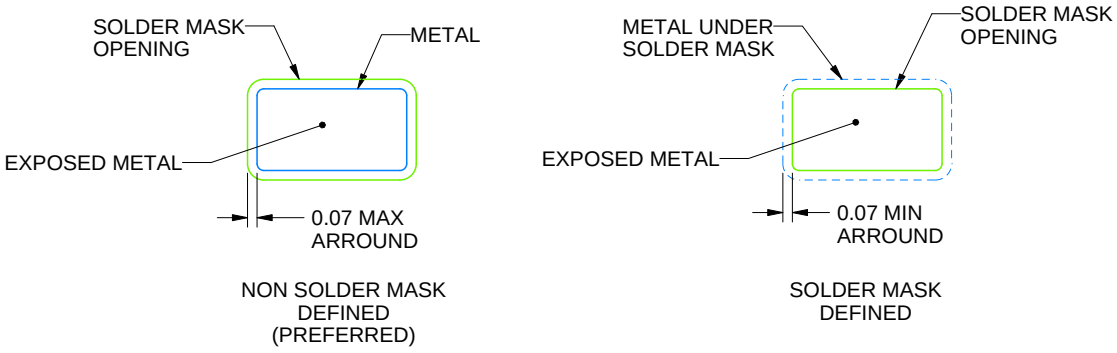
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X




SOLDER MASK DETAILS

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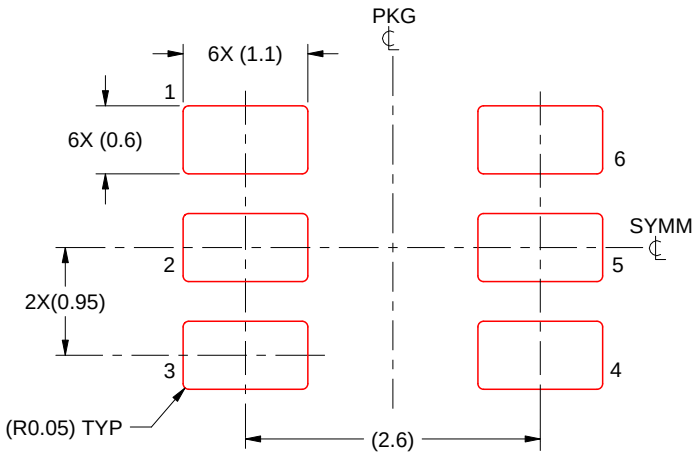
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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