TEXAS INSTRUMENTS

TLV521
JAJSC79 – MAY 2016

TLV521 NanoPower、350nA、RRIO、CMOS入力オペアンプ

1 特長

- 比類のないコストパフォーマンス
- V_S = 3.3Vについて、特に記載のない限り標準値
  - 非常に低い消費電流
    - 標準350nA、最大500nA
  - 広い動作電圧範囲: 1.7V〜5.5V
  - 低いTCV$_{OS}$ 1.5μV/°C
  - V_{OS} 3mV (最大)
  - 入力バイアス電流1pA
  - PSRR 100dB
  - CMRR 90dB
  - オープンループ・ゲイン110dB
  - ゲイン帯域幅積6kHz
  - スルーレート2.5V/ms
  - 入力電圧ノイズ: f = 100Hz時に300nV/√Hz
  - 温度範囲-40ºC〜125ºC
  - レール・ツー・レールの入出力(RRIO)

2 アプリケーション

- ワイヤレス・リモート・センサ
- 電力線監視
- パワー・メーター
- バッテリ駆動の産業用センサ
- マイクロパワー酸素センサおよび有毒ガス・センサ
- アクティブRFIDリーダー
- HVAC制御用のZigbeeベースのセンサ
- 環境発電で動作するセンサ・ネットワーク
- 電流検出
- 血糖監視

3 概要

TLV521 350nA NanoPowerオペアンプは、TIのNanoPowerファミリのオペアンプの中でも最高のコストパフォーマンスを提供します。TLV521には、注意深く設計されたCMOS入力ステージが存在し、Ibiasが 1pAと非常に低いため、I$_{BIAS}$およびI$_{OS}$の誤差が低減され、これらの影響を受けやすいメガオーム抵抗、高インピーダンスのフォトダイオード、電荷感知などのアプリケーションに適しています。さらに、EMI保護が組み込まれているため、携帯電話やRFIDリーダーなどから発生する不要なRF信号への感受性が低減されています。
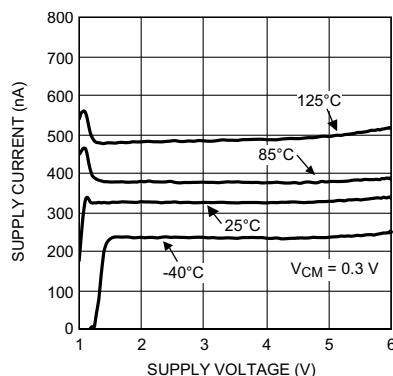
TLV521は 5ピンのSC70パッケージで提供され、動作温度範囲は-40°C〜125°Cです。

製品情報[1]

型番	パッケージ	本体サイズ(公称)
TLV521	SC70 (5)	2.00mm×1.25mm

[1] 提供されているすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

NanoPowerの消費電流

目次

4 改訂履歴

日付	改訂内容	注
2016年5月	*	初版

5 Pin Configuration and Functions

DCK Package
5-Pin (SC70) SC70-5
Top View
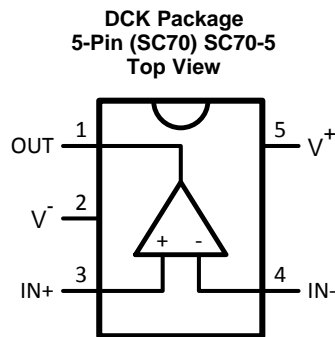
Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	OUT	O	Output
2	V–	P	Negative Power Supply
3	IN+	I	Noninverting Input
4	IN–	I	Inverting Input
5	V+	P	Positive Power Supply

6 Specifications

6.1 Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Any pin relative to V⁻		−0.3	6	V
IN+, IN−, OUT Pins		V^- – 0.3 V	V^+ + 0.3 V	V
V^+, V^-, OUT Pins			40	mA
Differential Input Voltage (V_{IN+} - V_{IN-})		−300	300	mV
Junction Temperature		−40	150	°C
Mounting Temperature	Infrared or Convection (30 sec.)		260	°C
	Wave Soldering Lead Temp. (4 sec.)		260	°C
Storage temperature, T_{stg}		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	
		Machine Model	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions[1]

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Temperature Range	−40	125	°C
Supply Voltage (V_S = V^+ - V^-)	1.7	5.5	V

(1) *Absolute Maximum Ratings* indicate limits beyond which damage may occur. *Recommended Operating Conditions* indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and test conditions, see *Electrical Characteristics*.

6.4 Thermal Information

THERMAL METRIC[1]		TLV521 DCK (SC70) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	269.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	93.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	48.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	47.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Unless otherwise specified, all limits for T_A = 25°C, V^+ = 3.3 V, V^- = 0 V, V_{CM} = V_O = V^+/2, and R_L > 1 MΩ. [1]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OS}	Input Offset Voltage	V_{CM} = 0.3 V	–3	0.1	3	mV
		V_{CM} = 3 V	–3	0.1	3	
TCV_{OS}	Input Offset Voltage Drift			±1.5		µV/°C
I_{BIAS}	Input Bias Current			1		pA
I_{OS}	Input Offset Current			50		fA
CMRR	Common Mode Rejection Ratio	0 V ≤ V_{CM} ≤ 3.3 V	70	90		dB
		0 V ≤ V_{CM} ≤ 2.2 V		100		
PSRR	Power Supply Rejection Ratio	V^+ = 1.8 V to 3.3 V; V_{CM} = 0.3 V	80	100		dB
CMVR	Common Mode Voltage Range	CMRR ≥ 70 dB	0		3.3	V
A_{VOL}	Large Signal Voltage Gain	V_O = 0.5 V to 2.8 V R_L = 100 kΩ to V^+/2	80	110		dB
V_O	Output Swing High	R_L = 100 kΩ to V^+/2 V_{IN}(diff) = 100 mV		3	50	mV from either rail
	Output Swing Low	R_L = 100 kΩ to V^+/2 V_{IN} (diff) = −100 mV		2	50	
I_O	Output Current	Sourcing, V_O to V^- V_{IN}(diff) = 100 mV		11		mA
		Sinking, V_O to V^+ V_{IN}(diff) = −100 mV		12		
I_S	Supply Current	V_{CM} = 0.3 V		350	500	nA

(1) *Electrical Characteristics* values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that TJ = TA. Parametric performance, as indicated in the electrical tables, is not ensured under conditions of self heating where TJ > TA. *Absolute Maximum Ratings* indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.

6.6 AC Electrical Characteristics[1]

Unless otherwise specified, all limits for T_A = 25°C, V^+ = 3.3 V, V^- = 0 V, V_{CM} = V_O = $V^+/2$, and R_L > 1 MΩ.

PARAMETER		TEST CONDITIONS		MIN (2)	TYP (3)	MAX (2)	UNIT
GBW	Gain-Bandwidth Product	C_L = 20 pF, R_L = 100 kΩ			6		kHz
SR	Slew Rate	A_V = +1, V_{IN} = 0 V to 3.3 V	Falling Edge		2.9		V/ms
			Rising Edge		2.5		
θ_m	Phase Margin	C_L = 20 pF, R_L = 100 kΩ			73		deg
G_m	Gain Margin	C_L = 20 pF, R_L = 100 kΩ			19		dB
e_n	Input-Referred Voltage Noise Density	f = 100 Hz			300		nV/√Hz
	Input-Referred Voltage Noise	0.1 Hz to 10 Hz			22		μV_{PP}
I_n	Input-Referred Current Noise	f = 100 Hz			100		fA/√Hz
EMIRR	EMI Rejection Ratio, IN+ and IN−[4]	V_{RF_PEAK} = 100 mV_P (−20 dB_P), f = 400 MHz			121		dB
		V_{RF_PEAK} = 100 mV_P (−20 dB_P), f = 900 MHz			121		
		V_{RF_PEAK} = 100 mV_P (−20 dB_P), f = 1800 MHz			124		
		V_{RF_PEAK} = 100 mV_P (−20 dB_P), f = 2400 MHz			142		

(1)   *Electrical Characteristics* values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that TJ = TA. Parametric performance, as indicated in the electrical tables, is not ensured under conditions of self heating where TJ > TA. *Absolute Maximum Ratings* indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2)   All limits are ensured by testing, statistical analysis or design.
(3)   Typical values represent the most likely parametric norm at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4)   The EMI Rejection Ratio is defined as EMIRR = 20log (VRF_PEAK/ΔVOS).

6.7 Typical Characteristics

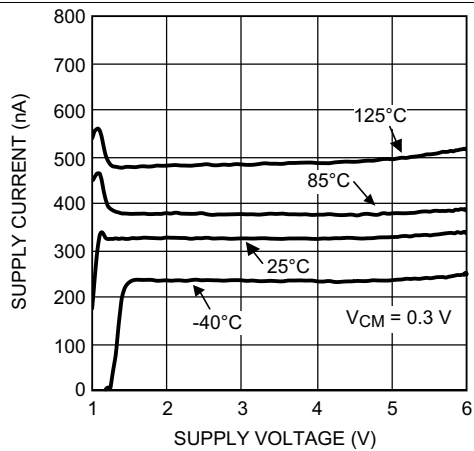At T_J = 25°C, unless otherwise specified.

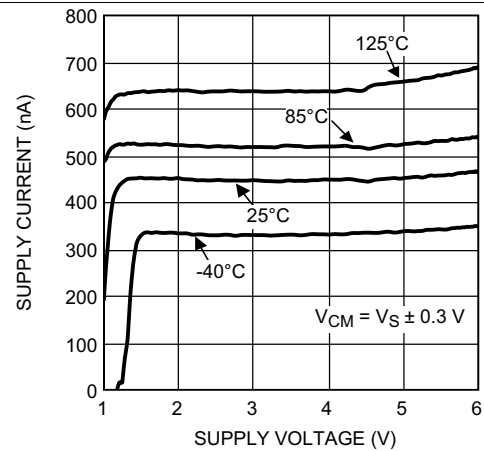**Figure 1. Supply Current vs. Supply Voltage**

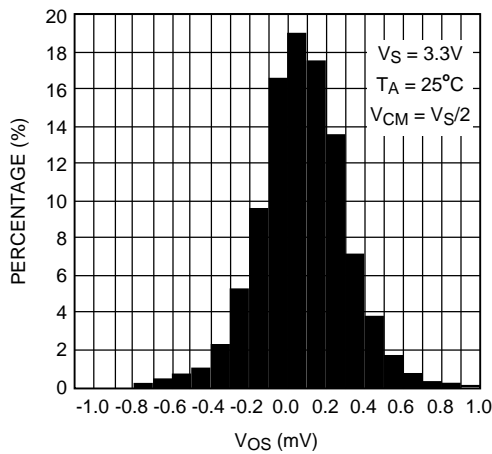**Figure 2. Supply Current vs. Supply Voltage**

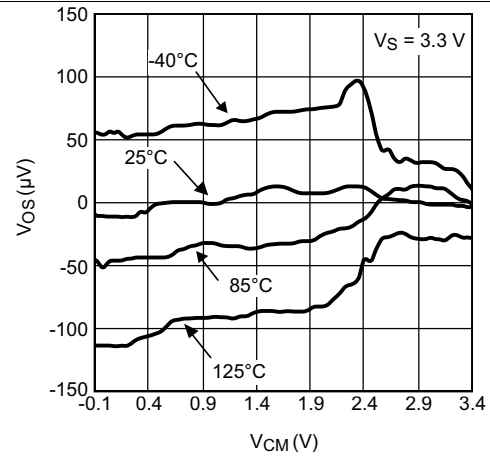**Figure 3. Offset Voltage Distribution**

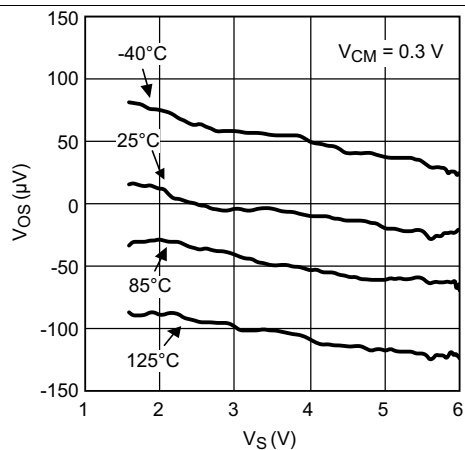**Figure 4. Input Offset Voltage vs. Input Common Mode**
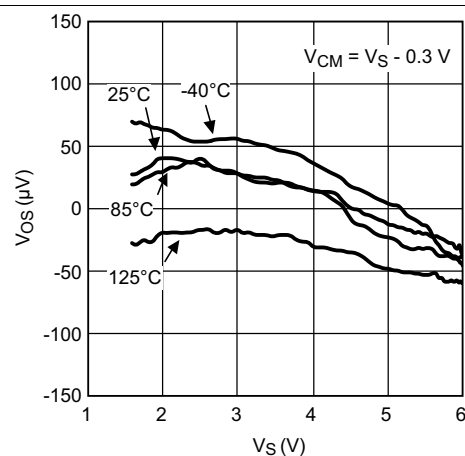

Figure 5. Input Offset Voltage vs. Supply Voltage

Figure 6. Input Offset Voltage vs. Supply Voltage

Typical Characteristics (continued)

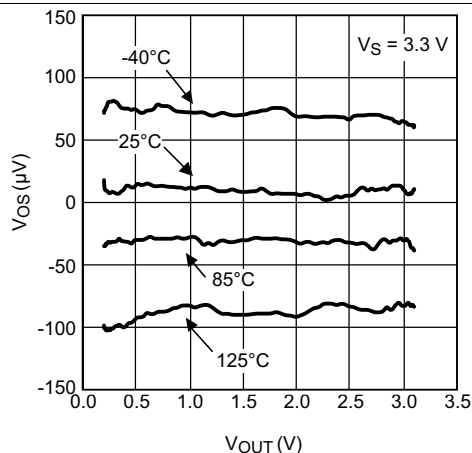At T_J = 25°C, unless otherwise specified.

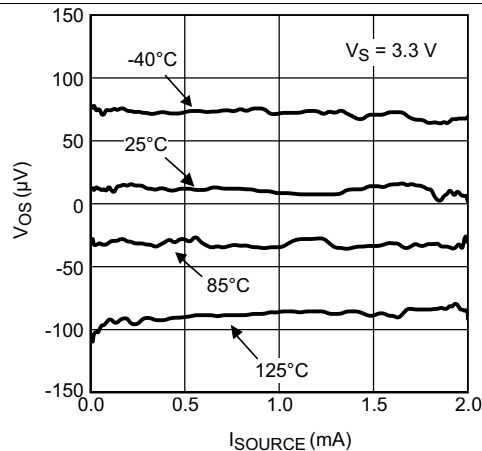**Figure 7. Input Offset Voltage vs. Output Voltage**

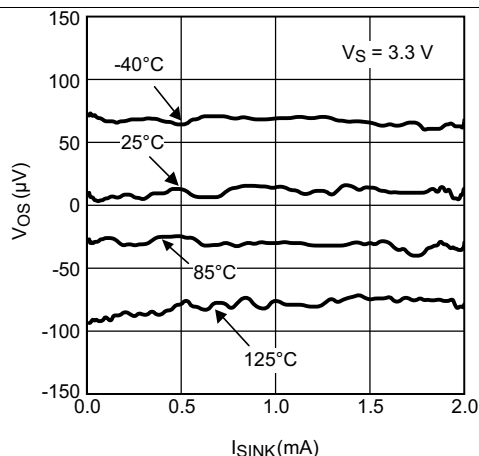**Figure 8. Input Offset Voltage vs. Sourcing Current**
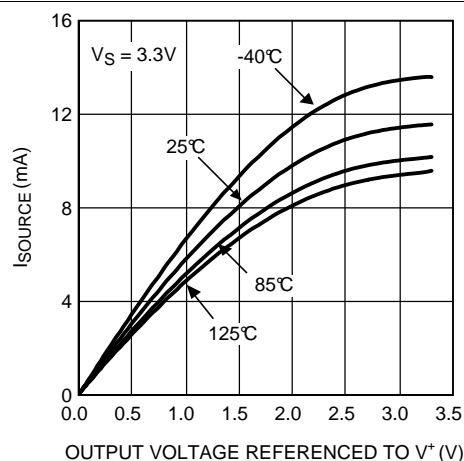

Figure 9. Input Offset Voltage vs. Sinking Current

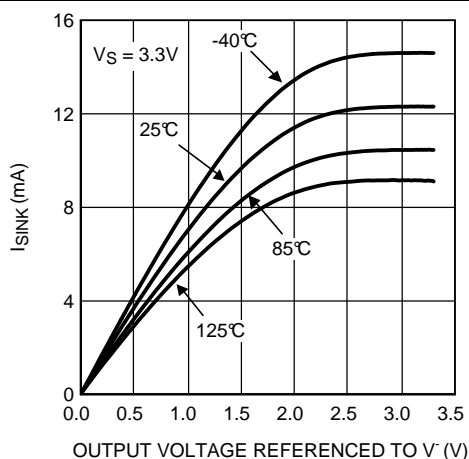**Figure 10. Sourcing Current vs. Output Voltage**

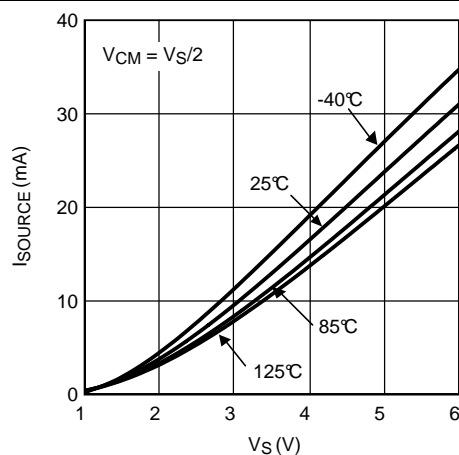**Figure 11. Sinking Current vs. Output Voltage**

Figure 12. Sourcing Current vs. Supply Voltage

Typical Characteristics (continued)
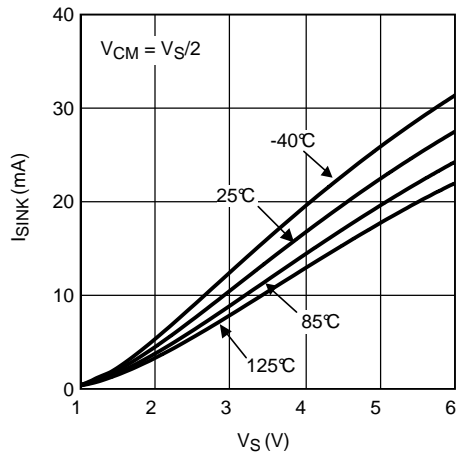
At T_J = 25°C, unless otherwise specified.

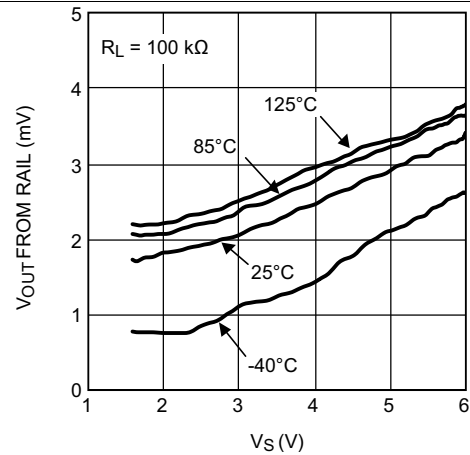**Figure 13. Sinking Current vs. Supply Voltage**

Figure 14. Output Swing High vs. Supply Voltage
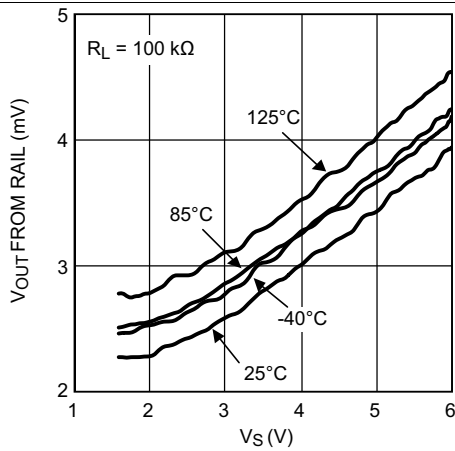
Figure 15. Output Swing Low vs. Supply Voltage
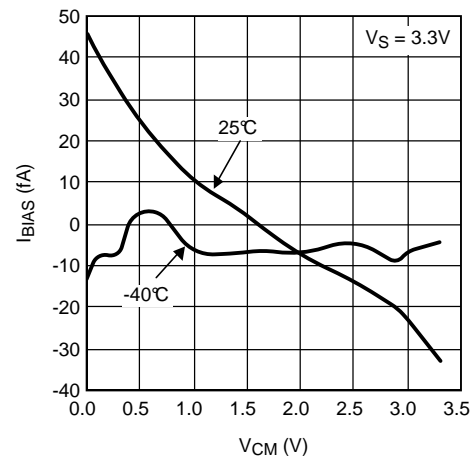
Figure 16. Input Bias Current vs. Common Mode Voltage
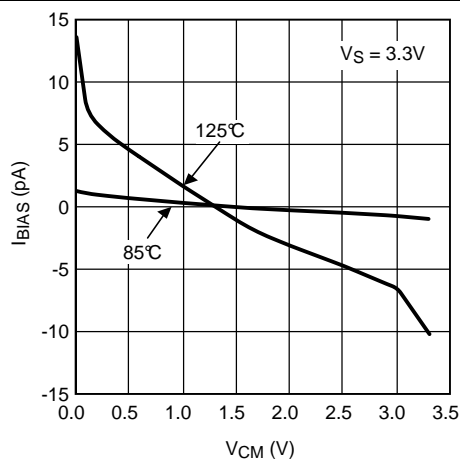
Figure 17. Input Bias Current vs. Common Mode Voltage
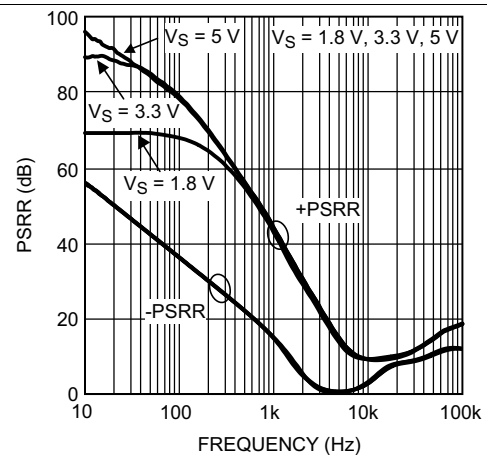
Figure 18. PSRR vs. Frequency

Typical Characteristics (continued)

At T_J = 25°C, unless otherwise specified.
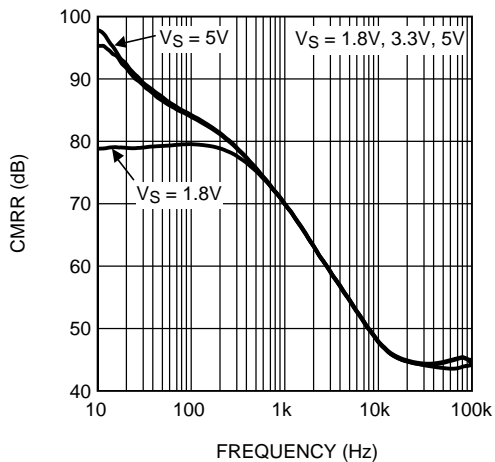
Figure 19. CMRR vs. Frequency
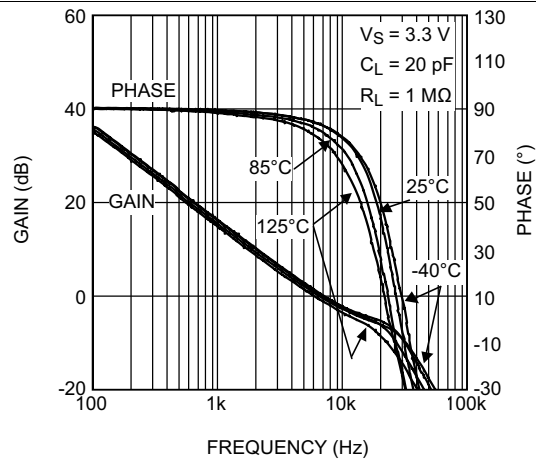
Figure 20. Frequency Response vs. Temperature
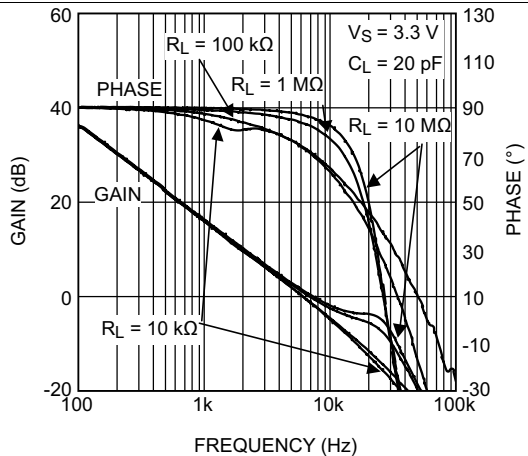
Figure 21. Frequency Response vs. R_L
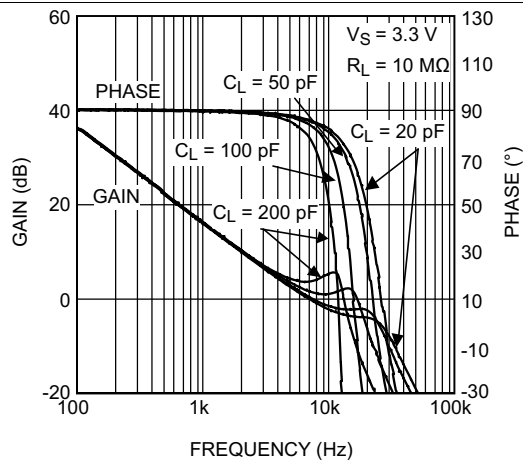
Figure 22. Frequency Response vs. C_L

Figure 23. Slew Rate vs. Supply Voltage

Figure 24. 0.1 to 10 Hz Time Domain Voltage Noise

Typical Characteristics (continued)

At T_J = 25°C, unless otherwise specified.

Figure 25. Large Signal Pulse Response

Figure 26. Large Signal Pulse Response

Figure 27. Overload Recovery Waveform

Figure 28. EMIRR vs. Frequency

7 Detailed Description

7.1 Overview

The TLV521 is fabricated with Texas Instruments' state-of-the-art VIP50 process. This proprietary process dramatically improves the performance of Texas Instru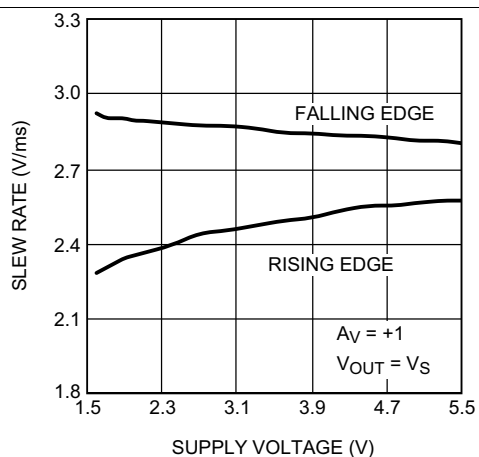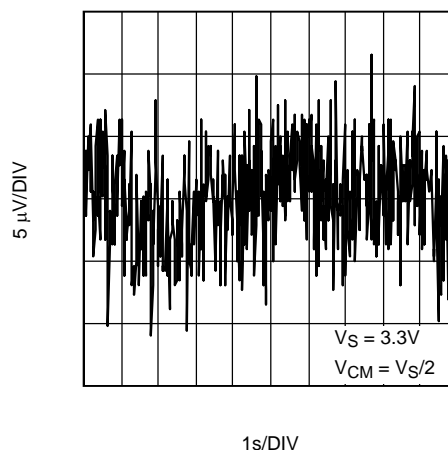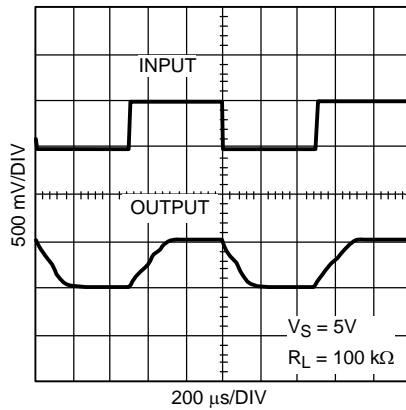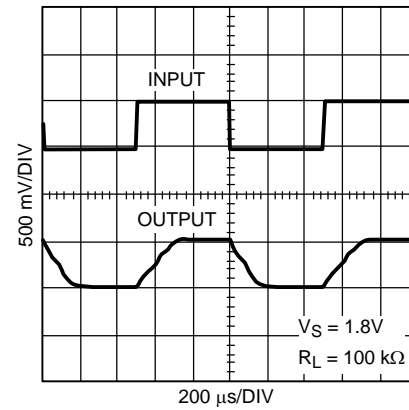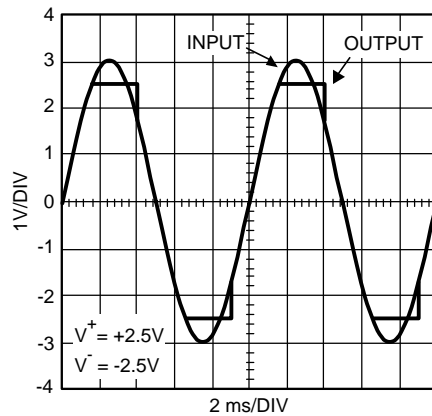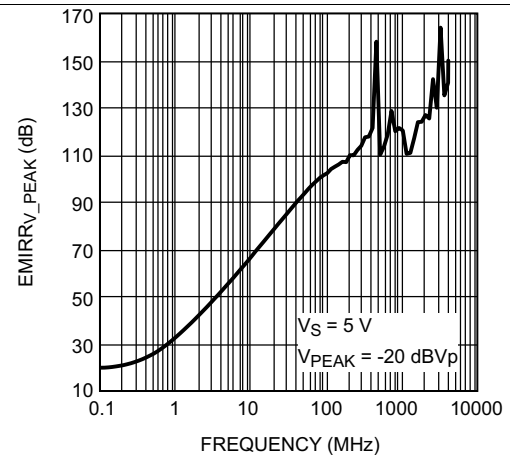ments' low-power and low-voltage operational amplifiers. The following sections showcase the advantages of the VIP50 process and highlight circuits which enable ultra-low power consumption.

7.2 Functional Block Diagram
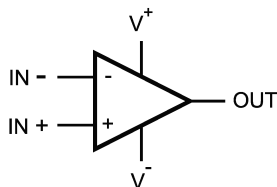
Figure 29. Block Diagram

7.3 Feature Description

The amplifier's differential inputs consist of a noninverting input (IN+) and an inverting input (IN−). The amplifier amplifies only the difference in voltage between the two inputs, which is called the differential input voltage. The output voltage of the op-amp Vout is given by Equation 1:

$$V_{OUT} = A_{OL} \ (IN^+ - IN^-) \tag{1}$$

where A_{OL} is the open-loop gain of the amplifier, typically around 100 dB.

7.4 Device Functional Modes

7.4.1 Input Stage

The TLV521 has a rail-to-rail input which provides more flexibility for the system designer. Rail-to-rail input is achieved by using in parallel, one PMOS differential pair and one NMOS differential pair. When the common mode input voltage (V_{CM}) is near V+, the NMOS pair is on and the PMOS pair is off. When V_{CM} is near V−, the NMOS pair is off and the PMOS pair is on. When V_{CM} is between V+ and V−, internal logic decides how much current each differential pair will get. This special logic ensures stable and low distortion amplifier operation within the entire common mode voltage range.

Because both input stages have their own offset voltage (V_{OS}) characteristic, the offset voltage of the TLV521 becomes a function of V_{CM}. V_{OS} has a crossover point at 1.0 V below V+. Refer to the 'V_{OS} vs. V_{CM}' curve in the Typical Performance Characteristics section. Caution should be taken in situations where the input signal amplitude is comparable to the V_{OS} value and/or the design requires high accuracy. In these situations, it is necessary for the input signal to avoid the crossover point. In addition, parameters such as PSRR and CMRR which involve the input offset voltage will also be affected by changes in V_{CM} across the differential pair transition region.

7.4.2 Output Stage

The TLV521 output voltage swings 3 mV from rails at 3.3-V supply, which provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

The TLV521 Maximum Output Voltage Swing defines the maximum swing possible under a particular output load. The TLV521 output swings 50 mV from the rail at 5-V supply with an output load of 100 kΩ.

8 Applications and Implementation

> **NOTE**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLV521 is specified for operation from 1.7 V to 5.5 V (±0.85 V to ±2.275 V). The TLV521 features rail to rail input and rail-to-rail output swings while consuming only nanowatts of power. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics* section.

8.1.1 Driving Capacitive Load

The TLV521 is internally compensated for stable unity gain operation, with a 6-kHz, typical gain bandwidth. However, the unity gain follower is the most sensitive configuration to capacitive load. The combination of a capacitive load placed at the output of an amplifier along with the amplifier's output impedance creates a phase lag, which reduces the phase margin of the amplifier. If the phase margin is significantly reduced, the response will be under damped which causes peaking in the transfer and, when there is too much peaking, the op amp might start oscillating.
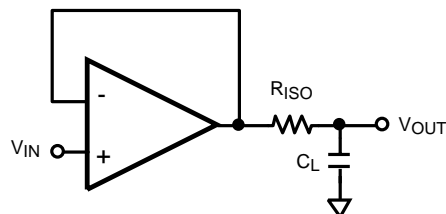
Figure 30. Resistive Isolation of Capacitive Load

In order to drive heavy capacitive loads, an isolation resistor, R_{ISO}, should be used, as shown in Figure 30. By using this isolation resistor, the capacitive load is isolated from the amplifier's output. The larger the value of R_{ISO}, the more stable the amplifier will be. If the value of R_{ISO} is sufficiently large, the feedback loop will be stable, independent of the value of C_L. However, larger values of R_{ISO} result in reduced output swing and reduced output current drive.

Recommended minimum values for R_{ISO} are given in the following table, for 5-V supply. Figure 31 shows the typical response obtained with the C_L = 50 pF and R_{ISO} = 154 kΩ. The other values of R_{ISO} in the table were chosen to achieve similar dampening at their respective capacitive loads. Notice that for the TLV521 with larger C_L a smaller R_{ISO} can be used for stability. However, for a given C_L a larger R_{ISO} will provide a more damped response. For capacitive loads of 20 pF and below no isolation resistor is needed.

Table 1. Capacitive Loads vs. Needed Isolation Resistors

C_L	R_{ISO}
0 – 20 pF	not needed
50 pF	154 kΩ
100 pF	118 kΩ
500 pF	52.3 kΩ
1 nF	33.2 kΩ
5 nF	17.4 kΩ
10 nF	13.3 kΩ
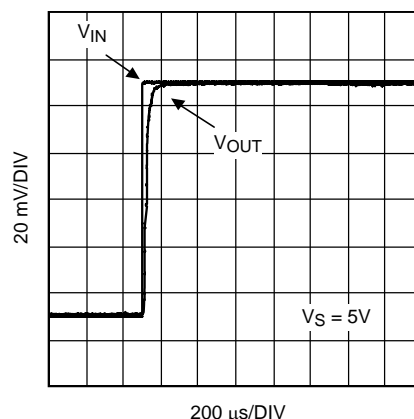
Figure 31. Step Response

8.1.2 EMI Suppression

The near-ubiquity of cellular, Bluetooth, and Wi-Fi signals and the rapid rise of sensing systems incorporating wireless radios make electromagnetic interference (EMI) an evermore important design consideration for precision signal paths. Though RF signals lie outside the op amp band, RF carrier switching can modulate the DC offset of the op amp. Also some common RF modulation schemes can induce down-converted components. The added DC offset and the induced signals are amplified with the signal of interest and thus corrupt the measurement. The TLV521 uses on chip filters to reject these unwanted RF signals at the inputs and power supply pins; thereby preserving the integrity of the precision signal path.

Twisted pair cabling and the active front-end's common-mode rejection provide immunity against low-frequency noise (i.e. 60-Hz or 50-Hz mains) but are ineffective against RF interference. Even a few centimeters of PCB trace and wiring for sensors located close to the amplifier can pick up significant 1 GHz RF. The integrated EMI filters of the TLV521 reduce or eliminate external shielding and filtering requirements, thereby increasing system robustness. A larger EMIRR means more rejection of the RF interference. For more information on EMIRR, please refer to AN-1698.

8.2 Typical Applications

8.2.1 60-Hz Twin T-Notch Filter

Figure 32. 60-Hz Notch Filter

Typical Applications (continued)

8.2.1.1   Design Requirements

Small signals from transducers in remote and distributed sensing applications commonly suffer strong 60-Hz interference from AC power lines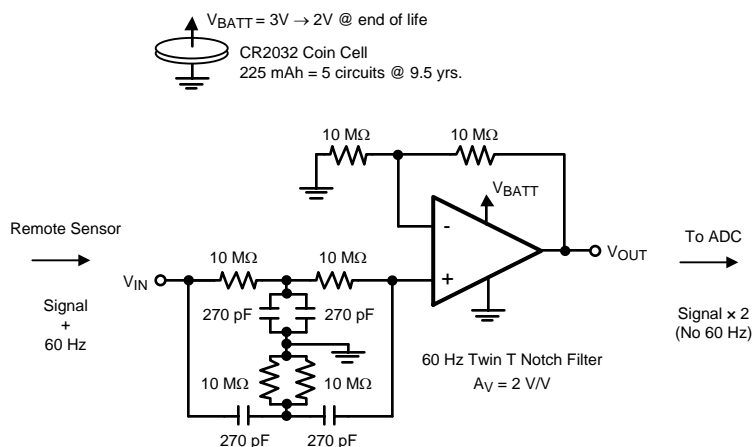. The circuit of Figure 32 notches out the 60 Hz and provides a gain $A_V = 2$ for the sensor signal represented by a 1-kHz sine wave. Similar stages may be cascaded to remove 2nd and 3rd harmonics of 60 Hz. Thanks to the nA power consumption of the TLV521, even 5 such circuits can run for 9.5 years from a small CR2032 lithium cell. These batteries have a nominal voltage of 3 V and an end of life voltage of 2 V. With an operating voltage from 1.7 V to 5.5 V the TLV521 can function over this voltage range.

8.2.1.2   Detailed Design Procedure

The notch frequency is set by $F_0 = 1 / 2\pi RC$. To achieve a 60-Hz notch use R = 10 MΩ and C = 270 pF. If eliminating 50-Hz noise, which is common in European systems, use R = 11.8 MΩ and C = 270 pF.

The Twin T Notch Filter works by having two separate paths from V_{IN} to the amplifier's input. A low frequency path through the resistors R - R and another separate high frequency path through the capacitors C - C. However, at frequencies around the notch frequency, the two paths have opposing phase angles and the two signals will tend to cancel at the amplifier's input.

To ensure that the target center frequency is achieved and to maximize the notch depth (Q factor) the filter needs to be as balanced as possible. To obtain circuit balance, while overcoming limitations of available standard resistor and capacitor values, use passives in parallel to achieve the 2C and R/2 circuit requirements for the filter components that connect to ground.

To make sure passive component values stay as expected clean board with alcohol, rinse with deionized water, and air dry. Make sure board remains in a relatively low humidity environment to minimize moisture which may increase the conductivity of board components. Also large resistors come with considerable parasitic stray capacitance which effects can be reduced by cutting out the ground plane below components of concern.

Large resistors are used in the feedback network to minimize battery drain. When designing with large resistors, resistor thermal noise, op amp current noise, as well as op amp voltage noise, must be considered in the noise analysis of the circuit. The noise analysis for the circuit in Figure 32 can be done over a bandwidth of 5 kHz, which takes the conservative approach of overestimating the bandwidth (TLV521 typical GBW/A_V is lower). The total noise at the output is approximately 800 µVpp, which is excellent considering the total consumption of the circuit is only 540 nA. The dominant noise terms are op amp voltage noise (550 µVpp), current noise through the feedback network (430 µVpp), and current noise through the notch filter network (280 µVpp). Thus the total circuit's noise is below ½ LSB of a 10 bit system with a 2-V reference, which is 1 mV.

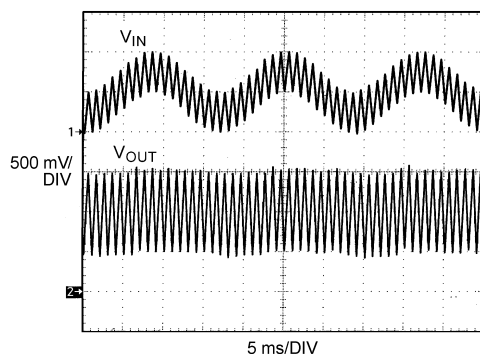### 8.2.1.3   Application Curve

Figure 33. 60-Hz Notch Filter Waveform

Typical Applications (continued)

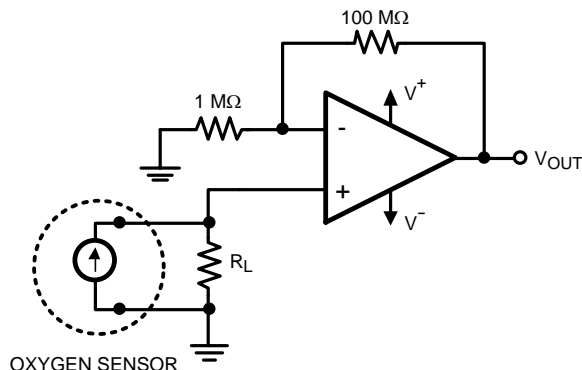## 8.2.2 Portable Gas Detection Sensor

Figure 34. Precision Oxygen Sensor

8.2.2.1 *Design Requirements*

Gas sensors are used in many different industrial and medical applications. They generate a current which is proportional to the percentage of a particular gas sensed in an air sample. This current goes through a load resistor and the resulting voltage drop is measured. The TLV521 makes an excellent choice for this application as it only draws 350 nA of current and operates on supply voltages down to 1.7 V. Depending on the sensed gas and sensitivity of the sensor, the output current can be in the order of tens of microamperes to a few milliamperes. Gas sensor data sheets often specify a recommended load resistor value or they suggest a range of load resistors to choose from.

Oxygen sensors are used when air quality or oxygen delivered to a patient needs to be monitored. Fresh air contains 20.9% oxygen. Air samples containing less than 18% oxygen are considered dangerous. This application detects oxygen in air. Oxygen sensors are also used in industrial applications where the environment must lack oxygen. An example is when food is vacuum packed. There are two main categories of oxygen sensors, those which sense oxygen when it is abundantly present (i.e. in air or near an oxygen tank) and those which detect traces of oxygen in ppm.

8.2.2.2 *Detailed Design Procedure*

Figure 34 shows a typical circuit used to amplify the output of an oxygen detector. The oxygen sensor outputs a known current through the load resistor. This value changes with the amount of oxygen present in the air sample. Oxygen sensors usually recommend a particular load resistor value or specify a range of acceptable values for the load resistor. The use of the nanopower TLV521 means minimal power usage by the op amp and it enhances the battery life. With the components shown in Figure 34 the circuit can consume less than 0.5 µA of current ensuring that even batteries used in compact portable electronics, with low mAh charge ratings, could last beyond the life of the oxygen sensor. The precision specifications of the TLV521, such as its very low offset voltage, low TCV_{OS} , low input bias current, high CMRR, and high PSRR are other factors which make the TLV521 a great choice for this application.

Typical Applications (continued)
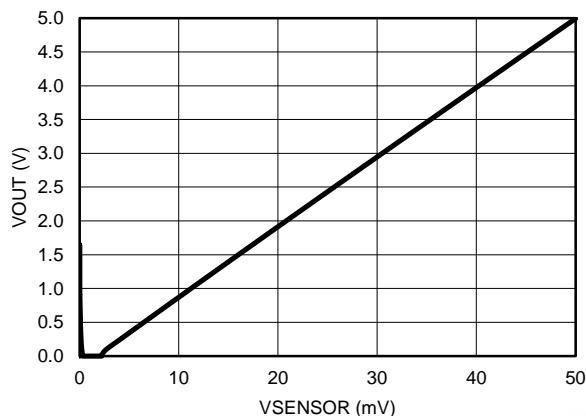
8.2.2.3 Application Curve

Figure 35. Calculated Oxygen Sensor Circuit Output (Single 5V Supply)

8.2.3 High-Side Battery Current Sensing

$$V_{OUT} = \frac{R_{SENSE} \times R_3}{R_1} \times I_{CHARGE}$$
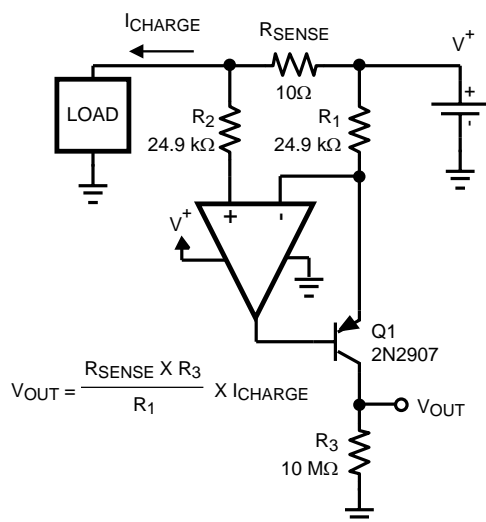
Figure 36. High-Side Current Sensing

8.2.3.1 Design Requirements

The rail-to-rail common mode input range and the very low quiescent current make the TLV521 ideal to use in high-side and low-side battery current sensing applications. The high-side current sensing circuit in Figure 36 is commonly used in a battery charger to monitor the charging current in order to prevent over charging. A sense resistor R_{SENSE} is connected in series with the battery.

8.2.3.2 Detailed Design Procedure

The theoretical output voltage of the circuit is $V_{OUT} = [R_{SENSE} \times R_3) / R_1] \times I_{CHARGE}$. In reality, however, due to the finite Current Gain, β, of the transistor the current that travels through R_3 will not be I_{CHARGE}, but instead, will be $\alpha \times I_{CHARGE}$ or $\beta/(\beta+1) \times I_{CHARGE}$. A Darlington pair can be used to increase the β and performance of the measuring circuit.

Using the components shown in Figure 36 will result in $V_{OUT} \approx 4000 \ \Omega \times I_{CHARGE}$. This is ideal to amplify a 1 mA I_{CHARGE} to near full scale of an ADC with V_{REF} at 4.1 V. A resistor, R2 is used at the noninverting input of the amplifier, with the same value as R1 to minimize offset voltage.

Typical Applications (continued)

Selecting values per Figure 36 will limit the current traveling through the $R_1 - Q1 - R_3$ leg of the circuit to under 1 µA which is on the same order as the TLV521 supply current. Increasing resistors R_1, R_2, and R_3 will decrease the measuring circuit supply current and extend battery life.

Decreasing R_{SENSE} will minimize error due to resistor tolerance, however, this will also decrease $V_{SENSE} = I_{CHARGE} \times R_{SENSE}$, and in turn the amplifier offset voltage will have a more significant contribution to the total error of the circuit. With the components shown in Figure 36 the measurement circuit supply current can be kept below 1.5 µA and measure 100 µA to 1 mA.

8.2.3.3 Application Curve
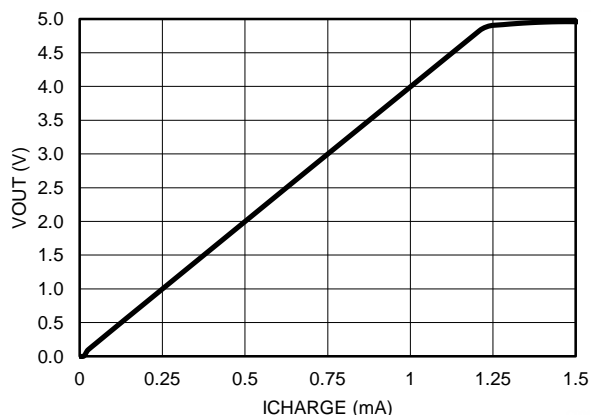
Figure 37. Calculated High-Side Current Sense Circuit Output

9 Power Supply Recommendations

The TLV521 is specified for operation from 1.7 V to 5.5 V (±0.85 V to ±2.275 V) over a –40°C to 125°C temperature range. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

> **CAUTION**
>
> Supply voltages larger than 6 V can permanently damage the device.

Low bandwidth nanopower devices do not have good high frequency (>1kHz) AC PSRR rejection against high-frequency switching supplies and other kHz and above noise sources, so extra supply filtering is recommended if kHz range noise is expected on the power supply lines.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
- Connect low-ESR, 0.1-μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information refer to *Circuit Board Layout Techniques*, SLOA089.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in *Layout Example*, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
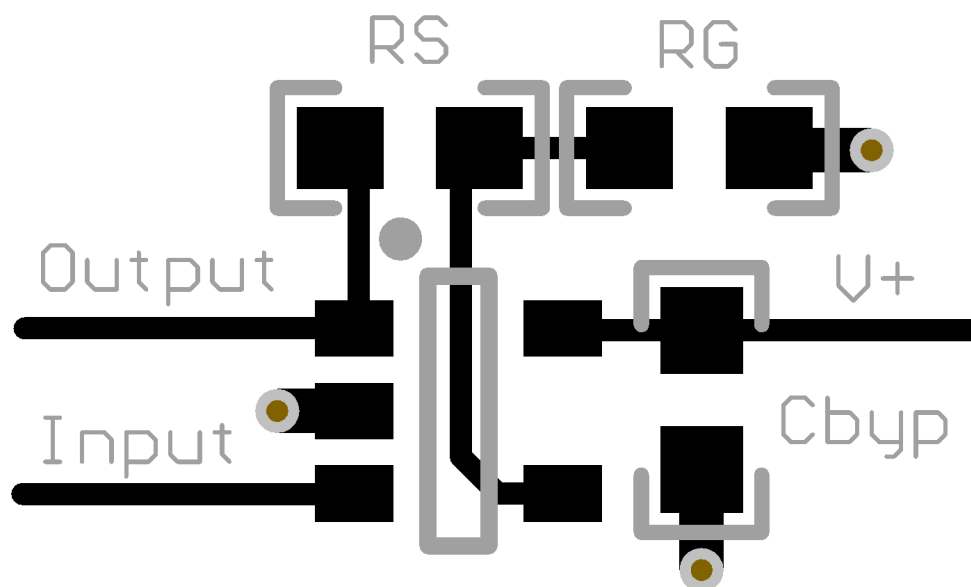
10.2 Layout Example

Figure 38. Noninverting Layout Example

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 開発サポート

TLV521 PSPICEモデル、SNOM024

TINA-TI SPICEベースのアナログ・シミュレーション・プログラム、http://www.ti.com/tool/tina-ti

TI Filterproソフトウェア、http://www.ti.com/tool/filterpro

DIPアダプタ評価モジュール、http://www.ti.com/tool/dip-adapter-evm

TIユニバーサル・オペアンプ評価モジュール、http://www.ti.com/tool/opampevm

SC70パッケージの5ピン、北向きアンプ用評価ボード、SNOA487

LMH730268評価ボード用マニュアル551012922-001

11.2 ドキュメントのサポート

11.2.1 関連資料

関連資料については、以下を参照してください。

- 『Feedback Plots Define Op Amp AC Performance (フィードバック・プロットによるオペアンプAC性能の定義)』、SBOA015 (AB-028)
- 『Circuit Board Layout Techniques (基板のレイアウト技法)』、SLOA089
- 『Op Amps for Everyone (誰でも使えるオペアンプ)』、SLOD006
- 『AN-1698 A Specification for EMI Hardened Operational Amplifiers (EMI強化されたオペアンプの仕様)』、SNOA497
- 『EMI Rejection Ratio of Operational Amplifiers (オペアンプのEMI除去率)』、SBOA128
- 『Capacitive Load Drive Solution using an Isolation Resistor (絶縁抵抗を使用した容量性負荷駆動ソリューション)』、TIPD128
- 『Handbook of Operational Amplifier Applications (オペアンプ・アプリケーション・ハンドブック)』、SBOA092

11.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 商標

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11.5 静電気放電に関する注意事項

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静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.6 Glossary

SLYZ022 — *TI Glossary.*

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV521DCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	14F
TLV521DCKR.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	14F
TLV521DCKT	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	14F
TLV521DCKT.A	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	14F

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

TEXAS INSTRUMENTS

www.ti.com

DCK0005A

5X (0.95)

PKG ℄

1

5X (0.4)

2

2X (0.65)

3

(R0.05) TYP

SYMM ℄

5

(1.3)

4

(2.2)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.07 MAX
ARROUND

NON SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.07 MIN
ARROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

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NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.
10. Board assembly site may have different recommendations for stencil design.