TLV4062-Q1、TLV4082-Q1 リファレンス内蔵、デュアルチャネル、低電力コンパレータ

1 特長

- 車載アプリケーションに対応
- 下記内容で AEC-Q100 認定済み:
  - デバイス温度グレード 1:-40℃～125℃の動作時周囲温度範囲
  - デバイス HBM ESD 分類レベル H1C
  - デバイス CDM ESD 分類レベル C4B
- 広い電源電圧範囲:1.5V～5.5V
- 小型パッケージの 2 チャネル検出器
- 高いスレッショルド精度:温度範囲全体で 1%
- 高精度ヒステリシス:60mV
- 低い静止電流:2µA (標準値)
- 温度範囲:-40℃～+125℃
- プッシュプル (TLV4062-Q1) およびオープン・ドレイン (TLV4082-Q1) 出力オプション
- SOT-23 パッケージで供給

2 アプリケーション

- 緊急通話 (eCall)
- 車載用ヘッド・ユニット
- インストルメント・クラスタ
- オンボード・チャージャ (OBC) / ワイヤレス・チャージャ

3 概要

TLV4062-Q1 および TLV4082-Q1 は高精度のデュアルチャネル・コンパレータ・ファミリで、低消費電力と小さなソリューション・サイズが特長です。IN1 および IN2 入力には、短時間のグリッチを除去するためのヒステリシスが含まれているため、誤ったトリガが発生せず出力動作が安定します。

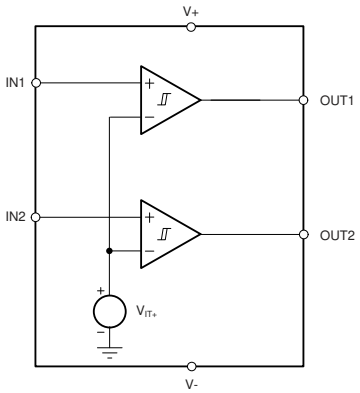
TLV4062-Q1 および TLV4082-Q1 には可変の INx 入力があり、1 対の外付け分圧抵抗によって構成可能です。IN1 または IN2 入力の電圧が下降時のスレッショルドを下回ると、それぞれ OUT1 または OUT2 が LOW になります。IN1 または IN2 が上昇時のスレッショルドよりも高くなると、それぞれ OUT1 または OUT2 が HIGH になります。

これらのコンパレータは静止電流が 2µA (標準値) と非常に小さく、低消費電力で電圧を監視するための、高精度で省スペースのソリューションを実現します。TLV4062-Q1 および TLV4082-Q1 の動作電圧範囲は、-40℃～+125℃の温度範囲全体で 1.5V～5.5V です。

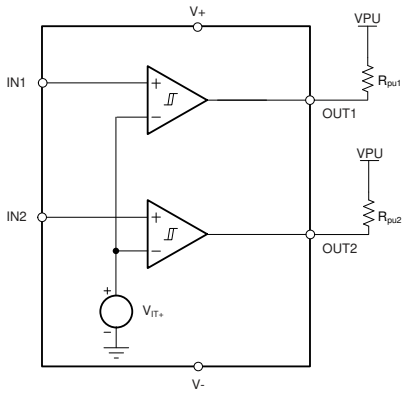
製品情報 (1)

部品番号	パッケージ	本体サイズ (公称)
TLV4062-Q1、TLV4082-Q1	SOT-23 (6)	2.90mm × 1.60mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。



TLV4062-Q1 のブロック図



TLV4082-Q1 のブロック図

Table of Contents

1 特長 ... 1
2 アプリケーション ... 1
3 概要 ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 5
6.5 Electrical Characteristics ... 5
6.6 Timing Requirements ... 6
6.7 Timing Diagrams ... 6
6.8 Typical Characteristics ... 7
7 Detailed Description ... 10
7.1 Overview ... 10
7.2 Functional Block Diagrams ... 10
7.3 Feature Description ... 11
7.4 Device Functional Modes ... 11
8 Application and Implementation ... 13
8.1 Application Information ... 13
8.2 Typical Applications ... 13
9 Power Supply Recommendations ... 19
10 Layout ... 20
10.1 Layout Guidelines ... 20
10.2 Layout Example ... 20
11 Device and Documentation Support ... 21
11.1 Documentation Support ... 21
11.2 Receiving Notification of Documentation Updates ... 21
11.3 サポート・リソース ... 21
11.4 Trademarks ... 21
11.5 静電気放電に関する注意事項 ... 21
11.6 用語集 ... 21

4 Revision History

DATE	REVISION	NOTES
October 2020	*	Initial release.

5 Pin Configuration and Functions

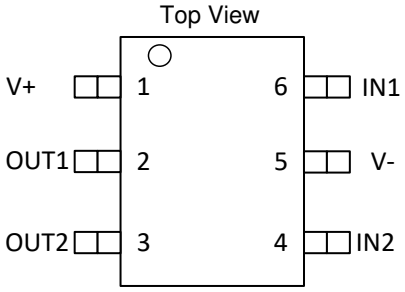


図 5-1. DBV Package, 6-Pin SOT-23

表 5-1. Pin Functions

NAME	NO.	I/O	DESCRIPTION
	DBV		
GND	5	—	Ground
OUT1	2	O	OUT1 is the output for IN1. OUT1 is asserted (driven low) when the voltage at IN1 falls below V_{IT-}. OUT1 is deasserted (goes high) after IN1 rises higher than V_{IT+}. OUT1 is a push-pull output for the TLV4062 and an open-drain output for the TLV4082. The open-drain device (TLV4082) can be pulled up to 5.5 V independent of V+; a pullup resistor is required for this device.
OUT2	3	O	OUT2 is the output for IN2. OUT2 is asserted (driven low) when the voltage at IN2 falls below V_{IT-}. OUT2 is deasserted (goes high) after IN2 rises higher than V_{IT+}. OUT2 is a push-pull output for the TLV4062 and an open-drain output for the TLV4082. The open-drain device (TLV4082) can be pulled up to 5.5 V independent of V+; a pullup resistor is required for this device.
IN1	6	I	This pin is connected to the voltage to be monitored with the use of an external resistor divider. When the voltage at this pin drops below the threshold voltage (V_{IT-}), OUT1 is asserted.
IN2	4	I	This pin is connected to the voltage to be monitored with the use of an external resistor divider. When the voltage at this pin drops below the threshold voltage (V_{IT-}), OUT2 is asserted.
V+	1	I	Supply voltage input. Connect a 1.5-V to 5.5-V supply to V+ in order to power the device. Good analog design practice is to place a 0.1-µF ceramic capacitor close to this pin (required for V+ < 1.5 V).

6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	VDD	–0.3	7	V
	OUT1, OUT2 (push-pull only)	–0.3	VDD + 0.3	
	OUT1, OUT2 (open-drain only)	–0.3	7	
	IN1, IN2	–0.3	7	
Current	IN1, IN2(2)		10	mA
	OUT1, OUT2		±20	
Temperature	Operating junction, T_J (3)	–40	125	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to GND. Input signals that can swing 0.3V below GND must be current-limited to 10mA or less.
(3) For low-power devices, the junction temperature rise above the ambient temperature is negligible; therefore, the junction temperature is considered equal to the ambient temperature ($T_J = T_A$).

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
	Power-supply voltage		1.5		5.5	V
	Input voltage	IN1, IN2	0		5.5	V
	Output voltage (push-pull only)	OUT1, OUT2	0		VDD + 0.3	V
	Output voltage (open-drain only)	OUT1, OUT2	0		5.5	V
R_{PU}	Pullup resistor (open-drain only)		1.5		10,000	kΩ
	Current	OUT1, OUT2	–5		5	mA
C_{IN}	Input capacitor			0.1		µF
T_J	Junction temperature		–40	25	125	°C

6.4 Thermal Information

THERMAL METRIC[1]		TLV4062, TLV4082		UNIT
		DBV (SOT-23)	DRY (µSON)	
		6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	193.9	306.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	134.5	174.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	39.0	173.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	30.4	30.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	38.5	171.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	65.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

all specifications are over the operating temperature range of –40°C < T_J < +125°C and 1.5 V ≤ VDD ≤ 5.5 V (unless otherwise noted); typical values are at T_J = 25°C and VDD = 3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD	Input supply range		1.5		5.5	V
$V_{(POR)}$	Power-on-reset voltage[1]	V_{OL} (max) = 0.2 V, I_{OL} = 15 µA			0.8	V
I_{DD}	Supply current (into VDD pin)	VDD = 3.3 V, no load		2.09	5.80	µA
		VDD = 5.5 V, no load		2.29	6.50	
V_{IT+}	Positive-going (rising) input threshold voltage	$V_{(INx)}$ rising		1.194		V
			–1%		1%	
$V_{IT–}$	Negative-going (falling) input threshold voltage	$V_{(INx)}$ falling		1.134		V
			–1%		1%	
V_{HYS}	In-built Hysteresis			60		mV
$I_{(INx)}$	Input current	$V_{(INx)}$ = 0 V or VDD	–15		15	nA
V_{OL}	Low-level output voltage	VDD ≥ 1.5 V, I_{SINK} = 0.4 mA			0.25	V
		VDD ≥ 2.7 V, I_{SINK} = 2 mA			0.25	
		VDD ≥ 4.5 V, I_{SINK} = 3.2 mA			0.30	
V_{OH}	High-level output voltage (push-pull only)	VDD ≥ 1.5 V, I_{SOURCE} = 0.4 mA	0.8 VDD			V
		VDD ≥ 2.7 V, I_{SOURCE} = 1 mA	0.8 VDD			
		VDD ≥ 4.5 V, I_{SOURCE} = 2.5 mA	0.8 VDD			
$I_{lkg(OD)}$	Open-drain output leakage current (open-drain only)	High impedance, $V_{(INx)}$ = $V_{(OUTx)}$ = 5.5 V	–250		250	nA

(1) Outputs are undetermined below $V_{(POR)}$.

6.6 Timing Requirements

typical values are at T_J = 25°C and VDD = 3.3 V; INx transitions between 0 V and 1.3 V

		MIN	NOM	MAX	UNIT
$t_{PD(r)}$	INx (rising) to OUTx propagation delay		5.5		µs
$t_{PD(f)}$	INx (falling) to OUTx propagation delay		10		µs
t_{SD}	Startup delay(1)		570		µs

(1) During power-on or when a VDD transient is below VDD(min), the outputs reflect the input conditions 570 µs after VDD transitions through VDD(min).

6.7 Timing Diagrams

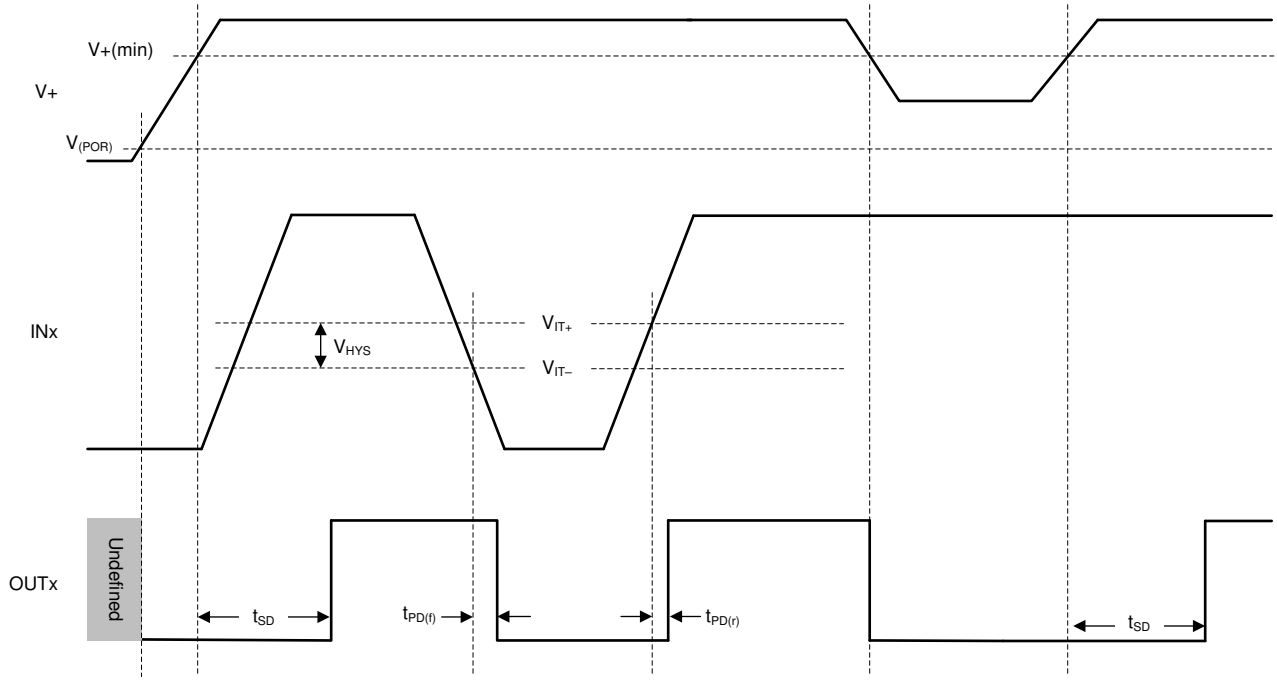
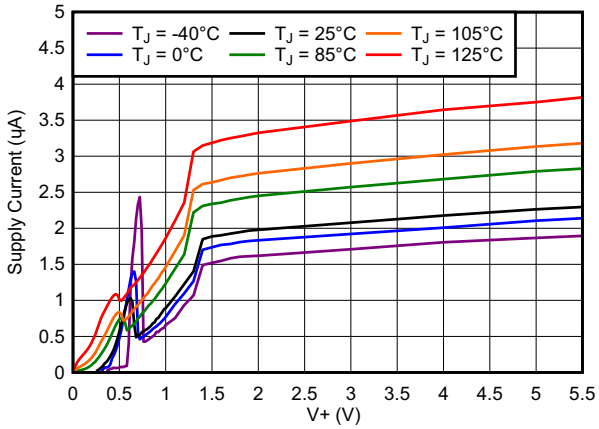


図 6-1.

6.8 Typical Characteristics

at T_J = 25°C with a 0.1-µF capacitor close to V+ (unless otherwise noted)



IN1 = IN2 = 1.5 V

図 6-2. Supply Current vs Supply Voltage

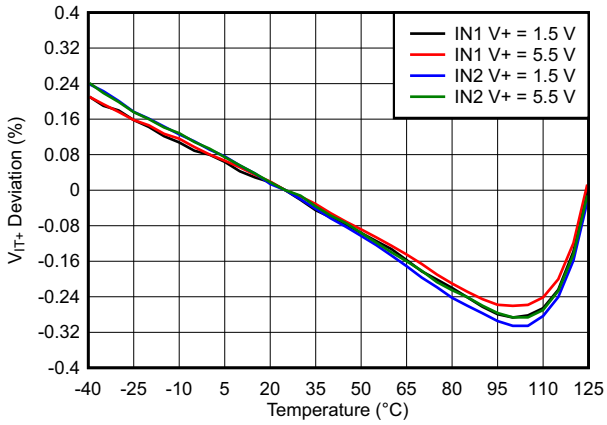


図 6-3. INx Threshold (V_{IT+}) Deviation vs Temperature

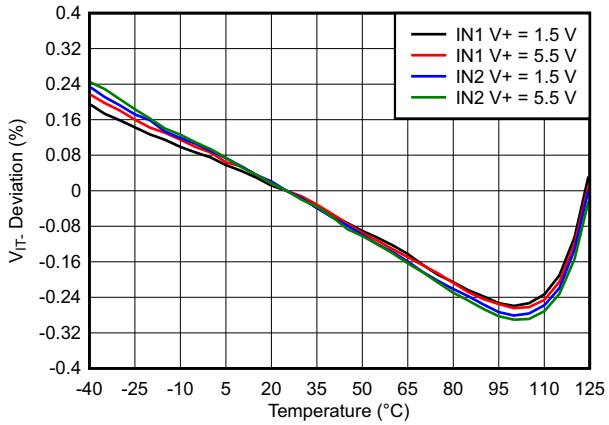
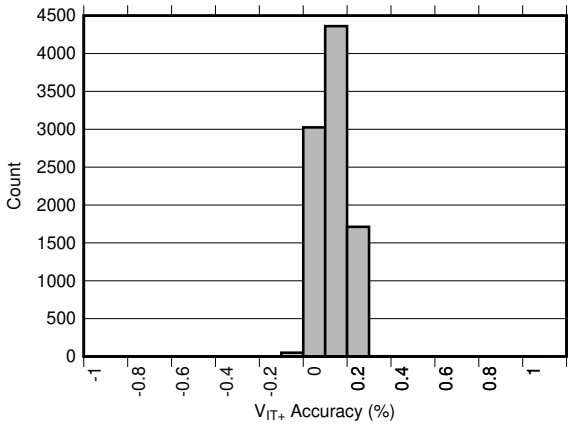
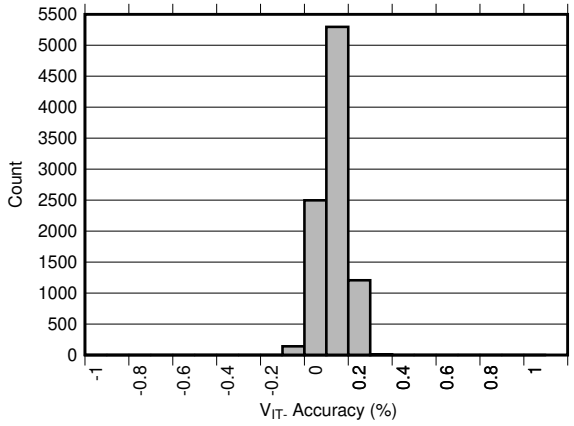


図 6-4. INx Threshold (V_{IT-}) Deviation vs Temperature



V+ = 5.5 V

図 6-5. INx Threshold (V_{IT+})



V+ = 5.5 V

図 6-6. INx Threshold (V_{IT-})

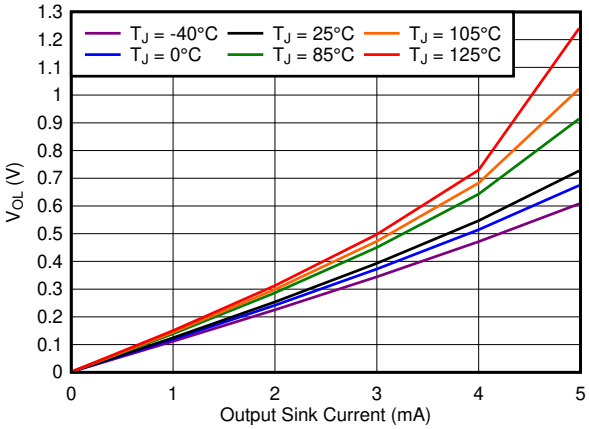


図 6-7. Output Voltage Low vs Output Current (V+ = 1.5 V)

6.8 Typical Characteristics (continued)

at T_J = 25°C with a 0.1-µF capacitor close to V+ (unless otherwise noted)

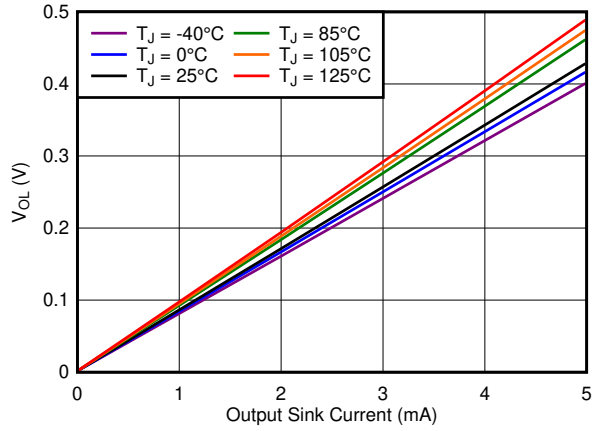


図 6-8. Output Voltage Low vs Output Current (V+ = 3.3 V)

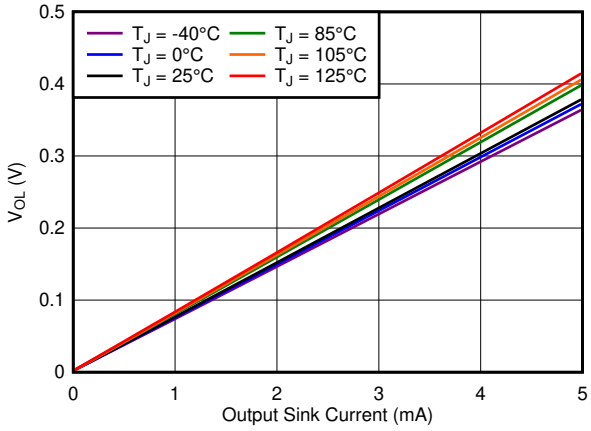


図 6-9. Output Voltage Low vs Output Current (V+ = 5.5 V)

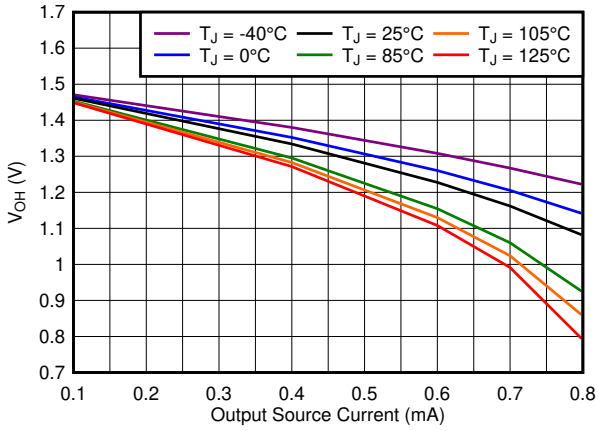


図 6-10. Output Voltage High vs Output Current (V+ = 1.5 V)

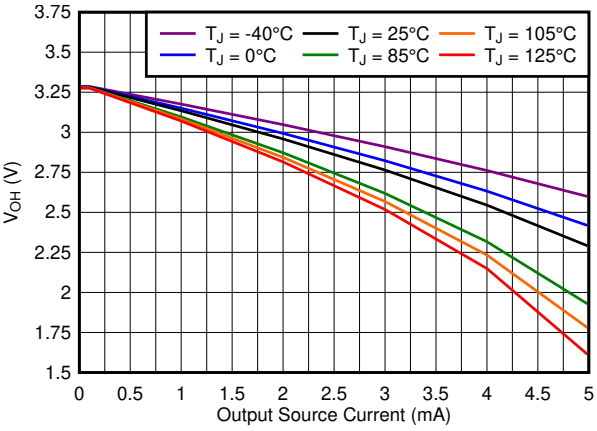


図 6-11. Output Voltage High vs Output Current (V+ = 3.3 V)

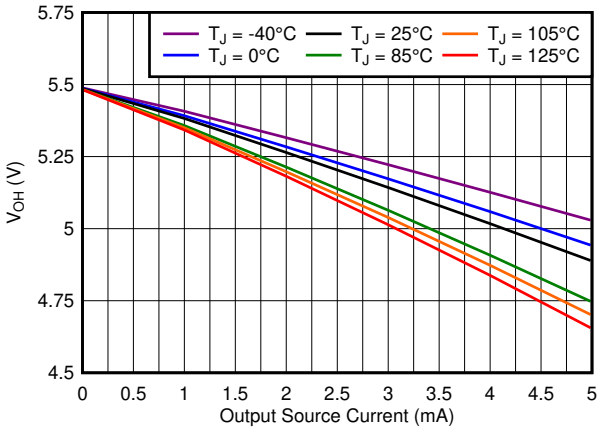
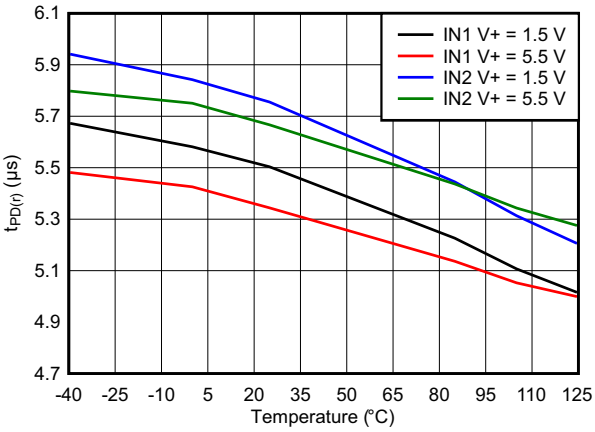


図 6-12. Output Voltage High vs Output Current (V+ = 5.5 V)

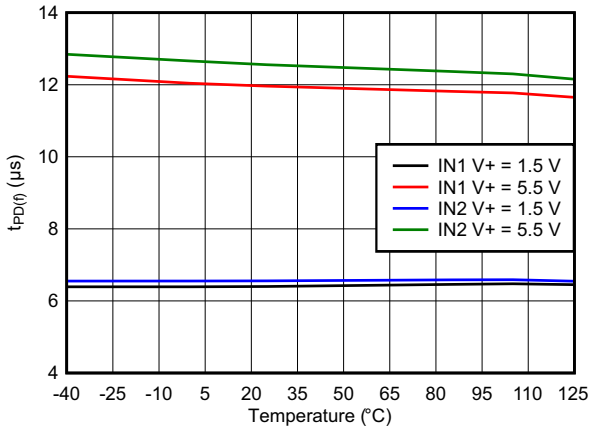


IN1 = IN2 = 0 V to 1.3 V

図 6-13. Propagation Delay from INx High to Output High

6.8 Typical Characteristics (continued)

at T_J = 25°C with a 0.1-µF capacitor close to V+ (unless otherwise noted)



IN1 = IN2 = 1.3 V to 0 V

図 6-14. Propagation Delay from INx Low to Output Low

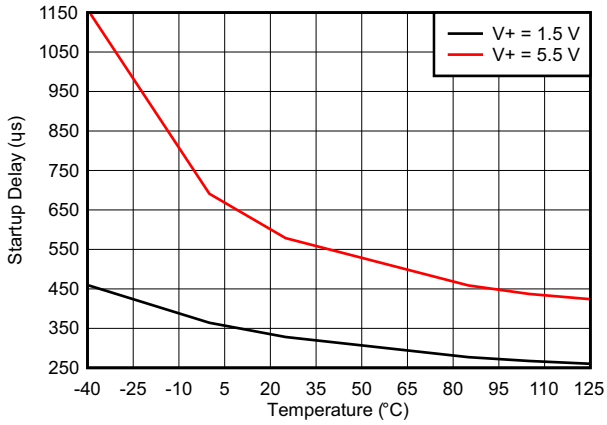
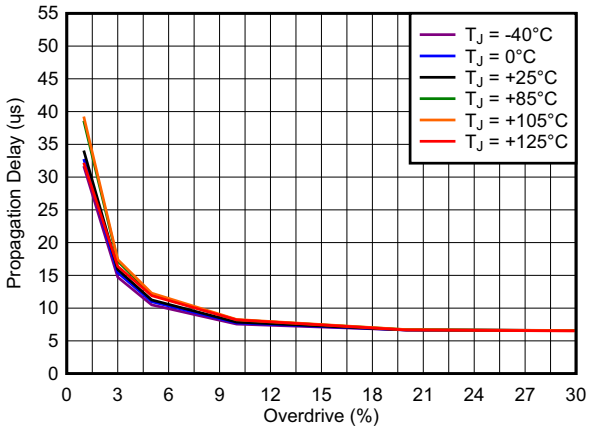
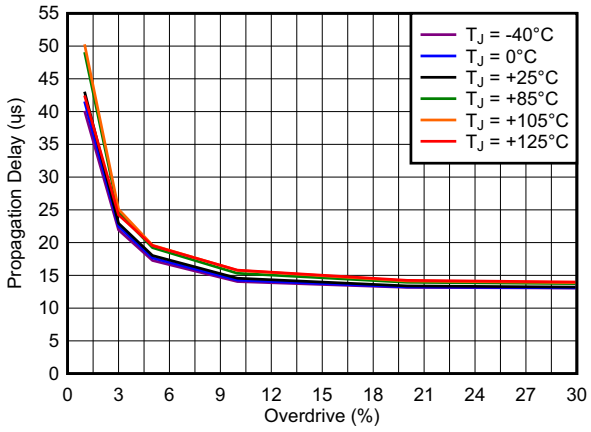


図 6-15. Startup Delay



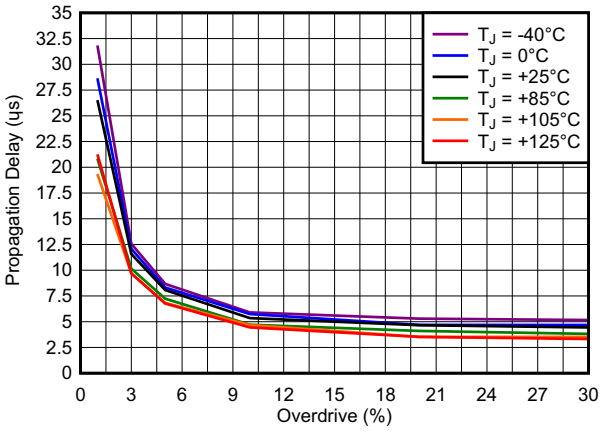
High-to-low transition occurs above the curve

図 6-16. Propagation Delay vs Overdrive (V+ = 1.5 V)



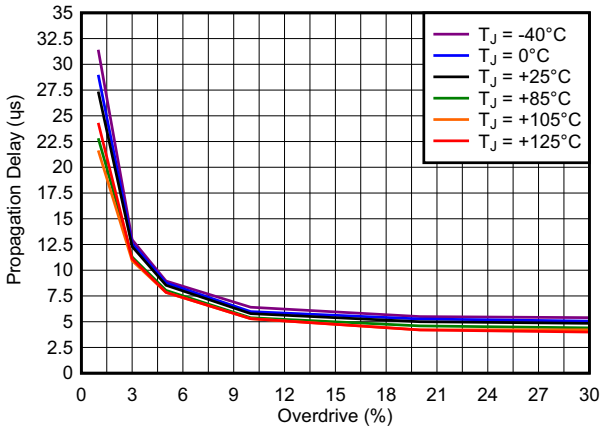
High-to-low transition occurs above the curve

図 6-17. Propagation Delay vs Overdrive (V+ = 5.5 V)



Low-to-high transition occurs above the curve

図 6-18. Propagation Delay vs Overdrive (V+ = 1.5 V)



Low-to-high transition occurs above the curve

図 6-19. Propagation Delay vs Overdrive (V+ = 5.5 V)

7 Detailed Description

7.1 Overview

The TLV4062-Q1 and TLV4082-Q1 are small, low quiescent current (I_{DD}), dual-channel comparators. These devices have high-accuracy, rising and falling input thresholds, and assert the output as shown in 表 7-1. The output (OUTx) transitions high when the input (INx) is rising and greater than V_{IT+}; the output (OUTx) will remain high until the input is falling and drops below V_{IT-} . The TLV4062-Q1 and TLV4082-Q1 can be used in systems where multiple voltage rails are required to be monitored, or where one channel can be used as an early warning signal and the other channel can be used as the system reset signal.

表 7-1. TLV4062-Q1 and TLV4082-Q1 Truth Table

DEVICE	(V_{IT+}, V_{IT-})	OUTPUT TOPOLOGY	INPUT VOLTAGE		OUTPUT LOGIC LEVEL
TLV4062-Q1	1.194V, 1.134V	Push-Pull	IN1 < V_{IT-}	IN1 falling	OUT1 = low
			IN2 < V_{IT-}	IN2 falling	OUT2 = low
			IN1 > V_{IT+}	IN1 rising	OUT1 = high
			IN2 > V_{IT+}	IN2 rising	OUT2 = high
TLV4082-Q1		Open-Drain	IN1 < V_{IT-}	IN1 falling	OUT1 = low
			IN2 < V_{IT-}	IN2 falling	OUT2 = low
			IN1 > V_{IT+}	IN1 rising	OUT1 = high
			IN2 > V_{IT+}	IN2 rising	OUT2 = high

7.2 Functional Block Diagrams

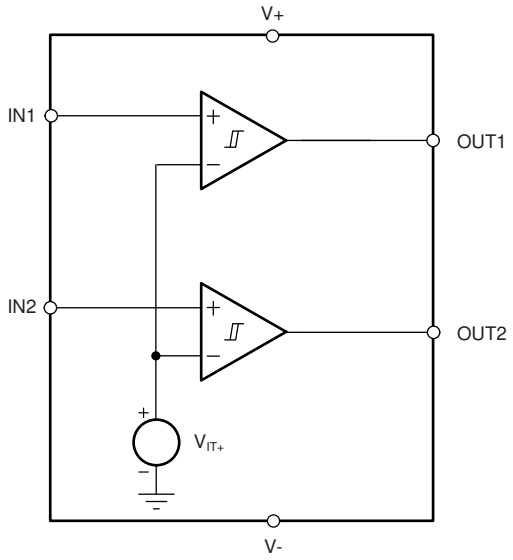


図 7-1. TLV4062-Q1 (Push-Pull Output) Block Diagram

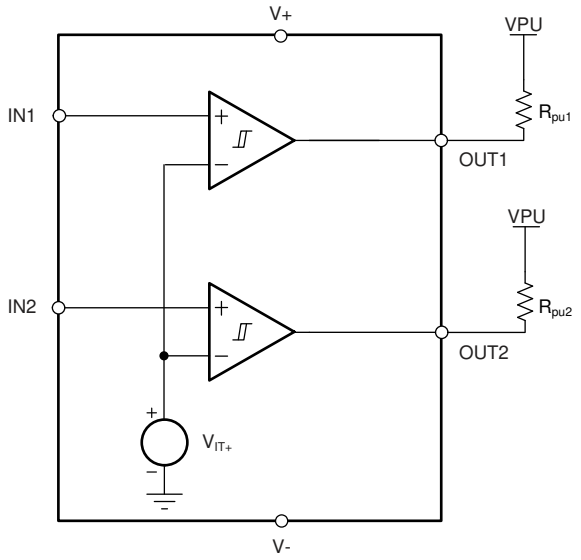


図 7-2. TLV4082-Q1 (Open-Drain Output) Block Diagram

7.3 Feature Description

The TLV4062-Q1 (push-pull) and TLV4082-Q1 (open-drain) devices are micro-power, dual-channel comparators that are capable of operating at low voltages. The TLV4062-Q1 and TLV4082-Q1 features high-accuracy integrated reference thresholds with internal hysteresis of 60mV. If the voltage at the inputs, INx, rises above the threshold, the outputs, OUTx, are driven high; if the voltage at the inputs, INx, falls below the threshold, the outputs, OUTx, are driven low.

7.4 Device Functional Modes

When the voltage on V+ is lower than $V_{(POR)}$, both outputs are undefined and are not to be relied upon for proper system function.

7.4.1 Inputs (IN1, IN2)

The TLV4062-Q1 and TLV4082-Q1 each have two comparators for voltage detection. Each comparator has one external input; the other input is connected to the internal reference. The comparator rising threshold is designed and trimmed to be equal to V_{IT+}, and the falling threshold is trimmed to be equal to V_{IT-}. The difference between V_{IT+} and V_{IT-} is referred to as the comparator hysteresis and is 60 mV. The integrated hysteresis makes the TLV40x2 less sensitive to supply-rail nose and provides stable operation in noisy environments without having to add external positive feedback to create hysteresis.

The comparator inputs can swing from ground to 5.5 V, regardless of the device supply voltage used. This includes the instance when no supply voltage is applied to the comparator (V+ = 0 V). As a result, the TLV40x2 is referred to as fault tolerant, meaning it mainitains the same high input impedance when V+ is unpowered or ramping up. Although not required in most cases, for extremely noisy applications, good analog design practice is to place a 1-nF to 10-nF bypass capacitor at the comparator input in order to reduce sensitivity to transients and layout parasitic.

For each INx input, the corresponding output (OUTx) is driven to logic low when the input voltage drops below V_{IT-}. When the voltage exceeds V_{IT+}, the output (OUTx) is driven high; see 図 6-1.

7.4.2 Outputs (OUT1, OUT2)

The TLV4062-Q1 features push-pull output stages which eliminates the need for an external pull-up resistor, thus saving board space, while providing a low impedance output driver. The logic high level of the outputs is determined by the V+ pin voltage.

The TLV4082-Q1 features open-drain output stages which enables the output logic levels to be pulled-up to an external source as high as 5.5 V independent of the supply voltage. Pull-up resistors must be used to hold these lines high when the output goes to a high-impedance condition (not asserted). By connecting pull-up resistors to the proper voltage rails, the outputs can be connected to other devices at correct interface voltage levels. To ensure proper voltage levels, make sure to choose the correct pull-up resistor values. The pull-up resistor value is determined by V_{OL}, the sink current capability, and the output leakage current ($I_{lkg(OD)}$). These values are specified in the *セクション 6.5* table. By using wired-OR logic, OUT1 and OUT2 can be combined into one logic signal. The *セクション 7.4.1* section describes how the outputs are asserted or de-asserted. See 図 6-1 for a description of the relationship between threshold voltages and the respective output.

7.4.3 Switching Threshold and Hysteresis

The TLV40x2-Q1 transfer curve is show in 図 7-3.

- V_{IT+} represents the rising input threshold that causes the comparator output to change from a logic low state to a logic high state.
- V_{IT-} represents the falling input threshold that causes the comparator output to change from logic high state to a logic low state.
- V_{HYS} represents the difference between V_{IT+} and V_{IT-} and is 60 mV for TLV40x2-Q1.

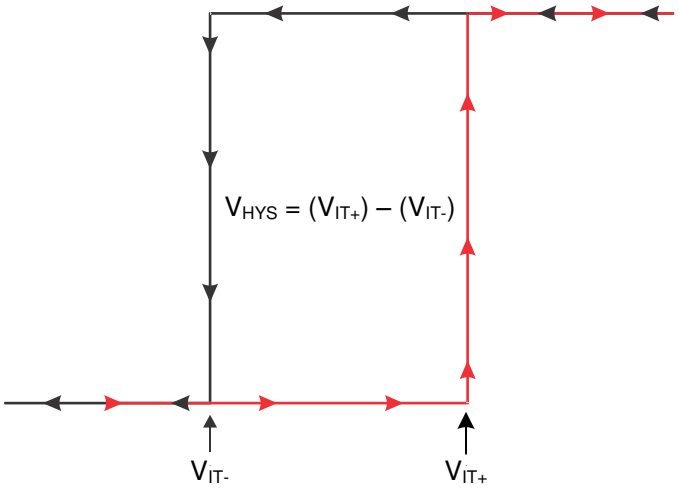


図 7-3. TLV40x2 Transfer Curve

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The TLV4062-Q1 and TLV4082-Q1 are used as precision, dual-voltage monitors. The monitored voltage, V+ voltage, and output pullup voltage (TLV4082-Q1 only) can be independent voltages or connected in any configuration.

In a typical device application, the outputs are connected to a reset or enable input of another device, such as a digital signal processor (DSP), central processing unit (CPU), field-programmable gate array (FPGA), or application-specific integrated circuit (ASIC); or the outputs are connected to the enable input of a voltage regulator, such as a dc-dc or low-dropout (LDO) regulator.

8.1.1 Threshold Overdrive

Threshold overdrive is how much V_{IN1} or V_{IN2} exceeds the specified threshold, and is important to know because a smaller overdrive results in a slower OUTx response. Threshold overdrive is calculated as a percent of the threshold in question, as shown in 式 1:

$$\text{Overdrive} = | (V_{IN1,2} / V_{IT} - 1) \times 100\% | \quad (1)$$

where

- V_{IT} is either V_{IT-} or V_{IT+}, depending on whether calculating the overdrive for the falling input threshold or the rising input threshold, respectively
- $V_{IN1,2}$ is the voltage at the IN1 or IN2 input

図 6-16 and 図 6-17 illustrates the minimum detectable pulse on the INx inputs versus overdrive, and is used to visualize the relationship that overdrive has on $t_{PD(f)}$ for high to low transitions. 図 6-18 and 図 6-19 is used to visual the relationship that overdrive has on $t_{PD(r)}$ for low to high transitions.

8.2 Typical Applications

8.2.1 Monitoring Two Separate Rails

The TLV40x2-Q1 series can be used to monitor two separate rails for over voltage detection. Over-voltage monitoring is frequently used for system protection to alert the system to shutdown to prevent from damage. The TLV4062-Q1 and TLV4082-Q1 also have adjustable INx inputs that can be configured to monitor voltages using external resistor divider, as shown in 図 8-1.

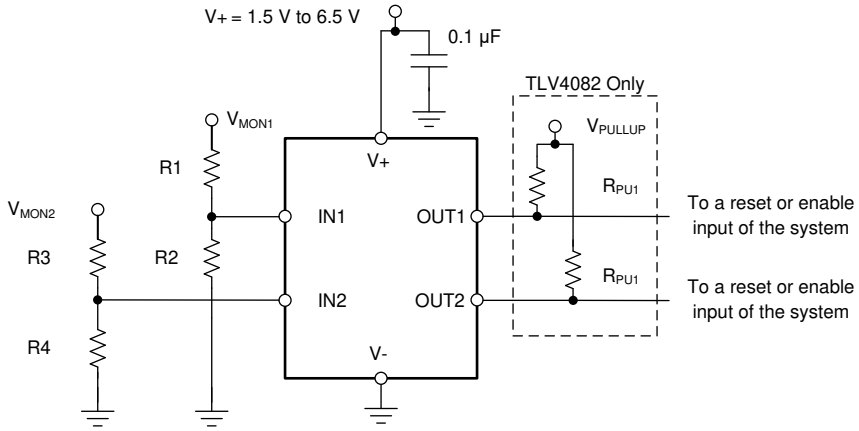


図 8-1. Monitoring Two Separate Rails Schematic

8.2.1.1 Design Requirements

For this design, follow these requirements:

- V_{MON1} = 5 V and V_{MON2} = 3.3 V
- Set V_{MON1} over-voltage condition at 6.5 V
- Set V_{MON2} over-voltage condition at 4 V

8.2.1.2 Detailed Design Procedure

Configure the circuit as shown in 図 8-1. Connect V+ to a power supply that is compatible with the input logic level of the device connected to the output, and connect V- to ground. Resistors R_1 and R_2 create the over-voltage alert level at 6.5 V and resistors R_3 and R_4 create the over-voltage alert level at 4 V. When the V_{MON} rises, the resistor divider voltage crosses V_{IT+}. This causes the comparator output to transition from a logic low level (normal operation), to a logic high level. When V_{MON} falls back down and the resistor divider voltage crosses V_{IT-} and signal that the system is approaching normal operating voltage levels once again. Make sure to set V_{MON} at a value below the absolute maximum voltage of the system in question.

$$V_{IT+} = \frac{R_2}{R_2+R_1} \times V_{MON} \tag{2}$$

where

- R_1/R_3 and R_2/R_4 are the resistor values for the resistor divider connected to INx
- V_{MON} is the voltage source that is being monitored for an over-voltage condition
- V_{IT+} is the rising edge threshold where the comparator output changes state from low to high

Rearranging 式 2 and solving for R_1 yields 式 3. Set R_2/R_4 to a fixed value.

$$R_1 = \frac{V_{MON} - V_{IT+}}{V_{IT+}} \times R_2 \tag{3}$$

Using the nearest 1% resistors and the equation above, R_1 = 300 kΩ, R_2 =1.33 MΩ, R_3 = 953 kΩ, and R_4 = 407 kΩ. To get the trip point as close as possible to rising threshold, V_{IT+}, V_{MON} are adjusted so that V_{MON1} = 6.49 V and V_{MON2} = 3.99 V. Using equation 式 4 will determine when the output will fall low (crossing V_{IT-}). The over-voltage signal will go low when V_{MON1} = 6.16 V and V_{MON2} = 3.79 V.

$$V_{MON} = \frac{R_2+R_1}{R_2} \times V_{IT-} \tag{4}$$

where

- V_{MON} is the voltage at which the resistor divider crosses the falling threshold, V_{IT-}.

Choose R_{TOTAL} (equal to R1 + R2 & R3 + R4) so that the current through the divider is approximately 100 times higher than the input current at the INx pins. The resistors can have high values to minimize current consumption as a result of low input bias current without adding significant error to the resistive divider. For details on sizing input resistors, see the *Optimizing Resistor Dividers at a Comparator Input* application report (SLVA450), available for download from www.ti.com.

8.2.1.3 Application Curve

図 8-2 shows the simulated results of monitoring two independent voltage rails for an over-voltage event.

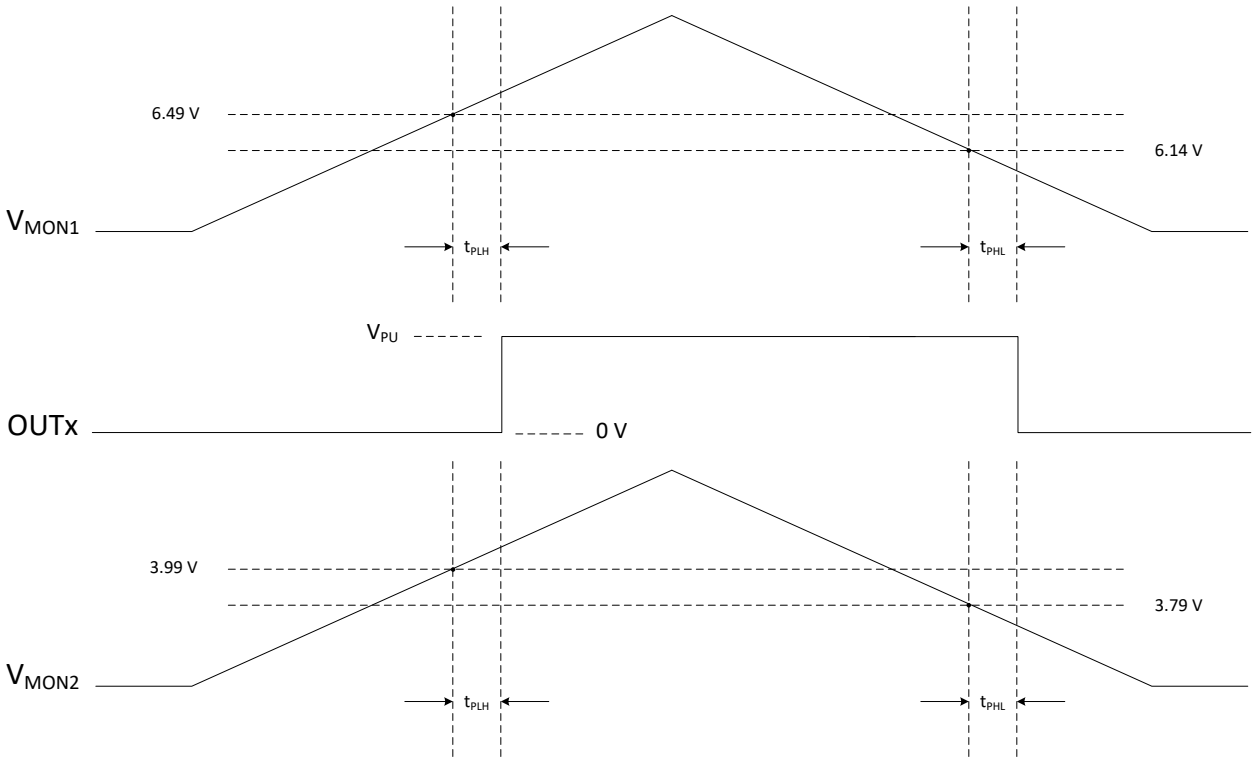


図 8-2. Overvoltage Detection

8.2.2 Early Warning Detection

The TLV40x2-Q1 series can be used to monitor for early warning detection where OUT1 sends an early warning alert signal and OUT2 sends an alert signal. This type of topology can be used for sensitive systems so a warning alert can trigger before system shutdown occurs. The TLV4062-Q1 and TLV4082-Q1 also have adjustable INx inputs that can be configured to monitor voltages using external resistor divider, as shown in 図 8-3.

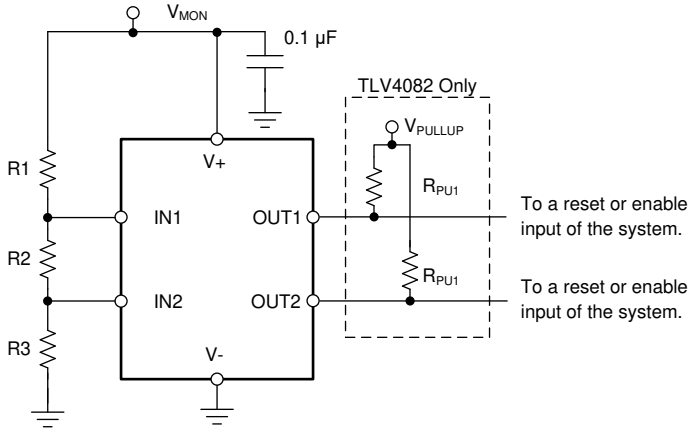


図 8-3. Early Warning Detection Schematic

8.2.2.1 Design Requirements

For this design, follow these requirements:

- V_{MON} = 3.3V
- Set the transition points V_{MON1} = 3.5 V and V_{MON2}= 3.9 V

8.2.2.2 Detailed Design Procedure

Configure the circuit as shown in 図 8-3. Connect V+ to a 3.3 V power rail and connect V- to ground. The resistor network is used to create an early warning detection signal at OUT2, which will give a warning alert as V_{MON} approaches the max limit, changing state from a logic low to a logic high. OUT2 will stay high for a longer period until V_{MON} is no longer in the warning zone. OUT1 will be used when V_{MON} reaches the max limit and transition from a logic low to a logic high. This type of topology can be used for sensitive systems where advanced notice of the power supply over-voltage detection is needed.

Use V_{MON2}, the threshold for a low to high transition at OUT2, I_{IN_RES}, the current flow through the resistor network, to determine the minimum total resistance necessary to achieve the current consumption specification.

$$R_{total} = \frac{V_{MON\,2}}{I_{IN\_RES}} \tag{5}$$

where

- V_{MON2} is the target voltage at which OUT2 goes high when V_{MON} rises
- I_{IN_RES} is the current flowing through the resistor network

After R_{TOTAL} is determined, R3 can be calculated using 式 6. Select the nearest 1% resistor value for R3. In this case, 845 kΩ is the closest value.

$$R_3 = \frac{V_{IT+}}{I_{IN\_RES}} \tag{6}$$

Use the voltage divider equation 式 7 The voltage divider equation controls the V_{MON1} voltage at which OUT1 will transition from a logic high to a logic low.

$$V_{IT+} = \frac{R_2+R_3}{R_{TOTAL}} \times V_{MON\,1} \tag{7}$$

where

- V_{MON1} is the target voltage at which OUT1 goes low when V_{MON} falls

Rearranging 式 7 to solve for R2 yields 式 8 Select the nearest 1% resistor value for R2. In this case, 55.6kΩ is the closest value.

$$R_2 = \frac{R_{TOTAL}}{V_{MON\,1}} \times V_{IT-} - R_3 \tag{8}$$

Use 式 9 to calculate R1. Select the nearest 1% resistor value for R1. In this case, 1.87 MΩ is a 1% resistor.

$$R_1 = R_{TOTAL} - R_2 - R_3 \tag{9}$$

8.2.2.3 Application Curve

図 8-4 shows the simulated results of the early warning detection circuit. OUT2 provides the early warning alert whereas OUT1 provides the warning alert.

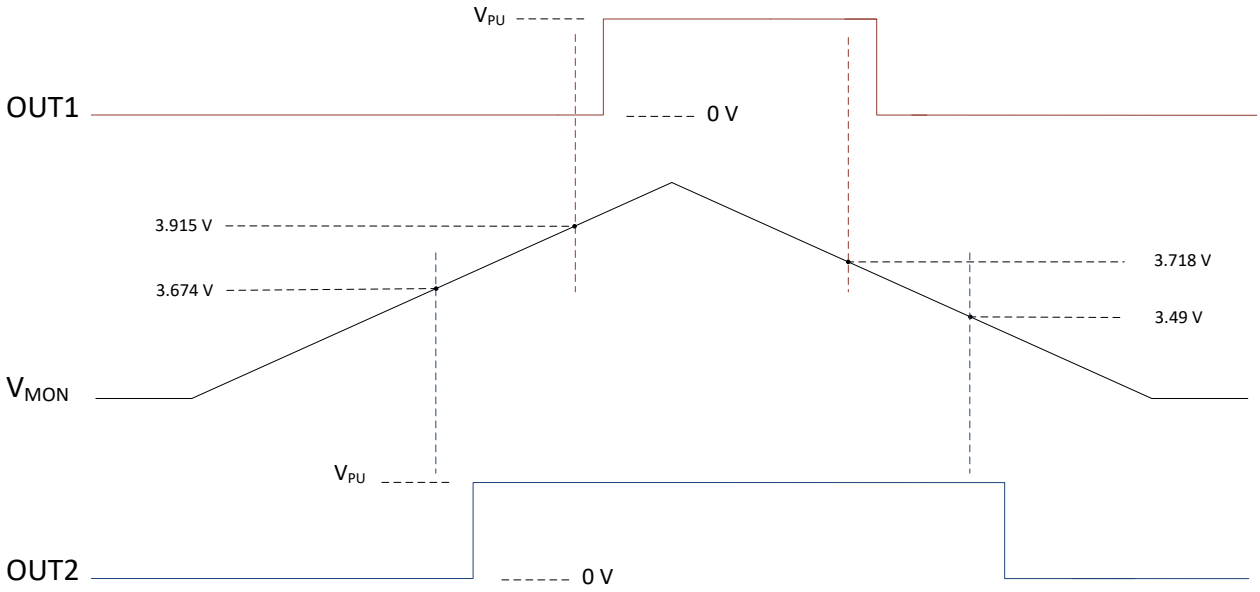


図 8-4. Early Warning Detection

8.2.3 Additional Application Information

8.2.3.1 Pull-Up Resistor Selection

For the TLV4082-Q1 (open-drain outputs), care should be taken in selecting the pull-up resistor (R_{PU}) value to ensure proper output voltage levels. First, consider the required output high logic level requirement of the logic device that is being drive by the comparator when calculating the maximum R_{PU} value. When in a logic high output state, the output impedance of the comparator is very high but there is finite amount of leakage current that needs to be accounted for. Use the $|I_{lkg(OD)}|$ from the EC table and the $V_{IH\ (min)}$ of the logic device being driven by the TLV4082 to determine R_{PU} using 式 10 .

$$R_{PU}(max) = \frac{(V_{PU} - V_{IH(min)})}{I_{O-LKG}} \tag{10}$$

Next determine the minimum value for R_{PU} by using the $V_{IL\ (max)}$ of the logic device being driven by the TLV4082-Q1. In order for the comparator output to be recognized as a logic low, $V_{IL\ (max)}$ is used to determine the upper boundary of the comparator's V_{OL}. $V_{OL\ (max)}$ for the comparator is available in the EC table from specific sink current levels and can be found from the V_{OUT} versus I_{SINK} curve in the Typical Applications curve. A good design practice is to choose a value for V_{OL} that is ½ the value of V_{IL} for the input logic device. The corresponding sink current and V_{OL} value will be needed to calculate the minimum R_{PU}. This method will ensure enough noise margin for the logic low level. With i_{SINK} determined and the corresponding R_{PU} obtained, the minimum) is calculated with 式 11.

$$R_{PU}(min) = \frac{(V_{PU} - V_{OL(max)})}{I_{SINK}} \tag{11}$$

Since the range of possible R_{PU} values is large, a value between 5 kΩ and 100kΩ is generally recommended. A smaller R_{PU} value provides faster output transition time and better noise immunity, while a larger R_{PU} value consumes less power when in a logic low output state.

8.2.3.2 INx Capacitor

Although not required in most cases, for extremely noisy applications, place a 1 nF to 100 nF bypass capacitor from the comparator input (INx) to the (V-) for good analog design practice. This capacitor placement reduces device sensitivity to transients.

9 Power Supply Recommendations

The TLV4062-Q1 and TLV4082-Q1 are designed to operate from an input voltage supply range between 1.5 V and 5.5V. An input supply capacitor is not required for this device; however, good analog practice is to place a 0.1-µF or greater capacitor between the V+ pin and the GND pin. This device has a 7-V absolute maximum rating on the V+ pin. If the voltage supply providing power to V+ is susceptible to any large voltage transient that can exceed 7 V, additional precautions must be taken.

For applications where INx is greater than 0 V before V+, and is subject to a startup slew rate of less than 200 mV per 1 ms, the output can be driven to logic high in error. To correct the output, cycle the INx lines below V_{IT-} or sequence INx after V+.

10 Layout

10.1 Layout Guidelines

Place the V+ decoupling capacitor close to the device.

Avoid using long traces for the V+ supply node. The V+ capacitor, along with parasitic inductance from the supply to the capacitor, can form an LC tank circuit that creates ringing with peak voltages above the maximum V+ voltage.

10.2 Layout Example

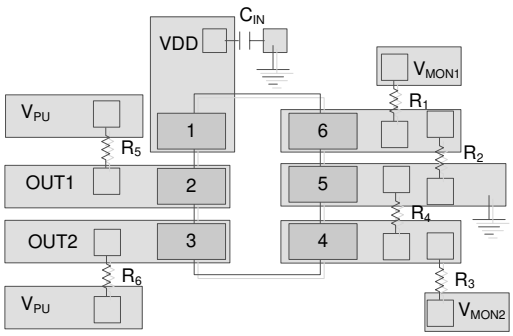


図 10-1. Example SOT-23 Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 サポート・リソース

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11.6 用語集

TI 用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV4062QDBVRQ1	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2DK5
TLV4062QDBVRQ1.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2DK5
TLV4082QDBVRQ1	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2DJ5
TLV4082QDBVRQ1.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2DJ5

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TLV4062-Q1, TLV4082-Q1 :

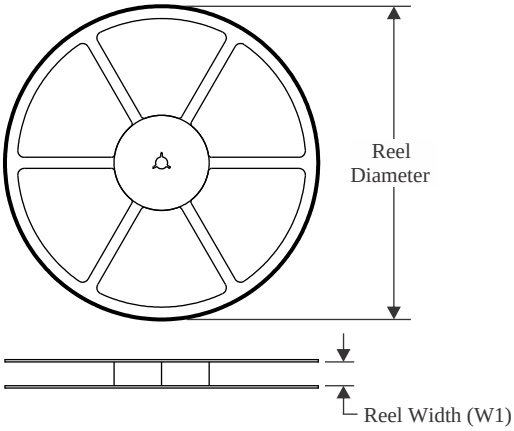
- Catalog : TLV4062, TLV4082

NOTE: Qualified Version Definitions:

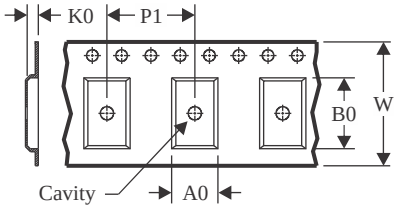
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

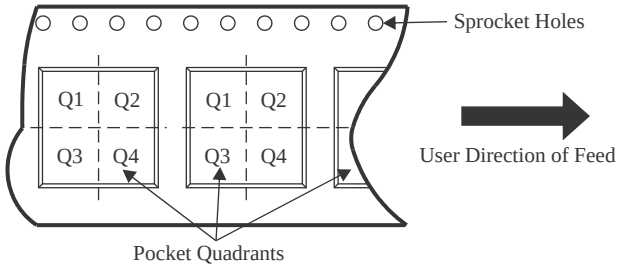


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

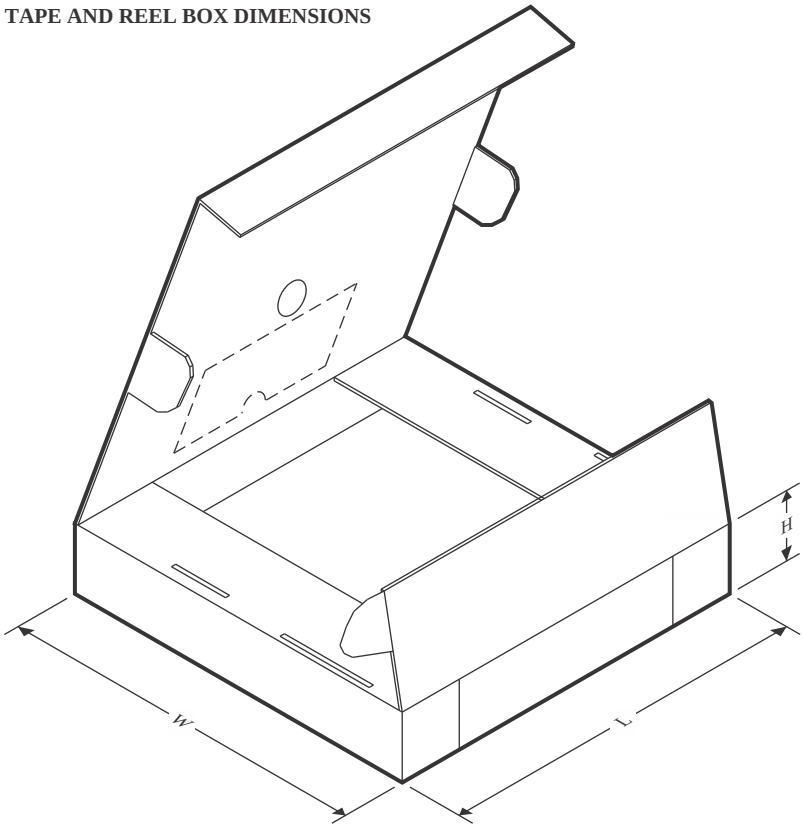
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV4062QDBVRQ1	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV4082QDBVRQ1	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

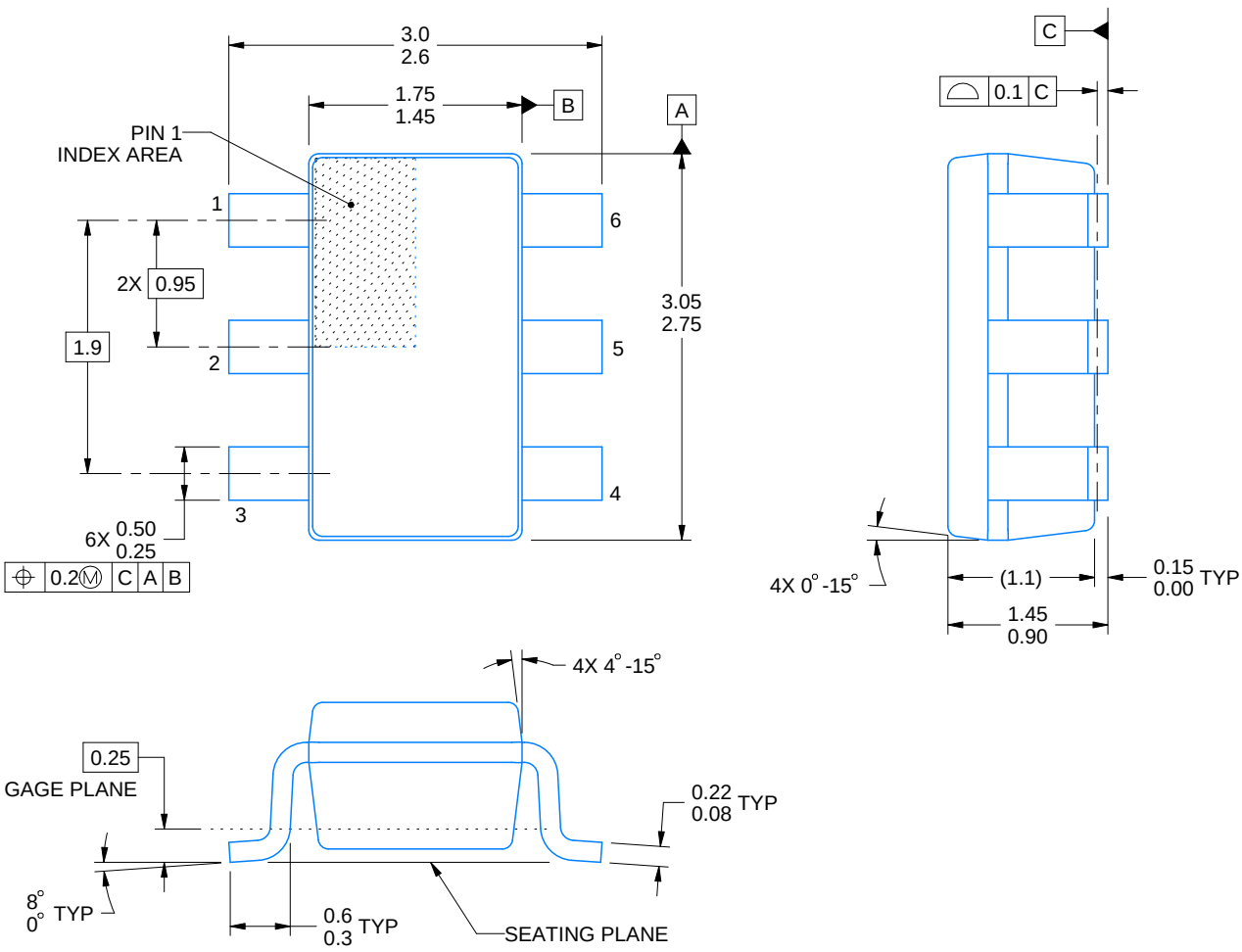
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV4062QDBVRQ1	SOT-23	DBV	6	3000	180.0	180.0	18.0
TLV4082QDBVRQ1	SOT-23	DBV	6	3000	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

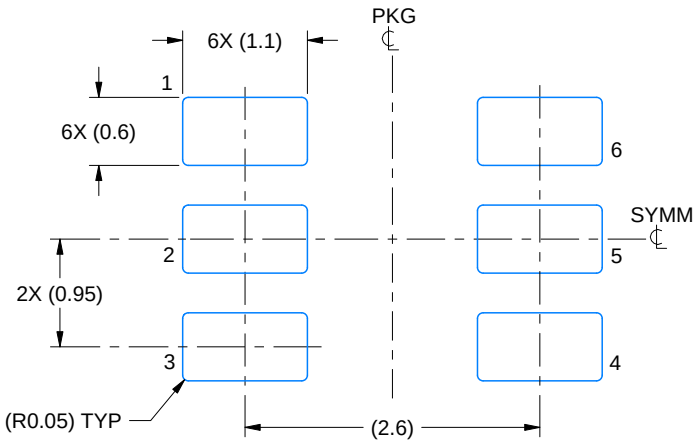
SMALL OUTLINE TRANSISTOR



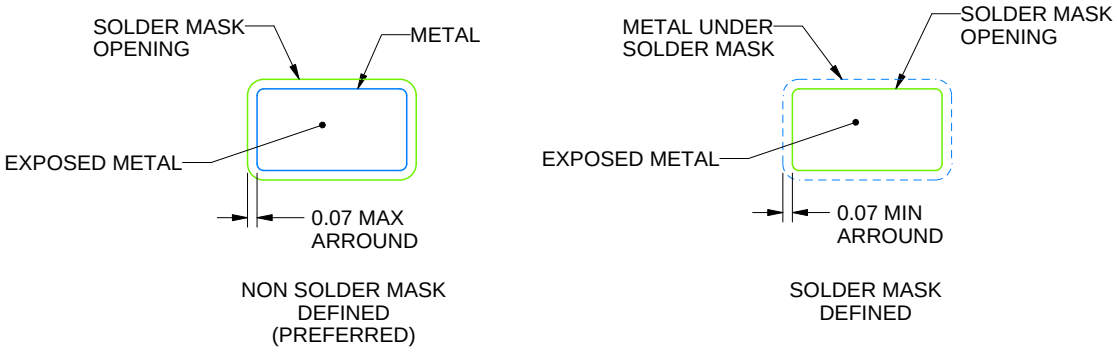
4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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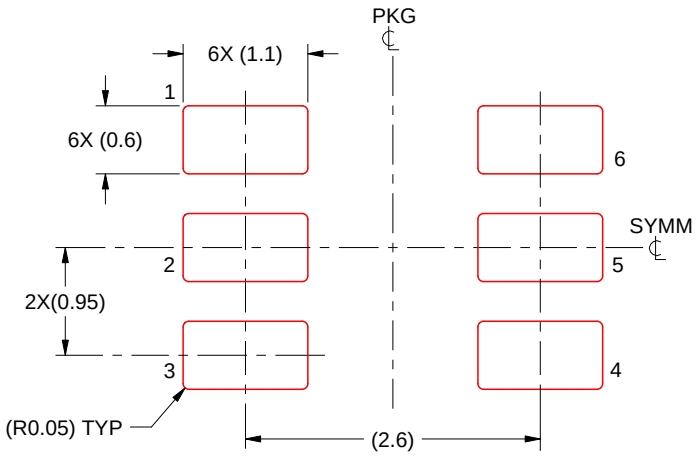
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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