TLV3801-Q1/TLV3802-Q1 LVDS 出力、225ps の高速コンパレータ

1 特長

- 小さい伝搬遅延時間:225ps
- 小さいオーバードライブ分散:5ps
- 静止電流:19 mA
- 高いトグル周波数:3GHz/6Gbps
- 狭パルス幅検出性能:240ps
- LVDS 出力
- 入力と出力のグランド基準電圧を分離
- 単一電源電圧:2.7V～5.25V
- 低い入力オフセット電圧:±0.5mV
- 内部ヒステリシス:2mV
- パッケージ:TLV3801-Q1 (8 ピン WSON)、TLV3802-Q1 (12 ピン WSON)

2 アプリケーション

- LIDAR の距離センシング
- タイム・オブ・フライト (ToF) センサ
- オシロスコープとロジック・アナライザの高速トリガ機能
- 高速差動ライン・レシーバ
- ドローン・ビジョン

3 概要

TLV380x-Q1 は、広い電源電圧範囲と 3GHz の非常に高いトグル周波数に対応する 225ps 高速コンパレータです。動作電源電圧範囲が 2.7V～5.25V (単一電源の場合)、2.7V～5.25V (分割電源の場合) であることに加えて、これらの機能はすべて業界標準の小型パッケージで供給されるため、これらのデバイスは LIDAR、差動ライン・レシーバ・アプリケーション、試験 / 測定システムに最適です。

TLV380x-Q1 は、5ps という非常に強力な入力オーバードライブ性能と、わずか 240ps の狭パルス幅性能を備えています。ばらつきの小さい伝搬遅延特性 (入力オーバードライブ起因) と、短いパルスを検出する能力を併せ持つこれらのデバイスは、ファクトリ・オートメーション、ドローン・ビジョンなどのタイム・オブ・フライト (ToF) アプリケーションに最適です。

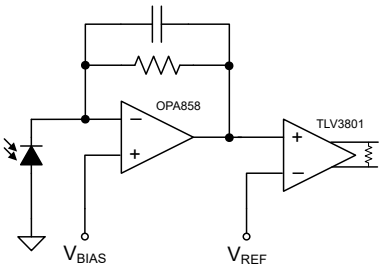
TLV380x-Q1 の低電圧差動信号 (LVDS) 出力は、データスループットの向上と消費電力の最適化にも役立ちます。同様に相補出力は、各出力の同相ノイズを抑制することで、EMI 低減に役立ちます。LVDS 出力は、アプリケーション内の下流の大半の FPGA や CPU など、標準 LVDS 入力を受け入れるその他のデバイスの直接駆動およびインターフェイスを可能にします。

TLV3801-Q1 は 8 ピン WSON パッケージ、TLV3802-Q1 はウェッタブル フランク付きの 12 ピン WSON パッケージで提供されているため、スペースの制約が厳しい車載用アプリケーションに適しています。

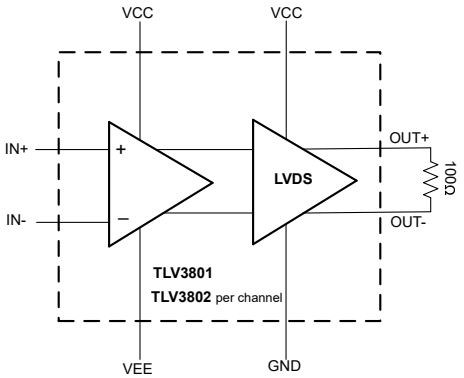
製品情報

部品番号	パッケージ (1)	本体サイズ (公称)
TLV3801-Q1	WSON (8)	2.00mm × 2.00mm
TLV3802-Q1	WSON (12)	3.00mm × 2.00mm

1. 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。



TLV3801 光レシーバ回路



機能ブロック図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (October 2022) to Revision A (December 2023)	Page
• データシート全体にわたって TLV3802-Q1 を追加	1

5 Pin Configuration and Functions

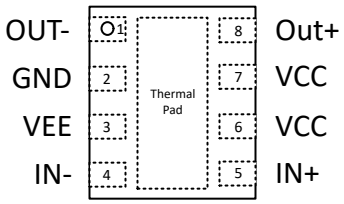


図 5-1. WSON Package
8-Pin DSG
Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	TLV3801		
IN+	5	I	Non-inverting input
IN–	4	I	Inverting input
OUT+	8	O	Non-inverting output
OUT–	1	O	Inverting output
V_{EE}	3	I	Negative power supply (If using single supply, connect to GND)
V_{CC}	6, 7	I	Positive power supply
GND	2	I	Ground

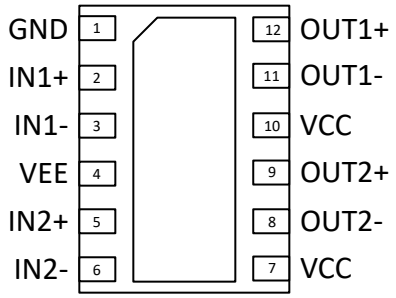


図 5-2. WSON Package
12-Pin DSS
Top View

表 5-2. Pin Functions

PIN		I/O	DESCRIPTION
NAME	TLV3802		
GND	1	I	Ground
IN1+	2	I	Channel 1 Non-inverting input
IN1–	3	I	Channel 1 Inverting input
VEE	4	I	Negative power supply (If using single supply, connect to GND)
IN2+	5	I	Channel 2 Non-inverting input
IN2–	6	I	Channel 2 Inverting input
VCC	7	I	Positive power supply
OUT2–	8	O	Channel 2 Inverting output
OUT2+	9	O	Channel 2 Non-inverting output
VCC	10	I	Positive power supply
OUT1–	11	O	Channel 1 Inverting output
OUT1+	12	O	Channel 1 Non-inverting output
Thermal Pad	–	–	Connect directly to VEE

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage: (V_{CC} – V_{EE}) and (V_{CC} – GND) (2)	–0.3	5.5	V
Input pins (IN+, IN–) from V_{EE} (3)	V_{EE} – 0.3	V_{CC} + 0.3	V
Current into input pins (IN+, IN–)	–10	10	mA
Output (OUT+, OUT–)	GND	V_{CC}	V
Current into output pins (OUT+, OUT–)		10	mA
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) VEE less than or equal to GND
(3) Input terminals are diode-clamped to V_{EE} and V_{CC}

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), , per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-0111	±1000	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Thermal Information

THERMAL METRIC(1)		TLV3801-Q1 DSG (WSON) 8 PINS	TLV3802-Q1 DSS (WSON) 12 PINS	UNIT
R_{qJA}	Junction-to-ambient thermal resistance	69.4	63.2	°C/W
$R_{qJC(top)}$	Junction-to-case (top) thermal resistance	95.7	61.9	°C/W
R_{qJB}	Junction-to-board thermal resistance	36.2	30.7	°C/W
y_{JT}	Junction-to-top characterization parameter	3.5	2.4	°C/W
y_{JB}	Junction-to-board characterization parameter	36.0	30.7	°C/W
$R_{qJC(bot)}$	Junction-to-case (bottom) thermal resistance	9.4	8.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Single supply operation: V_{CC} – V_{EE} with V_{EE} = GND	2.7	5.25	V
Split supply operation: V_{CC} – V_{EE} with V_{EE} < GND	2.7	5.25	V
Split supply operation: V_{CC} – GND with V_{EE} < GND	2.4	5.25	V
Input voltage range	V_{EE} + 1.5	V_{CC} + 0.1	V
Differential Input voltage range	–1.5	+1.5	V
Ambient temperature, T_A	–40	125	°C

6.5 Electrical Characteristics

For V_{CC} = 3.3 V, V_{EE} = GND = 0, V_{CM} = 2.5 V at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC Input Characteristics						
V_{OS}	Input offset voltage	T_A = –40°C to +125°C	–5(1)	±0.5	+5(1)	mV
V_{HYS}	Input hysteresis voltage			2		mV
$V_{CM-Range}$	Common-mode voltage range	Single Supply: V_{EE} = GND V_{CC} – V_{EE} = 2.7 V to 5.25 V T_A = –40 °C to +125°C	V_{EE} + 1.5		V_{CC}	V
$V_{CM-Range}$	Common-mode voltage range	Split Supply: V_{EE} < GND V_{CC} – V_{EE} = 2.7 V to 5.25 V and V_{CC} – GND = 2.4 V to 5.25 V T_A = –40 °C to +125°C	V_{EE} + 1.5		V_{CC}	V
CMRR	Common mode rejection ratio	V_{CM} = V_{EE} + 1.5V to V_{CC}		80		dB
PSRR	Power supply rejection ratio	Single Supply: V_{EE} = GND V_{CC} – V_{EE} = 2.7 V to 5.25 V		80		dB
PSRR	Power supply rejection ratio	Split Supply: V_{EE} < GND V_{CC} – V_{EE} = 2.7 V to 5.25 V and V_{CC} – GND = 2.4 V to 5.25 V		80		dB
I_B	Input bias current	T_A = –40 °C to +125 °C	–10	2	10	µA
I_{OS}	Input offset current	T_A = –40 °C to +125 °C	–4	±0.1	4	µA
C_{IC}	Input capacitance, common mode			1		pF
DC Output Characteristics						
V_{OCM}	Output common mode voltage	V_{CC} - GND ≥ 2.6 V T_A = –40°C to +125°C	1.125	1.25	1.375	V
	Output common mode voltage	V_{CC} - GND < 2.6 V T_A = –40°C to +125°C	0.92	1.2	1.29	V
ΔV_{OCM}	Output common mode voltage mismatch	T_A = –40°C to +125°C	–30		30	mV
V_{OCM_PP}	Peak-to-Peak output common mode voltage			50		mVpp
V_{OD}	Differential output voltage	T_A = –40°C to +125°C	250	350	450	mV
ΔV_{OD}	Differential output voltage mismatch	T_A = –40°C to +125°C	-30		30	mV
Power Supply						
I_Q (TLV3801)	Quiescent current per comparator	T_A = –40°C to +125°C		20	26.6	mA
I_Q (TLV3802)	Quiescent current per comparator	T_A = –40°C to +125°C		19	23.5	mA
AC Characteristics						
t_{PD}	Propagation delay	$V_{OVERDRIVE}$ = 50 mV, $V_{UNDERDRIVE}$ = 50 mV, 50 MHz Squarewave		225		ps
Tempco of t_{PD}	Temperature Coefficient of propagation delay			±0.2		ps/°C
t_{PD_SKEW}	Propagation delay skew	$V_{OVERDRIVE}$ = 50mV, $V_{UNDERDRIVE}$ = 50 mV, 50 MHz Squarewave		±2.5		ps

6.5 Electrical Characteristics (続き)

For V_{CC} = 3.3 V, V_{EE} = GND = 0, V_{CM} = 2.5 V at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Δt_{PD} (TLV3802 only)	Channel-to-channel propagation delay skew	$V_{OVERDRIVE}$ = $V_{UNDERDRIVE}$ = 50mV, 50 MHz Squarewave		6		ps
$t_{CM\_DISPERSION}$	Common mode dispersion	V_{CM} varied from V_{CM} (min) to V_{CM} (max)		2		ps
$t_{OD\_DISPERSION}$	Overdrive dispersion	Overdrive varied from 20 mV to 100 mV		5		ps
$t_{OD\_DISPERSION}$	Overdrive dispersion	Overdrive varied from 10 mV to 1 V		15		ps
$t_{UD\_DISPERSION}$	Underdrive dispersion	Underdrive varied from 20 mV to 100 mV		7		ps
$t_{UD\_DISPERSION}$	Underdrive dispersion	Underdrive varied from 10 mV to 1 V		10		ps
t_R	Rise time	20% to 80%		135		ps
t_F	Fall time	80% to 20%		135		ps
f_{TOGGLE}	Input toggle frequency	V_{IN} = 200 mV_{PP} Sine Wave, V_{OD} = 550 mV		2.3		GHz
f_{TOGGLE}	Input toggle frequency	V_{IN} = 200 mV_{PP} Sine Wave, 50% Output swing		3		GHz
TR	Toggle Rate	V_{IN} = 200 mV_{PP} Sine Wave, V_{OD} = 550 mV		4.6		Gbps
TR	Toggle Rate	V_{IN} = 200 mV_{PP} Sine Wave, 50% Output swing		6		Gbps
PulseWidth	Minimum allowed input pulse width	$V_{OVERDRIVE}$ = $V_{UNDERDRIVE}$ = 50mV PW_{OUT} = 90% of PW_{IN}		240		ps

(1) Ensured by charaterization

6.6 Timing Diagrams

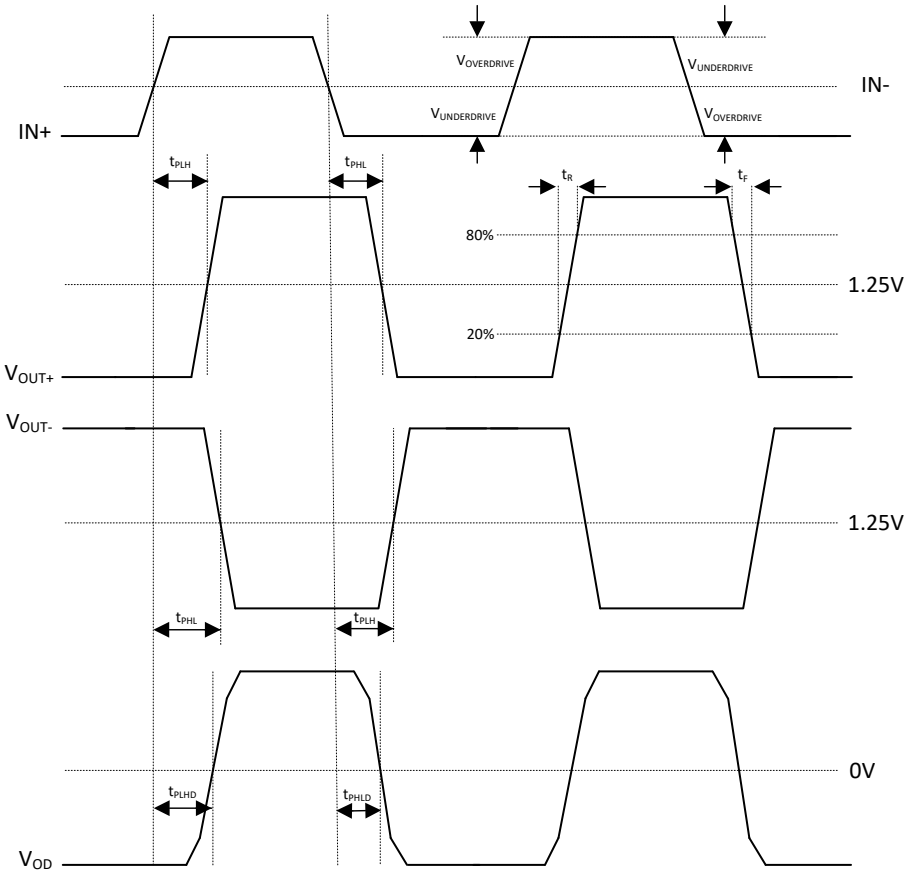


図 6-1. General Timing Diagram

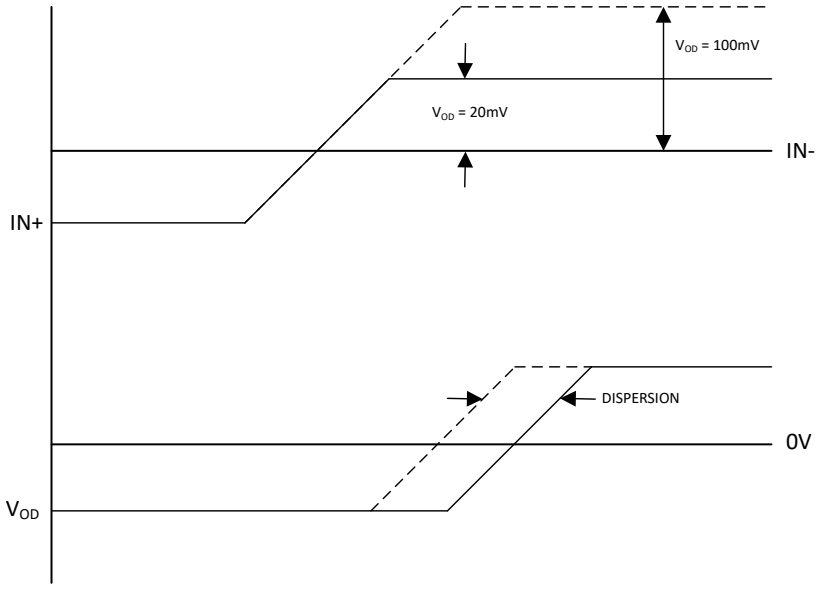


図 6-2. Overdrive Dispersion

6.7 Typical Characteristics

At T_A = 25°C, V_{CC} - V_{EE} = 3.3 V to 5 V while V_{EE} = GND = 0, V_{CM} = 2.5 V, and input overdrive/underdrive = 50 mV, unless otherwise noted.

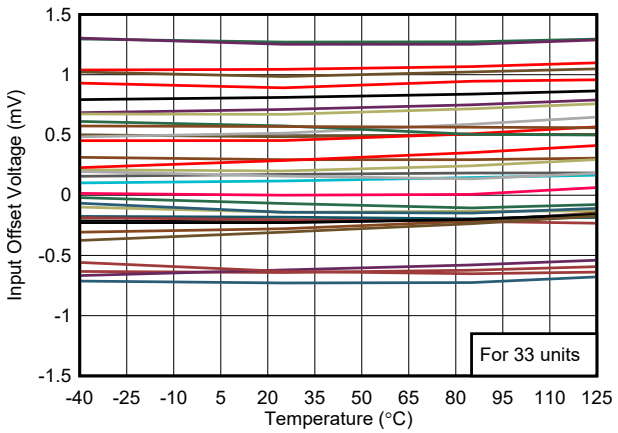


図 6-3. Offset vs. Temperature

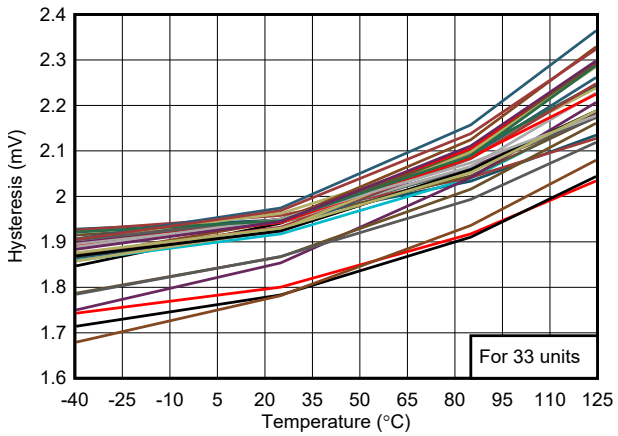


図 6-4. TLV3801 Hysteresis vs. Temperature

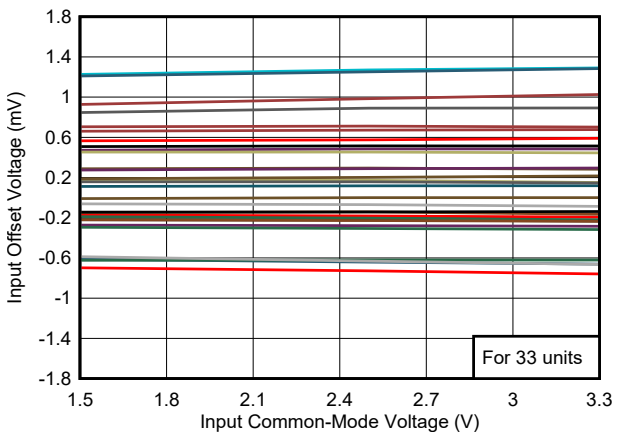


図 6-5. Offset vs. Common-Mode, 3.3 V

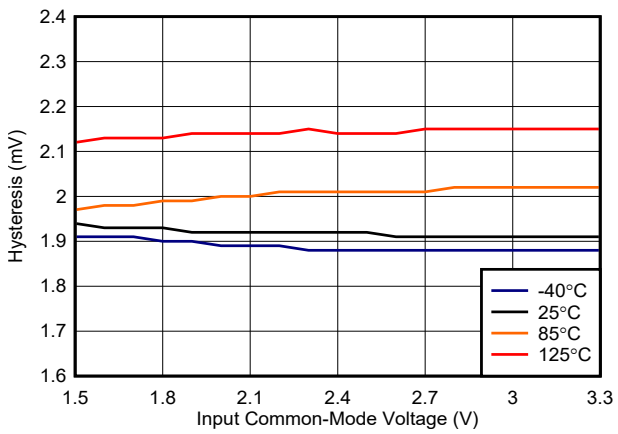


図 6-6. TLV3801 Hysteresis vs. Common-Mode, 3.3 V

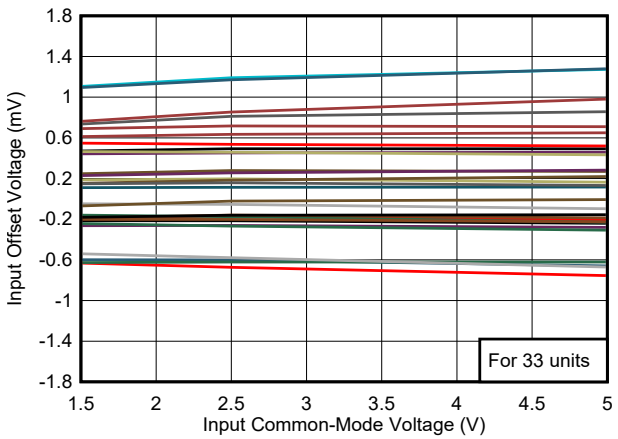


図 6-7. Offset vs. Common-Mode, 5 V

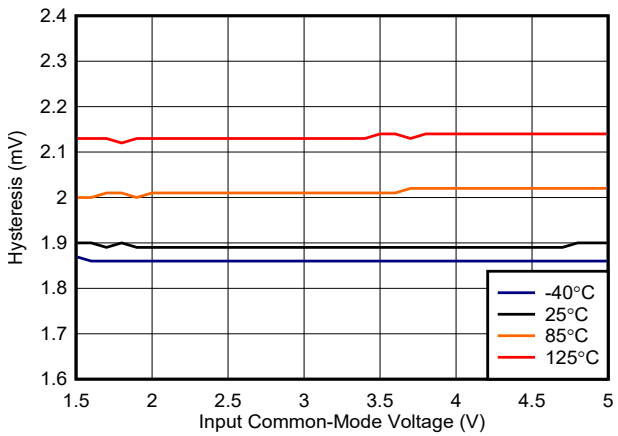


図 6-8. TLV3801 Hysteresis vs. Common-Mode, 5 V

6.7 Typical Characteristics (continued)

At T_A = 25°C, V_{CC} - V_{EE} = 3.3 V to 5 V while V_{EE} = GND = 0, V_{CM} = 2.5 V, and input overdrive/underdrive = 50 mV, unless otherwise noted.

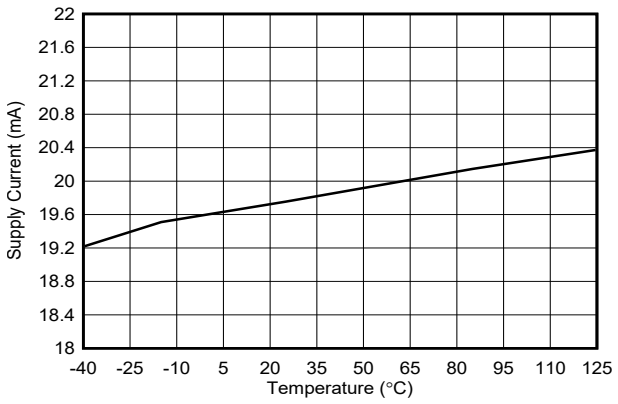


図 6-9. Supply Current vs. Temperature, Output Low

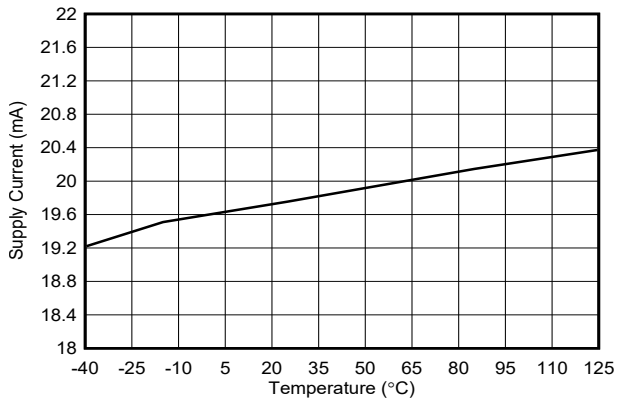


図 6-10. Supply Current vs. Temperature, Output High

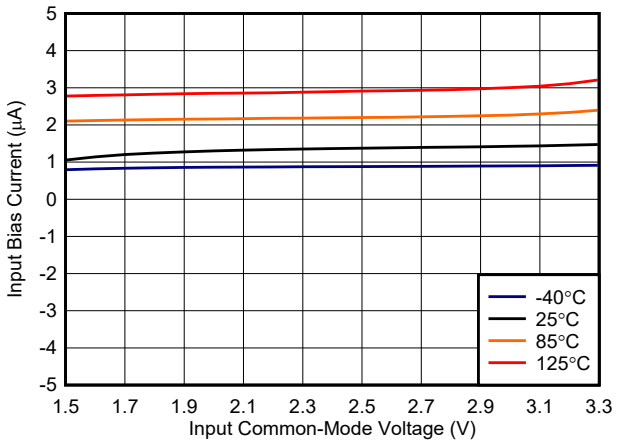


図 6-11. Bias Current vs. Common-Mode, 3.3 V

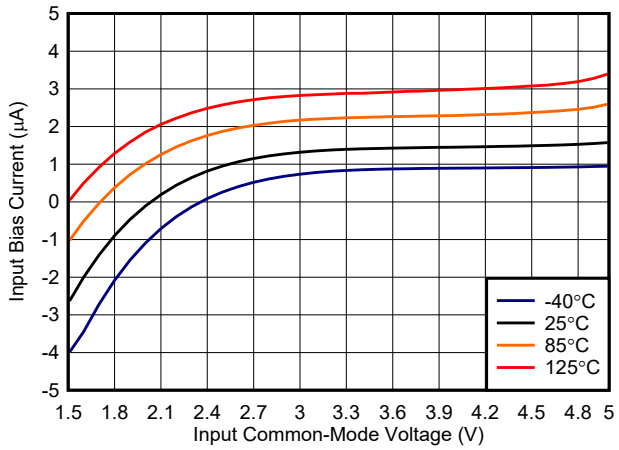


図 6-12. Bias Current vs. Common-Mode, 5 V

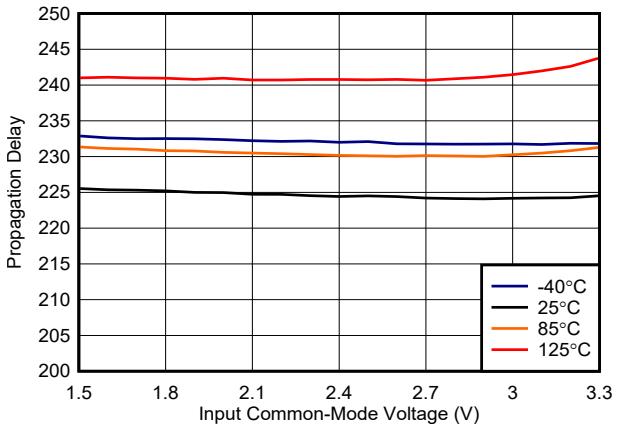


図 6-13. Propagation Delay vs. Common-Mode, 3.3 V

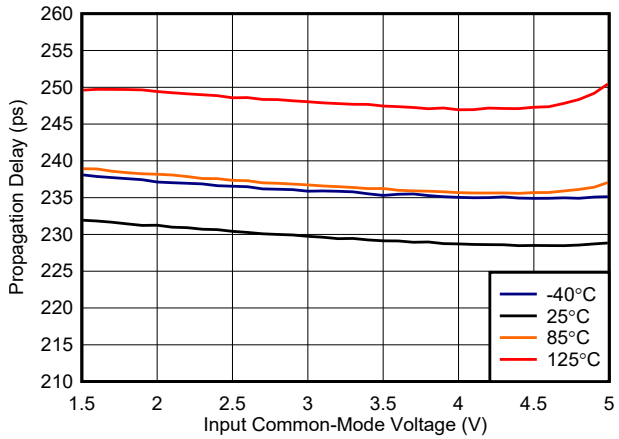


図 6-14. Propagation Delay vs. Common-Mode, 5 V

6.7 Typical Characteristics (continued)

At T_A = 25°C, V_{CC} - V_{EE} = 3.3 V to 5 V while V_{EE} = GND = 0, V_{CM} = 2.5 V, and input overdrive/underdrive = 50 mV, unless otherwise noted.

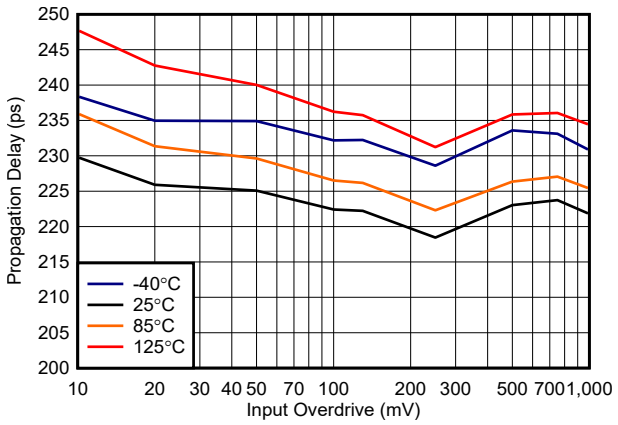


図 6-15. Propagation Delay vs. Overdrive, 3.3 V

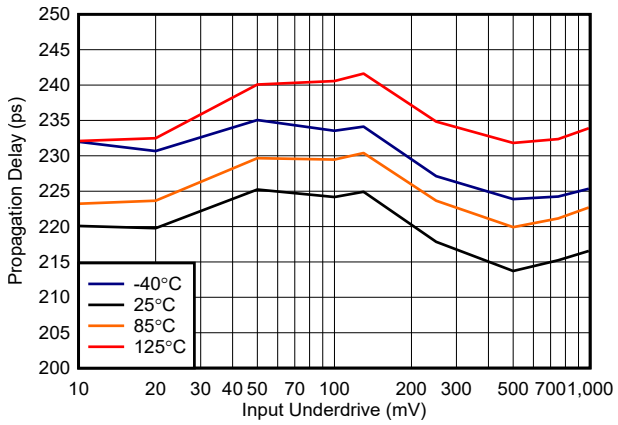


図 6-16. Propagation Delay vs. Underdrive, 3.3 V

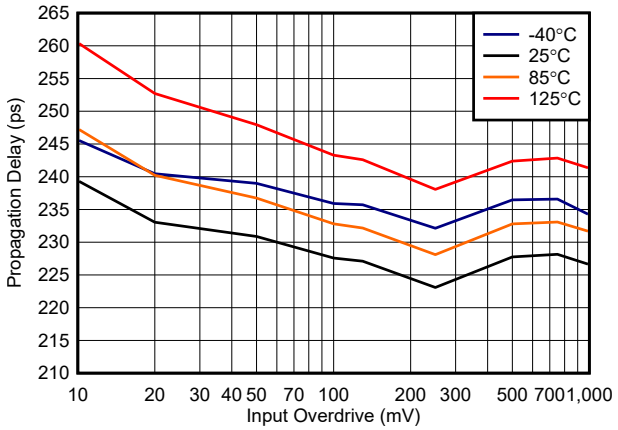


図 6-17. Propagation Delay vs. Overdrive, 5 V

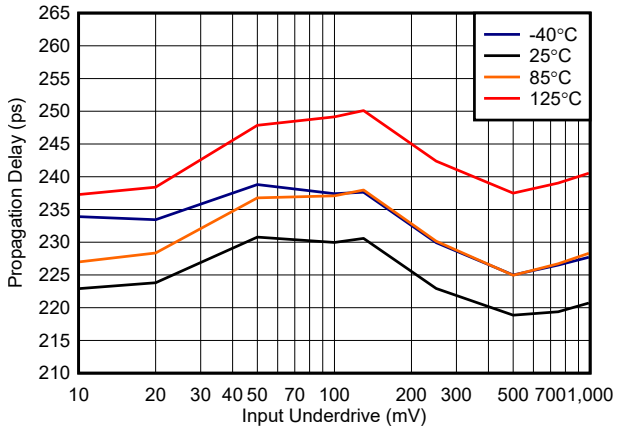


図 6-18. Propagation Delay vs. Underdrive, 5 V

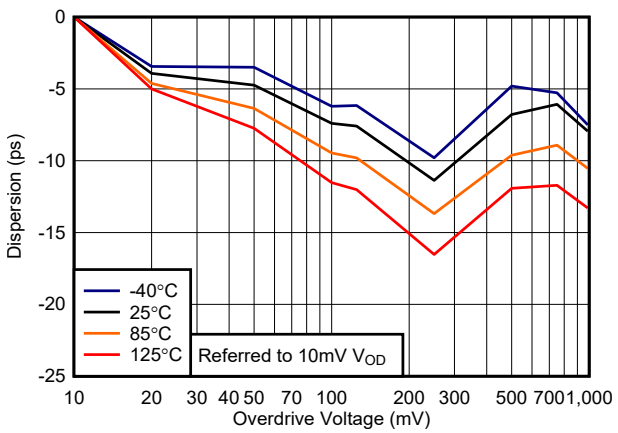


図 6-19. Dispersion vs. Overdrive, 3.3 V

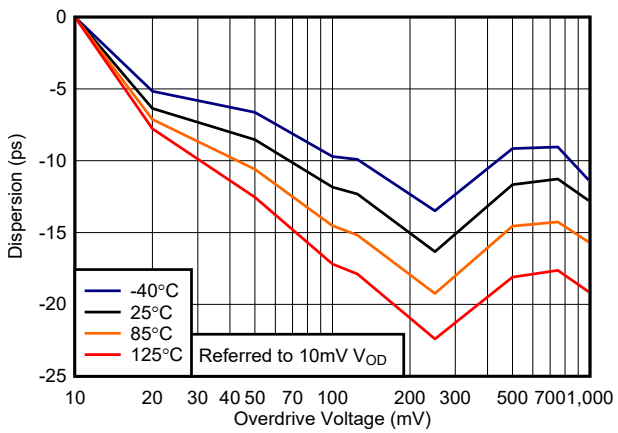


図 6-20. Dispersion vs. Overdrive, 5 V

6.7 Typical Characteristics (continued)

At T_A = 25°C, V_{CC} - V_{EE} = 3.3 V to 5 V while V_{EE} = GND = 0, V_{CM} = 2.5 V, and input overdrive/underdrive = 50 mV, unless otherwise noted.

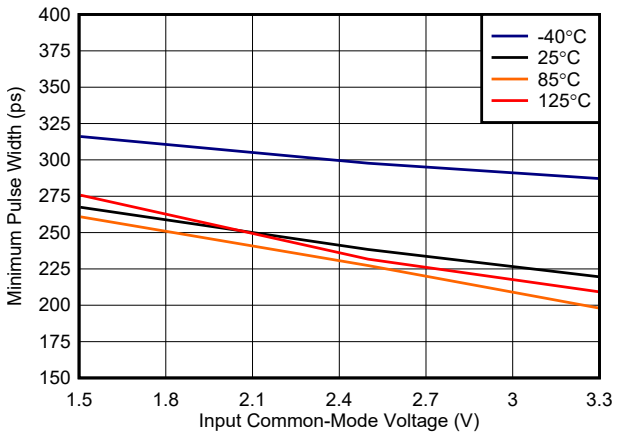


図 6-21. Minimum Pulse Width vs. Common-Mode, 3.3 V

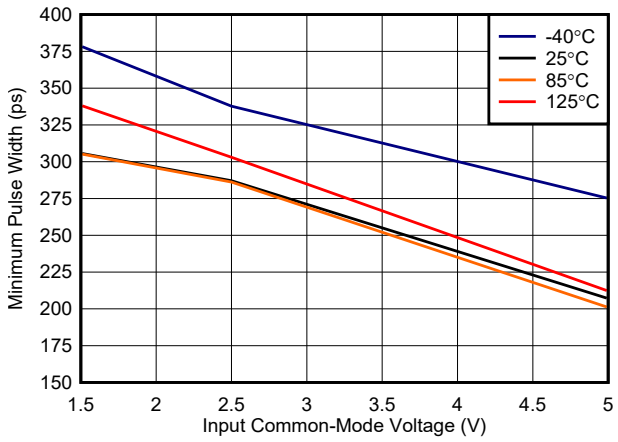


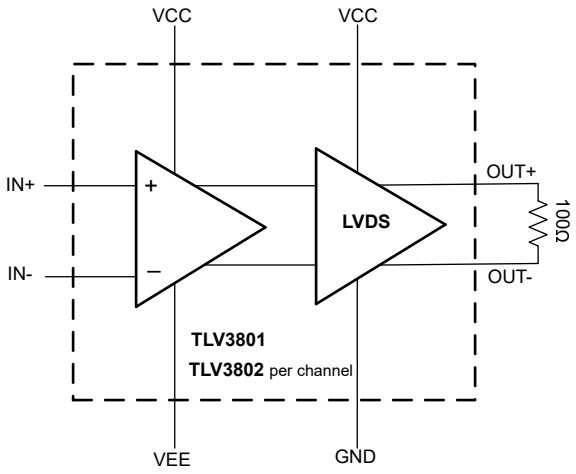
図 6-22. Minimum Pulse Width vs. Common-Mode, 5 V

7 Detailed Description

7.1 Overview

The TLV380x-Q1 is a high-speed comparators with LVDS output. The fast response time of these comparators make them well suited for applications that require narrow pulse width detection or high toggle frequencies. The TLV3801-Q1 is available in the 8-pin WSON package and the TLV3802-Q1 is available in the 12-pin WSON package.

7.2 Functional Block Diagram



7.3 Feature Description

The TLV380x-Q1 are high-speed comparators with a typical propagation delay of 225 ps and LVDS output. The minimum pulse width detection capability is 240 ps and the typical toggle frequency is 3 GHz (6 Gbps). These comparators are well suited for distance sensing for LIDAR and time-of-flight applications as well as for high-speed test and measurement systems. The TLV380x-Q1 has two separate power rails for the input and the output; this allows the input to be referenced from either single or split supply (VCC and VEE) while the output is referenced from ground (VCC and GND).

7.4 Device Functional Modes

The TLV380x-Q1 has a single functional mode and is operational on the condition that both the input supply voltage (VCC - VEE) is greater than or equal to 2.7 V and the output supply voltage (VCC - GND) is greater than or equal to 2.4 V.

7.4.1 Inputs

The TLV380x-Q1 features an input stage, capable of operating between 1.5 V above VEE and 0.1 V above VCC, with an internal ESD protection circuit that includes two pairs of front-to-back diodes between IN+ and IN- as well as two 50 Ω resistors, as shown in 図 7-1. This prevents damage to the input stage by limiting the differential input voltage to be no more than twice the diode's forward-voltage drop 2 × V_F (2 × 0.7 V).

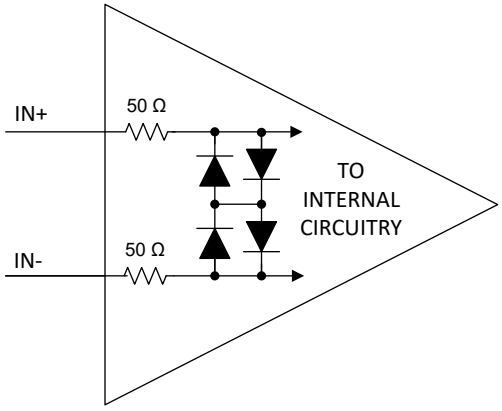


図 7-1. Input Stage Circuitry

When the differential input voltage exceeds 2 × V_F, the input bias current increases at the input pins IN+ and IN-, as shown in 式 1.

$$\text{Input Current} = [(V_{IN+} - V_{IN-}) - 2 \times V_F] / (2 \times 50) \quad (1)$$

To avoid damaging the inputs when exceeding the recommended input voltage range, an external resistor should be used to limit the current. The current should be limited to less than 10 mA.

7.4.2 LVDS Output

The TLV380x-Q1 outputs are LVDS compliant. When the input of the downstream device is terminated with a 100 Ω resistor, the comparators provide a ±350 mV differential swing at an output common-mode voltage of 1.25 V above GND. Fully differential outputs enable fast digital toggling and reduce EMI compared to single-ended output standards.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Capacitive Loads

Under reasonable capacitive loads, the device maintains specified propagation delay. However, excessive capacitive loading under high switching frequencies may increase supply current, propagation delay, or induce decreased slew rate.

8.1.2 Hysteresis

A comparator's high, open-loop gain creates a small band of input differential voltage where the comparator may produce "chatter" which causes the output to toggle back and forth between a “logic high” and a “logic low”. This can cause design challenges for inputs with slow rise and fall times or systems with excessive noise. These challenges can be prevented by adding hysteresis to the comparator. However, hysteresis must be added strategically when input signals are small since it can cuase signals to go undetected. As a result, TLV380x-Q1 has 2 mV of internal hysteresis.

Since the TLV380x-Q1 only have a minimal amount of internal hysteresis, external hysteresis can be applied in the form of a positive feedback loop that adjusts the trip point of the comparator depending on its current output state. See the Non-Inverting Comparator With Hysteresis section for more details.

8.2 Typical Application

8.2.1 Optical Receiver

The TLV380x-Q1 can be used in conjunction with a high performance amplifier such as the OPA858 to create an optical receiver as shown in the 図 8-1. The photodiode operates in photoconductive mode: exposure to light will cause a reverse current through the photodiode. A bias voltage is applied to the op amp's non-inverting input to prevent saturation at the negative power supply. The OPA858 takes the current conducting through the diode and translates it into a voltage for a high speed comparator to detect. The TLV380x-Q1 will then output the proper LVDS signal according to the threshold set (V_{REF}).

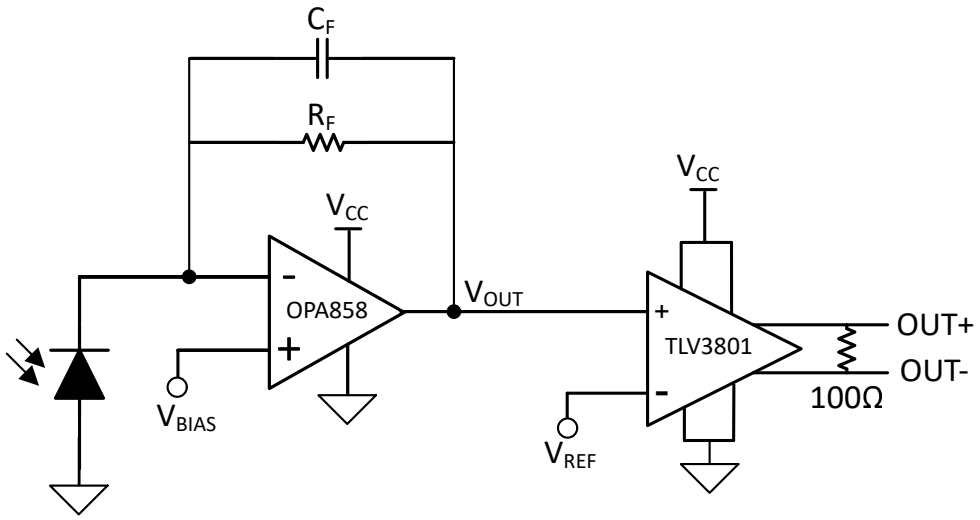


図 8-1. Optical Receiver

8.2.1.1 Design Requirements

表 8-1. Design Parameters

PARAMETER	VALUE
V_{CC}	+5 V
V_{EE}	0 V
$V_{OUT, SWING}$	100 mV
I_{DIODE}	100 µA
f_p	159 MHz

8.2.1.2 Detailed Design Procedure

Set V_{BIAS} to be in the recommended common-mode voltage range of the OPA858. This is also the minimum output voltage of the op amp $V_{OUT, MIN}$ as the op amp will attempt to settle at the voltage applied to the non-inverting input.

The maximum output voltage of the op amp $V_{OUT, MAX}$ can be calculated from the desired output voltage swing $V_{OUT, SWING}$ and $V_{OUT, MIN}$, as shown in 式 2.

$$V_{OUT, MAX} = V_{OUT, SWING} + V_{OUT, MIN} \quad (2)$$

The gain resistor R_F is determined by the desired $V_{OUT, MAX}$ and $V_{OUT, MIN}$ and the maximum current I_{DIODE} through the diode, as shown in 式 2.

$$R_F = (V_{OUT, MAX} - V_{OUT, MIN}) / I_{DIODE} \quad (3)$$

The feedback capacitor, in combinaton with the gain resistor, forms a pole in the frequency response of the amplifier. The feedback capacitor can be determined by the gain resistor and the desired pole frequency f_p, as shown in 式 2.

$$C_F = 1 / (2 \times \pi \times R_F \times f_p) \quad (4)$$

Set V_{REF} to be the switching threshold voltage between $V_{OUT, MAX}$ and $V_{OUT, MIN}$.

Select values for V_{BIAS} and V_{REF}. Plug in given values for $V_{OUT, MAX}$, I_{DIODE}, and f_p. For the given example, V_{BIAS} = 1.5 V, V_{REF} = 1.55 V, and R_F, C_F is solved as 1 kΩ and 1 pF, respectively.

For more information, please refer to the op amp tutorials for stability analysis on the transimpedance amplifier Spice Stability Analysis and Op Amp Stability. See application note SBOA268A Transimpedance Amplifier Circuit for more detailed procedures.

8.2.1.3 Application Performance Plots

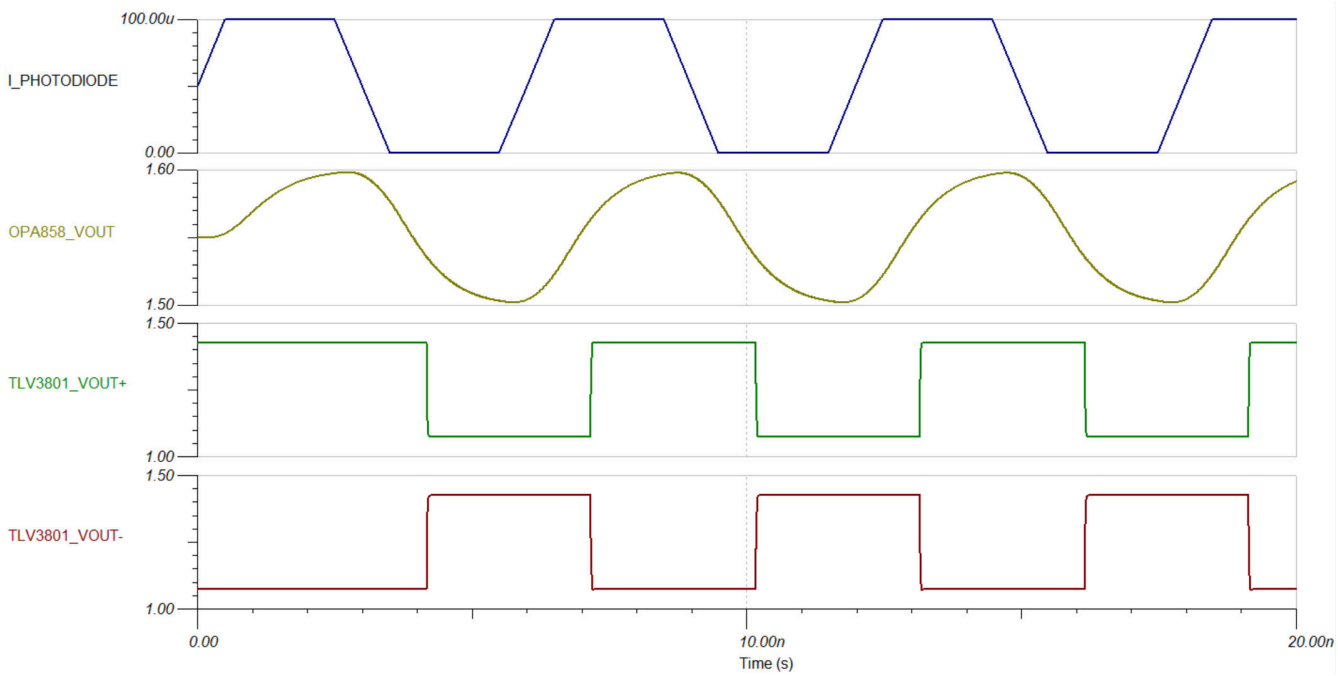


図 8-2. Optical Receiver Output Waveforms

8.2.2 Non-Inverting Comparator With Hysteresis

A way to implement external hysteresis is to add two resistors to the circuit: one in series between the reference voltage and the inverting pin, and another from the inverting pin to one of the differential output pins.

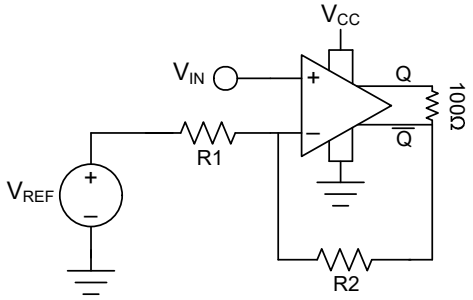


図 8-3. Non-Inverting Comparator with Hysteresis Circuit

8.2.2.1 Design Requirements

表 8-2. Design Parameters

PARAMETER	VALUE
V_{HYS}	50 mV
V_{REF}	2.5 V
V_{T1}	2.34 V
V_{T2}	2.29 V
Q	1.375 V
$\overline{Q}$	1.025 V

8.2.2.2 Detailed Design Procedure

First, create an equation for V_T that covers both output voltages when the output is high or low.

$$V_{T1} = \frac{V_{REF}R_2}{R_1+R_2} + \frac{QR_1}{R_1+R_2} \quad (5)$$

$$V_{T2} = \frac{V_{REF}R_2}{R_1+R_2} + \frac{\overline{Q}R_1}{R_1+R_2} \quad (6)$$

The hysteresis voltage in this network is equal to the difference in the two threshold voltage equations.

$$V_{HYS} = V_{T1}-V_{T2} \quad (7)$$

$$V_{HYS} = \frac{V_{REF}R_2}{R_1+R_2} + \frac{QR_1}{R_1+R_2} - \frac{V_{REF}R_2}{R_1+R_2} - \frac{\overline{Q}R_1}{R_1+R_2} \quad (8)$$

$$V_{HYS} = \frac{(Q-\overline{Q})R_1}{R_1+R_2} \quad (9)$$

$$V_{HYS} = \frac{V_{OD}R_1}{R_1+R_2} \quad (10)$$

Note that these equations do not take into account the effects of the internal hysteresis and offset voltage of the comparator. Design parameters will need to be adjusted accordingly.

Select a value for R2. Plug in given values for V_{REF}, V_{T1}, V_{T2}, Q, and $\overline{Q}$, and solve for R1. For the given example, R2 = 50 kΩ, and R1 is solved as = 8.3 kΩ.

8.2.2.3 Application Performance Plots

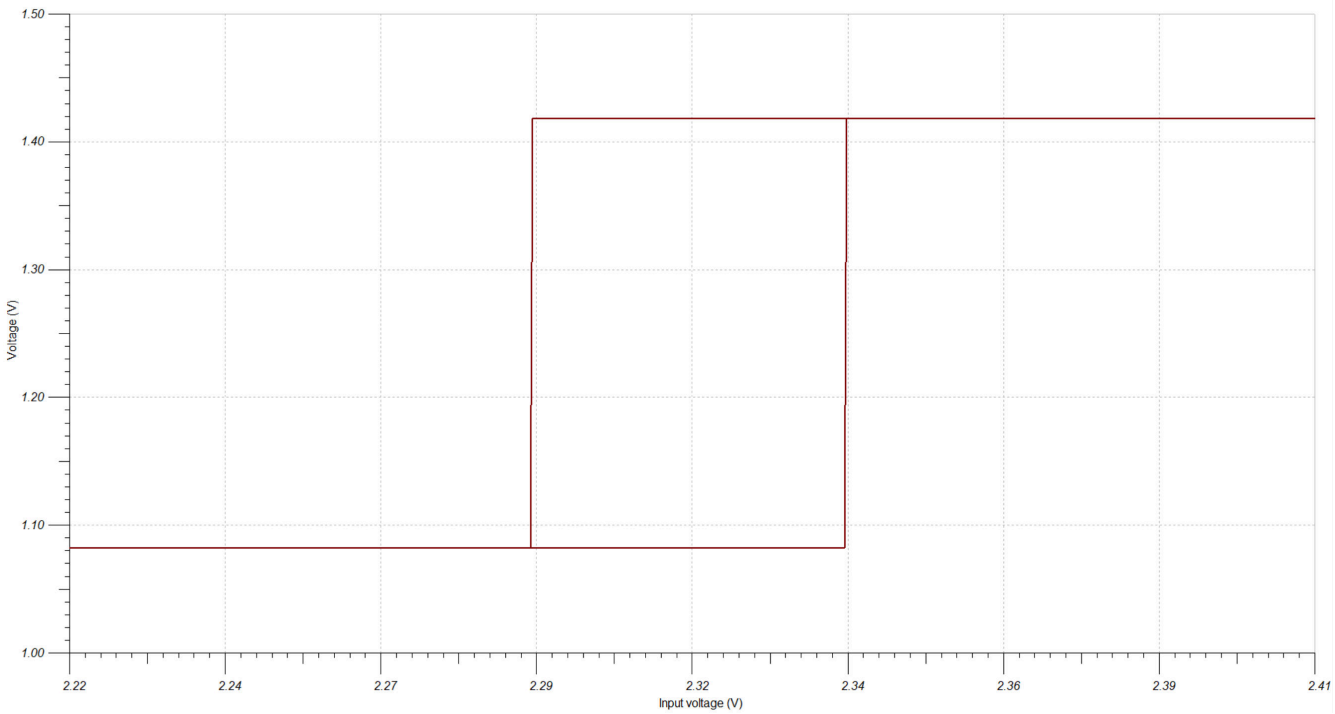


図 8-4. Hysteresis Curve for LVDS Comparator

8.2.3 Logic Clock Source to LVDS Transceiver

The 図 8-5 shows a logic clock source being terminated and driven with the TLV380x-Q1 across a CAT6 Cable to receive an equivalent LVDS clock signal at the receiver end.

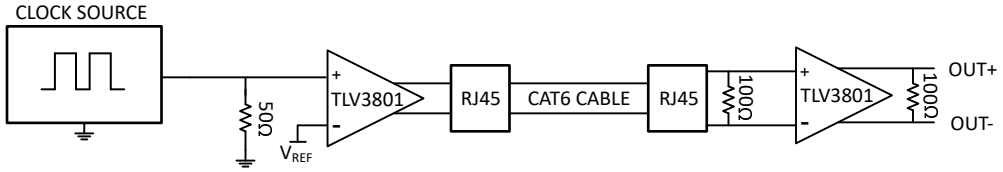


図 8-5. LVDS Clock Transceiver

8.2.4 External Trigger Function for Oscilloscopes

図 8-6 is a typical configuration for creating an external trigger on oscilliscopes. The user adjusts the trigger level, and a DAC converts this trigger level to a voltage the TLV380x-Q1 can use as a reference. The input voltage from an oscilloscope channel is then compared to the trigger reference voltage, and the TLV380x-Q1 sends an LVDS signal to a downstream FPGA to begin a capture. It is common to see bipolar inputs in test and measurement systems such as oscilloscopes; therefore, the TLV380x-Q1 can be configured in split supply so that the inputs are in the allowable input voltage range.

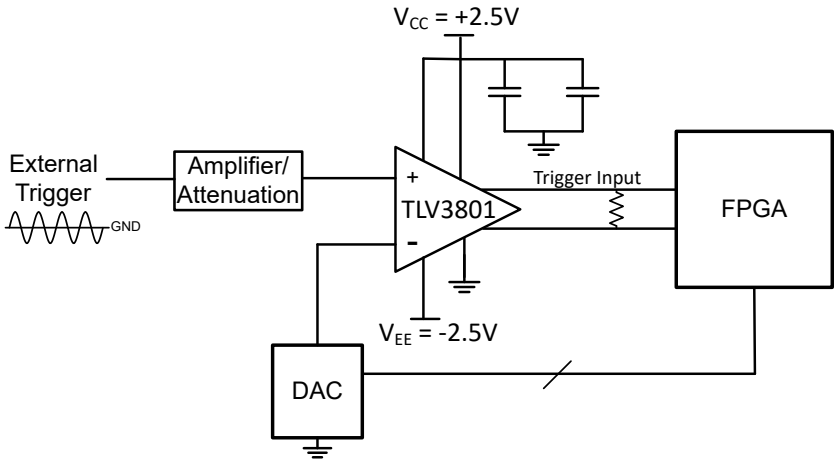


図 8-6. External Trigger Function

8.3 Power Supply Recommendations

The TLV380x-Q1 has two seperate power rails: VCC - VEE for the input stage and VCC - GND for the output stage. This allows for both single and split supply capabilities for the input stage with a seperate ground reference for the LVDS output stage. Split supply operation allows users to apply both positive and negative (bipolar) voltages to the input pins.

When operating from a single supply, the supply voltage range for both the input and output stage is 2.7 V to 5.25 V. When operating from split supply rails, the supply voltage range for the input stage (VCC - VEE) is 2.7 V to 5.25 V, and the supply voltage range for the output stage (VCC - GND) is 2.4 V to 5.25 V. The output logic level is independent of the VCC and VEE levels.

Regardless of single supply or split supply operation, proper decoupling capacitors are required. It is recommended to use a scheme of multiple, low-ESR ceramic capacitors from the supply pins to the ground plane for optimum performance. A good combination would be 100 pF, 10 nF, and 1 uF with the lowest value capacitor closest to the comparator.

8.4 Layout

8.4.1 Layout Guidelines

Comparators are very sensitive to input noise. For best results, adhere to the following layout guidelines.

1. Use a printed-circuit-board (PCB) with a good, unbroken, low-inductance ground plane. Proper grounding (use of a ground plane) helps maintain specified device performance.
2. To minimize supply noise for single and split supply, place decoupling capacitor arrays as close as possible to V_{CC}.
3. On the inputs and the output, keep lead lengths as short as possible to avoid unwanted parasitic feedback around the comparator. Keep inputs away from the output.
4. Solder the device directly to the PCB rather than using a socket.
5. For slow-moving input signals, take care to prevent parasitic feedback. A small capacitor (1000 pF or less) placed between the inputs can help eliminate oscillations in the transition region. This capacitor causes some degradation to propagation delay when impedance is low. The topside ground plane runs between the output and inputs.
6. Use a 100 Ω termination resistor across the device's LVDS output.
7. Use higher performance substrate materials such as Rogers.

8.4.2 Layout Example

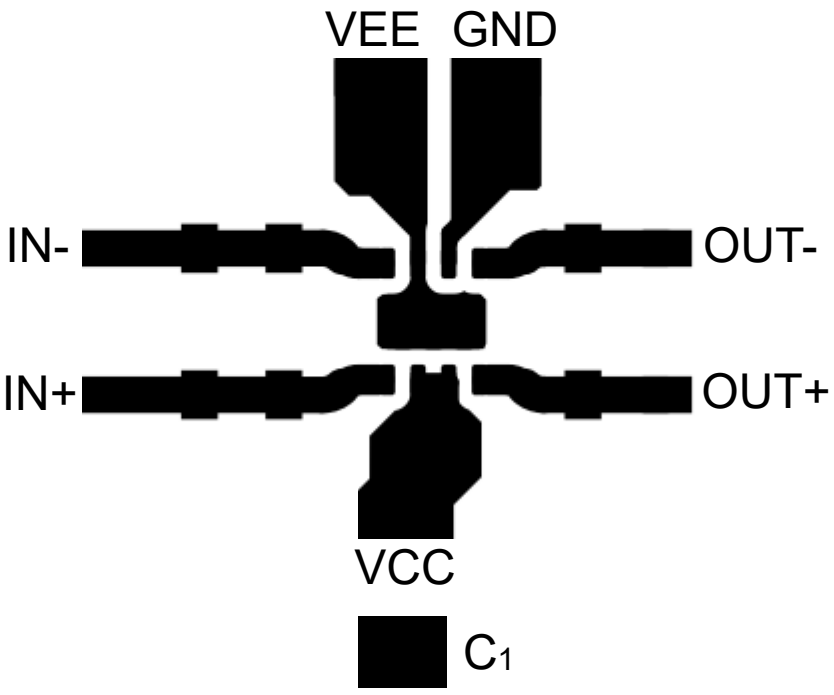


図 8-7. TLV3801EVM Layout Example

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

LIDAR Pulsed Time of Flight Reference Design

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

9.4 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

9.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV3801QDSGRQ1	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	380Q
TLV3801QDSGRQ1.B	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	380Q
TLV3802QDSSRQ1	Active	Production	WSON (DSS) | 12	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	3802Q
TLV3802QDSSRQ1.B	Active	Production	WSON (DSS) | 12	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	3802Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TLV3801-Q1, TLV3802-Q1 :

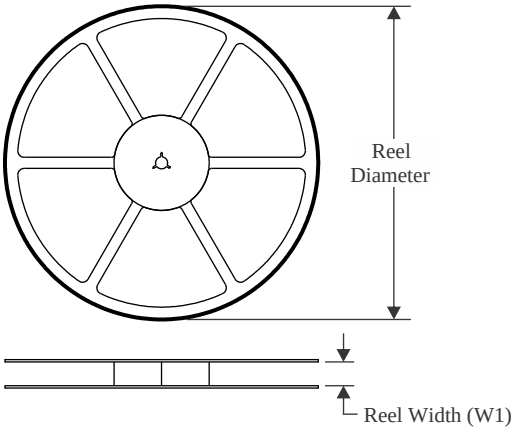
- Catalog : TLV3801, TLV3802

NOTE: Qualified Version Definitions:

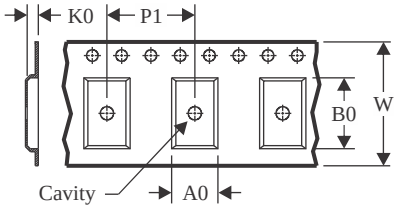
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

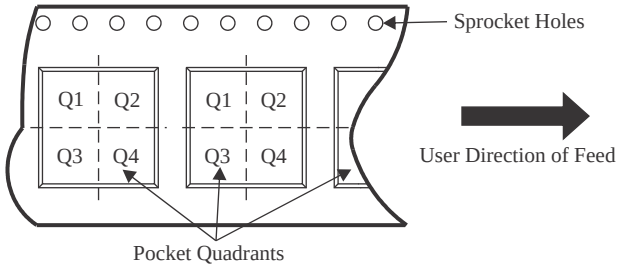


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

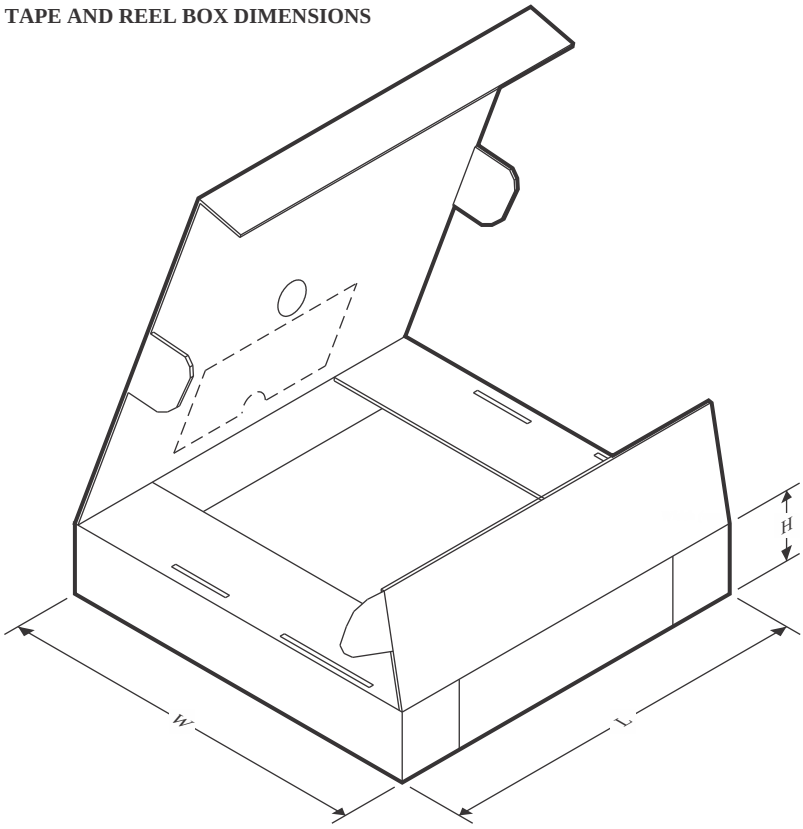
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV3801QDSGRQ1	WSON	DSG	8	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TLV3802QDSSRQ1	WSON	DSS	12	3000	180.0	8.4	2.3	3.2	1.0	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV3801QDSGRQ1	WSON	DSG	8	3000	213.0	191.0	35.0
TLV3802QDSSRQ1	WSON	DSS	12	3000	213.0	191.0	35.0

GENERIC PACKAGE VIEW

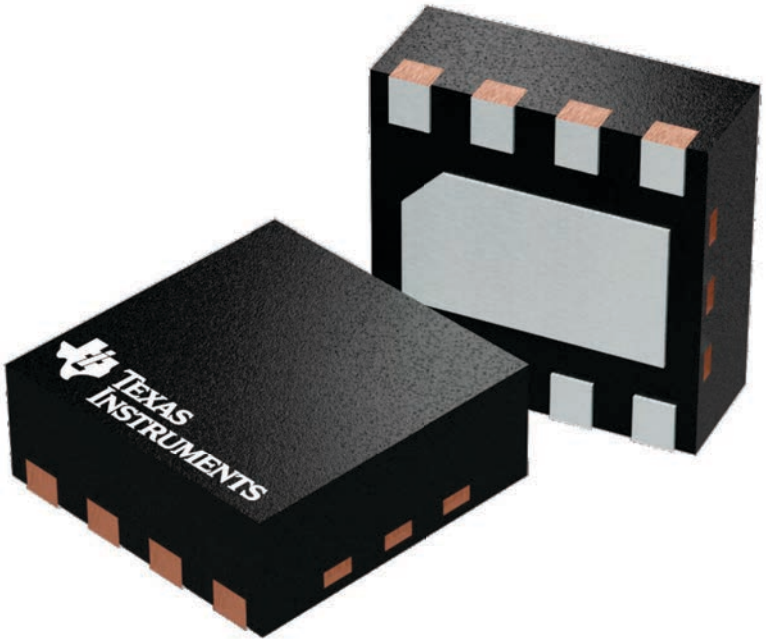
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



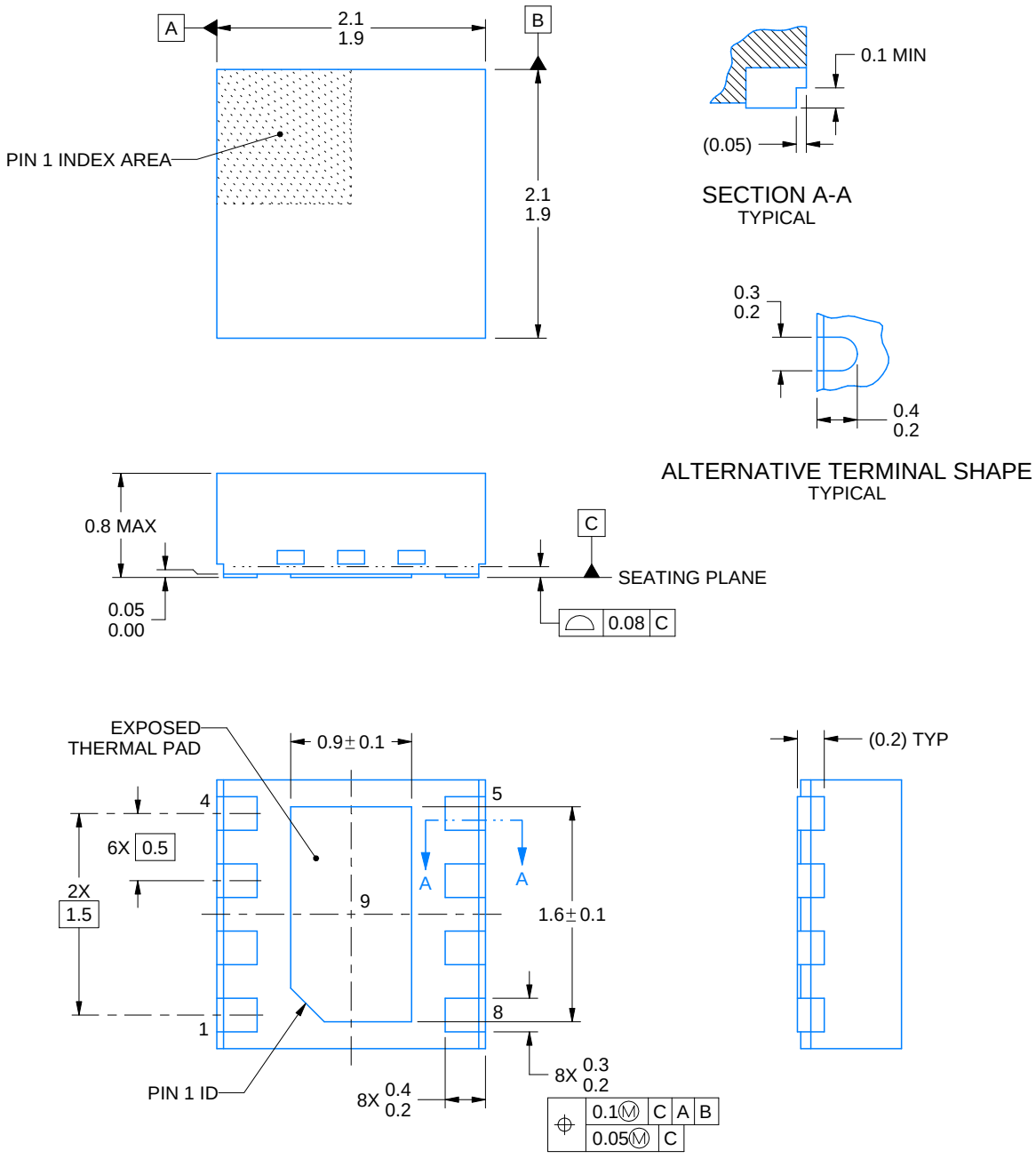
4224783/A

PACKAGE OUTLINE

DSG0008B

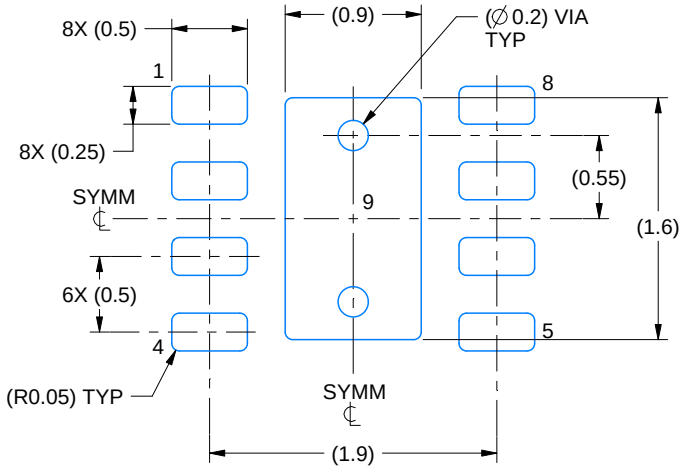
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

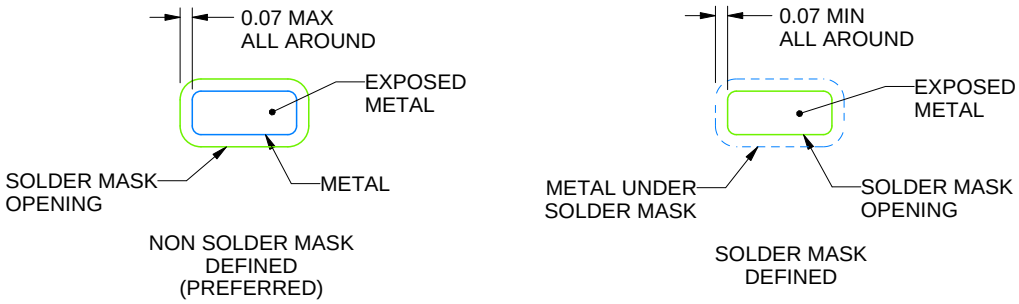


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4222124/E 05/2020

NOTES: (continued)

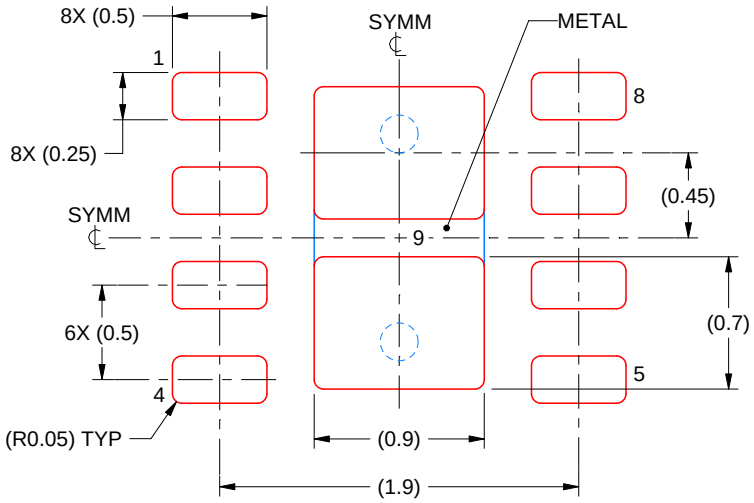
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DSG0008B

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4222124/E 05/2020

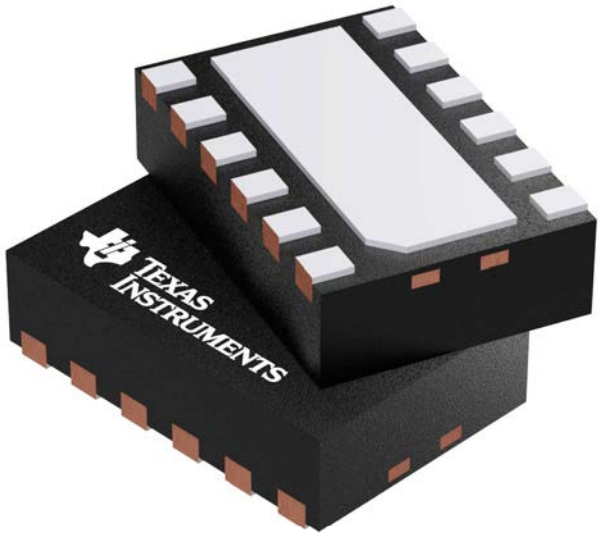
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

DSS 12 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



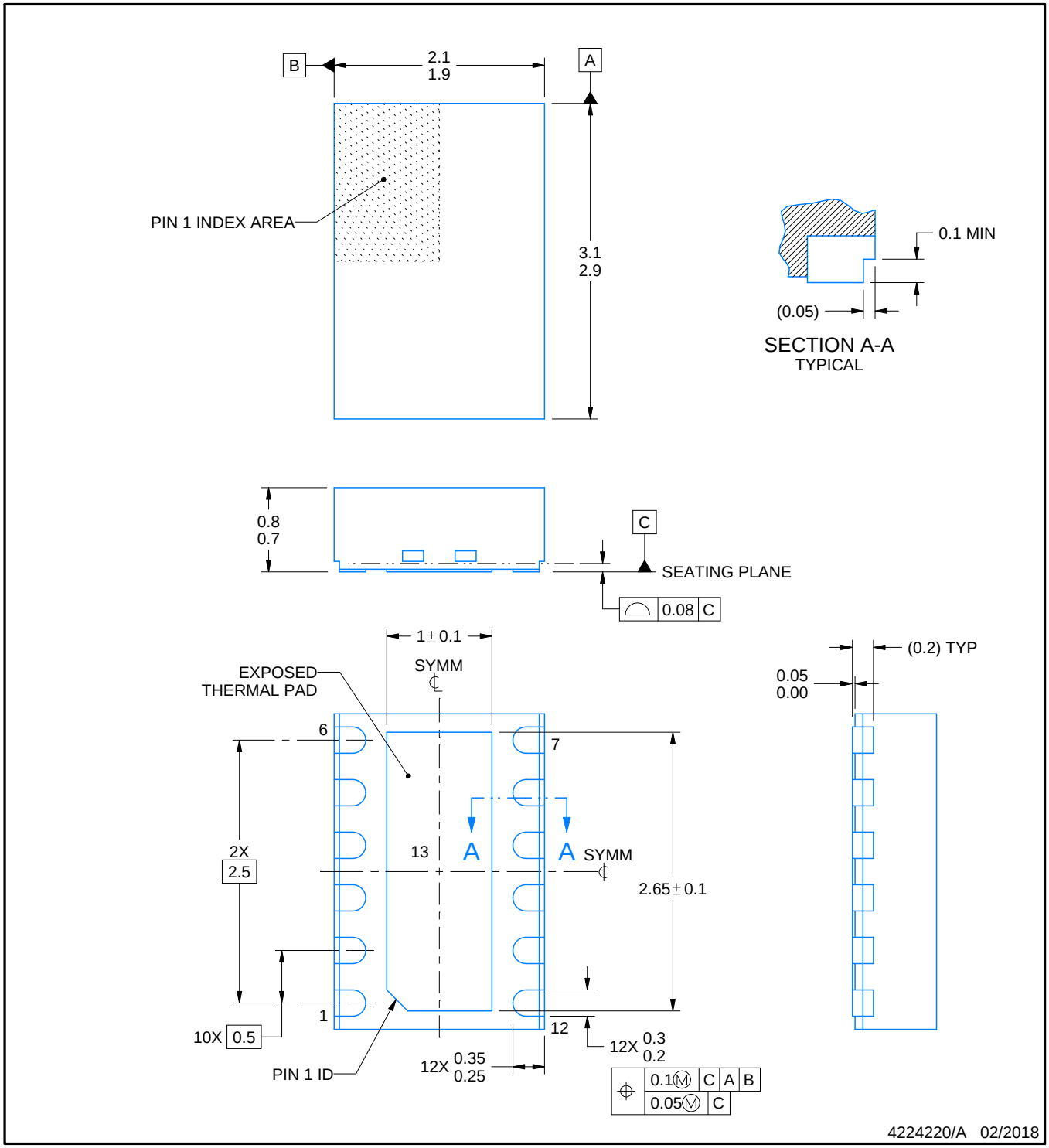
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DSS0012C

PACKAGE OUTLINE

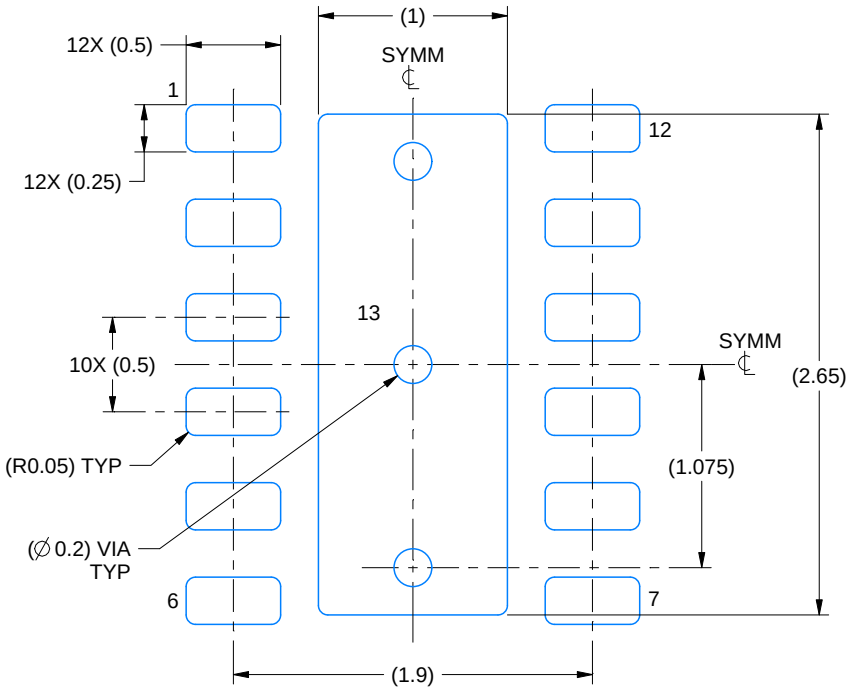
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

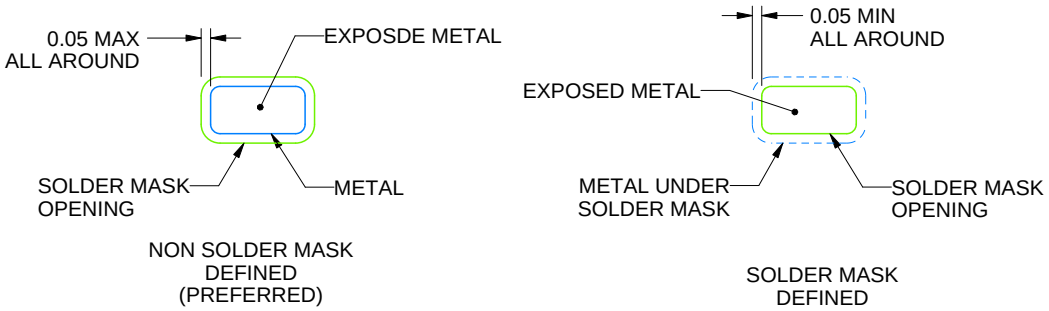


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X

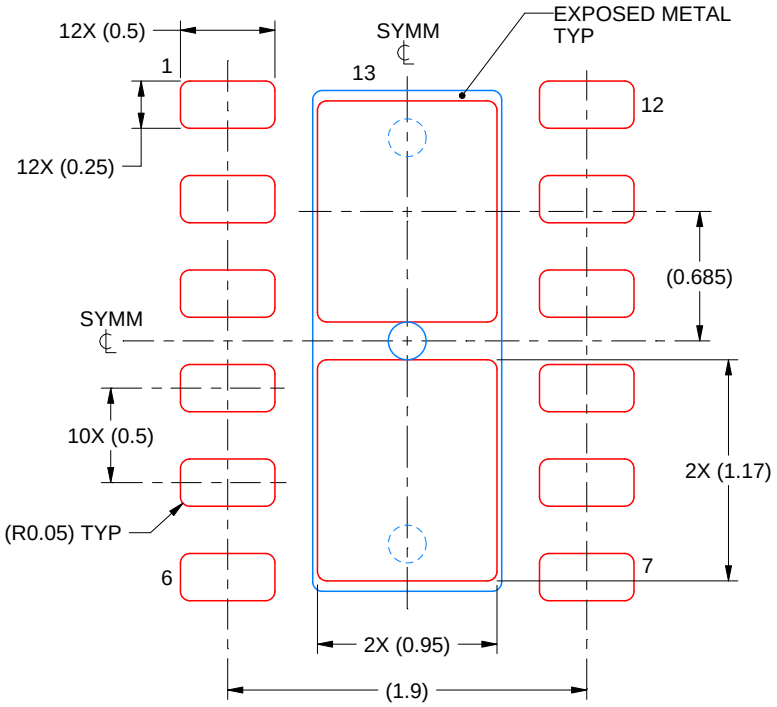


SOLDER MASK DETAILS

4224220/A 02/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 13:
83% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4224220/A 02/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月