# TLVx314-Q1 3MHz、低消費電力、EMI フィルタ内蔵の RRIO オペアンプ

## 1 特長

- 車載アプリケーションに対応
- 下記内容でAEC-Q100認定済み：
  - デバイス温度グレード1: 動作時周囲温度範囲 –40°C～+125°C
  - デバイスHBM ESD分類レベル3A
  - デバイスCDM ESD分類レベルC6
- 低いオフセット電圧: 0.75mV (標準値)
- 低い入力バイアス電流: 1pA (標準値)
- 広い電源電圧範囲: 1.8V～5.5V
- レール・ツー・レール入出力
- ゲイン帯域幅: 3MHz
- 低い$I_Q$: 250µA/ch (最大値)
- 低ノイズ: 1kHz時に16nV/√Hz
- 内部RFおよびEMIフィルタ
- チャネル数
  - TLV314-Q1: 1
  - TLV2314-Q1: 2
  - TLV4314-Q1: 4
- 拡張温度範囲: –40℃～+125℃

## 2 アプリケーション

- ローサイド・センシング
- バッテリ管理システム
- パッシブ型安全運転支援システム
- 静電容量式センシング
- 燃料ポンプ

## 3 概要

TLVx314-Q1ファミリのシングル、デュアル、クワッド・チャネルのオペアンプは、新世代の低消費電力、汎用オペアンプを代表する製品です。レール・ツー・レール入出力(RRIO)、低い静止電流(5Vにおいて標準値150µA)と、3MHzの広い帯域幅により、このファミリはコストと性能との適切なバランスを必要とする各種のバッテリ駆動アプリケーションにおいて非常に魅力的です。TLVx314-Q1ファミリは1pAという低い入力バイアス電流を実現しているため、高インピーダンスのセンサ用の非常に優れた選択肢です。

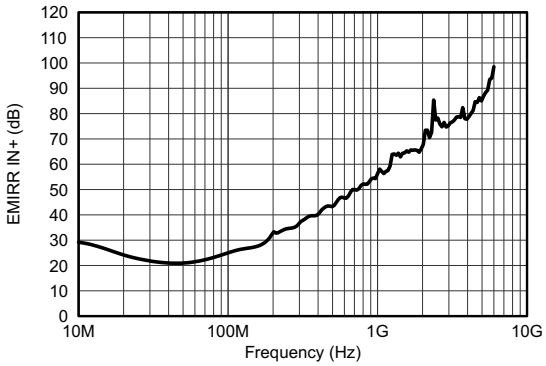
TLVx314-Q1デバイスは堅牢に設計されており、ユニティ・ゲイン安定性、RRIO、300pFまでの容量性負荷、RFおよびEMI除去フィルタの内蔵、オーバードライブ状態で位相反転が発生しない、高い静電放電(ESD)保護(4kV HBM)という特長から、回路設計者が簡単に使用できます。

**製品情報(1)**

| 型番 | パッケージ | 本体サイズ(公称) |
|---|---|---|
| TLV314-Q1 | SOT-23 (5) | 2.90mm×1.60mm |
| | SC70 (5) | 2.00mm×1.25mm |
| TLV2314-Q1 | SOIC (8) | 4.90mm×3.91mm |
| TLV4314-Q1 | TSSOP (14) | 5.00mm×4.40mm |

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

**EMIRRと周波数との関係**




英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.comで閲覧でき、その内容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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## 4 改訂履歴

**2016年11月発行のものから更新** **Page**

- 「*製品情報*」で TLV2314-Q1 のプレビュー表記を 削除 ... 1
- 「*製品情報*」から VSSOP (8) パッケージを 削除 ... 1
- Deleted VSSOP package information and preview notation for 8-Pin SOIC in *Pin Functions* ... 5
- Deleted DGK (VSSOP) thermal information ... 8


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## 5 概要（続き）

最小1.8V (±0.9V)、最大5.5V (±2.75V)の電圧で動作するよう最適化されており、工業用拡張温度範囲の-40℃～+125℃での動作が規定されています。

TLV314-Q1 (シングル)は、5ピンのSC70およびSOT-23パッケージで供給されます。TLV2314-Q1 (デュアル)は、8ピンのSOICおよびVSSOPパッケージで供給されます。クワッド・チャネルのTLV4314-Q1は、14ピンのTSSOPパッケージで供給されます。

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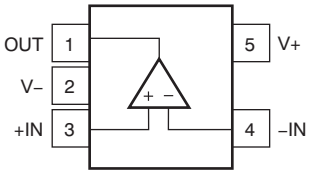
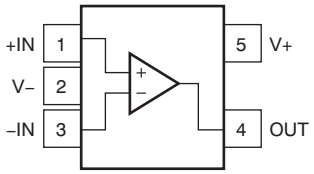
# 6 Pin Configuration and Functions

**TLV314-Q1 DBV Package**
**5-Pin SOT-23**
**Top View**




**TLV314-Q1 DCK Package**
**5-Pin SC70**
**Top View**




**Pin Functions: TLV314-Q1**

| PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | DBV (SOT-23) | DCK (SC70) | | |
| –IN | 4 | 3 | I | Inverting input |
| +IN | 3 | 1 | I | Noninverting input |
| OUT | 1 | 4 | O | Output |
| V– | 2 | 2 | — | Negative (lowest) supply |
| V+ | 5 | 5 | — | Positive (highest) supply |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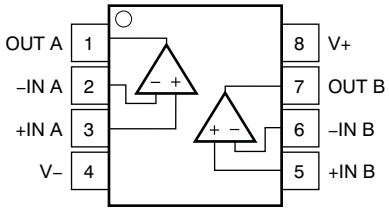
**TLV2314-Q1 D Package**
**8-Pin SOIC**
**Top View**




## Pin Functions: TLV2314-Q1

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| –IN A | 2 | I | Inverting input, channel A |
| +IN A | 3 | I | Noninverting input, channel A |
| –IN B | 6 | I | Inverting input, channel B |
| +IN B | 5 | I | Noninverting input, channel B |
| OUT A | 1 | O | Output, channel A |
| OUT B | 7 | O | Output, channel B |
| V– | 4 | — | Negative (lowest) supply |
| V+ | 8 | — | Positive (highest) supply |

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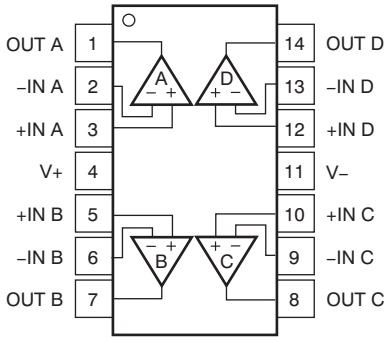
**TLV4314-Q1 PW Package**
**14-Pin TSSOP**
**Top View**




## Pin Functions: TLV4314-Q1

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| –IN A | 2 | I | Inverting input, channel A |
| +IN A | 3 | I | Noninverting input, channel A |
| –IN B | 6 | I | Inverting input, channel B |
| +IN B | 5 | I | Noninverting input, channel B |
| –IN C | 9 | I | Inverting input, channel C |
| +IN C | 10 | I | Noninverting input, channel C |
| –IN D | 13 | I | Inverting input, channel D |
| +IN D | 12 | I | Noninverting input, channel D |
| OUT A | 1 | O | Output, channel A |
| OUT B | 7 | O | Output, channel B |
| OUT C | 8 | O | Output, channel C |
| OUT D | 14 | O | Output, channel D |
| V– | 11 | — | Negative (lowest) supply |
| V+ | 4 | — | Positive (highest) supply |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# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted).[1]

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage $V_S$= (V+) – (V–) | | | 7 | V |
| Signal input pins | Voltage[2] | (V–) – 0.5 | (V+) + 0.5 | V |
| | Current[2] | –10 | 10 | mA |
| Output short-circuit[3] | | Continuous | | mA |
| Temperature | Specified, $T_A$ | –40 | 125 | °C |
| | Junction, $T_J$ | | 150 | |
| | Storage, $T_{stg}$ | –65 | 150 | |

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

## 7.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002[1] | ±4000 | V |
| | | Charged-device model (CDM), per AEC Q100-011 | ±1000 | |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_S$ | Supply voltage | Single-supply | 1.8 | | 5.5 | V |
| | | Dual-supply | ±0.9 | | ±2.75 | |
| | Specified temperature range | | –40 | | 125 | °C |

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## 7.4 Thermal Information: TLV314-Q1

| THERMAL METRIC[1] | | TLV314-Q1 | | UNIT |
|---|---|---|---|---|
| | | DBV (SOT-23) | DCK (SC70) | |
| | | 5 PINS | 5 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 228.5 | 281.4 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case(top) thermal resistance | 99.1 | 91.6 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 54.6 | 59.6 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 7.7 | 1.5 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 53.8 | 58.8 | °C/W |

(1) For more information about traditional and new thermal metrics, see Semiconductor and IC Package Thermal Metrics (SPRA953).

## 7.5 Thermal Information: TLV2314-Q1

| THERMAL METRIC[1] | | TLV2314-Q1 | UNIT |
|---|---|---|---|
| | | D (SOIC) | |
| | | 8 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 138.4 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case(top) thermal resistance | 89.5 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 78.6 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 29.9 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 78.1 | °C/W |

(1) For more information about traditional and new thermal metrics, see Semiconductor and IC Package Thermal Metrics (SPRA953).

## 7.6 Thermal Information: TLV4314-Q1

| THERMAL METRIC[1] | | TLV4314-Q1 | UNIT |
|---|---|---|---|
| | | PW (TSSOP) | |
| | | 14 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 121 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case(top) thermal resistance | 49.4 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 62.8 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 5.9 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 62.2 | °C/W |

(1) For more information about traditional and new thermal metrics, see Semiconductor and IC Package Thermal Metrics (SPRA953).


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## 7.7 Electrical Characteristics

$V_S$ = 1.8 V to 5.5 V; at $T_A$ = 25°C, $R_L$ = 10 kΩ connected to $V_S$ / 2, $V_{CM}$ = $V_S$ / 2, and $V_{OUT}$ = $V_S$ / 2 (unless otherwise noted)(1)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | | | |
| $V_{OS}$ | Input offset voltage | | $V_{CM}$ = ($V_S$+) – 1.3 V, $T_A$ = 25°C | | ±0.75 | ±3 | mV |
| $dV_{OS}/dT$ | $V_{OS}$ vs temperature | | $T_A$ = –40°C to +125°C | | 2 | | µV/°C |
| PSRR | Power-supply rejection ratio | | $V_{CM}$ = ($V_S$+) – 1.3 V, $T_A$ = 25°C | | ±30 | ±135 | µV/V |
| | Channel separation, dc | | At dc, $T_A$ = 25°C | | 100 | | dB |
| **INPUT VOLTAGE RANGE** | | | | | | | |
| $V_{CM}$ | Common-mode voltage range | | $T_A$ = 25°C | (V–) – 0.2 | | (V+) + 0.2 | V |
| CMRR | Common-mode rejection ratio | | $V_S$ = 5.5 V, ($V_S$–) – 0.2 V < $V_{CM}$ < ($V_S$+) – 1.3 V, $T_A$ = 25°C | 72 | 96 | | dB |
| | | | $V_S$ = 5.5 V, $V_{CM}$ = –0.2 V to 5.7 V(2), $T_A$ = 25°C | | 75 | | |
| **INPUT BIAS CURRENT** | | | | | | | |
| $I_B$ | Input bias current | | $T_A$ = 25°C | | ±1.0 | | pA |
| $I_{OS}$ | Input offset current | | $T_A$ = 25°C | | ±1.0 | | pA |
| **NOISE** | | | | | | | |
| | Input voltage noise (peak-to-peak) | | $f$ = 0.1 Hz to 10 Hz, $T_A$ = 25°C | | 5 | | $µV_{PP}$ |
| $e_n$ | Input voltage noise density | | $f$ = 10 kHz, $T_A$ = 25°C | | 15 | | nV/√Hz |
| | | | $f$ = 1 kHz, $T_A$ = 25°C | | 16 | | |
| $i_n$ | Input current noise density | | $f$ = 1 kHz, $T_A$ = 25°C | | 6 | | fA/√Hz |
| **INPUT CAPACITANCE** | | | | | | | |
| $C_{IN}$ | Input capacitance | Differential | $V_S$ = 5 V, $T_A$ = 25°C | | 1 | | pF |
| | | Common-mode | $V_S$ = 5 V, $T_A$ = 25°C | | 5 | | |
| **OPEN-LOOP GAIN** | | | | | | | |
| $A_{OL}$ | Open-loop voltage gain | | $V_S$ = 1.8 V to 5.5 V, 0.2 V < $V_O$ < (V+) – 0.2 V, $R_L$ = 10 kΩ, $T_A$ = 25°C | 85 | 115 | | dB |
| | | | $V_S$ = 1.8 V to 5.5 V, 0.5 V < $V_O$ < (V+) – 0.5 V, $R_L$ = 2 kΩ(2), $T_A$ = 25°C | 85 | 100 | | |
| | Phase margin | | $V_S$ = 5 V, G = 1, $R_L$ = 10 kΩ, $T_A$ = 25°C | | 65 | | ° |
| **FREQUENCY RESPONSE** | | | | | | | |
| GBW | Gain-bandwidth product | | $V_S$ = 1.8 V, $R_L$ = 10 kΩ, $C_L$ = 10 pF, $T_A$ = 25°C | | 2.7 | | MHz |
| | | | $V_S$ = 5 V, $R_L$ = 10 kΩ, $C_L$ = 10 pF, $T_A$ = 25°C | | 3 | | |
| SR | Slew rate(3) | | $V_S$ = 5 V, G = 1, $T_A$ = 25°C | | 1.5 | | V/µs |
| $t_S$ | Settling time | | To 0.1%, $V_S$ = 5 V, 2-V step , G = 1, $T_A$ = 25°C | | 3 | | µs |
| | Overload recovery time | | $V_S$ = 5 V, $V_{IN}$ × gain > $V_S$, $T_A$ = 25°C | | 8 | | µs |
| THD+N | Total harmonic distortion + noise(4) | | $V_S$ = 5 V, $V_O$ = 1 $V_{RMS}$, G = 1, f = 1 kHz, $R_L$ = 10 kΩ, $T_A$ = 25°C | | 0.005% | | |
| **OUTPUT** | | | | | | | |
| $V_O$ | Voltage output swing from supply rails | | $V_S$ = 1.8 V to 5.5 V, $R_L$ = 10 kΩ, $T_A$ = 25°C | | 5 | 25 | mV |
| | | | $V_S$ = 1.8 V to 5.5 V, $R_L$ = 2 kΩ, $T_A$ = 25°C | | 22 | 45 | |
| $I_{SC}$ | Short-circuit current | | $V_S$ = 5 V, $T_A$ = 25°C | | ±20 | | mA |
| $R_O$ | Open-loop output impedance | | $V_S$ = 5.5 V, $f$ = 100 Hz, $T_A$ = 25°C | | 570 | | Ω |
| **POWER SUPPLY** | | | | | | | |
| $V_S$ | Specified voltage range | | | 1.8 | | 5.5 | V |
| $I_Q$ | Quiescent current per amplifier, over temperature | | $V_S$ = 5 V, $I_O$ = 0 mA, $T_A$ = –40°C to +125°C | | 150 | 250 | µA |
| **TEMPERATURE** | | | | | | | |
| | Specified range | | | –40 | | 125 | °C |
| $T_{stg}$ | Storage range | | | –65 | | 150 | °C |

(1) Parameters with minimum or maximum specification limits are 100% production tested at 25ºC, unless otherwise noted. Over-temperature limits are based on characterization and statistical analysis.
(2) Specified by design and characterization; not production tested.
(3) Signifies the slower value of the positive or negative slew rate.
(4) Third-order filter; bandwidth = 80 kHz at –3 dB.

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## 7.8 Typical Characteristics

**表 1. Table of Graphs**

| TITLE | FIGURE |
|---|---|
| Open-Loop Gain and Phase vs Frequency | 図 1 |
| Quiescent Current vs Supply Voltage | 図 2 |
| Offset Voltage Production Distribution | 図 3 |
| Offset Voltage vs Common-Mode Voltage (Maximum Supply) | 図 4 |
| Input Voltage Noise Spectral Density vs Frequency (1.8 V, 5.5 V) | 図 5 |
| Input Bias and Offset Current vs Temperature | 図 6 |
| Output Voltage Swing vs Output Current (Overtemperature) | 図 7 |
| Small-Signal Overshoot vs Load Capacitance | 図 8 |
| Small-Signal Step Response, Noninverting (1.8 V) | 図 9 |
| Large-Signal Step Response, Noninverting (1.8 V) | 図 10 |
| No Phase Reversal | 図 11 |
| Channel Separation vs Frequency (Dual) | 図 12 |
| EMIRR | 図 13 |


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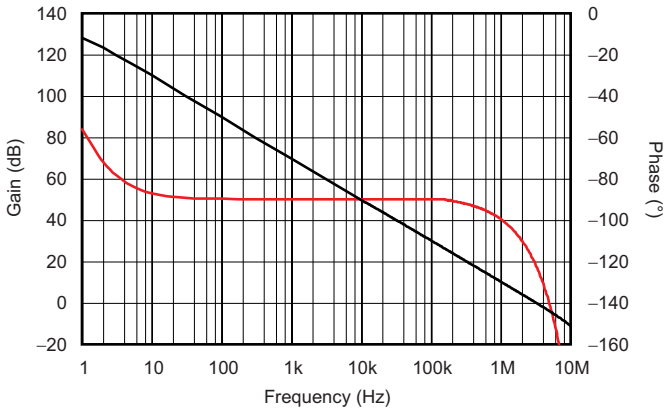
## 7.9 Typical Characteristics

at $T_A$ = 25°C, $R_L$ = 10 kΩ connected to $V_S$ / 2, $V_{CM}$ = $V_S$ / 2, and $V_{OUT}$ = $V_S$ / 2 (unless otherwise noted)




$R_L$ = 10 kΩ and 10 pF, $V_S$ = ±2.5 V

**図 1. Open-Loop Gain and Phase vs Frequency**

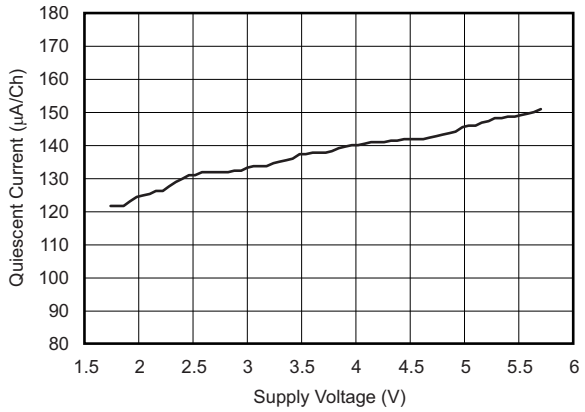



**図 2. Quiescent Current vs Supply**

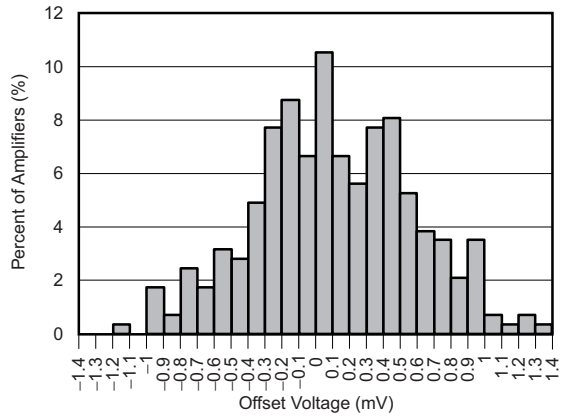
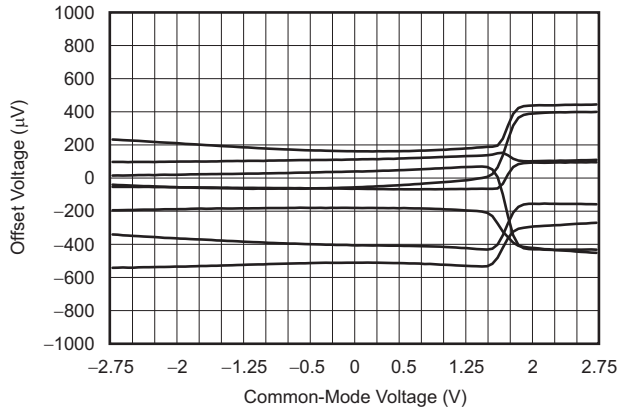



**図 3. Offset Voltage Production Distribution**




Typical units, $V_S$ = ±2.75 V

**図 4. Offset Voltage vs Common-Mode Voltage**

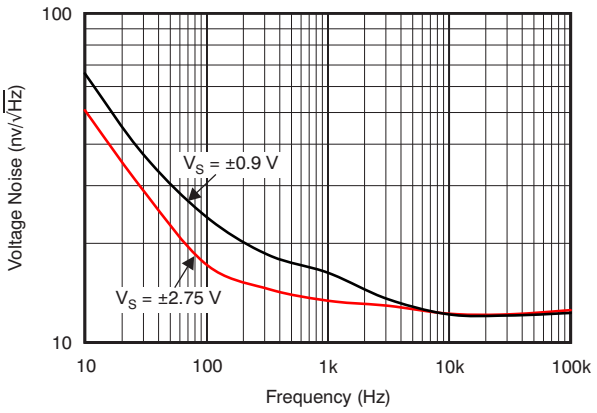



**図 5. Input Voltage Noise Spectral Density vs Frequency**

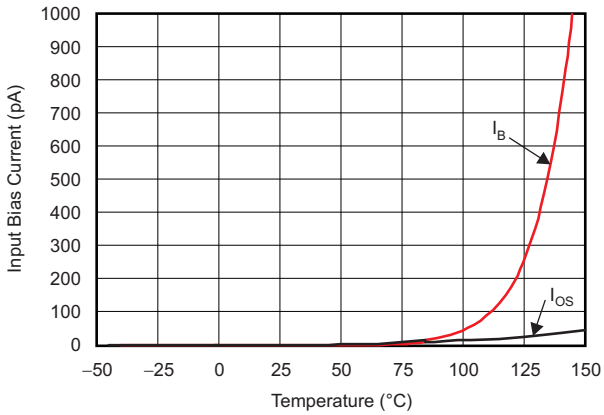
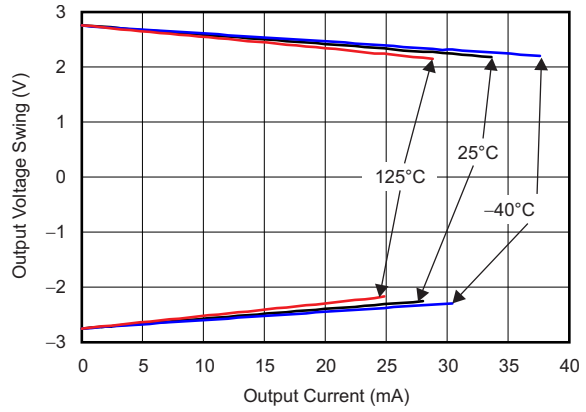



**図 6. Input Bias and Offset Current vs Temperature**

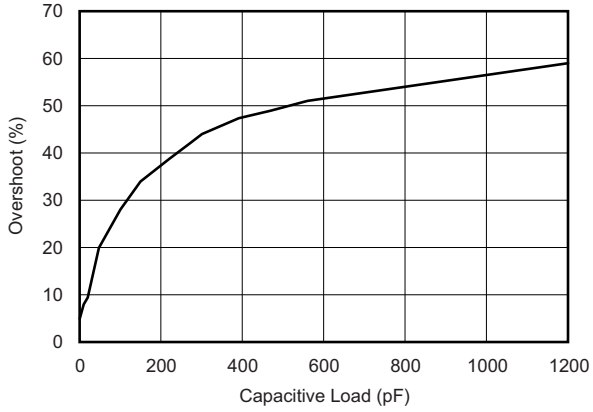
## Typical Characteristics (continued)

at $T_A$ = 25°C, $R_L$ = 10 kΩ connected to $V_S$ / 2, $V_{CM}$ = $V_S$ / 2, and $V_{OUT}$ = $V_S$ / 2 (unless otherwise noted)



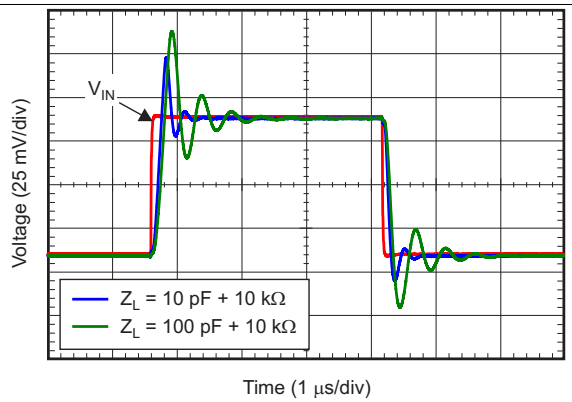

$V_S$ = ±2.75 V

**図 7. Output Voltage Swing vs Output Current (Overtemperature)**



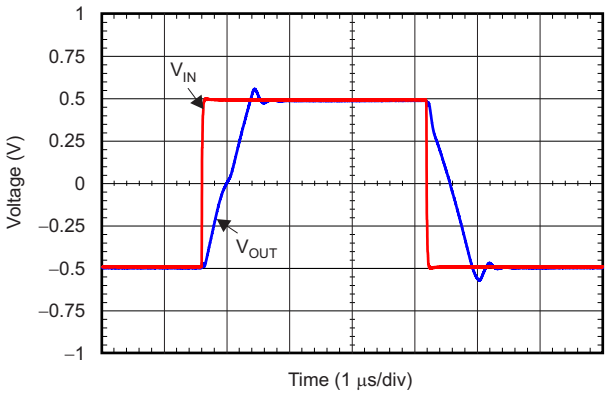

$V_S$ = ±2.75 V Gain = 1 V/V $R_L$ = 10 kΩ

**図 8. Small-Signal Overshoot vs Load Capacitance**




$V_S$ = ±0.9 V Gain = 1 V/V $R_F$ = 10 kΩ

**図 9. Small-Signal Pulse Response (Noninverting)**




$V_S$ = ±0.9 V Gain = 1 V/V $R_L$ = 10 kΩ

**図 10. Large-Signal Pulse Response (Noninverting)**

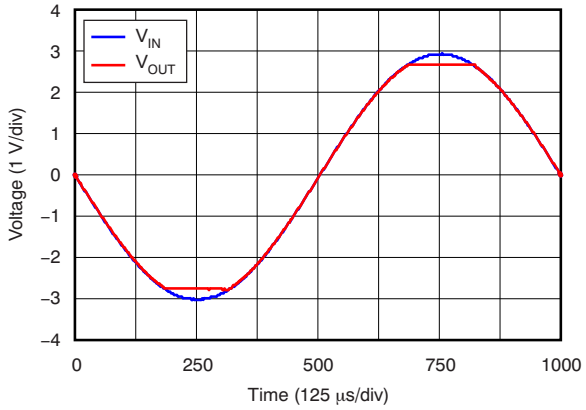
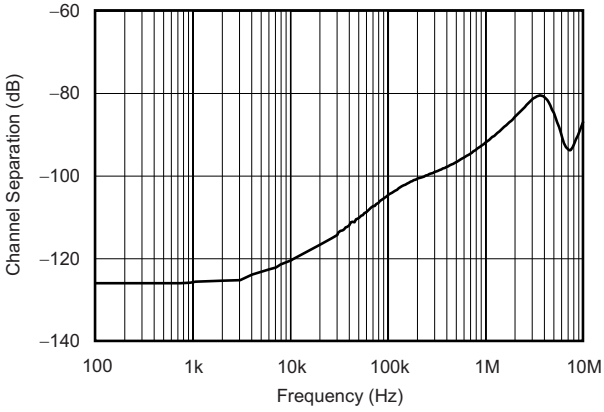



**図 11. No Phase Reversal**




$V_S$ = ±2.75 V

**図 12. Channel Separation vs Frequency (TLV2314)**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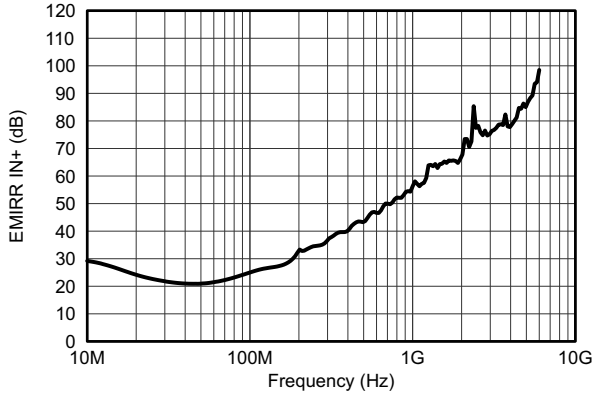
## Typical Characteristics (continued)

at $T_A$ = 25°C, $R_L$ = 10 kΩ connected to $V_S$ / 2, $V_{CM}$ = $V_S$ / 2, and $V_{OUT}$ = $V_S$ / 2 (unless otherwise noted)




$P_{RF}$ = –10 dBm $V_S$ = ±2.5 V $V_{CM}$ = 0 V

**図 13. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR IN+) vs Frequency**

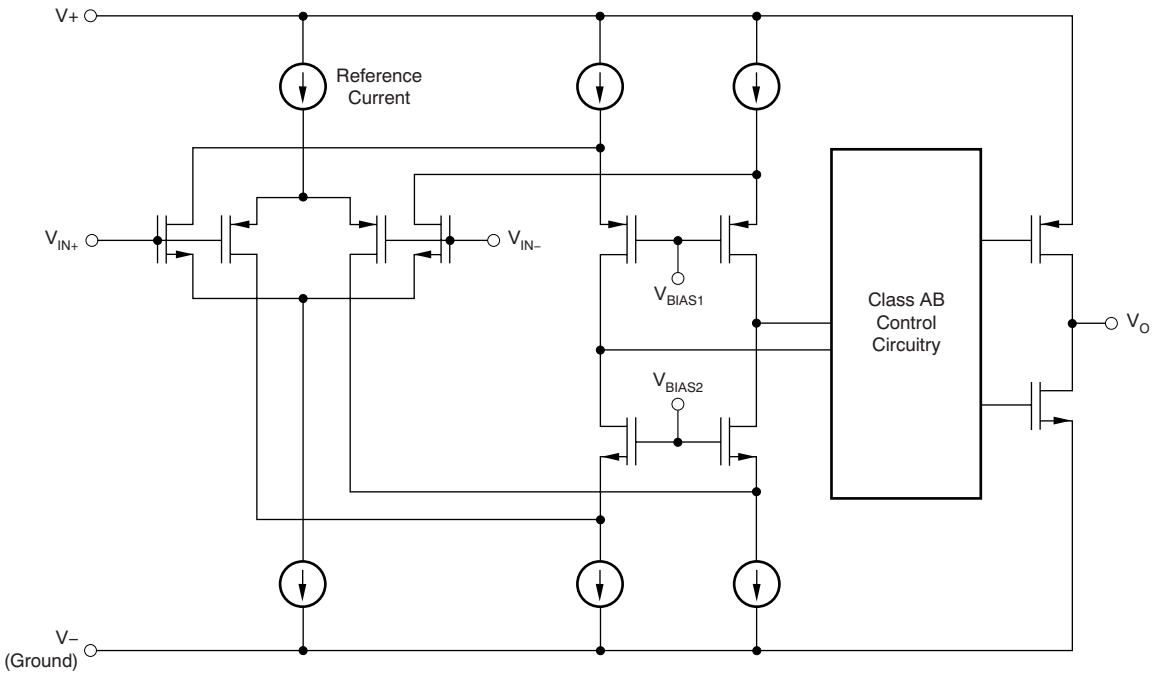
# 8 Detailed Description

## 8.1 Overview

The TLVx314-Q1 is a family of low-power, rail-to-rail input and output operational amplifiers specifically designed for portable applications. These devices operate from 1.8 V to 5.5 V, are unity-gain stable, and suitable for a wide range of general-purpose applications. The class AB output stage is capable of driving ≤ 10-kΩ loads connected to any point between V+ and ground. The input common-mode voltage range includes both rails, and allows the TLVx314-Q1 to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and makes these devices suitable for driving sampling analog-to-digital converters (ADCs).

The TLVx314-Q1 family features 3-MHz bandwidth and 1.5-V/µs slew rate with only 150-µA supply current per channel, providing good ac performance at very-low-power consumption. DC applications are also well served with a very low input noise voltage of 14 nV / √Hz at 1 kHz, low input bias current (0.2-pA), and a typical input offset voltage of 0.5 mV.

## 8.2 Functional Block Diagram





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## 8.3 Feature Description

### 8.3.1 Operating Voltage

The TLVx314-Q1 series of operational amplifiers is fully specified and ensured for operation from 1.8 V to 5.5 V. In addition, many specifications apply from –40°C to +125°C. Parameters that vary significantly with operating voltages or temperature are provided in the *Typical Characteristics* section. Bypass power-supply pins with 0.01-μF ceramic capacitors.

### 8.3.2 Rail-to-Rail Input

The input common-mode voltage range of the TLVx314-Q1 extends 200 mV beyond the supply rails. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair, as shown in the *Functional Block Diagram*. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1.3 V to 200 mV above the positive supply, and the P-channel pair is on for inputs from 200 mV below the negative supply to approximately (V+) – 1.3 V. There is a small transition region, typically (V+) – 1.4 V to (V+) – 1.2 V, in which both pairs are on. This 200-mV transition region may vary up to 300 mV with process variation. Thus, the transition region (with both stages on) ranges from (V+) – 1.7 V to (V+) – 1.5 V on the low end, up to (V+) – 1.1 V to (V+) – 0.9 V on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can degrade compared to device operation outside this region.

### 8.3.3 Rail-to-Rail Output

Designed as a micro-power, low-noise operational amplifier, the TLVx314-Q1 delivers a robust output drive capability. A class AB output stage with common-source transistors achieves full rail-to-rail output swing capability. For resistive loads up to 10-kΩ, the output typically swings to within 5 mV of either supply rail regardless of the applied power-supply voltage . Different load conditions change the ability of the amplifier to swing close to the rails, as shown in 図 7.

### 8.3.4 Common-Mode Rejection Ratio (CMRR)

The CMRR for the TLVx314-Q1 is specified in several ways so the best match for a given application can be used; see the *Electrical Characteristics* table. First, the CMRR of the device in the common-mode range below the transition region [$V_{CM}$ < (V+) – 1.3 V] is given. This specification is the best indicator of the capability of the device when the application requires using one of the differential input pairs. Second, the CMRR over the entire common-mode range is specified at ($V_{CM}$ = –0.2 V to 5.7 V). This last value includes the variations measured through the transition region, as shown in 図 4.

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## Feature Description (continued)

### 8.3.5 Capacitive Load and Stability

The TLVx314-Q1 is designed for applications where driving a capacitive load is required. As with all operational amplifiers, there may be specific instances where the TLVx314-Q1 can become unstable. The particular operational amplifier circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether or not an amplifier is stable in operation. An operational amplifier in the unity-gain (1 V/V) buffer configuration that drives a capacitive load exhibits a greater tendency to be unstable than an amplifier operated at a higher noise gain. The capacitive load, in conjunction with the operational amplifier output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases when capacitive loading increases. When operating in the unity-gain configuration, the TLVx314-Q1 remains stable with a pure capacitive load up to approximately 1 nF. The equivalent series resistance (ESR) of some very large capacitors ($C_L$ capacitors with a value greater than 1 μF) is sufficient to alter the phase characteristics in the feedback loop so the amplifier remains stable. Increasing the amplifier closed-loop gain allows the amplifier to drive increasingly larger capacitance. This increased capability is evident when measuring the overshoot response of the amplifier at higher voltage gains, as shown in 図 8.

Inserting a small resistor (typically 10-Ω to 20-Ω) can increase the capacitive load drive of the amplifier in a unity-gain configuration, as shown in 図 14. This resistor significantly reduces the overshoot and ringing associated with large capacitive loads. One possible problem with this technique, however, is that a voltage divider is created with the added series resistor and any resistor connected in parallel with the capacitive load. The voltage divider introduces a gain error at the output that reduces the output swing.

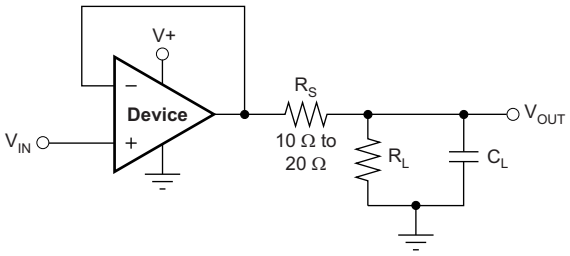


**図 14. Improving Capacitive Load Drive**

### 8.3.6 EMI Susceptibility and Input Filtering

Operational amplifiers vary with regard to the susceptibility of the device to electromagnetic interference (EMI). If conducted EMI enters the operational amplifier, the dc offset at the amplifier output can shift from the nominal value when EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. Although EMI can affect all operational amplifier pin functions, the signal input pins are likely to be the most susceptible. The TLVx314-Q1 operational amplifier family incorporates an internal input low-pass filter that reduces the amplifiers response to EMI. The filter provides common-mode and differential mode filtering. The filter is designed for a cutoff frequency of approximately 80 MHz (–3 dB), with a roll-off of 20 dB per decade.

Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. The EMI rejection ratio (EMIRR) metric allows operational amplifiers to be directly compared to the EMI immunity. 図 13 illustrates the testing results on the TLVx314-Q1. For more detailed information, see *EMI Rejection Ratio of Operational Amplifiers* (SBOA128), available for download from www.ti.com.

## 8.4 Device Functional Modes

The TLVx314-Q1 family has a single functional mode. These devices are powered on as long as the power-supply voltage is between 1.8 V (±0.9 V) and 5.5 V (±2.75 V).


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# 9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The TLVx314-Q1 device is a low-power, rail-to-rail input and output operational amplifier specifically designed for portable applications. These devices operate from 1.8 V to 5.5 V, are unity-gain stable, and suitable for a wide range of general-purpose applications. The class AB output stage is capable of driving ≤ 10-kΩ loads connected to any point between V+ and ground. The input common-mode voltage range includes both rails, and allows the TLVx314-Q1 family to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and makes the device suitable for driving sampling analog-to-digital converters (ADCs).

The TLVx314-Q1 features a 3-MHz bandwidth and 1.5-V/µs slew rate with only 150-µA supply current per channel, providing good ac performance at very-low-power consumption. DC applications are also well served with a very-low input noise voltage of 14 nV/√Hz at 1 kHz, low-input bias current (0.2 pA), and a typical input offset voltage of 0.5 mV.

## 9.2 Typical Application

A typical application for an operational amplifier is an inverting amplifier, as shown in 図 15. An inverting amplifier takes a positive voltage on the input and outputs a signal inverted to the input, making a negative voltage of the same magnitude. In the same manner, the amplifier also makes negative input voltages positive on the output. In addition, amplification can be added by selecting the input resistor ($R_I$) and the feedback resistor ($R_F$).

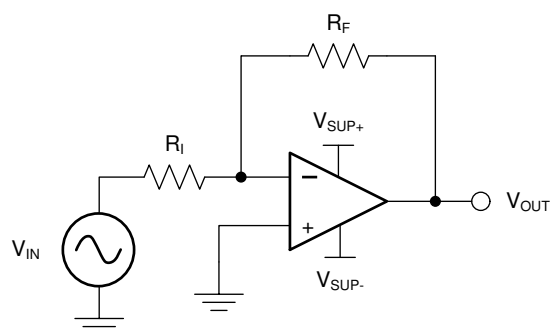



**図 15. Application Schematic**

### 9.2.1 Design Requirements

The supply voltage must be chosen to be larger than the input voltage range and the desired output range. The limits of the input common-mode range ($V_{CM}$) and the output voltage swing to the rails ($V_O$) must also be considered. For instance, this application scales a signal of ±0.5 V (1 V) to ±1.8 V (3.6 V). Setting the supply at ±2.5 V is sufficient to accommodate this application.

### 9.2.2 Detailed Design Procedure

Calculate the gain required by the inverting amplifier using 式 1 and 式 2:

$$A_V = \frac{V_{OUT}}{V_{IN}} \tag{1}$$

$$A_V = \frac{1.8}{-0.5} = -3.6 \tag{2}$$

## Typical Application (continued)

When the desired gain is determined, select a value for $R_I$ or $R_F$. Selecting a value in the kilohm range is desirable for general-purpose applications because the amplifier circuit uses currents in the milliamp range. This milliamp current range ensures the device does not draw too much current. The trade-off is that very large resistors (hundreds of kilohms) draw the smallest current, but generate the highest noise. Very small resistors (hundreds of ohms) generate low noise but draw high current. This example uses 10 kΩ for $R_I$, and $R_F$ uses 36 kΩ. These values are calculated using 式 3:

$$A_V = -\frac{R_F}{R_I} \tag{3}$$

### 9.2.3 Application Curve

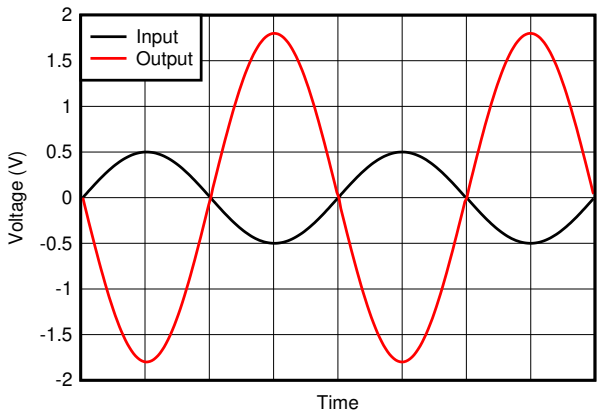
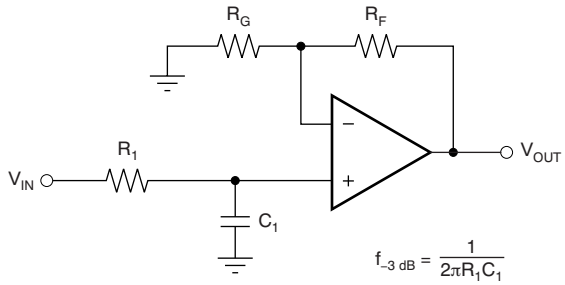



**図 16. Inverting Amplifier Input and Output**

## 9.3 System Examples

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to establish this limited bandwidth is to place an RC filter at the noninverting terminal of the amplifier, as 図 17 shows.




$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR_1C_1}\right)$$

**図 17. Single-Pole, Low-Pass Filter**

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task, as 図 18 shows. For best results, the amplifier must have a bandwidth that is eight to ten times the filter frequency bandwidth. Failure to follow this guideline can result in phase shift of the amplifier.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## System Examples (continued)

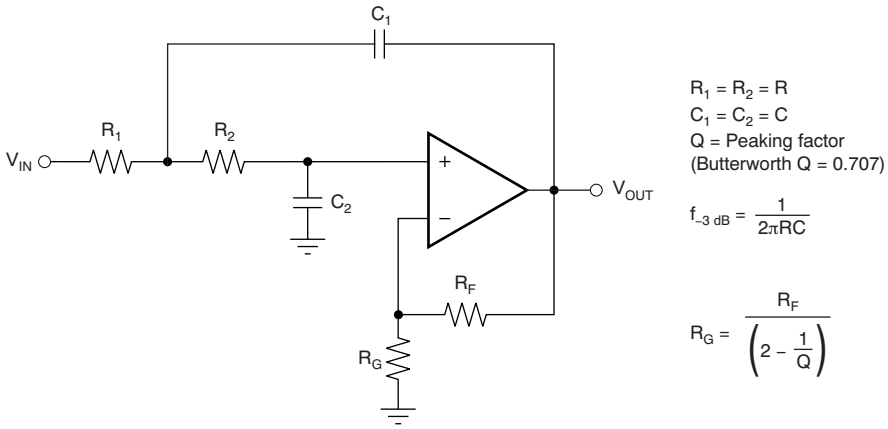


**図 18. Two-Pole, Low-Pass, Sallen-Key Filter**

# 10 Power Supply Recommendations

The TLVx314-Q1 family is specified for operation from 1.8 V to 5.5 V (±0.9 V to ±2.75 V); many specifications apply from –40°C to +125°C. *Typical Characteristics* presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

> **注意**
>
> Supply voltages larger than 7 V can permanently damage the device (see the *Absolute Maximum Ratings* table).

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement; see *Layout Guidelines*.

## 10.1 Input and ESD Protection

The TLVx314-Q1 family incorporates internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA, as stated in the *Absolute Maximum Ratings* table. 図 19 shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input, which must be kept to a minimum in noise-sensitive applications.

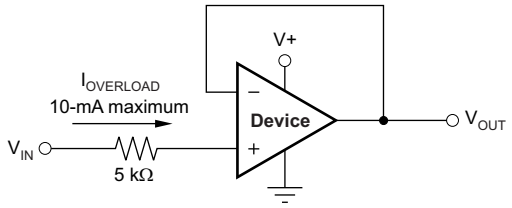


**図 19. Input Current Protection**


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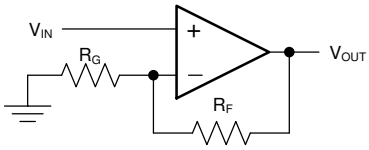
# 11 Layout

## 11.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier. Use bypass capacitors to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of the circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are typically devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see *Circuit Board Layout Techniques* (SLOA089).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicularly is much better than crossing in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keep $R_F$ and $R_G$ close to the inverting input in order to minimize parasitic capacitance, as shown in 図 20.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

## 11.2 Layout Example




(Schematic Representation)

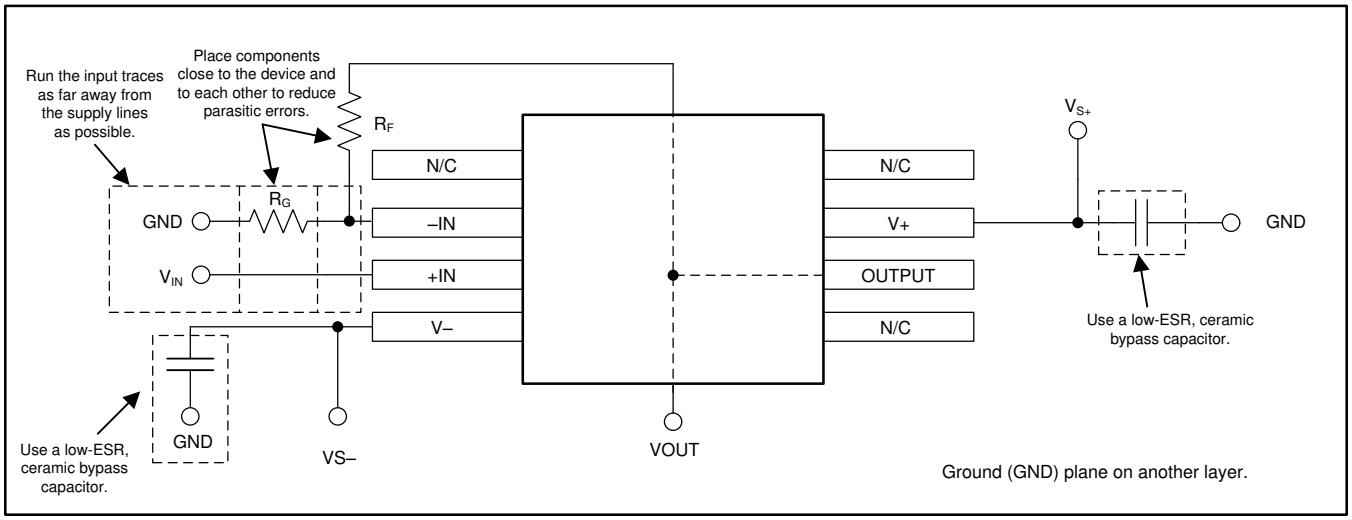



**図 20. Operational Amplifier Board Layout for Noninverting Configuration**

# 12 デバイスおよびドキュメントのサポート

## 12.1 デバイス・サポート

### 12.1.1 開発サポート

## 12.2 ドキュメントのサポート

### 12.2.1 関連資料

関連資料については、以下を参照してください。

- *『オペアンプのEMI除去率』*(SBOA128)
- *『基板のレイアウト技法』*(SLOA089)
- *『QFN/SONのPCB実装』*(SLUA271)
- *『クワッド・フラットパック・リードレス・ロジック・パッケージ』*(SCBA017)

## 12.3 関連リンク

表 2 に、クイック・アクセス・リンクの一覧を示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

**表 2. 関連リンク**

| 製品 | プロダクト・フォルダ | サンプルとご購入 | 技術資料 | ツールとソフトウェア | サポートとコミュニティ |
|---|---|---|---|---|---|
| TLV314 - Q1 | ここをクリック | ここをクリック | ここをクリック | ここをクリック | ここをクリック |
| TLV2314 - Q1 | ここをクリック | ここをクリック | ここをクリック | ここをクリック | ここをクリック |
| TLV4314 - Q1 | ここをクリック | ここをクリック | ここをクリック | ここをクリック | ここをクリック |

## 12.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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**設計サポート** ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

## 12.5 商標

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## 12.6 静電気放電に関する注意事項

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## 12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.


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## 13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TLV2314QDRQ1 | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | V2314Q |
| TLV2314QDRQ1.B | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | V2314Q |
| TLV314QDBVRQ1 | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-2-260C-1 YEAR | -40 to 125 | 16SD |
| TLV314QDBVRQ1.B | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 16SD |
| TLV314QDBVTQ1 | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU \| SN | Level-2-260C-1 YEAR | -40 to 125 | 16SD |
| TLV314QDBVTQ1.B | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 16SD |
| TLV4314QPWRQ1 | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | V4314Q1 |
| TLV4314QPWRQ1.B | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | V4314Q1 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TLV2314-Q1, TLV314-Q1, TLV4314-Q1 :**

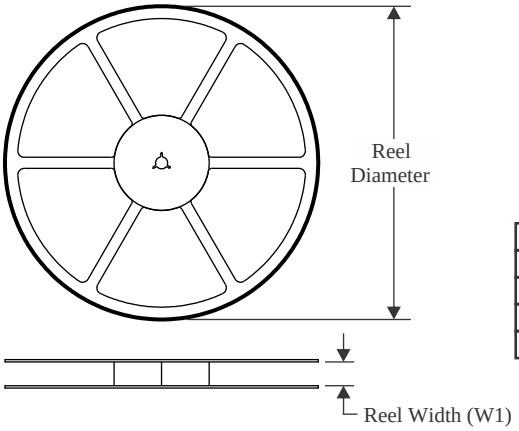
- Catalog : TLV2314, TLV314, TLV4314

NOTE: Qualified Version Definitions:

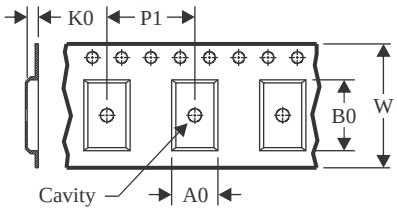
- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

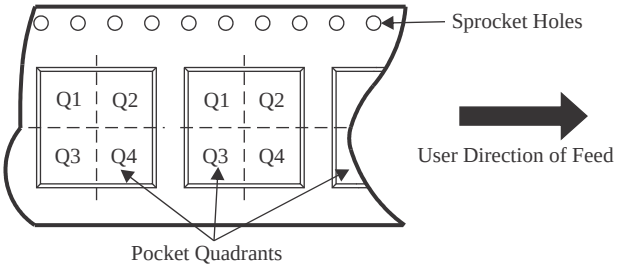



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

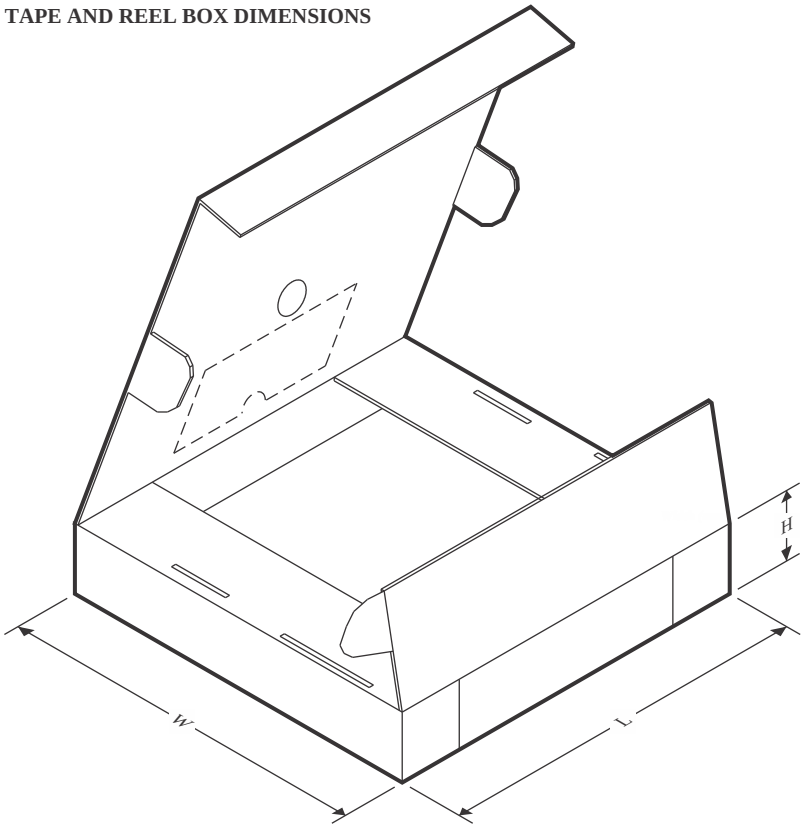
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

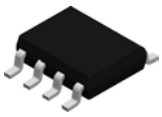
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV2314QDRQ1 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV314QDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV314QDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV314QDBVTQ1 | SOT-23 | DBV | 5 | 250 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV314QDBVTQ1 | SOT-23 | DBV | 5 | 250 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV4314QPWRQ1 | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TLV2314QDRQ1 | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| TLV314QDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TLV314QDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TLV314QDBVTQ1 | SOT-23 | DBV | 5 | 250 | 210.0 | 185.0 | 35.0 |
| TLV314QDBVTQ1 | SOT-23 | DBV | 5 | 250 | 210.0 | 185.0 | 35.0 |
| TLV4314QPWRQ1 | TSSOP | PW | 14 | 2000 | 353.0 | 353.0 | 32.0 |

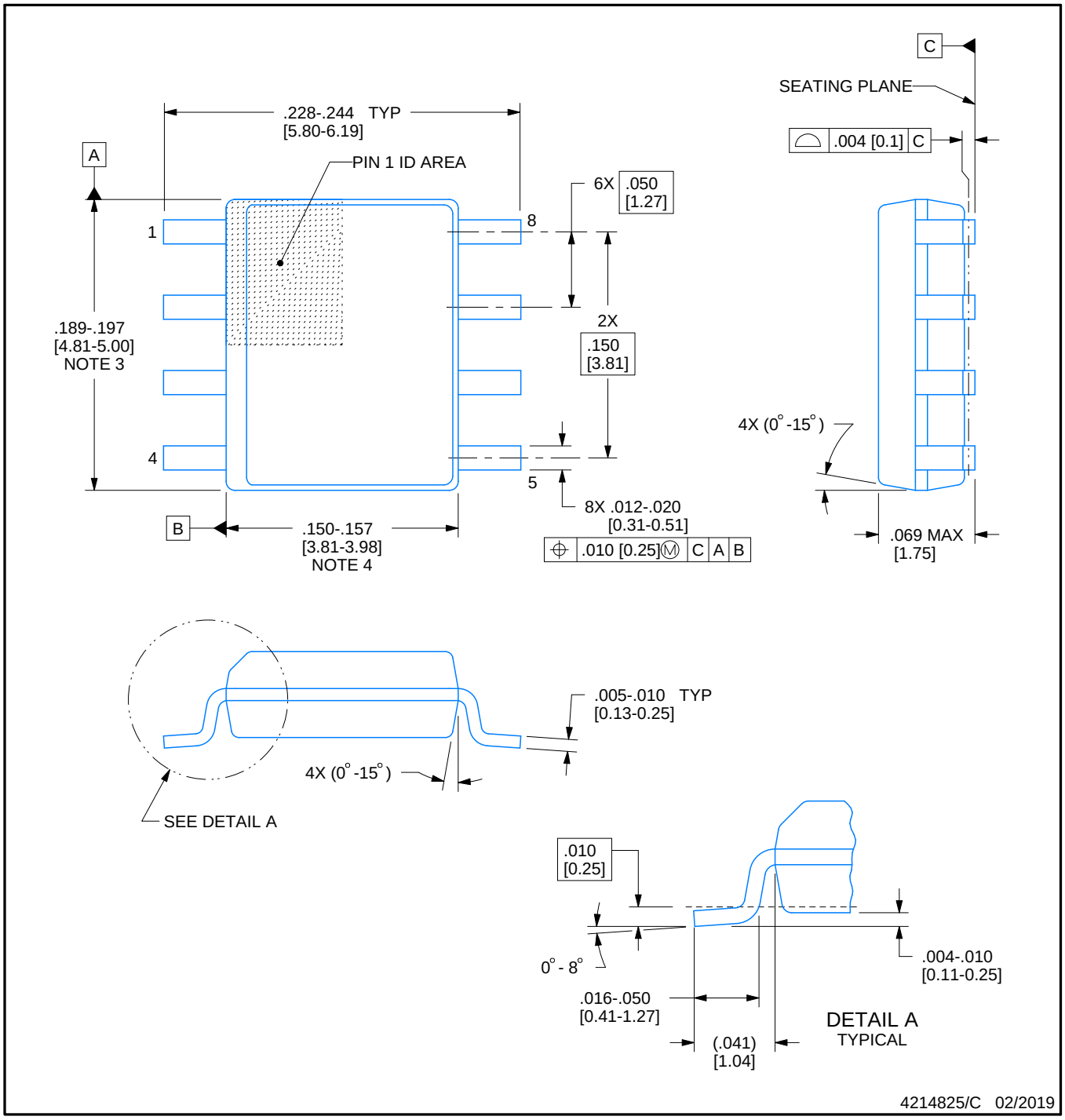


# PACKAGE OUTLINE

## D0008A

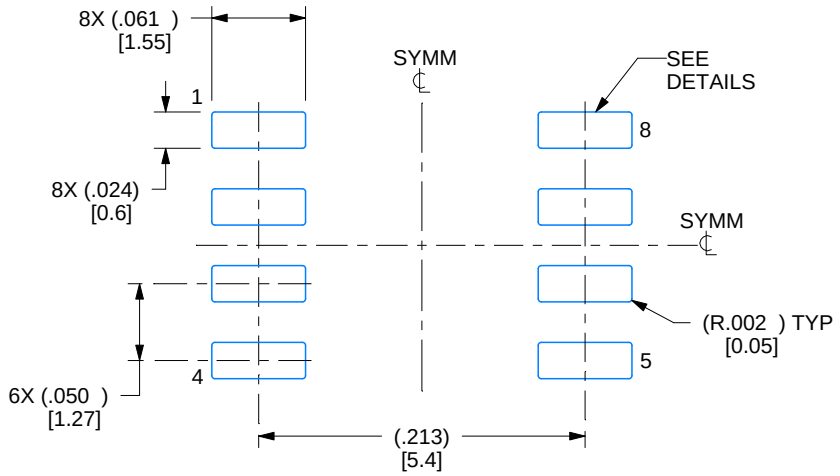
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

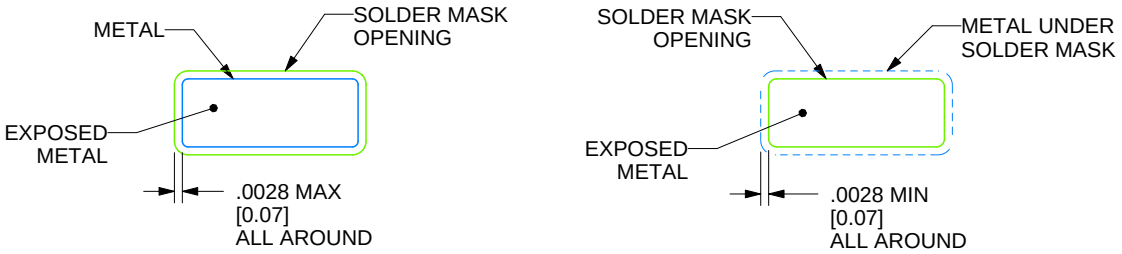



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

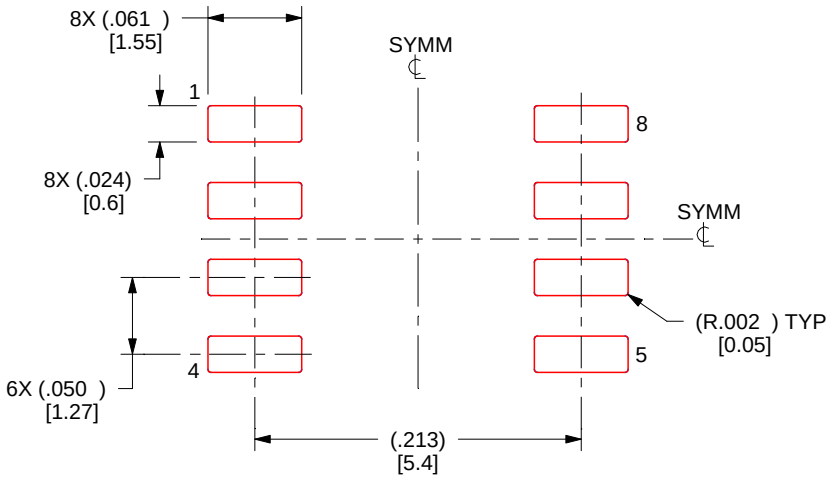



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



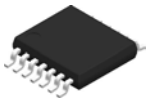

SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

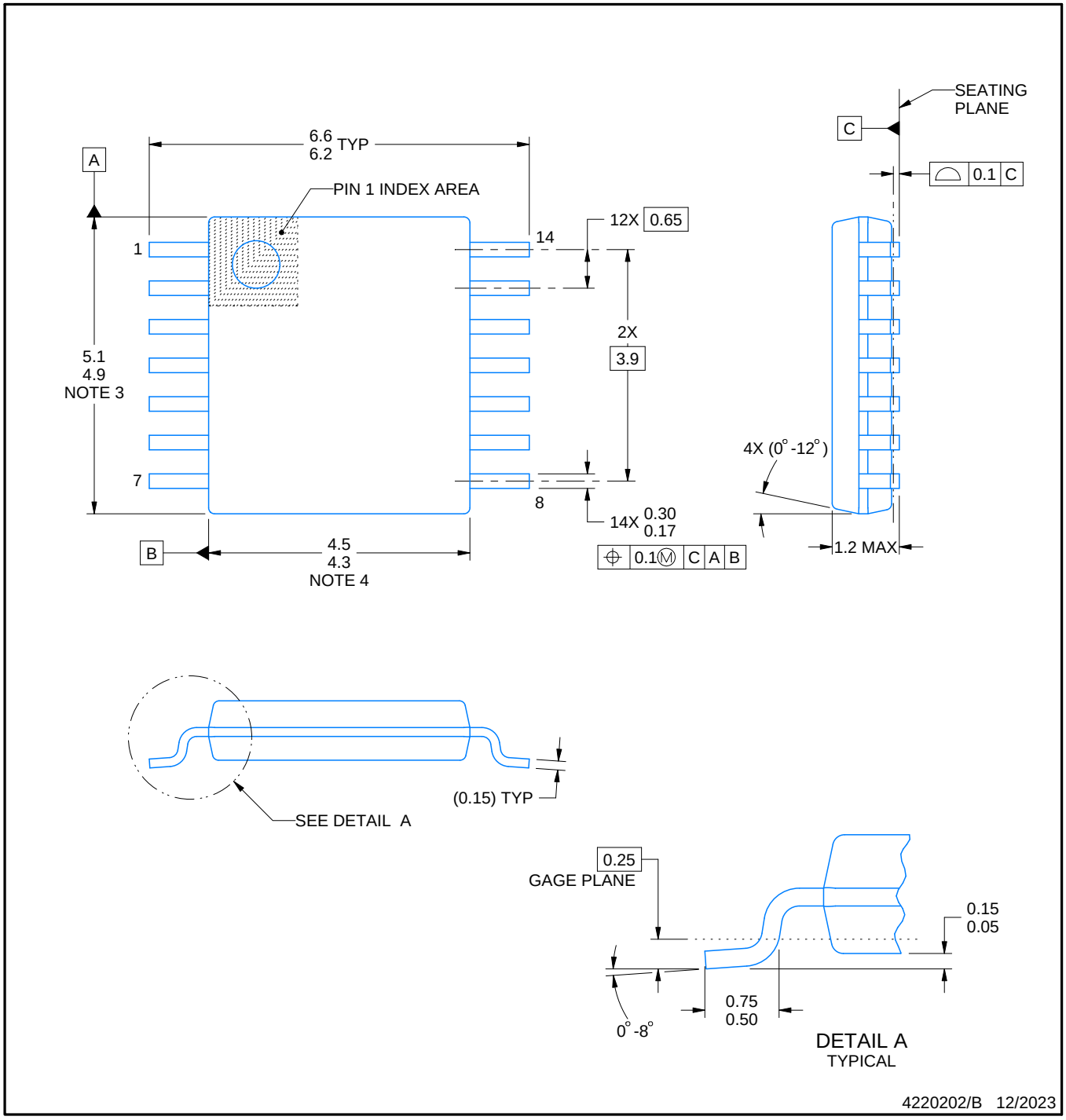
# PW0014A



# PACKAGE OUTLINE

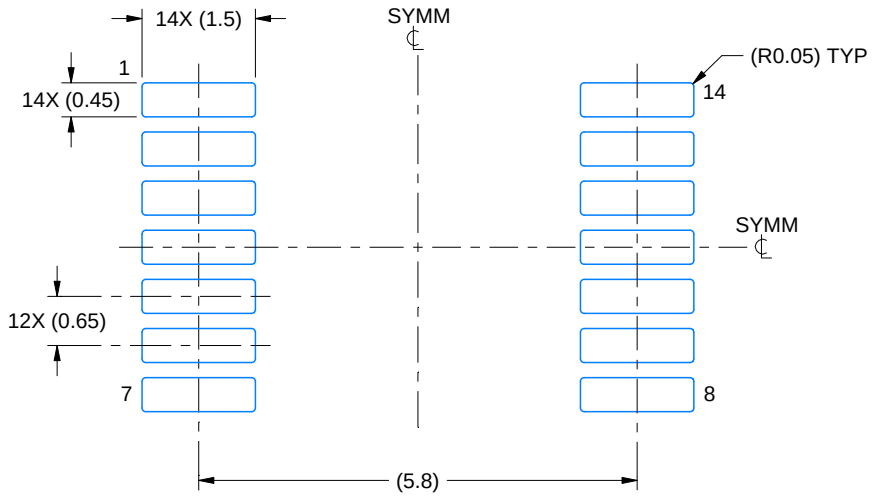
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

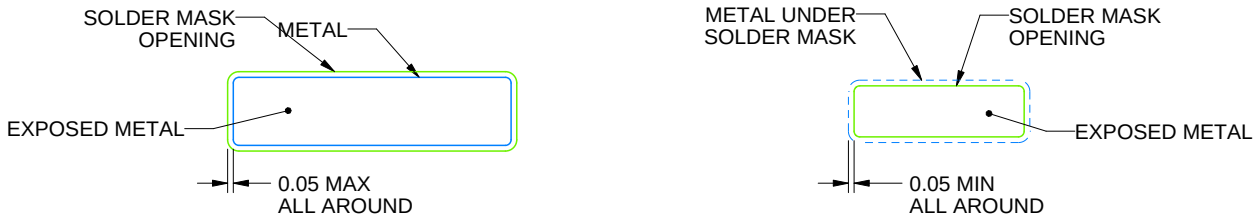



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X




NON-SOLDER MASK DEFINED (PREFERRED)

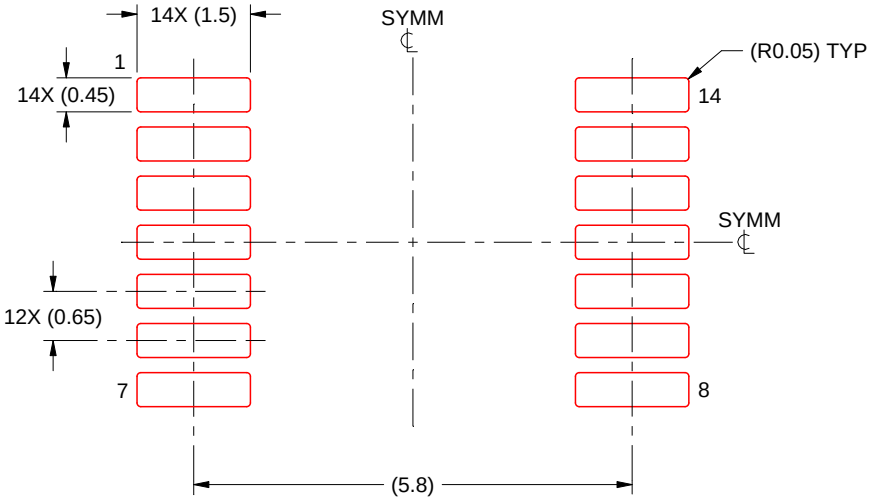
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

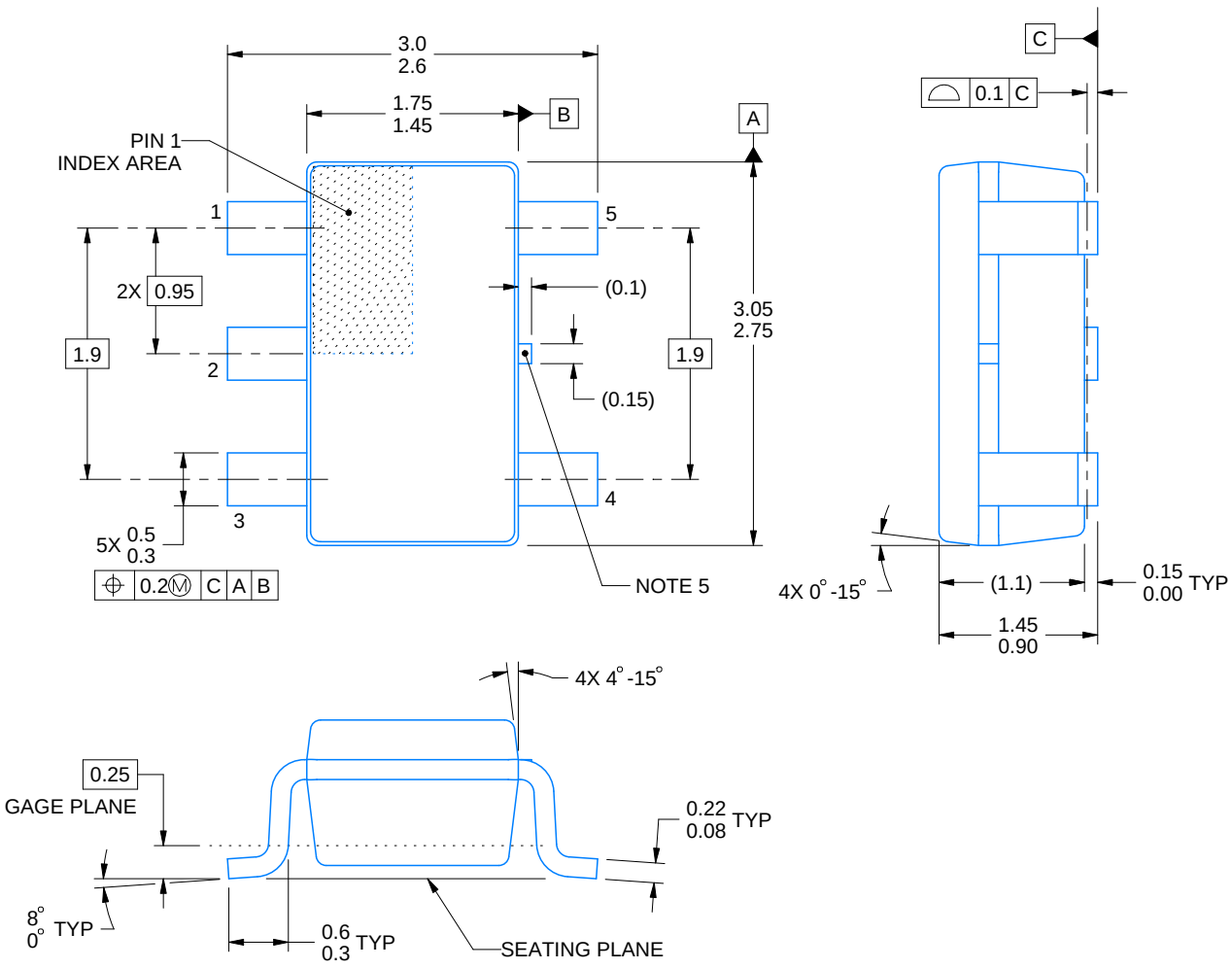



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

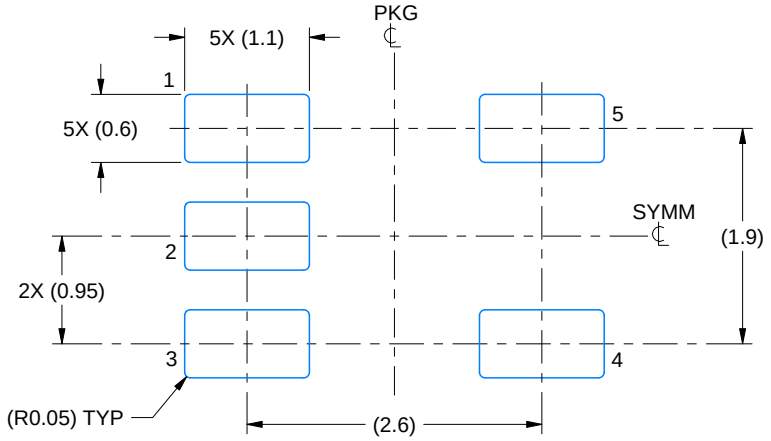
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



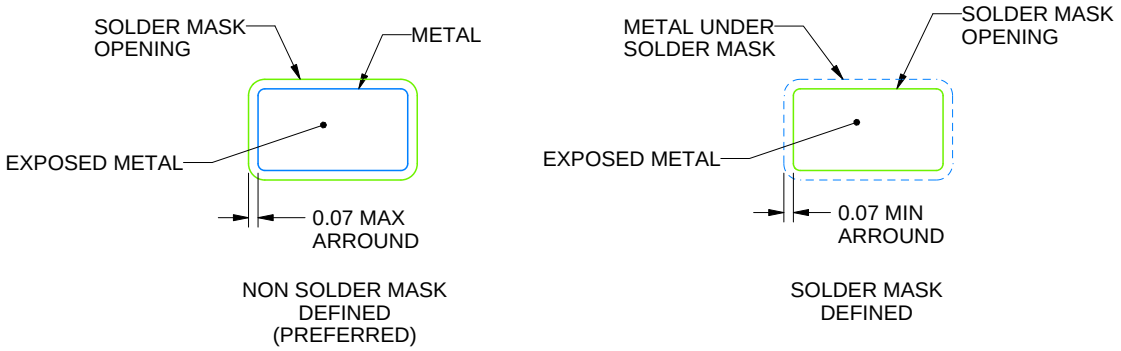

4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

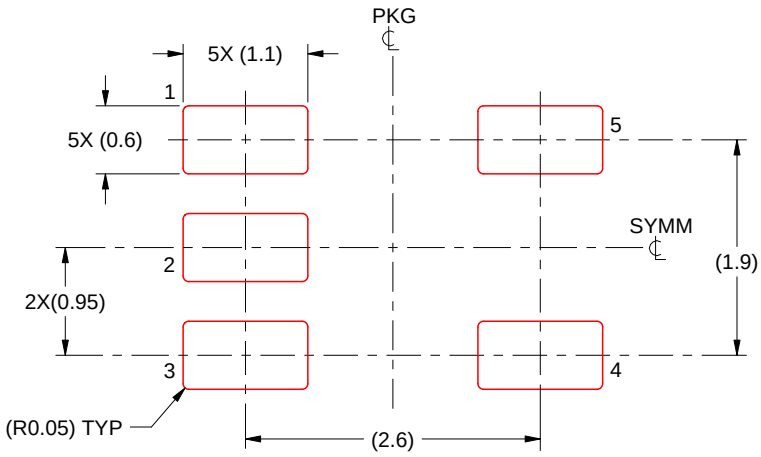



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月