TLV243x and TLV243xA Rail-to-Rail Output, Wide-Input-Voltage Operational Amplifiers

1 Features

- Output swing includes both supply rails
- Extended common-mode input voltage range:
  - 0V to 4.5V (minimum) with 5V single supply
- No phase inversion
- Low Noise: 18nV/√Hz typical at f = 1kHz
- Low input offset voltage 950µV max at T_A = 25°C (TLV243xA)
- Low input bias current: 1pA typ
- Very low supply current: 125µA per channel maximum
- 600Ω output drive
- Automotive version available: TLV243x-Q1

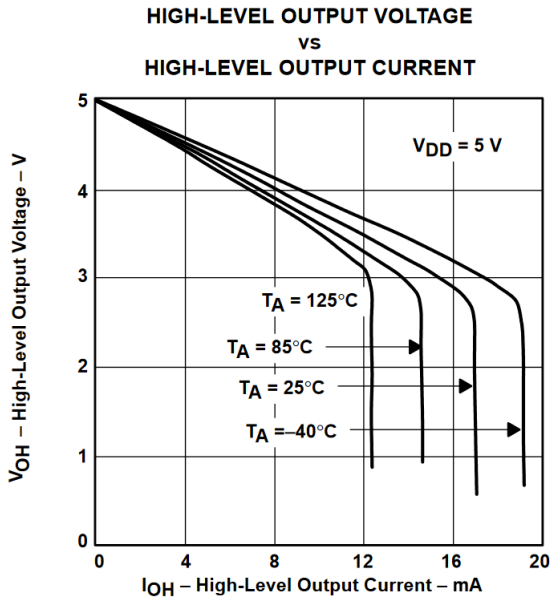
2 Description

The TLV243x and TLV243xA are low-voltage operational amplifiers from Texas Instruments. The common-mode input voltage range for each device is extended over the typical CMOS amplifiers making them an excellent choice for a wide range of applications. In addition, these devices do not phase invert when the common-mode input is driven to the supply rails. This feature satisfies most design requirements without paying a premium for rail-to-rail input performance. These devices also exhibit rail-to-rail output performance for increased dynamic range in single- or split-supply applications. These devices are fully characterized for 3V and 5V supplies, and are optimized for low-voltage operation. The TLV243x and TLV243xA only require 100µA (typical) of supply current per channel, making these devices an excellent choice for battery-powered applications. The TLV243x also have increased output drive over previous rail-to-rail operational amplifiers and are able to drive 600Ω loads for telecom applications.

Device Information

PART NUMBER(1)	CHANNEL COUNT	PACKAGE
TLV2432, TLV2432A	Dual	D (SOIC, 8)
		PW (TSSOP, 8)
TLV2434, TLV2434A	Quad	D (SOIC, 14)
		PW (TSSOP, 14)

(1) For more information, see Section 8.



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3 Pin Configuration and Functions

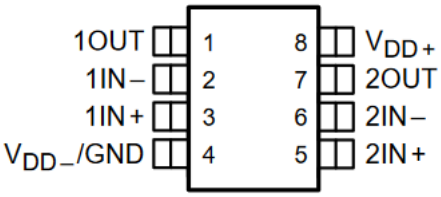


Figure 3-1. TLV2432x: D Package, 8-Pin SOIC (Top View)

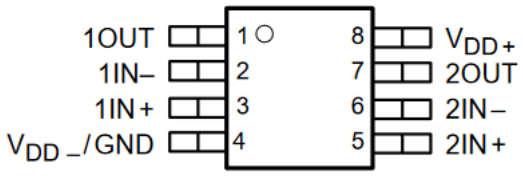


Figure 3-2. TLV2432x: PW Package, 8 Pin TSSOP (Top View)

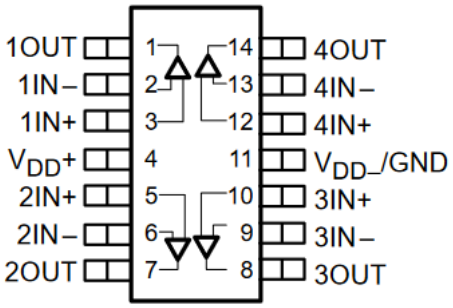


Figure 3-3. TLV2434x: D Package, 14-Pin SOIC, and PW Package, 14-Pin TSSOP (Top View)

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			VALUE	UNIT
V_{DD}	Supply voltage(2)		12	V
V_{ID}	Differential input voltage(3)		$V_{DD±}$	V
V_I	Input voltage range, (any input)		–0.3 to v_{DD}	V
I_I	Input current		± 5	mA
I_O	Output current		± 50	mA
	Total current into V_{DD+}		± 50	mA
	Total current out of $V_{DD–}$		± 50	mA
	Duration of short-circuit current at (or below) T_A = 25°C(4)		Unlimited	
	Continuous total dissipation		See Section 4.2	
T_A	Operating free-air temperature	C suffix	0 to 70	°C
		I suffix (dual)	–40 to +85	
		I suffix (quad)	–40 to +125	
		Q suffix	–40 to +125	
T_{stg}	Storage temperature		–65 to +150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and $V_{CC–}$.
(3) Differential voltages are at IN+ with respect to IN−. Excessive current flows, if input, are brought to less than $V_{CC–}$ −0.3 V.
(4) The output is able to short to either supply. Limit temperature, supply voltages, or both to not exceed the maximum dissipation ratings.

4.2 Dissipation Ratings

PACKAGE	T_A≤ 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D (8)	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
D (14)	1022 mW	7.6 mW/°C	900 mW	777 mW	450 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
PW (8)	525 mW	4.2 mW/°C	336 mW	273 mW	105 mW
PW (14)	720 mW	5.6 mW/°C	634 mW	547 mW	317 mW
U	675 mW	5.4 mW/°C	432 mW	350 mW	135 mW

4.3 Recommended Operating Conditions

		C SUFFIX		I SUFFIX (DUAL)		I SUFFIX (QUAD)		Q SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{DD}	Supply voltage	2.7	10	2.7	10	2.7	10	2.7	10	V
V_I	Input voltage	$V_{DD–}$	V_{DD+}– 0.8	$V_{DD–}$	V_{DD+}– 0.8	$V_{DD–}$	V_{DD+}– 0.8	$V_{DD–}$	V_{DD+}– 0.8	V
V_{IC}	Common-mode input voltage	$V_{DD–}$	V_{DD+}– 1.3	$V_{DD–}$	V_{DD+}– 1.3	$V_{DD–}$	V_{DD+}– 1.3	$V_{DD–}$	V_{DD+}– 1.3	V
T_A	Operating free-air temperature	0	70	−40	85	−40	125	−40	125	°C

4.4 Electrical Characteristics, V_{DD} = 3 V, I and C Suffixes

at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	TLV243xC, TLV243xI, TLV243xAC, TLV243xAI			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0 V, V_O = 0 V, R_S = 50 Ω, $V_{DD±}$ = ±1.5 V	TLV243xC, TLV243xI	25°C		300	2000	µV
				Full range			2500	
			TLV243xAC, TLV243xAI	25°C		300	950	
				Full range			1500	
α_{VIO}	Temperature coefficient of input offset voltage	VO = 0 V, VIC = 0 V, $V_{DD±}$ = ±1.5 V, R_S = 50 Ω		25°C to 70°C		2		µV/°C
	Input offset voltage long-term drift (2)			25°C		0.003		µV/MO
I_{IO}	Input offset current			25°C		0.5	60	pA
				Full Range			150	
I_{IB}	Input bias current			25°C		1	60	pA
				Full Range			150	
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\| \le$ 5 mV, R_S = 50 Ω		25°C	0 to 2.5	–0.25 to 2.75		V
				Full range	0 to 2.2			V
V_{OH}	High-level output voltage	I_{OH} = –100 µA		25°C		2.98		V
		I_{OH} = –3 mA		25°C		2.5		
				Full range	2.25			
V_{OL}	Low-level output voltage	V_{IC} = 1.5 V, I_{OL} = 100 µA		25°C		0.02		V
		V_{IC} = 1.5 V, I_{OL} = 3 mA		25°C		0.83		
				Full range			1	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 2 V	R_L = 2 kΩ(3)	25°C	1.5	2.5		V/mV
				Full range	1			
			R_L = 1 MΩ(3)	Full range		750		
$ri_{(d)}$	Differential input resistance			25°C		1000		$G_Ω$
$ri_{(c)}$	Common-mode input resistance			25°C		1000		$G_Ω$
$ci_{(c)}$	Common-mode input capacitance			25°C		8		pF
z_o	Closed-loop output impedance			25°C		130		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 V to 2.5 V, V_O = 1.5 V, R_S = 50 Ω		25°C	63	83		dB
				Full range	63			
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} /ΔV_{IO})	V_{DD} = 2.7 V to 8 V, V_{IC} = V_{DD}/2, no load		25°C	80	95		dB
				Full range	80			
I_{DD}	Supply current (per channel)	V_O = 1.5 V, no load		25°C		115	150	µA
				Full range			175	

(1) Full range for C suffix is 0°C to 70°C. Full range for dual I suffix is – 40°C to +85°C. Full range for quad I suffix is – 40°C to +125°C.
(2) Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A= 150°C extrapolated to T_A= 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.
(3) Referenced to 2.5 V.

4.5 Operating Characteristics, V_{DD} = 3 V, I and C Suffixes

at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	TLV243xC, TLV243xI, TLV243xAC,TLV243xAI			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1 V to 2 V, R_L = 2 kΩ(2), C_L = 100 pF(2)		25°C	0.15	0.25		V/μs
				Full range	0.1			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		120		nV/√Hz
		f = 1 kHz		25°C		22		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		2.7		μV
		f = 0.1 Hz to 10 Hz		25°C		4		
I_n	Equivalent input noise current			25°C		0.6		fA√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 1 kHz, R_L = 2 kΩ(2)	A_V = 1	25°C		0.065%		
			A_V = 10	25°C		0.5%		
	Gain-bandwidth product	f = 10 kHz, R_L = 2 kΩ(2), C_L = 100 pF(2)		25°C		0.5		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 1 V, A_V = 1, R_L = 2 kΩ(2), C_L = 100 pF(2)		25°C		220		kHz
t_s	Settling time	A_V = –1, step = 0.5 V to 2.5 V, R_L = 2 kΩ(2), C_L = 100 pF(2)	To 0.1%	25°C		6.4		μs
			To 0.01%	25°C		14.1		
φ_m	Phase margin at unity gain	R_L = 2 kΩ(2), C_L = 100 pF(2)		25°C		62°		
	Gain margin	R_L = 2 kΩ(2), C_L = 100 pF(2)		25°C		11		dB

(1) Full range for C suffix is 0°C to 70°C. Full range for dual I suffix is – 40°C to 85°C. Full range for quad I suffix is – 40°C to 125°C.
(2) Referenced to 2.5 V.

4.6 Electrical Characteristics, V_{DD} = 3 V, Q Suffix

at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	TLV243xQ, TLV243xAQ			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0 V, V_O = 0 V, R_S = 50 Ω, $V_{DD±}$ = ±1.5 V	TLV243xQ	25°C		300	2000	µV
				–40°C to +125°C			2500	
			TLV243xAQ	25°C		300	950	
				–40°C to +125°C			2000	
α_{VIO}	Temperature coefficient of input offset voltage	VO = 0 V, VIC = 0 V, $V_{DD±}$ = ±1.5 V, R_S = 50 Ω		25°C to 70°C		2		µV/°C
	Input offset voltage long-term drift (1)			25°C		0.003		µV/MO
I_{IO}	Input offset current			25°C		0.5	60	pA
				–40°C to +125°C			150	
I_{IB}	Input bias current			25°C		1	60	pA
				–40°C to +125°C			300	
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\| \le$ 5 mV, R_S = 50 Ω		25°C	0 to 2.5	–0.25 to 2.75		V
				–40°C to +125°C	0 to 2.2			V
V_{OH}	High-level output voltage	I_{OH} = –100 µA		25°C		2.98		V
		I_{OH} = –3 mA		25°C		2.5		
				–40°C to +125°C	2.25			
V_{OL}	Low-level output voltage	V_{IC} = 1.5 V, I_{OL} = 100 µA		25°C		0.02		V
		V_{IC} = 1.5 V, I_{OL} = 3 A		25°C		0.83		
				–40°C to +125°C			1	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 2 V	R_L = 2 kΩ(2)	25°C	1.5	2.5		V/mV
				–40°C to +125°C	0.5			
			R_L = 1 MΩ(2)	–40°C to +125°C		750		
$ri_{(d)}$	Differential input resistance			25°C		1000		$G_Ω$
$ri_{(c)}$	Common-mode input resistance			25°C		1000		$G_Ω$
$ci_{(c)}$	Common-mode input capacitance			25°C		8		pF
z_o	Closed-loop output impedance			25°C		130		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 V to 2.5 V, V_O = 1.5 V, R_S = 50 Ω		25°C	63	83		dB
				–40°C to +125°C	63			
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} /ΔV_{IO})	V_{DD} = 2.7 V to 8 V, V_{IC} = V_{DD}/2, no load		25°C	80	95		dB
				–40°C to +125°C	80			
I_{DD}	Supply current (per channel)	V_O = 1.5 V, no load		25°C		115	150	µA
				–40°C to +125°C			175	

(1) Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A= 150°C extrapolated to T_A= 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.
(2) Referenced to 2.5 V.

4.7 Operating Characteristics, V_{DD} = 3 V, Q Suffix

at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	TLV243xQ, TLV243xAQ			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1 V to 2 V, R_L = 2 kΩ(1), C_L = 100 pF(1)		25°C	0.15	0.25		V/μs
				–40°C to +125°C	0.1			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		120		nV/√Hz
		f = 1 kHz		25°C		22		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		2.7		μV
		f = 0.1 Hz to 10 Hz		25°C		4		
I_n	Equivalent input noise current			25°C		0.6		fA√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 1 kHz, R_L = 2 kΩ(2)	A_V = 1	25°C		0.065%		
			A_V = 10	25°C		0.5%		
	Gain-bandwidth product	f = 10 kHz, R_L = 2 kΩ(2), C_L = 100 pF(2)		25°C		0.5		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 1 V, A_V = 1, R_L = 2 kΩ(2), C_L = 100 pF(2)		25°C		220		kHz
t_s	Settling time	A_V = –1, step = 0.5 V to 2.5 V, R_L = 2 kΩ(1), C_L = 100 pF(1)	To 0.1%	25°C		6.4		μs
			To 0.01%	25°C		14.1		
φ_m	Phase margin at unity gain	R_L = 2 kΩ(1), C_L = 100 pF(1)		25°C		62°		
	Gain margin	R_L = 2 kΩ(1), C_L = 100 pF(1)		25°C		11		dB

(1) Referenced to 2.5 V.

4.8 Electrical Characteristics, V_{DD} = 5 V, I and C Suffixes

at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	TLV243xC, TLV243xI, TLV243xAC, TLV243xAI			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0 V, V_O = 0 V, R_S = 50 Ω, $V_{DD±}$ = ±2.5 V	TLV243xC, TLV243xI	25°C		300	2000	μV
				Full range			2500	
			TLV243xAC, TLV243xAI	25°C		300	950	
				Full range			1500	
α_{VIO}	Temperature coefficient of input offset voltage	VO = 0 V, VIC = 0$V_{DD±}$ = ±2.5 V, R_S = 50 Ω		25°C to 70°C		2		μV/°C
	Input offset voltage long-term drift (2)			25°C		0.003		μV/MO
I_{IO}	Input offset current			25°C		0.5	60	pA
				Full Range			150	
I_{IB}	Input bias current			25°C		1	60	pA
				Full Range			150	
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\| \le$ 5 mV, R_S = 50 Ω		25°C	0 to 4.5	–0.25 to 4.75		V
				Full range	0 to 4.2			V
V_{OH}	High-level output voltage	I_{OH} = –100 μA		25°C		4.97		V
		I_{OH} = –5 mA		25°C	4	4.35		
				Full range	4			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V, I_{OL} = 100 μA		25°C		0.01		V
		V_{IC} = 2.5 V, I_{OL} = 5 mA		25°C		0.8		
				Full range			1.25	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 2 kΩ(3)	25°C	2.5	3.8		V/mV
				Full range	1.5			
			R_L = 1 MΩ(3)	Full range		950		
$ri_{(d)}$	Differential input resistance			25°C		1000		$G_Ω$
$ri_{(c)}$	Common-mode input resistance			25°C		1000		$G_Ω$
$ci_{(c)}$	Common-mode input capacitance	f = 10 kHz		25°C		8		pF
z_o	Closed-loop output impedance	f = 100 kHz, A_V = 10		25°C		130		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 V to 4.5 V, V_O = 2.5 V, R_S = 50 Ω		25°C	63	90		dB
				Full range	63			
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} /ΔV_{IO})	V_{DD} = 4.4 V to 8 V, V_{IC} = V_{DD}/2, no load		25°C	80	95		dB
				Full range	80			
I_{DD}	Supply current (per channel)	V_O = 2.5 V, no load		25°C		115	150	μA
				Full range			175	

(1) Full range for C suffix is 0°C to 70°C. Full range for dual I suffix is – 40°C to +85°C. Full range for quad I suffix is – 40°C to +125°C.
(2) Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A= 150°C extrapolated to T_A= 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.
(3) Referenced to 2.5 V.

4.9 Operating Characteristics, V_{DD} = 5 V, C and I Suffixes

at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	TLV243xC, TLV243xI, TLV243xAC, TLV243xAI			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1.5 V to 3 V, R_L = 2 kΩ(2), C_L = 100 pF(2)		25°C	0.15	0.25		V/μs
				Full range	0.1			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		100		nV/√Hz
		f = 1 kHz		25°C		18		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		1.9		μV
		f = 0.1 Hz to 10 Hz		25°C		2.8		
I_n	Equivalent input noise current			25°C		0.6		fA√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 3.5 V, f = 1 kHz, R_L = 2 kΩ(2)	A_V = 1	25°C		0.045%		
			A_V = 10	25°C		0.4%		
	Gain-bandwidth product	f = 10 kHz, R_L = 2 kΩ(2), C_L = 100 pF(2)		25°C		0.55		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, A_V = 1, R_L = 2 kΩ(2), C_L = 100 pF(2)		25°C		100		kHz
t_s	Settling time	A_V = –1, step = 0.5 V to 3.5 V, R_L = 2 kΩ(2), C_L = 100 pF(2)	To 0.1%	25°C		6.4		μs
			To 0.01%	25°C		13.1		
φ_m	Phase margin at unity gain	R_L = 2 kΩ(2), C_L = 100 pF(2)		25°C		66°		
	Gain margin	R_L = 2 kΩ(2), C_L = 100 pF(2)		25°C		11		dB

(1) Full range for C suffix is 0°C to 70°C. Full range for dual I suffix is –40°C to +85°C. Full range for quad I suffix is –40°C to +125°C.
(2) Referenced to 2.5 V.

4.10 Electrical Characteristics, V_{DD} = 5 V, Q Suffix

at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	TLV243xQ, TLV243xAQ			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0 V, V_O = 0V, R_S = 50 Ω, $V_{DD±}$ = ±2.5 V	TLV2453xQ	25°C		300	2000	µV
				–40°C to +125°C			2500	
			TLV2453xAQ	25°C		300	950	
				–40°C to +125°C			2000	
α_{VIO}	Temperature coefficient of input offset voltage	VO = 0 V, VIC = 0 V, $V_{DD±}$ = ±2.5 V, R_S = 50 Ω		25°C to 70°C		2		µV/°C
	Input offset voltage long-term drift(1)			25°C		0.003		µV/MO
I_{IO}	Input offset current			25°C		0.5	60	pA
				–40°C to +125°C			150	
I_{IB}	Input bias current			25°C		1	60	pA
				–40°C to +125°C			300	
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\| \le$ 5 mV, R_S = 50 Ω		25°C	0 to 4.5	–0.25 to 4.75		V
				–40°C to +125°C	0 to 4.2			V
V_{OH}	High-level output voltage	I_{OH} = –100 µA		25°C		4.97		V
		I_{OH} = –5 mA		25°C	4	4.35		
				–40°C to +125°C	4			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V, I_{OL} = 100 µA		25°C		0.01		V
		V_{IC} = 2.5 V, I_{OL} = 5 mA		25°C		0.8		
				–40°C to +125°C			1.25	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 2 kΩ(2)	25°C	2.5	3.8		V/mV
				–40°C to +125°C	1.5			
			R_L = 1 MΩ(2)	–40°C to +125°C		950		
$ri_{(d)}$	Differential input resistance			25°C		1000		$G_Ω$
$ri_{(c)}$	Common-mode input resistance			25°C		1000		$G_Ω$
$ci_{(c)}$	Common-mode input capacitance	f = 10 kHz		25°C		8		pF
z_o	Closed-loop output impedance	f = 100 kHz, A_V = 10		25°C		130		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 4.5 V, V_O = 2.5 V, R_S = 50 Ω		25°C	63	90		dB
				–40°C to +125°C	63			
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} /ΔV_{IO})	V_{DD} = 4.4 V to 8 V, V_{IC} = V_{DD}/2, no load		25°C	80	95		dB
				–40°C to +125°C	80			
I_{DD}	Supply current (per channel)	V_O = 2.5 V, no load		25°C		115	150	µA
				–40°C to +125°C			175	

(1) Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A= 150°C extrapolated to T_A= 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.
(2) Referenced to 2.5 V.

4.11 Operating Characteristics, V_{DD} = 5 V, Q Suffix

at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	TLV243xQ, TLV243xAQ			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1.5 V to 3 V, R_L = 2 kΩ(1), C_L = 100 pF(1)		25°C	0.15	0.25		V/μs
				–40°C to +125°C	0.1			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		100		nV/√Hz
		f = 1 kHz		25°C		18		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		1.9		μV
		f = 0.1 Hz to 10 Hz		25°C		2.8		
I_n	Equivalent input noise current			25°C		0.6		fA√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 3.5 V, f = 1 kHz, R_L = 2 kΩ(1)	A_V = 1	25°C		0.045%		
			A_V = 10	25°C		0.4%		
	Gain-bandwidth product	f = 10 kHz, R_L = 2 kΩ(1), C_L = 100 pF(1)		25°C		0.55		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, A_V = 1, R_L = 2 kΩ(1), C_L = 100 pF(1)		25°C		100		kHz
t_s	Settling time	A_V = –1, step = 0.5 V to 3.5 V, R_L = 2 kΩ(1), C_L = 100 pF(1)	To 0.1%	25°C		6.4		μs
			To 0.01%	25°C		13.1		
φ_m	Phase margin at unity gain	R_L = 2 kΩ(1), C_L = 100 pF(1)		25°C		66°		
	Gain margin	R_L = 2 kΩ(1), C_L = 100 pF(1)		25°C		11		dB

(1) Referenced to 2.5 V.

4.12 Typical Characteristics

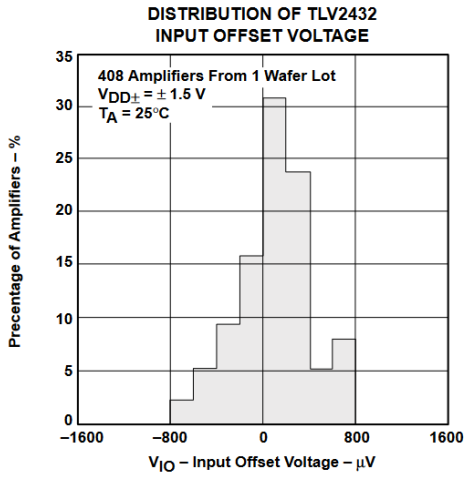


Figure 4-1.

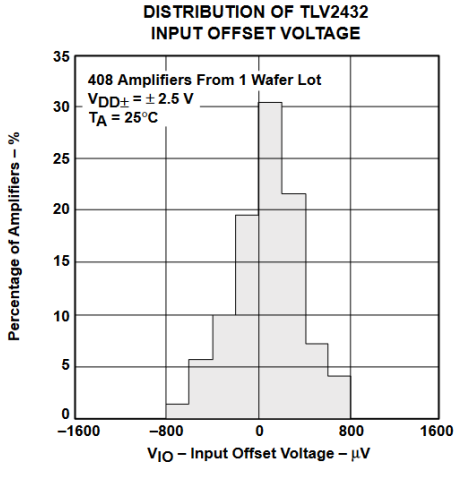
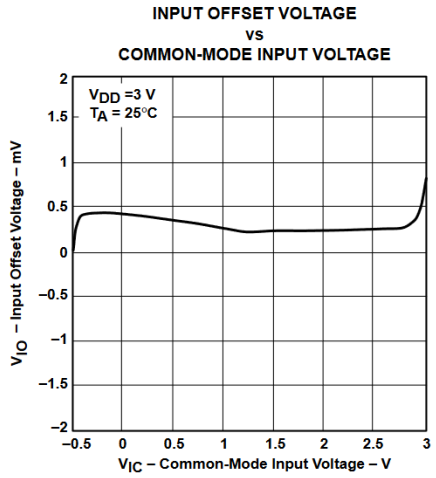


Figure 4-2.



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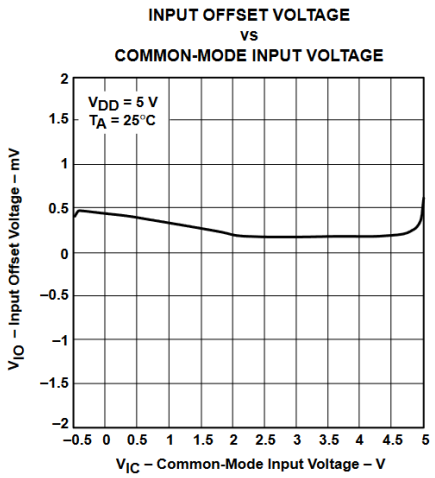

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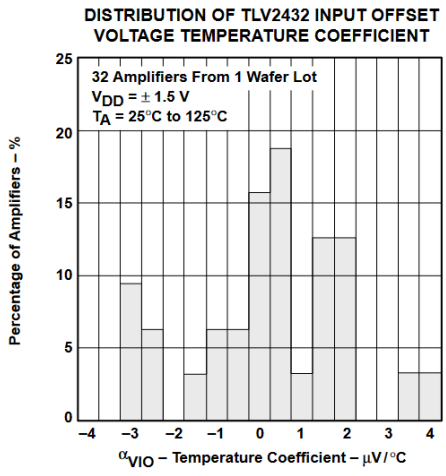

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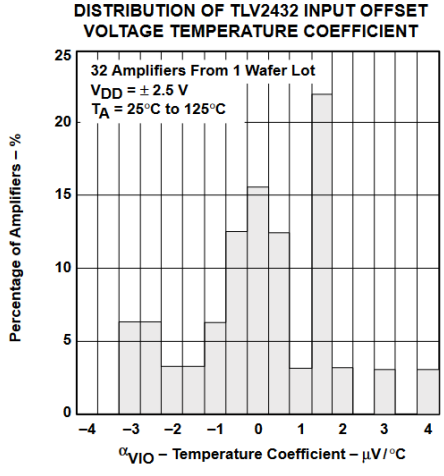
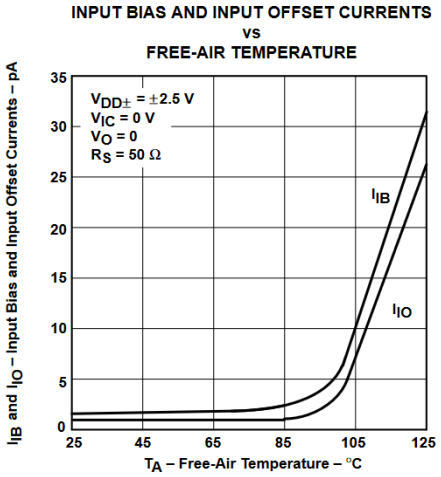


Figure 4-6.

4.12 Typical Characteristics (continued)



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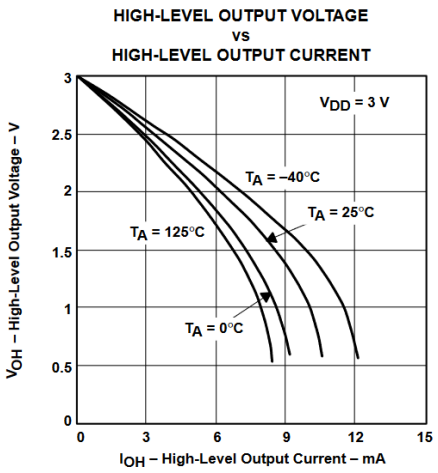

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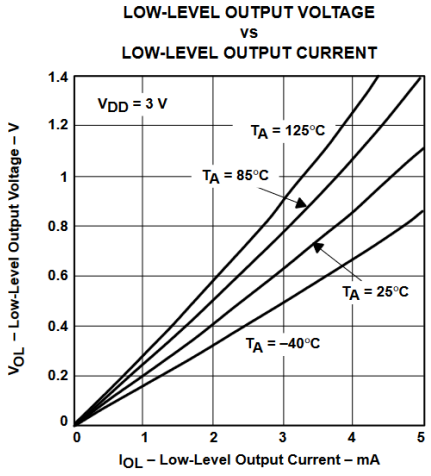

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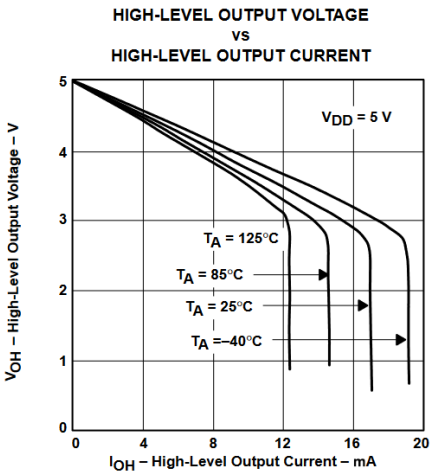

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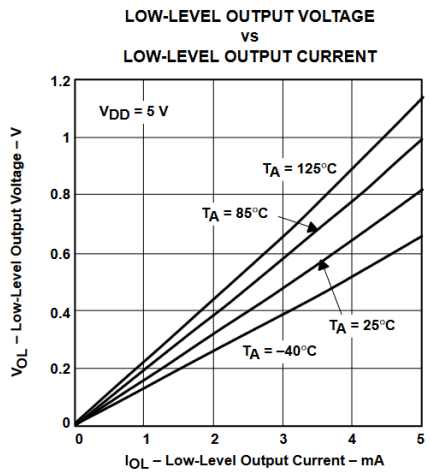

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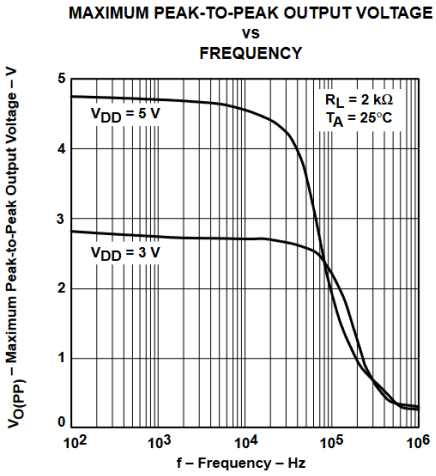
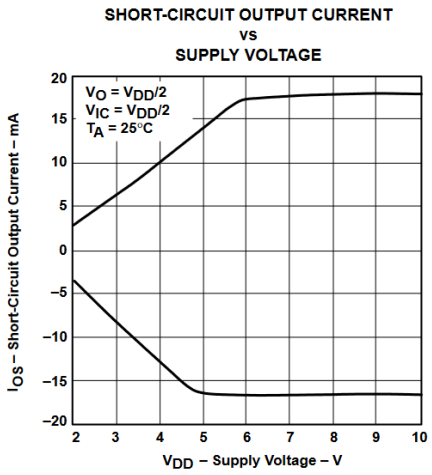


Figure 4-12.

4.12 Typical Characteristics (continued)



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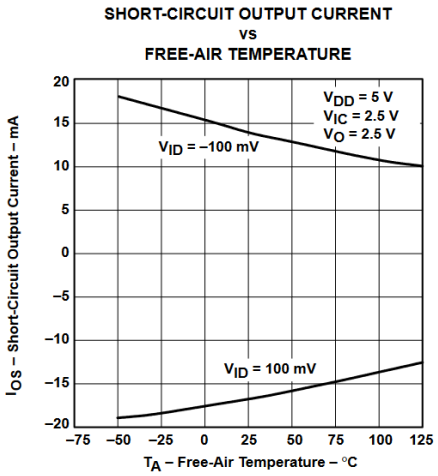

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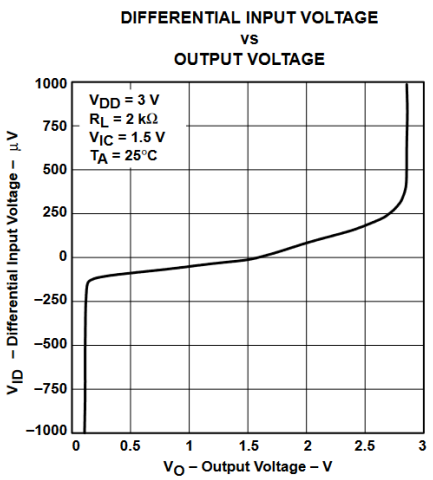

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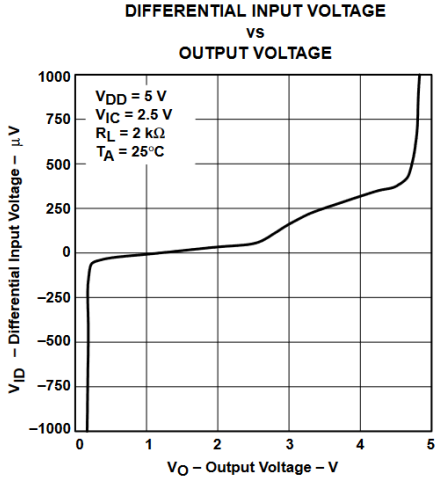

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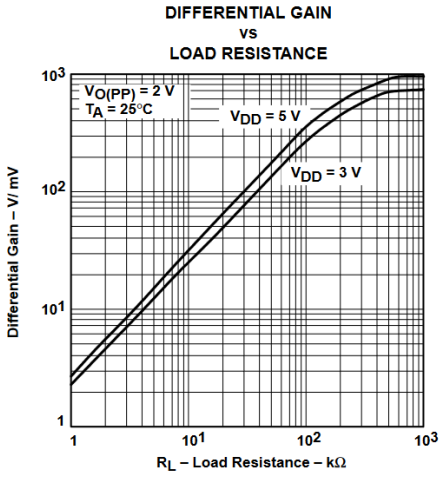

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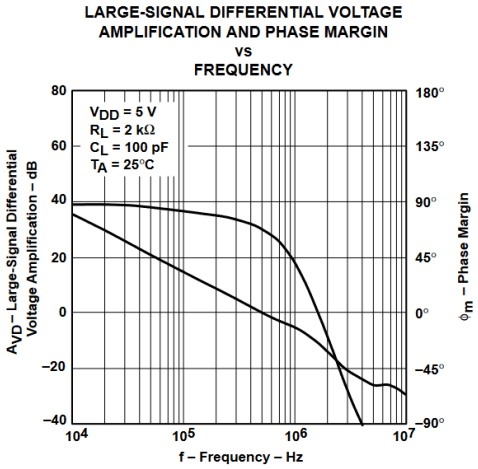
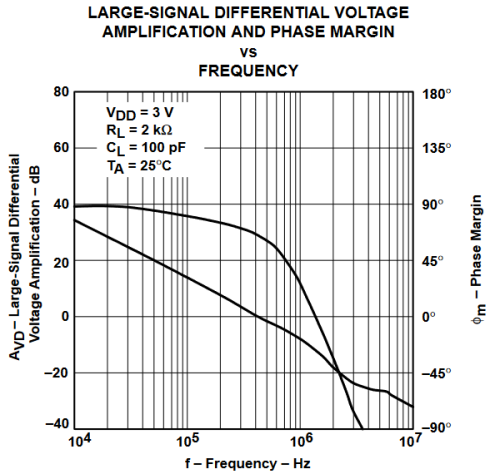


Figure 4-18.

4.12 Typical Characteristics (continued)



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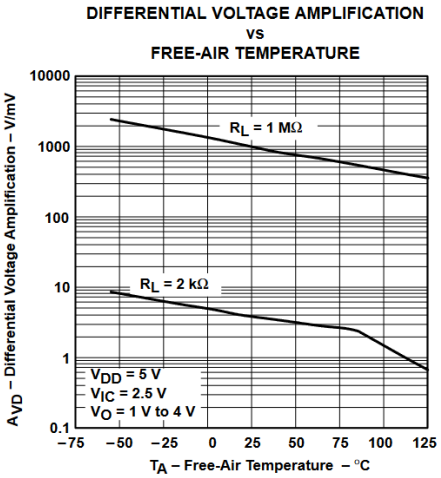

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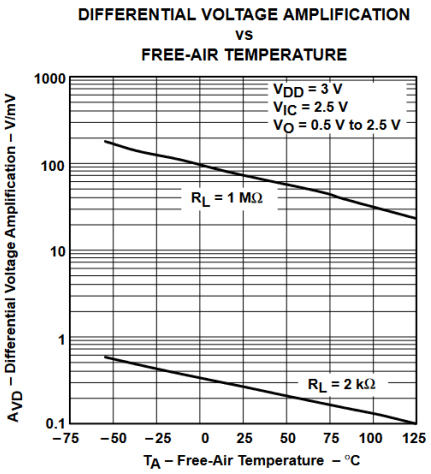

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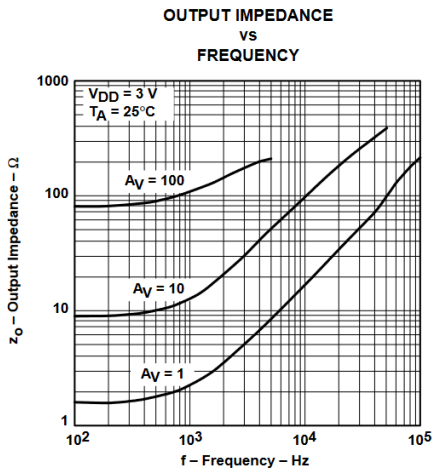

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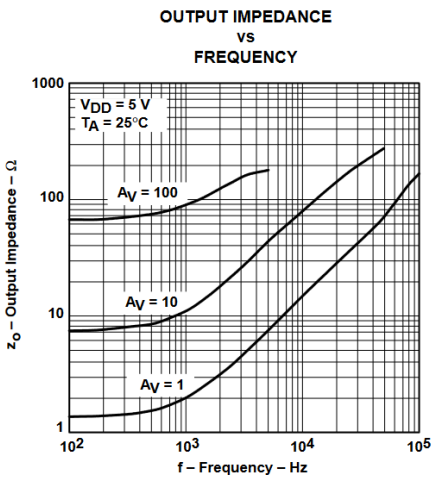

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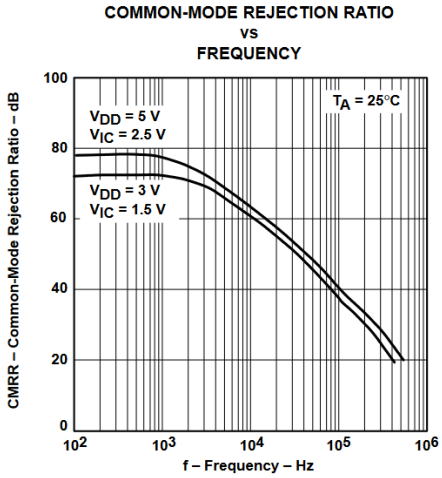
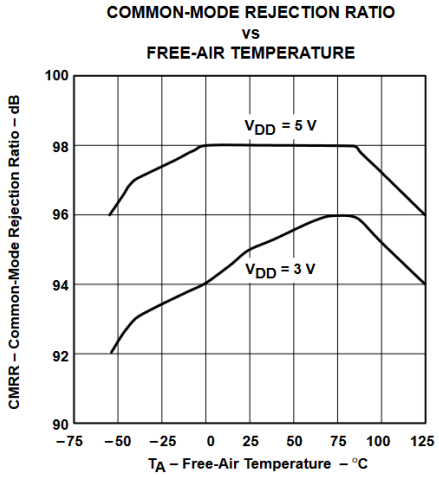


Figure 4-24.

4.12 Typical Characteristics (continued)



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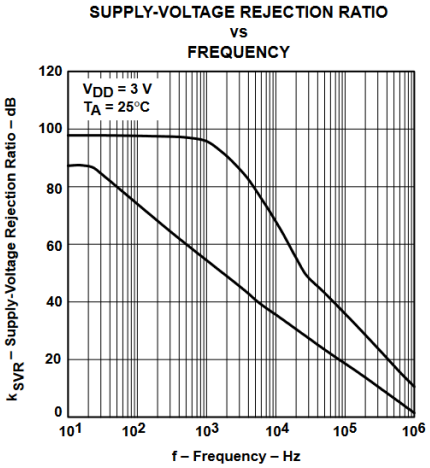

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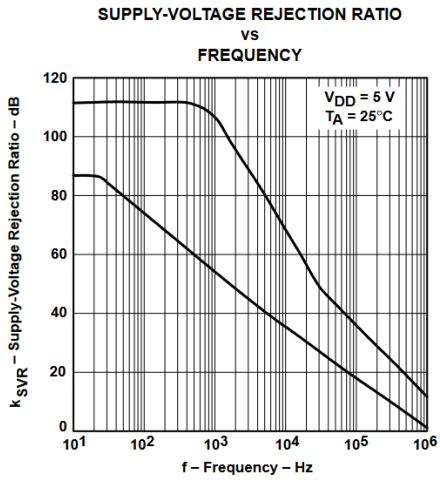

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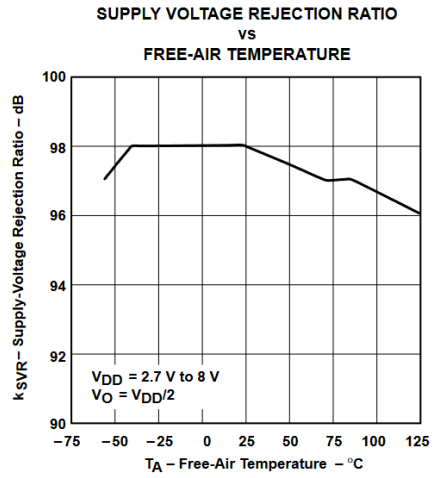

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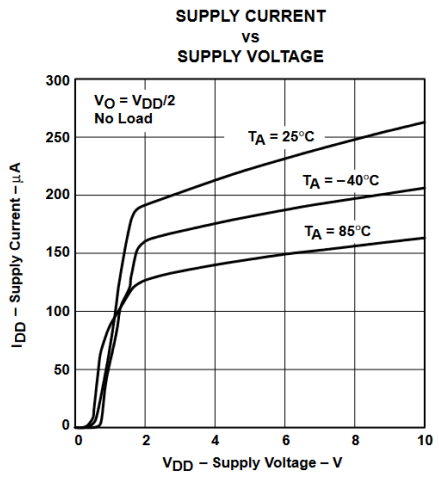

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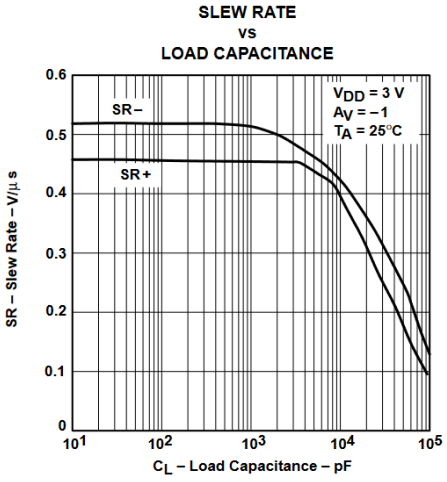
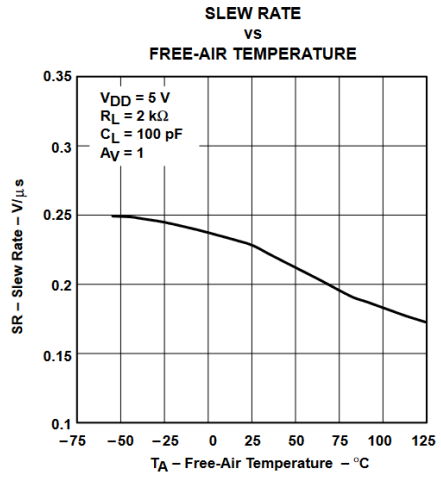


Figure 4-30.

4.12 Typical Characteristics (continued)



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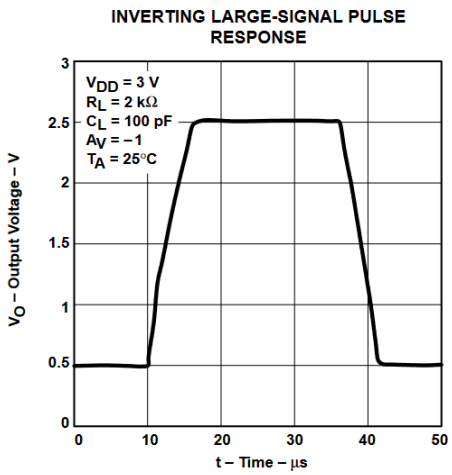

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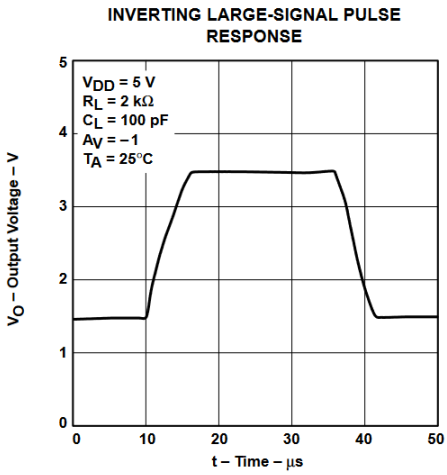

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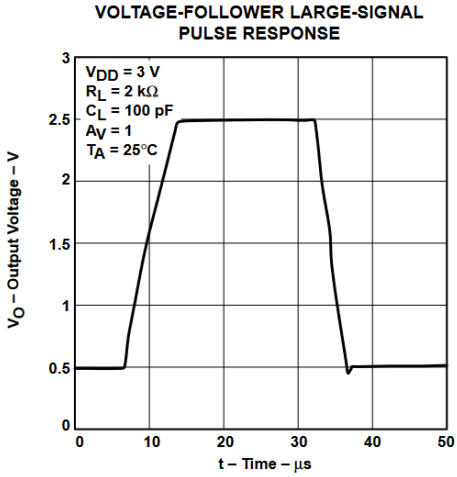

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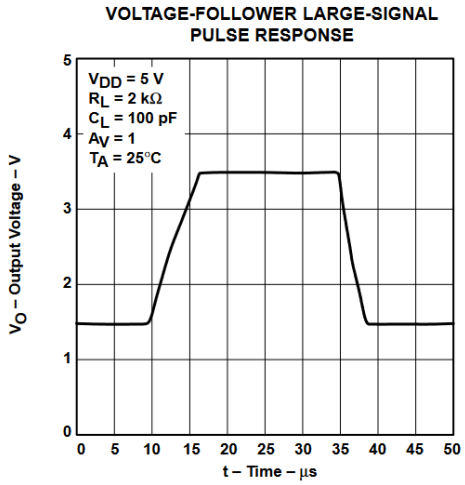

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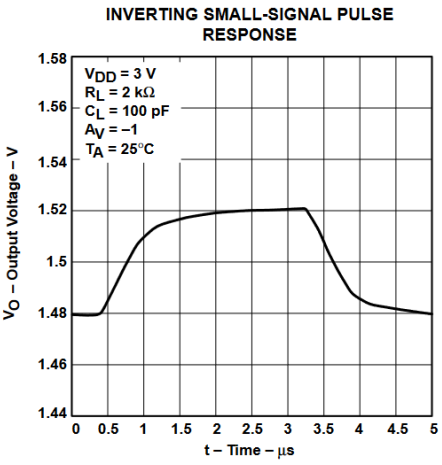
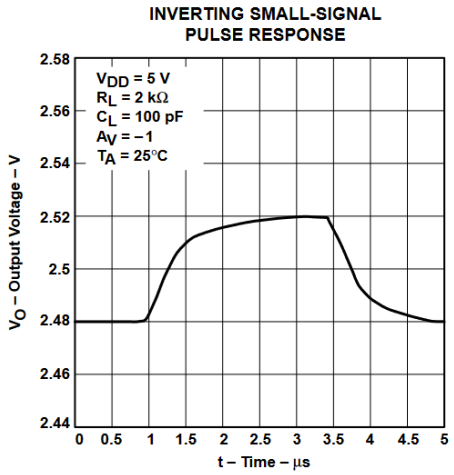


Figure 4-36.

4.12 Typical Characteristics (continued)



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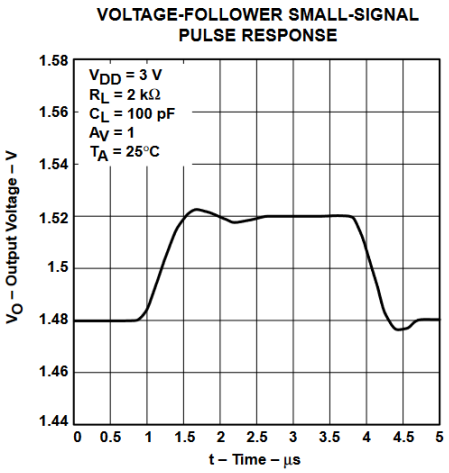
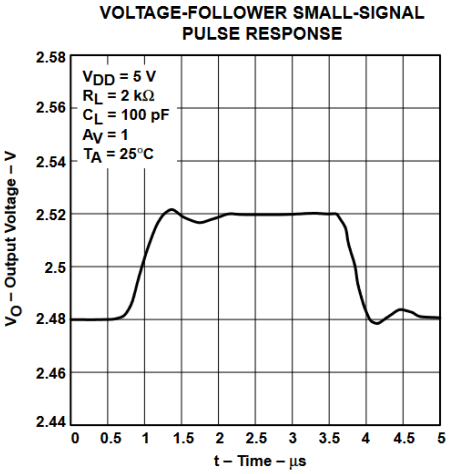


Figure 4-38.



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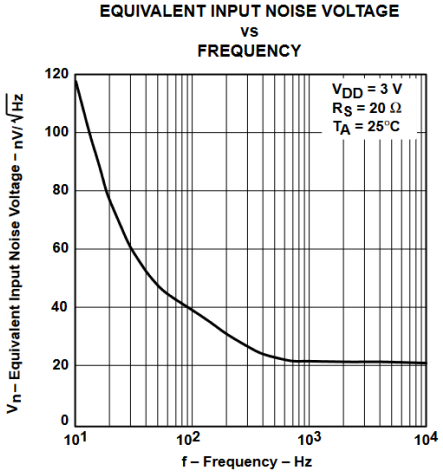

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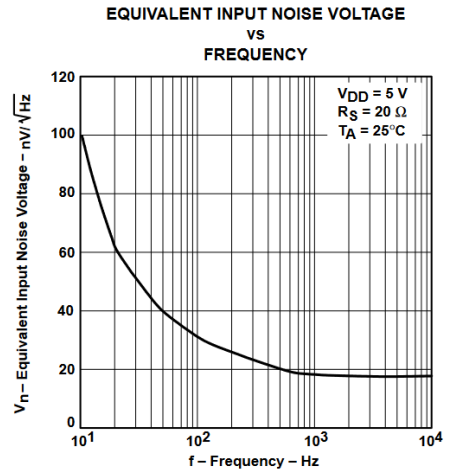


Figure 4-41.

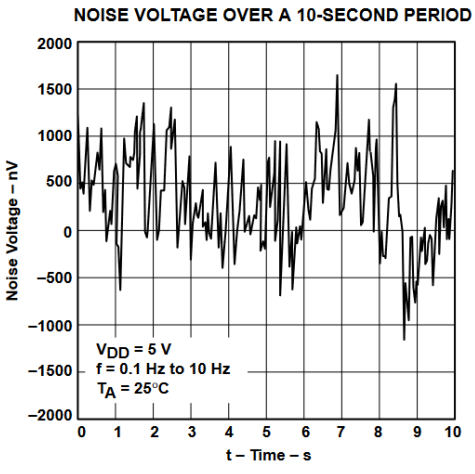
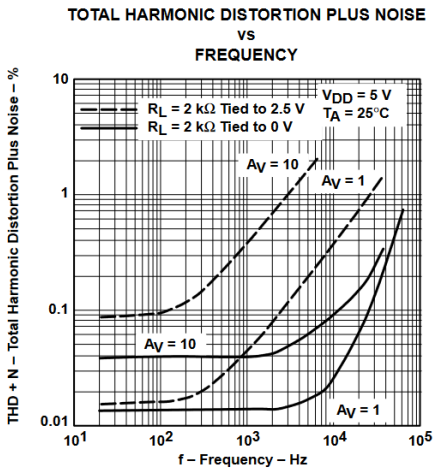


Figure 4-42.

4.12 Typical Characteristics (continued)



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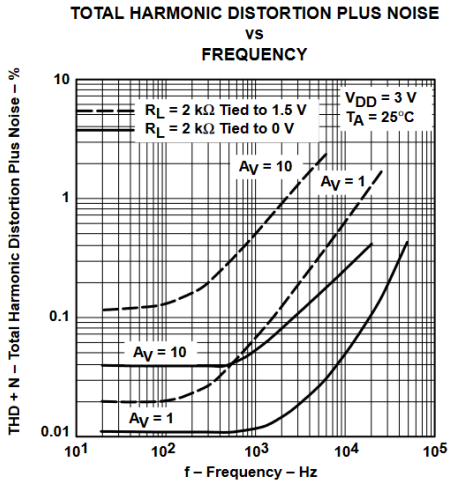


Figure 4-44.

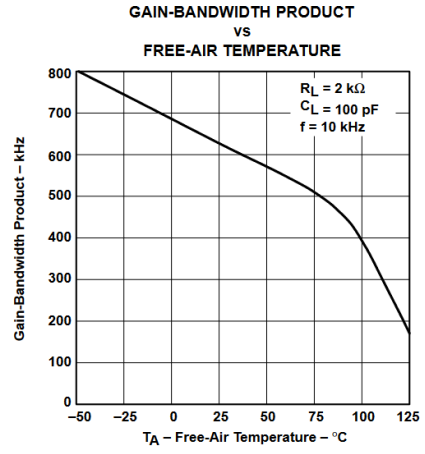


Figure 46

Figure 4-45.

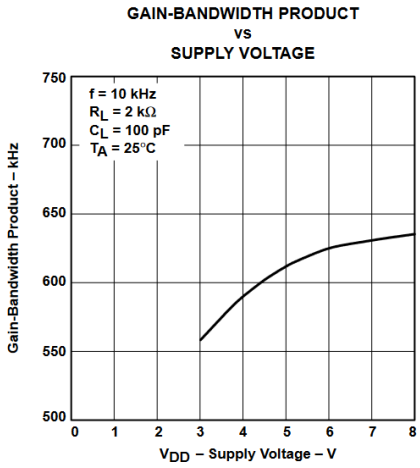
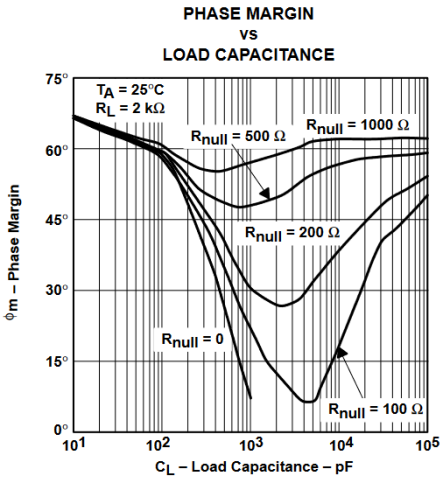


Figure 4-46.



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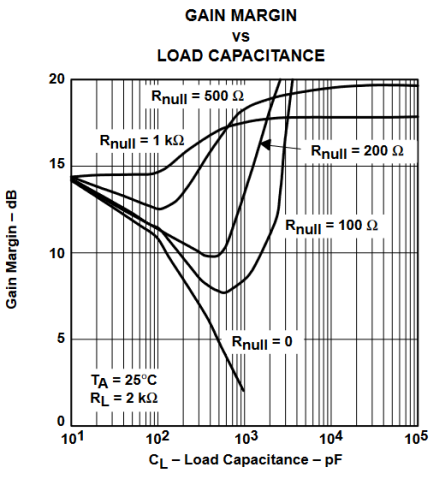


Figure 4-48.

4.12 Typical Characteristics (continued)

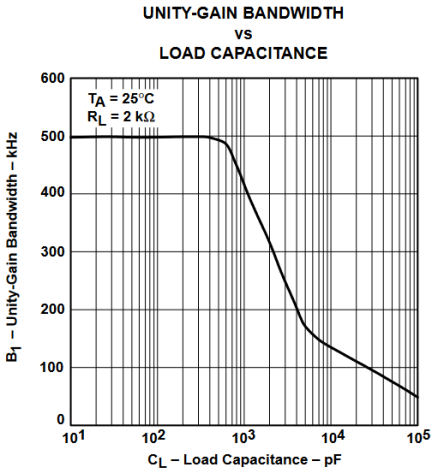


Figure 4-49.

5 Detailed Description

5.1 Overview

The other members of the TLV243x and TLV243xA family are the high-power TLV244xTLV244x, and micro-power TLV2422.

The TLV243x, exhibiting high input impedance and low noise, are excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. As a result of the micropower dissipation levels and low-voltage operation, these devices work well in portable monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single- or split-supplies makes this family a great choice when interfacing with analog-to-digital converters (ADCs). For precision applications, the TLV243xA are available and have a maximum input offset voltage of 950 µV.

If the design requires single operational amplifiers, see the TLV2211, TLV2221, and TLV2231. This family of rail-to-rail output operational amplifiers is available in the SOT-23 package. The small size and low power consumption make these devices an excellent choice for high-density, battery-powered equipment.

5.2 Functional Block Diagram

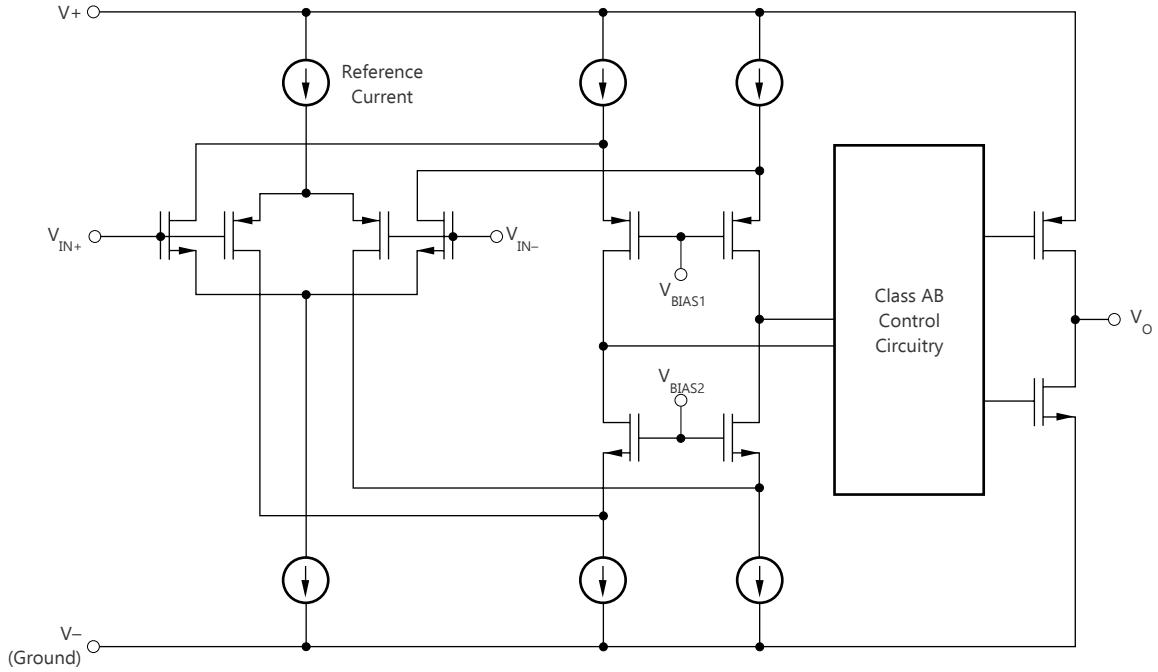


Figure 5-1. Equivalent Schematic (Each Amplifier)

6 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

6.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

6.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (Nov 1999) to Revision G (July 2025)	Page
• Deleted obsolete FK, JG, and U packages from data sheet	1
• Deleted obsolete M-suffix device from data sheet	1
• Updated *Features* to delete "Macromodel Included" and add link to automotive data sheet	1
• Deleted *Equivalent Schematic*	2
• Changed CMRR minimum value for all temperatures from 70 dB to 63 dB in all *Electrical Characteristics*	4
• Changed I_{DD} at T_A = 25°C TYP value from 98 µA to 115 µA, and MAX value from 125 µA to 150 µA	4
• Changed I_{DD} at T_A = Full range MAX value from 125 µA to 175 µA	4
• Changed I_{DD} at T_A = 25°C TYP value from 195 µA to 115 µA, and MAX value from 250 µA to 150 µA	6
• Changed I_{DD} at T_A = Full range from 260 µA to 175 µA	6
• Changed I_{DD} at T_A = 25°C TYP value from 100 µA to 115 µA, and MAX value from 125 µA to 150 µA	8
• Changed I_{DD} at T_A = Full range from 125 µA to 175 µA	8
• Changed I_{DD} at T_A = 25°C TYP value from 200 µA to 115 µA, and MAX value from 250 µA to 150 µA	10
• Changed I_{DD} at T_A = Full range from 270 µA to 175 µA	10
• Updated functional block diagram	21
• Deleted *Application Information* and *Macromodel Information* section	21

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV2432AID	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	2432AI
TLV2432AIDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2432AI
TLV2432AIDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2432AI
TLV2432AIPW	Obsolete	Production	TSSOP (PW) | 8	-	-	Call TI	Call TI	-40 to 85	TV2432
TLV2432AIPWR	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-1-260C-UNLIM	-40 to 85	2432AI
TLV2432AIPWR.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2432AI
TLV2432AQD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2432A
TLV2432AQD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2432A
TLV2432AQDG4	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2432A
TLV2432AQDG4.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2432A
TLV2432AQDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2432A
TLV2432AQDRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2432A
TLV2432CD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	2432C
TLV2432CDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	2432C
TLV2432CDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	2432C
TLV2432ID	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	2432I
TLV2432IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2432I
TLV2432IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2432I
TLV2432QD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2432Q
TLV2432QD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2432Q
TLV2434AID	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 85	2434AI
TLV2434AIDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2434AI
TLV2434AIDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2434AI
TLV2434AIPWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2434AI
TLV2434AIPWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2434AI
TLV2434CD	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	0 to 70	2434C
TLV2434CDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	2434C
TLV2434CDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	2434C
TLV2434CPW	Obsolete	Production	TSSOP (PW) | 14	-	-	Call TI	Call TI	0 to 70	2434C

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV2434CPWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	2434C
TLV2434CPWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	2434C
TLV2434ID	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 85	2434I
TLV2434IDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2434I
TLV2434IDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2434I
TLV2434IDRG4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2434I
TLV2434IDRG4.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2434I
TLV2434IPW	Obsolete	Production	TSSOP (PW) | 14	-	-	Call TI	Call TI	-40 to 85	2434I
TLV2434IPWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2434I
TLV2434IPWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2434I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV2432, TLV2432A, TLV2434A :

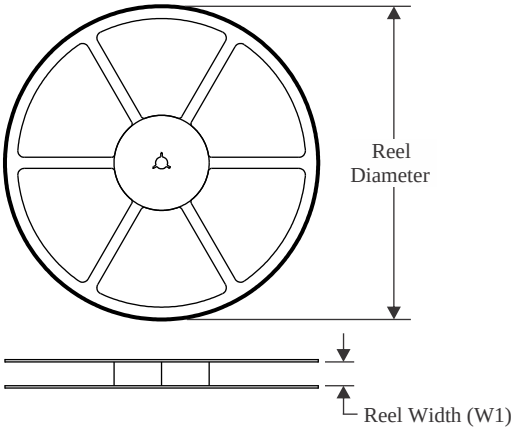
- Automotive : TLV2432-Q1, TLV2432A-Q1, TLV2434A-Q1

NOTE: Qualified Version Definitions:

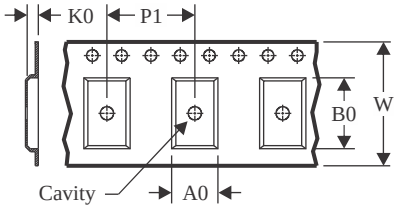
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

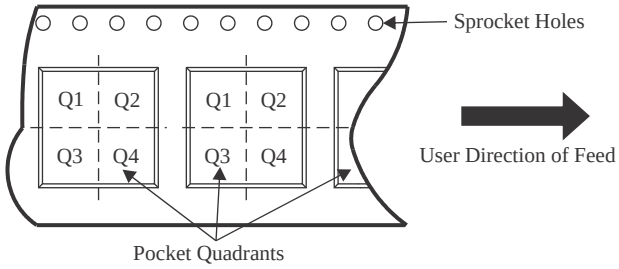


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

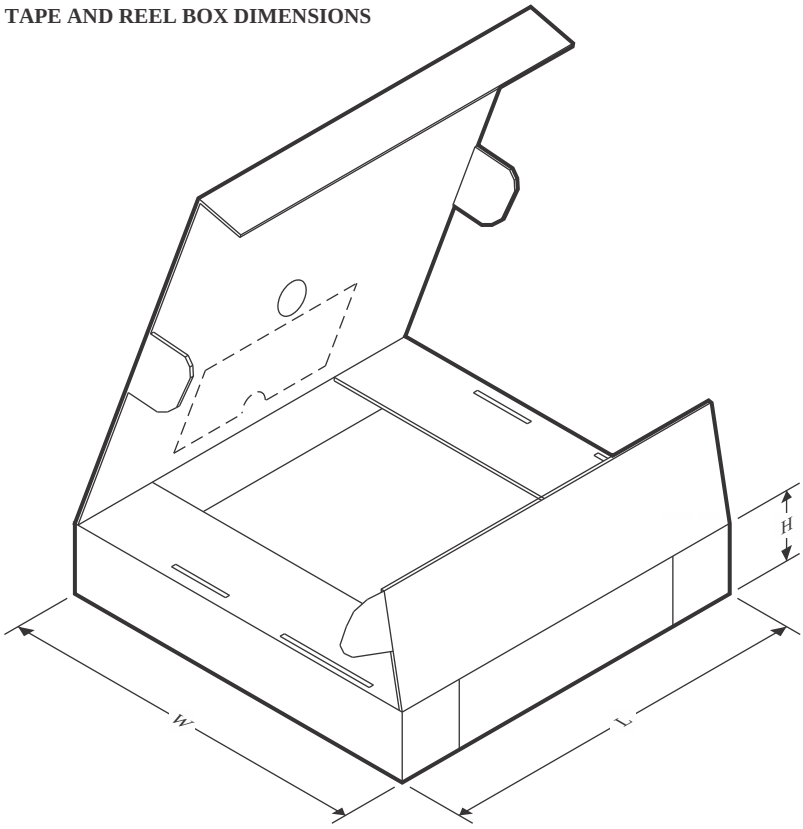
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2432AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2432AIPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV2432CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2432IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2434AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV2434AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV2434AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV2434CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV2434CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV2434CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV2434IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV2434IDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV2434IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV2434IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

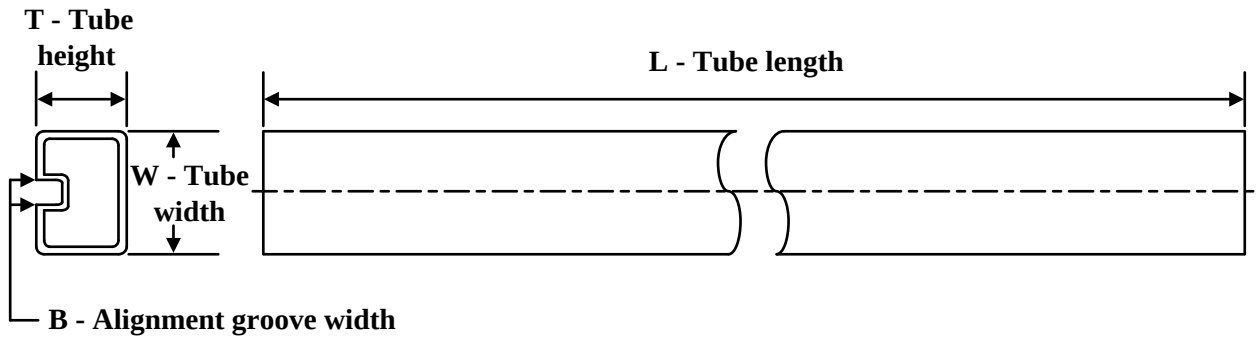
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

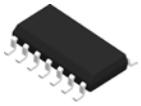
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2432AIDR	SOIC	D	8	2500	353.0	353.0	32.0
TLV2432AIPWR	TSSOP	PW	8	2000	353.0	353.0	32.0
TLV2432CDR	SOIC	D	8	2500	353.0	353.0	32.0
TLV2432IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2434AIDR	SOIC	D	14	2500	353.0	353.0	32.0
TLV2434AIPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
TLV2434AIPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
TLV2434CDR	SOIC	D	14	2500	353.0	353.0	32.0
TLV2434CPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
TLV2434CPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
TLV2434IDR	SOIC	D	14	2500	353.0	353.0	32.0
TLV2434IDRG4	SOIC	D	14	2500	353.0	353.0	32.0
TLV2434IPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
TLV2434IPWR	TSSOP	PW	14	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLV2432AQD	D	SOIC	8	75	507	8	3940	4.32
TLV2432AQD.A	D	SOIC	8	75	507	8	3940	4.32
TLV2432AQDG4	D	SOIC	8	75	507	8	3940	4.32
TLV2432AQDG4.A	D	SOIC	8	75	507	8	3940	4.32
TLV2432QD	D	SOIC	8	75	507	8	3940	4.32
TLV2432QD.A	D	SOIC	8	75	507	8	3940	4.32

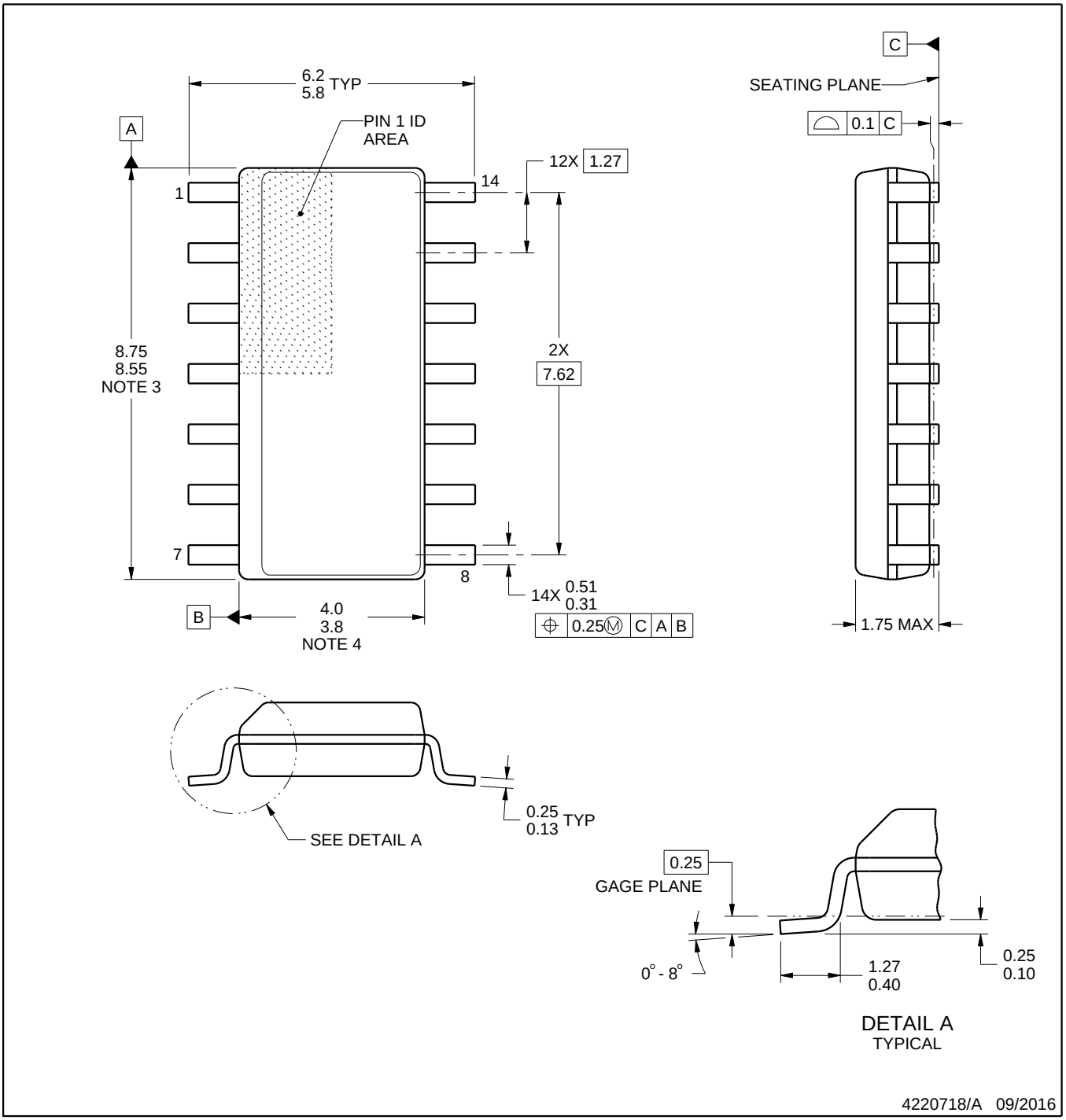


PACKAGE OUTLINE

D0014A

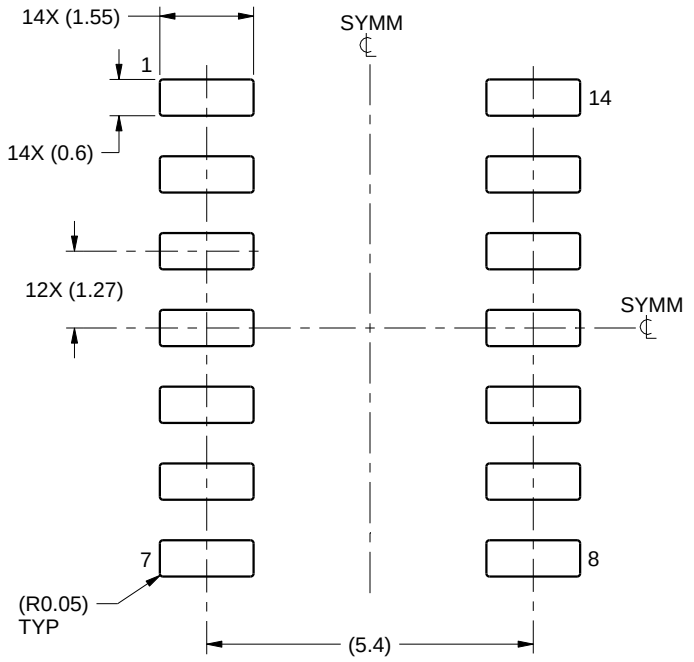
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

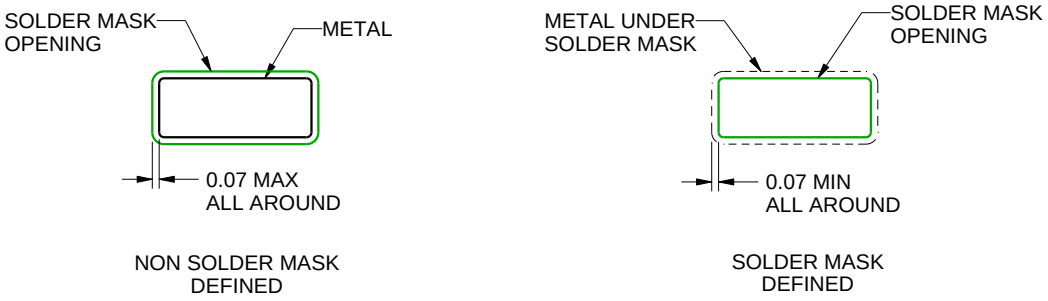


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

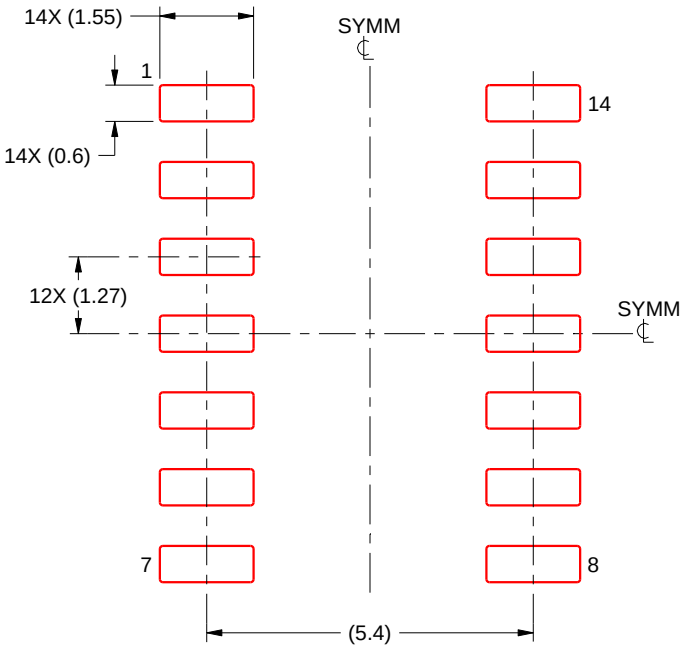
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

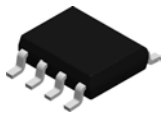


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

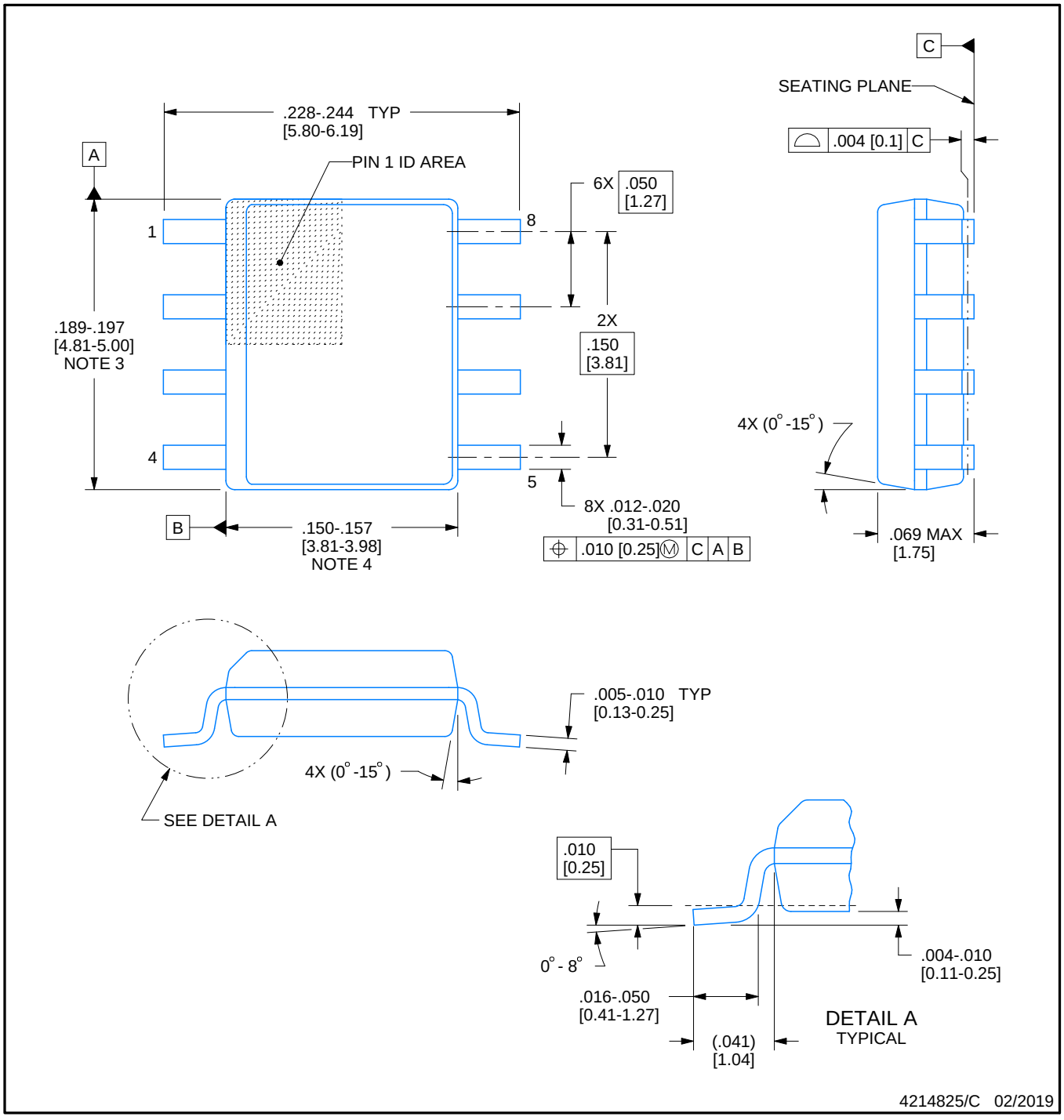


PACKAGE OUTLINE

D0008A

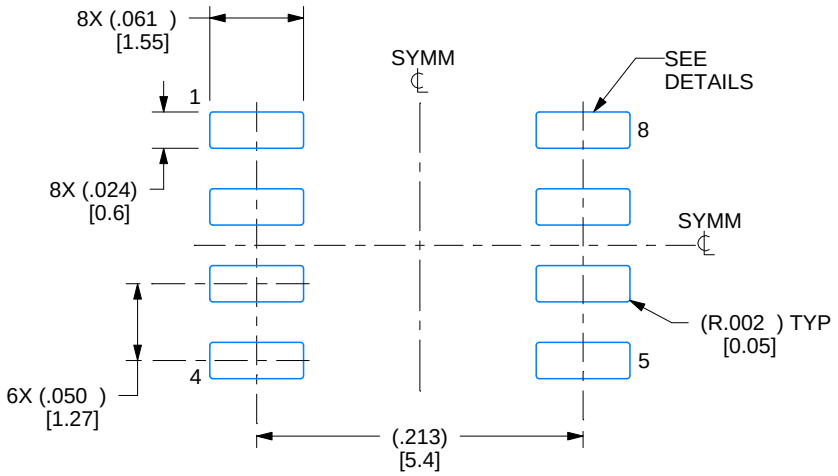
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

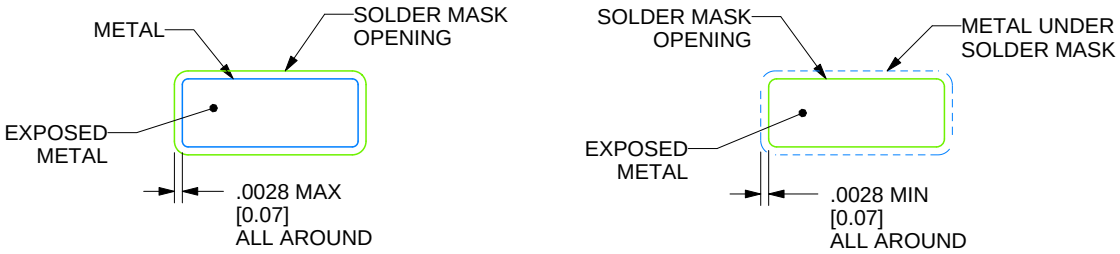


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

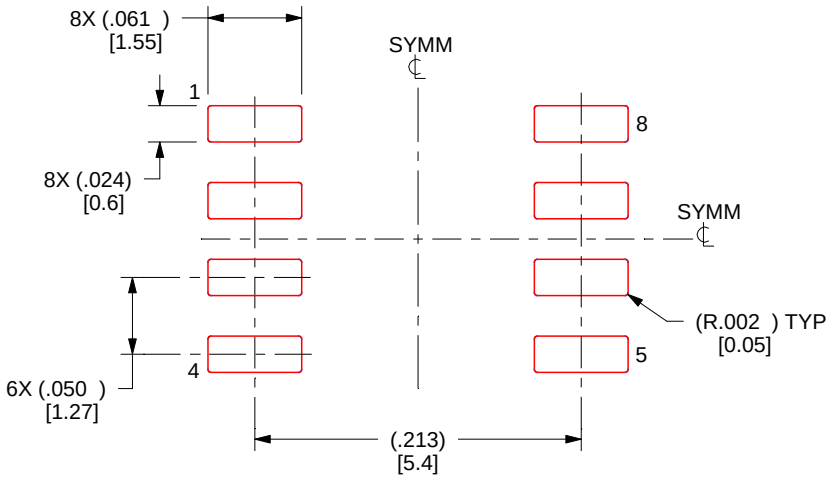
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

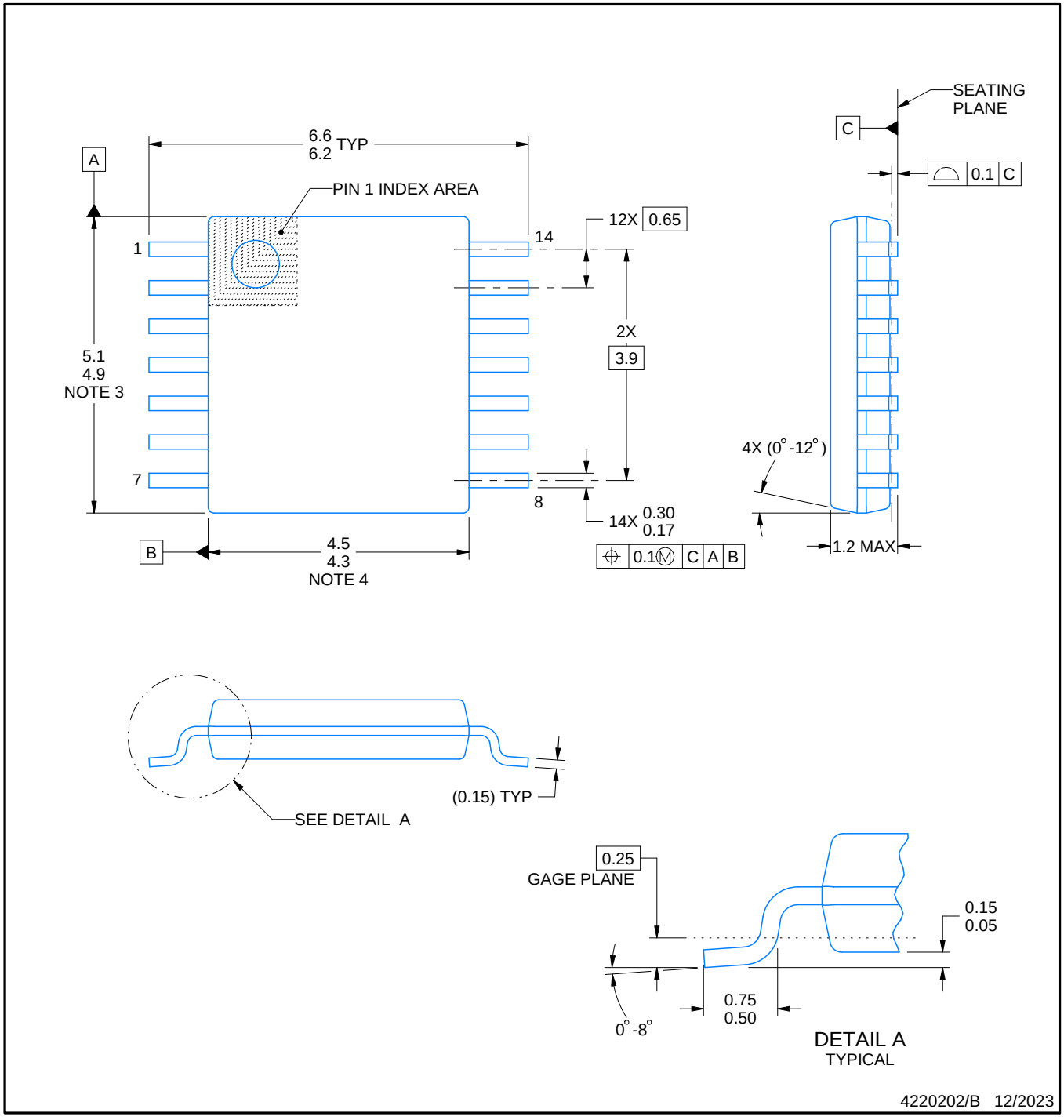
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

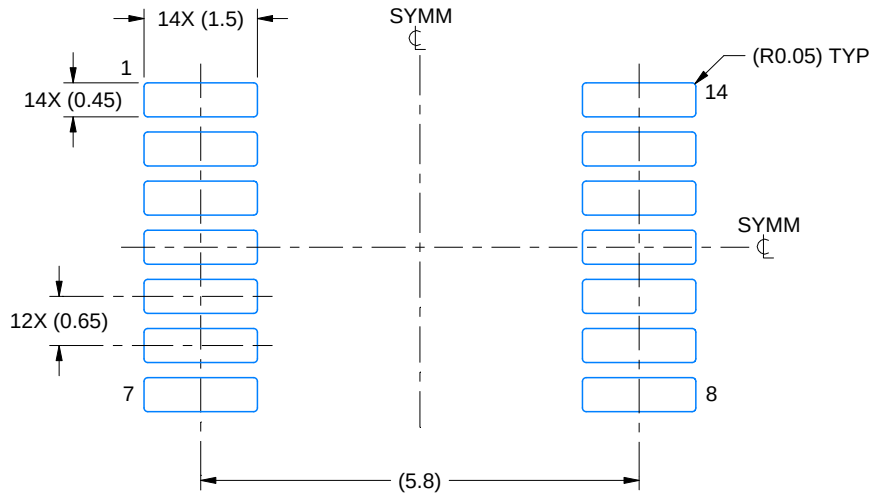
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

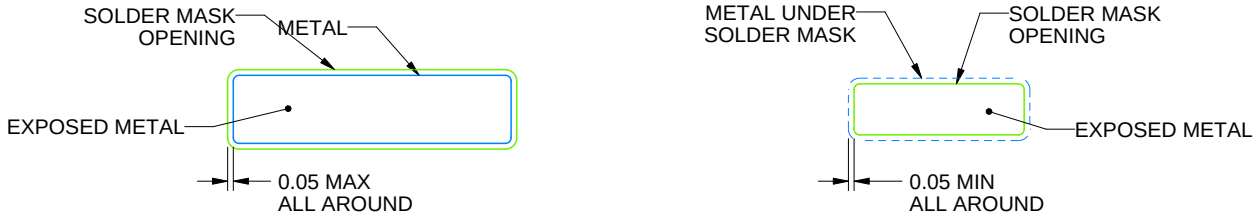


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

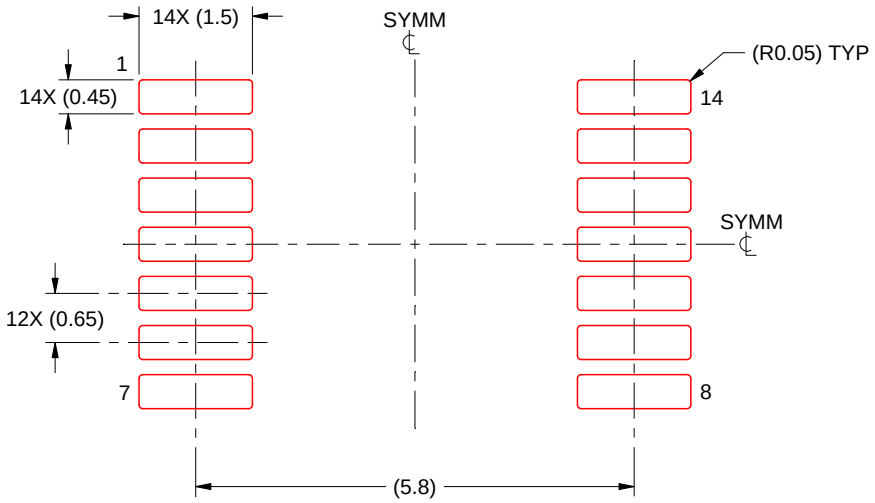


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

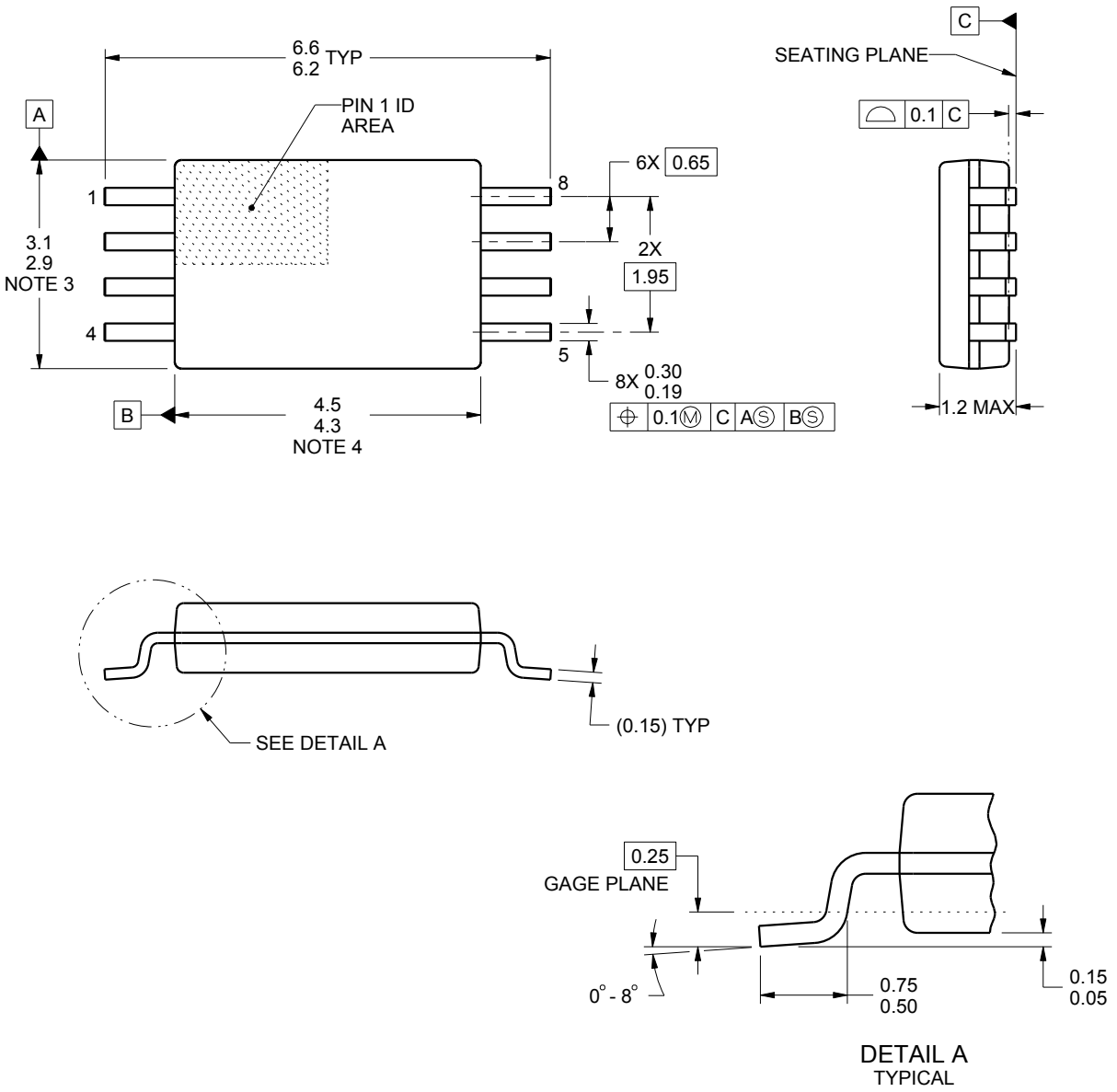
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0008A

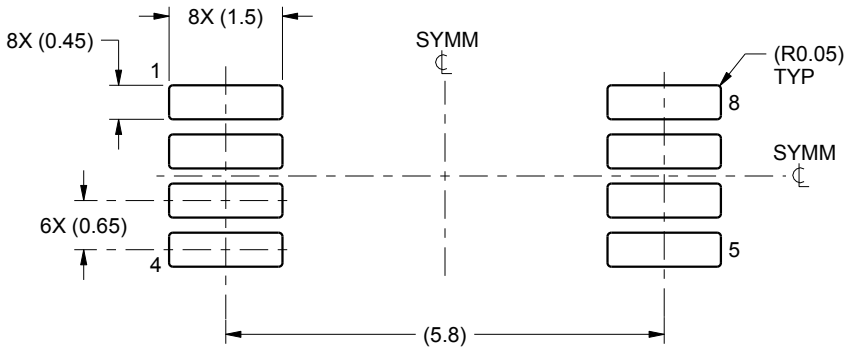
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

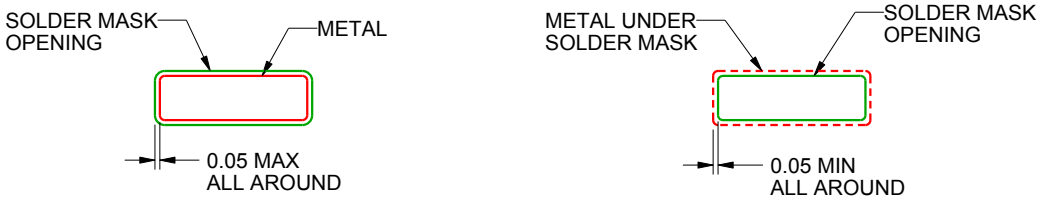


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

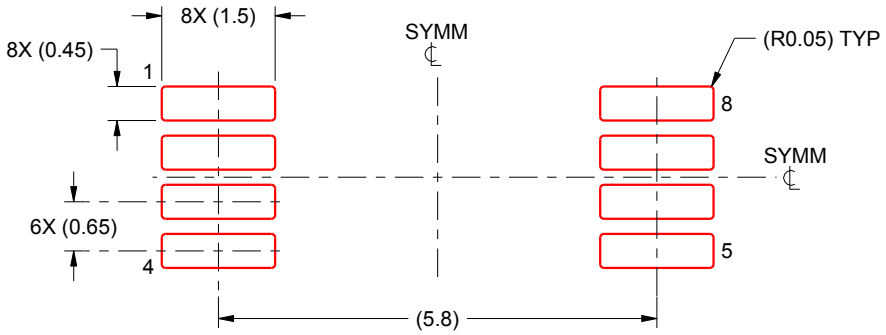


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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