TLV1H103-SEP 耐放射線特性、高速コンパレータ、伝搬遅延時間 2.5ns

1 特長

- VID V62/22606-01XE
- 放射線 - トータル ドーズ効果 (TID)
  - 30krad (Si) まで吸収線量 (TID) 特性を評価済み
  - 30krad (Si) まで ELDRS フリー
  - 30krad (Si) まで RHA/RLAT
- 放射線 - シングル イベント効果 (SEE)
  - SEL 耐性：LET = 43MeV·cm ^{2} /mg
  - SET 特性：LET = 43MeV·cm ^{2} /mg
- 宇宙向けに強化されたプラスチック
  - 管理されたベースライン
  - 単一のアセンブリ / テスト施設
  - 単一の製造施設
  - 長期にわたる製品ライフ サイクル
  - 製品のトレーサビリティ
- 小さい伝搬遅延：2.5ns
- 小さいオーバードライブ分散：700ps
- 高いトグル周波数：325MHz
- 狭パルス幅検出性能：1.5ns
- 両方のレールから 200mV 拡張された入力同相モード範囲
- 電源電圧範囲：2.4V～5.5V
- 可変ヒステリシス制御
- 出力ラッチ機能

2 アプリケーション

- 衛星用電源システム (EPS)
- レーダー画像処理ペイロード
- 通信ペイロード
- 飛行制御ユニット

3 概要

TLV1H103-SEP は、レール ツー レール入力、2.5ns の伝搬遅延時間、325MHz 動作の高速コンパレータです。本コンパレータは、速い応答と広い動作電圧範囲を備えており、レーダー画像処理および通信ペイロードシステムの狭信号パルス検出およびデータ / クロック リカバリ アプリケーションに最適です。

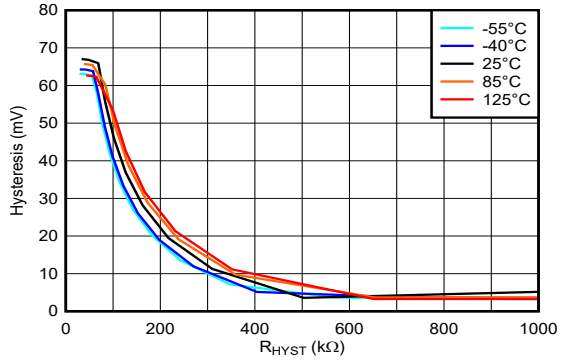
TLV1H103-SEP のプッシュプル (シングルエンド) 出力を使うと、他の高速差動出力コンパレータに比べて消費電力を低減できるとともに、I/O インターフェイスの基板間配線を簡素化し、コストを削減できます。さらに、TLV1H103-SEP は可変ヒステリシス制御や出力ラッチ機能などの機能を備えています。このコンパレータは、下流でよく使われるほとんどのデジタル コントローラおよび IO エクスパンダと直接接続できます。

TLV1H103-SEP は、高速相補型 BiCMOS プロセスを使用し、6 ピンの SOT-23 パッケージで供給されます。

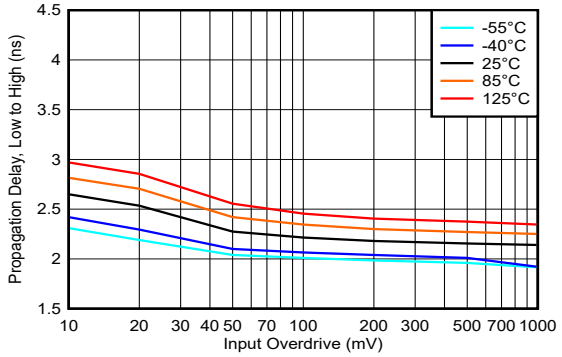
製品情報

部品番号	パッケージ (1)	本体サイズ (公称)(2)
TLV1H103-SEP	SOT-23 (6)	1.25 mm × 2.00mm

(1) 利用可能なすべてのパッケージについては、データの末尾にある追加の注文情報を参照してください
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



ヒステリシスと抵抗の関係、5V



伝搬遅延 (Low から High) と入力オーバードライブ、5V

Table of Contents

4 Pin Configuration and Functions

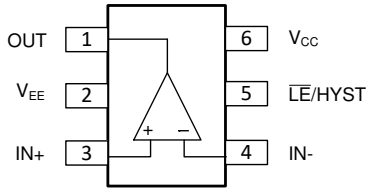


図 4-1. DBV Package
6-Pin SOT-23
Top View

表 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	TLV1H103		
IN+	3	I	Non-inverting input
IN–	4	I	Inverting input
OUT	1	O	Output (Push-pull)
V_{EE}	2	I	Negative power supply
V_{CC}	6	I	Positive power supply
$\overline{LE}$/HYS	5	I	Adjustable hysteresis control and latch

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Input Supply Voltage: V_{CC} – V_{EE}	–0.3	6	V
Input Voltage (IN+, IN–)(2)	V_{EE} – 0.3	V_{CC} + 0.3	V
Differential Input Voltage (V_{DI} = IN+ – IN–)	–(V_{CC} – V_{EE} + 0.3)	+ (V_{CC} –V_{EE} + 0.3)	V
Output Voltage (OUT)(3)	V_{EE} – 0.3	V_{CC} + 0.3	V
Latch and Hysteresis Control ($\overline{LE}$/HYS)	V_{EE} – 0.3	V_{CC} + 0.3	V
Current into Input pins (IN+, IN–, $\overline{LE}$/HYS)(2)		±10	mA
Current into Output pins (OUT)(3)		±50	mA
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings can cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3V beyond the supply rails must be current-limited to 10mA or less.
(3) Output terminals are diode-clamped to the power-supply rails. Output signals that can swing more than 0.3V beyond the supply rails must be current-limited to 50mA or less.

5.2 ESD Ratings

			VALUE	UNIT
TLV1H103				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
$V_{(ESD)}$	Electrostatic discharge	Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Input Supply Voltage: V_{CC} – V_{EE}	2.4	5.5	V
Input Voltage Range (IN+, IN–)	V_{EE} – 0.3	V_{CC} + 0.3	V
Latch and Hysteresis Control ($\overline{LE}$/HYS)	V_{EE} – 0.3	V_{CC} + 0.3	V
Ambient temperature, T_A	–55	125	°C

5.4 Thermal Information

THERMAL METRIC(1)		TLV1H103 DBV (SOT-23) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	191.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	117.1	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case (bottom) thermal resistance	79.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	78.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics report.

5.5 Electrical Characteristics

V_{CC} = 2.5, 3.3 and 5V, V_{EE} = 0V, V_{CM} = V_{EE} + 300mV, C_L = 5pF probe capacitance, typical at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC Input Characteristics						
V_{IO}	Input offset voltage	T_A = –55°C to +125°C	-7	±0.5	7	mV
dV_{IO}/dT	Input offset voltage drift			±3.0		µV/°C
V_{CM}	Input common mode voltage range	T_A = –55°C to +125°C	V_{EE} – 0.2		V_{CC} + 0.2	V
C_{IN}	Input capacitance			1		pF
R_{DM}	Input differential mode resistance			67		kΩ
R_{CM}	Input common mode resistance			5		MΩ
I_B	Input bias current	T_A = –55°C to +125°C		1	5	uA
I_{OS}	Input offset current			±0.03		uA
CMRR	Common-mode rejection ratio	V_{CM} = V_{EE} – 0.2V to V_{CC} + 0.2V		80		dB
PSRR	Power-supply rejection ratio	V_{CC} = 2.4 to 5.5V		80		dB
DC Output Characteristics						
V_{OH}	Output high voltage from V_{CC}	I_{SOURCE} = 1mA T_A = –55°C to +125°C		60	80	mV
V_{OL}	Output low voltage from V_{EE}	I_{SINK} = 1mA T_A = –55°C to +125°C		60	80	mV
I_{SC_SOURCE}	Output Short-Circuit Current - Source	T_A = –55°C to +125°C	10	30		mA
I_{SC_SINK}	Output Short-Circuit Current - Sink	T_A = –55°C to +125°C	10	30		mA
Power Supply						
I_{CC}	quiescent current	Output being high T_A = –55°C to +125°C		5.7	7.8	mA
$V_{POR\ (postive)}$	Power-On Reset Voltage			2.1		V
AC Characteristics						
t_{PD}	Propagation delay	$V_{OVERDRIVE}$ = $V_{UNDERDRIVE}$ = 50mV T_A = –55°C to +125°C		2.5	4.5(1)	ns
$t_{CM\_DISPERSION}$	Common dispersion	V_{CM} varied from V_{EE} to V_{CC}		80		ps
$t_{OD\_DISPERSION}$	Overdrive dispersion	Overdrive varied from 10mV to 125mV		700		ps
$t_{UD\_DISPERSION}$	Underdrive dispersion	Underdrive varied from 10mV to 125mV		330		ps
t_R	Rise time	10% to 90%		0.75		ns
t_F	Fall time	90% to 10%		0.75		ns
t_{JITTER}	RMS Jitter	V_{IN} = 100mV_{P-P}, f_{IN} = 100MHz, Jitter BW = 10Hz – 50MHz		4		ps
f_{TOGGLE}	Input toggle frequency	V_{IN} = 200mV_{PP} Sine Wave, When output high reaches 90% of V_{CC} - V_{EE} or output low reaches 10% of V_{CC} - V_{EE}		325		MHz
PulseWidth	Minimum allowed input pulse width	$V_{OVERDRIVE}$ = $V_{UNDERDRIVE}$ = 50mV PW_{OUT} = 90% of PW_{IN}		1.5		ns

5.5 Electrical Characteristics (続き)

V_{CC} = 2.5, 3.3 and 5V, V_{EE} = 0V, V_{CM} = V_{EE} + 300mV, C_L = 5pF probe capacitance, typical at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Latching/Adjustable Hysteresis						
V_{HYST}	Input hysteresis voltage	V_{HYST} = Logic High		0		mV
V_{HYST}	Input hysteresis voltage	R_{HYST} = Floating		3		mV
V_{HYST}	Input hysteresis voltage	R_{HYST} = 150kΩ		30		mV
V_{HYST}	Input hysteresis voltage	R_{HYST} = 56kΩ		60		mV
V_{IH_LE}	$\overline{LE}$ pin input high level	T_A = –55℃ to +125℃	V_{EE} + 1.5			V
V_{IL_LE}	$\overline{LE}$ pin input low level	T_A = –55℃ to +125℃			V_{EE} + 0.35	V
I_{IH_LE}	$\overline{LE}$ pin input leakage current	V_{LE} = V_{CC} T_A = –55℃ to +125℃			15	uA
I_{IL_LE}	$\overline{LE}$ pin input leakage current	V_{LE} = V_{EE}, T_A = –55℃ to +125℃			40	uA
t_{SETUP}	Latch setup time			–1.4		ns
t_{HOLD}	Latch hold time			7.2		ns
t_{PL}	Latch to OUT delay			7		ns

(1) Assured by characterization

5.6 Timing Diagrams

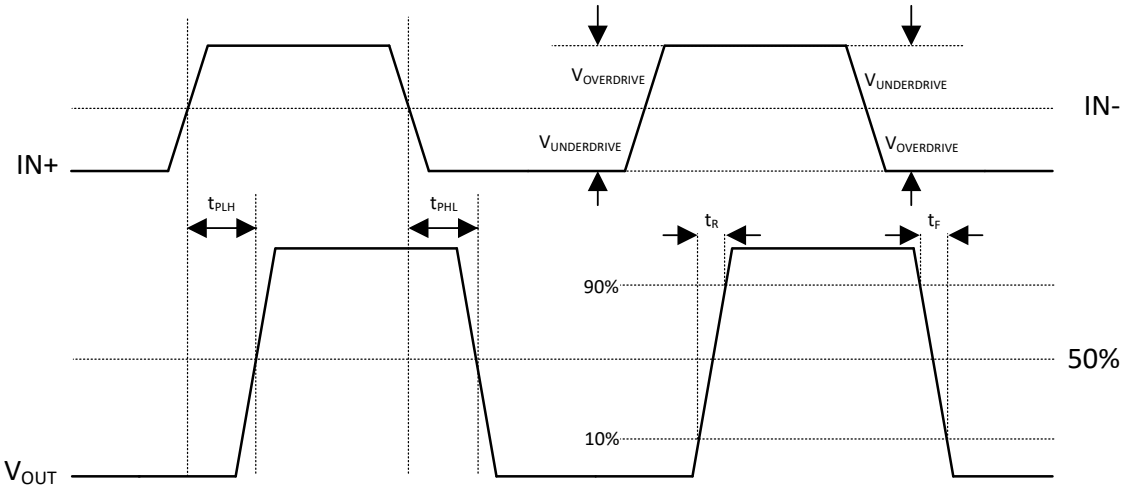


図 5-1. General Timing Diagram

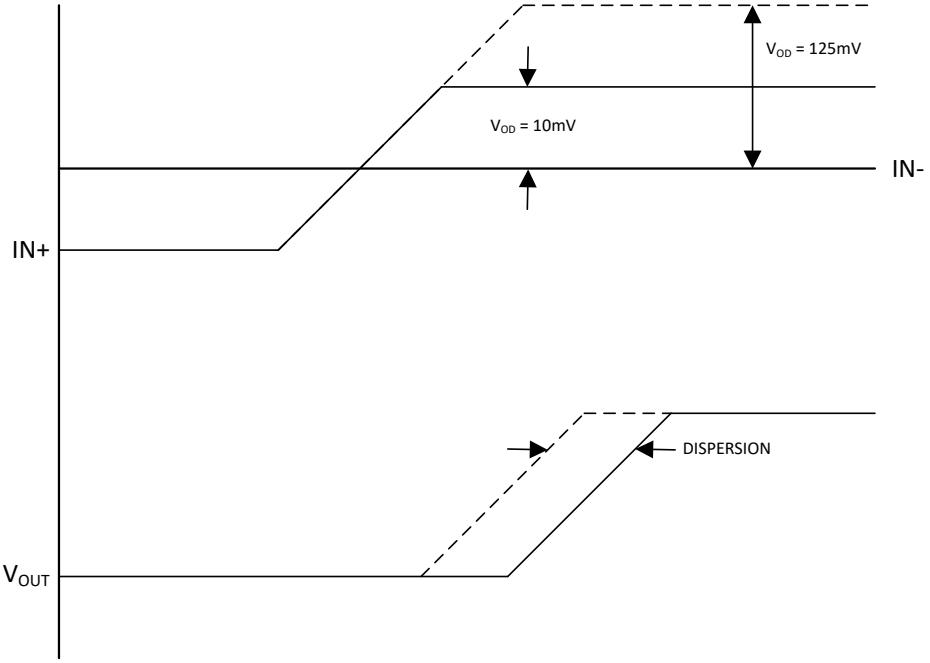


図 5-2. Overdrive Dispersion

5.7 Typical Characteristics

At T_A = 25°C, V_{CC} - V_{EE} = 2.5V to 5V, V_{CM} = 300mV, R_{HYST} = 150kΩ, and input overdrive = 50mV, unless otherwise noted.

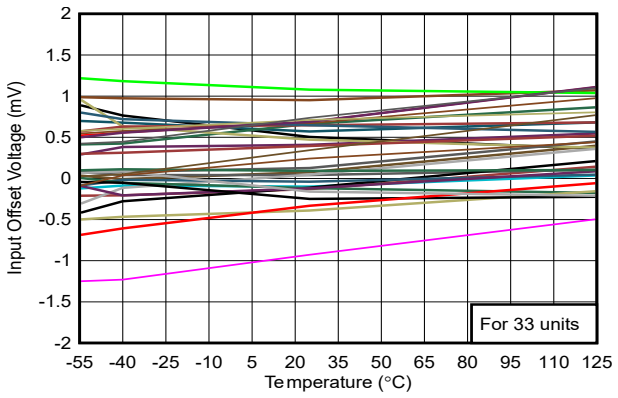


図 5-3. Offset vs. Temperature

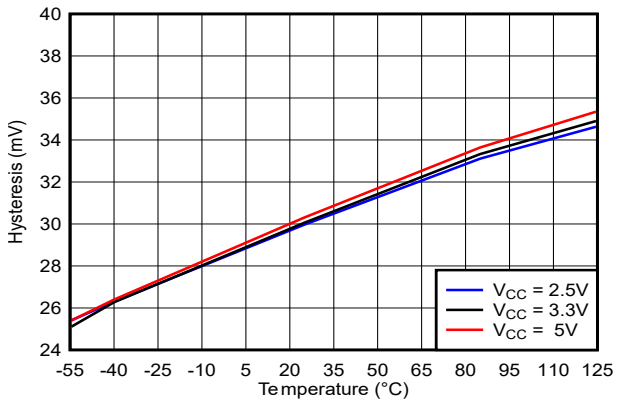


図 5-4. Hysteresis vs. Temperature

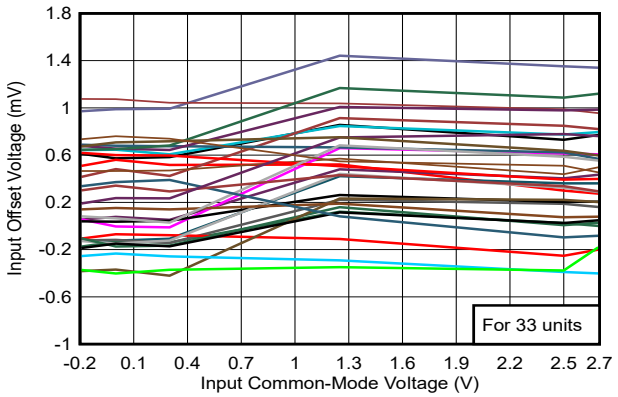


図 5-5. Offset vs. Common-Mode, 2.5V

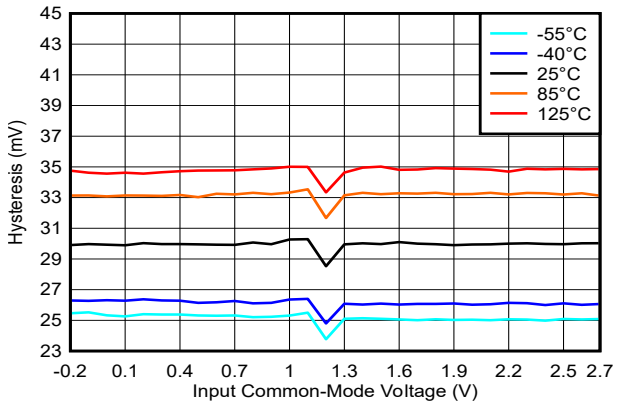


図 5-6. Hysteresis vs. Common-Mode, 2.5V

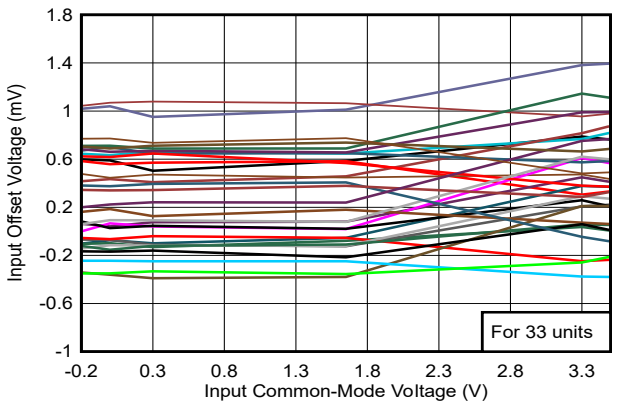


図 5-7. Offset vs. Common-Mode, 3.3V

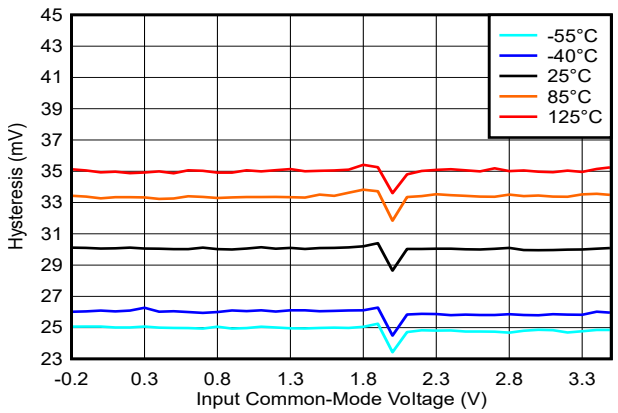


図 5-8. Hysteresis vs. Common-Mode, 3.3V

5.7 Typical Characteristics (continued)

At T_A = 25°C, V_{CC} - V_{EE} = 2.5V to 5V, V_{CM} = 300mV, R_{HYST} = 150kΩ, and input overdrive = 50mV, unless otherwise noted.

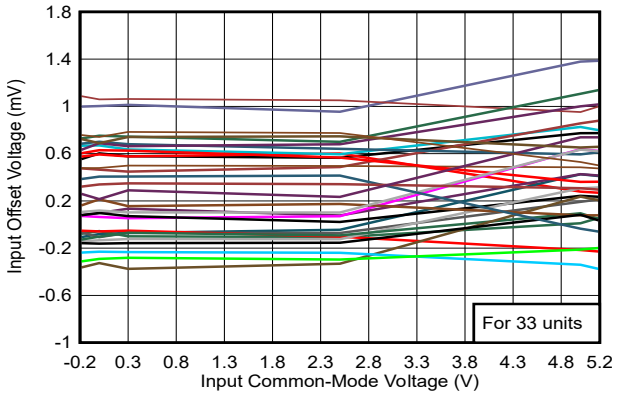


図 5-9. Offset vs. Common-Mode, 5V

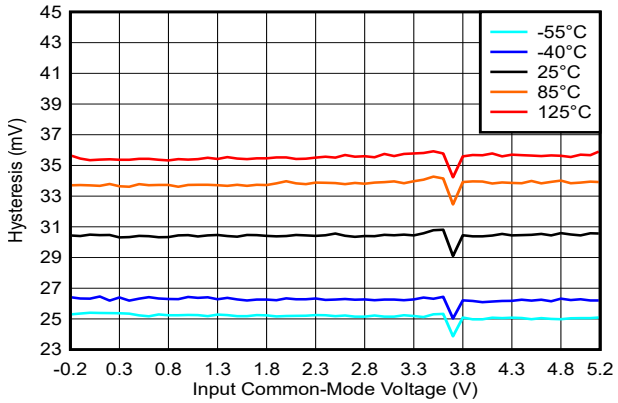


図 5-10. Hysteresis vs. Common-Mode, 5V

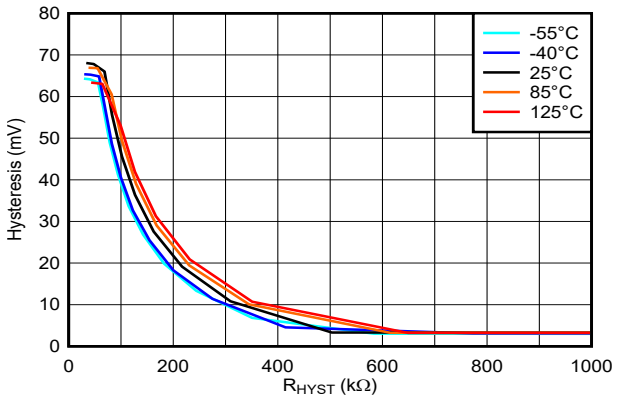


図 5-11. Hysteresis vs. Resistance, 2.5V

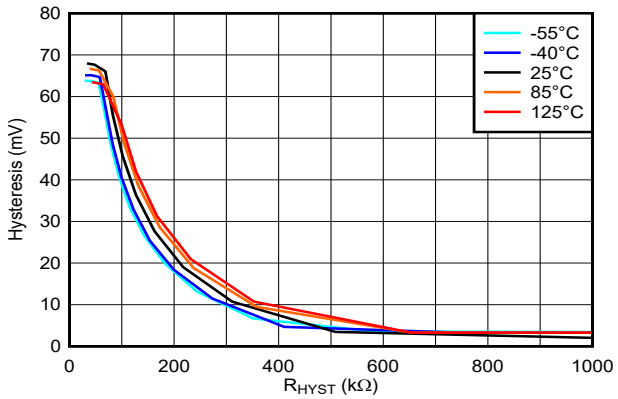


図 5-12. Hysteresis vs. Resistance, 3.3V

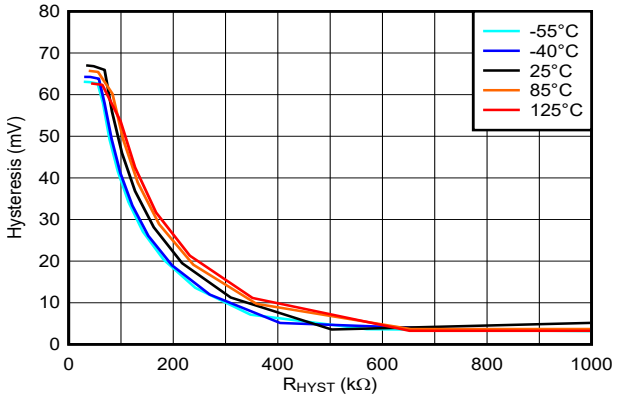


図 5-13. Hysteresis vs. Resistance, 5V

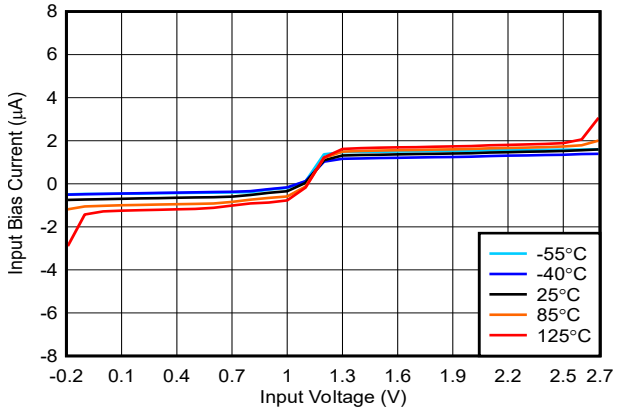


図 5-14. Bias Current vs. Input Voltage, 2.5V

5.7 Typical Characteristics (continued)

At T_A = 25°C, V_{CC} - V_{EE} = 2.5V to 5V, V_{CM} = 300mV, R_{HYST} = 150kΩ, and input overdrive = 50mV, unless otherwise noted.

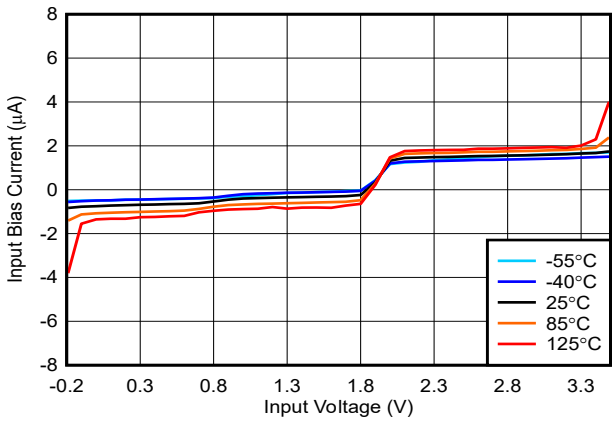


図 5-15. Bias Current vs. Input Voltage, 3.3V

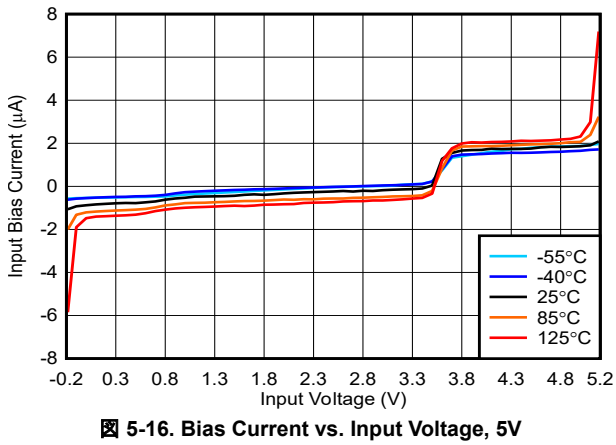


図 5-16. Bias Current vs. Input Voltage, 5V

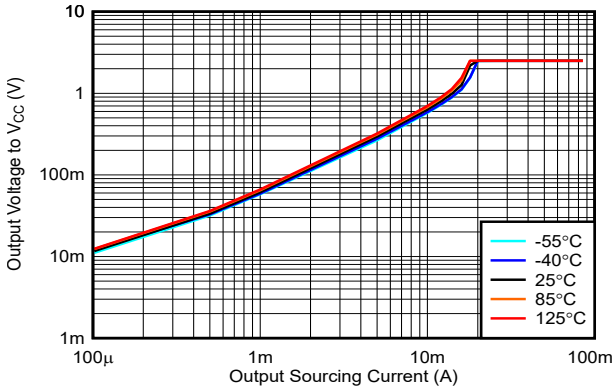


図 5-17. Output Voltage vs. Output Sourcing Current, 2.5V

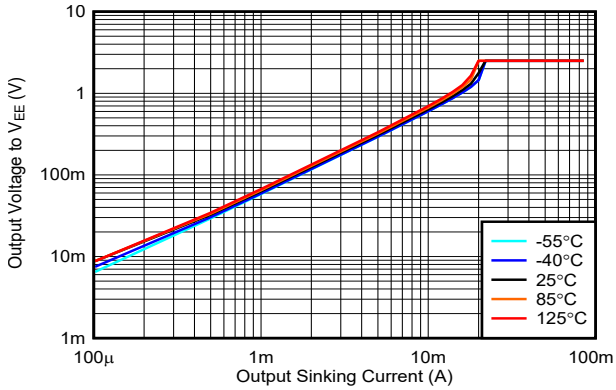


図 5-18. Output Voltage vs. Output Sinking Current, 2.5V

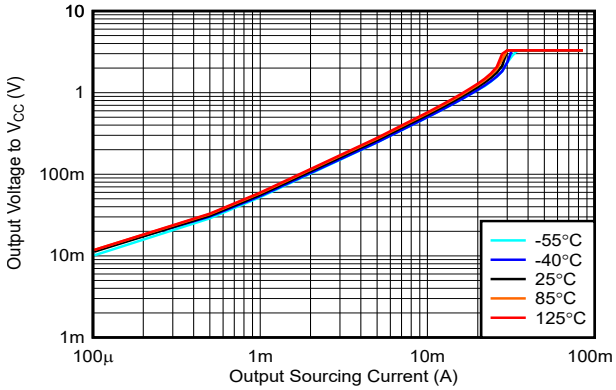


図 5-19. Output Voltage vs. Output Sourcing Current, 3.3V

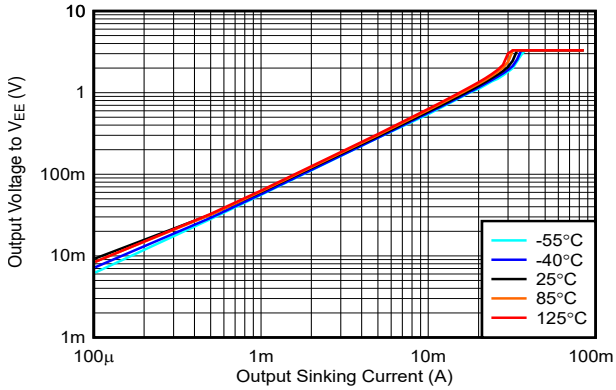


図 5-20. Output Voltage vs. Output Sinking Current, 3.3V

5.7 Typical Characteristics (continued)

At T_A = 25°C, V_{CC} - V_{EE} = 2.5V to 5V, V_{CM} = 300mV, R_{HYST} = 150kΩ, and input overdrive = 50mV, unless otherwise noted.

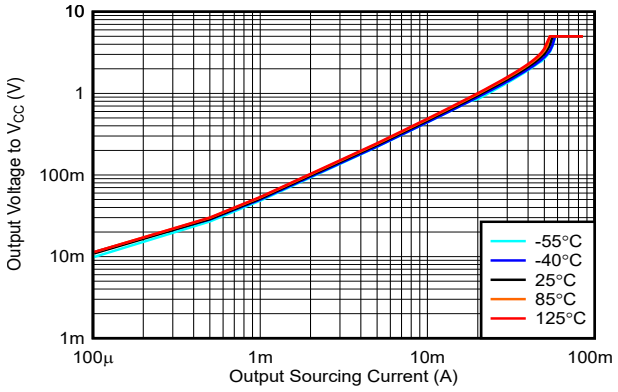


図 5-21. Output Voltage vs. Output Sourcing Current, 5V

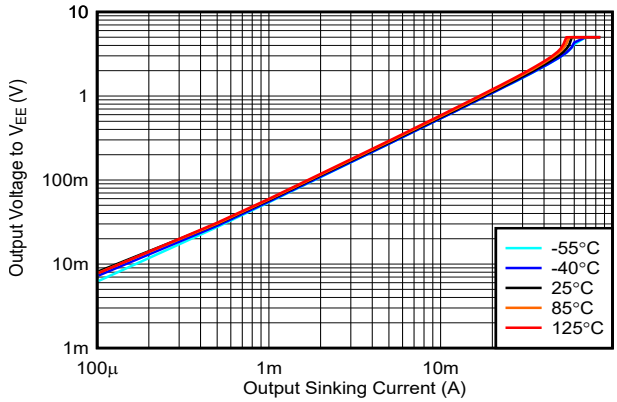


図 5-22. Output Voltage vs. Output Sinking Current, 5V

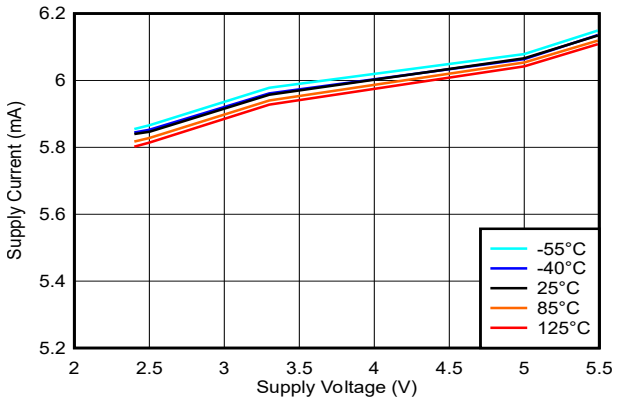


図 5-23. Supply Current vs. Voltage (Output Low)

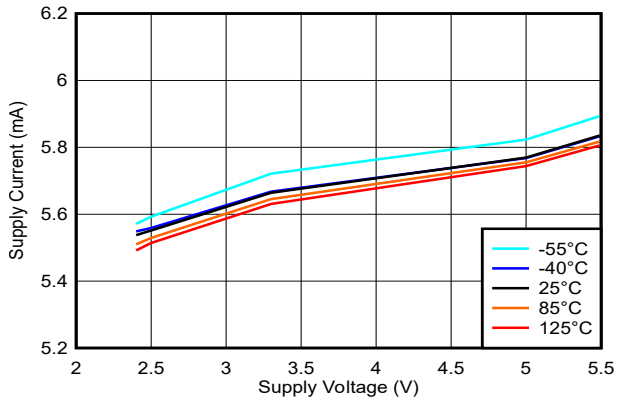


図 5-24. Supply Current vs. Voltage (Output High)

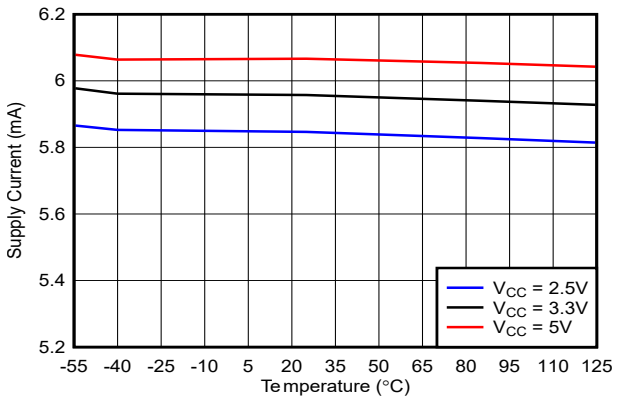


図 5-25. Supply Current vs. Temp (Output Low)

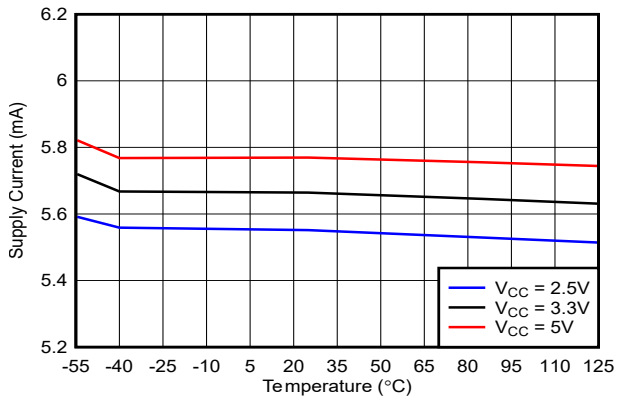


図 5-26. Supply Current vs. Temp (Output High)

5.7 Typical Characteristics (continued)

At T_A = 25°C, V_{CC} - V_{EE} = 2.5V to 5V, V_{CM} = 300mV, R_{HYST} = 150kΩ, and input overdrive = 50mV, unless otherwise noted.

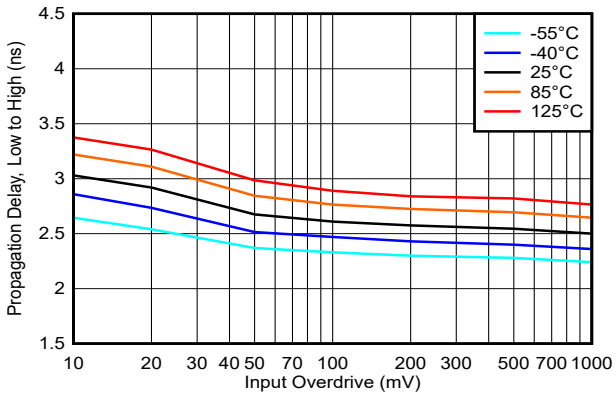


図 5-27. Propagation Delay, Low to High, 2.5V

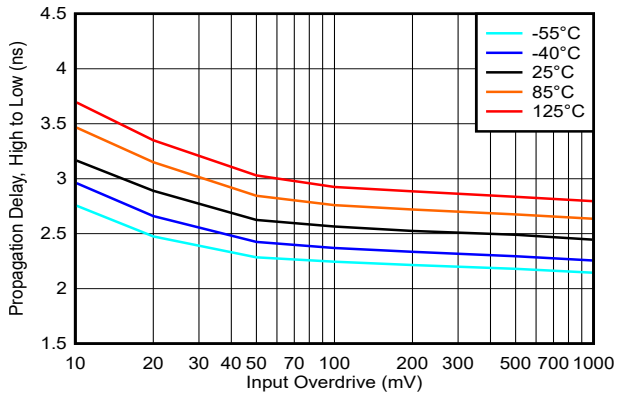


図 5-28. Propagation Delay, High to Low, 2.5V

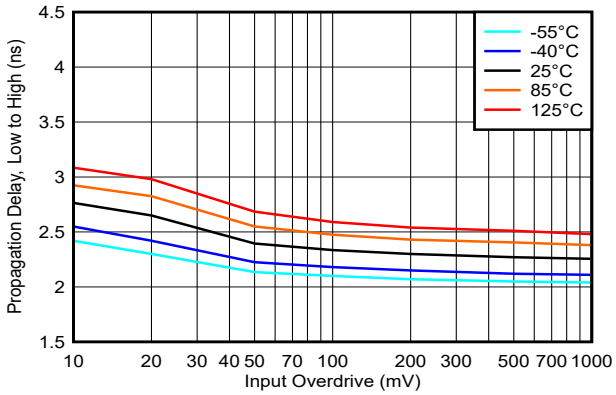


図 5-29. Propagation Delay, Low to High, 3.3V

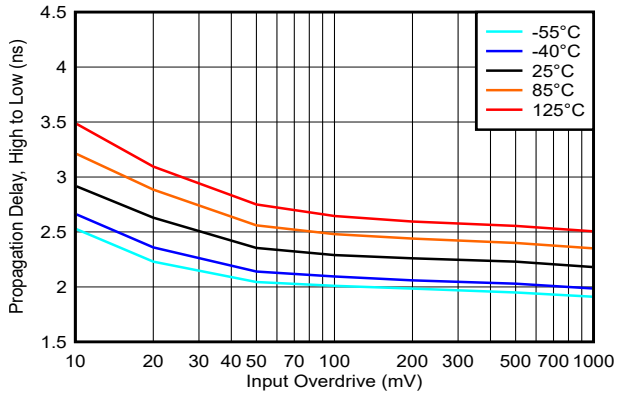


図 5-30. Propagation Delay, High to Low, 3.3V

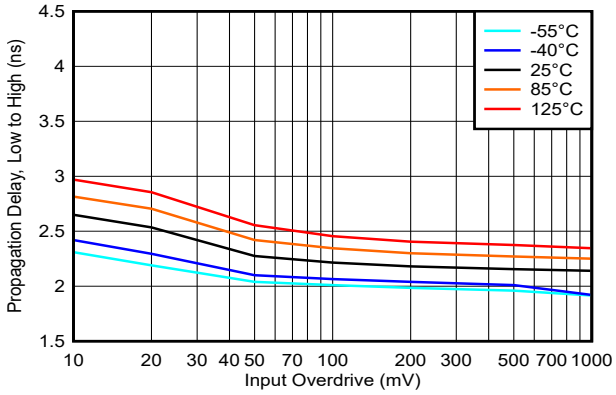


図 5-31. Propagation Delay, Low to High, 5V

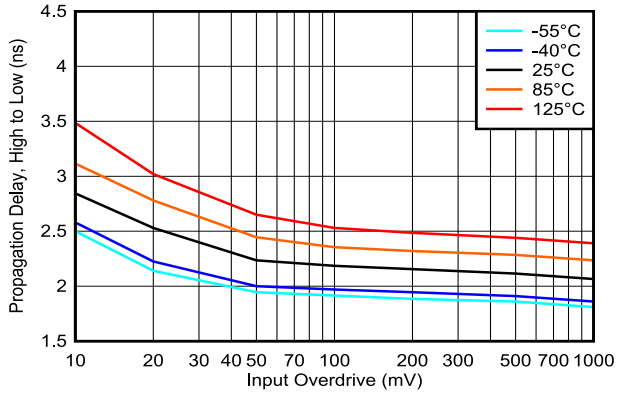


図 5-32. Propagation Delay, High to Low, 5V

5.7 Typical Characteristics (continued)

At T_A = 25°C, V_{CC} - V_{EE} = 2.5V to 5V, V_{CM} = 300mV, R_{HYST} = 150kΩ, and input overdrive = 50mV, unless otherwise noted.

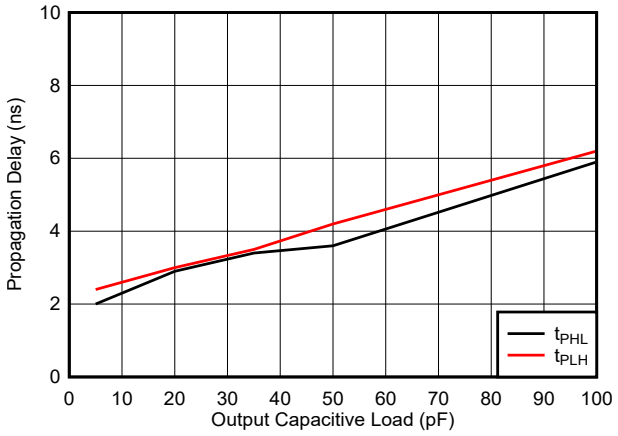


図 5-33. Propagation Delay vs. Load Capacitance, 3.3V

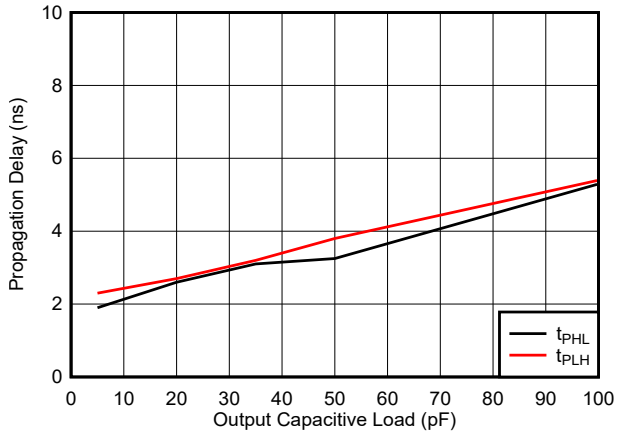


図 5-34. Propagation Delay vs. Load Capacitance, 5V

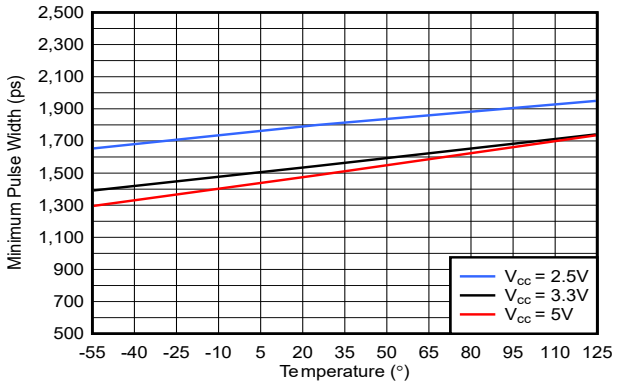


図 5-35. Minimum Pulse Width vs. Temperature

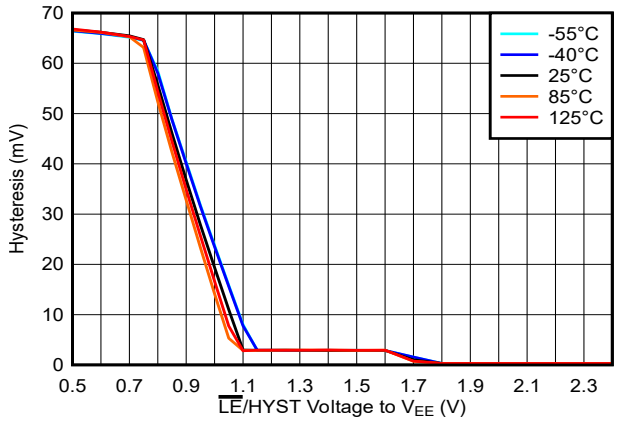


図 5-36. Hysteresis Voltage vs. LE/HYST Voltage, 2.5V

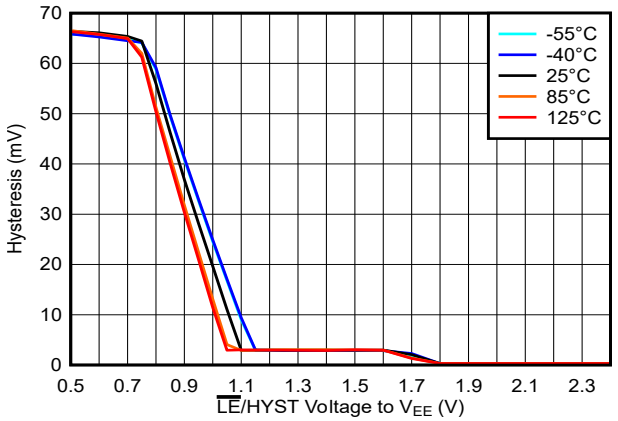


図 5-37. Hysteresis Voltage vs. LE/HYST Voltage, 3.3V

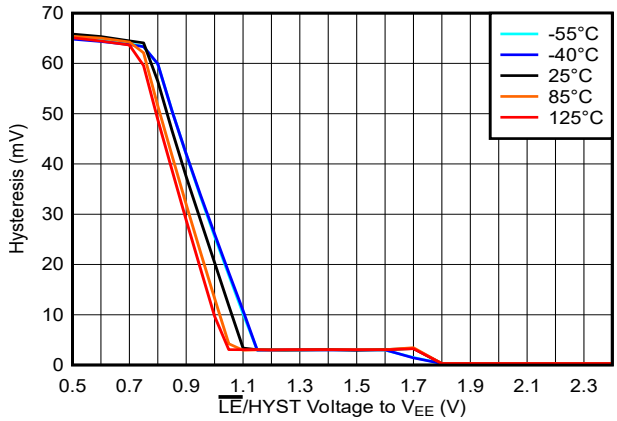


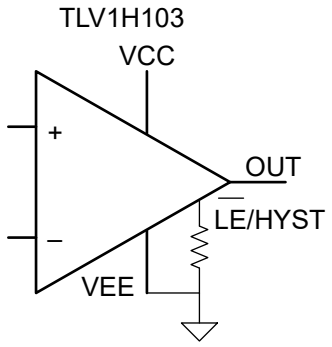
図 5-38. Hysteresis Voltage vs. LE/HYST Voltage, 5V

6 Detailed Description

6.1 Overview

The TLV1H103-SEP is a high-speed comparator with single-ended (push-pull) output stage. The fast response time of this comparator is well suited for applications that require narrow pulse width detection or high toggle frequencies. The TLV1H103-SEP is available in a 6-pin SOT-23 package.

6.2 Functional Block Diagram



6.3 Feature Description

The TLV1H103-SEP is a single channel, high speed comparator with a typical propagation delay of 2.5ns and a push-pull output. The minimum pulse width detection capability is 1.5ns and the typical toggle rate is 325MHz. This comparator is well-suited for distance measurement applications that utilize a time-of-flight architecture as well as systems that suffer from capacitive loading and require data and clock recovery. In addition to high speed, the TLV1H103-SEP offers a rail-to-rail input stage capable of operating up to 300mV beyond each power supply rail combined with a maximum 7mV input offset. The TLV1H103-SEP also provides adjustable hysteresis via an external resistor for noise supression or a latching mode to hold the output of the comparators.

6.4 Device Functional Modes

The TLV1H103-SEP has two modes of operation. The first is an active mode where the output reflects the condition at the inputs when an external resistor is connected to ground on the $\overline{LE}$/HYS pin. The resistor value creates a specified amount of internal hysteresis for the comparator without requiring external, positive feedback. The second is a latch mode where the output is held at the last active state when the $\overline{LE}$/HYS pin is pulled low. The TLV1H103-SEP returns to active mode after a short delay when the pin is pulled high.

6.4.1 Inputs

The TLV1H103-SEP features an input stage capable of operating 300mV below negative power supply (ground) and 300mV beyond the positive supply voltage, allowing for zero cross detection and maximizing input dynamic range given a certain power supply. The input stages are protected from conditions where the voltage on either pin exceeds this level by internal ESD protection diodes to VCC and VEE. An external resistor must be used to limit the current to less than 10mA to avoid damaging the inputs when exceeding the recommended input voltage range.

6.4.2 Push-Pull (Single-Ended) Output

The TLV1H103-SEP output has excellent drive capability and is designed to connect directly to CMOS logic input devices. Likewise, the comparator output stage is capable of driving capacitive loads. Transient performance parameters in the Electrical Characteristics Tables and Typical Characteristics section are for a load of 5pF, corresponding to a standard CMOS load. Device performance for larger capacitive loads can be found in the typical performance curves titled Propagation Delay vs Load Capacitance. For maximum speed and performance, output load capacitance must be minimized.

6.4.3 Known Startup Condition

The TLV1H103-SEP have a Power-on-Reset (POR) circuit which provides system designers a known start-up condition for the output of the comparators. When the power supply (VCC) is ramping up or ramping down, the POR circuit is active when VCC is below V_{POR}. When active, the POR circuit holds the output low at VEE. When VCC is greater than or equal to V_{POR} as stated in Electrical Characteristics , the comparator output reflects the state of the input pins.

図 6-1 shows how the TLV1H103-SEP output respond for VCC rising. The input is configured with a logic high input to highlight the transition from the POR circuit control (logic low output) to a standard comparator operation where the output reflects the input condition. Note how the output goes high when VCC reaches 2.1V.

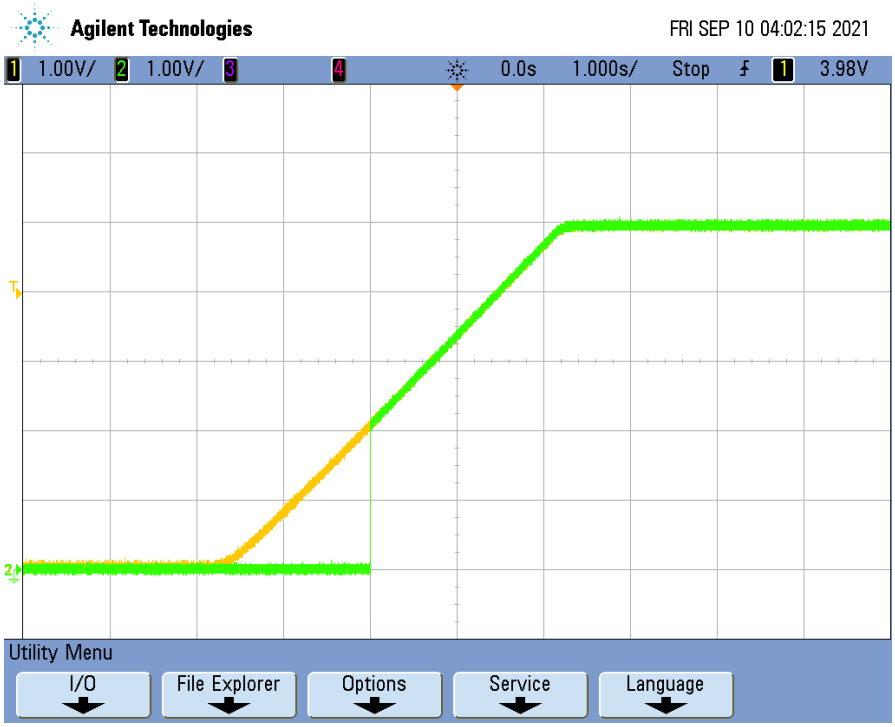


図 6-1. TLV1H103-SEP Output for VCC Rising

7 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant the accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing end equipment design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Adjustable Hysteresis

As a result of a comparator's high open loop gain, there is a small band of input differential voltage where the output can toggle back and forth between "logic high" and "logic low" states. This can cause design challenges for inputs with slow rise and fall times or systems with excessive noise. These challenges can be overcome by adding hysteresis to the comparator.

The TLV1H103-SEP has a $\overline{LE}$/HYS pin that can be used to increase the internal hysteresis of the comparator. To change the internal hysteresis of the comparator, connect a single resistor as shown in the adjusting hysteresis figure between the $\overline{LE}$/HYS pin and VEE. A curve of hysteresis versus resistance is provided below to provide guidance in setting the desired amount of hysteresis.

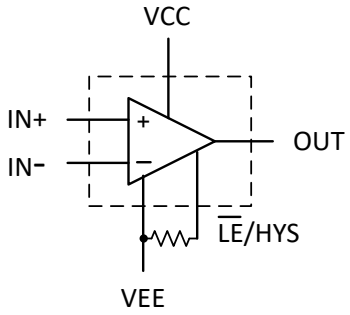


図 7-1. Adjustable Hysteresis using External Resistor

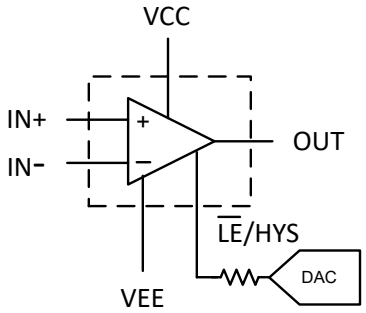


図 7-2. Adjustable Hysteresis using External Voltage

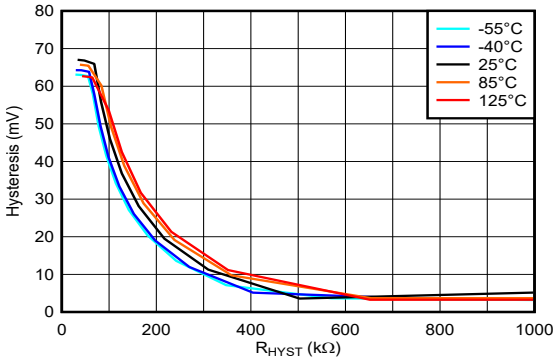


図 7-3. Hysteresis vs. R_{HYS} at V_{CC} = 5V

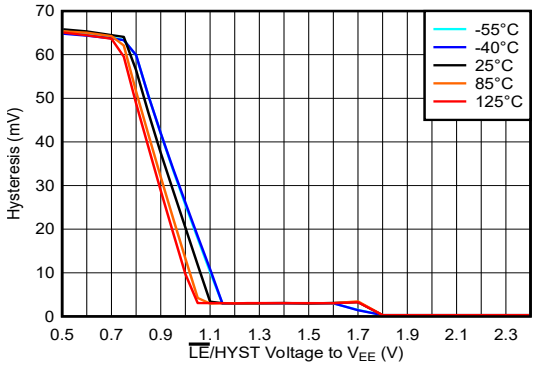


図 7-4. Hysteresis vs. V_{HYS} at V_{CC} = 5V

To provide adjustable hysteresis, an external 0.7V to 1.2V voltage, such as from a DAC, can be forced into the $\overline{LE}$/HYST pin, as shown in 図 7-2 and 図 7-4. The $\overline{LE}$/HYST pin can be internally modeled as a 40k resistor in

series with a 1.25V source to VEE, so any driving circuitry must be able to sink up to 32uA. Note that the output goes into latch when $\overline{LE}$/HYST is ≤ 400mV, or go into shutdown when ≥ 1.25V.

7.1.2 Capacitive Loads

Under reasonable capacitive loads, the device maintains specified propagation delay (see Typical Characteristics). However, excessive capacitive loading under high switching frequencies can increase supply current, propagation delay, or induce decreased slew rate.

7.1.3 Latch Functionality

The latch pin for the TLV1H103-SEP holds the output state of the device when the voltage at the $\overline{LE}$/HYS pin is a logic low. This is particularly useful when the output state is intended to remain unchanged. An important consideration of the latch functionality is the latch hold and setup times. Latch hold time is the minimum time required (after the latch pin is asserted) for properly latching the comparator output. Likewise, latch setup time is defined as the time that the input must be stable before the latch pin is asserted low. The figure below illustrates when the input can transition for a valid latch. Note that the typical setup time in the EC table is negative; this is due to the internal trace delays of the $\overline{LE}$/HYS pin relative to the input pin trace delays. A small delay (t_{PL}) in the output response is shown below when the TLV1H103-SEP exits a latched output stage.

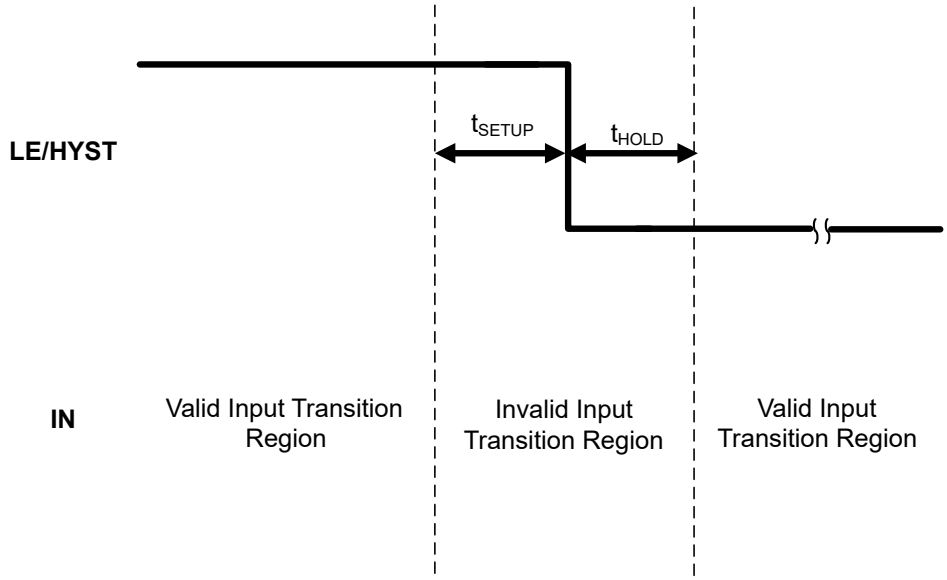


図 7-5. Input Change Properly Latched

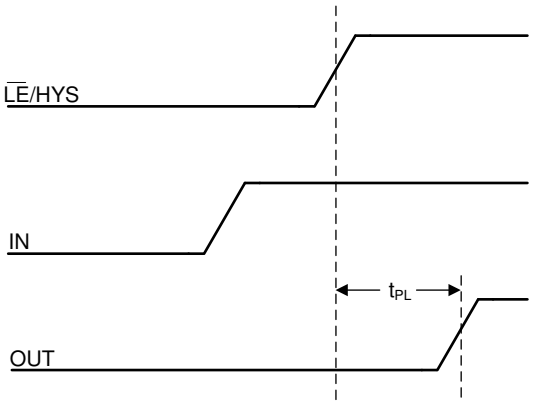


図 7-6. Latch Disable with Input Change

7.2 Typical Application

7.2.1 Implementing Adjustable Hystseresis

A comparator may produce “chatter” (multiple transitions) at the output when there are noise or signal variations around the reference threshold; this causes the output to change states in rapid random successions as the comparator input goes above and below the threshold of the reference. This usually occurs when the input signal is moving very slowly across the switching threshold of the comparator. This problem can be prevented by using the internal hysteresis feature of the TLV1H103-SEP.

The TLV1H103-SEP has a $\overline{LE}$/HYS pin that allows for variable internal hysteresis depending on the resistor value connected between the pin and VEE, where increasing the resistance decreases the hysteresis to a minimum level.

7.2.1.1 Design Requirements

For this design, follow these design requirements.

表 7-1. Design Parameters

PARAMETER	VALUE
Supply Voltage (V_{CC})	5V
V_{REF}	2.5V
V_{HYS}	30mV
Lower Threshold (V_L)	2.485V
Upper Threshold (V_H)	2.515V

7.2.1.2 Detailed Design Procedure

The hysteresis vs. resistance curve (Figure 8-2) is used as guidance to set the desired amount of hysteresis.

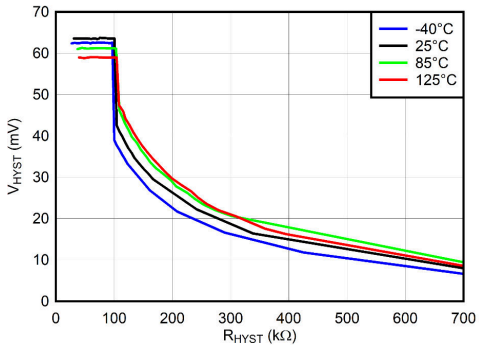


図 7-7. V_{HYST} vs. R_{HYST} at 5V curve

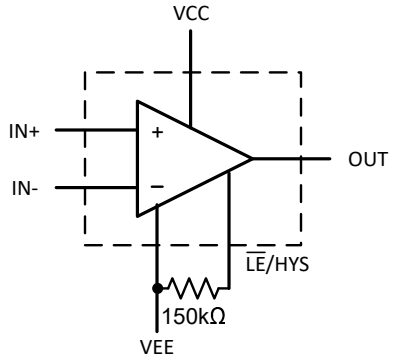


図 7-8. Setting the Hysteresis using a Resistor using the TLV1H103-SEP

Figure 8-2 shows that for a 30mV hysteresis, a 150kΩ resistor must be placed from the $\overline{LE}$/HYS pin to VEE, as shown in 図 7-8.

Also possible is to use an external voltage to dynamically program the V_{HYST}. Please see the Adjustable Hysteresis section for more details.

7.2.1.3 Application Curve

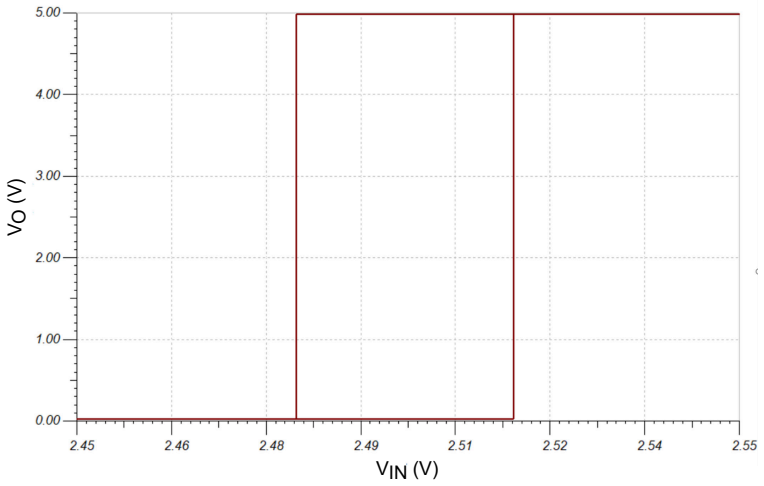


図 7-9. Hysteresis Transfer Curve using TLV1H103-SEP

7.2.2 Optical Receiver

The TLV1H103-SEP can be used in conjunction with a high performance amplifier such as the OPA858 to create an optical receiver as shown in the figure below. The photodiode is connected to a bias voltage and is being driven with a pulsed laser. The OPA858 takes the current conducting through the diode and translates the current into a voltage for a high speed comparator to detect. The TLV1H103-SEP then outputs the proper output level according to the threshold set (V_{REF}).

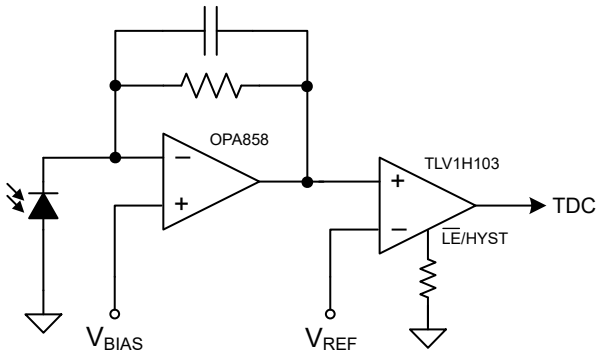


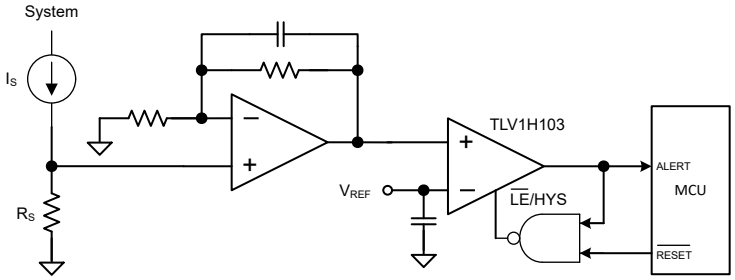
図 7-10. Optical Receiver

7.2.3 Over-Current Latch Condition

When the design is required to detect a brief over-current condition, the latching feature of the TLV1H103-SEP can be utilized. By latching the comparator output, the MCU does not miss the over-current occurrence. The circuit below shows one way to implement the latching function.

When an over-current condition is detected by the TLV1H103-SEP, the output transitions high. The occurrence of the output going high coupled with a logic high from the RESET signal from the MCU creates a logic low signal at the output of the 2-channel NAND gate. This causees the output of the TLV1H103-SEP to be held in a logic high state (latched), thus allowing the MCU to detect the fault condition regardless of how narrow the over-current condition persists. The addition of the NAND gate also provides a means of clearing the latch state of the comparator once the MCU is done processing the event. This is accomplished by the MCU passing a logic low state to the NAND input causing the $\overline{LE}$/HYS pin of the comparator to be returned to a logic high state. The latched status is cleared and the TLV1H103-SEP output can continue to track the status of the input pins.

Over-Current Latched Output Circuit



7.2.4 External Trigger Function

Below is a typical configuration for creating an external trigger signal. The user adjusts the trigger level, and a DAC converts this trigger level to a voltage the TLV1H103-SEP can use as a reference. The input voltage is then compared to the trigger reference voltage, and the TLV1H103-SEP sends an LVDS signal to a downstream FPGA to begin a capture.

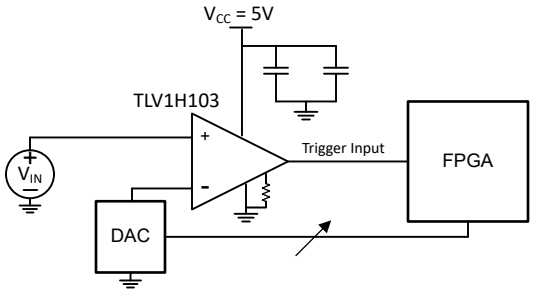


図 7-11. External Trigger Function

7.3 Power Supply Recommendations

The TLV1H103-SEP is designed for operation from 2.4V to 5.5V. While most applications require single supply operation where VEE is connected to the ground and VCC is connected to the intended power supply level, the comparators can also be operated with split supplies. One caution when using split supplies is that the output logic levels are determined by the VCC and VEE levels. For example, if split supplies of +/- 2.5V are used, the output levels are 2.5V and -2.5V accordingly. In addition, the logic level of the $\overline{\text{LE}}$/HYS pin is also referenced to VEE. This means that the external hysteresis resistor or voltage source on the TLV1H103-SEP needs to be connected between the LE/HYS pin and VEE (not to ground) for proper operation.

Regardless of single supply or split supply operation, proper decoupling capacitors are required. TI recommends using a scheme of multiple, low-ESR ceramic capacitors from the supply pins to the ground plane for optimum performance. A good combination is 100pF, 10nF, and 1uF with the lowest value capacitors closest to the comparator.

7.4 Layout

7.4.1 Layout Guidelines

Comparators are very sensitive to input noise. For best results, adhere to the following layout guidelines.

1. Use a printed-circuit-board (PCB) with a good, unbroken, low-inductance ground plane. Proper grounding (use of a ground plane) helps maintain specified device performance.

   Likewise, high performance board materials such as Rogers or high speed FR4 is also recommended.
2. Place a decoupling capacitor (100pF ceramic, surface-mount capacitor) between V_{CC} and

   V_{EE} as close to the device as possible. Using multiple bypass capacitors in different decade ranges such as 100pF, 100nF, and 1µF provides the best noise reduction across frequency ranges.

3. On the inputs and the output, keep lead lengths as short and minimize capacitive coupling to the traces by having a keepout area around the traces that is 3x the width of the traces. Also recommended is to keep input traces away from the output traces.
4. Solder the device directly to the PCB rather than using a socket.

7.4.2 Layout Example

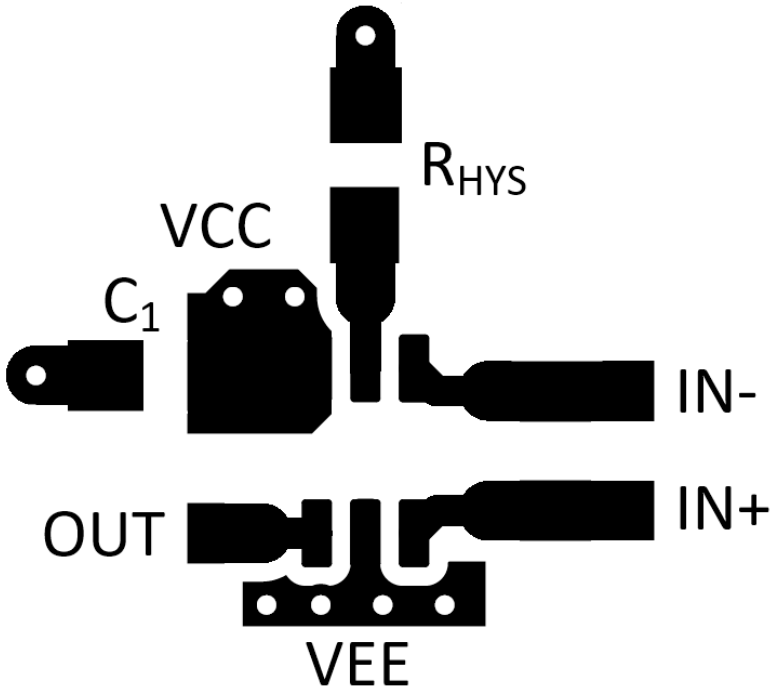


図 7-12. TLV1H103-SEP Layout Example

8 Documentation Support

8.1 Related Documentation

TLV1H103-SEP Single-Event Latch-Up (SEE) Radiation Report (SLOK017)

TLV1H103-SEP Total Ionizing Dose (TID) Report (SLOK018)

TLV1H103-SEP Neutron Displacement Damage Characterization (NDD) (SBOK088)

TLV1H103-SEP Production Flow and Reliability Report (SLOK021)

Quality Conformance Inspection (QCI) Website - Lot testing results for TI Military and Space Products

8.1.1 Development Support

LIDAR Pulsed Time of Flight Reference Design (TIDA-00663)

8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.3 サポート・リソース

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8.4 Trademarks

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8.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.6 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

DATE	REVISION	NOTES
August 2024	*	Initial release.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV1H103MDBVTSEP	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	T103
V62/22606-01XE	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	T103

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

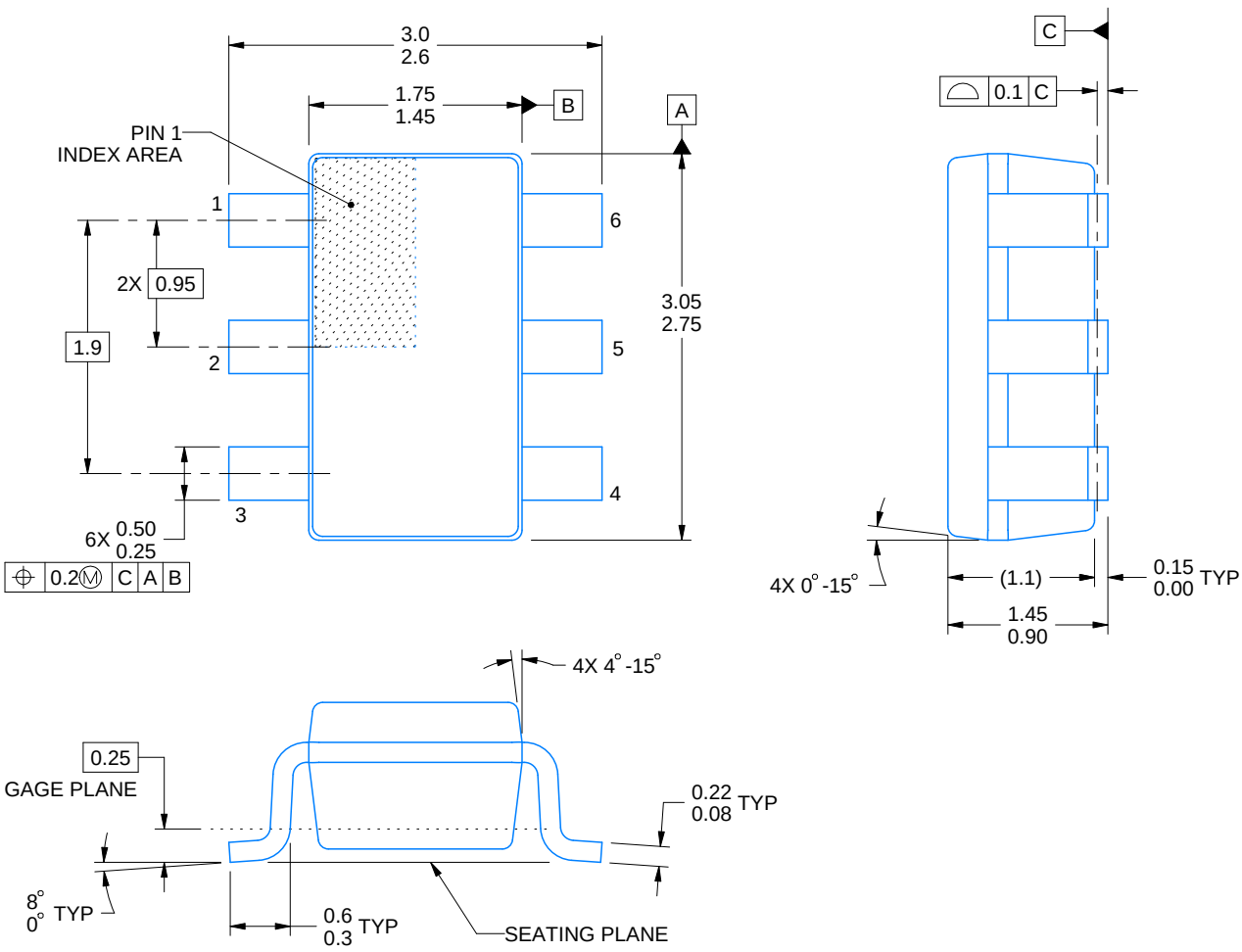
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

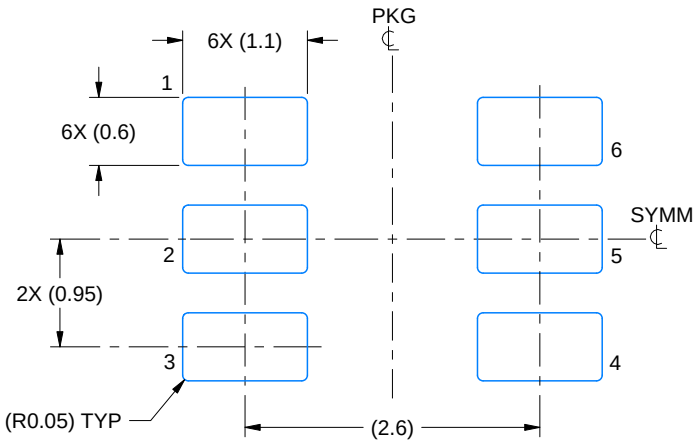
SMALL OUTLINE TRANSISTOR



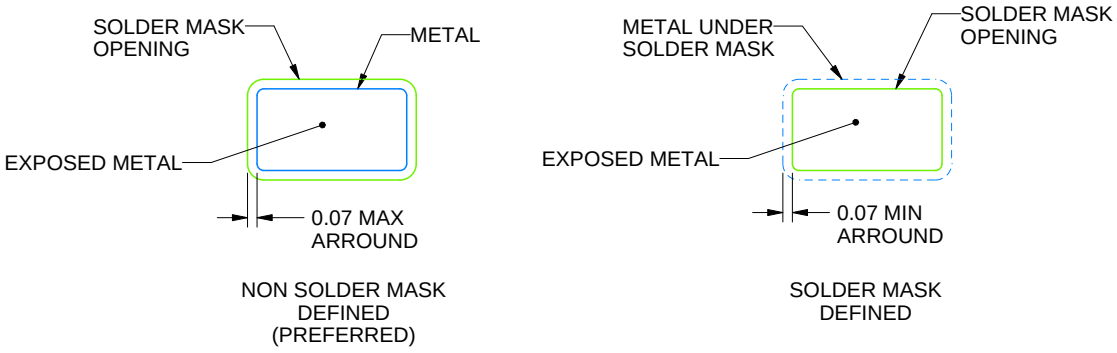
4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

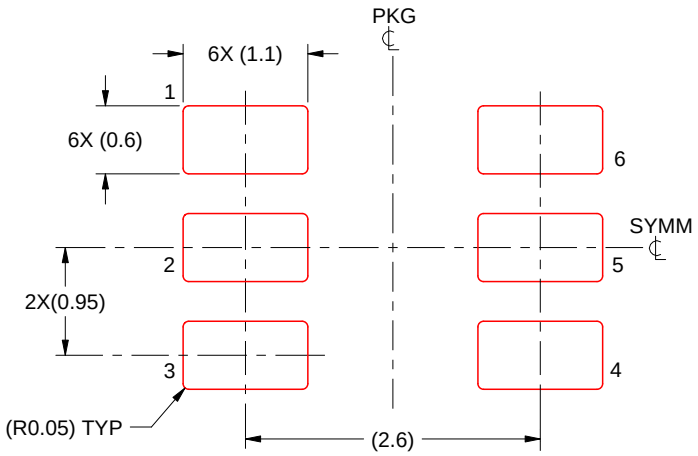


SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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