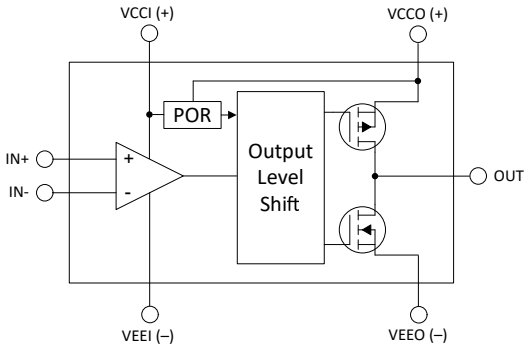
TLV1871/2 入力電源と出力電源が独立した 40V 高速コンパレータ

1 特長

- 幅広い電源電圧範囲:2.7V～40V (±1.35V～±20V)
- 伝搬遅延時間:65ns
- 単一電源または分割電源動作
- 個別電源で「フローティング」プッシュプル出力
- レール ツー レール入力
- パワーオン リセット (POR)
- 低い消費電流:75µA (チャネルあたり)
- 温度範囲:-40℃～+125℃

2 アプリケーション

- クラス D アンプ
- レベル トランスレータ
- モーター ドライブ
- バイポーラ ゼロ クロス検出器



概略内部図

3 概要

TLV187x は、レール ツー レール入力、プッシュプル出力段を備え、入力側と出力側の電源が独立している 40V 高速コンパレータです。これらの特長と 65ns の伝搬遅延の組み合わせにより、このファミリはバイポーラのゼロクロス検出、クラス D オーディオ アンプ システム、レベル変換と伝搬遅延の対称性を必要とするその他のアプリケーションに最適です。

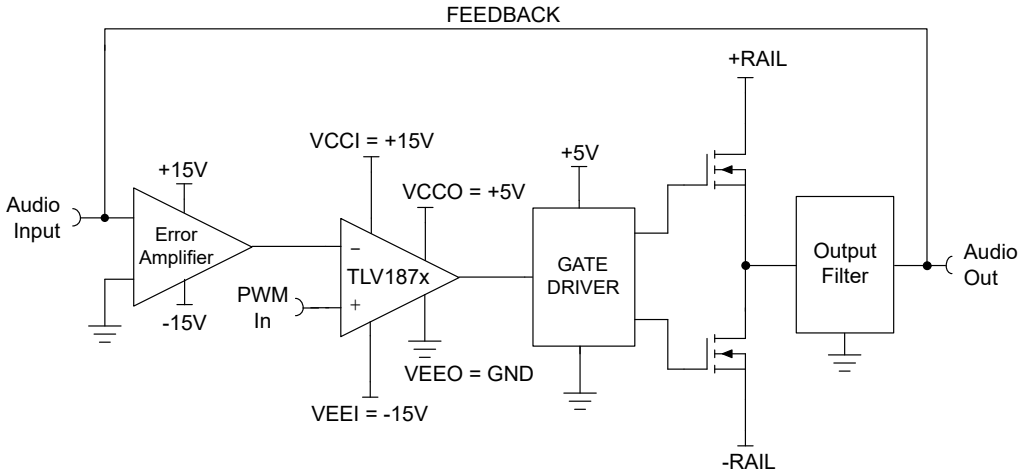
このデバイスは、パワーオン リセット (POR) 機能を搭載しており、電源電圧が最小値に達するまでの間、出力が入力に応答する前に、出力を既知の状態に維持するので、システムの電源オンおよび電源オフ時に誤った出力が発生するのを防止できます。

TLV187x にはプッシュプル出力段があるため、立ち上がりと立ち下がりの出力応答に対称性が求められるアプリケーションに最適です。このデバイスは、入力電源と出力電源が独立しているため、より低い電圧の下流デバイスに対するレベル変換が可能です。

製品情報

部品番号	パッケージ (1)	本体サイズ (公称)(2)
TLV1871	SOT-23 (8)	1.60mm × 2.90mm
TLV1872	VSSOP (10)	3.00mm × 3.00mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



クラス D アンプの例

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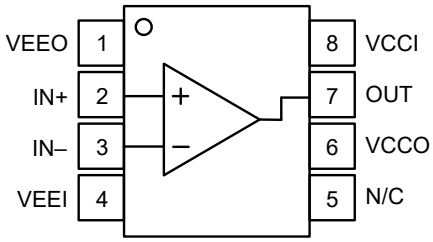
4 Pin Configuration and Functions

4.1 Pin Configurations: TLV1871 Single

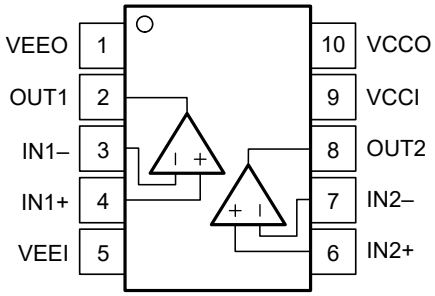


DDF Package
8-Pin SOT-23
Top View

表 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VEEO	1	—	Output negative supply voltage
IN+	2	I	Non-Inverting input
IN-	3	I	Inverting input
VEEI	4	—	Input negative supply voltage
NC	5	—	No connect
VCCO	6	O	Output positive supply voltage
OUT	7	—	Output
VCCI	8	—	Input positive supply voltage

Pin Configurations: TLV1872 Dual



DGS Package
10-Pin VSSOP
Top View

表 4-2. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VEEO	1	—	Output negative supply voltage
OUT1	2	O	Output pin of the comparator 1
IN1–	3	I	Inverting input pin of comparator 1
IN1+	4	I	Non-Inverting input pin of comparator 1
VEEI	5	—	Input negative supply voltage
IN2+	6	I	Non-Inverting input pin of comparator 2
IN2–	7	I	Inverting input pin of comparator 2
OUT2	8	O	Output pin of the comparator 2
VCCI	9	—	Input positive supply voltage
VCCO	10	—	Output positive supply voltage

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Input Supply Voltage: (V_{CCI} – V_{EEI})	–0.3	42	V
Output Negative Supply Voltage: V_{EEO}	V_{EEI}	V_{EEI} + 20	V
Output Positive Supply Voltage: V_{CCO}	V_{EEO} – 0.3	V_{CCI} + 0.3	V
Input pins (IN+, IN–) (2)	V_{EEI} – 0.3	V_{CCI} + 0.3	V
Current into input pins (IN+, IN–) (2)	–10	10	mA
Output (OUT) from V_{EEO} (3)	–0.3	(V_{CCO}) + 0.3	V
Output short circuit current(4) (5)	–10	10	mA
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings can cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Input terminals are diode-clamped to (V_{EEI}) and (V_{CCI}). Input signals that can swing more than 0.3V beyond the supply rails must be current-limited to 10mA or less.
(3) Output (OUT) is diode-clamped to (V_{EEO}) and (V_{CCO}). Please see the *Outputs* and *ESD Protection* section of the *Application Information* Section for more information.
(4) Output sinking and sourcing current is internally limited to <35mA when operating within the Absolute Maximum output voltage limits. The Absolute Maximum Output Current limit specified here is the maximum current through the clamp structure when exceeding the supply voltage below (V_{EEO}) or above (V_{CCO}).
(5) Continuous output short circuits at elevated supply voltages can result in excessive heating and exceeding the maximum allowed junction temperature, leading to eventual device destruction.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Thermal Information

THERMAL METRIC[1]		TLV1871 DDF (SOT-23) 8 PINS	TLV1872 DGS (WSON) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	165.8	151.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	86.0	55.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	83.5	84.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.6	3.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	83.2	83.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	–	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics report.

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input Supply Voltage: $V_{CCI} – V_{EEI}$		2.7	40	V
Output Negative Supply Voltage: V_{EEO}		V_{EEI}	V_{EEI} + 18	V
Output Positive Supply Voltage: V_{CCO}		V_{EEO} + 2.7	V_{CCI}	V
Input voltage range from V_{EEI}		– 0.2	V_{CCI} + 0.2	V
Ambient temperature, T_A		–40	125	°C

5.5 Electrical Characteristics

For VCCI = 12V, VEEI = 0V, VCCO = 3.3V, VEEO = 0V, V_{CM} = 0V at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	T_A = 25°C	–2.5	±0.3	2.5	mV
V_{OS}	Input offset voltage	T_A = –40°C to +125°C	–3.0		3.0	mV
dV_{IO}/dT	Input offset voltage drift	T_A = –40°C to +125°C		±1.2		µV/°C
POWER SUPPLY						
I_Q	Quiescent current per comparator (2)	No Load, Output High T_A = 25°C		75	100	µA
		No Load, Output High T_A = –40°C to +125°C			105	µA
		No Load, Output Low T_A = 25°C		100	135	µA
		No Load, Output Low T_A = –40°C to +125°C			140	µA
V_{POR}				1.9		V
INPUT BIAS CURRENT						
I_B	Input bias current (1)			500		pA
I_B	Input bias current (1) (3)	T_A = –40°C to +125°C	-5		5	nA
I_{OS}	Input offset current			10		pA
INPUT CAPACITANCE						
C_{ID}	Input Capacitance, Differential			5		pF
C_{IC}	Input Capacitance, Common Mode			5		pF
INPUT COMMON MODE RANGE						
$V_{CM\text{-}Range}$	Common-mode voltage range	V_{CCI} - V_{EEI} = 2.7V to 36V T_A = –40°C to +125°C	V_{EEI} – 0.2		V_{CCI} + 0.2	V
OUTPUT						
V_{OL}	Voltage swing from (V_{EEO})	I_{SINK} = 4mA T_A = –40°C to +125°C			300	mV
V_{OH}	Voltage swing from (V_{CCO})	I_{SOURCE} = 4mA T_A = –40°C to +125°C			300	mV
I_{OL}	Short-circuit current	Sinking T_A = –40°C to +125°C		30		mA
I_{OH}	Short-circuit current	Sourcing T_A = –40°C to +125°C		30		mA

(1) Please see figure for I_{BIAS} vs V_{ID} performance curve
(2) Current shown is the sum of the current through VCCI and VCCO. Please see Supply Current graphs in Typical Characteristics section.
(3) This parameter is assured by design and/or characterization and is not tested in production.

5.6 Switching Characteristics

For V_{CCI} = 12V, V_{EEI} = 0V, V_{CCO} = 3.3V, V_{EEO} = 0V, V_{CM} = VS/2, C_L = 15pF at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output						
T_{PD-HL}	Propagation delay time, high-to-low	V_{OD} = 10mV, V_{UD} = 100mV		110		ns
T_{PD-HL}	Propagation delay time, high-to-low,	V_{OD} = 100mV, V_{UD} = 100mV		65		ns
T_{PD-LH}	Propagation delay time, low-to-high	V_{OD} = 10mV, V_{UD} = 100mV		110		ns
T_{PD-LH}	Propagation delay time, low-to-high	V_{OD} = 100mV, V_{UD} = 100mV		65		ns
T_{RISE}	Output Rise Time, 20% to 80%	V_{OD} = 100mV, V_{UD} = 100mV		5		ns
T_{FALL}	Output Fall Time, 80% to 20%	V_{OD} = 100mV, V_{UD} = 100mV		5		ns
F_{TOGGLE}	Toggle Frequency	V_{ID} = 200mV		7.5		MHz
POWER ON TIME						
P_{ON}	Power on-time			80		µs

5.7 Typical Characteristics

At T_A = 25°C, V_{CCI} - V_{EEI} = 12V, V_{CCO} - V_{EEO} = 3.3V, V_{CM} = VS/2V, C_L = 15pF, Input Overdrive = Input Underdrive = 100mV unless otherwise noted.

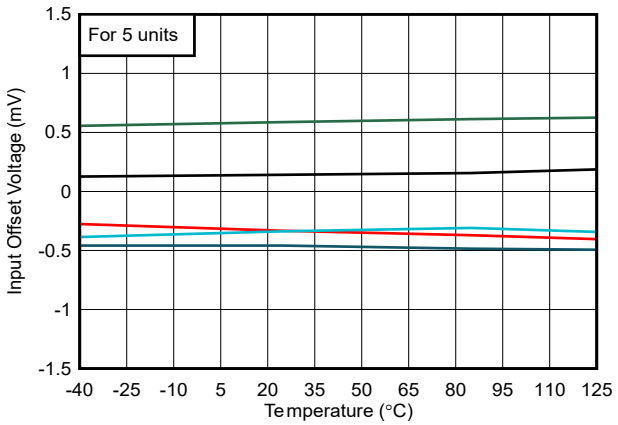


図 5-1. Offset vs. Temperature

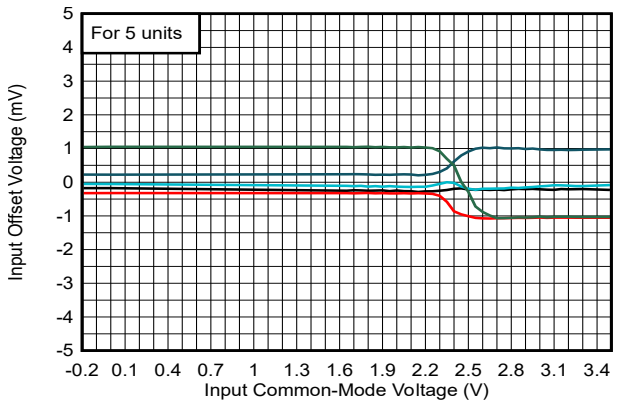


図 5-2. Offset vs. Common-Mode, 3.3V

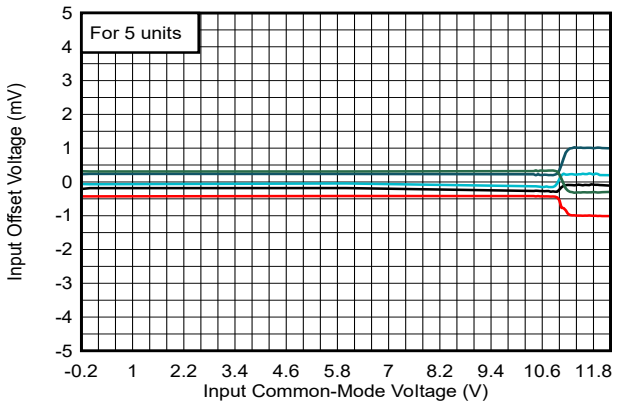


図 5-3. Offset Voltage vs. Common-Mode, 12V

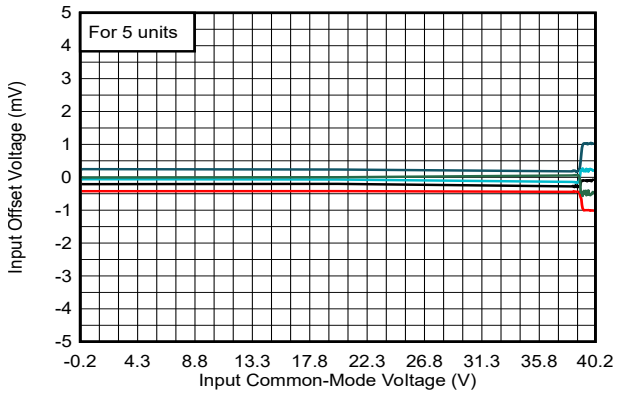


図 5-4. Offset Voltage vs. Common-Mode, 40V

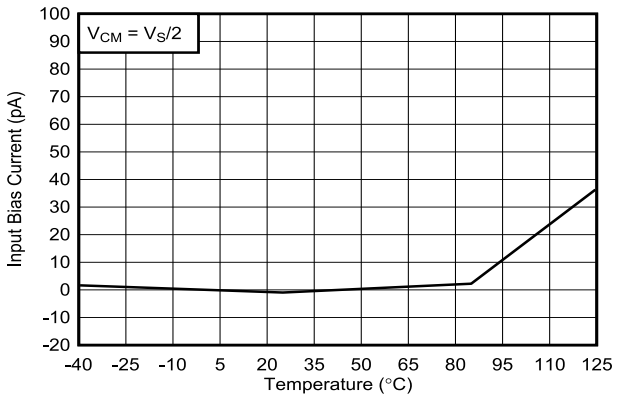


図 5-5. Bias Current vs. Temperature, 3.3V

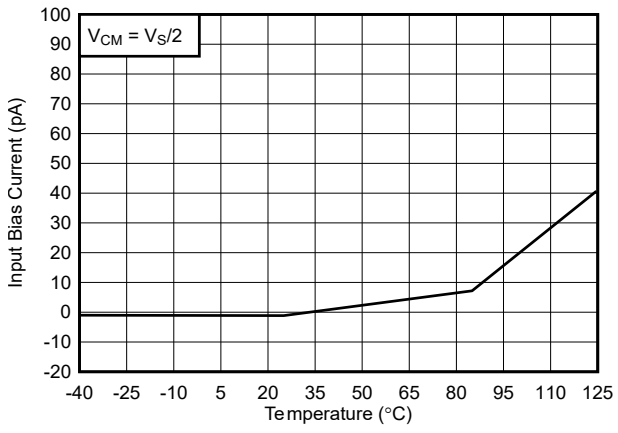


図 5-6. Bias Current vs. Temperature, 40V

5.7 Typical Characteristics (continued)

At T_A = 25°C, V_{CCI} - V_{EEI} = 12V, V_{CCO} - V_{EEO} = 3.3V, V_{CM} = VS/2V, C_L = 15pF, Input Overdrive = Input Underdrive = 100mV unless otherwise noted.

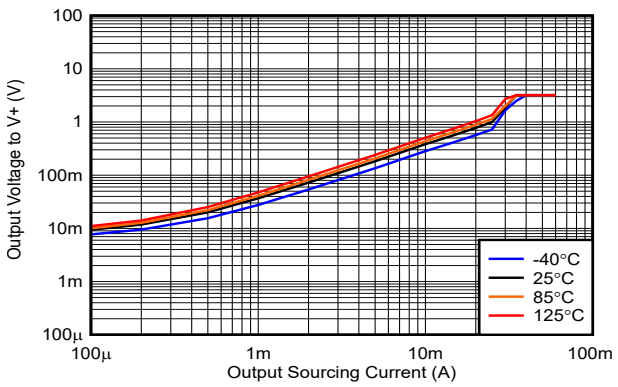


図 5-7. Output Voltage vs. Sourcing Current, 3.3V

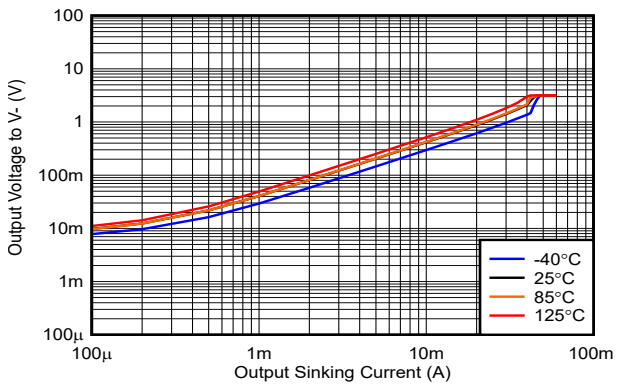


図 5-8. Output Voltage vs. Sinking Current, 3.3V

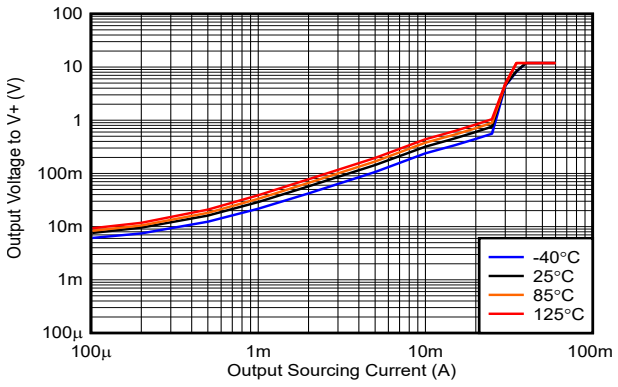


図 5-9. Output Voltage vs. Sourcing Current, 12V

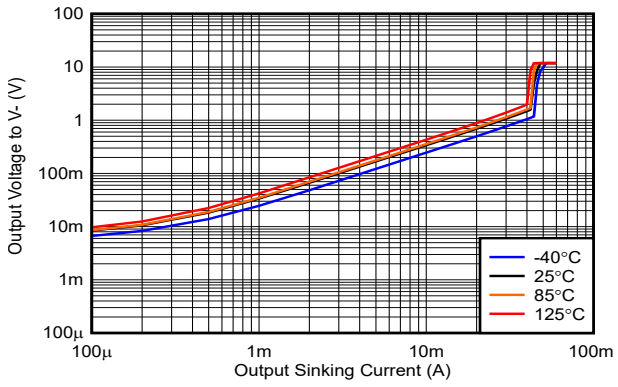


図 5-10. Output Voltage vs. Sinking Current, 12V

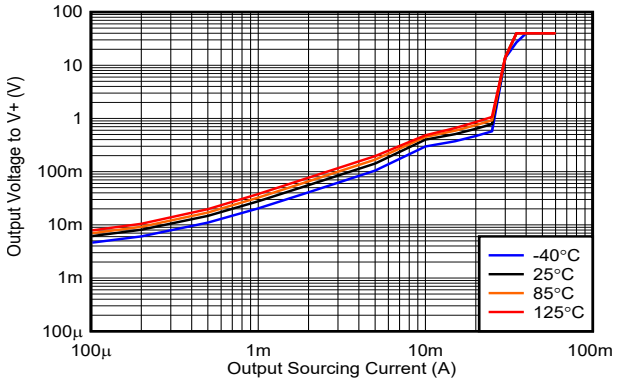


図 5-11. Output Voltage vs. Sourcing Current, 40V

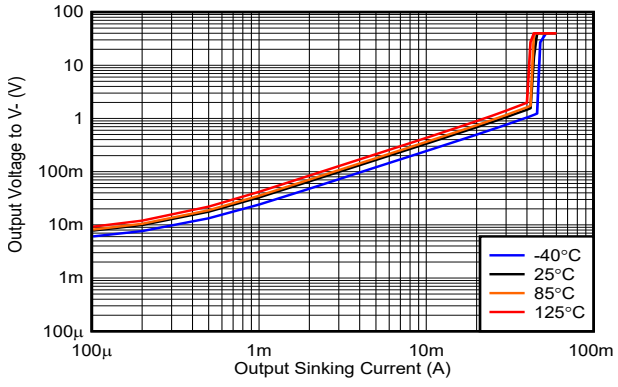


図 5-12. Output Voltage vs. Sinking Current, 40V

5.7 Typical Characteristics (continued)

At T_A = 25°C, V_{CCI} - V_{EEI} = 12V, V_{CCO} - V_{EEO} = 3.3V, V_{CM} = VS/2V, C_L = 15pF, Input Overdrive = Input Underdrive = 100mV unless otherwise noted.

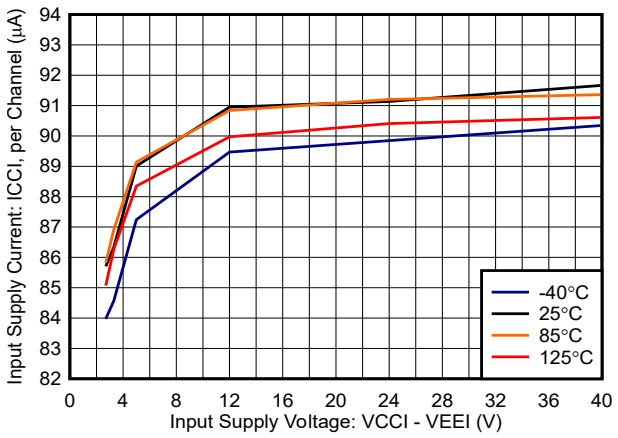


図 5-13. Input Supply Current vs. Input Supply Voltage, Output Low, No Load

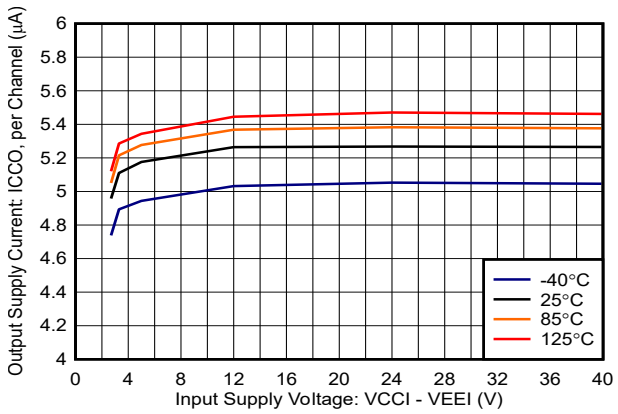


図 5-14. Output Supply Current vs. Input Supply Voltage, Output Low, No Load

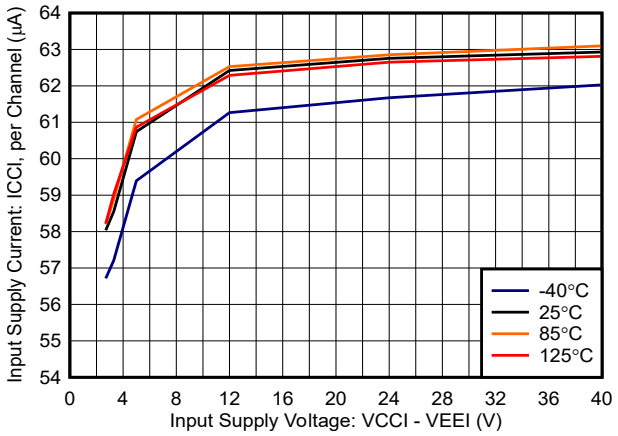


図 5-15. Input Supply Current vs. Input Supply Voltage, Output High, No Load

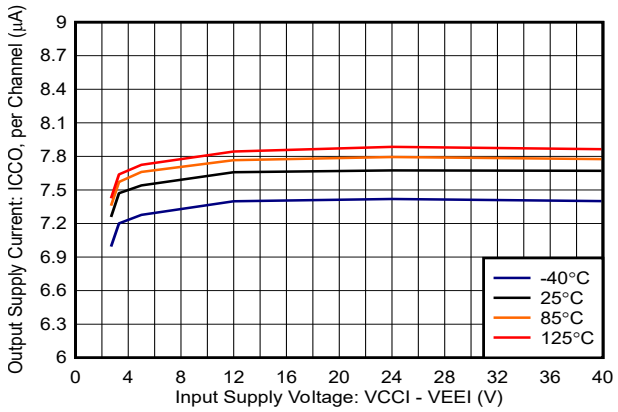


図 5-16. Output Supply Current vs. Input Supply Voltage, Output High, No Load

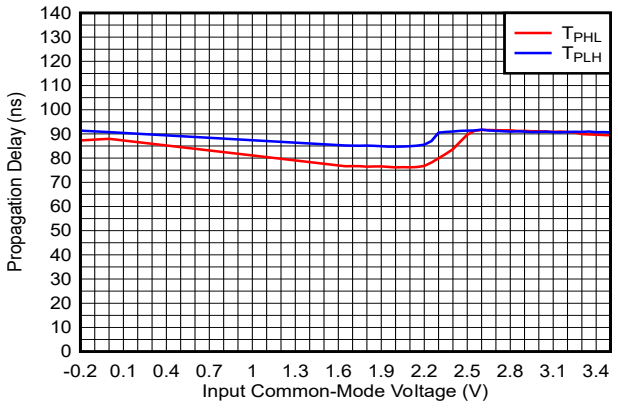


図 5-17. Propagation Delay vs. Common-Mode, 3.3V

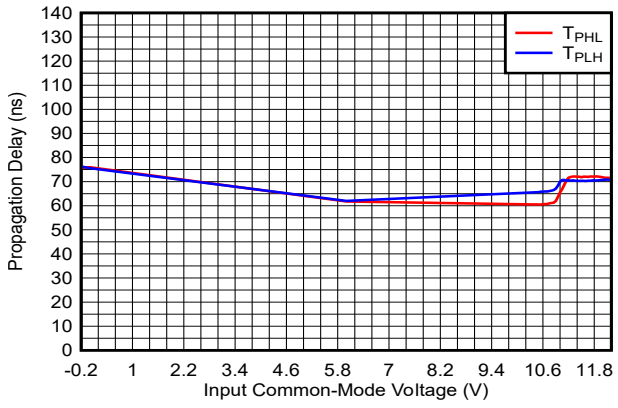


図 5-18. Propagation Delay vs. Common-Mode, 12V

5.7 Typical Characteristics (continued)

At T_A = 25°C, V_{CCI} - V_{EEI} = 12V, V_{CCO} - V_{EEO} = 3.3V, V_{CM} = VS/2V, C_L = 15pF, Input Overdrive = Input Underdrive = 100mV unless otherwise noted.

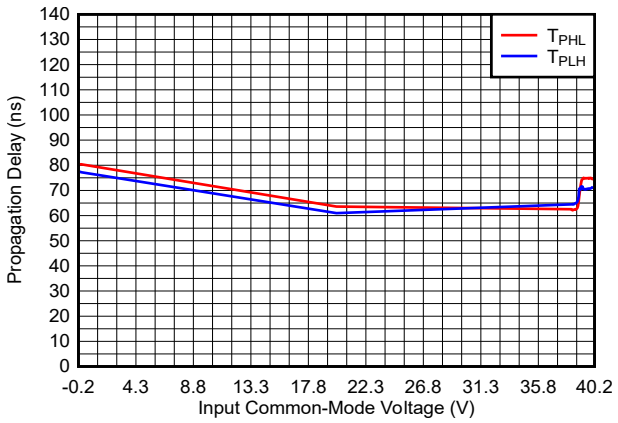


図 5-19. Propagation Delay vs. Common-Mode, 40V

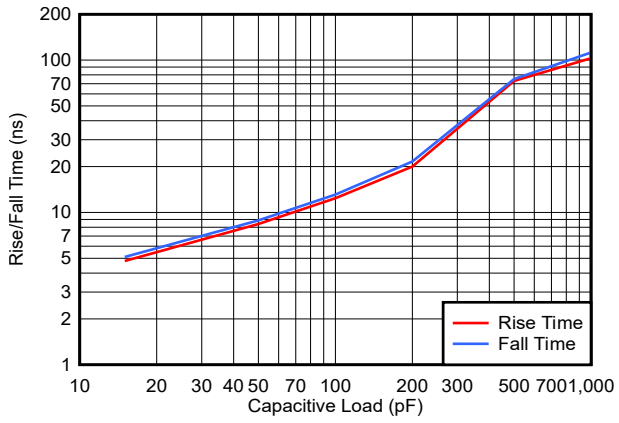


図 5-20. Rise/Fall Time vs. Capacitive Load, 12V

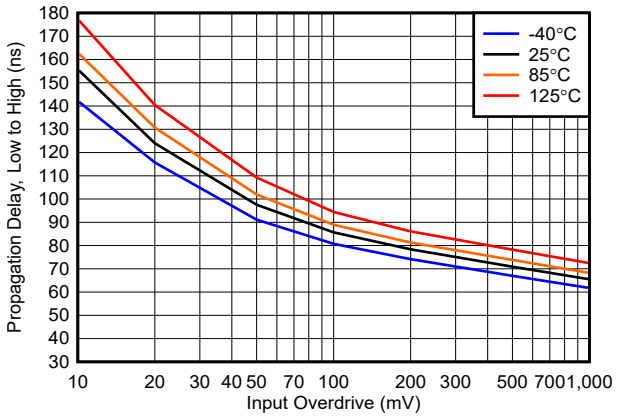


図 5-21. Propagation Delay, (Low to High) vs. Input Overdrive, 3.3V

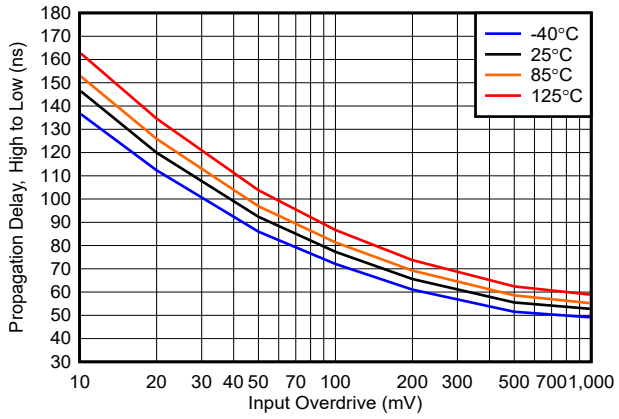


図 5-22. Propagation Delay, (High to Low) vs. Input Overdrive, 3.3V

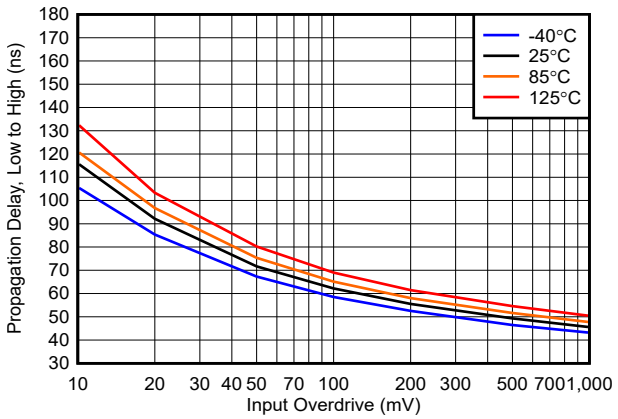


図 5-23. Propagation Delay, (Low to High) vs. Input Overdrive, 12V

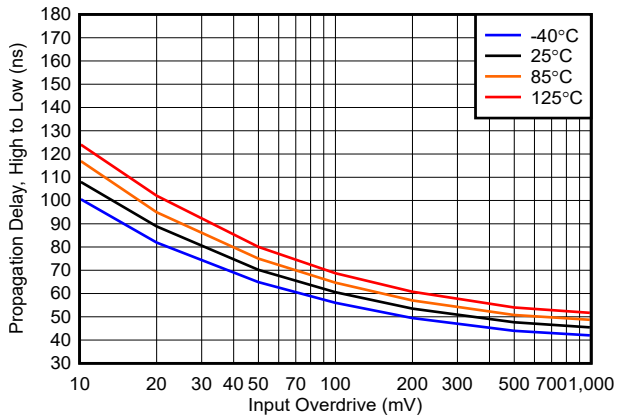


図 5-24. Propagation Delay, (High to Low) vs. Input Overdrive, 12V

5.7 Typical Characteristics (continued)

At T_A = 25°C, V_{CCI} - V_{EEI} = 12V, V_{CCO} - V_{EEO} = 3.3V, V_{CM} = VS/2V, C_L = 15pF, Input Overdrive = Input Underdrive = 100mV unless otherwise noted.

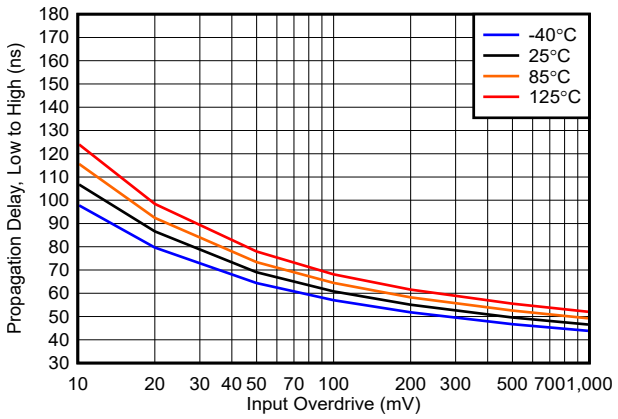


図 5-25. Propagation Delay, (Low to High) vs. Input Overdrive, 40V

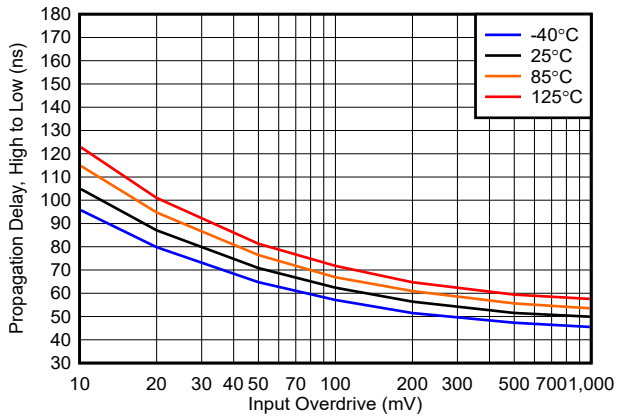


図 5-26. Propagation Delay, (High to Low) vs. Input Overdrive, 40V

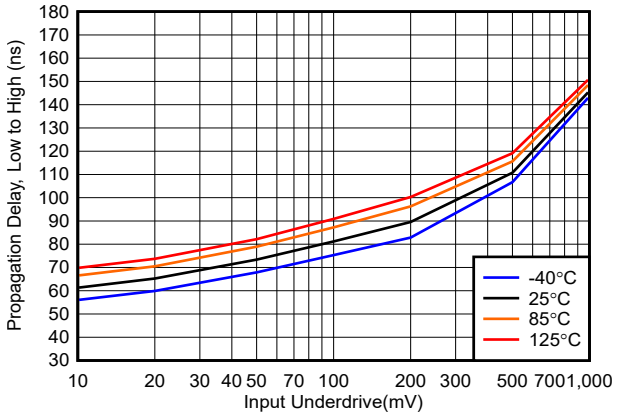


図 5-27. Propagation Delay, (Low to High) vs. Input Underdrive, 3.3V

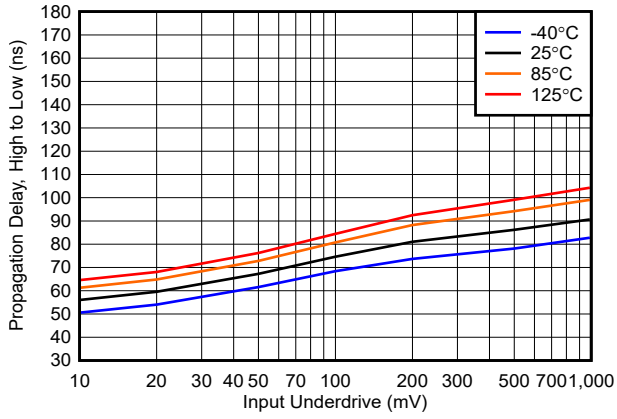


図 5-28. Propagation Delay, (High to Low) vs. Input Underdrive, 3.3V

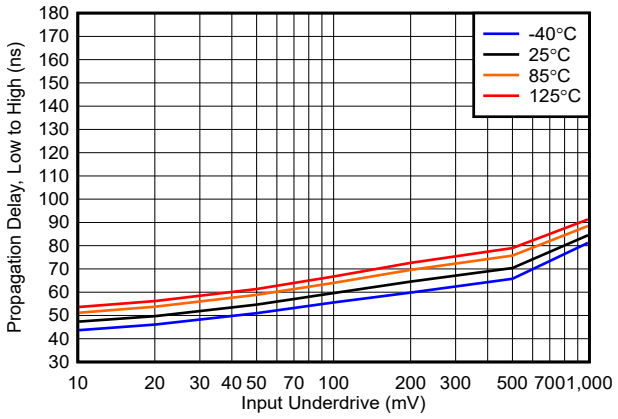


図 5-29. Propagation Delay, (Low to High) vs. Input Underdrive, 12V

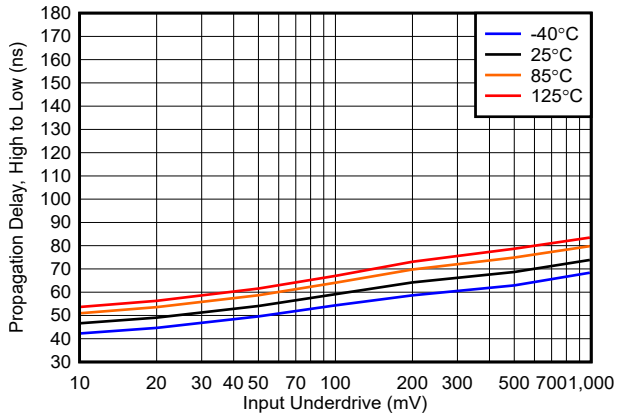


図 5-30. Propagation Delay, (High to Low) vs. Input Underdrive, 12V

5.7 Typical Characteristics (continued)

At T_A = 25°C, V_{CCI} - V_{EEI} = 12V, V_{CCO} - V_{EEO} = 3.3V, V_{CM} = VS/2V, C_L = 15pF, Input Overdrive = Input Underdrive = 100mV unless otherwise noted.

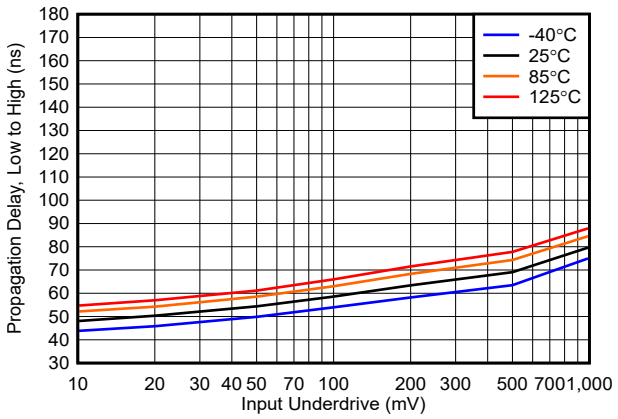


図 5-31. Propagation Delay, (Low to High) vs. Input Underdrive, 40V

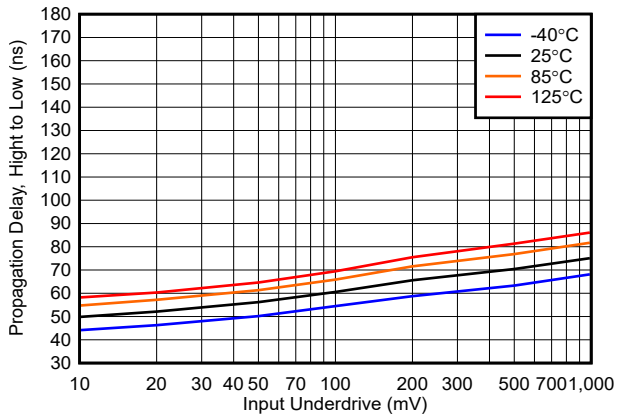


図 5-32. Propagation Delay, (High to Low) vs. Input Underdrive, 40V

6 Detailed Description

6.1 Overview

The TLV187x family are 40V high-speed comparators with push-pull output with separate input and output supplies allow for split supply capability on the inputs and level shifted outputs for downstream 5V or 3.3V logic devices. This makes the TLV187x well suited for bipolar zero-cross detection applications or Class-D audio amplifier systems. An internal power-on reset circuit makes sure that the output remains in a known state during power-up and power-down.

6.2 Functional Block Diagram

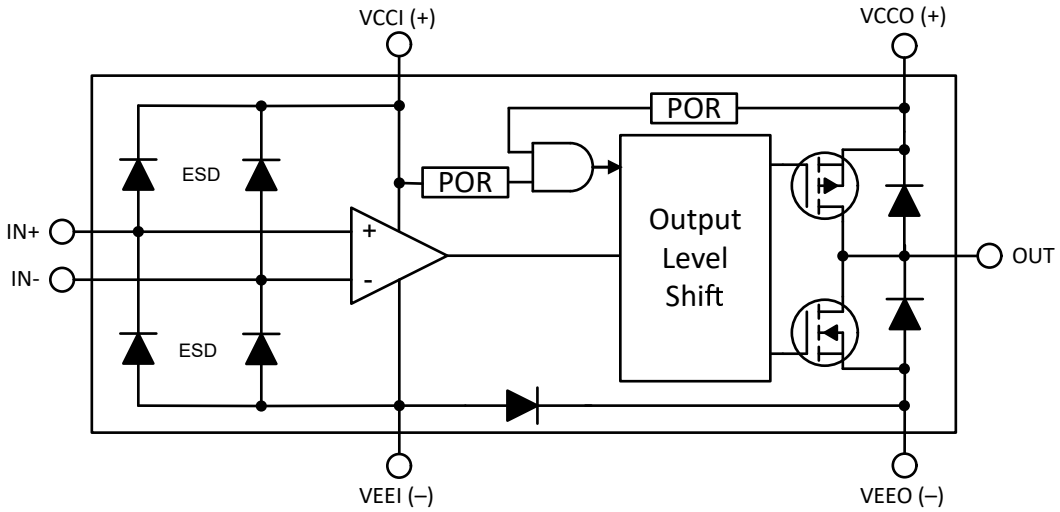


図 6-1. Block Diagram

6.3 Feature Description

The TLV187x (push-pull output) devices are high speed comparators with a typical propagation delay of 65ns and are capable of operating at voltages up to 40V. The separate input and output supplies make these comparators well-suited for applications that need bipolar signals to be level shifted to low voltage logic devices. This also eliminates the need for a pull-up resistor and offers propagation delay and edge-rate symmetry. These comparators also feature a rail-to-rail input stage capable of operating up to 200mV beyond the power supply rails combined with a maximum 2.5mV input offset and Power-On Reset (POR) for known start-up conditions.

6.4 Device Functional Modes

6.4.1 Separate Power Supplies

The TLV187x has a unique "floating" output stage where the input and output have separate power supplies to allow defining the output levels without external level shifting. This allows directly sensing bipolar input signals using a split supply, and ground-referenced, low-voltage logic output designed for directly driving processors, ASICs or gate drivers.

The VCCI and VEEI pins supply the power to the input stage and comparator core. The VCCO and VEEO pins provide the power for the output stage and set the output swing.

The VCCO and VEEO pins are bounded by the VEEI and VCCI pins. Please see the Absolute Maximum Ratings and Recommended Operating Conditions tables for the specifications. Below is a summary of the limits.

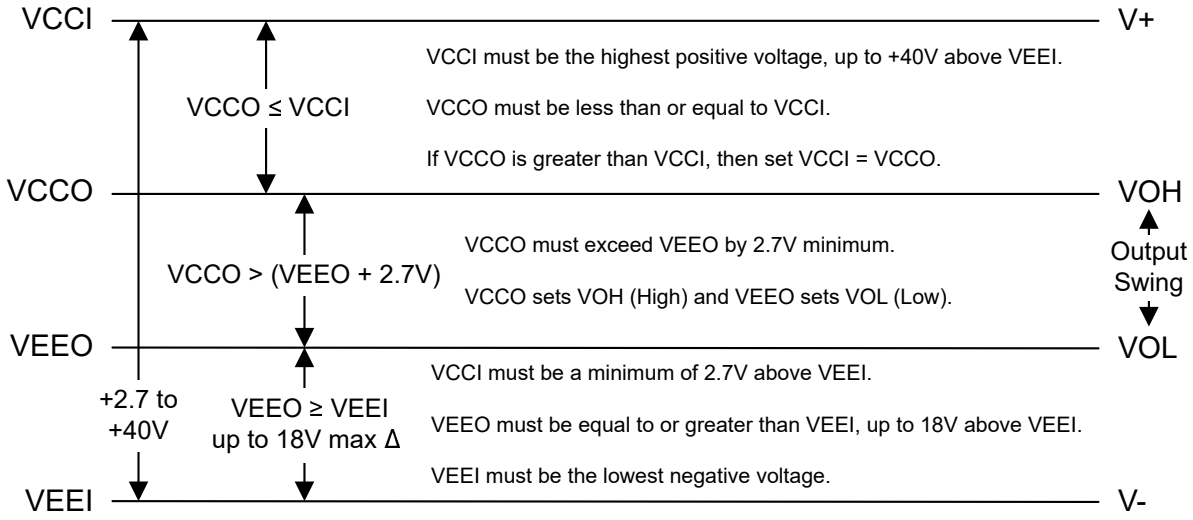


図 6-2. Graphical View of Supply Limits

VCCI is the positive supply for the input stage and sets the positive input voltage range (Positive VCM). VCCI must be a minimum of 2.7V and up to a maximum of 40V above VEEI to establish the total operating voltage (V_S).

VCCO is the positive supply for the output stage, and sets the output high voltage level (VOH). VCCO must be at least 2.7V above VEEO and up to a maximum of VCCI.

VEEO is the negative supply for the output stage, and sets the output low voltage level (VOL). The VEEO pin must be equal to, or greater than the VEEI pin with up to a maximum +18V difference between the VEEI and VEEO pins.

VEEI is the negative supply for the input stage, and sets the negative input voltage range (negative VCM). The VEEI pin is the most negative "substrate" supply of the device. **Therefore the VEEI pin must be at the most negative circuit potential.** There must never be any more than 40V across the entire device with any combination of supply pins.

For example, an application where the input stage is VCCI = +15V, VEEI = –15V, and the output stage is using a single supply with VCCO = +3.3V and VEEO = GND is acceptable.

However, an application where VCCI = +5V, VEEI = GND, and the output stage using a split supply with VCCO = +12V and VEEO =-12V is **NOT** possible as that violates VEEO >= VEEI (VEEI is not the lowest negative potential) and VCCI < VCCO. If VCCI is instead connected to the +12V supply, and the VEEI is connected the -12V supply, that is acceptable.

Conversely, a negative input voltage application where VCCI = GND, VEEI = -12V, and the output stage using a single supply with VCCO = +3V and VEEO = GND is **NOT** possible as that violates VCCO >= VCCI (VEEO is

greater than VCCI). In this case, instead tie VCCI to the +3V output supply and that is acceptable (VCCI = VCCO).

Single supply applications are also possible, with both VEEO and VEEI at GND, as long as VCCO is less than or equal to VCCI (VCCO <= VCCI). So VCCO = +3V and VCCI = +12V is acceptable, but VCCO = +12V and VCCI = +3V is **NOT** possible (instead, tie VCCI to the +12V to make acceptable).

Also possible is to have the output swing between two positive voltage values, such as +2V and +5V, (i.e., VEEO= +2V, VCCO = +5V) as long as the above conditions are followed (VCCI >= +5V and VEEO > VEEI) and there is a minimum of +2.7V between VEEO and VCCO.

6.4.2 Power-On Reset (POR)

The TLV187x devices have an internal Power-on-Reset (POR) circuit for known start-up or power-down conditions. While the power supplies are ramping up, the POR circuitry is activated for up to 80µs after the V_{POR} threshold of 1.7V is crossed.

The TLV187x Output is High Impedance ("Hi-Z") During the POR Period (t_{on}).

The input and output POR thresholds are "AND'ed" together. When *BOTH* the input supply (VCCI-VEEI) *AND* the output supply (VCCO - VEEO) are greater than the V_{POR} voltage, then after a delay period (t_{ON}), the comparator output reflects the state of the differential input (V_{ID}).

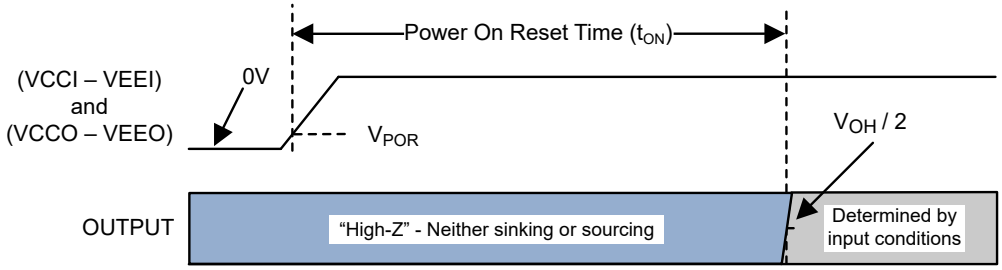


図 6-3. Power-On Reset Timing Diagram

There is no delay on power down. The output enters the POR state immediately when both the supplies fall below V_{POR}.

6.4.3 Inputs

6.4.3.1 Rail-to-Rail Inputs

The input voltage range extends from 200mV below VEEI to 200mV above VCCI, maximizing input dynamic range. The input stage has ESD clamps to the VCCI supply line and therefore the input voltages must not exceed the supply voltages by more than 200mV. Do not apply signals to the rail to rail inputs with no supply voltage. To avoid damaging the inputs when exceeding the recommended input voltage range, an external resistor must be used to limit the current to less than 1mA. Likewise, unlike high-speed amplifiers, the comparator inputs do not have clamping diodes between them. This allows for applications where the input differential voltage can match the supply voltage (V+). However, when the input differential voltage increases to 2V, bias current increases to the nA range occur. This is a result of internal circuitry intended to minimize propagation delay increases due to large input underdrive amplitudes.

6.4.3.2 Unused Inputs

If a channel is not to be used, DO NOT tie the inputs together. Due to the high equivalent bandwidth and low offset voltage, tying the inputs directly together can cause high frequency oscillations as the device triggers on it's own internal wideband noise. Instead, the inputs can be tied to any available voltage that resides within the specified input voltage range and provides a minimum of 50mV differential voltage. For example, one input can be grounded and the other input connected to a reference voltage, or even VCCI.

6.4.4 Push-Pull Output

The TLV187x features a push-pull output stage capable of both sinking and sourcing current. This allows driving loads such as LED's and MOSFET gates, as well as eliminating the need for a power-wasting external pull-up resistor. The push-pull output must never be connected to another output.

Directly shorting the output to the supply rails can result in thermal runaway and eventual device destruction. If output shorts are possible, a series current limiting resistor in series with the output is recommended to limit the power dissipation.

Unused push-pull outputs must be left floating, and never tied to a supply, ground, or another output.

6.4.5 ESD Protection

The rail-to-rail input has ESD clamps to both VCCI and VEEI, as shown in the Functional Block Diagram, and therefore the input voltage must not exceed the VCCI and VEEO supply voltages by more than 200mV. Do not apply signals directly to the inputs with no supply voltage without series input current limiting.

If the inputs are to be connected to a low impedance source, such as a power supply or buffered reference line, or a signal that can be present while the power is off, TI recommends adding a current-limiting resistor in series with the input to limit any transient currents in case the clamps conduct. The current must be limited to 10mA or less. This series resistance can be part of any resistive input dividers or networks.

The TLV187x push-pull output has ESD clamps to both VCCO and VEEO, as shown in the Functional Block Diagram. The output must not exceed the output supply rails by more than 200mV. Output excursions can be caused by output trace ringing, inductive load kick-back, or externally induced transients.

Due to the high (<10ns) output edge rates, unless matched impedance traces are used, a small series resistor (33 to 100Ω) can be added in series with the output trace to dampen unmatched trace reflections. See the Layout Example in the Layout Guidelines section.

7 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for custimer purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Basic Comparator Definitions

7.1.1.1 Operation

The basic comparator compares the input voltage (V_{IN}) on one input to a reference voltage (V_{REF}) on the other input. In the 図 7-1 example below, if V_{IN} is less than V_{REF}, the output voltage (V_O) is logic low (V_{OL}). If V_{IN} is greater than V_{REF}, the output voltage (V_O) is at logic high (V_{OH}). 表 7-1 summarizes the output conditions. The output logic can be inverted by simply swapping the input pins.

表 7-1. Output Conditions

Inputs Condition	Output
IN+ > IN-	HIGH (V_{OH})
IN+ = IN-	Indeterminate (chatters - see Hysteresis)
IN+ < IN-	LOW (V_{OL})

7.1.1.2 Propagation Delay

There is a delay between from when the input crosses the reference voltage and the output responds. This is called the Propagation Delay. Propagation delay can be different between high-to low and low-to-high input transitions. This is shown as t_{pLH} and t_{pHL} in 図 7-1 and is measured from the mid-point of the input to the midpoint of the output.

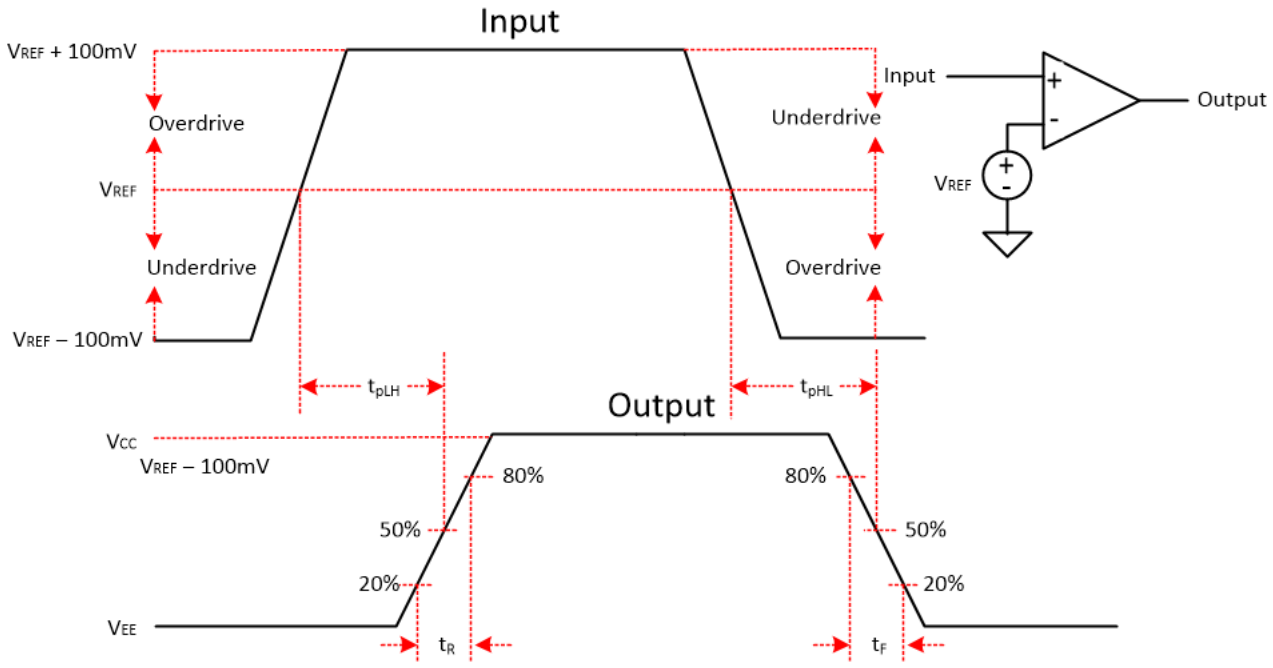


図 7-1. Comparator Timing Diagram

7.1.1.3 Overdrive Voltage

The overdrive voltage, V_{OD}, is the amount of input voltage beyond the reference voltage (and not the total input peak-to-peak voltage). The overdrive voltage is 100mV as shown in the 図 7-1 example. The overdrive voltage can influence the propagation delay (t_p). The smaller the overdrive voltage, the longer the propagation delay, particularly when <100mV. If the fastest speeds are desired, TI recommends applying the highest amount of overdrive possible.

The risetime (t_r) and falltime (t_f) is the time from the 20% and 80% points of the output waveform.

7.1.2 Hysteresis

The basic comparator configuration can produce a noisy "chatter" output if the applied differential input voltage is near the comparator's offset voltage. This usually occurs when the input signal is moving very slowly across the switching threshold of the comparator. This problem can be prevented by adding external hysteresis to the comparator.

Since the TLV187x has a minimal amount of internal hysteresis of 2.7mV, external hysteresis can be applied in the form of a positive feedback loop that adjusts the trip point of the comparator depending on the current output state.

The hysteresis transfer curve is shown in 図 7-2. This curve is a function of three components: V_{TH}, V_{OS}, and V_{HYST}:

- V_{TH} is the actual set voltage or threshold trip voltage.
- V_{OS} is the internal offset voltage between V_{IN+} and $V_{IN–}$. This voltage is added to V_{TH} to form the actual trip point at which the comparator must respond to change output states.
- V_{HYST} is the hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise.

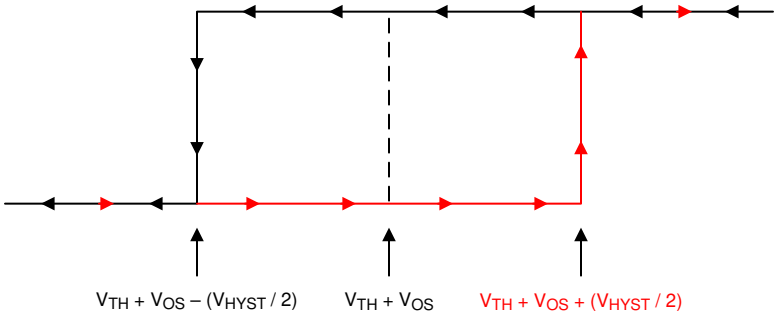


図 7-2. Hysteresis Transfer Curve

For more information, please see Application Note SBOA219 "Comparator with and without hysteresis circuit".

7.2 Typical Applications

7.2.1 Accurate Bipolar Zero-Cross Detector

図 7-3 below shows a bipolar input zero cross detector circuit. The signal source is the secondary of a current or voltage transformer which outputs a bipolar (±100 mVp to ±12 Vp) AC signal that swings around 0V (GND). Since the input voltages are not AC coupled, level shifted or further attenuated, DC accurate millivolt zero cross accuracy is possible (even with distorted waveforms). This is due to the direct DC coupled input allowing below-ground bipolar detection range afforded by the split ±12V supplies and rail-to-rail input of the TLV187x. DC coupling also avoids phase shifts caused by AC coupling and non-linearities caused by diode clamping. As the output does not require any further level-shifting or attenuation, the best possible output edge is available for the processor.

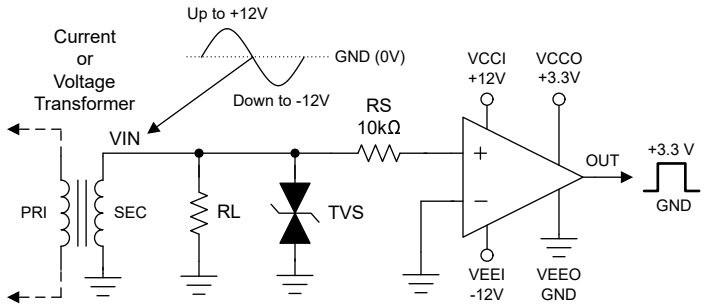


図 7-3. Bipolar Zero Cross Circuit using TLV187x

7.2.1.1 Design Requirements

表 7-2. Design Parameters

PARAMETER	VALUE
Supply Voltage	+3.3V, +12V and -12V
Input Voltage Range	Bipolar ±100mVp to ±12Vp
Threshold Level	0V (or GND)
Frequency Range	50 - 1000Hz
Logic Output Voltage	0 to 3.3V

7.2.1.2 Detailed Design Procedure

表 7-2 shows the requirements for the design. The input voltage is bipolar, ranging from ±100mV to ±12V, so split supplies on the comparator input are required.

RL is the required load resistance for the current or voltage transformer. The actual value is recommended by the transformer manufacturer.

RS limits the current into the ESD clamps when the comparator supplies are off and the AC signal can still be present from the transformer. All currents must be limited to 10mA or less (the less the better).

The TVS provides input protection against large transients that can pass through the transformer.

To accommodate the bipolar input range, the input supplies are set to VCCI = +12V, and VEEO = -12V. This allows for a full -12V to +12V input range.

The output supply is set to VCCO = +3.3V, and VEEO = GND for a 0 to 3.3V compatible logic output designed for direct input to a processor.

7.2.1.3 Application Performance Plots

図 7-4 shows the resulting output of the circuit. The output is high when the AC waveform is above ground, and low when the waveform is below ground.

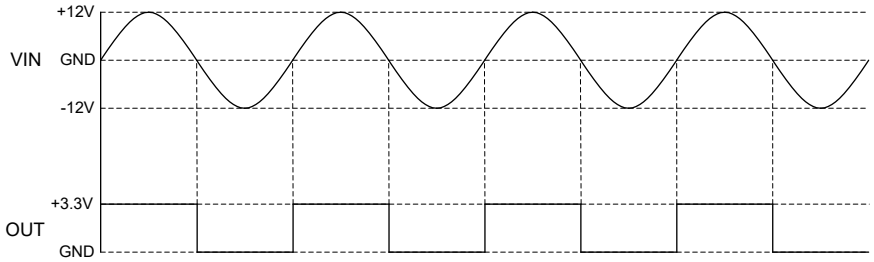


図 7-4. Typical Performance Plot for Zero-Cross Circuit

7.3 Power Supply Recommendations

Due to the fast output edges, proper bypass capacitors on the supply pin are critical to prevent supply ringing and false triggers and oscillations. Bypass the supply directly at *each* device with a low ESR 0.1µF ceramic SMT bypass capacitor as directly as possible between the supply pins and ground. Narrow peak currents are drawn during the output transition time due to the push-pull output device. These narrow pulses can cause poorly bypassed supply lines and poor grounds to ring, possibly causing common mode variations that can disturb the input voltage range and create an inaccurate comparison or even oscillations or false-triggers

For more information, please see the Separate Power Supplies section for more information.

7.4 Layout

7.4.1 Layout Guidelines

Accurate comparator applications must maintain a stable power supply with minimized noise and glitches. Output rise and fall times are in the tens of nanoseconds, and must be treated as high speed logic devices.

The bypass capacitors must be as close to the supply pin as possible and connected to a solid ground plane, and preferably directly between the VCCx or VEEx and GND pins. Pads need have two or more vias to minimize inductance to the power plane. Shared ground islands need multiple vias to the main ground plane.

Minimize coupling between outputs and inputs to prevent output oscillations. Do not run output and input traces in parallel unless there is a GND trace between output to reduce coupling. When series resistance is added to inputs (RIN), place resistor close to the device.

A low value (<100 ohms) resistor (ROUT) can be added in series with the output to dampen any ringing or reflections on long, non-impedance controlled traces. For best edge shapes, controlled impedance traces with back-terminations must be used when routing long distances.

7.4.2 Layout Example

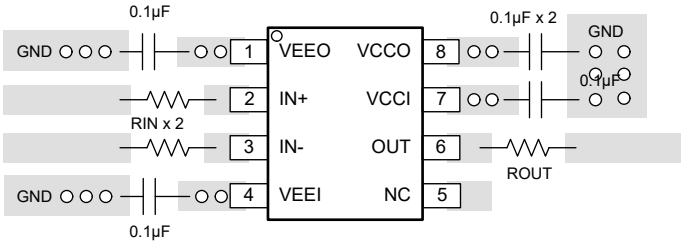


図 7-5. Layout Example

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

TLV1872 Evaluation Module - https://www.ti.com/tool/TLV1872EVM

Analog Engineers Circuit Cookbook: Amplifiers (See Comparators section) - SLYY137

Precision Design, Comparator with Hysteresis Reference Design— TIDU020

Window comparator circuit - SBOA221

Reference Design, Window Comparator Reference Design— TIPD178

Comparator with and without hysteresis circuit - SBOA219

Inverting comparator with hysteresis circuit - SNOA997

Non-Inverting Comparator With Hysteresis Circuit - SBOA313

A Quad of Independently Func Comparators - SNOA654

8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.3 サポート・リソース

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8.5 静電気放電に関する注意事項

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (March 2024) to Revision A (December 2024)	Page
• プレビュー タグを削除し、シングルの熱データを追加	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV1871DDFR	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3LDH
TLV1871DDFR.A	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3LDH
TLV1871DDFR.B	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3LDH
TLV1872DGSR	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	TL72
TLV1872DGSR.A	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	TL72

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

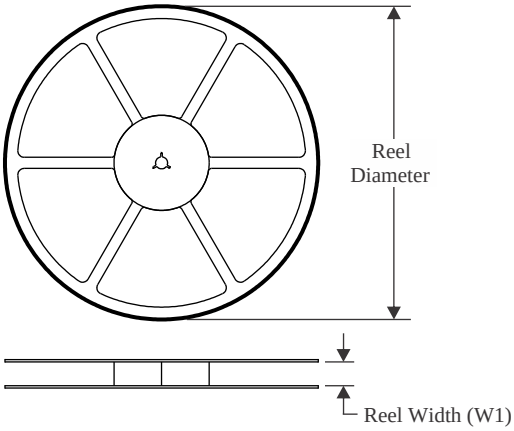
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

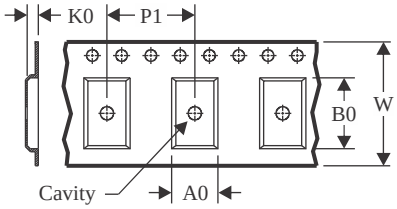
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

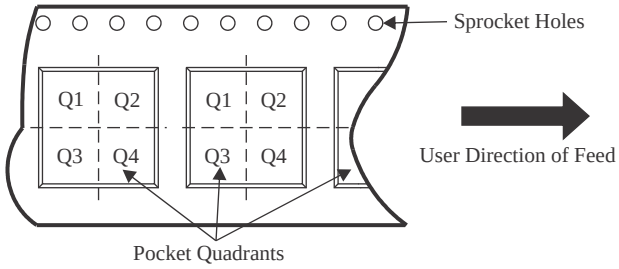


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

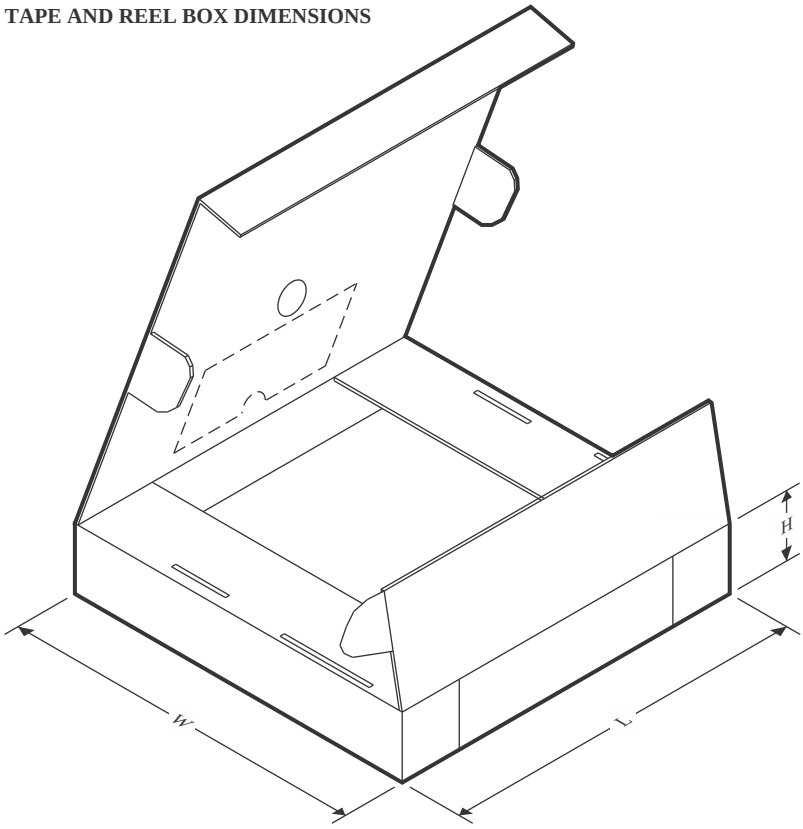
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV1871DDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV1872DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

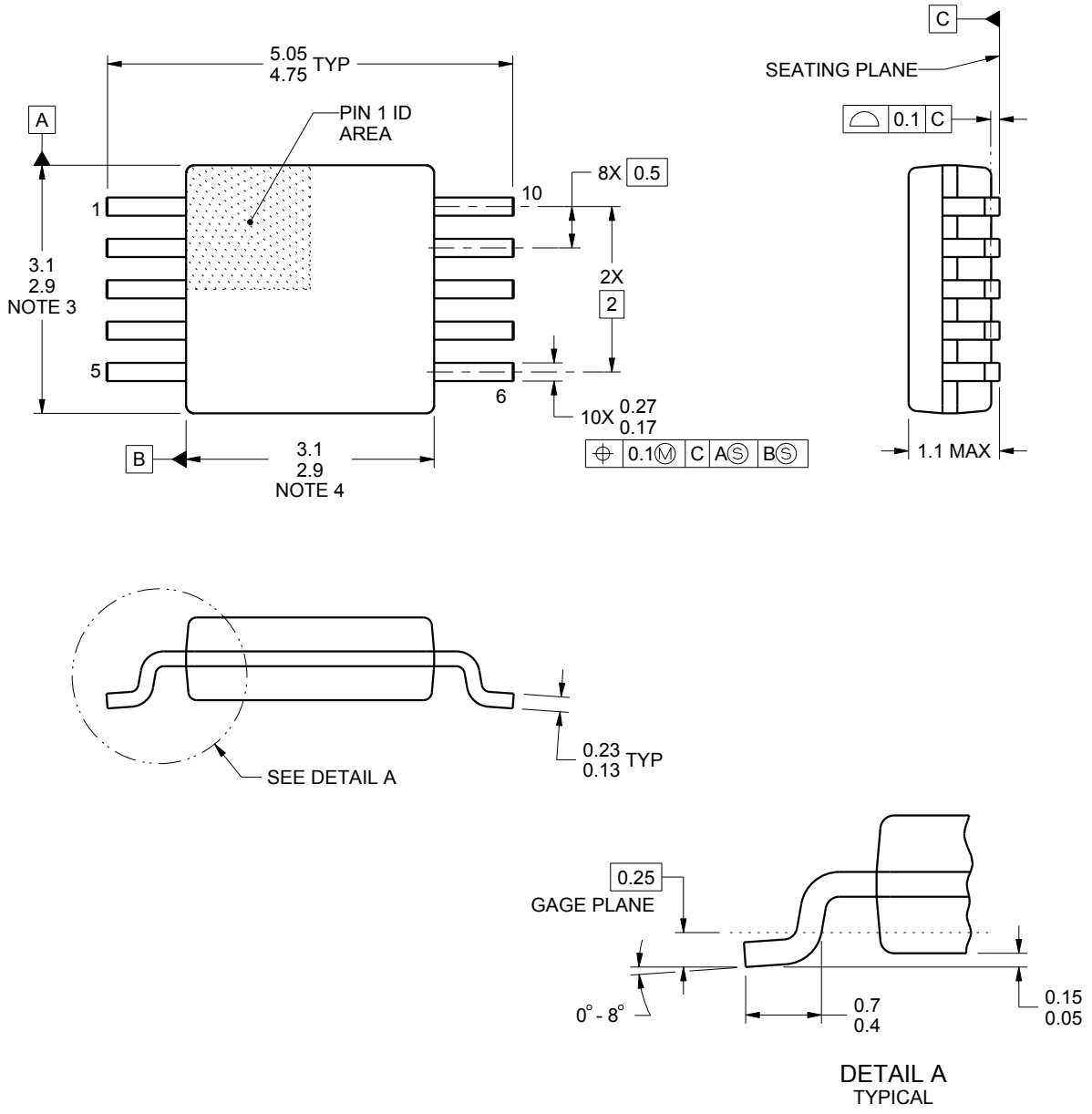
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV1871DDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TLV1872DGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0

PACKAGE OUTLINE

DGS0010A

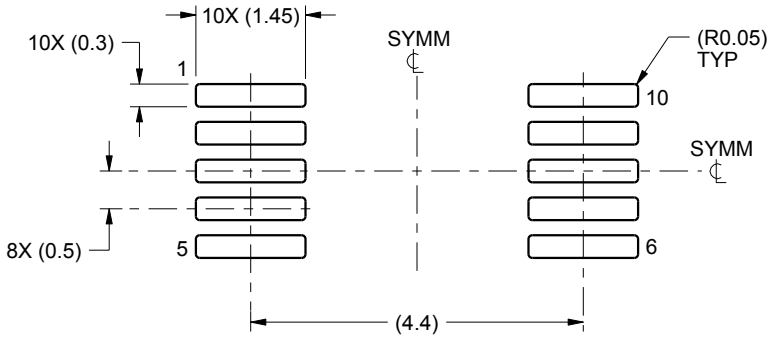
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

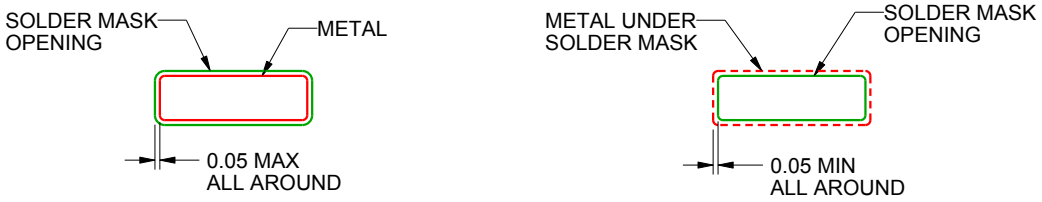


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

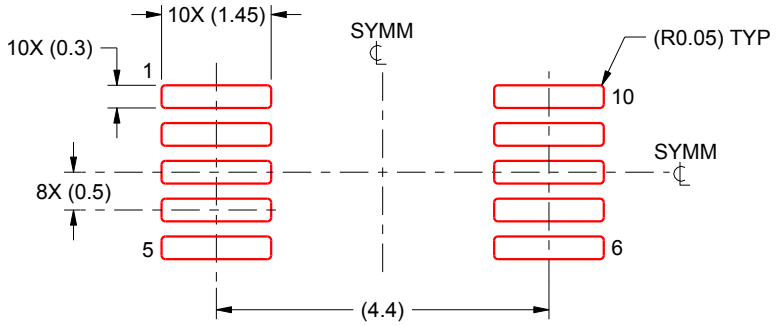


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

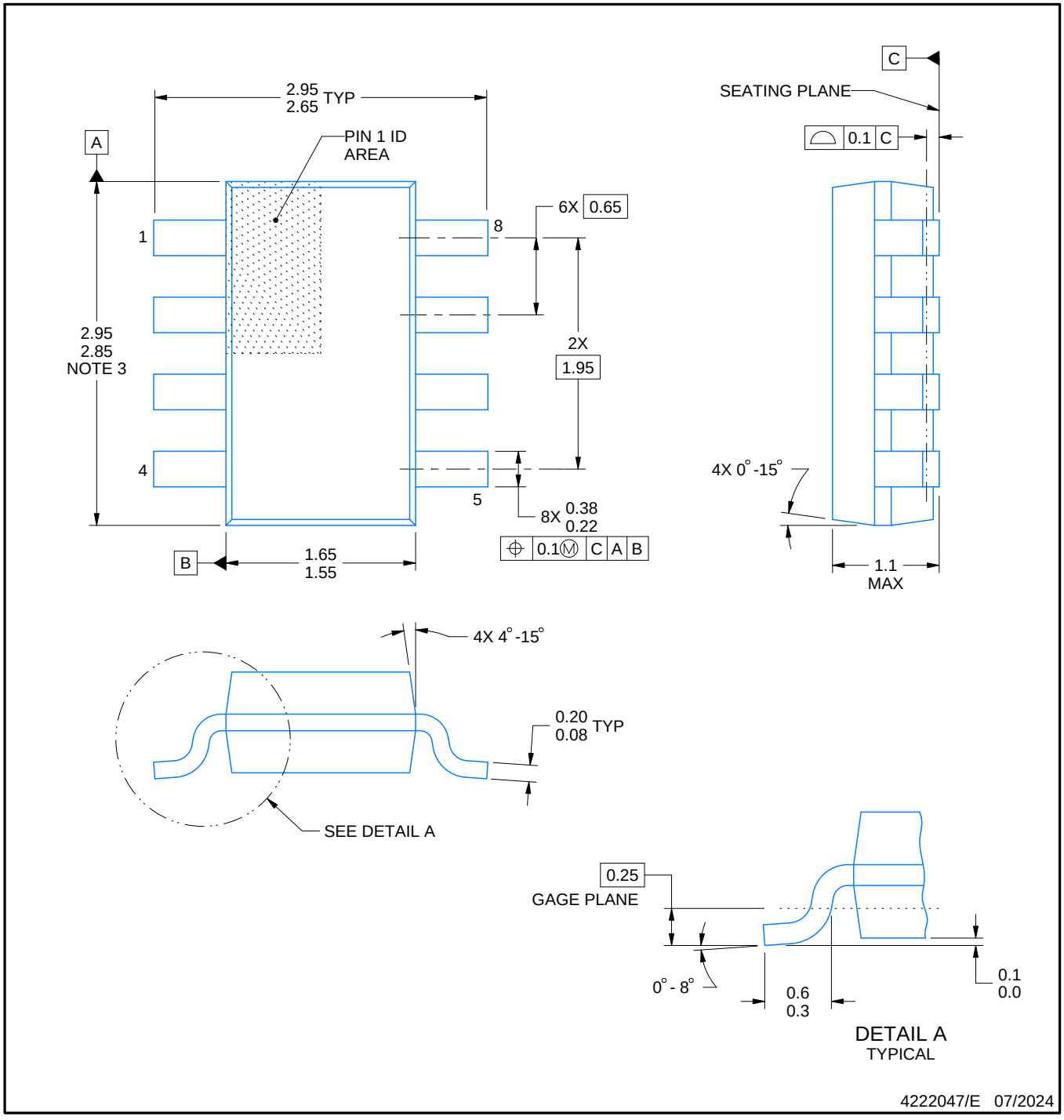
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DDF0008A

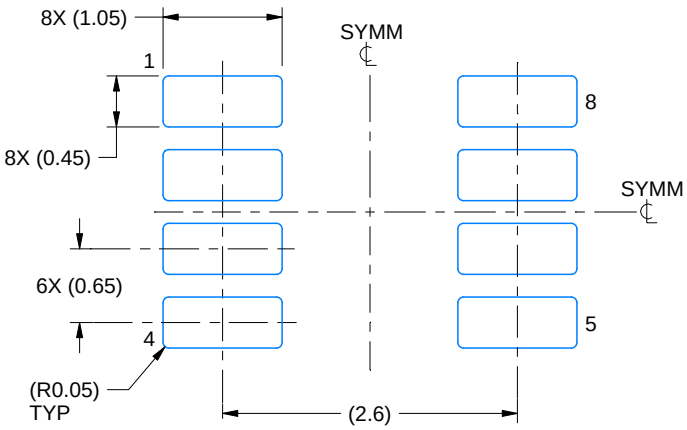
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

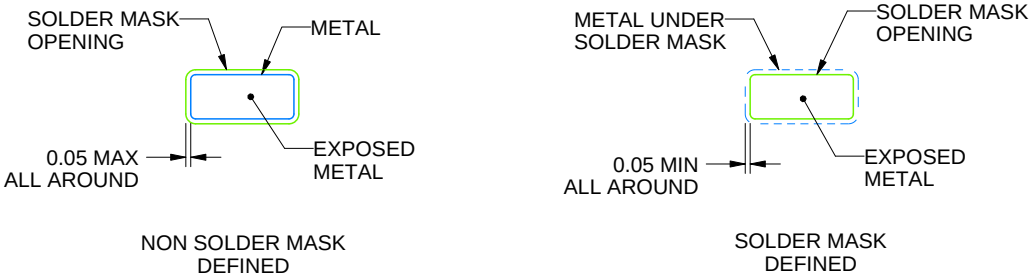


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4222047/E 07/2024

NOTES: (continued)

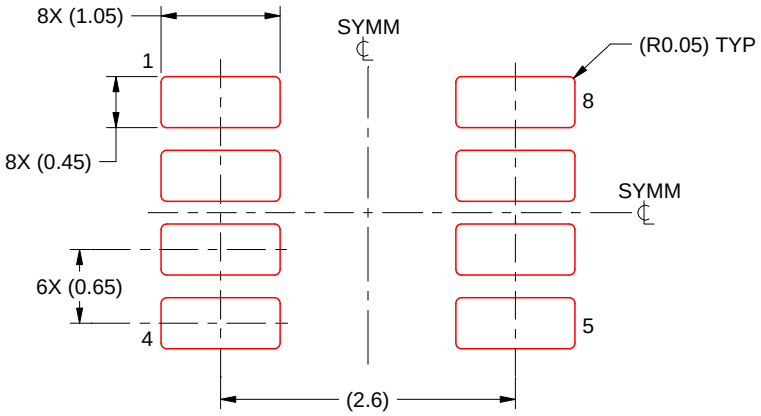
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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