TLV185x および TLV186x 40V ナノパワー コンパレータ ファミリ

1 特長

- 低い消費電流:チャネルあたり 440nA
- 幅広い電源電圧範囲:1.8V～40V
- レール上の入力: (V+) とは無関係に、同相範囲は (V-) + 40V まで
- フェイルセーフ:電源なしの高インピーダンス入力
- 既知の起動条件を提供するパワーオン リセット
- オーバードライブ入力についても位相反転なし
- 最高 40V までの逆バッテリ保護
- プッシュプル出力オプション (TLV185x)
- オープン ドレイン出力オプション (TLV186x)
- 温度範囲:-40℃～+125℃

2 アプリケーション

- 携帯電話、タブレット
- ヘッドセット / ヘッドホン、小型イヤホン
- PC、ノート PC
- ガス検出器
- 煙感知器、熱感知器
- モーション検出器
- ガス・メータ
- サーボ・ドライブ位置センサ

3 概要

TLV185x および TLV186x は、シングル、デュアル、クワッド チャネルのオプションがあるナノパワー 40V コンパレータ ファミリです。このファミリには、フェイルセーフ (FS) 入力と、プッシュプルおよびオープン ドレインの出力オプションがあります。これらの機能と、1.8V～40V の広い電源電圧範囲にわたるナノパワー動作により、このファミリは低消費電力の常時オン システムでの電圧および温度監視などのハウスキーピング機能に最適です。

どのデバイスもパワーオン リセット (POR) 機能を搭載しており、電源電圧が最小値に達するまでの間、出力が入力に応答する前に、出力が既知の状態であることが保証されるため、システムの電源オンおよび電源オフ時に誤った出力を防止できます。

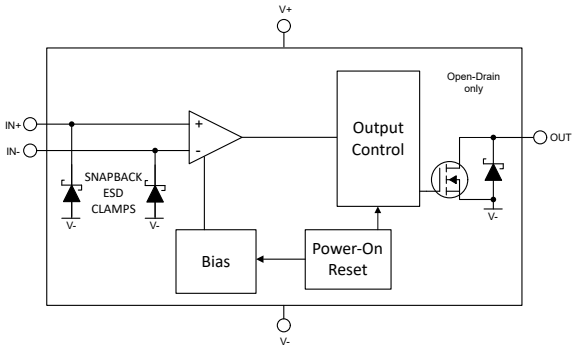
入力はオーバー ザ レール機能を備えており、両方の入力が最大 40 V の電源電圧を超えても正常に動作します。このため、このコンパレータは、比較可能な入力電圧の範囲を制限することなく、高電源電圧と低電源電圧の両方のシステムに適しています。同様に、内蔵の逆バッテリ保護機能により、電源ピンにバッテリが不適切に取り付けられた場合のコンパレータの損傷を防止します。

TLV185x コンパレータにはプッシュプル出力段があり、TLV186x コンパレータにはオープン ドレイン出力段があるため、レベル変換に適しています。

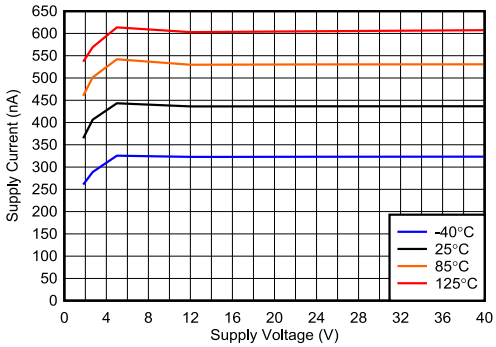
製品情報

部品番号	パッケージ (1)	本体サイズ (公称)(2)
TLV1851、TLV1861	SOT-23 (5)	1.60 mm × 2.90mm
TLV1852、TLV1862	VSSOP (8)	3.00mm × 3.00mm
TLV1854、TLV1864	TSSOP (14)	4.40 mm × 5.00mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



ブロック図



消費電流と電源電圧の関係

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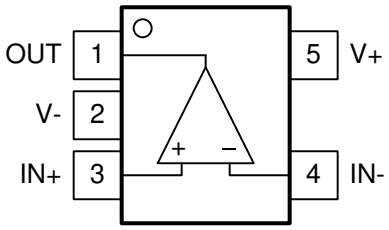
Pin Configuration: TLV1831 and TLV1841

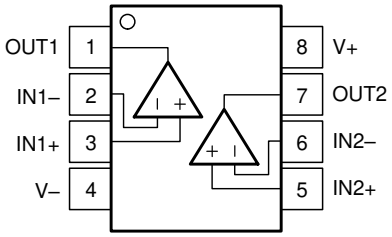


DBV, DCK Packages
SOT-23-5, SC-70-5
Top View
(Standard "north west" pinout)

表 4-1. Pin Functions: TLV1831 and TLV1841

PIN		I/O	DESCRIPTION
NAME	NO.		
OUT	1	O	Output
V-	2	-	Negative supply voltage
IN+	3	I	Non-inverting (+) input
IN-	4	I	Inverting (-) input
V+	5	-	Positive supply voltage

Pin Configurations: TLV1852 and TLV1862

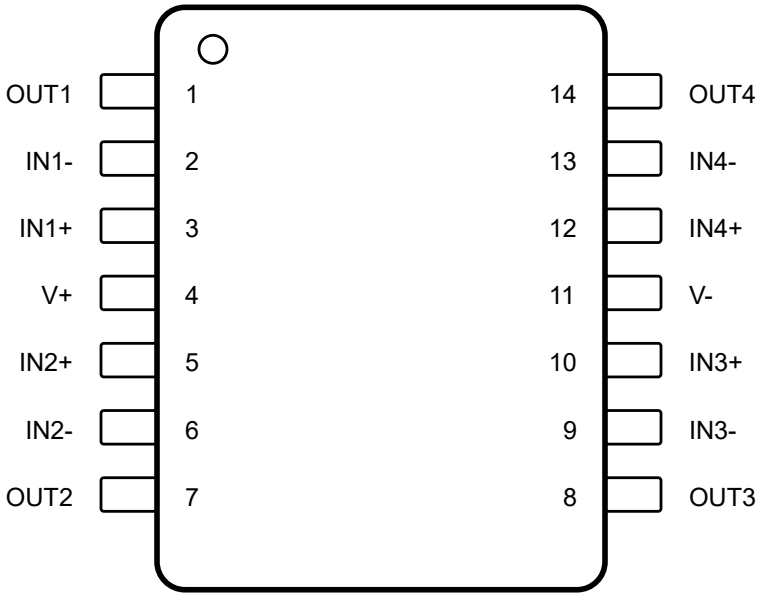


D, DGK Packages
8-Pin SOIC, VSSOP
Top View

表 4-2. Pin Functions: TLV1852 and TLV1862

PIN		I/O	DESCRIPTION
NAME	NO.		
OUT1	1	O	Output pin of the comparator 1
IN1–	2	I	Inverting input pin of comparator 1
IN1+	3	I	Noninverting input pin of comparator 1
V-	4	—	Negative supply voltage
IN2+	5	I	Noninverting input pin of comparator 2
IN2–	6	I	Inverting input pin of comparator 2
OUT2	7	O	Output pin of the comparator 2
V+	8	—	Positive supply voltage

Pin Configurations: TLV1854 and TLV1864



Not to scale

D, PW Packages
14-Pin SOIC, TSSOP
Top View

表 4-3. Pin Functions: TLV1854 and TLV1864

PIN		I/O	DESCRIPTION
NAME	NO.		
OUT1	1	O	Output pin of the comparator 1
IN1-	2	I	Negative input pin of the comparator 1
IN1+	3	I	Positive input pin of the comparator 1
V+	4	-	Positive supply voltage
IN2+	5	I	Positive input pin of the comparator 2
IN2-	6	I	Negative input pin of the comparator 2
OUT2	7	O	Output pin of the comparator 2
OUT3	8	O	Output pin of the comparator 3
IN3-	9	I	Negative input pin of the comparator 3
IN3+	10	I	Positive input pin of the comparator 3
V-	11	-	Negative supply voltage
IN4+	12	I	Positive input pin of the comparator 4
IN4-	13	I	Negative input pin of the comparator 4
OUT4	14	O	Output pin of the comparator 4

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage: V_S = (V+) – (V–)		42	V
Differential Input Voltage, VID	–42	42	V
Input pins (IN+, IN–) from (V–)(2)	–0.3	42	V
Current into Input pins (IN+, IN–)(3)	–10	10	mA
Output (Open-drain version only) from (V–)(4)	–0.3	42	V
Output (OUT) (Push-Pull) from (V–)	–0.3	(V+) + 0.3	V
Output short circuit current(5)	-10	10	mA
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to (V–). Inputs (IN+, IN–) can be greater than (V+) and OUT as long as it is within the –0.3V to 42V range
(3) Input terminals are diode-clamped to (V–). Input signals that swing more than 0.3 V below (V–) must be current-limited to 10mA or less.
(4) Output (OUT) for open drain can be greater than (V+) and inputs (IN+, IN–) as long as it is within the –0.3V to 42V range
(5) Short-circuit to (V–) or (V+).

5.2 ESD Ratings

			VALUE	UNIT
TLV1851, TLV1861				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1500	V
TLV1852, TLV1862				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	V
TLV1854, TLV1864				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±750	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Thermal Information

THERMAL METRIC[1]		TLV185x/6x			UNIT
		DBV (SOT-23)	DGK (VSSOP)	PW (TSSOP)	
		5 Pins	8 Pins	14 Pins	
R_{qJA}	Junction-to-ambient thermal resistance	168.1	163.1	94.2	°C/W
$R_{qJC(top)}$	Junction-to-case (top) thermal resistance	68.1	55.5	29	°C/W
R_{qJB}	Junction-to-board thermal resistance	37.4	84.7	51.8	°C/W
y_{JT}	Junction-to-top characterization parameter	11.4	5.7	1.3	°C/W
y_{JB}	Junction-to-board characterization parameter	37.1	83.1	51.1	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage: V_S = (V+) – (V–)	1.8	40	V
Input voltage range from (V–)	–0.1	40	V
Common-mode input voltage range from (V–)	0	40	V
Output voltage for open drain from (V–)	–0.1	40	V
Ambient temperature, T_A	–40	125	°C

5.5 Electrical Characteristics

For V_S = (V+) – (V–) = 12V, V_{CM} = V_S/2 at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage		–3.6	±0.25	3.6	mV
V_{OS}	Input offset voltage	T_A = –40°C to +125°C	–4.4		4.4	mV
dV_{IO}/dT	Input offset voltage drift			3		µV/°C
V_{HYS}	Input hysteresis voltage		1	2.8	5	mV
$V_{CM-Range}$	Common-mode voltage range from (V–)	V_S = 1.8V to 40V T_A = –40°C to +125°C	0		40	V
POWER SUPPLY						
I_Q	Quiescent current per comparator (output high)	Push Pull Output Option		520	750	nA
I_Q	Quiescent current per comparator (output high)	Push Pull Output Option, T_A = –40°C to 125°C			1000	nA
I_Q	Quiescent current per comparator (output high)	Open Drain Output option, no pull-up resistor		440	640	nA
I_Q	Quiescent current per comparator (output high)	Open Drain Output option, no pull-up resistor, T_A = –40°C to 125°C			850	nA
V_{POR}		During power on, VS must exceed V_{POR} for t_{ON} before the output will reflect the input.		1.5		V
INPUT BIAS CURRENT						
I_B	Input bias current (1)			1	250	pA
		T_A = –40°C to +125°C			1500	pA
I_{OS}	Input offset current (1)			0.1	100	pA
		T_A = –40°C to +125°C			1000	pA
OUTPUT						
V_{OL}	Voltage swing from (V–)	I_{SINK} = 2µA		1		mV
V_{OL}	Voltage swing from (V–)	I_{SINK} = 50µA		20	60	mV
		I_{SINK} = 50µA T_A = –40°C to +125°C			100	mV
V_{OH}	Voltage swing from (V+) (Push Pull only)	I_{SOURCE} = 2µA		1		mV
V_{OH}	Voltage swing from (V+) (Push Pull only)	I_{SOURCE} = 50µA		25	60	mV
		I_{SOURCE} = 50µA T_A = –40°C to +125°C			100	mV
I_{LKG}	Open-drain output leakage current	V_{ID} = +0.1V, V_{PULLUP} = (V+)		0.3		pA
I_{OL}	Short-circuit current	Sinking T_A = –40°C to +125°C		7		mA

5.5 Electrical Characteristics (続き)

For V_S = (V+) – (V–) = 12V, V_{CM} = V_S/2 at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OH}	Short-circuit current	Sourcing (for Push-Pull only) T_A = –40°C to +125°C		5		mA

(1) This parameter is ensured by design and/or characterization and is not tested in production.

5.6 Switching Characteristics

For V_S = (V+) – (V–) = 12V, V_{CM} = V_S / 2 at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
T_{PD-HL}	Propagation delay time, high-to-low	V_{OD} = 10mV, C_L = 25pF, V_{STEP} = 100mV		45		µs
		V_{OD} = 50mV, C_L = 25pF, V_{STEP} = 100mV		16		µs
		V_{OD} = 100mV, C_L = 25pF, V_{STEP} = 200mV		13		µs
T_{PD-LH}	Propagation delay time, low-to-high (Push-Pull output)	V_{OD} = 10mV, C_L = 10pF, V_{STEP} = 100mV		34		µs
T_{PD-LH}	Propagation delay time, low-to-high (Push-Pull output)	V_{OD} = 50mV, C_L = 10pF, V_{STEP} = 100mV		16		µs
T_{PD-LH}	Propagation delay time, low-to-high (Push-Pull output)	V_{OD} = 100mV, C_L = 10pF, V_{STEP} = 200mV		14		µs
T_{PD-LH}	Propagation delay time, low-to-high (Open-Drain output)	V_{OD} = 10mV, C_L = 25pF, R_P = 1MΩ, V_{STEP} = 100mV		57		µs
		V_{OD} = 50mV, C_L = 25pF, R_P = 1MΩ, V_{STEP} = 100mV		36		µs
		V_{OD} = 100mV, C_L = 25pF, R_P = 1MΩ, V_{STEP} = 200mV		35		µs
T_{RISE}	Output Rise Time, 20% to 80%, push-pull output	C_L = 25pF		0.2		µs
T_{FALL}	Output Fall Time, 80% to 20%	C_L = 25pF		0.2		µs
POWER ON TIME						
T_{ON}	Power on-time			3		ms

5.7 Typical Characteristics

At T_A = 25°C, V_S = 12V, VCM = V_S/2 V, R_P = 1MΩ (Open Drain only), C_L = 25pF, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

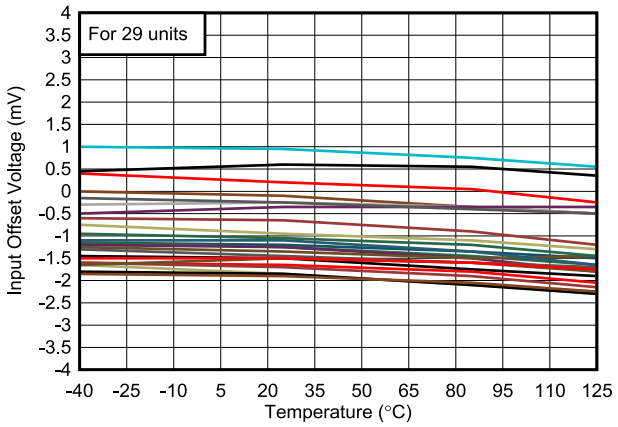


図 5-1. Offset vs. Temperature

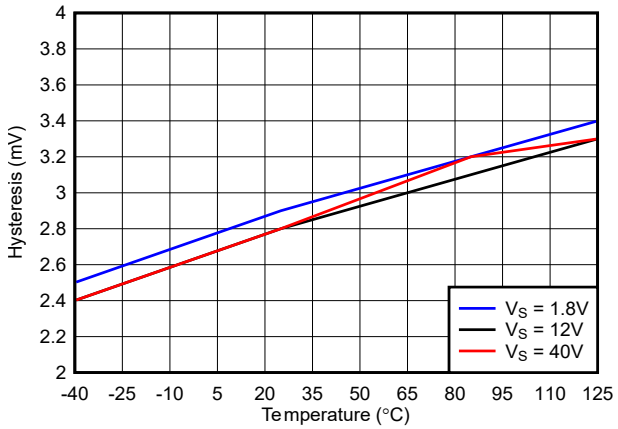


図 5-2. Hysteresis vs. Temperature

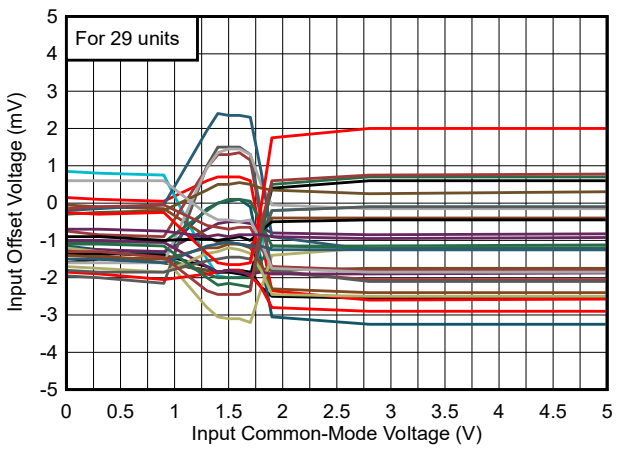


図 5-3. Offset vs. Common-Mode, 1.8V

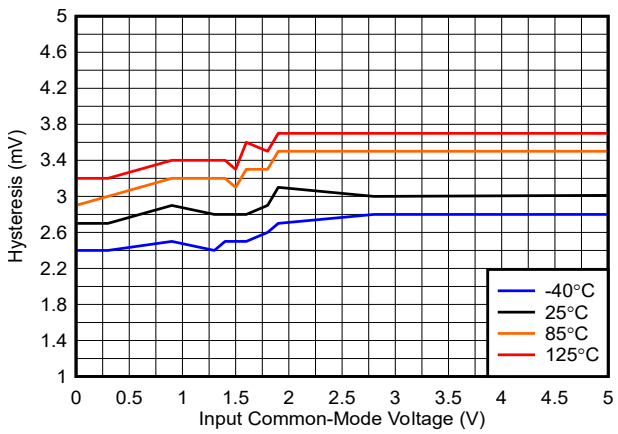


図 5-4. Hysteresis vs. Common-Mode, 1.8V

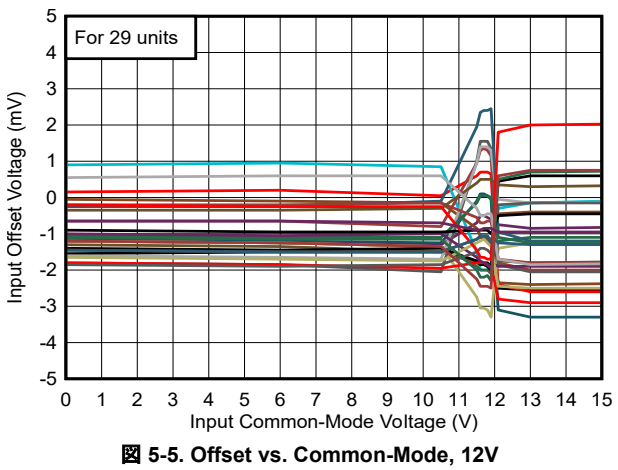


図 5-5. Offset vs. Common-Mode, 12V

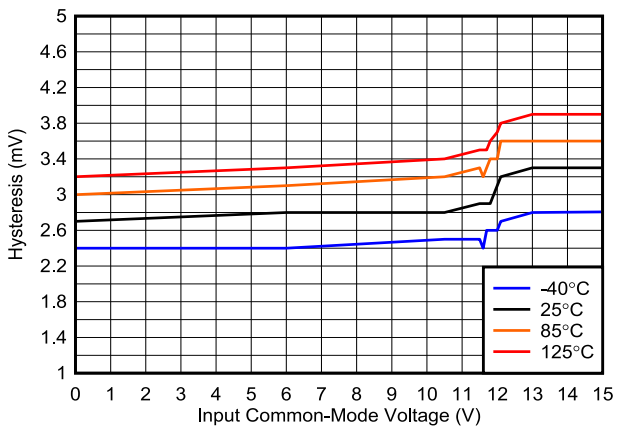


図 5-6. Hysteresis vs. Common-Mode, 12V

5.7 Typical Characteristics (continued)

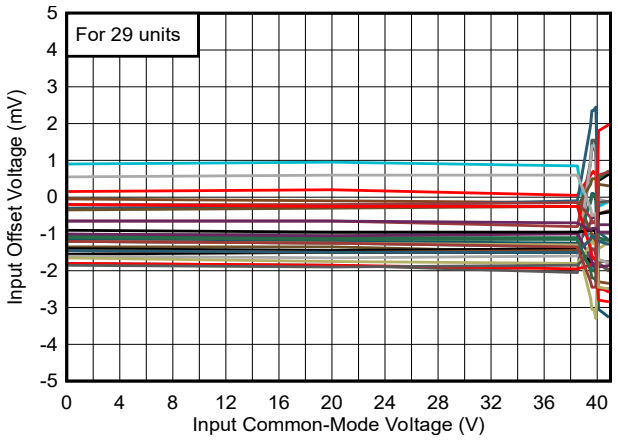


図 5-7. Offset vs. Common-Mode, 40V

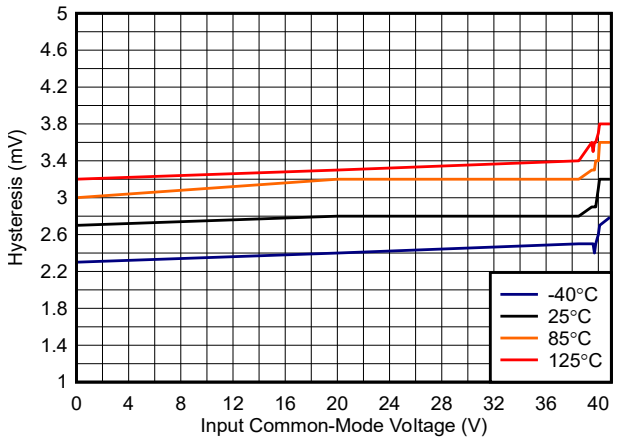


図 5-8. Hysteresis vs. Common-Mode, 40V

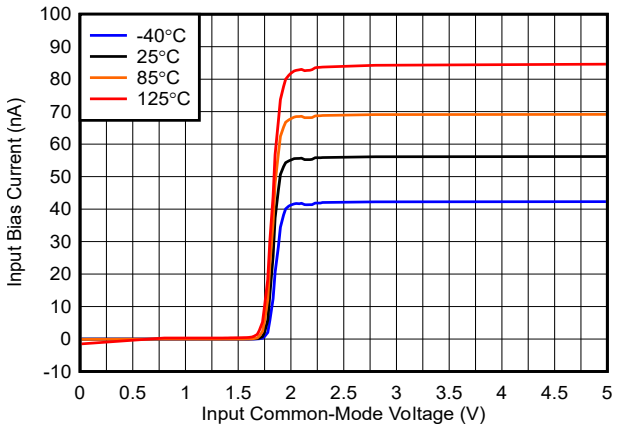


図 5-9. Bias Current vs. Common-Mode, 1.8V

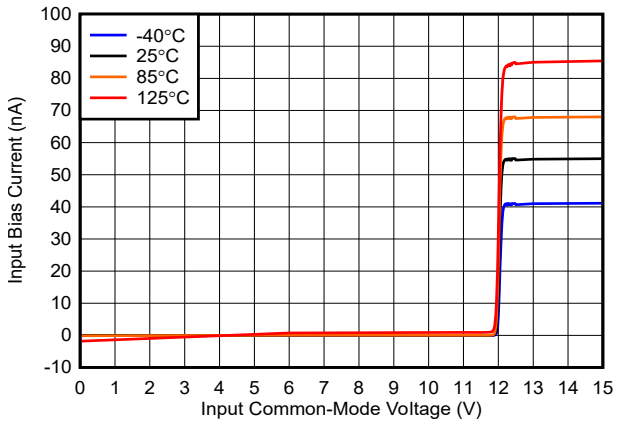


図 5-10. Bias Current vs. Common-Mode, 12V

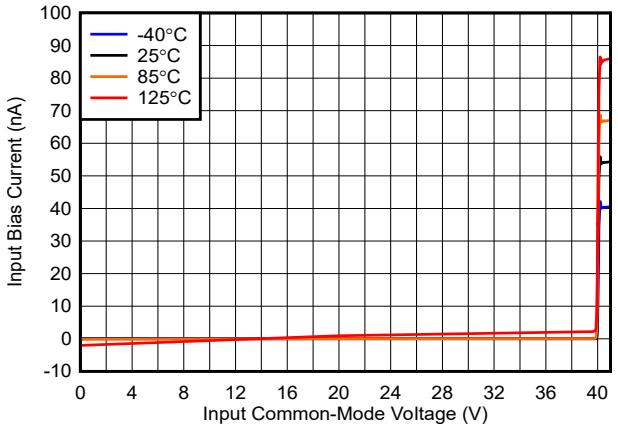


図 5-11. Bias Current vs. Common-Mode, 40V

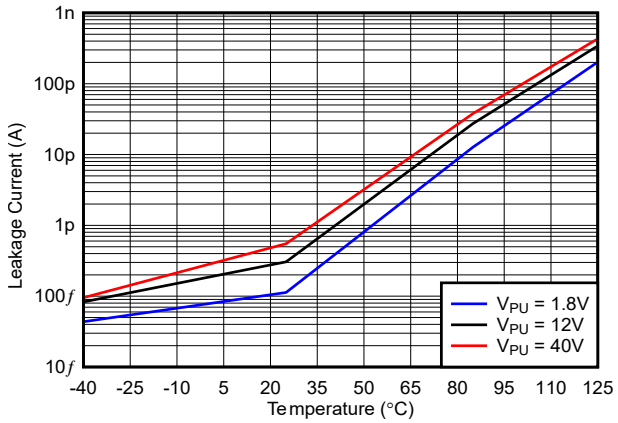


図 5-12. Leakage Current vs. Temperature (Open Drain only)

5.7 Typical Characteristics (continued)

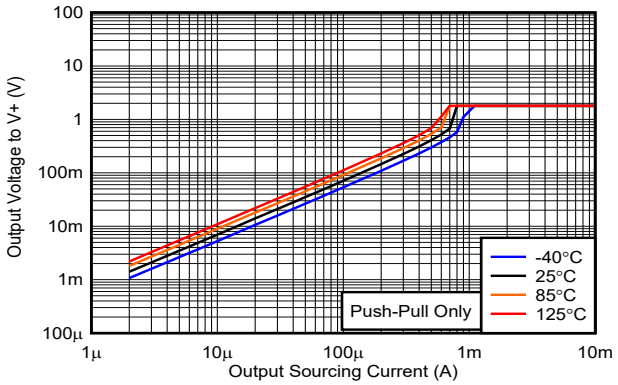


図 5-13. Output Voltage vs. Output Sourcing Current, 1.8V

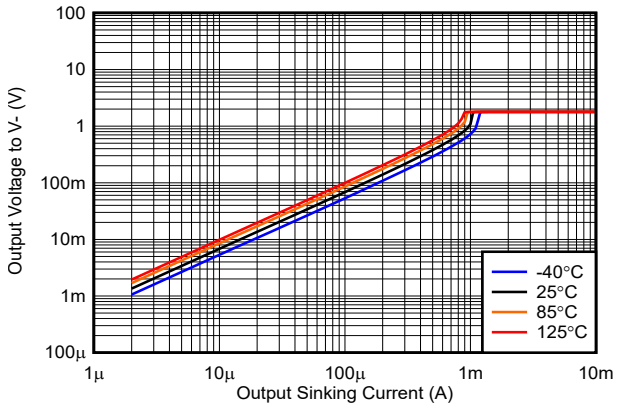


図 5-14. Output Voltage vs. Output Sinking Current, 1.8V

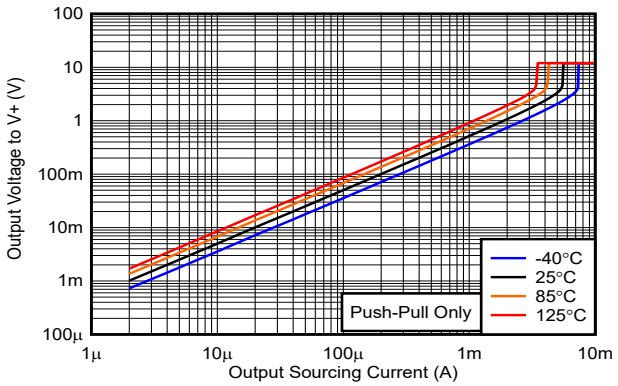


図 5-15. Output Voltage vs. Output Sourcing Current, 12V

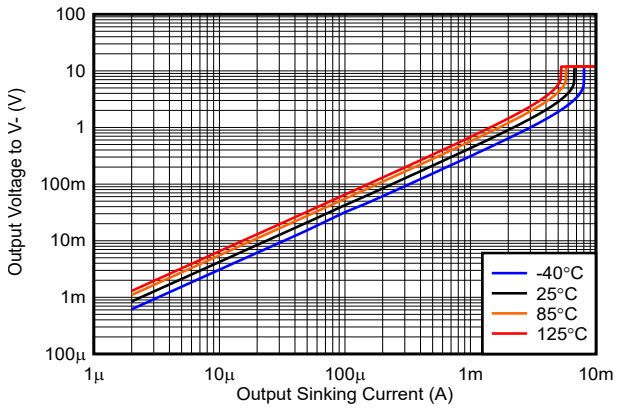


図 5-16. Output Voltage vs. Output Sinking Current, 12V

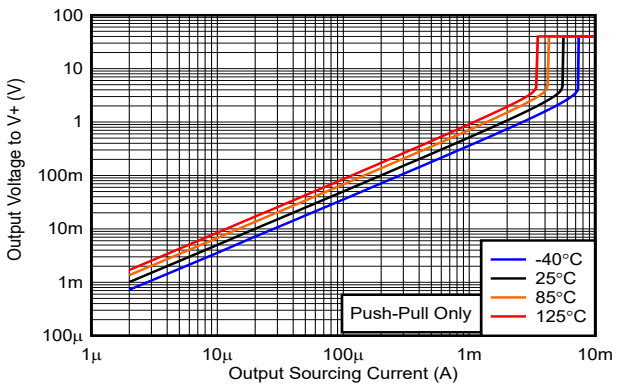


図 5-17. Output Voltage vs. Output Sourcing Current, 40V

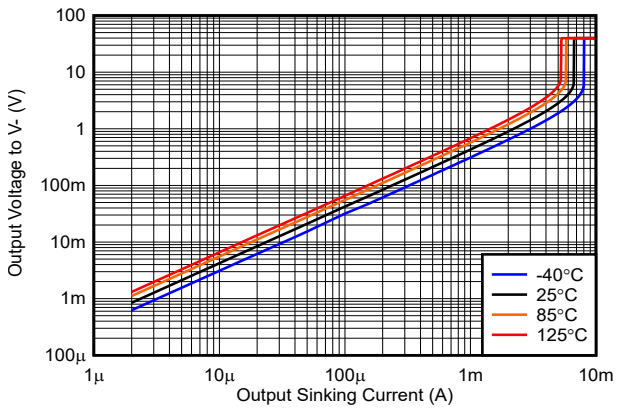


図 5-18. Output Voltage vs. Output Sinking Current, 40V

5.7 Typical Characteristics (continued)

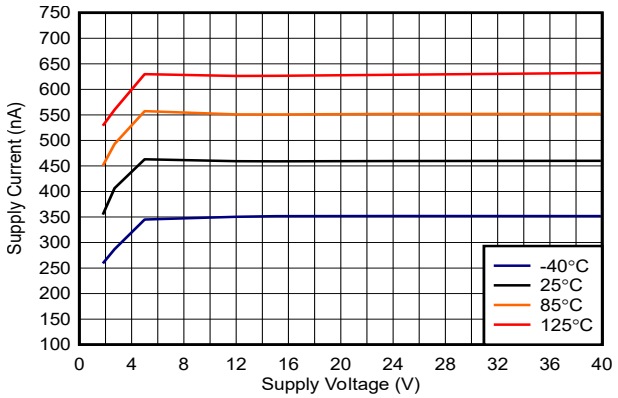


図 5-19. Supply Current vs. Supply Voltage (Output Low), Push-Pull

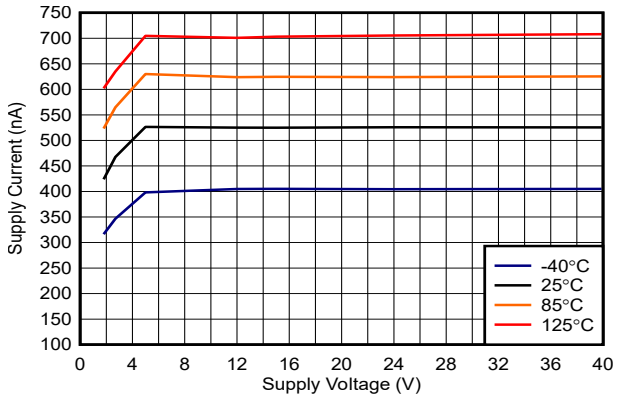


図 5-20. Supply Current vs. Supply Voltage (Output High), Push-Pull

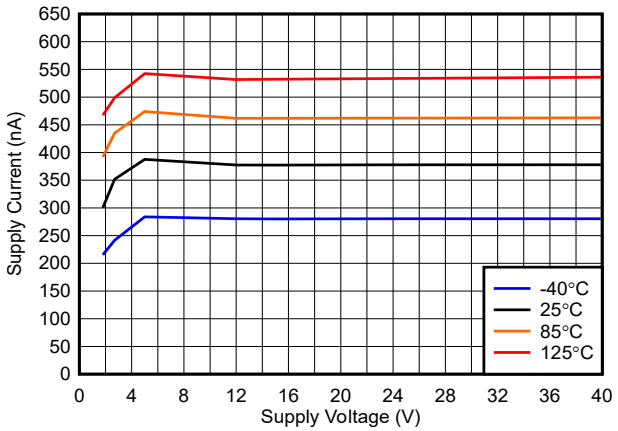


図 5-21. Supply Current vs. Supply Voltage (Output Low), Open Drain

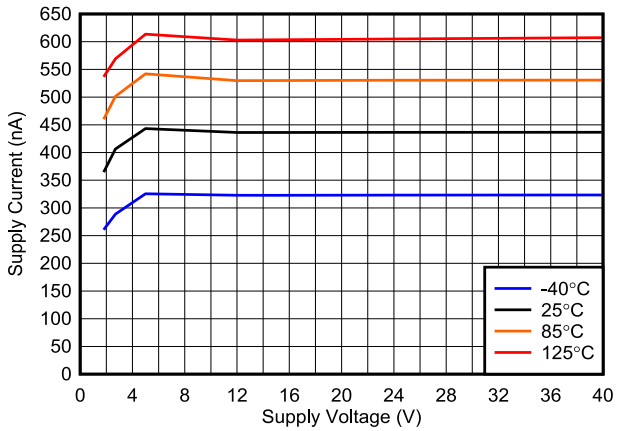


図 5-22. Supply Current vs. Supply Voltage (Output High), Open Drain

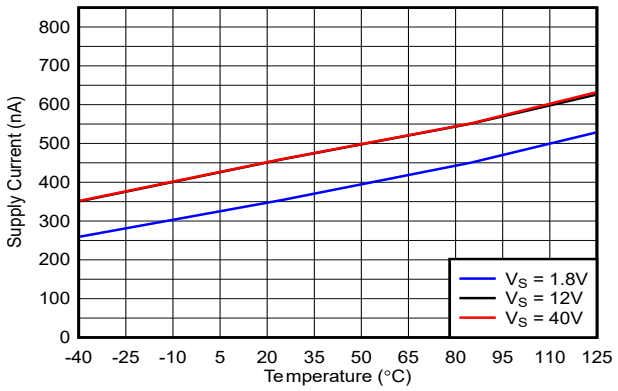


図 5-23. Supply Current vs. Temperature (Output Low), Push-Pull

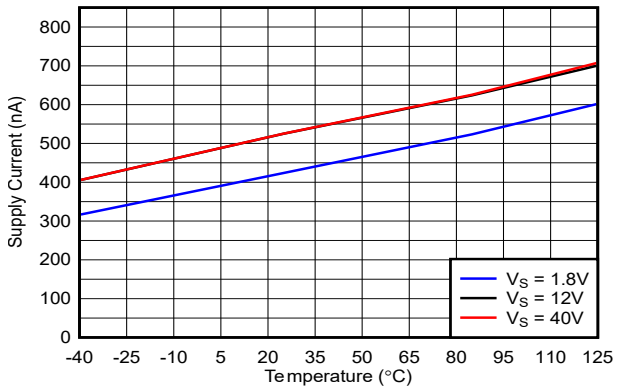


図 5-24. Supply Current vs. Temperature (Output High), Push-Pull

5.7 Typical Characteristics (continued)

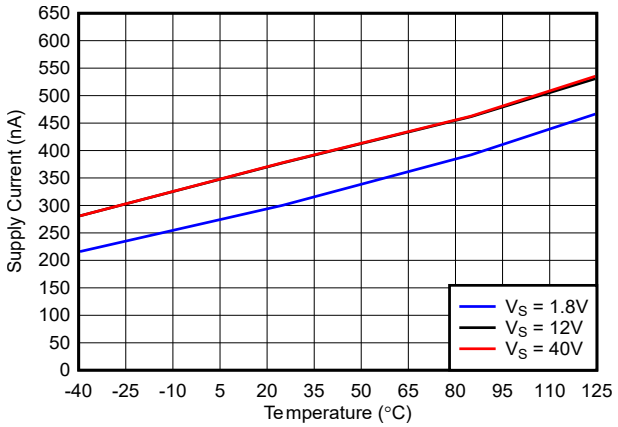


図 5-25. Supply Current vs. Temperature (Output Low), Open Drain

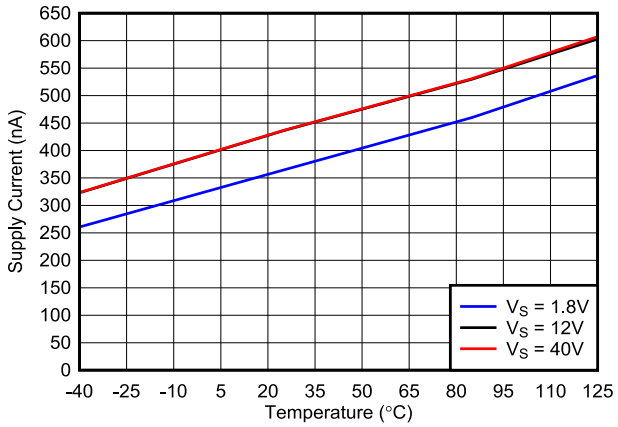


図 5-26. Supply Current vs. Temperature (Output High), Open Drain

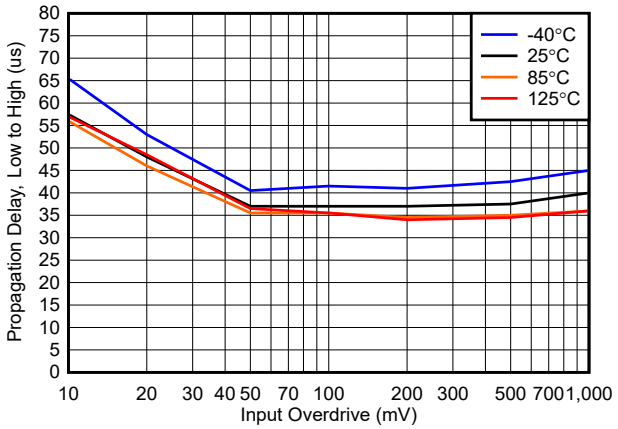


図 5-27. Propagation Delay, Low to High, 1.8V, Open Drain

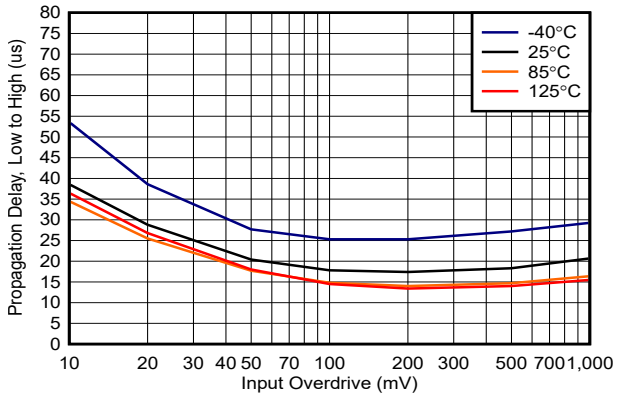


図 5-28. Propagation Delay, Low to High, 1.8V, Push-Pull

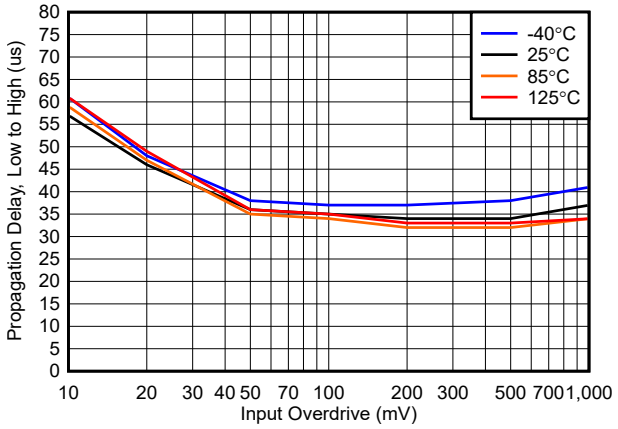


図 5-29. Propagation Delay, Low to High, 12V, Open Drain

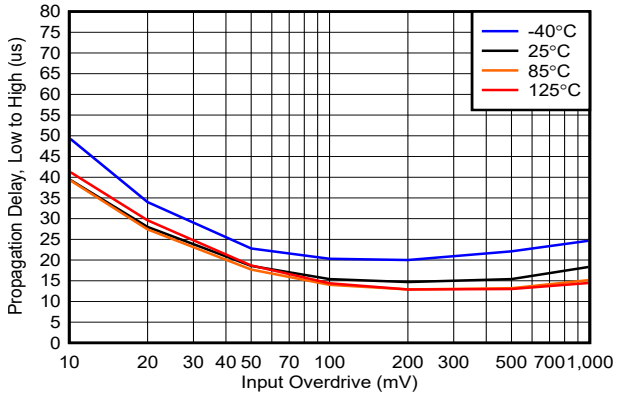


図 5-30. Propagation Delay, Low to High, 12V, Push-Pull

5.7 Typical Characteristics (continued)

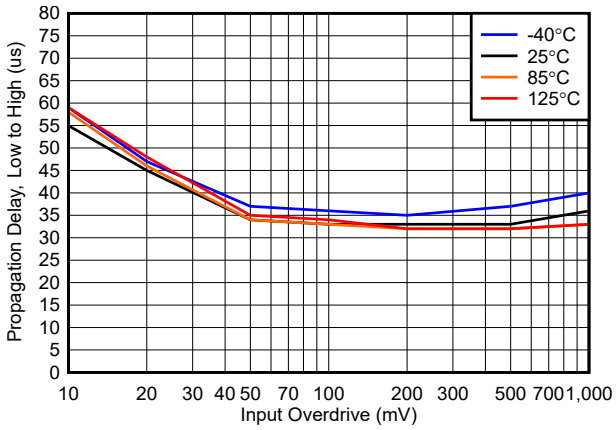


図 5-31. Propagation Delay, Low to High, 40V, Open Drain

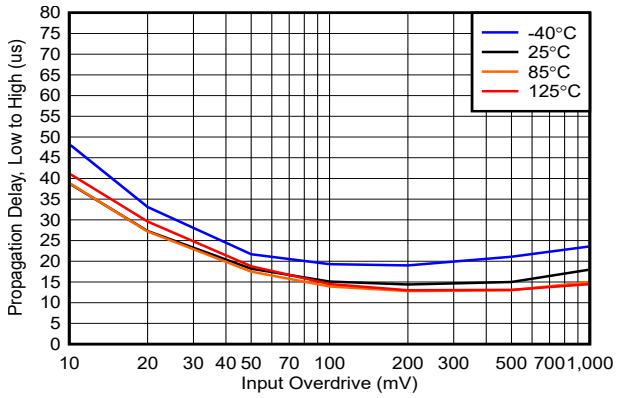


図 5-32. Propagation Delay, Low to High, 40V, Push-Pull

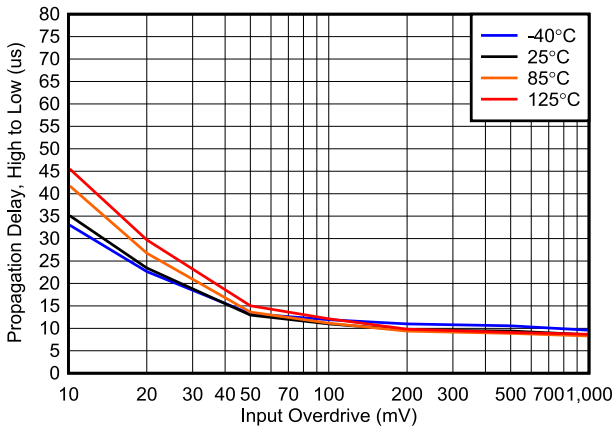


図 5-33. Propagation Delay, High to Low, 1.8V

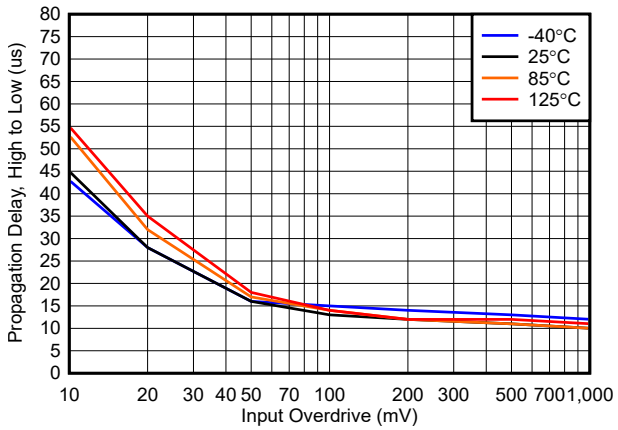


図 5-34. Propagation Delay, High to Low, 12V

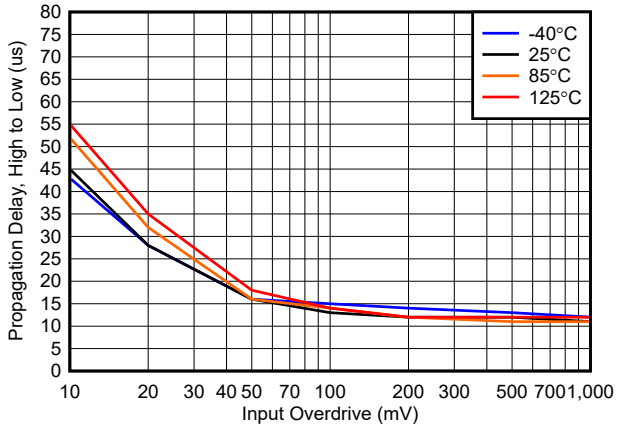


図 5-35. Propagation Delay, High to Low, 40V

6 Detailed Description

6.1 Overview

The TLV185x and TLV186x devices are nanopower comparators with push-pull and open-drain output options. Operating down to 1.8V while only consuming only 440nA per channel, the TLV185x and TLV186x are well suited for voltage, current, and temperature sensing in low and high voltage low-power, always-on systems. An internal power-on reset circuit ensures that the output remains in a known state during power-up and power-down. Inputs have fail-safe inputs that can tolerate input transients without damage or false outputs.

6.2 Functional Block Diagrams

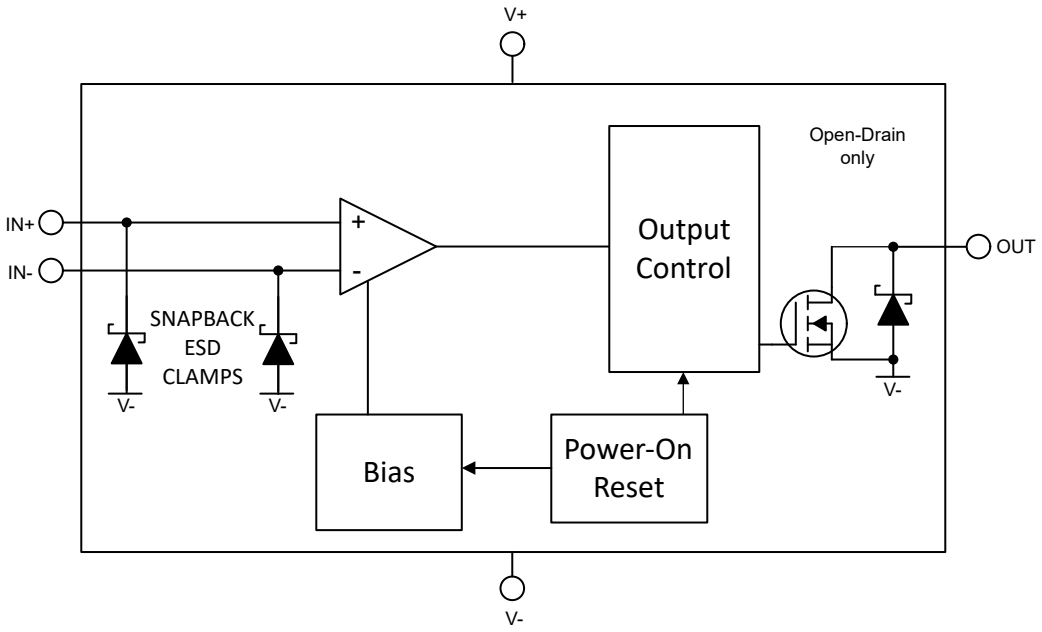


図 6-1. Block Diagram

6.3 Feature Description

The TLV185x (push-pull output) and TLV186x (open-drain output) devices are nano-power comparators that are capable of operating at high voltages. This family of comparators feature a fail safe input stage and over the rail operating condition mode capable of operating up to 40V, independent of V+. The comparators also have an internal reverse battery protection feature and Power-On-Reset for known start-up conditions.

6.4 Device Functional Modes

6.4.1 Inputs

6.4.1.1 Operating Common-Mode Ranges

The TLV185x and TLV186x devices have two operating common-mode ranges: within-the-rail and over-the-rail.

Within-the-Rail Operation: IN+ and IN- are less than (V+)

When an input pin is operating less than (V+), there are two operating regions defined where input voltages can be compared: low common-mode and high-common mode. In low-common mode which extends typically from 0V to (V+) - 1V, the typical input bias current is less than 1pA. In high common-mode which extends typically from (V+) - 1V to (V+), the typical input bias current is less than 14nA.

Over-the-Rail Operation: IN+ and/or IN- are greater than (V+)

The TLV185x and TLV186x devices have a distinctive input stage that allows the input common mode range to extend from 0V to 40V independent of the supply voltage. This feature means that operation at low supply

voltages does not limit the range of input voltages that can be compared. When an input pin is operating over-the-rail (above (V+)), the bias current increases to a typical value of 55nA.

See Figure 6-9 to 6-11 in the Typical Characteristics section for input bias current vs. common-mode voltages.

6.4.1.2 Fail-Safe Inputs

A feature of the TLV185x and TLV186x family is that the inputs are fail safe up to 40V, independent of (V+). The inputs are maintained as high input impedance and can be of any value between -0.1V and 40V, even while (V+) is unpowered or below the minimum supply voltage. This feature avoids power sequencing or transient issues since the inputs are not diode clamped to (V+).

6.4.1.3 Unused Inputs

If a channel is not to be used, DO NOT tie the inputs together. Due to the high equivalent bandwidth and low offset voltage, tying the inputs directly together can cause high frequency oscillations as the device triggers on it's own internal wideband noise. Instead, the inputs should be tied to any available voltage that resides within the specified input voltage range and provides a minimum of 50mV differential voltage. For example, one input can be grounded and the other input connected to a reference voltage, or even (V+).

6.4.2 Internal Hysteresis

The device hysteresis transfer curve is shown in 図 6-2. This curve is a function of three components: V_{TH}, V_{OS}, and V_{HYST}:

- V_{TH} is the actual set voltage or threshold trip voltage.
- V_{OS} is the internal offset voltage between V_{IN+} and $V_{IN–}$. This voltage is added to V_{TH} to form the actual trip point at which the comparator must respond to change output states.
- V_{HYST} is the internal hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise.

  (2.8 mV for the TLV185x/6x family)

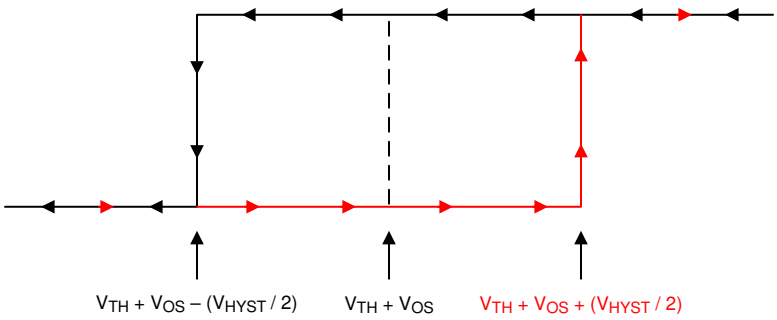


図 6-2. Hysteresis Transfer Curve

6.4.3 Outputs

6.4.3.1 TLV185x Push-Pull Output

The TLV185x features a push-pull output stage capable of both sinking and sourcing current. This allows driving loads such as LED's and MOSFET gates, as well as eliminating the need for a power-wasting external pull-up resistor. The push-pull output must never be connected to another output.

Directly shorting the output to the supply rails ((V+) when output "low" or (V-) when output "High") can result in thermal runaway and eventual device destruction at high (>12V) supply voltages. If output shorts are possible, a series current limiting resistor is recommended to limit the power dissipation.

Unused push-pull outputs should be left floating, and never tied to a supply, ground, or another output.

6.4.3.2 TLV186x Open-Drain Output

The TLV186x features an open-drain (also commonly called open collector) sinking-only output stage enabling the output logic levels to be pulled up to an external voltage from 0V up to 40V, independent of the comparator

supply voltage (V+). The open-drain output also allows logical OR'ing of multiple open drain outputs and logic level translation. TI recommends setting the pull-up resistor current to less than 100uA to optimize V_{OL} logic levels. Lower pull-up resistor values will help increase the rising edge risetime, but at the expense of increasing V_{OL} and higher power dissipation. The risetime will be dependent on the time constant of the total pull-up resistance and total load capacitance. Large value pull-up resistors (>1MΩ) will create an exponential rising edge due to the output RC time constant and increase the risetime.

Directly shorting the output to (V+) can result in thermal runaway and eventual device destruction at high (>12V) pull-up voltages. If output shorts are possible, a series current limitng resistor is recommended to limit the power dissipation.

Unused open drain outputs should be left floating, or can be tied to the (V-) pin if floating pins are not desired.

6.4.4 ESD Protection

6.4.4.1 Inputs

The fail-safe inputs incorporates internal ESD protection circuits on all pins. The fail-safe inputs have ESD protection from each pin to (V-) which allows these pins to exceed the supply voltage (V+) up to 40V. If input voltages are to exceed 40V, an external clamp would be required. Likewise, negative voltages on the inputs are ESD clamped to (V-) and should be limited to less than -0.1V.

If the inputs are to be connected to a low impedance source, such as a power supply or buffered reference line, TI recommends adding a current-limiting resistor in series with the input to limit any transient currents should the clamps conduct. The current should be limited to 10mA or less. This series resistance can be part of any resistive input dividers or networks.

6.4.4.2 Outputs

The TLV185x push-pull output protection also contains a conventional diode-type ESD clamps between the output and (V-), as the output should not exceed the supply rails.

The TLV186x open-drain output ESD protection also consists of a snapback ESD clamp between the output and (V-) to allow the output to be pulled above (V+) to a maximum of 40V.

6.4.5 Power-On Reset (POR)

The TLV185x and TLV186x devices have an internal Power-on-Reset (POR) circuit for known start-up or power-down conditions. While the power supply (V+) is ramping up or ramping down, the POR circuitry will be activated for up to 2ms after the V_{POR} of 1.5V is crossed. When the supply voltage is equal to or greater than the minimum supply voltage, and after the delay period, the comparator output reflects the state of the differential input (V_{ID}).

For the TLV185x push-pull output devices, the output is held low during the POR period (t_{on}).

For the TLV186x open drain output devices, the POR circuit will keep the output high impedance (Hi-Z) during the POR period (t_{on}).

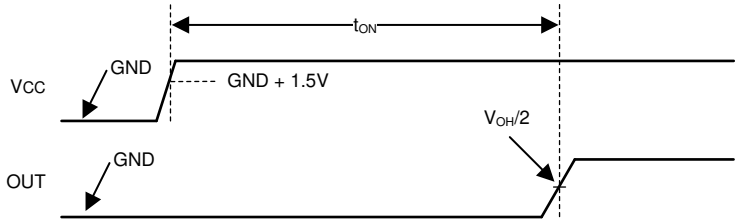


図 6-3. Power-On Reset Timing Diagram

Note that it the nature of an open collector output that the output will rise with the pull-up voltage during the POR period.

6.4.6 Reverse Battery Protection

The TLV185x and TLV186x devices have an internal reverse battery protection feature that prevents damage to the comparator in the event of improper battery installation to the supply pins. This protection feature works up to 40V.

7 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Basic Comparator Definitions

7.1.1.1 Operation

The basic comparator compares the input voltage (V_{IN}) on one input to a reference voltage (V_{REF}) on the other input. In the 図 7-1 example below, if V_{IN} is less than V_{REF}, the output voltage (V_O) is logic low (V_{OL}). If V_{IN} is greater than V_{REF}, the output voltage (V_O) is at logic high (V_{OH}). 表 7-1 summarizes the output conditions. The output logic can be inverted by simply swapping the input pins.

表 7-1. Output Conditions

Inputs Condition	Output
IN+ > IN-	HIGH (V_{OH})
IN+ = IN-	Indeterminate (chatters - see Hysteresis)
IN+ < IN-	LOW (V_{OL})

7.1.1.2 Propagation Delay

There is a delay between from when the input crosses the reference voltage and the output responds. This is called the Propagation Delay. Propagation delay can be different between high-to low and low-to-high input transitions. This is shown as t_{pLH} and t_{pHL} in 図 7-1 and is measured from the mid-point of the input to the midpoint of the output.

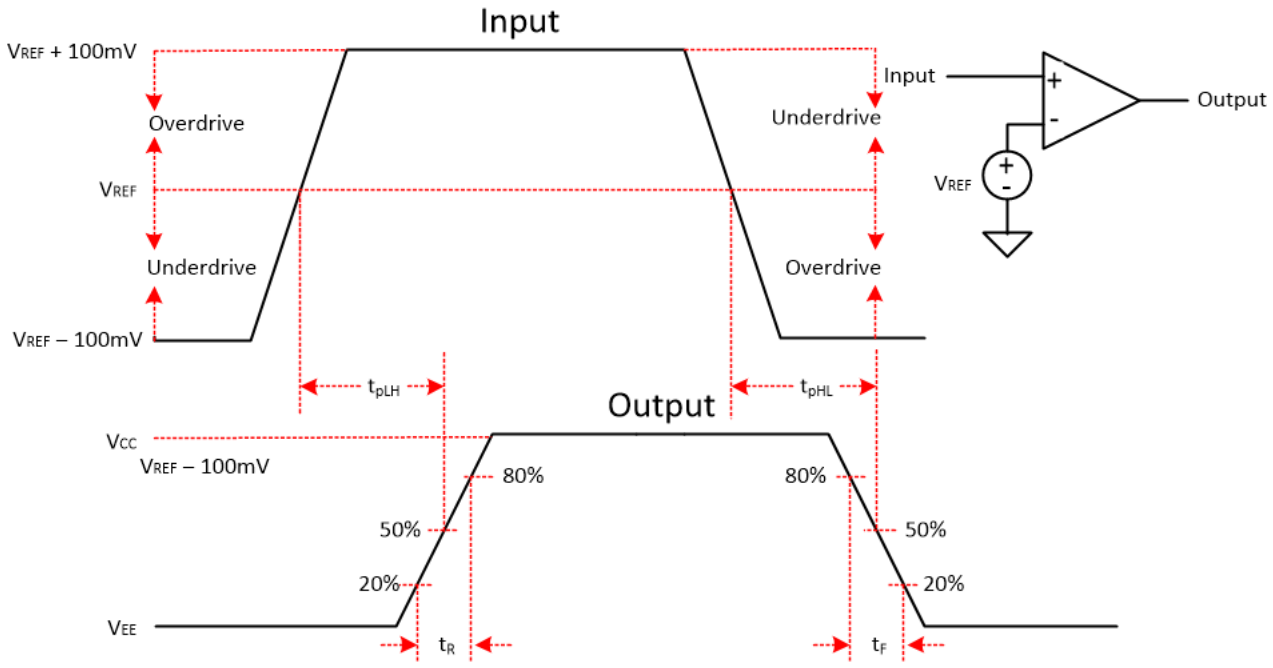


図 7-1. Comparator Timing Diagram

7.1.1.3 Overdrive Voltage

The overdrive voltage, V_{OD}, is the amount of input voltage beyond the reference voltage (and not the total input peak-to-peak voltage). The overdrive voltage is 100mV as shown in the 図 7-1 example. The overdrive voltage can influence the propagation delay (t_p). The smaller the overdrive voltage, the longer the propagation delay, particularly when <100mV. If the fastest speeds are desired, it is recommended to apply the highest amount of overdrive possible.

The risetime (t_r) and falltime (t_f) is the time from the 20% and 80% points of the output waveform.

7.1.2 Hysteresis

The basic comparator configuration may produce a noisy "chatter" output if the applied differential input voltage is near the comparator's offset voltage. This usually occurs when the input signal is moving very slowly across the switching threshold of the comparator. This problem can be prevented by adding external hysteresis to the comparator.

Since the TLV185x and TLV186x devices only have a minimal amount of internal hysteresis of 2.7mV, external hysteresis can be applied in the form of a positive feedback loop that adjusts the trip point of the comparator depending on its current output state.

The hysteresis transfer curve is shown in 図 7-2. This curve is a function of three components: V_{TH}, V_{OS}, and V_{HYST}:

- V_{TH} is the actual set voltage or threshold trip voltage.
- V_{OS} is the internal offset voltage between V_{IN+} and $V_{IN–}$. This voltage is added to V_{TH} to form the actual trip point at which the comparator must respond to change output states.
- V_{HYST} is the hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise.

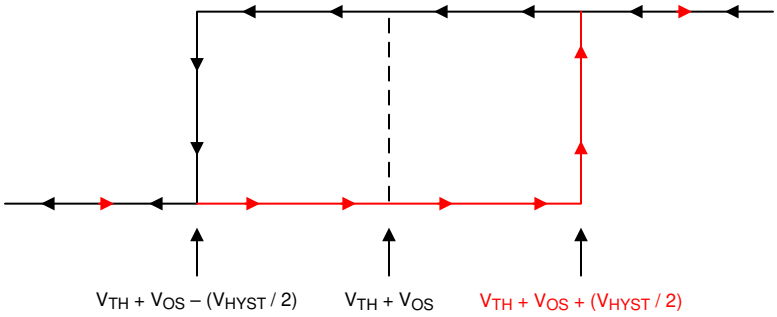


図 7-2. Hysteresis Transfer Curve

For more information, please see Application Note SBOA219 "Comparator with and without hysteresis circuit".

7.1.2.1 Inverting Comparator With Hysteresis

The inverting comparator with hysteresis requires a three-resistor network that is referenced to the comparator supply voltage (V_{CC}), as shown in 図 7-3.

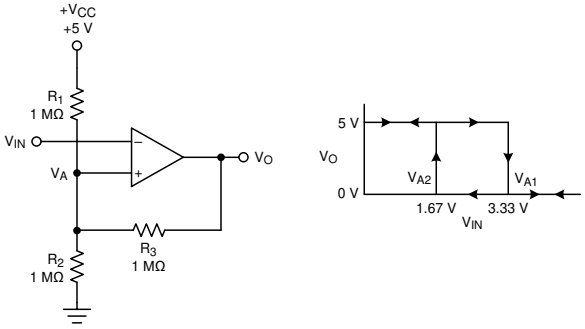


図 7-3. TLV185x in an Inverting Configuration With Hysteresis

The equivalent resistor networks when the output is high and low are shown in 図 7-3.

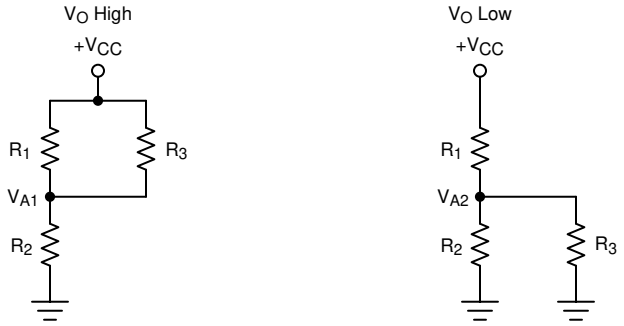


図 7-4. Inverting Configuration Resistor Equivalent Networks

When V_{IN} is less than V_A, the output voltage is high (for simplicity, assume V_O switches as high as V_{CC}). The three network resistors can be represented as R1 || R3 in series with R2, as shown in 図 7-4.

式 1 below defines the high-to-low trip voltage (V_{A1}).

$$V_{A1} = V_{CC} \times \frac{R2}{(R1 \parallel R3) + R2} \tag{1}$$

When V_{IN} is greater than V_A, the output voltage is low. In this case, the three network resistors can be presented as R2 || R3 in series with R1, as shown in 式 2.

Use 式 2 to define the low to high trip voltage (V_{A2}).

$$V_{A2} = V_{CC} \times \frac{R2 \parallel R3}{R1 + (R2 \parallel R3)} \tag{2}$$

式 3 defines the total hysteresis provided by the network.

$$\Delta V_A = V_{A1} - V_{A2} \tag{3}$$

7.1.2.2 Non-Inverting Comparator With Hysteresis

A non-inverting comparator with hysteresis requires a two-resistor network and a voltage reference (V_{REF}) at the inverting input, as shown in 図 7-5,

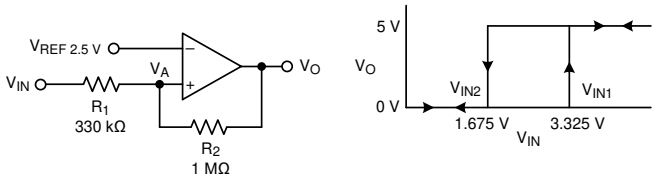


図 7-5. TLV185x in a Non-Inverting Configuration With Hysteresis

The equivalent resistor networks when the output is high and low are shown in 図 7-6.

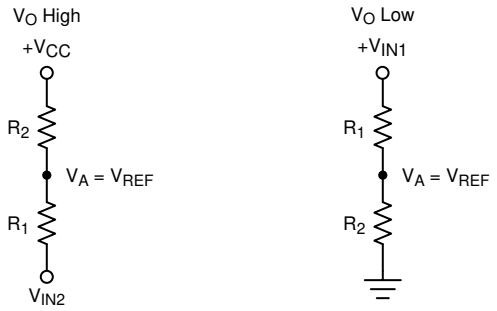


図 7-6. Non-Inverting Configuration Resistor Networks

When V_{IN} is less than V_{REF}, the output is low. For the output to switch from low to high, V_{IN} must rise above the V_{IN1} threshold. Use 式 4 to calculate V_{IN1}.

$$V_{IN1} = R1 \times \frac{V_{REF}}{R2} + V_{REF} \tag{4}$$

When V_{IN} is greater than V_{REF}, the output is high. For the comparator to switch back to a low state, V_{IN} must drop below V_{IN2}. Use 式 5 to calculate V_{IN2}.

$$V_{IN2} = \frac{V_{REF}\,(R1 + R2) - V_{CC} \times R1}{R2} \tag{5}$$

The hysteresis of this circuit is the difference between V_{IN1} and V_{IN2}, as shown in 式 6.

$$\Delta V_{IN} = V_{CC} \times \frac{R1}{R2} \tag{6}$$

For more information, please see Application Notes SNOA997 "Inverting comparator with hysteresis circuit" and SBOA313 "Non-Inverting Comparator With Hysteresis Circuit".

7.1.2.3 Inverting and Non-Inverting Hysteresis using Open-Drain Output

It is also possible to use an open drain output device, such as the TLV186x, but the output pull-up resistor must also be taken into account in the calculations. The pull-up resistor is seen in series with the feedback resistor when the output is high. Thus, the feedback resistor is actually seen as R2 + R_{PULLUP}. TI recommends that the pull-up resistor be at least 10 times less than the feedback resistor value.

7.2 Typical Applications

7.2.1 Window Comparator

Window comparators are commonly used to detect undervoltage and overvoltage conditions. 図 7-7 shows a simple window comparator circuit. Window comparators require open drain outputs (TLV186x if the outputs are directly connected together.

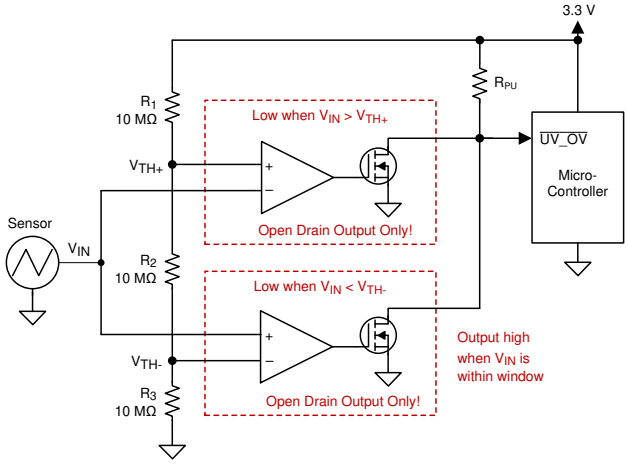


図 7-7. Window Comparator

7.2.1.1 Design Requirements

For this design, follow these design requirements:

- Alert (logic low output) when an input signal is less than 1.1V
- Alert (logic low output) when an input signal is greater than 2.2V
- Alert signal is active low
- Operate from a 3.3V power supply

7.2.1.2 Detailed Design Procedure

Configure the circuit as shown in 図 7-7. Connect V+ to a 3.3V power supply and V_{EE} to ground. Make R1, R2 and R3 each 10MΩ resistors. These three resistors are used to create the positive and negative thresholds for the window comparator (V_{TH+} and $V_{TH–}$).

With each resistor being equal, V_{TH+} is 2.2V and V_{TH-} is 1.1V. Large resistor values such as 10MΩ are used to minimize power consumption. The resistor values may be recalculated to provide the desired trip point values.

The sensor output voltage is applied to the inverting and noninverting inputs of the two comparators. Using two open-drain output comparators allows the two comparator outputs to be Wire-OR'ed together.

The respective comparator outputs will be low when the sensor is less than 1.1V or greater than 2.2V. The respective comparator outputs will be high when the sensor is in the range of 1.1V to 2.2V (within the "window"), as shown in 図 7-8.

7.2.1.3 Application Curve

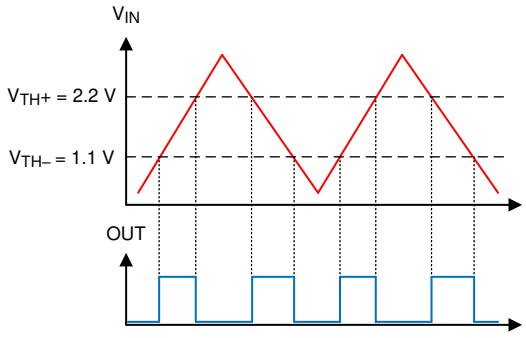


図 7-8. Window Comparator Results

For more information, please see Application note SBOA221 "Window comparator circuit".

7.2.2 Undervoltage Detection

Undervoltage detection is frequently required in low-power, always-on systems to alert the downstream device that a battery or supply voltage has drooped below the nominal voltage level. The TLV185x and TLV186x devices have an over-the-rail capability which allows the comparator to monitor high voltages up to 40V on the inputs while operating at lower supply voltages such as 3.3V, as shown in 図 7-9. The high voltage battery V_{BAT} is divided down to be compared against a reference voltage, which can be set by a shunt regulator such as the TL431. When the voltage on the non-inverting input drops below the reference voltage, then the output of the comparator will toggle and send an alert signal to a MCU.

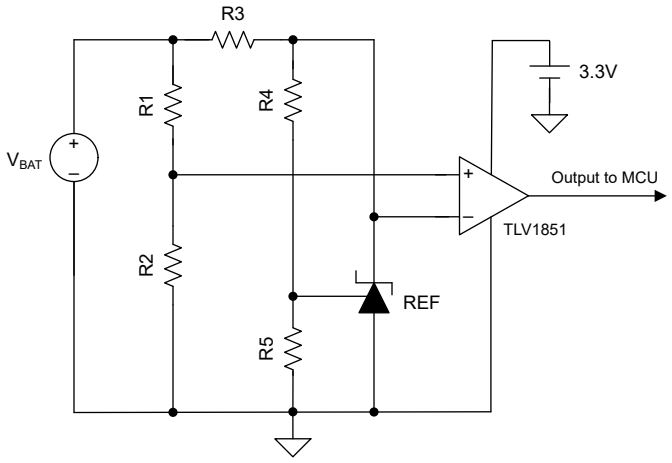


図 7-9. Undervoltage Detection

7.2.3 Reverse Battery and Overvoltage Protection Scheme

In battery powered applications, it is essential to have safeguards in place to protect the internal electronics against reverse battery connections. 図 7-10 shows a protection scheme using TLV1851 to prevent damage to the overall system in the events of both improper battery installation and overvoltage conditions. Under either of these instances, Q1 and Q2 will open, thus protecting the system from ever seeing reverse battery or overvoltage conditions.

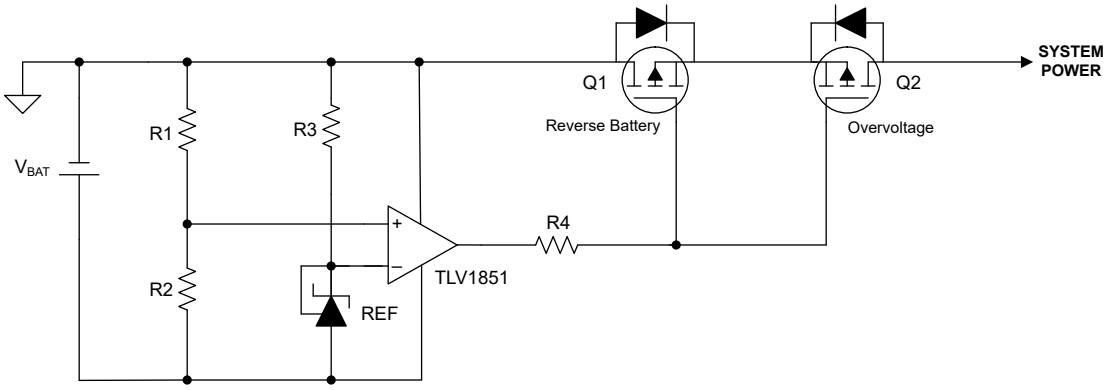


図 7-10. Reverse Battery and Overvoltage Protection Scheme

7.3 Power Supply Recommendations

Due to the fast output edges, it is critical to have bypass capacitors on the supply pin to prevent supply ringing and false triggers and oscillations. Bypass the supply directly at *each* device with a low ESR 0.1µF ceramic bypass capacitor directly between the (V+) pin and ground pins. Narrow peak currents will be drawn during the output transition time, particularly for the push-pull output device. These narrow pulses can cause un-bypassed

supply lines and poor grounds to ring, possibly causing variation that can eat into the input voltage range and create an inaccurate comparison or even oscillations.

The device may be powered from both "split" supplies ((V+) &(V-)), or "single" supplies ((V+) and GND), with GND applied to the (V-) pin. Input signals must stay within the recommended input range for either type. Note that with a "split" supply the output will now swing "low" (V_{OL}) to (V-) potential and not GND.

7.4 Layout

7.4.1 Layout Guidelines

For accurate comparator applications it is important maintain a stable power supply with minimized noise and glitches. Output rise and fall times are in the tens of nanoseconds, and should be treated as high speed logic devices. The bypass capacitor should be as close to the supply pin as possible and connected to a solid ground plane, and preferably directly between the (V+) and GND pins.

Minimize coupling between outputs and inputs to prevent output oscillations. Do not run output and input traces in parallel unless there is a (V+) or GND trace between output to reduce coupling. When series resistance is added to inputs, place resistor close to the device. A low value (<100ohms) resistor may also be added in series with the output to dampen any ringing or reflections on long, non-impedance controlled traces. For best edge shapes, controlled impedance traces with back-terminations should be used when routing long distances.

7.4.2 Layout Example

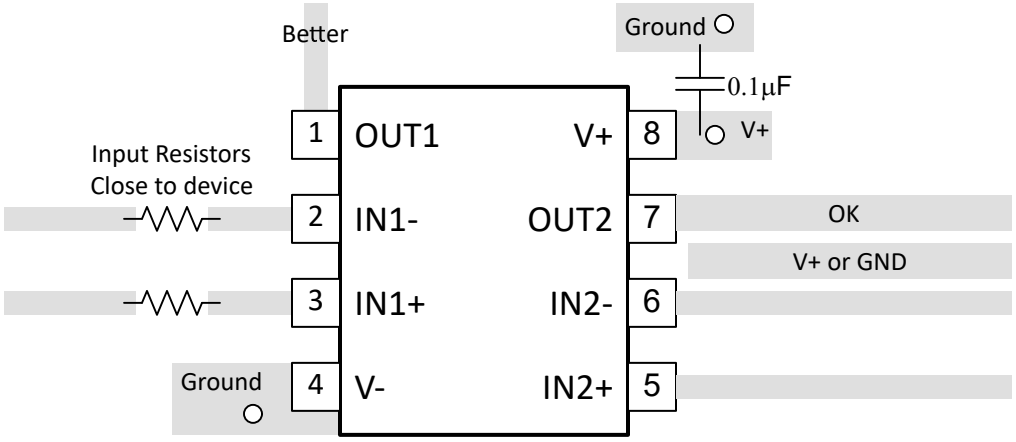


図 7-11. Dual Layout Example

8 デバイスおよびドキュメントのサポート

8.1 Documentation Support

8.1.1 Related Documentation

Analog Engineers Circuit Cookbook: Amplifiers (See Comparators section) - SLYY137

Precision Design, Comparator with Hysteresis Reference Design— TIDU020

Window comparator circuit - SBOA221

Reference Design, Window Comparator Reference Design— TIPD178

Comparator with and without hysteresis circuit - SBOA219

Inverting comparator with hysteresis circuit - SNOA997

Non-Inverting Comparator With Hysteresis Circuit - SBOA313

A Quad of Independently Func Comparators - SNOA654

8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.3 サポート・リソース

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8.4 Trademarks

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8.5 静電気放電に関する注意事項

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8.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (January 2023) to Revision B (September 2024)	Page
• デュアル チャネルおよびクワッド チャネルの部品を追加	1

Changes from Revision * (December 2022) to Revision A (January 2023) **Page**

- TLV1851 の量産データのリリース..... 1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV1851DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1851
TLV1851DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1851
TLV1852DGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	38OS
TLV1852DGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	38OS
TLV1854PWR	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV1854
TLV1854PWR.A	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV1854
TLV1861DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1861
TLV1861DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1861
TLV1862DGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	38PS
TLV1862DGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	38PS
TLV1864PWR	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV1864
TLV1864PWR.A	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV1864

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TLV1851, TLV1861 :

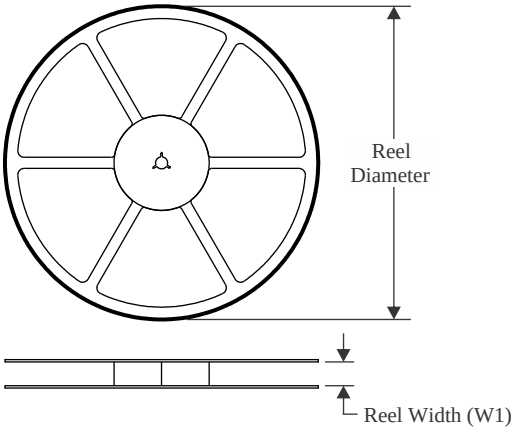
- Automotive : TLV1851-Q1, TLV1861-Q1

NOTE: Qualified Version Definitions:

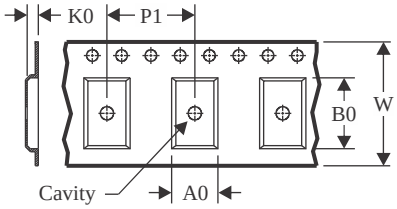
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

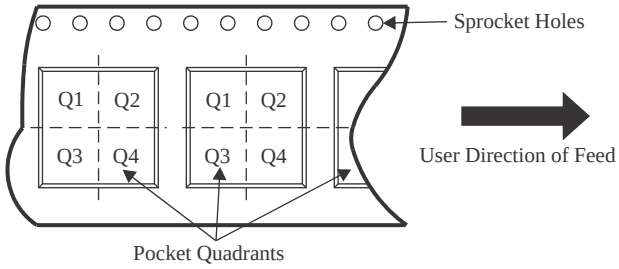


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

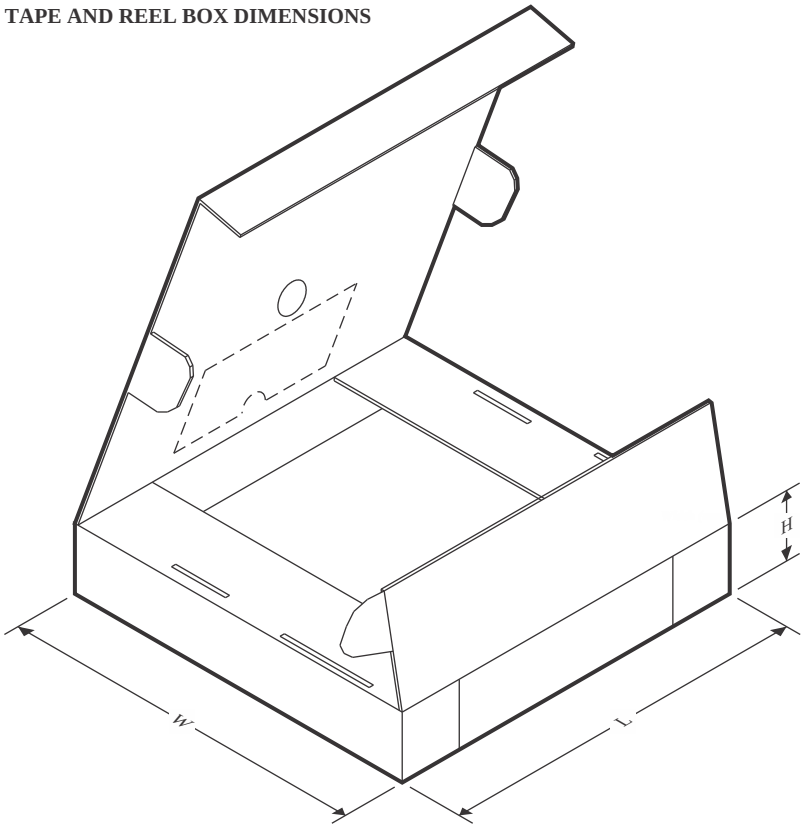
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV1851DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV1851DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV1852DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV1854PWR	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV1861DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV1861DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV1862DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV1864PWR	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

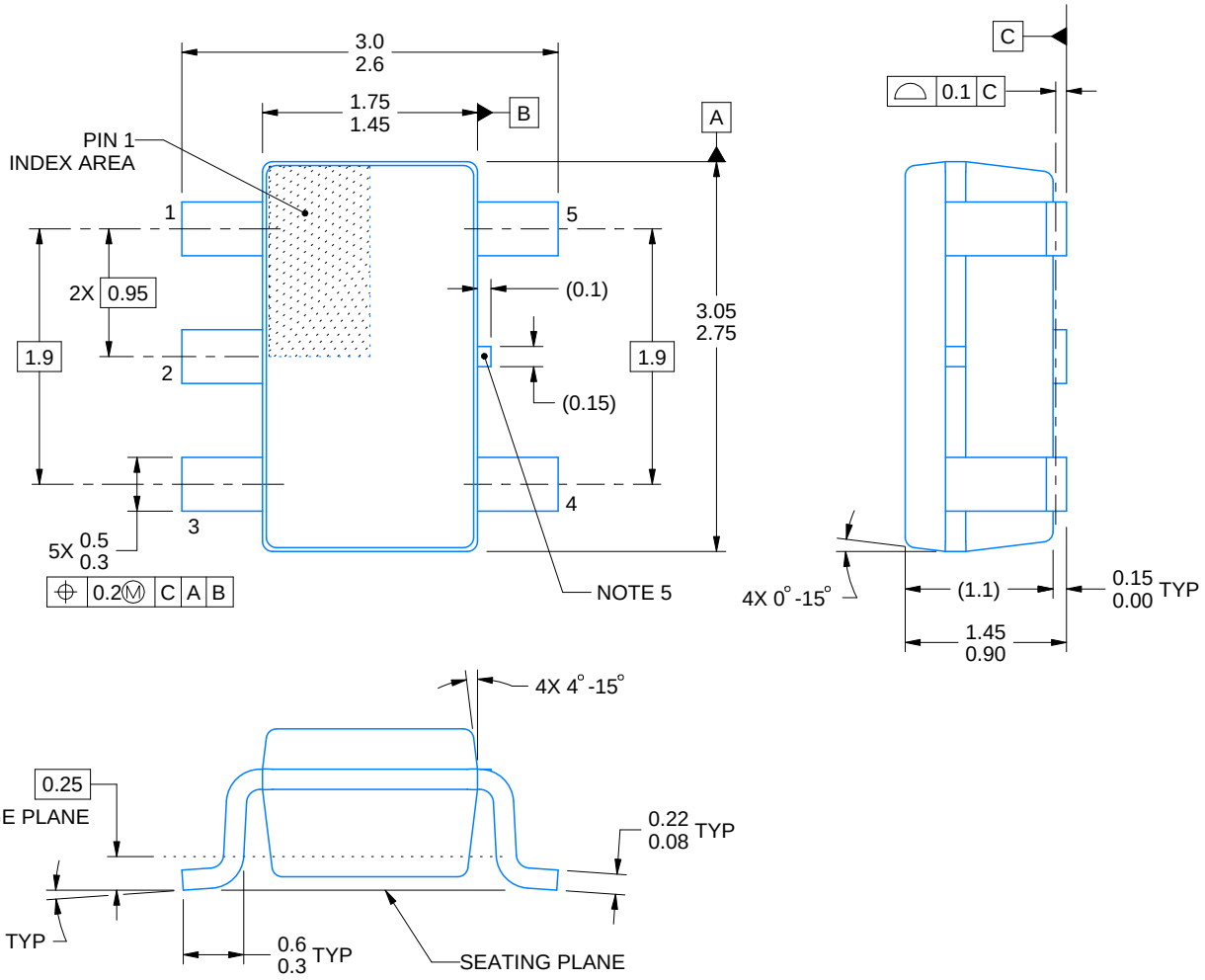
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV1851DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV1851DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV1852DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
TLV1854PWR	TSSOP	PW	14	3000	353.0	353.0	32.0
TLV1861DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV1861DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV1862DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
TLV1864PWR	TSSOP	PW	14	3000	353.0	353.0	32.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

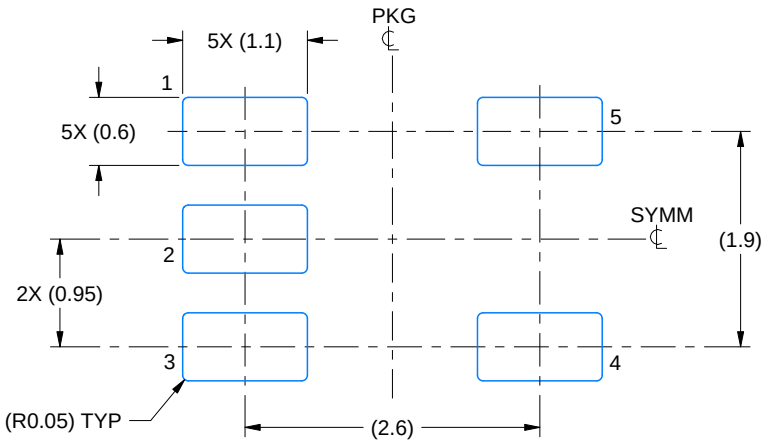
SMALL OUTLINE TRANSISTOR



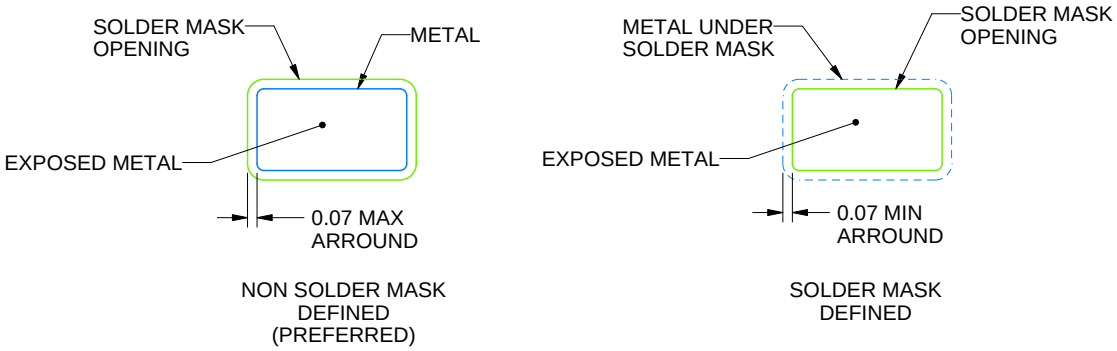
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

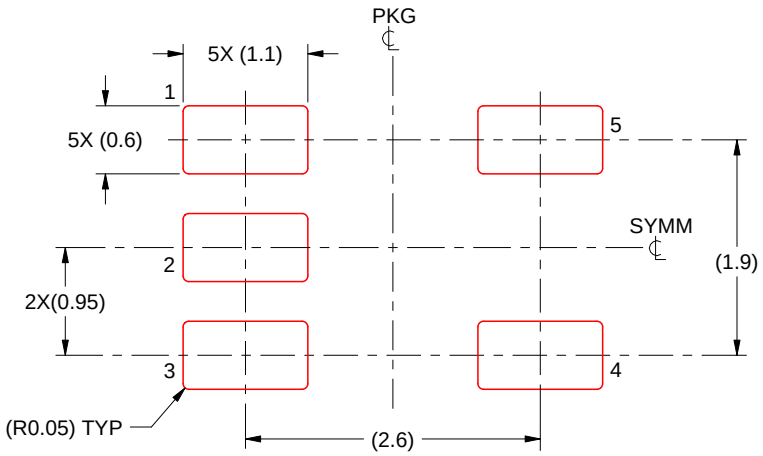


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

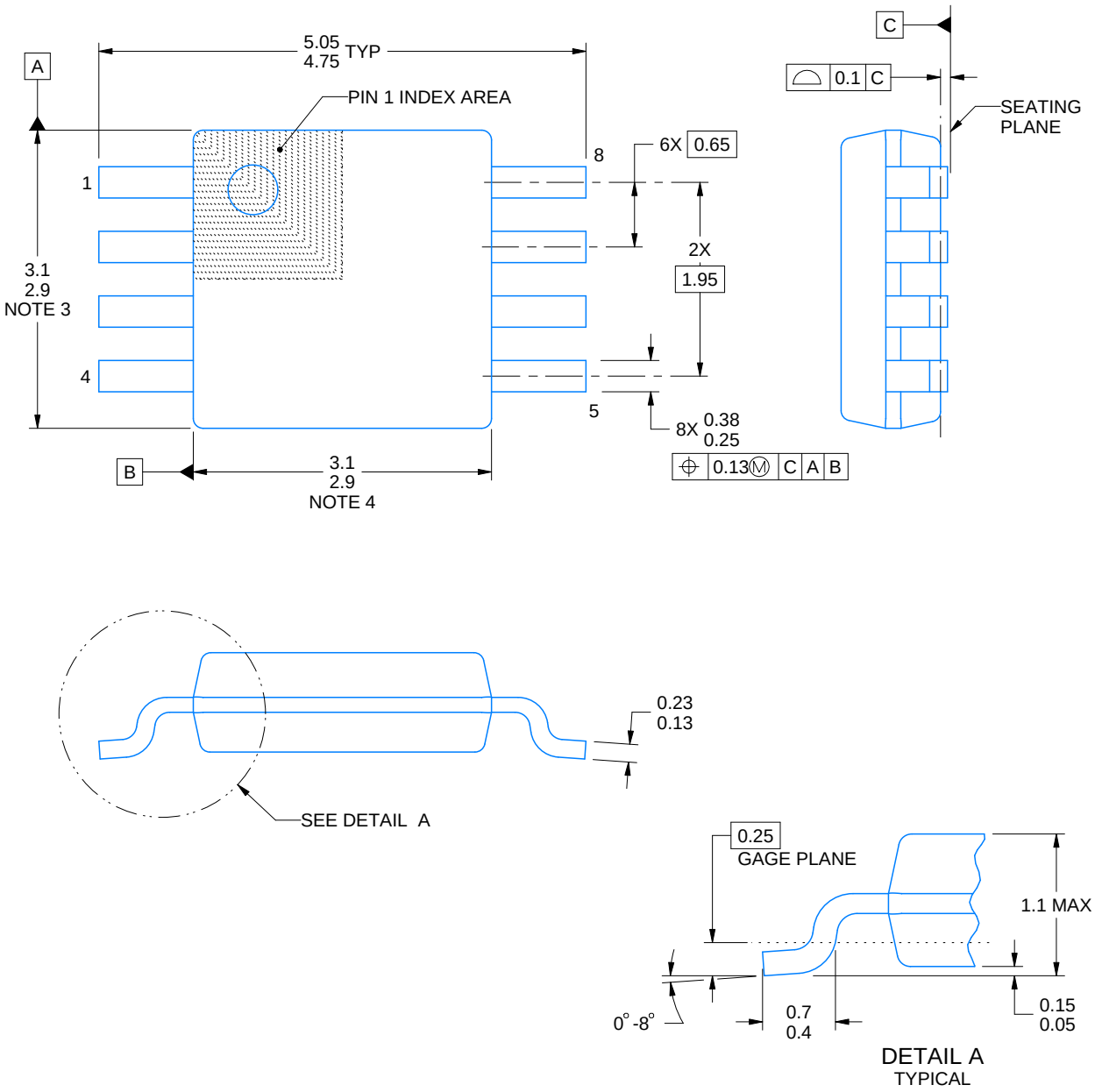
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

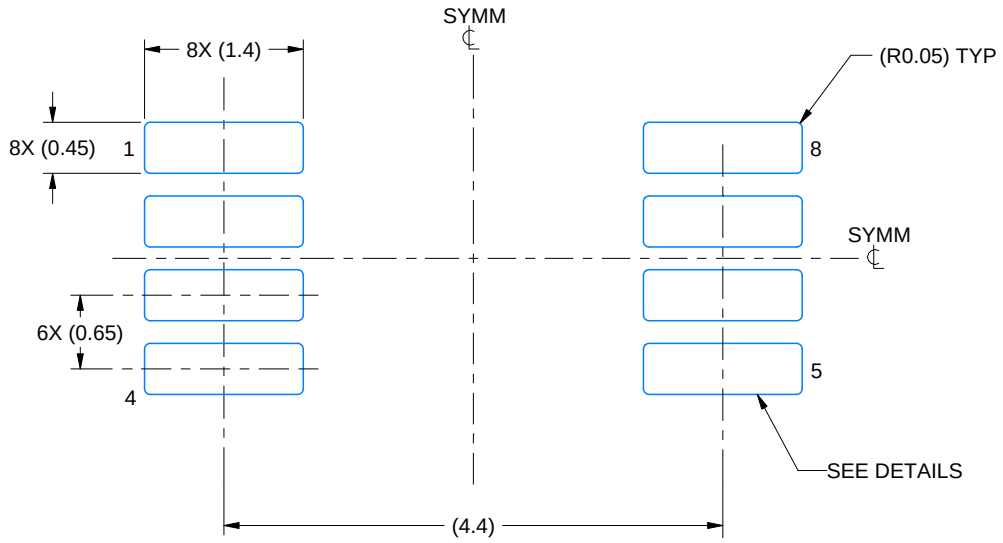
SMALL OUTLINE PACKAGE



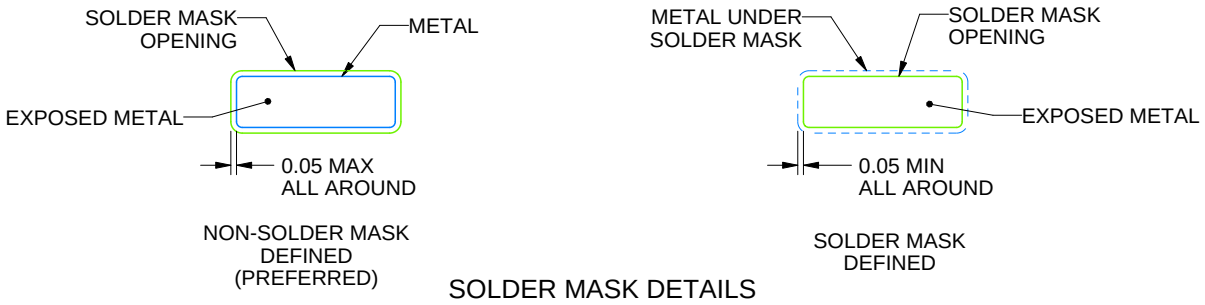
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

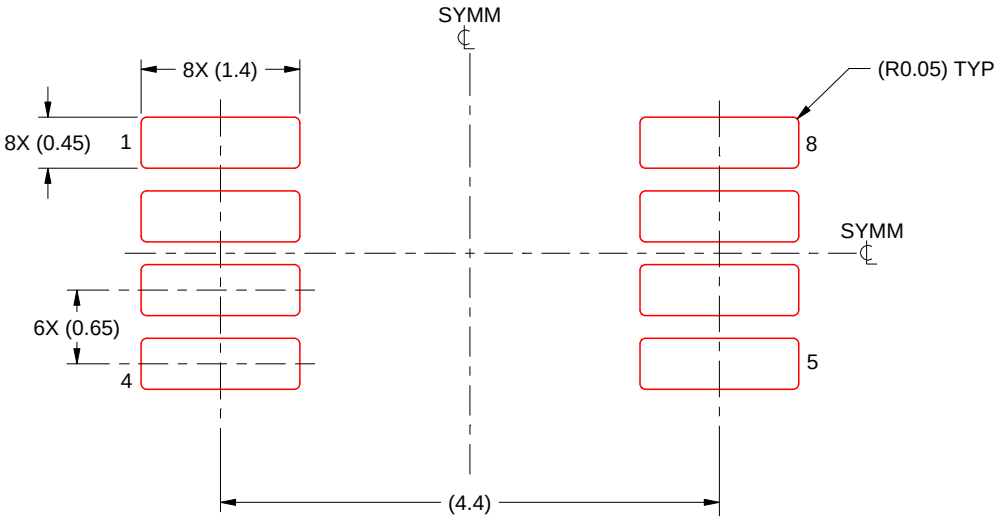


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

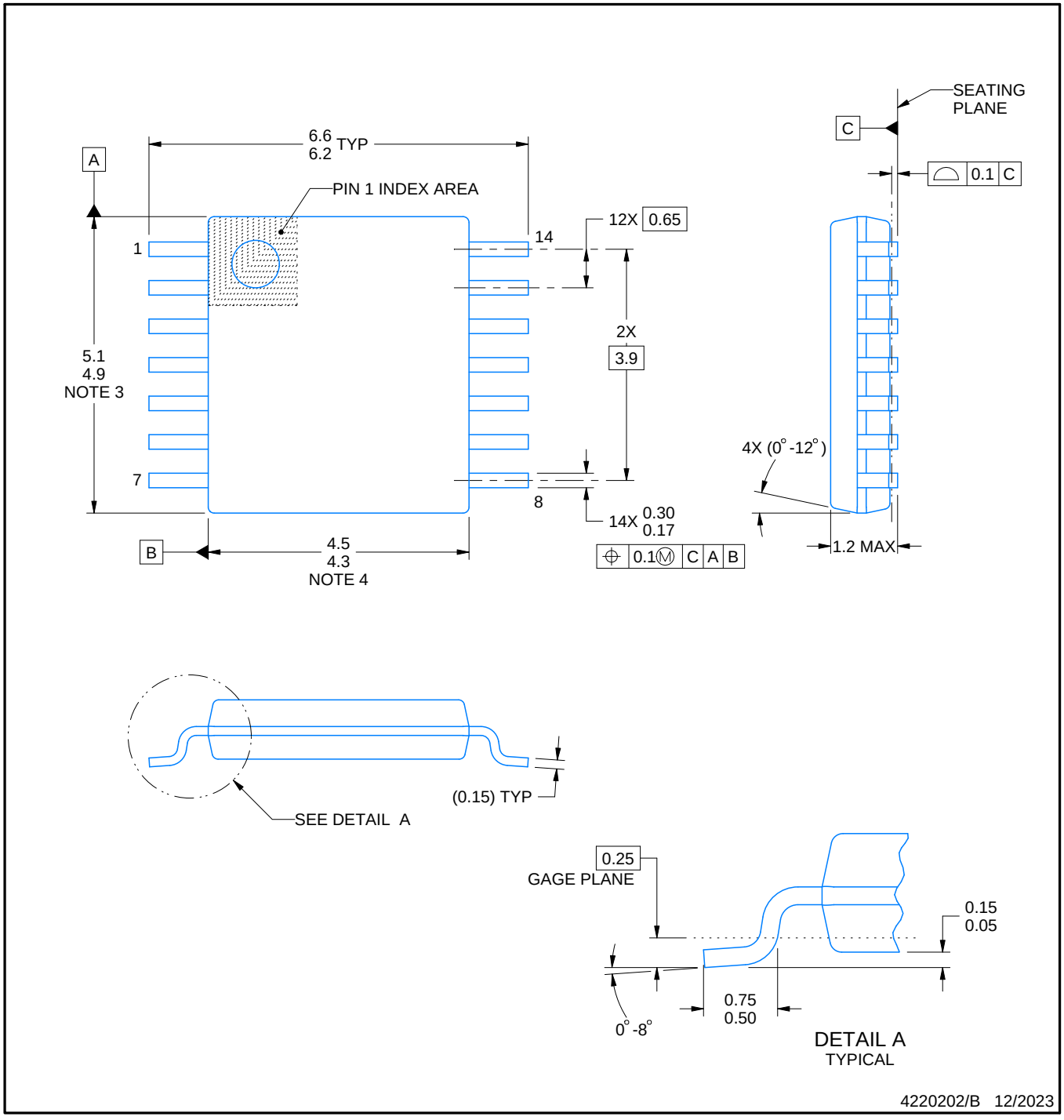
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

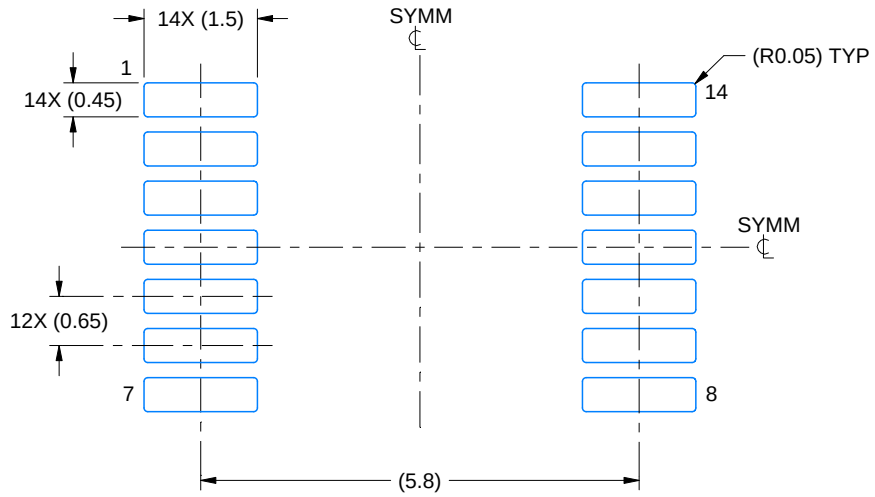
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

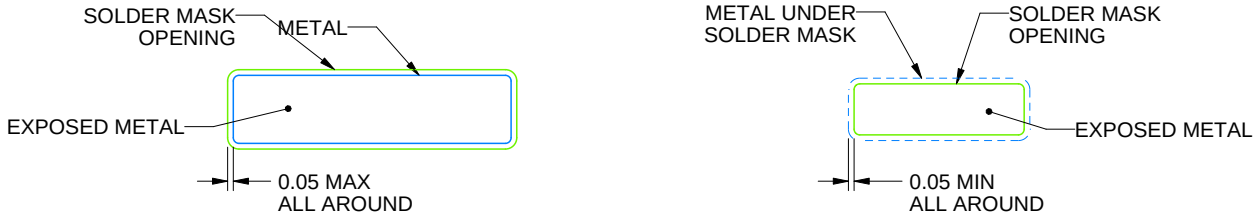


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

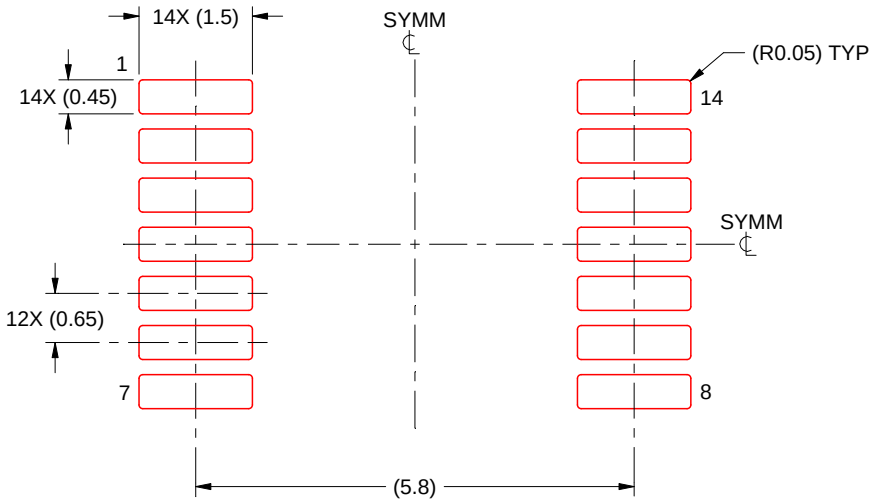


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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