TLV1811-Q1, TLV1821-Q1, TLV1812-Q1, TLV1822-Q1
TLV1814-Q1, TLV1824-Q1
JAJSJU2B – OCTOBER 2022 – REVISED SEPTEMBER 2023

TLV181x-Q1 および TLV182x-Q1 プッシュプルまたはオープン・ドレイン出力オプションを持つ 40V 車載用レール・ツー・レール入力コンパレータ・ファミリ

1 特長

- 車載アプリケーション向けに認定済み
- 以下の結果で AEC-Q100 認定済み:
  - デバイス温度グレード 1:動作時周囲温度範囲:–40℃～125℃
  - デバイス HBM ESD 分類レベル 2
  - デバイス CDM ESD 分類レベル C3
- 2.4V～40V の広い電源電圧範囲
- 低い静止電流:チャネルごとに 5µA
- レール・ツー・レール入力
- 既知のスタートアップへのパワーオン・リセット (POR)
- 低い入力オフセット電圧:500µV
- 伝搬遅延時間:420ns (代表値)
- プッシュプル出力オプション (TLV181x-Q1)
- オープン・ドレイン出力オプション (TLV182x-Q1)
- 機能安全対応
  - 機能安全準拠のシステム設計に役立つ資料を利用可能

2 アプリケーション

- HEV/EV およびパワー・トレイン
- インフォテインメントおよびクラスタ
- 車体制御モジュール

3 概要

TLV181x-Q1 および TLV182x-Q1 は、複数の出力オプションを備えた車載用グレード 40V シングル、デュアル、クワッド・チャネル・コンパレータのファミリです。このファミリは、プッシュプルまたはオープン・ドレイン出力オプションを持つレール・ツー・レール入力を提供します。このファミリは速度と消費電力の組み合わせが非常に優れており、伝搬遅延は 420ns、完全電源電圧範囲は 2.4V～40V、チャネルあたりの静止時電流はわずか 5µA です。

すべてのデバイスに、パワーオン・リセット (POR) 機能が搭載されています。これにより、出力が入力に応答する前、最小電源電圧に達するまでの間、出力が既知の状態であることが保証されるため、システムの電源オンおよび電源オフ時に誤った出力が発生することを防止できます。

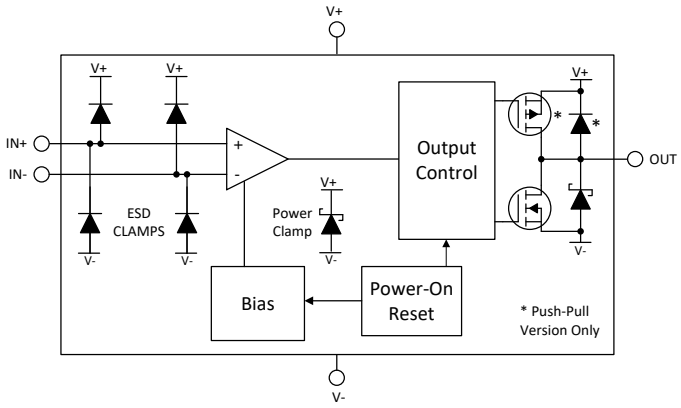
TLV181x-Q1 コンパレータは、LED の制御、または MOSFET ゲートなどの容量性負荷の駆動を行うときに数ミリアンペアの電流をシンクおよびソースできるプッシュプル出力段を備えています。

TLV182x-Q1 コンパレータは、コンパレータの電源電圧に関係なく最大 40V までプルアップできるオープン・ドレイン出力段を備えています。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
TLV1811-Q1、TLV1821-Q1 (シングル)	SC-70 (5)	1.25mm × 2.00mm
	SOT-23 (5)	1.60mm x 2.90mm
TLV1811L-Q1、TLV1821L-Q1 (シングル - 代替ピン配置)	SOT-23 (5)	1.60mm x 2.90mm
TLV1812-Q1、TLV1822-Q1 (デュアル)	SOIC (8)	3.91mm × 4.90mm
	TSSOP (8)	3.00mm × 4.40mm
	VSSOP (8)	3.00mm × 3.00mm
	WSON (8) (プレビュー)	2.00mm × 2.00mm
	SOT-23 (8)	1.60mm x 2.90mm
TLV1814-Q1、TLV1824-Q1 (クワッド)	SOIC (14)	3.91mm x 8.65mm
	TSSOP (14) (プレビュー)	4.40mm x 5.00mm
	SOT-23 (14) (プレビュー)	4.20mm x 2.00mm
	WQFN (16) (プレビュー)	3.00mm × 3.00mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



TLV18xx-Q1 のブロック図

Table of Contents

1 特長 ... 1
2 アプリケーション ... 1
3 概要 ... 1
4 Revision History ... 3
5 Pin Configuration and Functions ... 4
Pin Functions: TLV18x1-Q1 and TLV18x1L-Q1 ... 4
Pin Functions: TLV1812-Q1 and TLV1822-Q1 ... 5
Pin Functions: TLV1814-Q1 and TLV1824-Q1 ... 6
6 Specifications ... 7
6.1 Absolute Maximum Ratings ... 7
6.2 ESD Ratings ... 7
6.3 Recommended Operating Conditions ... 7
6.4 Thermal Information - Single ... 8
6.5 Thermal Information - Dual ... 8
6.6 Thermal Information - Quad ... 8
6.7 Electrical Characteristics ... 9
6.8 Switching Characteristics ... 10
7 Typical Characteristics ... 11
8 Detailed Description ... 14
8.1 Overview ... 14
8.2 Functional Block Diagrams ... 14
8.3 Feature Description ... 14
8.4 Device Functional Modes ... 14
9 Application and Implementation ... 17
9.1 Application Information ... 17
9.2 Typical Applications ... 20
9.3 Power Supply Recommendations ... 27
9.4 Layout ... 27
10 Device and Documentation Support ... 29
10.1 Documentation Support ... 29
10.2 ドキュメントの更新通知を受け取る方法 ... 29
10.3 サポート・リソース ... 29
10.4 Trademarks ... 29
10.5 静電気放電に関する注意事項 ... 29
10.6 用語集 ... 29
11 Mechanical, Packaging, and Orderable Information ... 29

4 Revision History

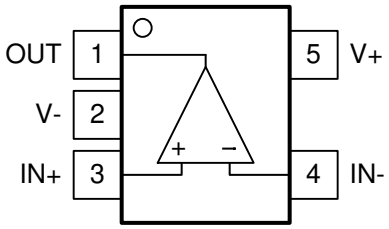
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (March 2023) to Revision B (September 2023)	Page
• デュアルおよび SOIC クワッド・リリースのプレビューを削除	1

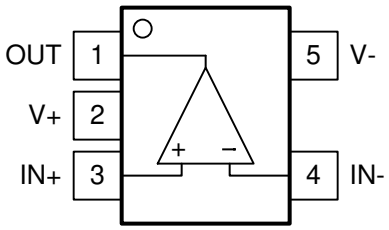
Changes from Revision * (October 2022) to Revision A (March 2023)	Page
• シングル・リリースのプレビューを削除	1

5 Pin Configuration and Functions

Pin Functions: TLV18x1-Q1 and TLV18x1L-Q1



TLV1811-Q1 and TLV1821-Q1
Standard "North West" pinout
DBV, DCK Packages,
SOT-23-5, SC-70-5
Top View

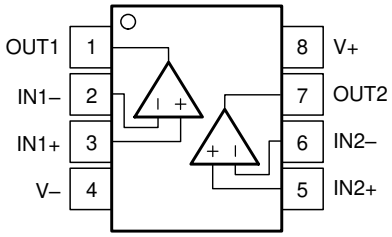


TLV1811L-Q1 and TLV1821L-Q1 DBV Package,
"LMC72x1/TLV72x1 type" pinout with reversed supplies
SOT-23-5,
Top View

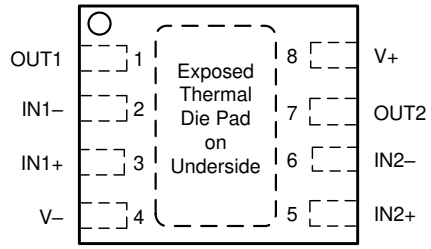
表 5-1. Pin Functions: TLV1811-Q1, TLV1821-Q1, TLV1811L-Q1 and TLV1821L-Q1

NAME	TLV18x1-Q1 PINS		TLV18x1L-Q1 PINS	I/O	DESCRIPTION
	SOT-23	SC-70	SOT-23		
OUT	1	1	1	O	Output
V-	2	2	**5**	-	Negative Supply Voltage
IN+	3	3	3	I	Non-Inverting (+) Input
IN-	4	4	4	I	Inverting (-) Input
V+	5	5	**2**	-	Positive Supply Voltage

Pin Functions: TLV1812-Q1 and TLV1822-Q1



D, DGK, PW, DDF Packages
8-Pin SOIC, VSSOP, TSSOP, SOT-23-8
Top View



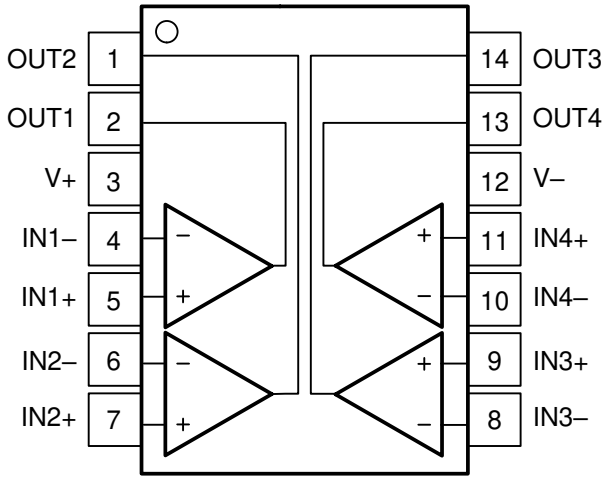
NOTE: Connect exposed thermal pad directly to V- pin.

DSG Package,
8-Pad WSON With Exposed Thermal Pad,
Top View

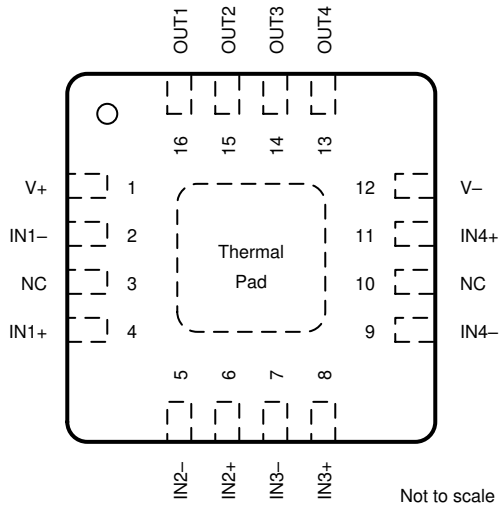
表 5-2. Pin Functions: TLV1812-Q1 and TLV1822-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
OUT1	1	O	Output pin of the comparator 1
IN1–	2	I	Inverting input pin of comparator 1
IN1+	3	I	Noninverting input pin of comparator 1
V-	4	—	Negative (low) supply
IN2+	5	I	Noninverting input pin of comparator 2
IN2–	6	I	Inverting input pin of comparator 2
OUT2	7	O	Output pin of the comparator 2
V+	8	—	Positive supply
Thermal Pad	—	—	Connect directly to V- pin

Pin Functions: TLV1814-Q1 and TLV1824-Q1



D, PW, DYY Package, 14-Pin SOIC, TSSOP, SOT-23, Top View



NOTE: Connect exposed thermal pad directly to V- pin.

RTE Package, 16-Pad WQFN With Exposed Thermal Pad, Top View

表 5-3. Pin Functions: TLV1814-Q1 and TLV1824-Q1

PIN			I/O	DESCRIPTION
NAME	SOIC	WQFN		
OUT2(1)	1	15	O	Output pin of the comparator 2
OUT1(1)	2	16	O	Output pin of the comparator1
V+	3	1	—	Positive supply
IN1–	4	2	I	Negative input pin of the comparator 1
IN1+	5	4	I	Positive input pin of the comparator 1
IN2–	6	5	I	Negative input pin of the comparator 2
IN2+	7	6	I	Positive input pin of the comparator 2
IN3–	8	7	I	Negative input pin of the comparator 3
IN3+	9	8	I	Positive input pin of the comparator 3
IN4–	10	9	I	Negative input pin of the comparator 4
IN4+	11	11	I	Positive input pin of the comparator 4
V-	12	12	—	Negative supply
OUT4	13	13	O	Output pin of the comparator 4
OUT3	14	14	O	Output pin of the comparator 3
NC	—	3	—	No Internal Connection - Leave floating or GND
NC	—	10	—	No Internal Connection - Leave floating or GND
Thermal Pad	—	PAD	—	Connect directly to V- pin.

(1) Some manufacturers transpose the names of channels 1 and 2. Electrically the pinouts are identical, just a difference in channel naming convention.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage: V_S = (V+) – (V–)	–0.3	42	V
Input pins (IN+, IN–) from (V–) (2)	–0.3	(V+) + 0.3	V
Current into Input pins (IN+, IN–)	–10	10	mA
Output (OUT) voltage (Open-Drain) from (V–)(4)	–0.3	42	V
Output (OUT) voltage (Push-Pull) from (V–)	–0.3	(V+) + 0.3	V
Output (OUT) current (4) (5) (6)	-10	10	mA
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Input terminals are diode-clamped to (V–). Input signals that can swing more than 0.3 V beyond the supply rails must be current-limited to 10 mA or less.
(3) Output (OUT) for open drain can be greater than (V+) and inputs (IN+, IN–) as long as it is within the –0.3 V to 42 V range
(4) The output is diode-clamped to (V-) for both output options, and diode clamped to (V+) for the push-pull output option. The open drain version does not have a clamp to V+. Please see the *Outputs* and *ESD Protection* section of the *Application Information* Section for more information.
(5) Output sinking and sourcing current is internally limited to <35mA when operating within the Absolute Maximum output voltage limits. The Absoulute Maximum Output Current limit specified here is the maximum current through the clamp structure when exceeding the supply votlage below (V-) for both output options, or above (V+) for the push-pull option.
(6) Short-circuit from output to (V–) or (V+). Continuous output short circuits at elevated supply voltages can result in excessive heating and exceeding the maximum allowed junction temperature, leading to eventual device destruction.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-0111	±1000	
		Charged-device model (CDM), per AEC Q100-0111, TLV1822-Q1 Only	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage: V_S = (V+) – (V–)		2.4	40	V
Input voltage range from (V–)		–0.2	(V+) + 0.2	V
Output voltage range from (V–)	Open Drain	–0.2	40	V
	Push Pull	–0.2	(V+) + 0.2	V
Ambient temperature, T_A		–40	125	°C

6.4 Thermal Information - Single

THERMAL METRIC[1]		TLV18x1-Q1		UNIT
		DCK (SC-70)	DBV (SOT-23)	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	226.6	203.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	129.5	105.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	78.6	106.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	51.5	54.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	78.3	106.0	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics report.

6.5 Thermal Information - Dual

THERMAL METRIC[1]		TLV18x2-Q1					UNIT
		D (SOIC)	PW (TSSOP)	DDF (SOT-23)	DSG (WSON)	DGK (VSSOP)	
		8 PINS	8 PINS	8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	136.1	187.5	170.4	79.9	178.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	76.8	76.7	90.3	100.1	66.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	79.7	118.1	88.1	46.4	100.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	26.8	14.4	7.5	5.3	9.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	78.9	116.4	87.6	46.4	98.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	–	–	21.6	–	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics report.

6.6 Thermal Information - Quad

THERMAL METRIC[1]		TLV18x4-Q1				UNIT
		D (SOIC)	PW (TSSOP)	DYY (SOT-23)	RTE (WQFN)	
		14 PINS	14 PINS	14 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	104.2	124.1	119.9	53.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	60.3	52.4	60.6	58.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60.2	67.2	79.0	29.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	20.7	7.5	3.3	2.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	59.8	66.6	41.2	28.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	–	–	13.1	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics report.

6.7 Electrical Characteristics

For V_S (Total Supply Votlage) = (V+) – (V–) = 12 V, V_{CM} = V_S / 2 at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage		–3	±0.5	3	mV
		T_A = –40°C to +125°C	–4		4	mV
dV_{IO}/dT	Input offset voltage drift	T_A = –40°C to +125°C		±1.2		µV/°C
PSRR	Power supply rejection ratio	V_S = 2.4 V to 40 V, V_{CM} = (V–)		100		dB
POWER SUPPLY						
I_Q	Quiescent current, No Load	Output Low, T_A = 25°C TLV1811-Q1 Only		6	7.5	µA
		Output Low, T_A = –40°C to +125°C TLV1811-Q1 Only			8.5	
		Output High, T_A = 25°C TLV1811-Q1 Only		8	10	
		Output High, T_A = –40°C to +125°C TLV1811-Q1 Only			11	
I_Q	Quiescent current per comparator, No Load	Output Low, T_A = 25°C		5	6.5	µA
		Output Low, T_A = –40°C to +125°C			7.5	
		Output High, T_A = 25°C		7	9	
		Output High, T_A = –40°C to +125°C			10	
V_{POR}	Power On Reset Voltage			1.7		V
INPUT BIAS CURRENT						
I_B	Input bias current (1)			150		fA
		T_A = –40°C to +125°C	–1.2		1.2	nA
I_{OS}	Input offset current (1)			10		fA
INPUT CAPACITANCE						
C_{ID}	Input Capacitance, Differential			2		pF
C_{IC}	Input Capacitance, Common Mode			8		pF
INPUT COMMON MODE RANGE						
$V_{CM-Range}$	Common-mode voltage range	V_S = 2.4 V to 40 V T_A = –40°C to +125°C, Rail to Rail	(V–) – 0.2		(V+) + 0.2	V
OUTPUT						
V_{OL}	Voltage swing from (V–)	I_{SINK} = 4 mA T_A = –40°C to +125°C			250	mV
V_{OH}	Voltage swing from (V+) (for Push-Pull only)	I_{SOURCE} = 4 mA T_A = –40°C to +125°C			250	mV
I_{LKG}	Open-drain output leakage current	V_{ID} = +0.1 V, V_{PULLUP} = (V+) T_A = –40°C to +125°C		0.1		nA
I_{OL}	Short-circuit current	Sinking	15	30		mA
I_{OH}	Short-circuit current	Sourcing (for Push-Pull only)	15	30		mA

(1) This parameter is ensured by design and/or characterization and is not tested in production .

6.8 Switching Characteristics

For V_S (Total Supply Voltage) = (V+) – (V–) = 12 V, V_{CM} = V_S / 2 at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
T_{PD-HL}	Propagation delay time, high-to-low	V_{OD} = 10 mV, C_L = 50 pF		900		ns
T_{PD-HL}	Propagation delay time, high-to-low	V_{OD} = 100 mV, C_L = 50 pF		450		ns
T_{PD-LH}	Propagation delay time, low-to-high, push-pull output	V_{OD} = 10 mV, C_L = 50 pF		900		ns
T_{PD-LH}	Propagation delay time, low-to-high, push-pull output	V_{OD} = 100 mV, C_L = 50 pF		420		ns
T_{RISE}	Output Rise Time, 20% to 80%, push-pull output	C_L = 50 pF		15		ns
T_{FALL}	Output Fall Time, 80% to 20%	C_L = 50 pF		15		ns
F_{TOGGLE}	Toggle Frequency	V_{ID} = 100 mV, C_L = 50 pF		500		kHz
POWER ON TIME						
P_{ON}	Power on-time			200		µs

7 Typical Characteristics

T_A = 25°C, V_S = 12 V, R_{PULLUP} = 2.5 k, C_L = 20 pF, V_{CM} = 0 V, $V_{UNDERDRIVE}$ = 100 mV, $V_{OVERDRIVE}$ = 100 mV unless otherwise noted.

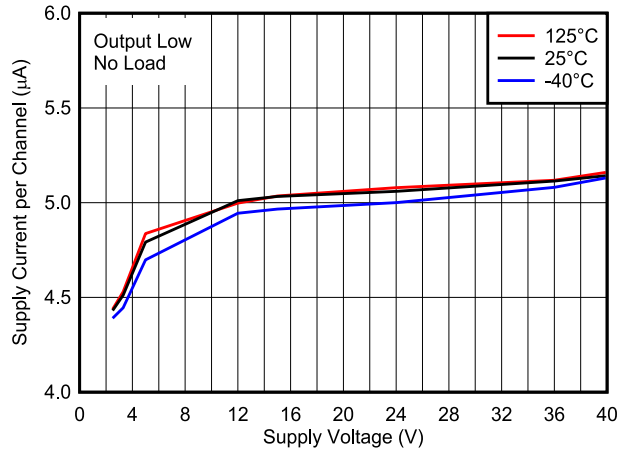


図 7-1. Supply Current per Channel vs. Supply Voltage, Output Low

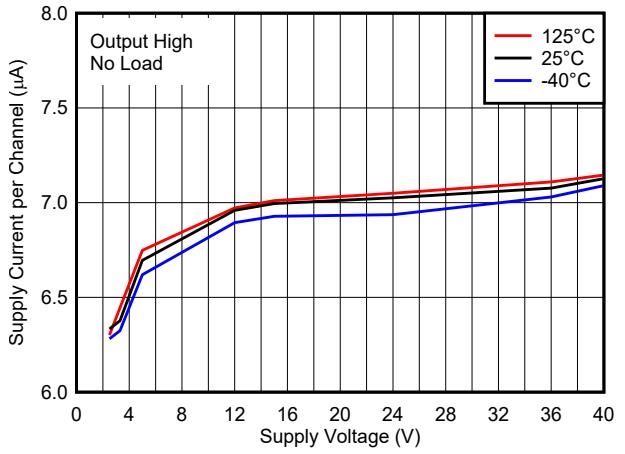


図 7-2. Supply Current per Channel vs. Supply Voltage, Output High

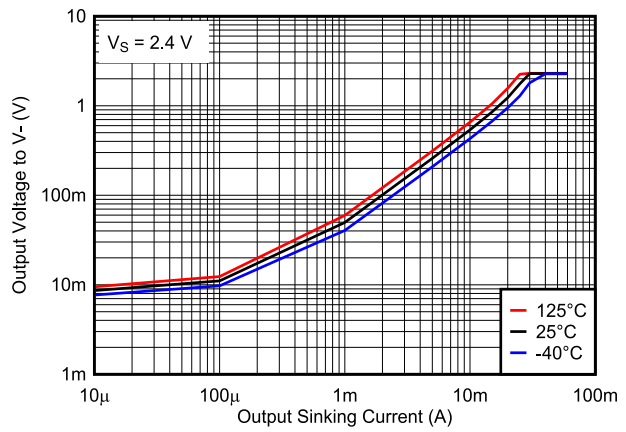


図 7-3. Output Voltage vs. Output Sinking Current, 2.4 V

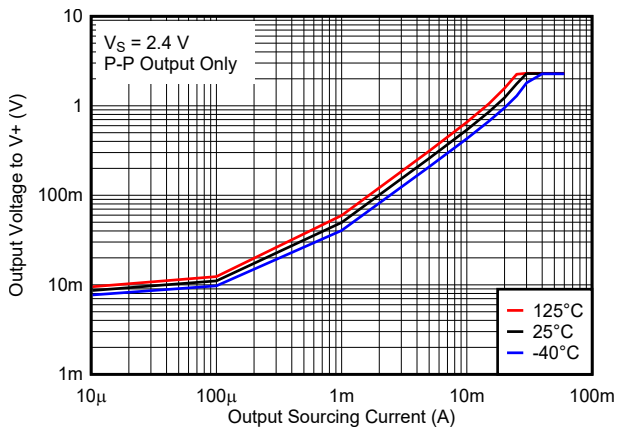


図 7-4. Output Voltage vs. Output Sourcing Current, 2.4 V

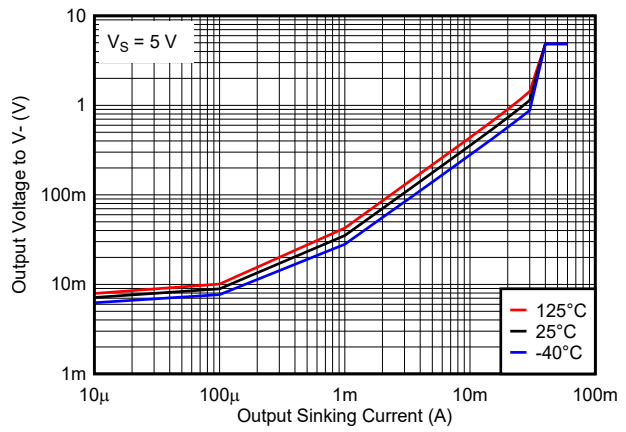


図 7-5. Output Voltage vs. Output Sinking Current, 5 V

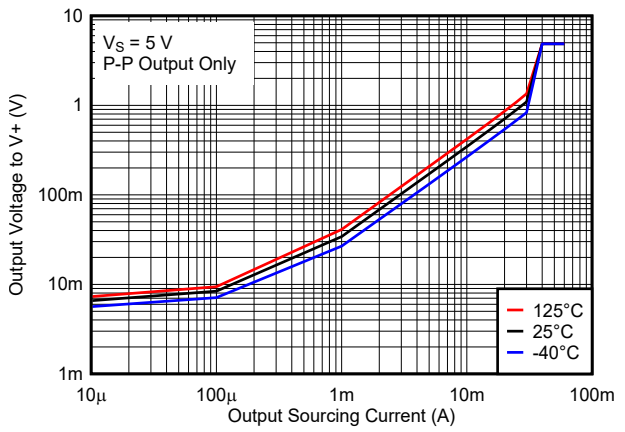


図 7-6. Output Voltage vs. Output Sourcing Current, 5 V

7 Typical Characteristics (continued)

T_A = 25°C, V_S = 12 V, R_{PULLUP} = 2.5 k, C_L = 20 pF, V_{CM} = 0 V, $V_{UNDERDRIVE}$ = 100 mV, $V_{OVERDRIVE}$ = 100 mV unless otherwise noted.

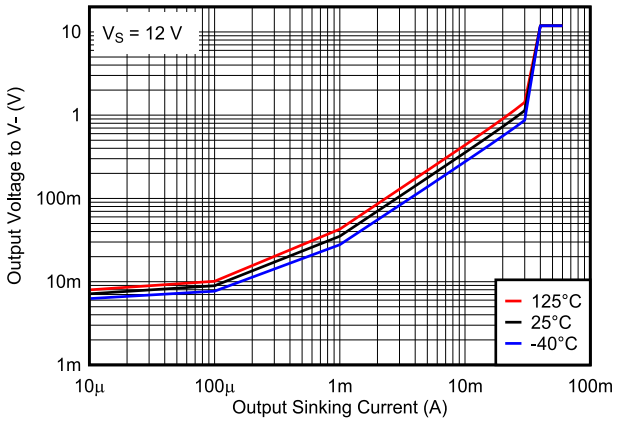


図 7-7. Output Voltage vs. Output Sinking Current, 12 V

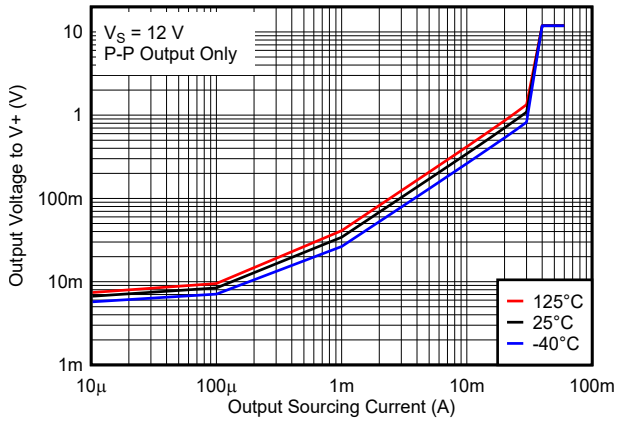


図 7-8. Output Voltage vs. Output Sourcing Current, 12 V

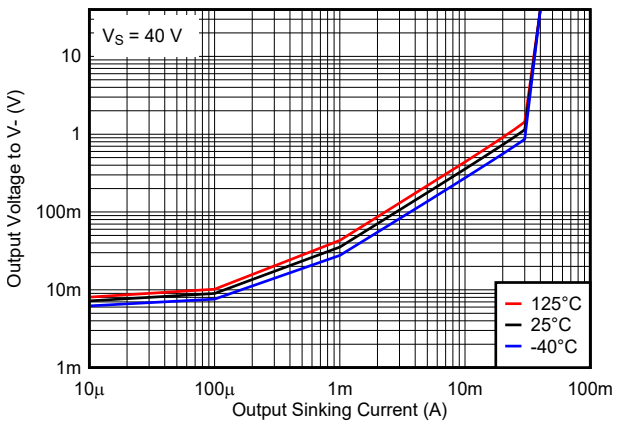


図 7-9. Output Voltage vs. Output Sinking Current, 40 V

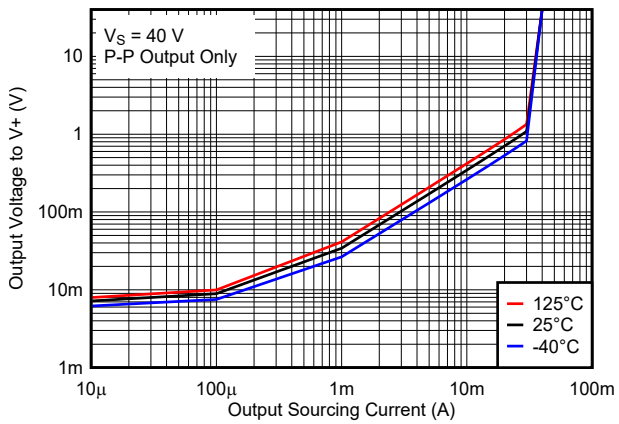


図 7-10. Output Voltage vs. Output Sourcing Current, 40 V

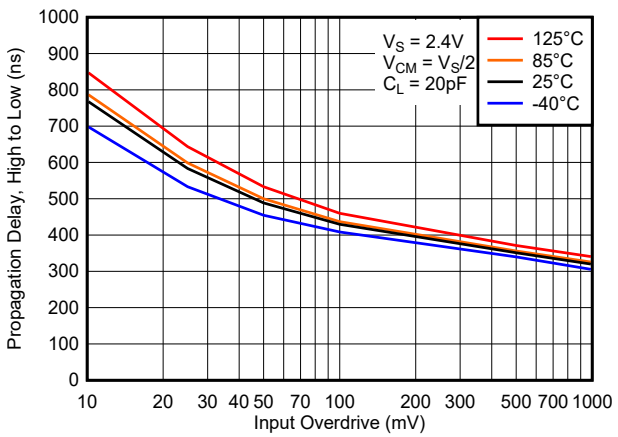


図 7-11. Propagation Delay, High to Low, 2.4 V

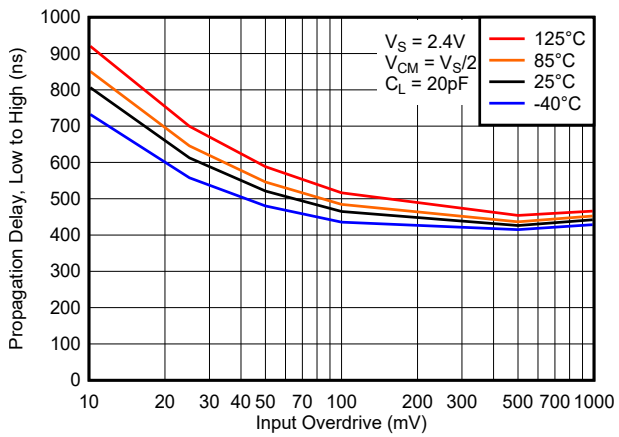


図 7-12. Propagation Delay, Low to High, 2.4 V

7 Typical Characteristics (continued)

T_A = 25°C, V_S = 12 V, R_{PULLUP} = 2.5 k, C_L = 20 pF, V_{CM} = 0 V, $V_{UNDERDRIVE}$ = 100 mV, $V_{OVERDRIVE}$ = 100 mV unless otherwise noted.

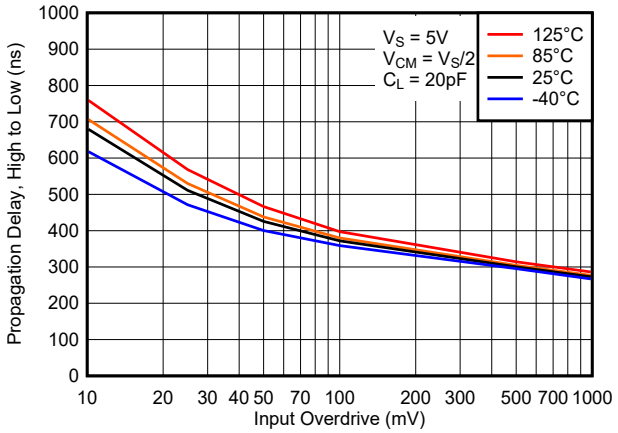


図 7-13. Propagation Delay, High to Low, 5 V

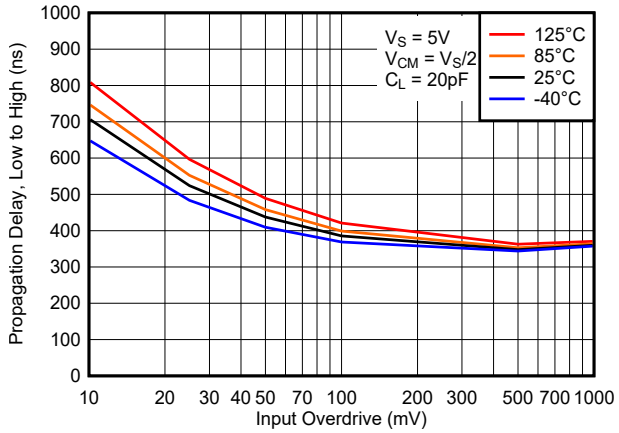


図 7-14. Propagation Delay, Low to High, 5 V

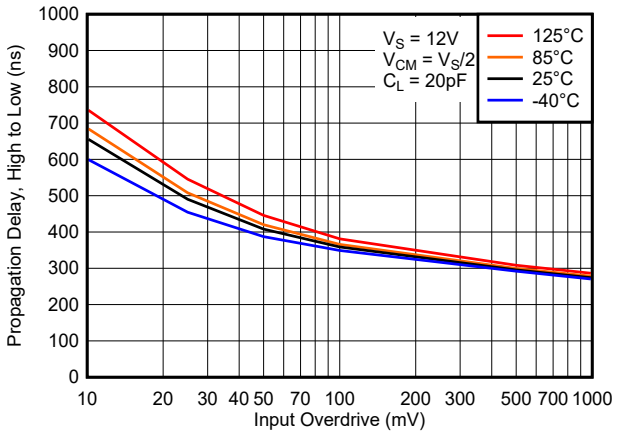


図 7-15. Propagation Delay, High to Low, 12 V

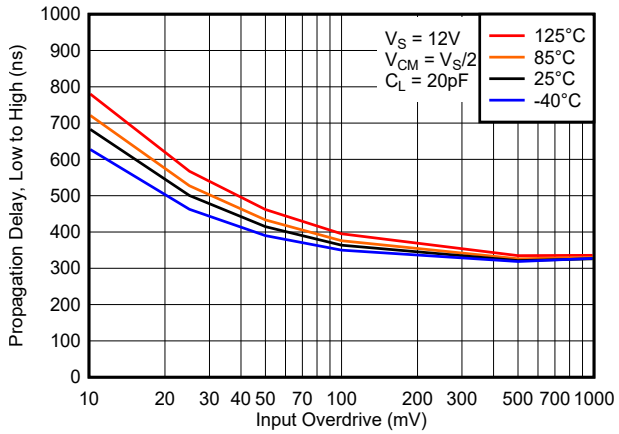


図 7-16. Propagation Delay, Low to High, 12 V

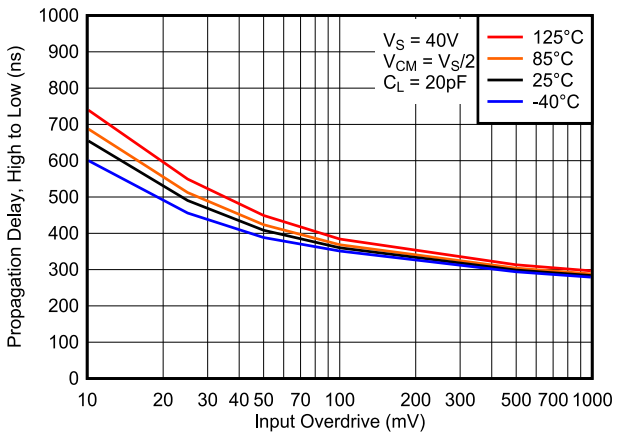


図 7-17. Propagation Delay, High to Low, 40 V

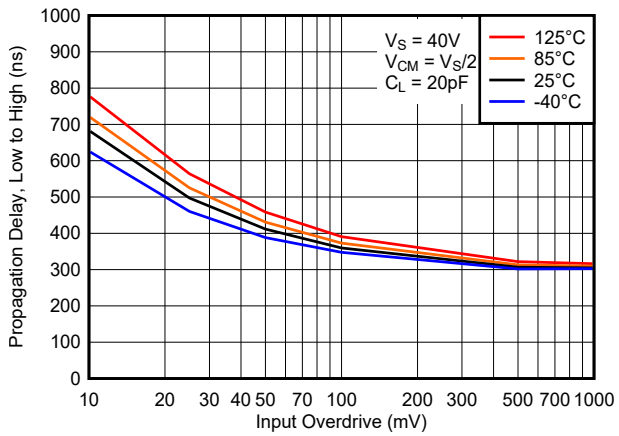


図 7-18. Propagation Delay, Low to High, 40 V

8 Detailed Description

8.1 Overview

The TLV181x-Q1 and TLV182x-Q1 devices are micro-power comparators with push-pull and open-drain output options. Operating down to 2.4 V while only consuming only 5 µA per channel, the TLV181x-Q1 and TLV182x-Q1 are well suited for portable, automotive and industrial applications. An internal power-on reset circuit ensures that the output remains in a known state during power-up and power-down.

8.2 Functional Block Diagrams

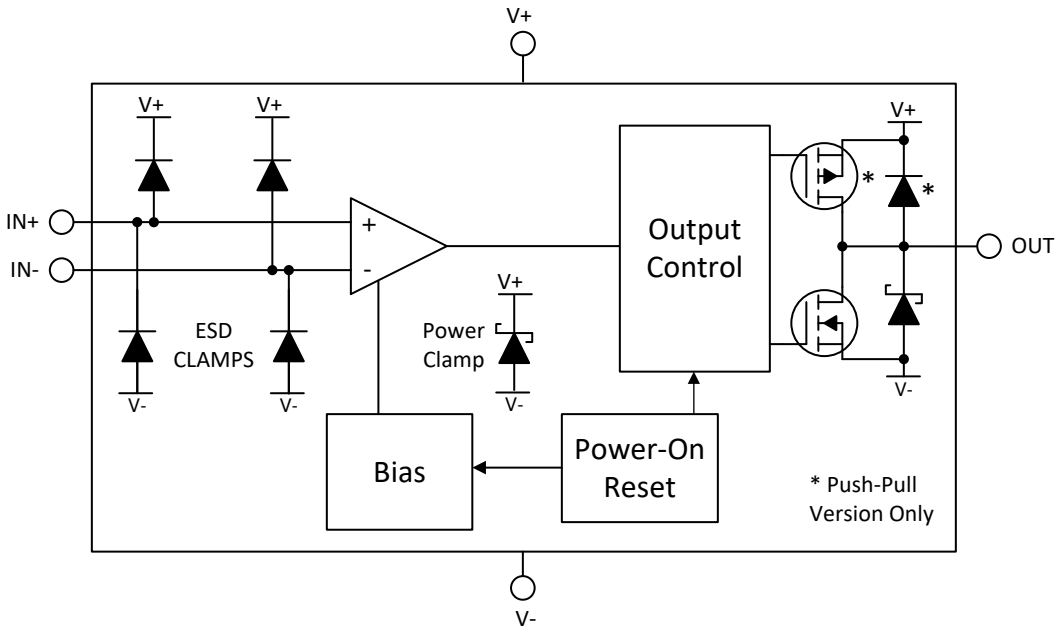


図 8-1. TLV18xx-Q1 Block Diagram

8.3 Feature Description

TLV18xx Family Options

The TLV18xxy family consists of several output and pinout options, all featuring 40 V operation, micro-power 5 µA supply currents, 420 ns propagation delay, and a Power-On Reset (POR) function.

The TLV18xx family has two output options:

The TLV18**1**x-Q1 has a **push-pull** (sink-source) output.

The TLV18**2**x-Q1 has a **open-drain** (sink only) output, capable of being pulled-up to any voltage up to 40 V, independent of comparator supply voltage.

The TLV1811L-Q1 and TLV1821L-Q1 are alternate pinouts of the TLV1811-Q1 and TLV1821-Q1 that allow upgrading older devices such as the TLV7211, TLV7221, LMC7211 and LMC7221 family.

8.4 Device Functional Modes

8.4.1 Inputs

8.4.1.1 TLV18xx Rail-to-Rail Input

The TLV18xx-Q1 input voltage range extends from 200 mV below V- to 200 mV above V+. The differential input voltage (V_{ID}) may be any voltage within these limits. No phase-inversion of the comparator output will occur when the input voltages stay within the specified range.

The Rail-to-Rail input does have an ESD clamp to the V+supply line and therefore the input voltage must not exceed the supply voltages by more than 200mV. It is not recommended to apply signals to the rail to rail inputs with no supply voltage.

8.4.1.2 ESD Protection

The TLV181x open-drain output ESD protection consists of a snapback ESD clamp between the output and V- to allow the output to be pulled above V+ to a maximum of 40 V. There is no "upper" ESD clamp diode between the output and V+ on the open-drain output. There is a "lower" clamp between V- and the output.

The TLV182x push-pull output ESD protection contains a conventional diode-type "upper" ESD clamp between the output and V+, and a "lower" ESD clamp between the output and V-. The output must not exceed the supply rails by more than 200mV.

If the inputs are to be connected to a low impedance source, such as a power supply or buffered reference line, TI recommends adding a current-limiting resistor in series with the input to limit any currents when the clamps conduct. The current must be limited 10 mA or less, though TI recommends limitng the current to 1mA or less. This series resistance may be part of any resistive input dividers or networks.

8.4.1.3 Unused Inputs

If a channel is not to be used, DO NOT tie the inputs together. Due to the high equivalent bandwidth and low offset voltage, tying the inputs directly together may cause high frequency chatter as the device triggers on it's own internal wideband noise. Instead, the inputs must be tied to any available voltage that resides within the specified input voltage range and provides a minimum of 50 mV differential voltage. For example, one input can be grounded and the other input connected to a reference voltage, or even V+ (as long as the input is directly connected to the V+ pin to avoid transients).

8.4.2 Outputs

8.4.2.1 TLV181x-Q1 Push-Pull Output

The TLV181x-Q1 features a push-pull output stage capable of both sinking and sourcing current. This allows driving loads such as LED's and MOSFET gates, as well as eliminating the need for a power-wasting external pull-up resistor. The push-pull output must never be connected to another output.

Directly shorting the output to the opposite supply rail (V+ when output "low" or V- when output "High") can result in thermal runaway and eventual device destruction at high (>12 V) supply voltages. If output shorts are possible, a series current limiting resistor is recommended to limit the power dissipation.

Unused push-pull outputs mustbe left floating, and never tied to a supply, ground, or another output.

8.4.2.2 TLV182x-Q1 Open-Drain Output

The TLV182x-Q1 features an open-drain (also commonly called open collector) sinking-only output stage enabling the output logic levels to be pulled up to an external voltage from 0 V up to 40 V, independent of the comparator supply voltage (V+). The open-drain output allows logical OR'ing of multiple open drain outputs and logic level translation. TI recommends setting the pull-up resistor current to between 100uA and 1mA. Lower value pull-up resistor values will help increase the rising edge rise-time, but at the expense of increasing V_{OL} and higher power dissipation. The rise-time is dependent on the time constant of the total pull-up resistance and total load capacitance. Large value pull-up resistors (>1 MΩ) will create an exponential rising edge due to the output RC time constant and increase the rise-time.

Directly shorting the output to V+ can result in thermal runaway and eventual device destruction at high (>12 V) pull-up voltages. If output shorts are possible, a series current limiting resistor is recommended to limit the power dissipation.

Unused open drain outputs may be left floating, or may be tied to the V- pin if floating pins are not desired.

8.4.3 Power-On Reset (POR)

The TLV18xx -Q1 family has an internal Power-on-Reset (POR) circuit for known start-up or power-down conditions. While the power supply (V+) is ramping up or ramping down, the POR circuitry will be activated for

up to 200 µs after the minimum supply voltage threshold of 2.4 V is crossed, or immediately when the supply voltage drops below 2.4 V. When the supply voltage is equal to or greater than the minimum supply voltage, and after the delay period, the comparator output reflects the state of the differential input (V_{ID}).

For the TLV181x-Q1 push-pull output devices, the output is held low during the POR period (t_{on}).

For the TLV182x-Q1 open drain output option the POR circuit will keep the output high impedance (Hi-Z) during the POR period (t_{on}).

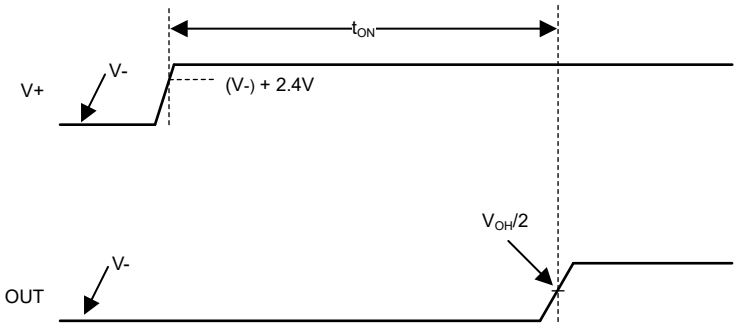


図 8-2. Power-On Reset Timing Diagram

Note: The output voltage rises with the pull-up voltage during the POR period.

8.4.4 Hysteresis

The TLV18xx-Q1 family does not have internal hysteresis. Due to the wide effective bandwidth and low input offset voltage, it is possible for the output to "chatter" when the absolute differential voltage is near zero as the comparator triggers on it's own internal wideband noise. This is normal comparator behavior and is expected. TI recommends that the user add external hysteresis if slow moving signals are expected. See セクション 9.1.2 in the following section.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Basic Comparator Definitions

9.1.1.1 Operation

The basic comparator compares the input voltage (V_{IN}) on one input to a reference voltage (V_{REF}) on the other input. In the 図 9-1 example below, if V_{IN} is less than V_{REF}, the output voltage (V_O) is logic low (V_{OL}). If V_{IN} is greater than V_{REF}, the output voltage (V_O) is at logic high (V_{OH}). 表 9-1 summarizes the output conditions. The output logic can be inverted by simply swapping the input pins.

表 9-1. Output Conditions

Inputs Condition	Output
IN+ > IN-	HIGH (V_{OH})
IN+ = IN-	Indeterminate (chatters - see Hysteresis)
IN+ < IN-	LOW (V_{OL})

9.1.1.2 Propagation Delay

There is a delay between from when the input crosses the reference voltage and the output responds. This is called the Propagation Delay. Propagation delay can be different between high-to low and low-to-high input transitions. This is shown as t_{pLH} and t_{pHL} in 図 9-1 and is measured from the mid-point of the input to the midpoint of the output.

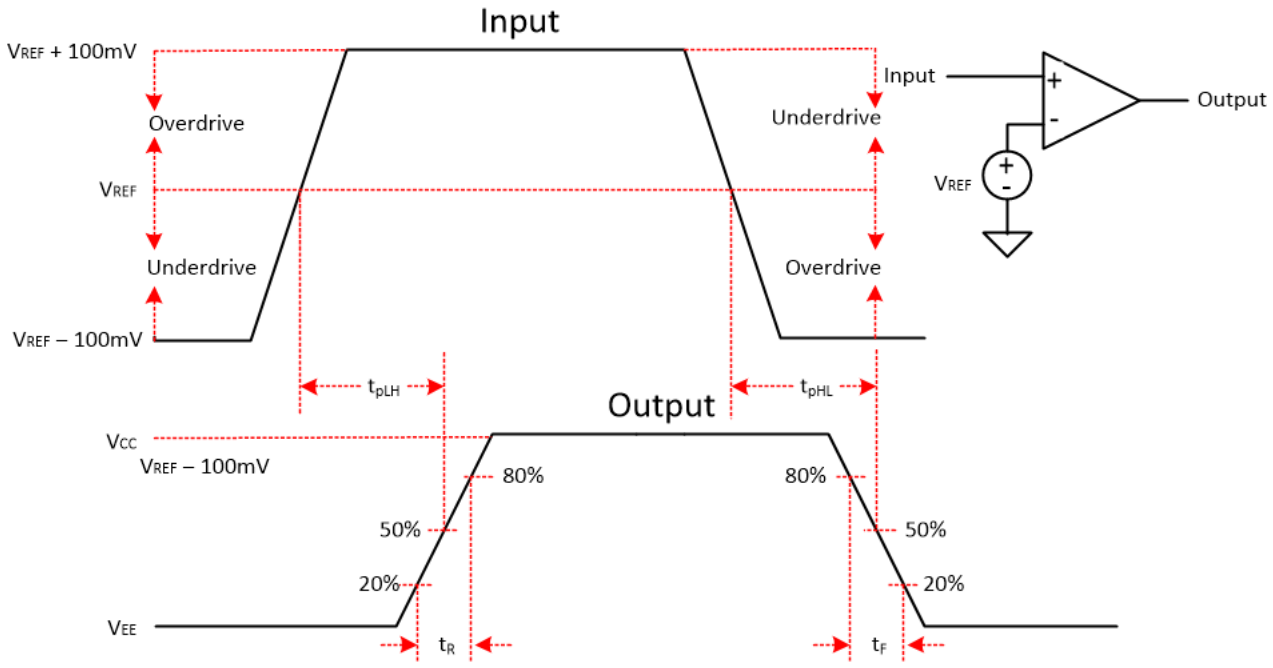


図 9-1. Comparator Timing Diagram

9.1.1.3 Overdrive Voltage

The overdrive voltage, V_{OD}, is the amount of input voltage beyond the reference voltage (and not the total input peak-to-peak voltage). The overdrive voltage is 100 mV as shown in the 図 9-1 example. The overdrive voltage can influence the propagation delay (t_p). The smaller the overdrive voltage, the longer the propagation delay, particularly when <100mV. If the fastest speeds are desired, it is recommended to apply the highest amount of overdrive possible.

The risetime (t_r) and falltime (t_f) is the time from the 20% and 80% points of the output waveform.

9.1.2 Hysteresis

The basic comparator configuration may oscillate or produce a noisy "chatter" output if the applied differential input voltage is near the comparator's offset voltage. This usually occurs when the input signal is moving very slowly across the switching threshold of the comparator.

This problem can be prevented by the addition of hysteresis or positive feedback.

The hysteresis transfer curve is shown in 図 9-2. This curve is a function of three components: V_{TH}, V_{OS}, and V_{HYST}:

- V_{TH} is the actual set voltage or threshold trip voltage.
- V_{OS} is the internal offset voltage between V_{IN+} and $V_{IN–}$. This voltage is added to V_{TH} to form the actual trip point at which the comparator must respond to change output states.
- V_{HYST} is the hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise.

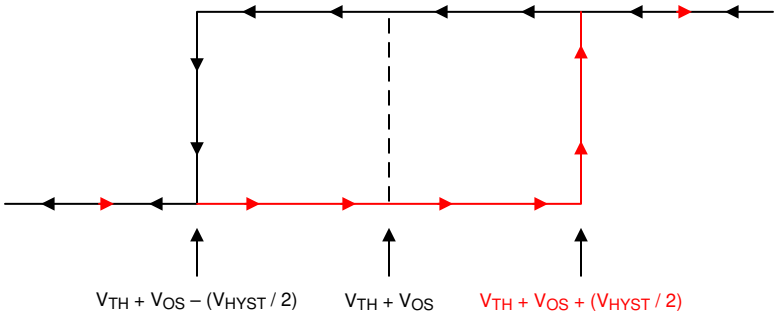


図 9-2. Hysteresis Transfer Curve

For more information, please see Application Note SBOA219 "Comparator with and without hysteresis circuit".

9.1.2.1 Inverting Comparator With Hysteresis

The inverting comparator with hysteresis requires a three-resistor network that is referenced to the comparator supply voltage (V_{CC}), as shown in 図 9-3.

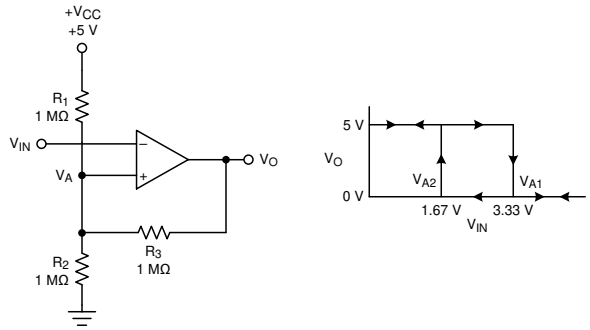


図 9-3. TLV181x-Q1in an Inverting Configuration With Hysteresis

The equivalent resistor networks when the output is high and low are shown in 図 9-3.

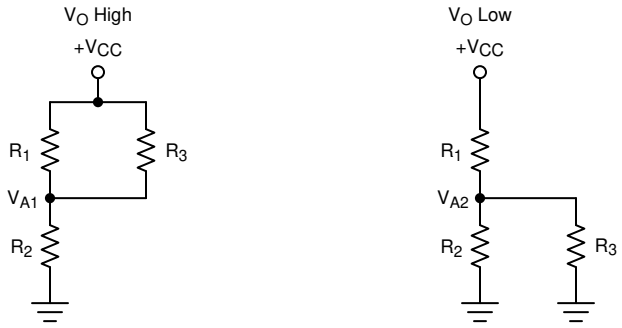


図 9-4. Inverting Configuration Resistor Equivalent Networks

When V_{IN} is less than V_A, the output voltage is high (for simplicity, assume V_O switches as high as V_{CC}). The three network resistors can be represented as R1 || R3 in series with R2, as shown in 図 9-4.

式 1 below defines the high-to-low trip voltage (V_{A1}).

$$V_{A1} = V_{CC} \times \frac{R2}{(R1 \parallel R3) + R2} \tag{1}$$

When V_{IN} is greater than V_A, the output voltage is low. In this case, the three network resistors can be presented as R2 || R3 in series with R1, as shown in 式 2.

Use 式 2 to define the low to high trip voltage (V_{A2}).

$$V_{A2} = V_{CC} \times \frac{R2 \parallel R3}{R1 + (R2 \parallel R3)} \tag{2}$$

式 3 defines the total hysteresis provided by the network.

$$\Delta V_A = V_{A1} - V_{A2} \tag{3}$$

9.1.2.2 Non-Inverting Comparator With Hysteresis

A non-inverting comparator with hysteresis requires a two-resistor network and a voltage reference (V_{REF}) at the inverting input, as shown in 図 9-5,

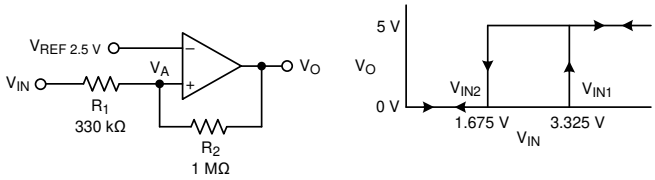


図 9-5. TLV181x-Q1 in a Non-Inverting Configuration With Hysteresis

The equivalent resistor networks when the output is high and low are shown in 図 9-6.

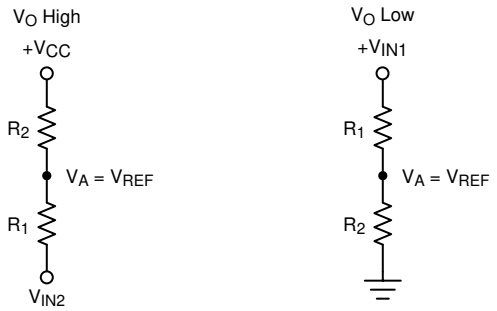


図 9-6. Non-Inverting Configuration Resistor Networks

When V_{IN} is less than V_{REF},, the output is low. For the output to switch from low to high, V_{IN} must rise above the V_{IN1} threshold. Use 式 4 to calculate V_{IN1}.

$$V_{IN1} = R1 \times \frac{V_{REF}}{R2} + V_{REF} \tag{4}$$

When V_{IN} is greater than V_{REF}, the output is high. For the comparator to switch back to a low state, V_{IN} must drop below V_{IN2}. Use 式 5 to calculate V_{IN2}.

$$V_{IN2} = \frac{V_{REF}\,(R1 + R2) - V_{CC} \times R1}{R2} \tag{5}$$

The hysteresis of this circuit is the difference between V_{IN1} and V_{IN2}, as shown in 式 6.

$$\Delta V_{IN} = V_{CC} \times \frac{R1}{R2} \tag{6}$$

For more information, please see Application Notes SNOA997 "Inverting comparator with hysteresis circuit" and SBOA313 "Non-Inverting Comparator With Hysteresis Circuit".

9.1.2.3 Inverting and Non-Inverting Hysteresis using Open-Drain Output

It is also possible to use an open drain output device, such as the TLV182x-Q1, but the output pull-up resistor must also be taken into account in the calculations. The pull-up resistor is seen in series with the feedback resistor when the output is high. Thus, the feedback resistor is actually seen as R2 + R_{PULLUP}. TI recommends that the pull-up resistor be at least 10 times less than the feedback resistor value.

9.2 Typical Applications

9.2.1 Window Comparator

Window comparators are commonly used to detect undervoltage and overvoltage conditions. 図 9-7 shows a simple window comparator circuit. Window comparators require open drain outputs (TLV182x-Q1) if the outputs are directly connected together.

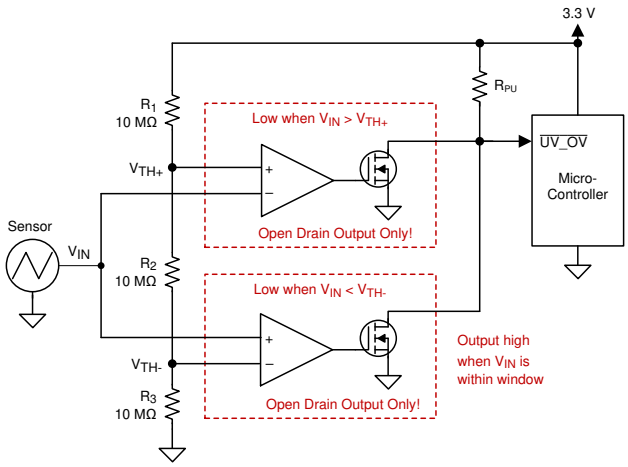


図 9-7. Window Comparator

9.2.1.1 Design Requirements

For this design, follow these design requirements:

- Alert (logic low output) when an input signal is less than 1.1 V
- Alert (logic low output) when an input signal is greater than 2.2 V
- Alert signal is active low
- Operate from a 3.3-V power supply

9.2.1.2 Detailed Design Procedure

Configure the circuit as shown in 図 9-7. Connect V_{CC} to a 3.3-V power supply and V_{EE} to ground. Make R1, R2 and R3 each 10-MΩ resistors. These three resistors are used to create the positive and negative thresholds for the window comparator (V_{TH+} and $V_{TH–}$).

With each resistor being equal, V_{TH+} is 2.2 V and V_{TH-} is 1.1 V. Large resistor values such as 10-MΩ are used to minimize power consumption. The resistor values may be recalculated to provide the desired trip point values.

The sensor output voltage is applied to the inverting and noninverting inputs of the two comparators. Using two open-drain output comparators allows the two comparator outputs to be Wire-OR'ed together.

The respective comparator outputs will be low when the sensor is less than 1.1 V or greater than 2.2 V. The respective comparator outputs will be high when the sensor is in the range of 1.1 V to 2.2 V (within the "window"), as shown in 図 9-8.

9.2.1.3 Application Curve

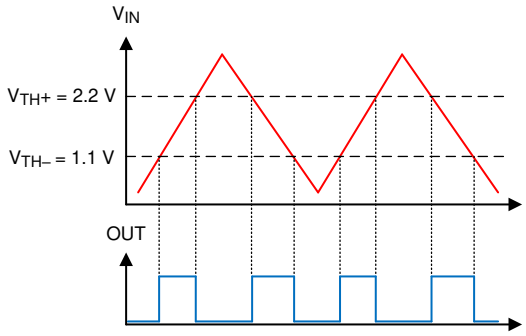


図 9-8. Window Comparator Results

For more information, please see Application note SBOA221 "Window comparator circuit".

9.2.2 Square-Wave Oscillator

Square-wave oscillator can be used as low cost timing reference or system supervisory clock source. A push-pull output (TLV181x-Q1) is recommended for best symmetry.

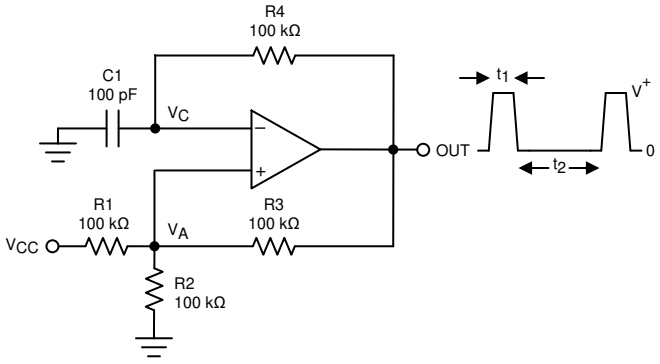


図 9-9. Square-Wave Oscillator

9.2.2.1 Design Requirements

The square-wave period is determined by the RC time constant of the capacitor C_1 and resistor R_4. The maximum frequency is limited by propagation delay of the device and the capacitance load at the output. The low input bias current allows a lower capacitor value and larger resistor value combination for a given oscillator frequency, which may help to reduce BOM cost and board space. TI recommends that R4 be over several kilo-ohms to minimize loading of the output.

9.2.2.2 Detailed Design Procedure

The oscillation frequency is determined by the resistor and capacitor values. The following calculation provides details of the steps.

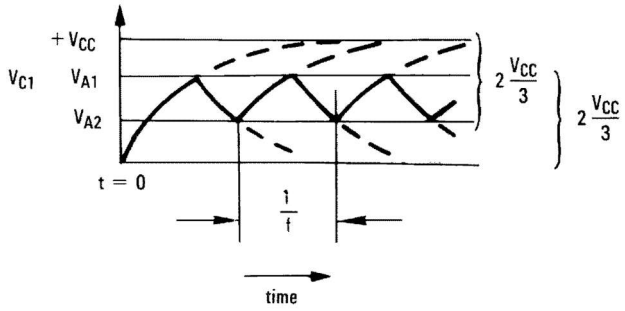


図 9-10. Square-Wave Oscillator Timing Thresholds

First consider the output of Figure 図 9-9 as high, which indicates the inverted input V_C is lower than the noninverting input (V_A). This causes the C_1 to be charged through R_4, and the voltage V_C increases until it is equal to the noninverting input. The value of V_A at the point is calculated by 式 7.

$$V_{A1} = \frac{V_{CC} \times R_2}{R_2 + R_1 \| R_3} \tag{7}$$

if $R_1 = R_2 = R_3$, then $V_{A1} = 2\ V_{CC}/\ 3$

At this time the comparator output trips pulling down the output to the negative rail. The value of $V_A$at this point is calculated by 式 8.

$$V_{A2} = \frac{V_{CC}(R_2 \| R_3)}{R_1 + R_2 \| R_3} \quad (8)$$

if $R_1 = R_2 = R_3$, then $V_{A2} = V_{CC}/3$

The C_1 now discharges though the R_4, and the voltage V_{CC} decreases until it reaches V_{A2}. At this point, the output switches back to the starting state. The oscillation period equals to the time duration from for C_1 from $2V_{CC}/3$ to V_{CC} / 3 then back to $2V_{CC}/3$, which is given by R_4C_1 × ln 2 for each trip. Therefore, the total time duration is calculated as 2 R_4C_1 × ln 2.

The oscillation frequency can be obtained by 式 9:

$$f = 1/(2\ R4 \times C1 \times In2) \quad (9)$$

9.2.2.3 Application Curve

図 9-11 shows the simulated results of an oscillator using the following component values:

- $R_1 = R_2 = R_3 = R_4 = 100\ k\Omega$
- $C_1 = 100\ pF$, $C_L = 20\ pF$
- V+ = 5 V, V– = GND
- C_{stray} (not shown) from V_A TO GND = 10 pF

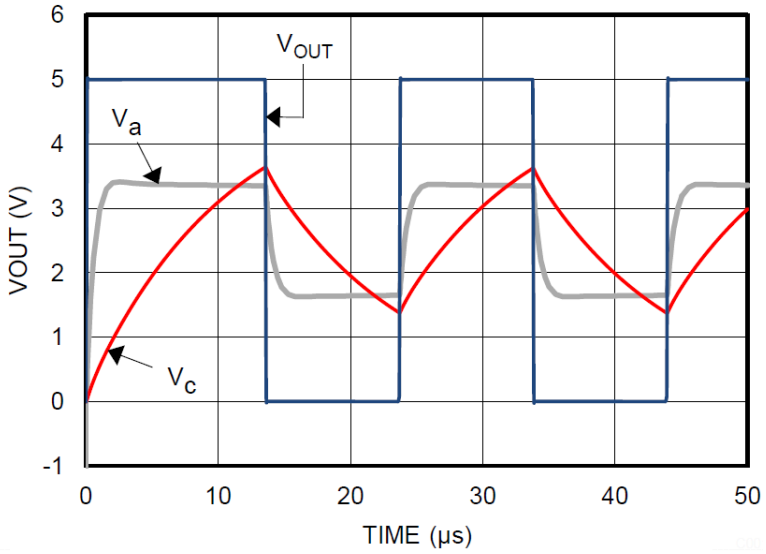


図 9-11. Square-Wave Oscillator Output Waveform

9.2.3 Adjustable Pulse Width Generator

図 9-12 is a variation on the square wave oscillator that allows adjusting the pulse widths.

R_4 and R_5 provide separate charge and discharge paths for the capacitor C depending on the output state.

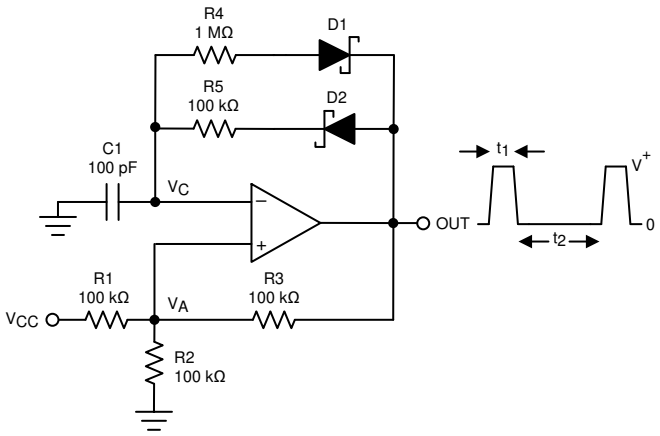


図 9-12. Adjustable Pulse Width Generator

The charge path is set through R_5 and D_2 when the output is high. Similarly, the discharge path for the capacitor is set by R_4 and D_1 when the output is low.

The pulse width t_1 is determined by the RC time constant of R_5 and C. Thus, the time t_2 between the pulses can be changed by varying R_4, and the pulse width can be altered by R_5. The frequency of the output can be changed by varying both R_4 and R_5. At low voltages, the effects of the diode forward drop (0.8 V, or 0.15 V for Shottky) must be taken into account by altering output high and low voltages in the calculations.

9.2.4 Time Delay Generator

The circuit shown in 図 9-13 provides output signals at a prescribed time interval from a time reference and automatically resets the output low when the input returns to 0 V. This is useful for sequencing a "power on" signal to trigger a controlled start-up of power supplies.

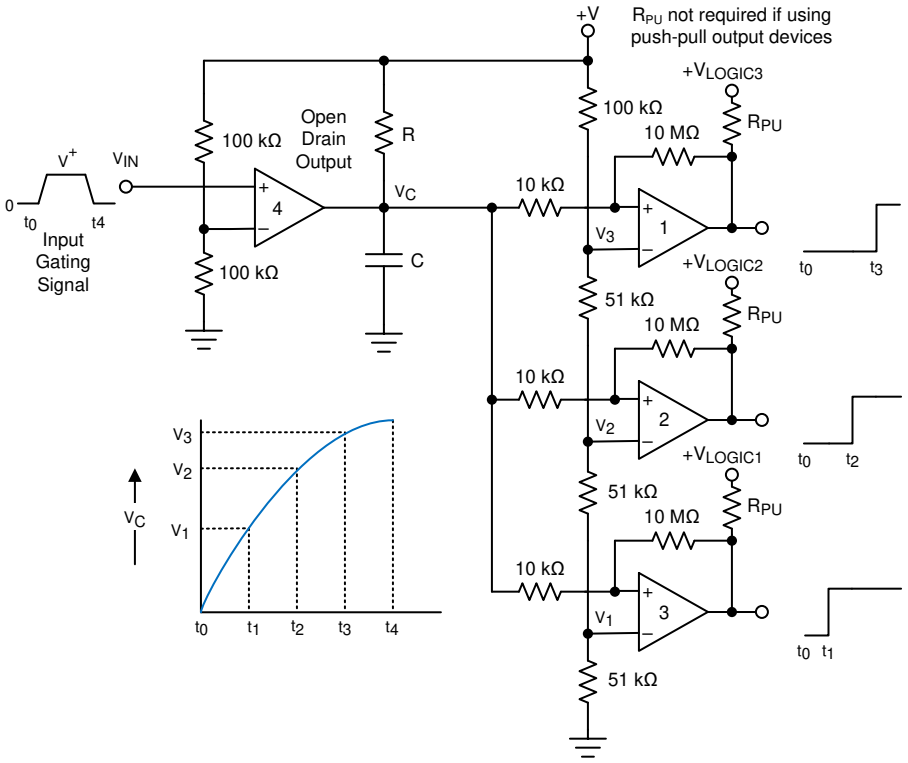


図 9-13. Time Delay Generator

Consider the case of V_{IN} = 0. The output of comparator 4 is also at ground, "shorting" the capacitor and holding it at 0V. This implies that the outputs of comparators 1, 2, and 3 are also at 0V. When an input signal is applied, the output of open drain comparator 4 goes High-Z and C charges exponentially through R. This is indicated in the graph. The output voltages of comparators 1, 2, and 3 switch to the high state in sequence when V_C rises above the reference voltages V_1, V_2 and V_3. A small amount of hysteresis has been provided by the 10 kΩ and 10 MΩ resistors to insure fast switching when the RC time constant is chosen to give long delay times. A good starting point is R = 100 kΩ and C = 0.01 µF to 1 µF.

All outputs will immediately go low when V_{IN} falls to 0V, due to the comparator output going low and immediately discharging the capacitor.

Comparator 4 must be a open-drain type output (TLV182x-Q1), whereas comparators 1 though 3 may be either open drain or push-pull output, depending on system requirements. R_{PU} is not required for push-pull output devices.

9.2.5 Logic Level Shifter

The output of the TLV182x-Q1 is the uncommitted drain of the output transistor. Many open-drain outputs can be tied together to provide an output OR'ing function if desired.

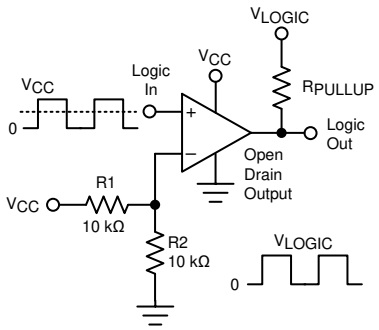


図 9-14. Universal Logic Level Shifter

The two 10 kΩ resistors bias the input to half of the input logic supply level to set the threshold in the mid-point of the input logic levels. Only one shared output pull-up resistor is needed and may be connected to any pull-up voltage between 0 V and 5.5 V. The pullup voltage should match the driven logic input "high" level.

9.2.6 One-Shot Multivibrator

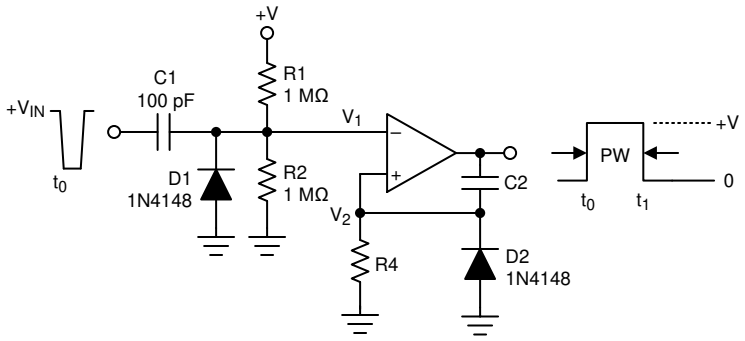


図 9-15. One-Shot Multivibrator

A monostable multivibrator has one stable state in which it can remain indefinitely. It can be triggered externally to another quasi-stable state. A monostable multivibrator can thus be used to generate a pulse of desired width.

The desired pulse width is set by adjusting the values of C_2 and R_4. The resistor divider of R_1 and R_2 can be used to determine the magnitude of the input trigger pulse. The output will change state when $V_1 < V_2$. Diode D_2 provides a rapid discharge path for capacitor C_2 to reset at the end of the pulse. The diode also prevents the non-inverting input from being driven below ground.

9.2.7 Bi-Stable Multivibrator

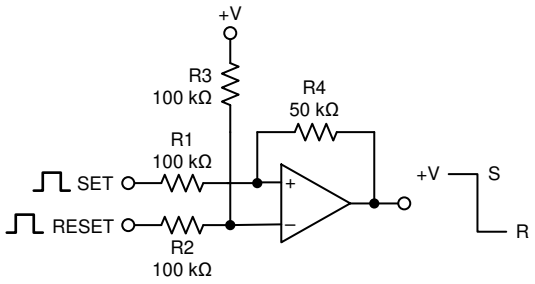


図 9-16. Bi-Stable Multivibrator

A bi-stable multivibrator has two stable states. The reference voltage is set up by the voltage divider of R_2 and R_3. A pulse applied to the SET terminal will switch the output of the comparator high. The resistor divider of R_1 and R4 now sets the non-inverting input to a voltage greater than the reference voltage. A pulse applied to RESET will now toggle the output low.

9.2.8 Zero Crossing Detector

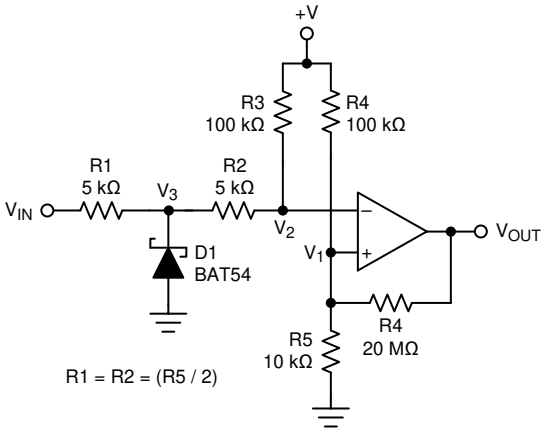


図 9-17. Zero Crossing Detector

A voltage divider of R_4 and R_5 establishes a reference voltage V_1 at the non-inverting input. By making the series resistance of R_1 and R_2 equal to R_5, the comparator will switch when V_{IN} = 0. Diode D_1 insures that V_3 clamps near ground. The voltage divider of R_2 and R_3 then prevents V_2 from going below ground. A small amount of hysteresis is setup to ensure rapid output voltage transitions.

9.2.9 Pulse Slicer

A Pulse Slicer is a variation of the Zero Crossing Detector and is used to detect the zero crossings on an input signal with a varying baseline level. This circuit works best with symmetrical waveforms. The RC network of R_1 and C_1 establishes an mean reference voltage V_{REF}, which tracks the mean amplitude of the V_{IN} signal. The non-inverting input is directly connected to V_{REF} through R2. R2 and R3 are used to produce hysteresis to keep transitions free of spurious toggles. The time constant is a tradeoff between long-term symmetry and response time to changes in amplitude.

If the waveform is data, it is recommended that the data be encoded in NRZ (Non-Return to Zero) format to maintain proper average baseline. Asymmetrical inputs may suffer from timing distortions caused by the changing V_{REF} average voltage.

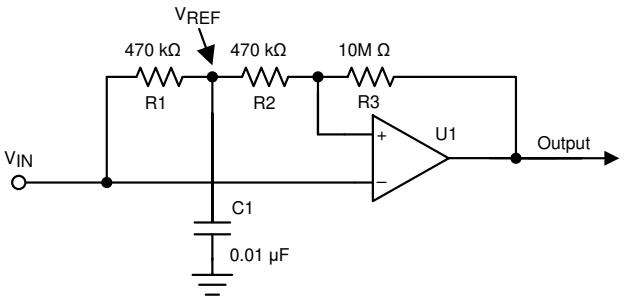


図 9-18. Pulse Slicer

For this design, follow these design requirements:

- The RC constant value (R_2 and C_1) must support the targeted data rate to maintain a valid tripping threshold.
- The hysteresis introduced with R_2 and R_{43} helps to avoid spurious output toggles.

The TLV182x-Q1 may also be used, but with the addition of a pull-up resistor on the output (not shown for clarity).

図 9-19 shows the results of a 9600 baud data signal riding on a varying baseline.

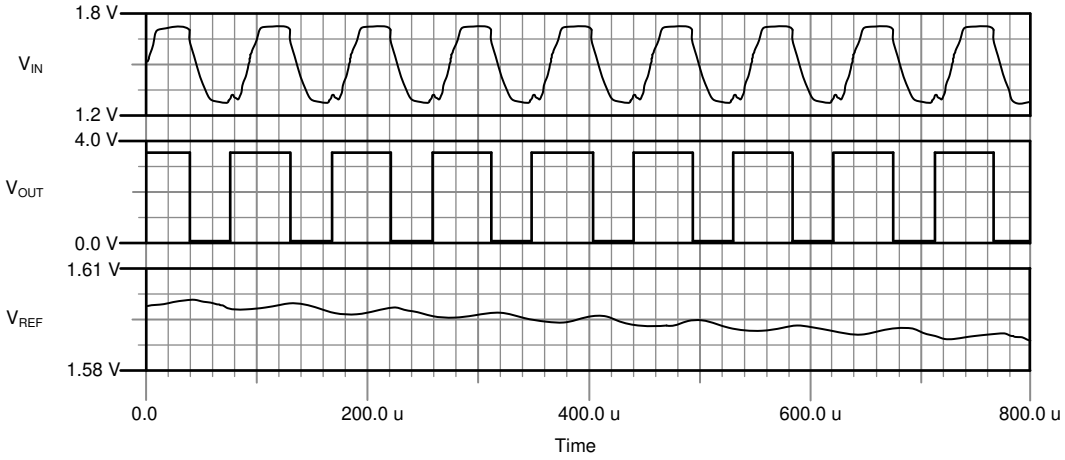


図 9-19. Pulse Slicer Waveforms

9.3 Power Supply Recommendations

Due to the fast output edges, it is critical to have bypass capacitors on the supply pin to prevent supply ringing and false triggers and oscillations. Bypass the supply directly at *each* device with a low ESR 0.1 µF ceramic bypass capacitor directly between V_{CC} pin and ground pins. Narrow, peak currents will be drawn during the output transition time, particularly for the push-pull output device. These narrow pulses can cause un-bypassed supply lines and poor grounds to ring, possibly causing variation that can eat into the input voltage range and create an inaccurate comparison or even oscillations.

The device may be powered from both "split" supplies (V+ and V-), or "single" supplies (V+ and GND), with GND applied to the V- pin. Input signals must stay within the specified input range (between V+ and V-) for either type. Note that with a "split" supply the ouptut will now swing "low" (V_{OL}) to V- potential and not GND.

9.4 Layout

9.4.1 Layout Guidelines

For accurate comparator applications it is important maintain a stable power supply with minimized noise and glitches. Output rise and fall times are in the tens of nanoseconds, and should be treated as high speed logic devices. The bypass capacitor should be as close to the supply pin as possible and connected to a solid ground plane, and preferably directly between the V_{CC} and GND pins.

Minimize coupling between outputs and inputs to prevent output oscillations. Do not run output and input traces in parallel unless there is a V_{CC} or GND trace between output to reduce coupling. When series resistance is added to inputs, place resistor close to the device. A low value (<100 ohms) resistor may also be added in series with the output to dampen any ringing or reflections on long, non-impedance controlled traces. For best edge shapes, controlled impedance traces with back-terminations should be used when routing long distances.

9.4.2 Layout Example

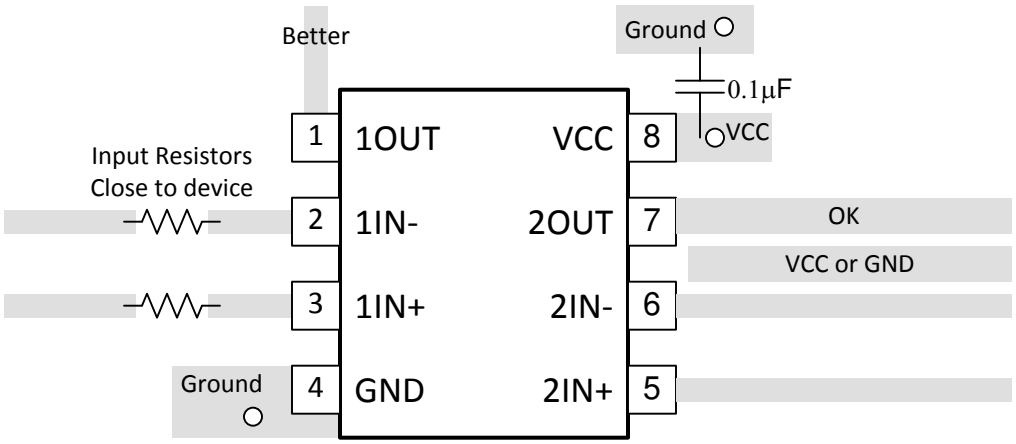


図 9-20. Dual Layout Example

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

Analog Engineers Circuit Cookbook: Amplifiers (See Comparators section) - SLYY137

Precision Design, Comparator with Hysteresis Reference Design— TIDU020

Window comparator circuit - SBOA221

Reference Design, Window Comparator Reference Design— TIPD178

Comparator with and without hysteresis circuit - SBOA219

Inverting comparator with hysteresis circuit - SNOA997

Non-Inverting Comparator With Hysteresis Circuit - SBOA313

Zero crossing detection using comparator circuit - SNOA999

PWM generator circuit - SBOA212

How to Implement Comparators for Improving Performance of Rotary Encoder in Industrial Drive Applications - SNOAA41

A Quad of Independently Func Comparators - SNOA654

10.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

10.3 サポート・リソース

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10.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV1811LQDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2XPT
TLV1811LQDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2XPT
TLV1811QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2XOT
TLV1811QDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2XOT
TLV1811QDCKRQ1	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2XWT
TLV1811QDCKRQ1.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2XWT
TLV1812QDDFRQ1	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	32BF
TLV1812QDDFRQ1.A	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	32BF
TLV1812QDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	31SS
TLV1812QDGKRQ1.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	31SS
TLV1812QDRQ1	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T1812Q
TLV1812QDRQ1.A	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T1812Q
TLV1812QPWRQ1	Active	Production	TSSOP (PW) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T1812Q
TLV1812QPWRQ1.A	Active	Production	TSSOP (PW) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T1812Q
TLV1814QDRQ1	Active	Production	SOIC (D) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV1814Q
TLV1814QDRQ1.A	Active	Production	SOIC (D) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV1814Q
TLV1814QDYYRQ1	Active	Production	SOT-23-THIN (DYY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV1814QB1
TLV1814QDYYRQ1.A	Active	Production	SOT-23-THIN (DYY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV1814QB1
TLV1814QPWRQ1	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T1814BQ
TLV1814QPWRQ1.A	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T1814BQ
TLV1821LQDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2XRT
TLV1821LQDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2XRT
TLV1821QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2XQT
TLV1821QDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2XQT
TLV1821QDCKRQ1	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2XVT
TLV1821QDCKRQ1.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2XVT
TLV1822QDDFRQ1	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	32CF
TLV1822QDDFRQ1.A	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	32CF

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV1822QDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	31TS
TLV1822QDGKRQ1.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	31TS
TLV1822QDRQ1	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T1822Q
TLV1822QDRQ1.A	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T1822Q
TLV1822QPWRQ1	Active	Production	TSSOP (PW) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T1822Q
TLV1822QPWRQ1.A	Active	Production	TSSOP (PW) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T1822Q
TLV1824QDRQ1	Active	Production	SOIC (D) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV1824Q
TLV1824QDRQ1.A	Active	Production	SOIC (D) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV1824Q
TLV1824QDYYRQ1	Active	Production	SOT-23-THIN (DYY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV1824QDYY
TLV1824QDYYRQ1.A	Active	Production	SOT-23-THIN (DYY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV1824QDYY
TLV1824QPWRQ1	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T1824BQ
TLV1824QPWRQ1.A	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T1824BQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TLV1811-Q1, TLV1812-Q1, TLV1814-Q1, TLV1821-Q1, TLV1822-Q1, TLV1824-Q1 :

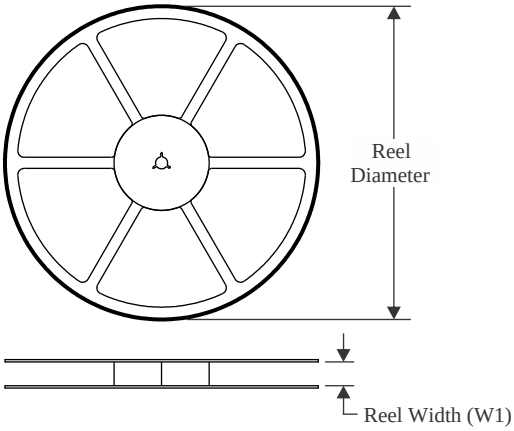
- Catalog : TLV1811, TLV1812, TLV1814, TLV1821, TLV1822, TLV1824
- Enhanced Product : TLV1812-EP, TLV1822-EP

NOTE: Qualified Version Definitions:

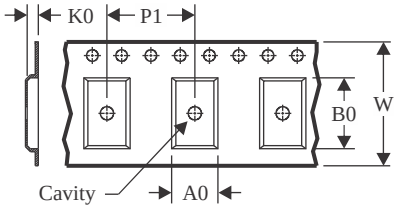
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

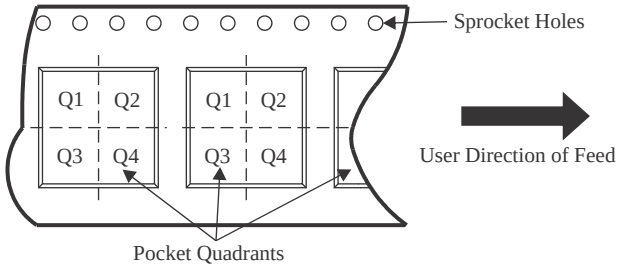


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

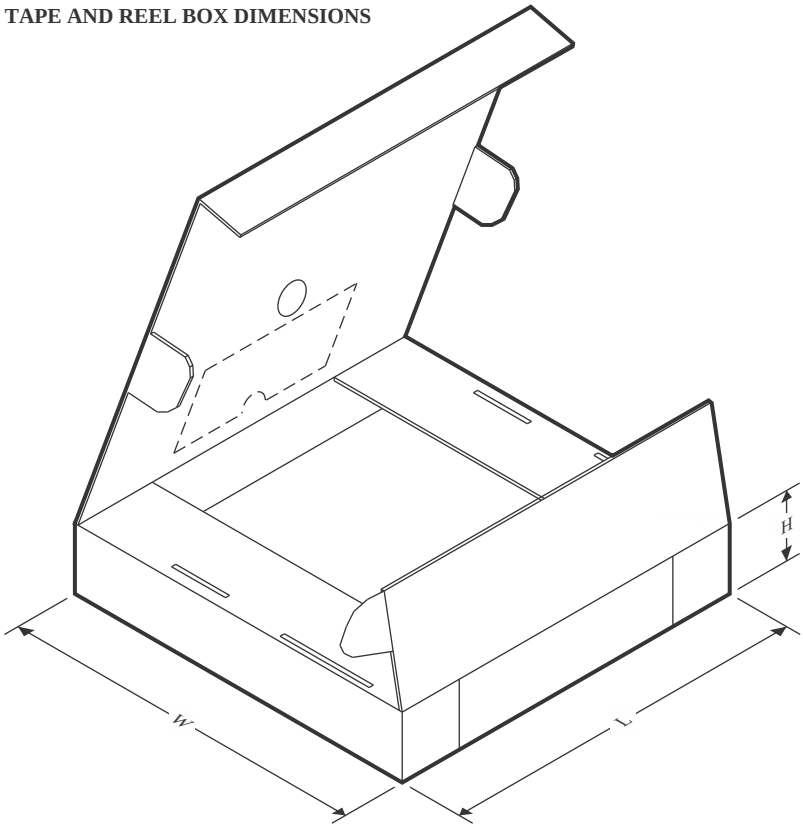


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV1811LQDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV1811QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV1811QDCKRQ1	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV1812QDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV1812QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV1812QDRQ1	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV1812QPWRQ1	TSSOP	PW	8	3000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV1814QDRQ1	SOIC	D	14	3000	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV1814QDYYRQ1	SOT-23-THIN	DYY	14	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
TLV1814QPWRQ1	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV1821LQDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV1821QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV1821QDCKRQ1	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV1822QDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV1822QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV1822QDRQ1	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV1822QPWRQ1	TSSOP	PW	8	3000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV1824QDRQ1	SOIC	D	14	3000	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV1824QDYYRQ1	SOT-23-THIN	DYY	14	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
TLV1824QPWRQ1	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV1811LQDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV1811QDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV1811QDCKRQ1	SC70	DCK	5	3000	180.0	180.0	18.0
TLV1812QDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TLV1812QDGKRQ1	VSSOP	DGK	8	2500	353.0	353.0	32.0
TLV1812QDRQ1	SOIC	D	8	3000	353.0	353.0	32.0
TLV1812QPWRQ1	TSSOP	PW	8	3000	353.0	353.0	32.0
TLV1814QDRQ1	SOIC	D	14	3000	353.0	353.0	32.0
TLV1814QDYYRQ1	SOT-23-THIN	DYY	14	3000	336.6	336.6	31.8
TLV1814QPWRQ1	TSSOP	PW	14	3000	353.0	353.0	32.0
TLV1821LQDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV1821QDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV1821QDCKRQ1	SC70	DCK	5	3000	180.0	180.0	18.0
TLV1822QDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TLV1822QDGKRQ1	VSSOP	DGK	8	2500	353.0	353.0	32.0
TLV1822QDRQ1	SOIC	D	8	3000	353.0	353.0	32.0
TLV1822QPWRQ1	TSSOP	PW	8	3000	353.0	353.0	32.0
TLV1824QDRQ1	SOIC	D	14	3000	353.0	353.0	32.0

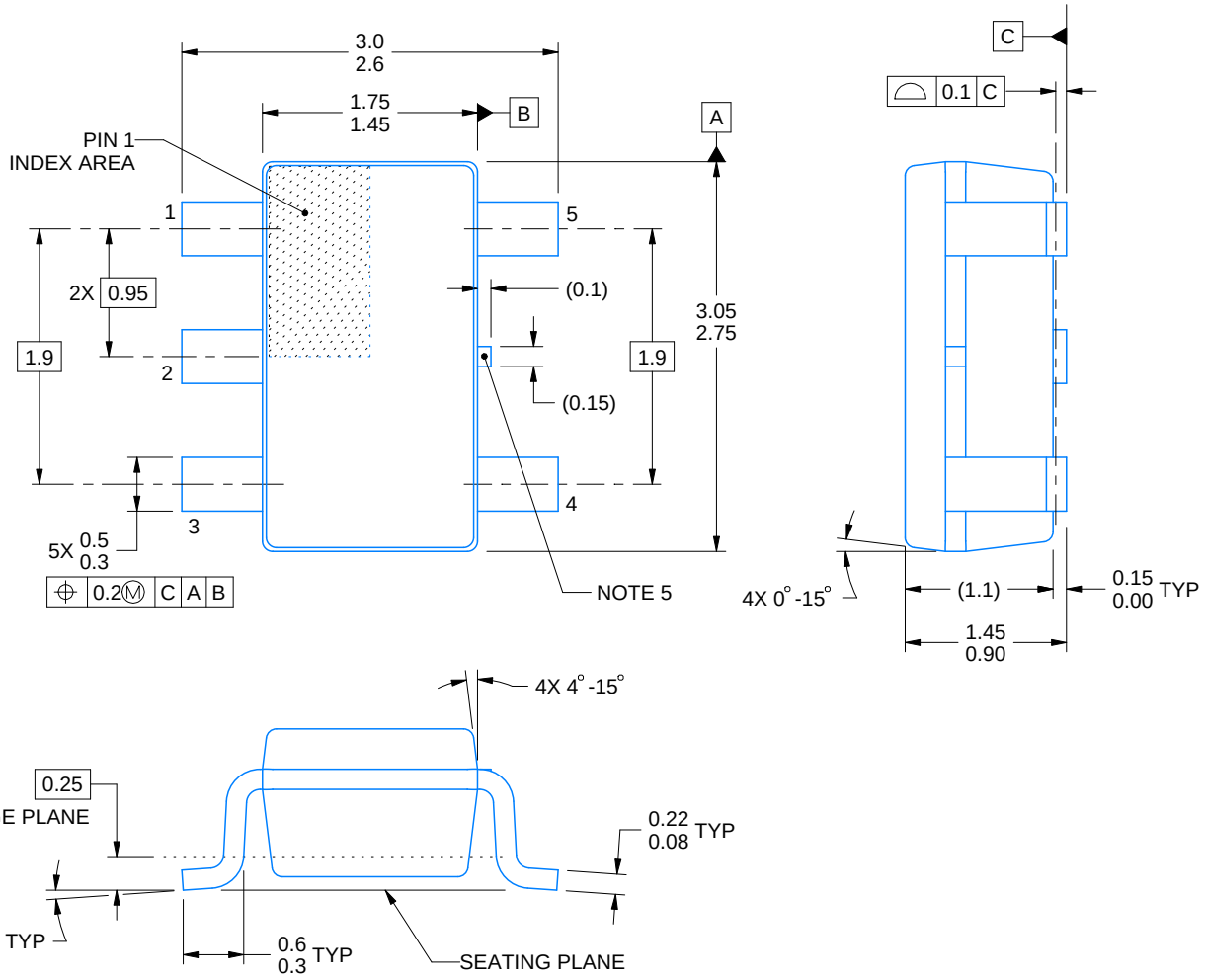
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV1824QDYYRQ1	SOT-23-THIN	DYY	14	3000	336.6	336.6	31.8
TLV1824QPWRQ1	TSSOP	PW	14	3000	353.0	353.0	32.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

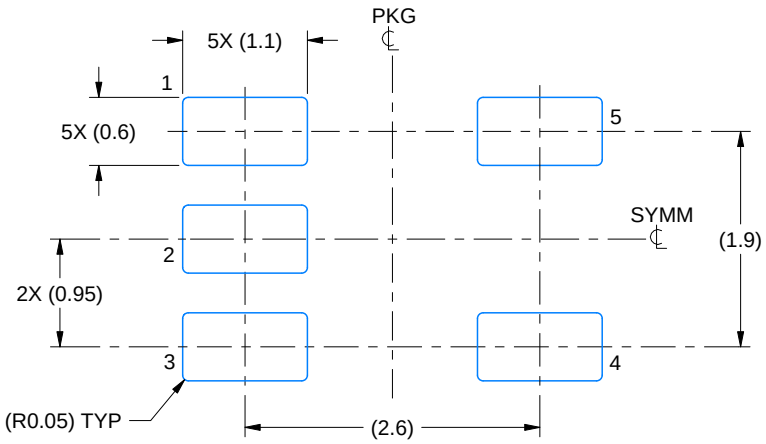
SMALL OUTLINE TRANSISTOR



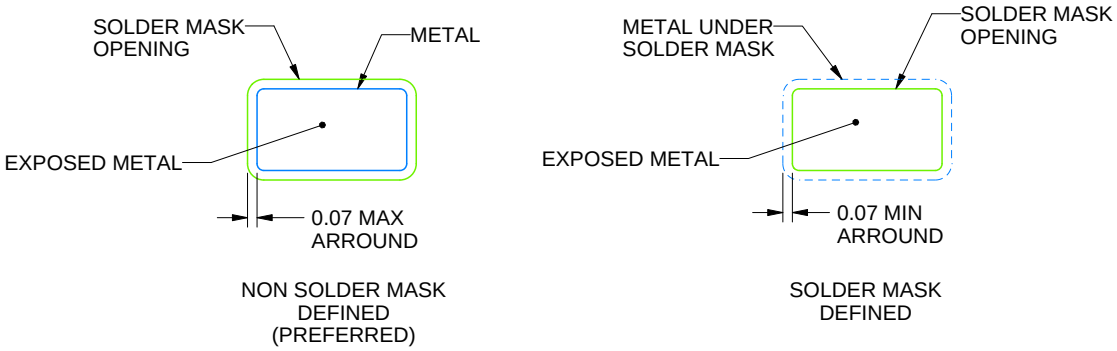
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

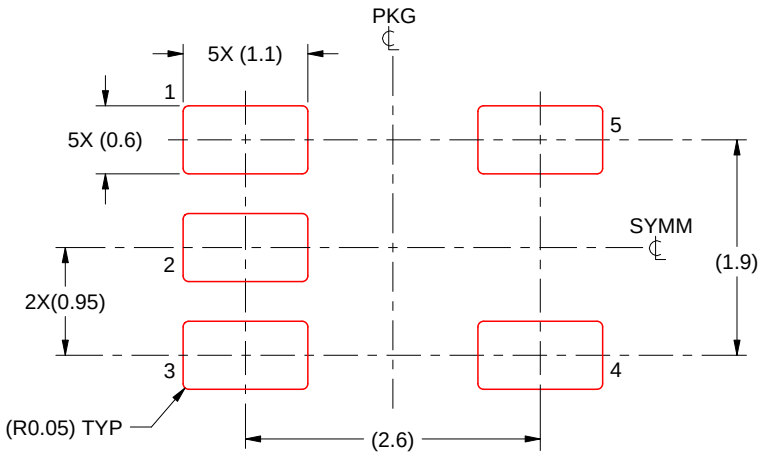


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

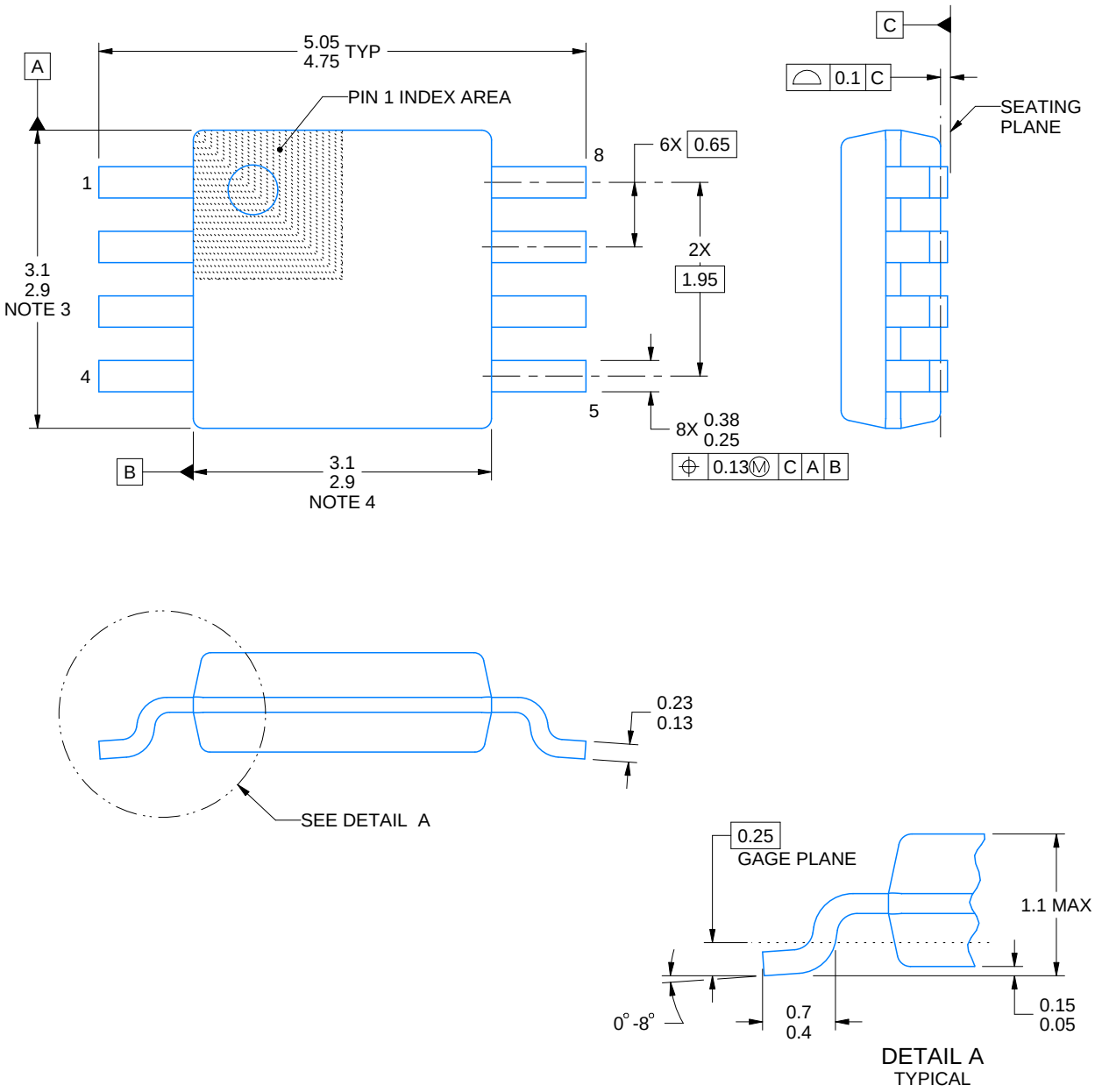
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

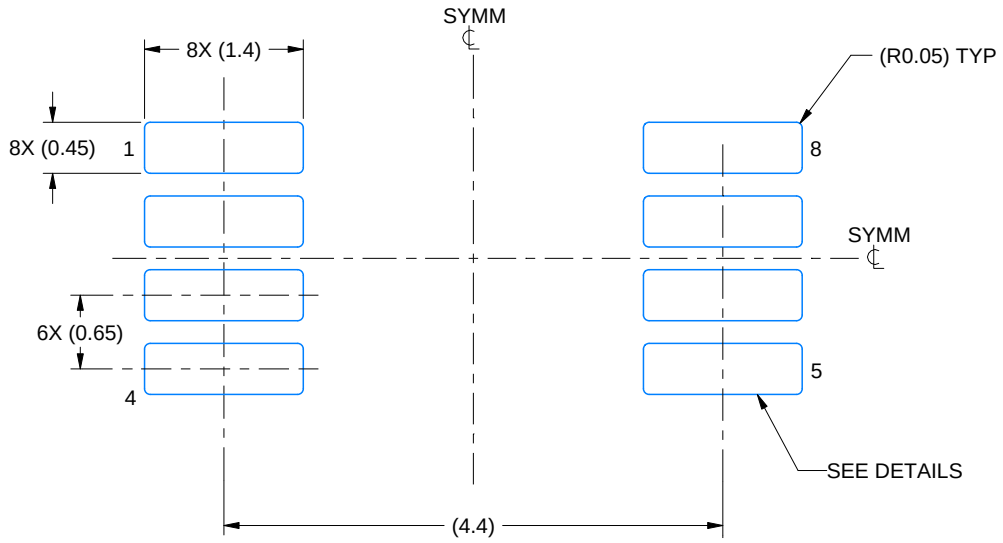
SMALL OUTLINE PACKAGE



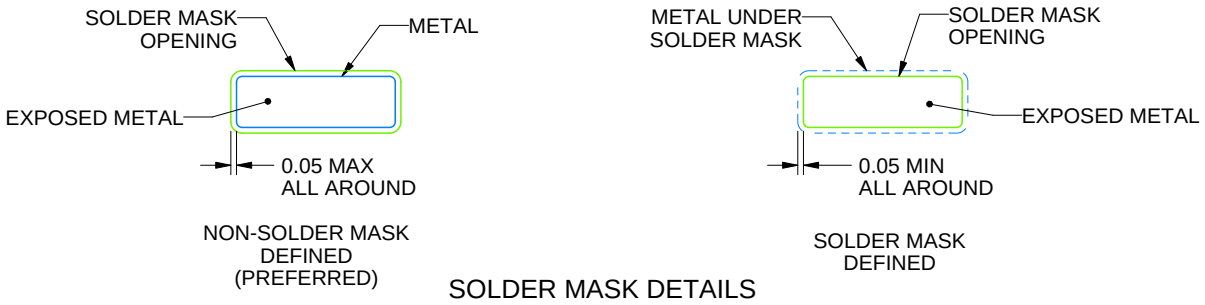
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

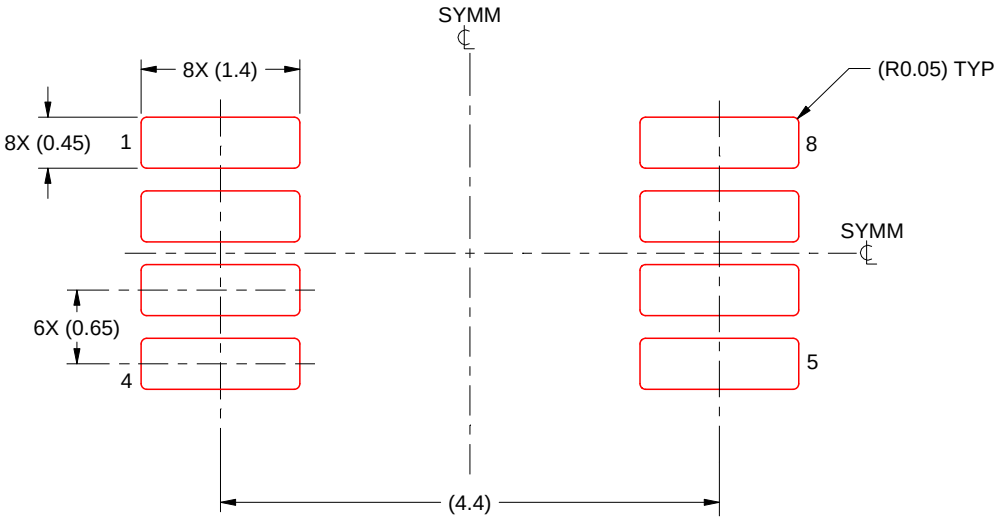


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

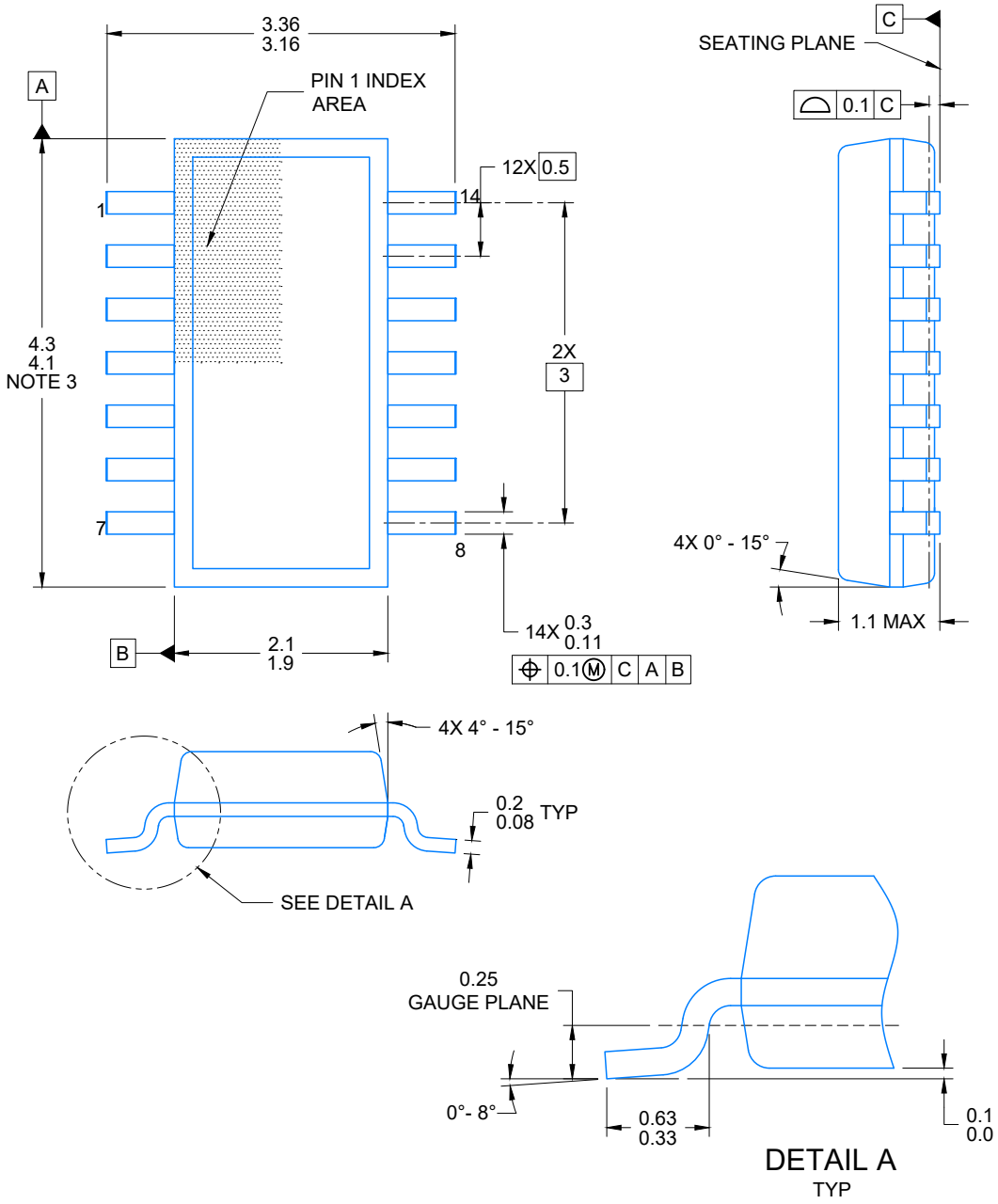
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DYY0014A

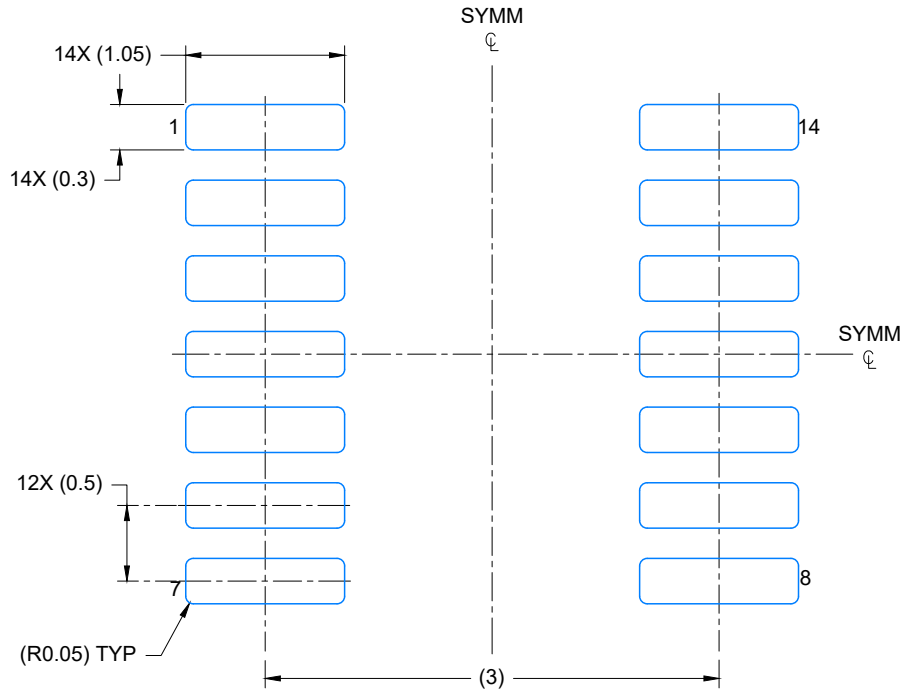
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

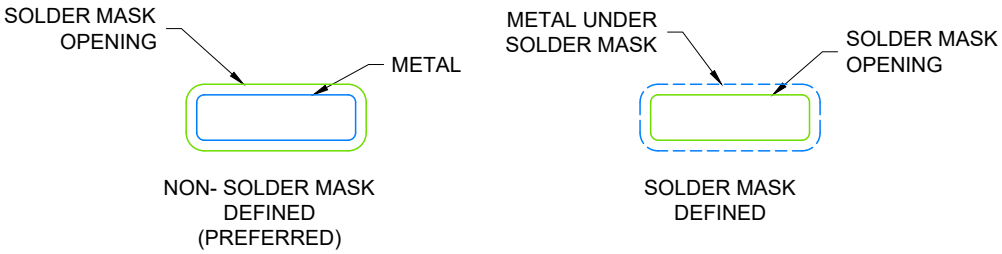


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

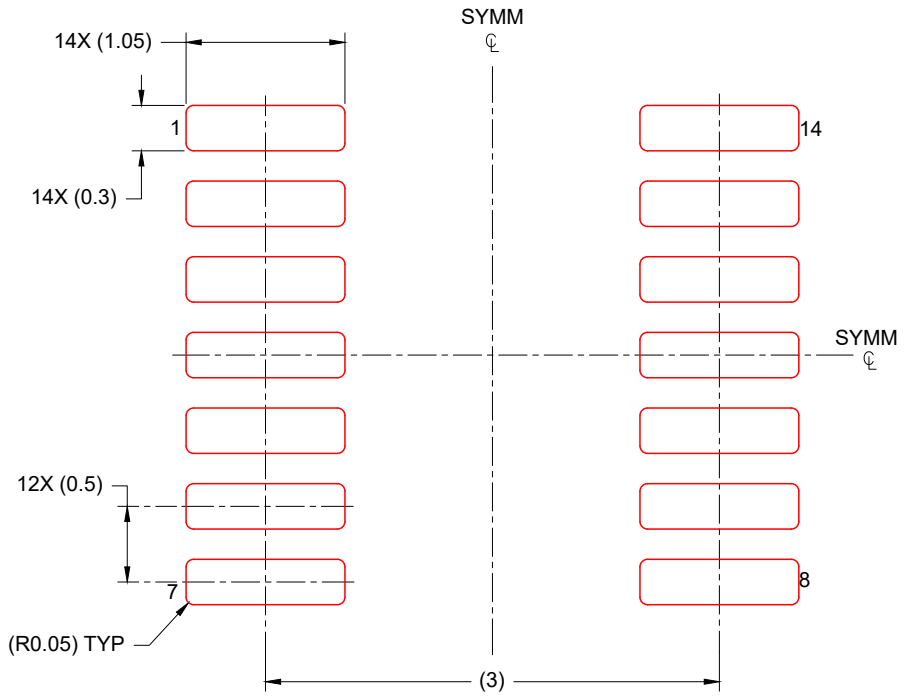


SOLDER MASK DETAILS

4224643/D 07/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

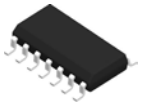


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224643/D 07/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

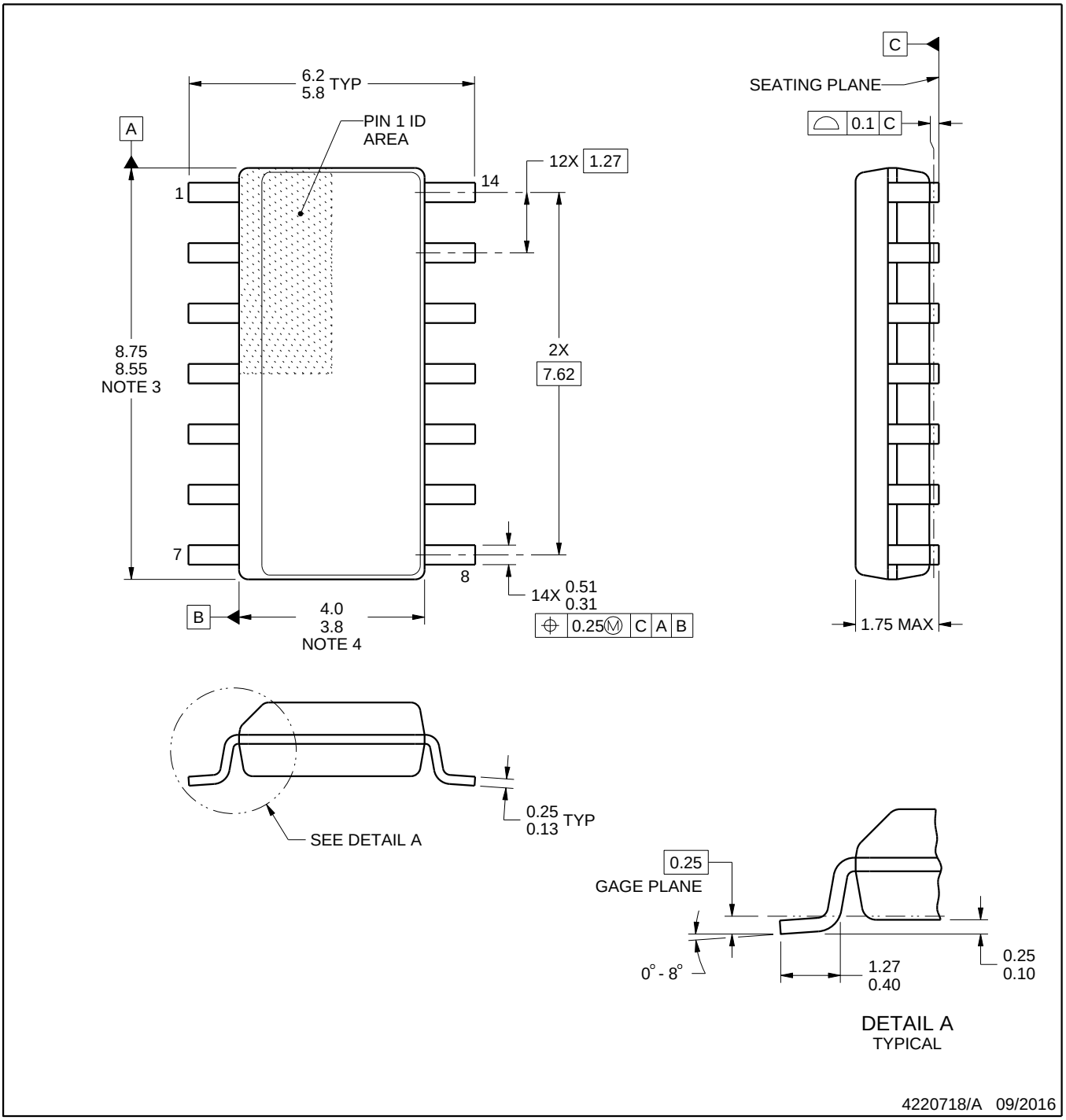


PACKAGE OUTLINE

D0014A

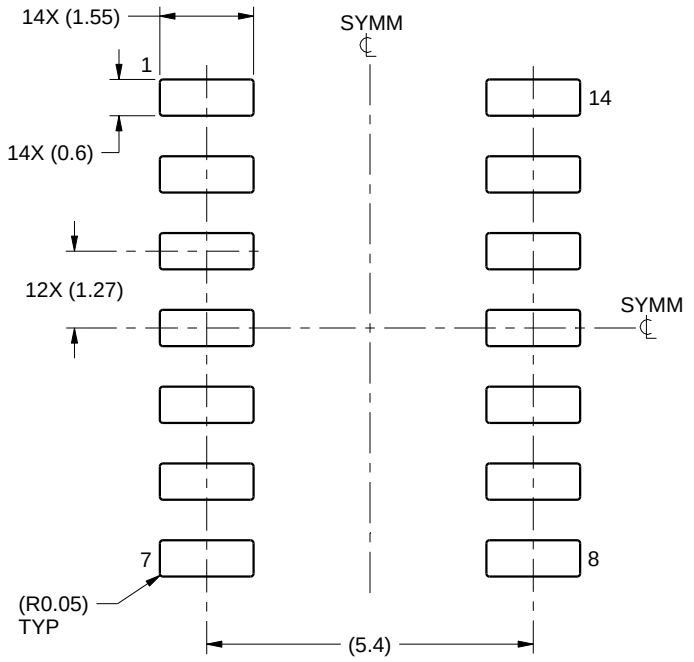
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

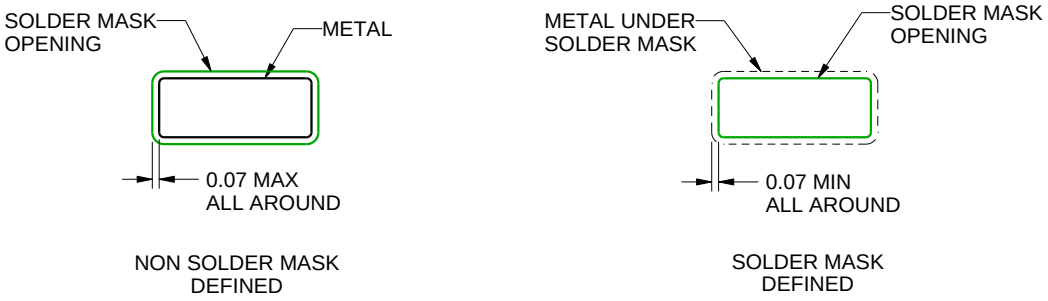


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

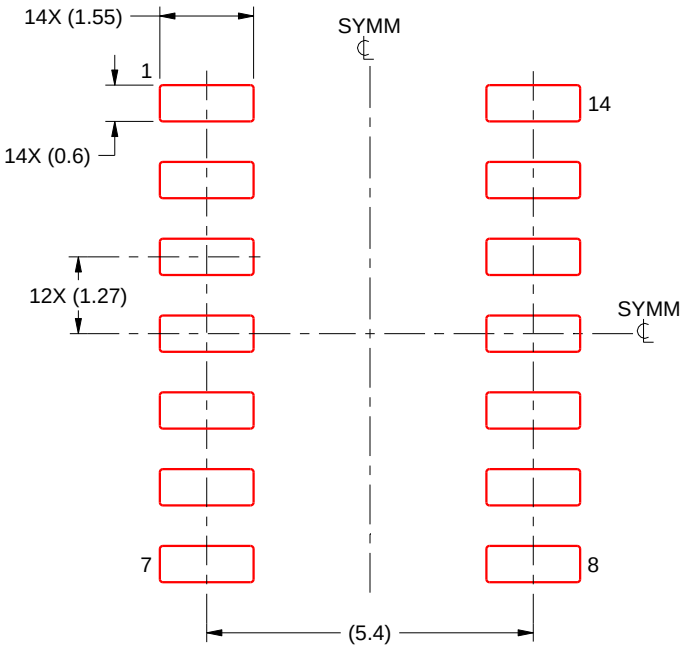
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

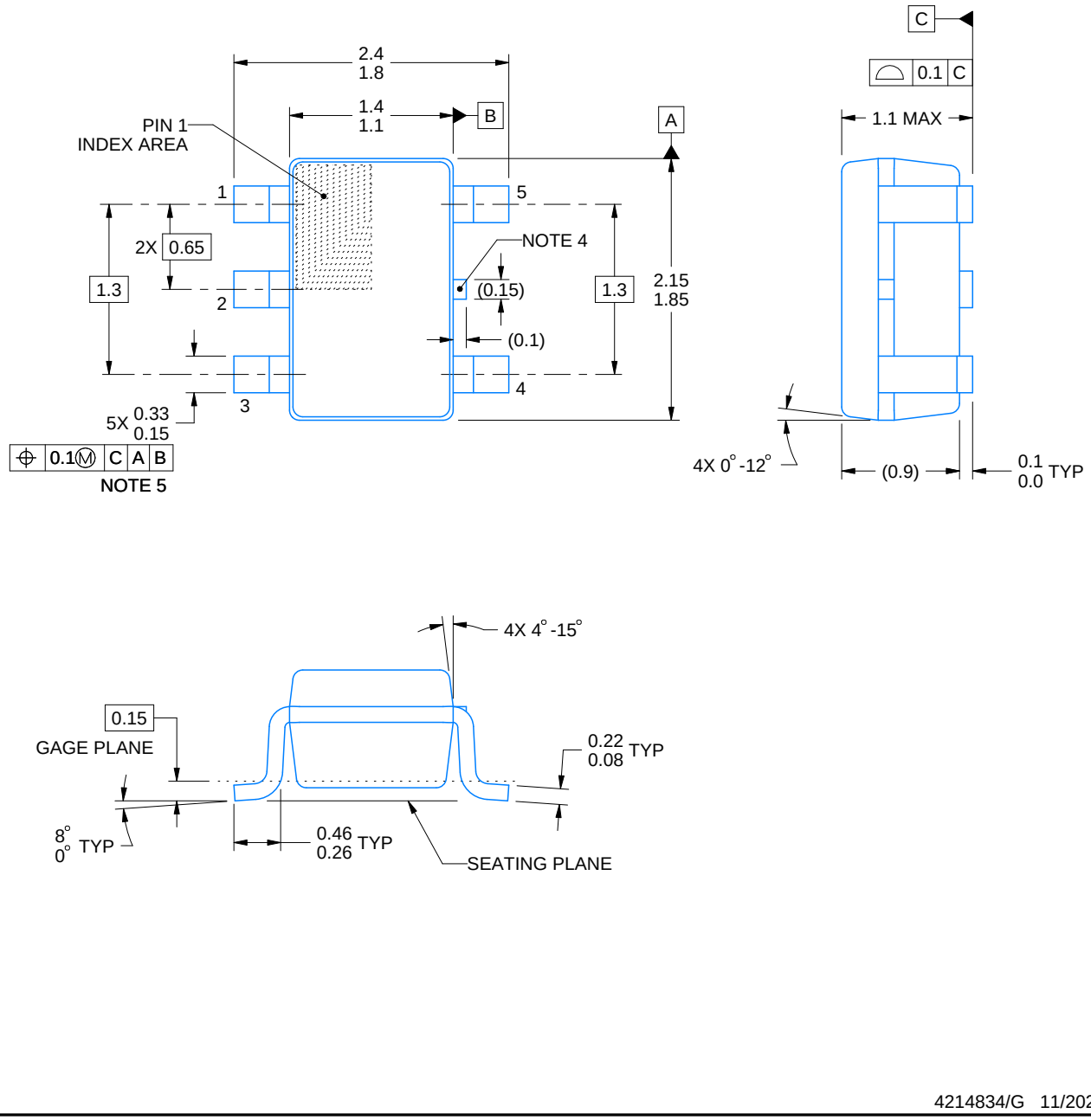
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

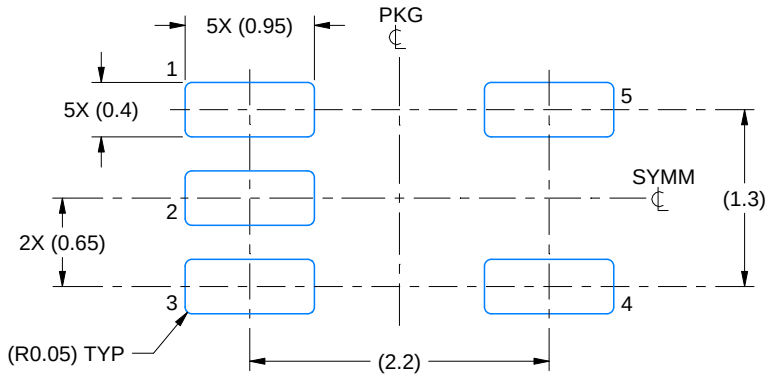
SMALL OUTLINE TRANSISTOR



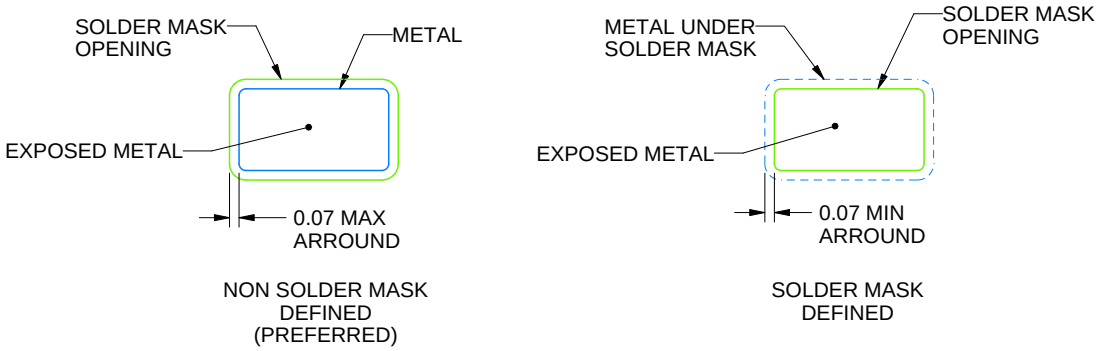
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

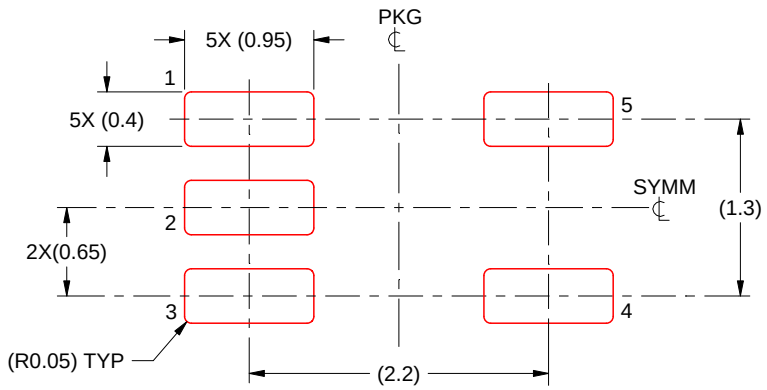


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

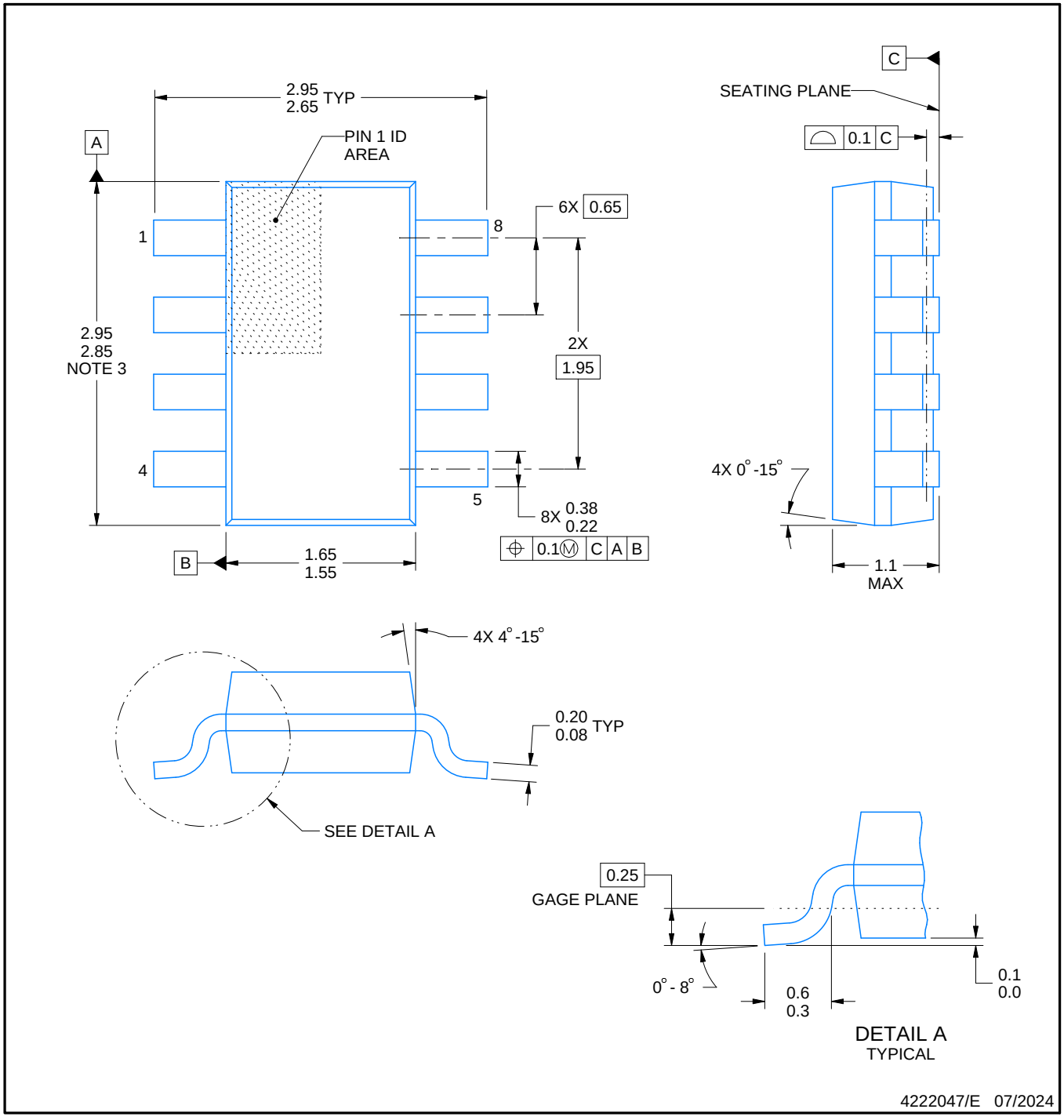
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DDF0008A

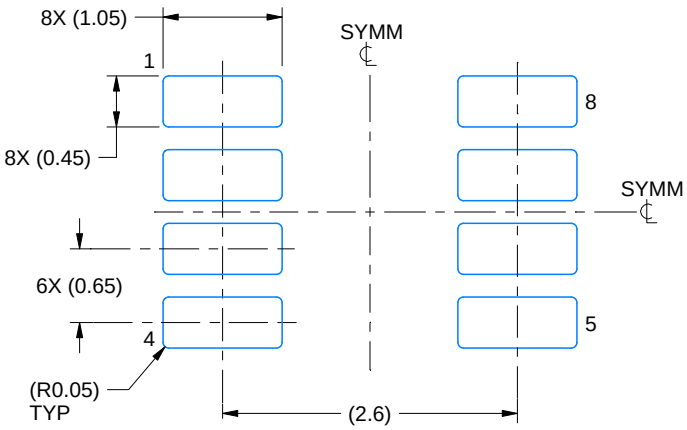
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

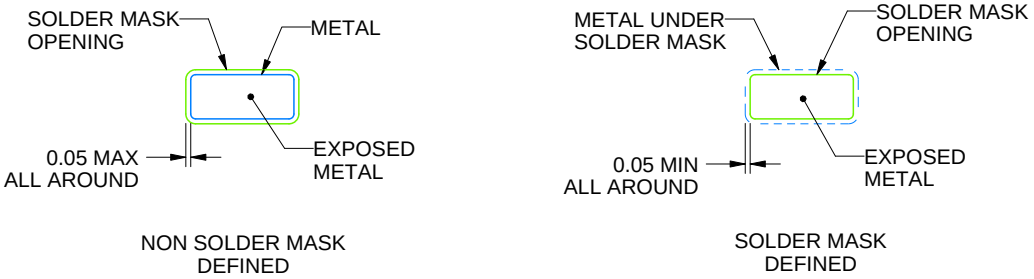


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4222047/E 07/2024

NOTES: (continued)

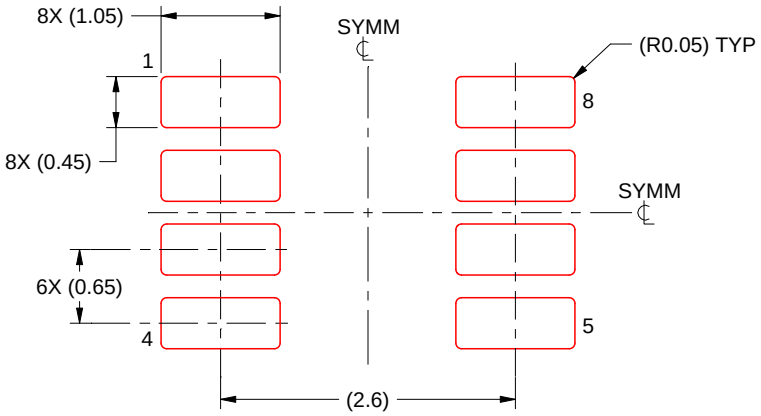
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

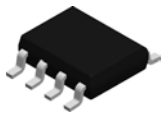


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

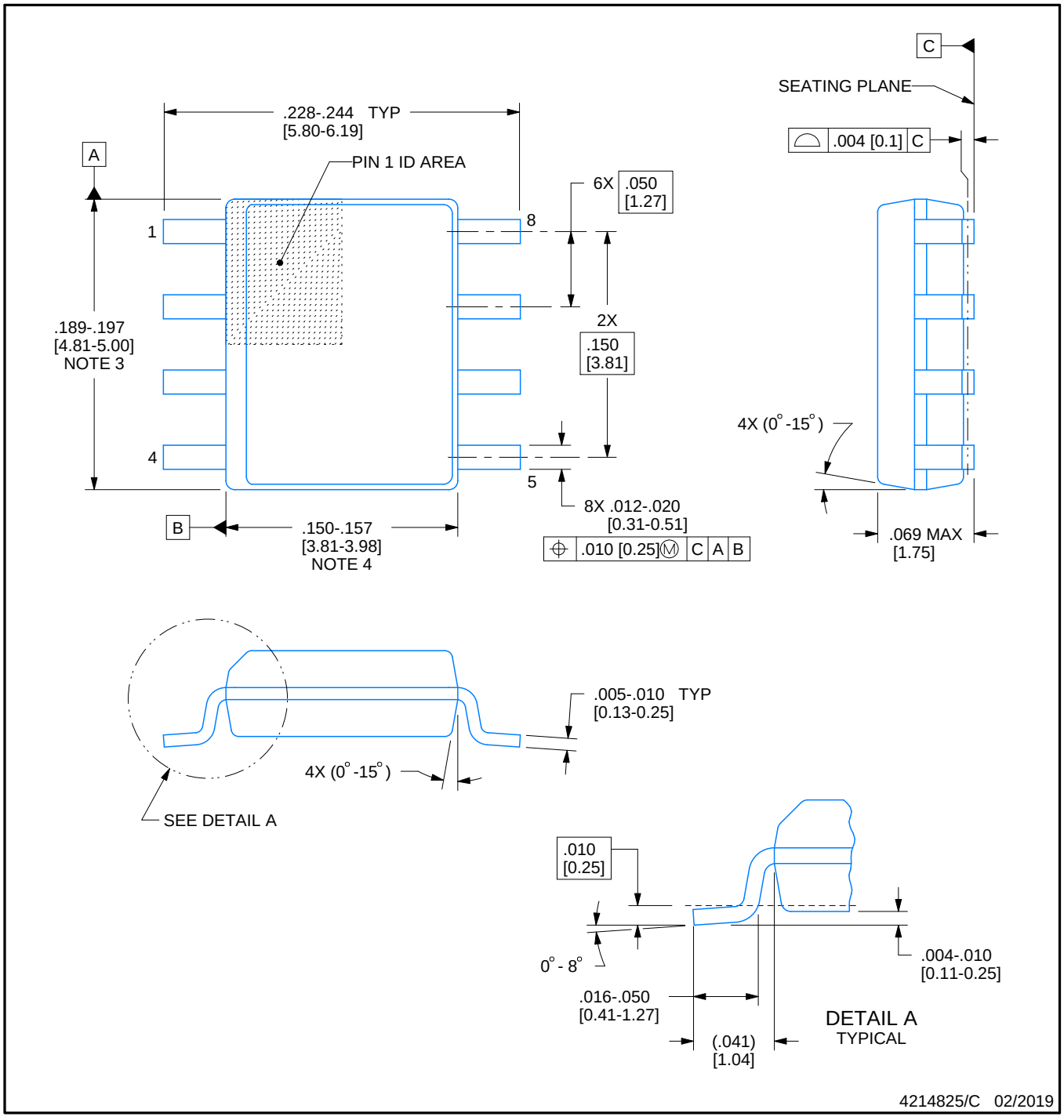


PACKAGE OUTLINE

D0008A

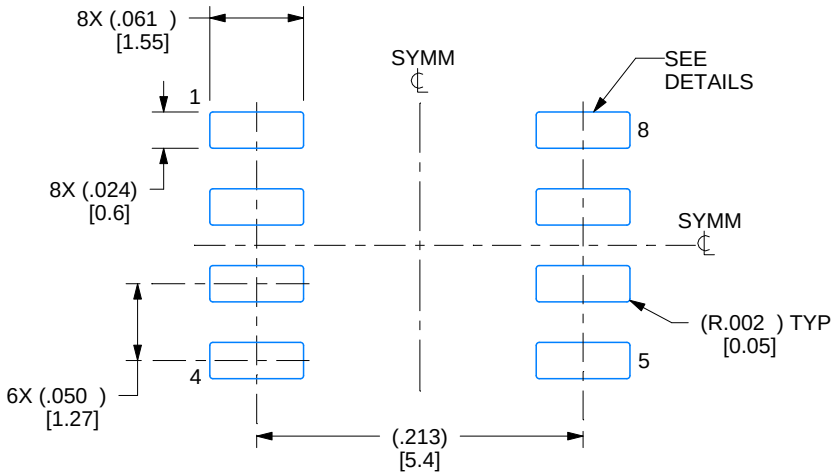
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

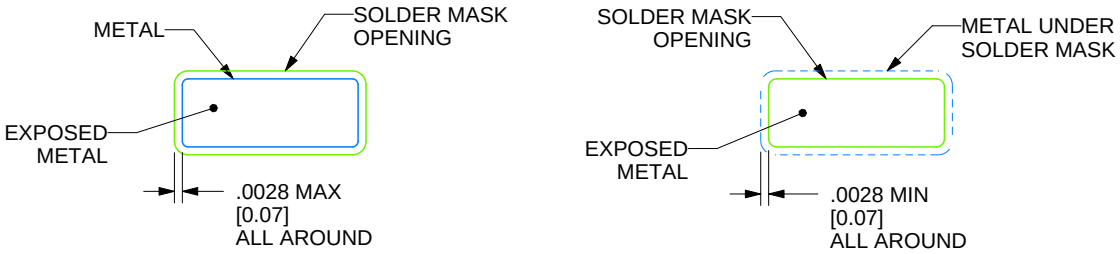


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

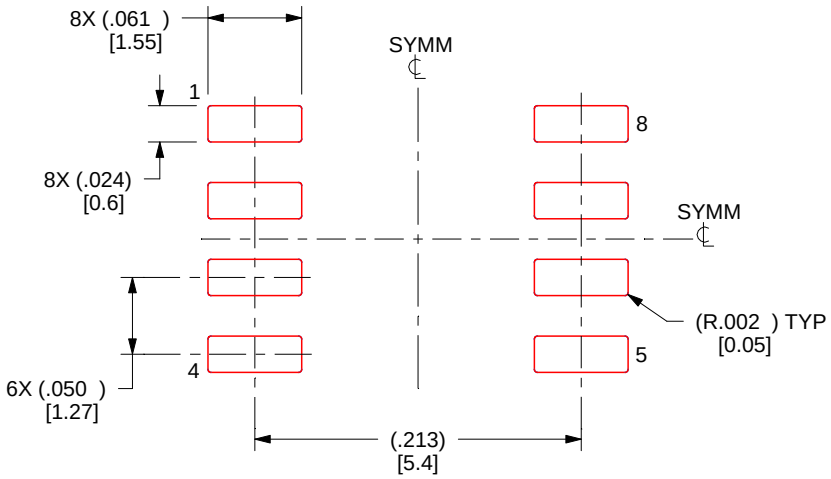
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

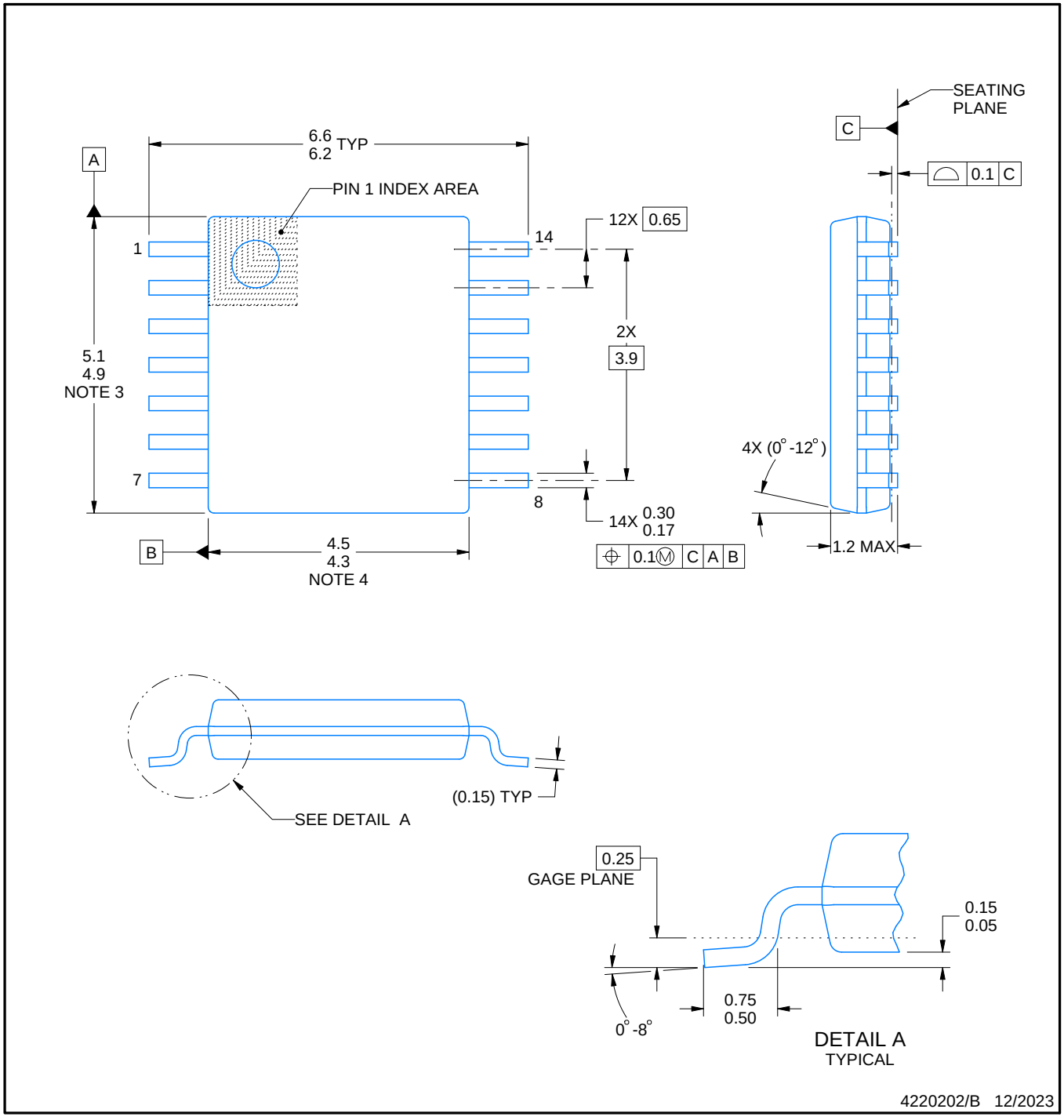
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

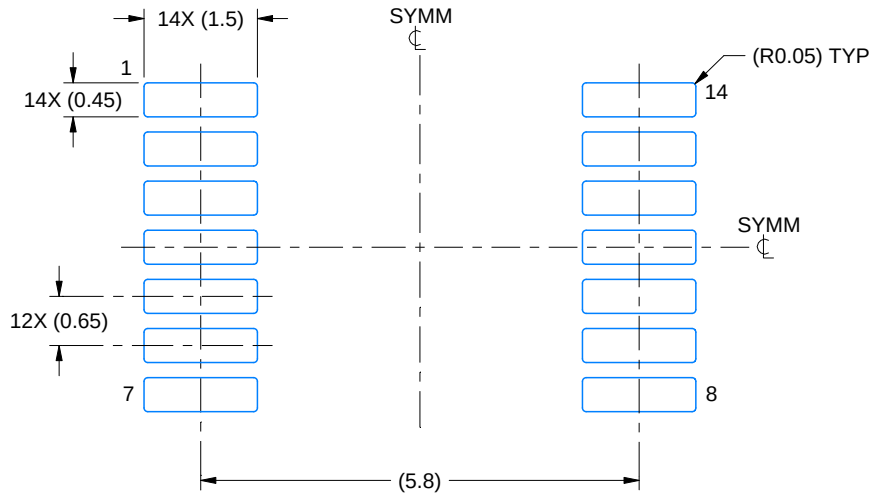
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

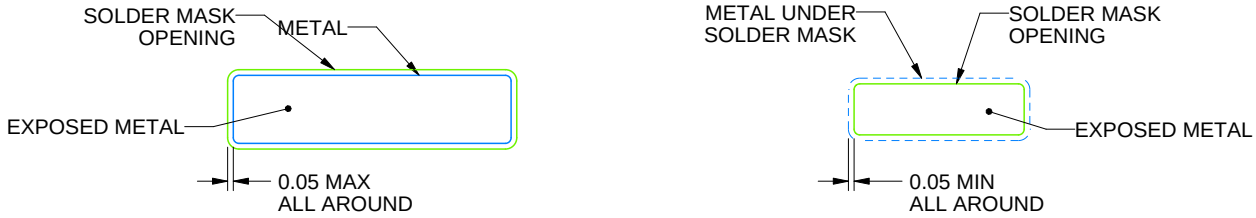


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

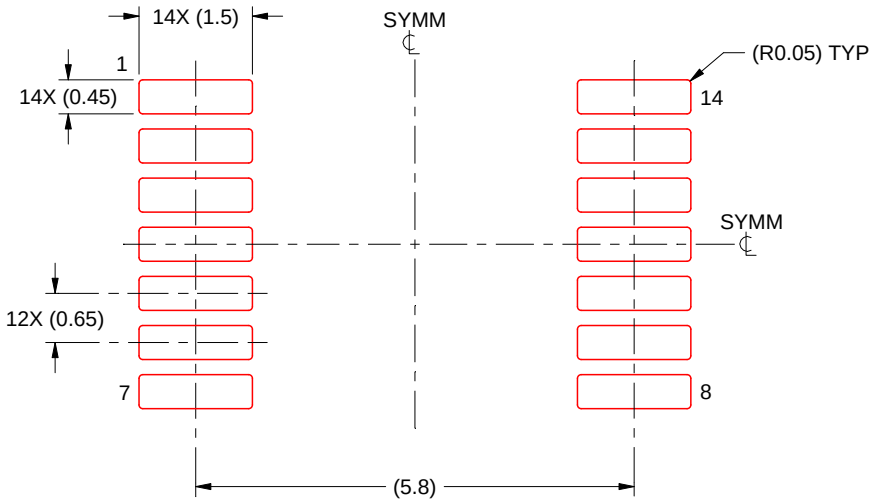


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

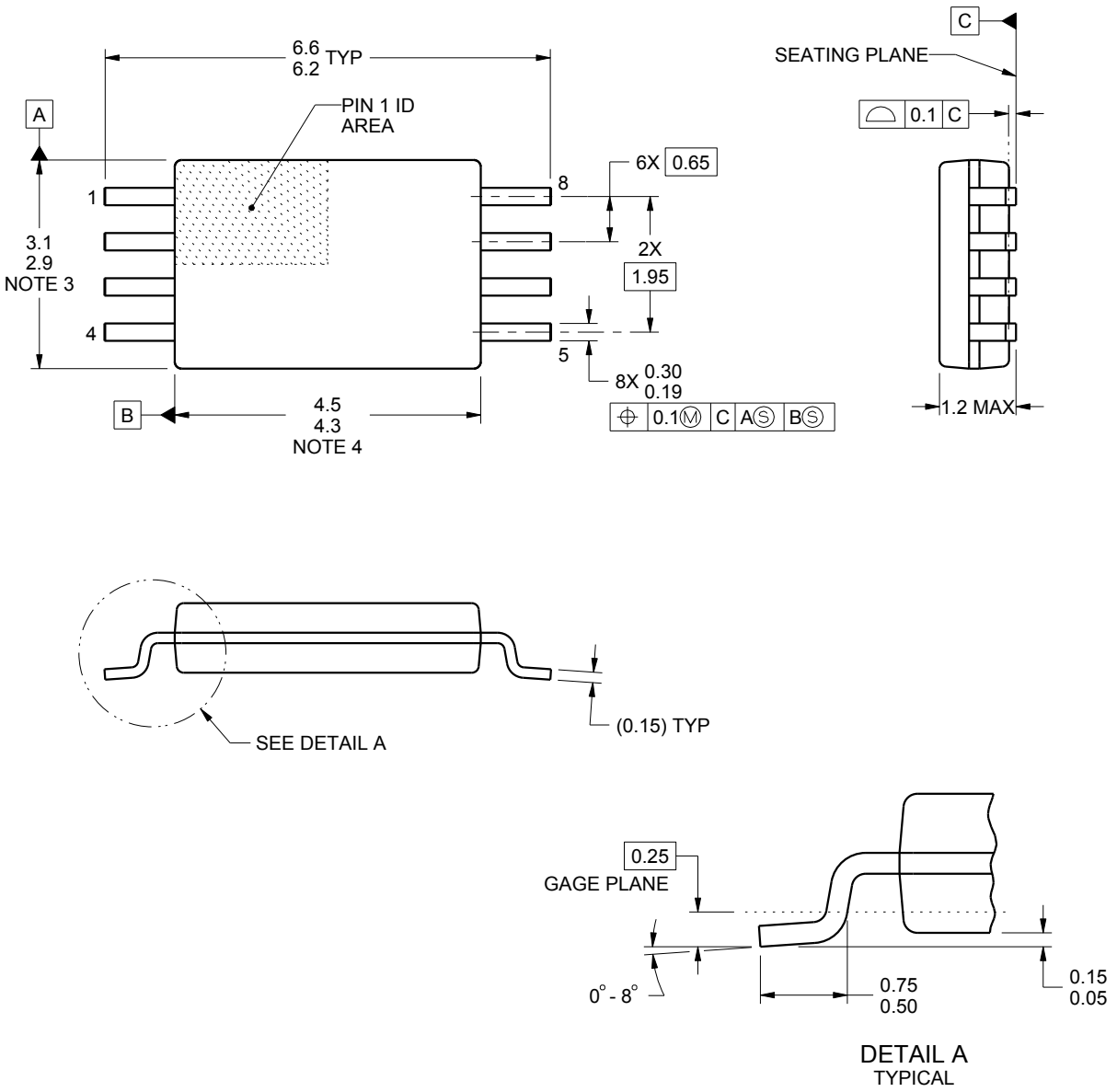
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0008A

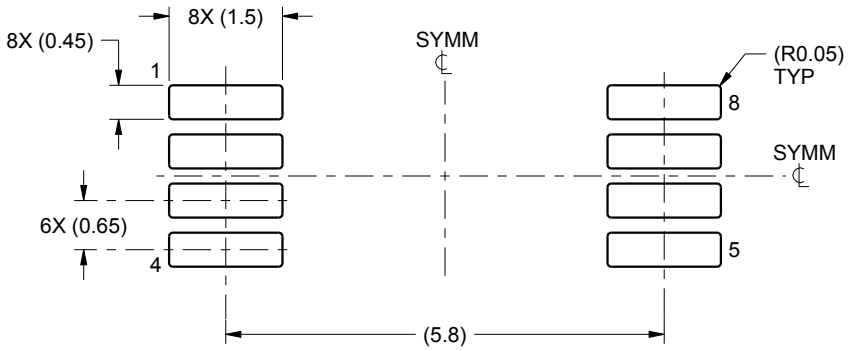
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

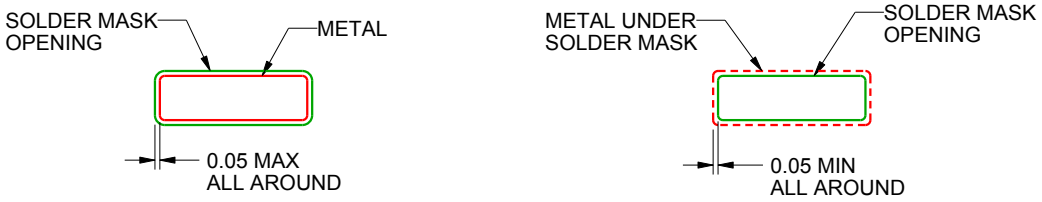


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

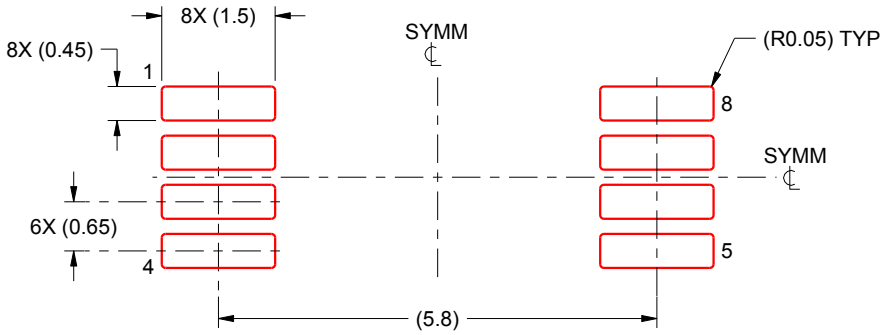


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月